Description

The 1338 is a serial real-time clock (RTC) device that consumes ultra-low power and provides a full binary-coded decimal (BCD) clock/calendar with 56 bytes of battery backed Non-Volatile Static RAM. The clock/calendar provides seconds, minutes, hours, day, date, month, and year information. The clock operates in either the 24-hour or 12-hour format with AM/PM indicator. The end of the month date is automatically adjusted for months with fewer than 31 days, including corrections for leap year. Access to the clock/calendar registers is provided by an I^2C interface capable of operating in fast I^2C mode. Built-in Power-sense circuitry detects power failures and automatically switches to the backup supply, maintaining time and date operation.

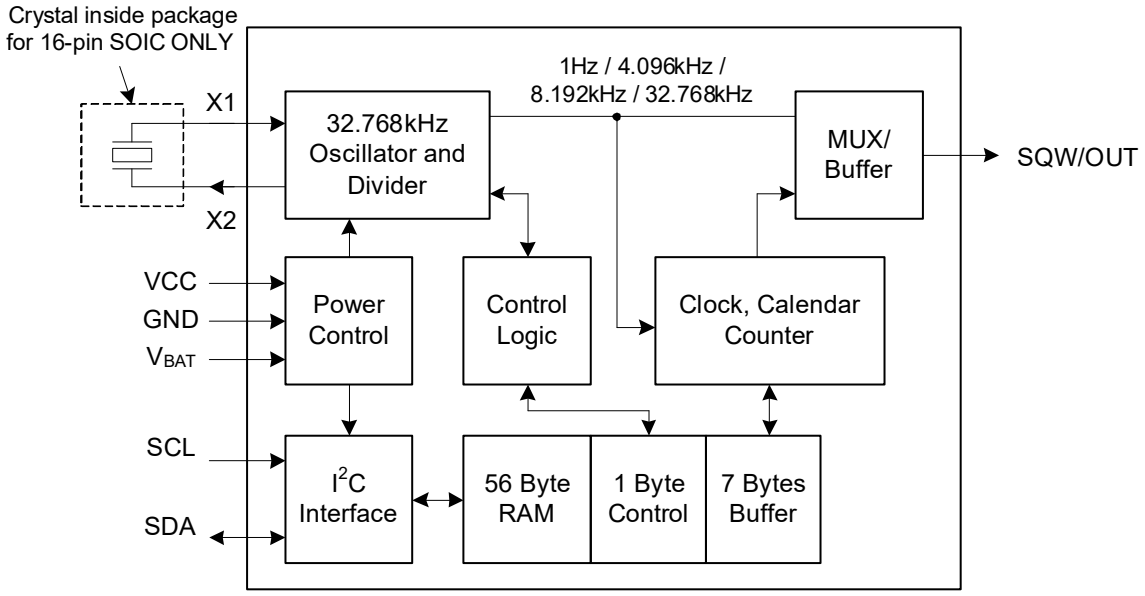
Features

- Real-Time Clock (RTC) counts seconds, minutes, hours, day, date, month, and year with leap-year compensation valid up to 2100
- 56-byte battery-backed Non-Volatile RAM for data storage
- Fast mode I^2C serial interface
- Automatic power-fail detect and switch circuitry
- Programmable square-wave output
- Packaged in 8-pin MSOP, 8-pin SOIC, or 16-pin SOIC (surface-mount package with an integrated crystal)
- Industrial temperature range (-40°C to +85°C)

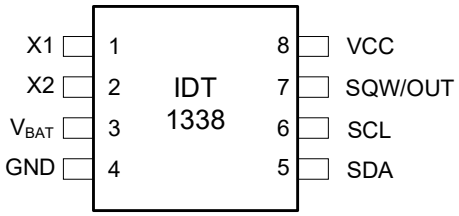
Typical Applications

- Telecom (Routers, Switches, Servers)
- Handheld (GPS, Point of Sale POS Terminals)
- Consumer Electronics (Set-Top Box, Digital Recording, Network Applications, Digital Photo Frames)
- Office (Fax/Printers, Copiers)
- Medical (Glucometer, Medicine Dispensers)
- Other (Thermostats, Vending Machines, Modems, Utility Meters)

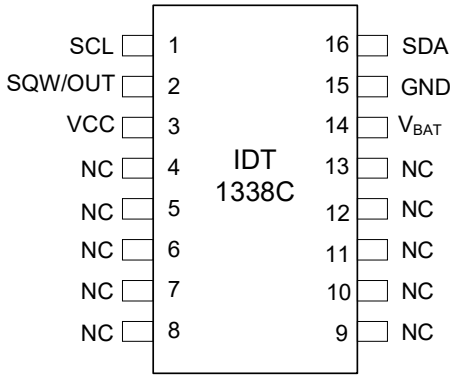
Block Diagram



Pin Assignment (8-pin MSOP/8-pin SOIC)



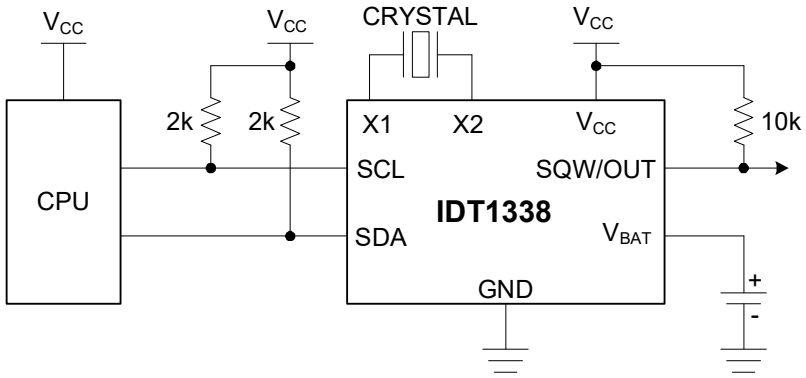
Pin Assignment (16-pin SOIC)



Pin Descriptions

Pin Number		Pin Name	Pin Description/Function
8MSOP, 8SOIC	16SOIC		
1	—	X1	Connections for standard 32.768kHz quartz crystal. The internal oscillator circuitry is designed for operation with a crystal having a specified load capacitance (CL) of 12.5pF. An external 32.768kHz oscillator can also drive the IDT1338. In this configuration, the X1 pin is connected to the external oscillator signal and the X2 pin is left floating.
2	—	X2	
3	14	V_{BAT}	Backup Supply Input for Lithium Coin Cell or Other Energy Source. Battery voltage must be held between the minimum and maximum limits for proper operation. Diodes placed in series between the backup source and the V_{BAT} pin may prevent proper operation. If a backup supply is not required, V_{BAT} must be connected to ground.
4	15	GND	Connect to ground.
5	16	SDA	Serial data input/output. SDA is the input/output pin for the I^2C serial interface. It is an open-drain output and requires an external pull-up resistor (2kOhm typical).
6	1	SCL	Serial clock input. SCL is used to synchronize data movement on the serial interface. It is an open-drain output and requires an external pull-up resistor (2kOhm typical)
7	2	SQW/OUT	Square-Wave/Output driver. When enabled and the SQWE bit set to 1, the SQW/OUT pin outputs one of four square-wave frequencies (1Hz, 4kHz, 8kHz, 32kHz). It is an open drain output and requires an external pull-up resistor (10K ohm typical). Operates when the device is powered with VCC or V_{BAT}.
8	3	V_{CC}	Device power supply. When voltage is applied within specified limits, the device is fully accessible by I^2C and data can be written and read.
—	4 – 13	NC	No connect. These pins are unused and must be connected to ground for proper operation.

Typical Operating Circuit



Detailed Description

The following sections discuss in detail the Oscillator block, Power Control block, Clock/Calendar Register Block and Serial I^2C block.

Oscillator Block

Selection of the right crystal, correct load capacitance and careful PCB layout are important for a stable crystal oscillator. Due to the optimization for the lowest possible current in the design for these oscillators, losses caused by parasitic currents can have a significant impact on the overall oscillator performance. Extra care needs to be taken to maintain a certain quality and cleanliness of the PCB.

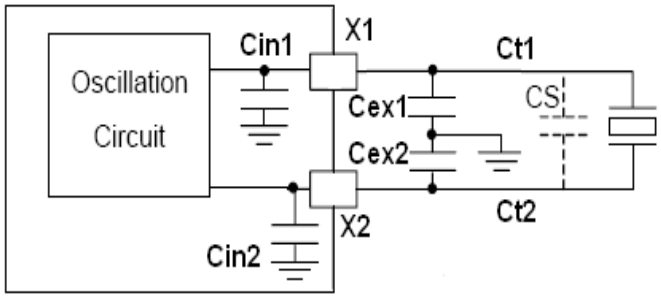
Crystal Selection

The key parameters when selecting a 32 kHz crystal to work with 1338 RTC are:

- Recommended Load Capacitance
- Crystal Effective Series Resistance (ESR)
- Frequency Tolerance

Effective Load Capacitance

Please see diagram below for effective load capacitance calculation. The effective load capacitance (CL) should match the recommended load capacitance of the crystal in order for the crystal to oscillate at its specified parallel resonant frequency with 0ppm frequency error.



$$CL = CS + ((CX1 * CX2) / (CX1+CX2))$$
$$CX1 = (Cin1+Cex1+Ct1)$$
$$CX2 = (Cin2+Cex2+Ct2)$$

In the above figure, X1 and X2 are the crystal pins of our device. Cin1 and Cin2 are the internal capacitors which include the X1 and X2 pin capacitance. Cex1 and Cex2 are the external capacitors that are needed to tune the crystal frequency. Ct1 and Ct2 are the PCB trace capacitances between the crystal and the device pins. CS is the shunt capacitance of the crystal (as specified in the crystal manufacturer's datasheet or measured using a network analyzer). Cex1 and Cex2 are not needed if the crystal circuit uses the recommended crystal with specified load capacitance (CL) of 12.5pF.

Note: 1338CSRI integrates a standard 32.768 kHz crystal in the package and contributes an additional frequency error of 10ppm at nominal V_{CC} (+3.3 V) and T_A=+25°C.

ESR (Effective Series Resistance)

Choose the crystal with lower ESR. A low ESR helps the crystal to start up and stabilize to the correct output frequency faster compared to high ESR crystals.

Frequency Tolerance

The frequency tolerance for 32kHz crystals should be specified at nominal temperature (+25°C) on the crystal manufacturer datasheet. The crystals used with 1338 typically have a frequency tolerance of ±20ppm at +25°C.

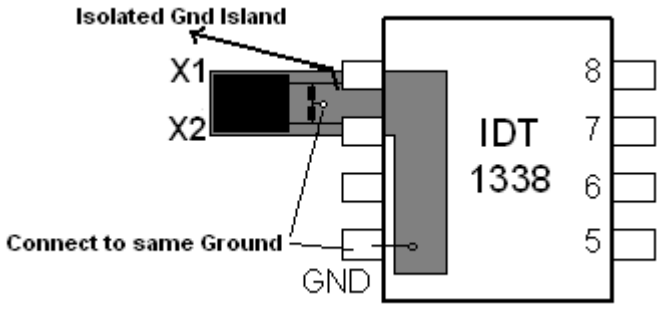
Specifications for a typical 32kHz crystal used with our device are shown in the table below.

Parameter	Symbol	Min	Typ	Max	Units
Nominal Freq.	f_O		32.768		kHz
Series Resistance	ESR			110	kΩ
Load Capacitance	C_L		12.5		pF

PCB Design Consideration

- Signal traces between the device pins and the crystal must be kept as short as possible. This minimizes parasitic capacitance and sensitivity to crosstalk and EMI. Note that the trace capacitances play a role in the effective crystal load capacitance calculation.
- Data lines and frequently switching signal lines should be routed as far away from the crystal connections as possible. Crosstalk from these signals may disturb the oscillator signal.
- Reduce the parasitic capacitance between X1 and X2 signals by routing them as far apart as possible.
- The oscillation loop current flows between the crystal and the load capacitors. This signal path (crystal to CL1 to CL2 to crystal) should be kept as short as possible and ideally be symmetric. The ground connections for both capacitors should be as close together as possible. Never route the ground connection between the capacitors all around the crystal, because this long ground trace is sensitive to crosstalk and EMI.
- To reduce the radiation / coupling from oscillator circuit, an isolated ground island on the GND layer could be made. This ground island can be connected at one point to the GND layer. This helps to keep noise generated by the oscillator circuit locally on this separated island. The ground connections for the load capacitors and the oscillator should be connected to this island.

PCB Layout



PCB Assembly, Soldering and Cleaning

Board-assembly production process and assembly quality can affect the performance of the 32kHz oscillator. Depending on the flux material used, the soldering process can leave critical residues on the PCB surface. High humidity and fast temperature cycles that cause humidity condensation on the printed circuit board can create process residuals. These process residuals cause the insulation of the sensitive oscillator signal lines towards each other and neighboring signals on the PCB to decrease. High humidity can lead to moisture condensation on the surface of the PCB and, together with process residuals, reduce the surface resistivity of the board. Flux residuals on the board can cause leakage current paths, especially in humid environments. Thorough PCB cleaning is therefore highly recommended in order to achieve maximum performance by removing flux residuals from the board after assembly. In general, reduction of losses in the oscillator circuit leads to better safety margin and reliability.

Power Control

A precise, temperature-compensated voltage reference and a comparator circuit provides power-control function that monitors the V_{CC} level. The device is fully accessible and data can be written and read when V_{CC} is greater than V_{PF}. However, when V_{CC} falls below V_{PF}, the internal clock registers are blocked from any access. If V_{PF} is less than V_{BAT}, the device power is switched from V_{CC} to V_{BAT} when V_{CC} drops below V_{PF}. If V_{PF} is greater than V_{BAT}, the device power is switched from V_{CC} to V_{BAT} when V_{CC} drops below V_{BAT}. The registers are maintained from the V_{BAT} source until V_{CC} is returned to nominal levels (Table 1). After V_{CC} returns above V_{PF}, read and write access is allowed after t_{REC} (see the "Power-Up/Down Timing" diagram).

Table 1. Power Control

Supply Condition	Read/Write Access	Powered By
$V_{CC} < V_{PF}$, $V_{CC} < V_{BAT}$	No	V_{BAT}
$V_{CC} < V_{PF}$, $V_{CC} > V_{BAT}$	No	V_{CC}
$V_{CC} > V_{PF}$, $V_{CC} < V_{BAT}$	Yes	V_{CC}
$V_{CC} > V_{PF}$, $V_{CC} > V_{BAT}$	Yes	V_{CC}

Power-up/down Timing

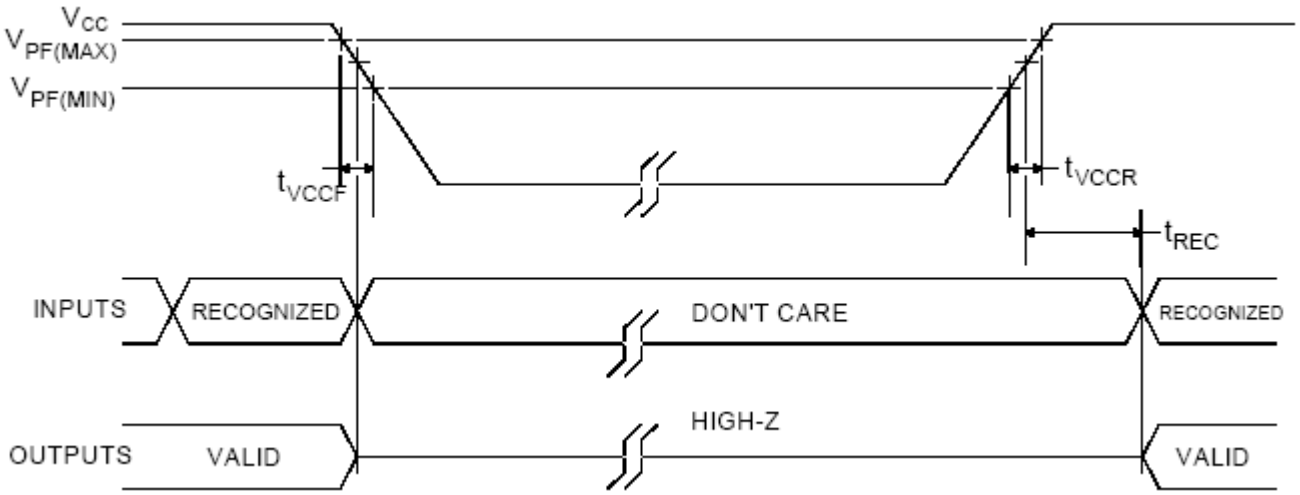


Table 2. Power-up/down Characteristics

Ambient Temperature -40 to +85°C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Recovery at Power-up	t_{REC}	(Note 1)			2	ms
V_{CC} Fall Time; $V_{PF(MAX)}$ to $V_{PF(MIN)}$	t_{VCCF}	1338-18 (Note 2)	3			ms
		1338-31 (Note 2)	3			ms
V_{CC} Rise Time; $V_{PF(MIN)}$ to $V_{PF(MAX)}$	t_{VCCR}		0			µs

Note 1: This delay applies only if the oscillator is running. If the oscillator is disabled or stopped, no power-up delay occurs.

Note 2: Measured at typical VBAT level.

RTC and RAM Address Map

The address map for the RTC and RAM registers shown in Table 3. The RTC registers and control register are located in address locations 00H to 07H The RAM registers are located in address locations 08H to 3FH. During a multibyte access, when the register pointer reaches 3FH (the end of RAM space) it wraps around to location 00H (the beginning of the clock space). On an I^2C START, STOP, or register pointer incrementing to location 00H, the current time and date is transferred to a second set of registers. The time and date in the secondary registers are read in a multibyte data transfer, while the clock continues to run. This eliminates the need to re-read the registers in case of an update of the main registers during a read.

Table 3. RTC and RAM Address Map

Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Function	Range
00H	CH	10 seconds			Seconds				Seconds	00 - 59
01H	0	10 minutes			Minutes				Minutes	00 - 59
02H	0	12/$\overline{24}$	$\overline{AM}$/PM 10 hour	10 hour	Hour				Hours	1 - 12 + AM/PM 00 - 23
03H	0	0	0	0	0	Day			Day	1 - 7
04H	0	0	10 date		Date				Date	01 - 31
05H	0	0	0	10 month	Month				Month	01 - 12
06H	10 year				Year				Year	00 - 99
07H	OUT	0	OSF	SQWE	0	0	RS1	RS0	Control	
08H - 3FH									RAM 56 x 8	00H - FFH

Note: Bits listed as “0” should always be written and read as 0.

Clock and Calendar

Table 3 shows the address map of the RTC registers. The time and date information is obtained by reading the appropriate register bytes. The time and calendar are set or initialized by writing the appropriate register bytes. The contents of the time and calendar registers are in the BCD format. Bit 7 of Register 0 is the clock halt (CH) bit. When this bit is set to 1, the oscillator is disabled. When cleared to 0, the oscillator is enabled. The clock can be halted whenever the timekeeping functions are not required, which decreases V_{BAT} current.

The day-of-week register increments at midnight. Values that correspond to the day of week are user-defined but must be sequential (i.e., if 1 equals Sunday, then 2 equals Monday, and so on). Illogical time and date entries result in undefined operation.

When reading or writing the time and date registers, secondary (user) buffers are used to prevent errors when the internal registers update. When reading the time and date registers, the user buffers are synchronized to the internal registers on any start or stop, and when the address pointer rolls over to zero.

The countdown chain is reset whenever the seconds register is written. Write transfers occurs on the acknowledge pulse from the device. To avoid rollover issues, once the countdown chain is reset, the remaining time and date registers must be written within one second. If enabled, the 1Hz square-wave output transitions high 500ms after the seconds data transfer, provided the oscillator is already running.

Note that the initial power-on state of all registers, unless otherwise specified, is not defined. Therefore, it is important to enable the oscillator (CH = 0) during initial configuration.

The IDT1338 runs in either 12-hour or 24-hour mode. Bit 6 of the hours register is defined as the 12-hour or 24-hour mode-select bit. When high, the 12-hour mode is selected. In the 12-hour mode, bit 5 is the $\overline{AM}$/PM bit, with logic high being PM. In the 24-hour mode, bit 5 is the second 10-hour bit (20–23 hours). If the 12/$\overline{24}$-hour mode select is changed, the hours register must be re-initialized to the new format.

On an I^2C START, the current time is transferred to a second set of registers. The time information is read from these secondary registers, while the clock continues to run. This eliminates the need to re-read the registers in case of an update of the main registers during a read.

Table 4. Control Register (07H)

The control register controls the operation of the SQW/OUT pin and provides oscillator status.

Bit #	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	OUT	0	OSF	SQWE	0	0	RS1	RS0
POR	1	0	1	1	0	0	1	1

Bit 7: Output Control (OUT). Controls the output level of the SQW/OUT pin when the square-wave output is disabled. If SQWE = 0, the logic level on the SQW/OUT pin is 1 if OUT = 1; it is 0 if OUT = 0.

Bit 5: Oscillator Stop Flag (OSF). A logic 1 in this bit indicates that the oscillator has stopped or was stopped for some time period and can be used to judge the validity of the clock and calendar data. This bit is edge triggered, and is set to logic 1 when the internal circuitry senses the oscillator has transitioned from a normal run state to a STOP condition. The following are examples of conditions that may cause the OSF bit to be set:

1) The first time power is applied.

2) The voltage present on VCC and VBAT are insufficient to support oscillation.

3) The CH bit is set to 1, disabling the oscillator.

4) External influences on the crystal (i.e., noise, leakage, etc.).

This bit remains at logic 1 until written to logic 0. This bit can only be written to logic 0. Attempting to write OSF to logic 1 leaves the value unchanged.

Bit 4: Square-Wave Enable (SQWE). When set to logic 1, this bit enables the oscillator output to operate with either VCC or V_{BAT} applied. The frequency of the square-wave output depends upon the value of the RS0 and RS1 bits.

Bits 1 and 0: Rate Select (RS1 and RS0). These bits control the frequency of the square-wave output when the square-wave output has been enabled. The table below lists the square-wave frequencies that can be selected with the RS bits.

Table 5. Square Wave Output

OUT	RS1	RS0	SQW Output	SQWE
X	0	0	1Hz	1
X	0	1	4.096kHz	1
X	1	0	8.192kHz	1
X	1	1	32.768kHz	1
0	X	X	0	0
1	X	X	1	0

I²C Serial Data Bus

The 1338 supports the I²C bus protocol. A device that sends data onto the bus is defined as a transmitter and a device receiving data as a receiver. The device that controls the message is called a master. The devices that are controlled by the master are referred to as slaves. The bus must be controlled by a master device that generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions. The 1338 operates as a slave on the I²C bus. Within the bus specifications, a standard mode (100kHz maximum clock rate) and a fast mode (400kHz maximum clock rate) are defined. The 1338 works in both modes. Connections to the bus are made via the open-drain I/O lines SDA and SCL.

The following bus protocol has been defined (see the "Data Transfer on I²C Serial Bus" figure):

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH are interpreted as control signals.

Accordingly, the following bus conditions have been defined:

Bus not busy: Both data and clock lines remain HIGH.

Start data transfer: A change in the state of the data line, from HIGH to LOW, while the clock is HIGH, defines a START condition.

Stop data transfer: A change in the state of the data line, from LOW to HIGH, while the clock line is HIGH, defines the STOP condition.

Data valid: The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal. The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

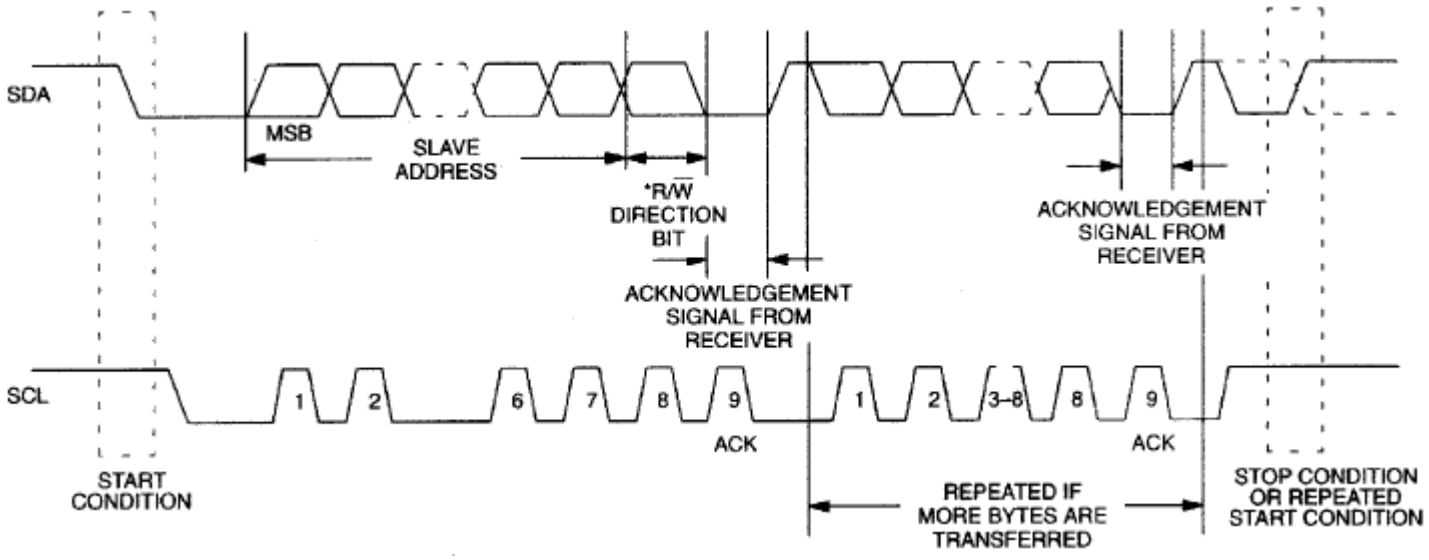
Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of data bytes transferred between START and STOP conditions is not limited, and is determined by the master device. The information is transferred byte-wise and each receiver acknowledges with a ninth bit.

Acknowledge: Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse that is associated with this acknowledge bit.

A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition.

Timeout: Timeout is where a slave device resets its interface whenever Clock goes low for longer than the timeout, which is typically 35msec. This added logic deals with slave errors and recovering from those errors. When timeout occurs, the slave interface should re-initialize itself and be ready to receive a communication from the master, but it will expect a Start prior to any new communication.

Data Transfer on I²C Serial Bus



Depending upon the state of the R/$\overline{W}$ bit, two types of data transfer are possible:

1) **Data transfer from a master transmitter to a slave receiver.** The first byte transmitted by the master is the slave address. Next follows a number of data bytes. The slave returns an acknowledge bit after each received byte. Data is transferred with the most significant bit (MSB) first.

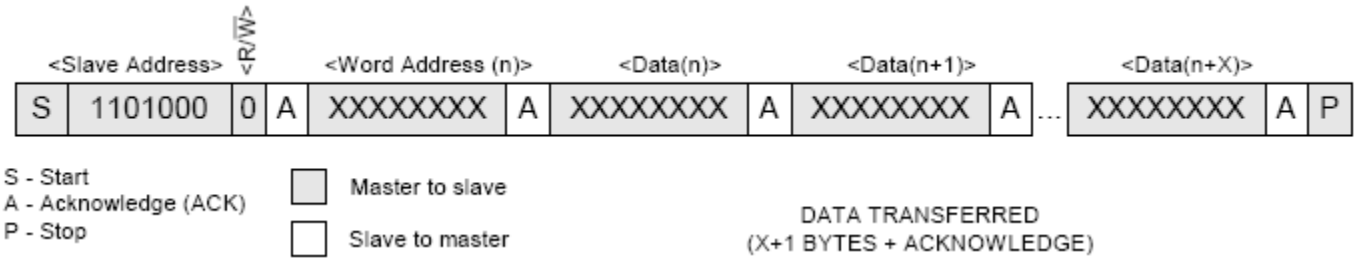
2) **Data transfer from a slave transmitter to a master receiver.** The first byte (the slave address) is transmitted by the master. The slave then returns an acknowledge bit. This is followed by the slave transmitting a number of data bytes. The master returns an acknowledge bit after all received bytes other than the last byte. At the end of the last received byte, a “not acknowledge” is returned. The master device generates all of the serial clock pulses and the START and STOP conditions. A transfer is ended with a STOP condition or with a repeated START condition. Since a repeated START condition is also the beginning of the next serial transfer, the bus is not released. Data is transferred with the most significant bit (MSB) first.

The 1338 can operate in the following two modes:

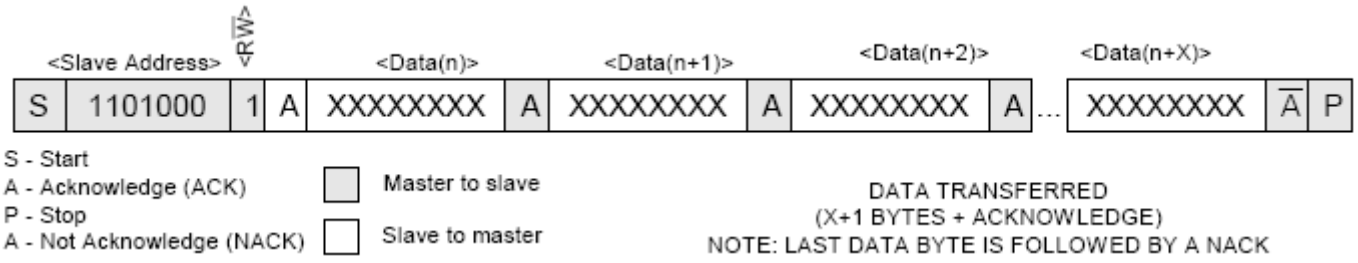
1) **Slave Receiver Mode (Write Mode):** Serial data and clock are received through SDA and SCL. After each byte is received an acknowledge bit is transmitted. START and STOP conditions are recognized as the beginning and end of a serial transfer. Address recognition is performed by hardware after reception of the slave address and direction bit (see the “Data Write–Slave Receiver Mode” figure). The slave address byte is the first byte received after the START condition is generated by the master. The slave address byte contains the 7-bit 1338 address, which is 1101000, followed by the direction bit (R/$\overline{W}$), which is 0 for a write. After receiving and decoding the slave address byte the slave outputs an acknowledge on the SDA line. After the 1338 acknowledges the slave address + write bit, the master transmits a register address to the 1338. This sets the register pointer on the 1338, with the 1338 acknowledging the transfer. The master may then transmit zero or more bytes of data, with the 1338 acknowledging each byte received. The address pointer increments after each data byte is transferred. The master generates a STOP condition to terminate the data write.

2) **Slave Transmitter Mode (Read Mode):** The first byte is received and handled as in the slave receiver mode. However, in this mode, the direction bit indicates that the transfer direction is reversed. Serial data is transmitted on SDA by the 1338 while the serial clock is input on SCL. START and STOP conditions are recognized as the beginning and end of a serial transfer (see the “Data Read–Slave Transmitter Mode” figure). The slave address byte is the first byte received after the START condition is generated by the master. The slave address byte contains the 7-bit 1338 address, which is 1101000, followed by the direction bit (R/$\overline{W}$), which is 1 for a read. After receiving and decoding the slave address byte the slave outputs an acknowledge on the SDA line. The 1338 then begins to transmit data starting with the register address pointed to by the register pointer. If the register pointer is not written to before the initiation of a read mode the first address that is read is the last one stored in the register pointer. The address pointer is incremented after each byte is transferred. The 1338 must receive a “not acknowledge” to end a read.

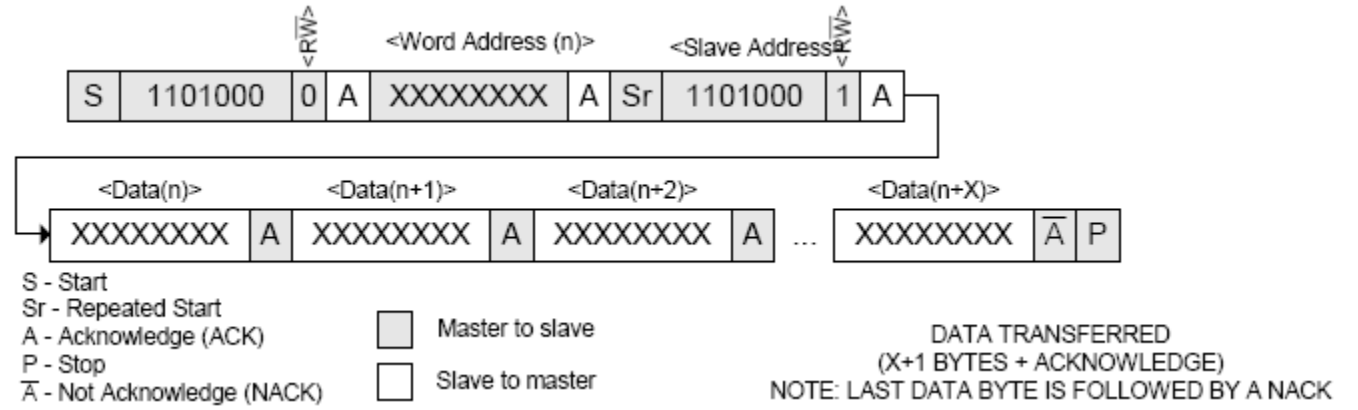
Data Write – Slave Receiver Mode



Data Read (from current Pointer location) – Slave Transmitter Mode



Data Read (Write Pointer, then Read) – Slave Receive and Transmit



Handling, PCB Layout, and Assembly

The IDT1338 package contains a quartz tuning-fork crystal. Pick-and-place equipment may be used, but precautions should be taken to ensure that excessive shocks are avoided. Ultrasonic cleaning equipment should be avoided to prevent damage to the crystal.

Avoid running signal traces under the package, unless a ground plane is placed between the package and the signal line. All NC (no connect) pins must be connected to ground.

Moisture-sensitive packages are shipped from the factory dry-packed. Handling instructions listed on the package label must be followed to prevent damage during re-flow. Refer to the IPC/JEDEC J-STD-020 standard for moisture-sensitive device (MSD) classifications.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the 1338. These ratings, which are standard values for Renesas commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
Voltage Range on Any Pin Relative to Ground	-0.3V to +6.0V
Storage Temperature	-55 to +125°C
Soldering Temperature	260°C

Recommended DC Operating Conditions

(V_{CC} = $V_{CC(MIN)}$ to $V_{CC(MAX)}$, TA = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = 3.3V, TA = +25°C, unless otherwise noted.) (Note 1)

Parameter	Symbol	Min.	Typ.	Max.	Units
Ambient Operating Temperature	T_A	-40		+85	°C
V_{BAT} Input Voltage, Note 2	V_{BAT}	1.3	3.0	3.7	
Pull-up Resistor Voltage (SQW/OUT), Note 2	V_{PU}			5.5	V
Logic 1, Note 2	V_{IH}	$0.8V_{CC}$		V_{CC} + 0.3	V
Logic 0, Note 2	V_{IL}	-0.3		$+0.2V_{CC}$	V
Supply Voltage					
1338-18	V_{CC}	V_{PF}	1.8	5.5	V
1338-31		V_{PF}	3.3	5.5	
Power Fail Voltage					
1338-18	V_{PF}	1.40	1.62	1.71	V
1338-31		2.45	2.7	2.97	

DC Electrical Characteristics

(V_{CC} = $V_{CC(MIN)}$ to $V_{CC(MAX)}$, TA = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = 3.3V, TA = +25°C, unless otherwise noted.) (Note 1)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Leakage	I_{LI}	Note 3			1	µA
I/O Leakage	I_{LO}	Note 4			1	µA
SDA Logic 0 Output	I_{OLSDA}	V_{CC} > 2V; V_{OL} = 0.4V			3.0	mA
		V_{CC} < 2V; V_{OL} = 0.2V_{CC}			3.0	
SQW/OUT Logic 0 Output	I_{OLSQW}	V_{CC} > 2V; V_{OL} = 0.4V			3.0	mA
		1.71V < V_{CC} < 2V; V_{OL} = 0.2V_{CC}			3.0	mA
		1.3V < V_{CC} < 1.71V; V_{OL} = 0.2V_{CC}			250	µA
Active Supply Current (Note 5)	I_{CCA}	1338-18		7.5	15	µA
		1338-31; $V_{CC} \leq$ 3.63V		12	20	
		1338-31; 3.63V < $V_{CC} \leq$ 5.5V		14	25	
Standby Current (Note 6)	I_{CCS}	1338-18		1	2	µA
		1338-31; $V_{CC} \leq$ 3.63 V		1	2	
		1338-31; 3.63V < $V_{CC} \leq$ 5.5V		2	5	
V_{BAT} Leakage Current (V_{CC} Active)	I_{BATLKG}			25	100	nA

DC Electrical Characteristics

(V_{CC} = 0V, TA = -40°C to +85°C, unless otherwise noted. Typical values are at V_{BAT} = 3.0V, TA = +25°C, unless otherwise noted.) (Note 1)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
V_{BAT} Current (OSC ON); V_{BAT} = 3.7V, SQW/OUT OFF	$I_{BATOSC1}$	Note 7		800	1200	nA
V_{BAT} Current (OSC ON); V_{BAT} = 3.7V, SQW/OUT ON	$I_{BATOSC2}$	Note 7		1025	1400	nA
V_{BAT} Data-Retention Current (OSC OFF); V_{BAT} = 3.7V	I_{BATDAT}	Note 7		120	300	nA

AC Electrical Characteristics

(V_{CC} = $V_{CC(MIN)}$ to $V_{CC(MAX)}$, TA = -40°C to +85°C) (Note 1)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
SCL Clock Frequency	f_{SCL}	Fast Mode	100		400	kHz
		Standard Mode	0		100	
Bus Free Time Between a STOP and START Condition	t_{BUF}	Fast Mode	1.3			µs
		Standard Mode	4.7			
Hold Time (Repeated) START Condition, Note 8	$t_{HD:STA}$	Fast Mode	0.6			µs
		Standard Mode	4.0			
Low Period of SCL Clock	t_{LOW}	Fast Mode	1.3			µs
		Standard Mode	4.7			
High Period of SCL Clock	t_{HIGH}	Fast Mode	0.6			µs
		Standard Mode	4.0			
Setup Time for a Repeated START Condition	$t_{SU:STA}$	Fast Mode	0.6			µs
		Standard Mode	4.7			
Data Hold Time (Notes 9, 10)	$t_{HD:DAT}$	Fast Mode	0		0.9	µs
		Standard Mode	0			
Data Setup Time (Note 11)	$t_{SU:DAT}$	Fast Mode	100			ns
		Standard Mode	250			
Rise Time of Both SDA and SCL Signals (Note 12)	t_R	Fast Mode	$20 + 0.1C_B$		300	ns
		Standard Mode	$20 + 0.1C_B$		1000	
Fall Time of Both SDA and SCL Signals (Note 12)	t_F	Fast Mode	$20 + 0.1C_B$		300	ns
		Standard Mode	$20 + 0.1C_B$		300	
Setup Time for STOP Condition	$t_{SU:STO}$	Fast Mode	0.6			µs
		Standard Mode	4.0			
Capacitive Load for Each Bus Line (Note 12)	C_B				400	pF
I/O Capacitance (SDA, SCL)	$C_{I/O}$	Note 13			10	pF
Oscillator Stop Flag (OSF) Delay	t_{OSF}	Note 14		100		ms

WARNING: Negative undershoots below -0.3V while the device is in battery-backed mode may cause loss of data.

Note 1: Limits at -40°C are guaranteed by design and are not production tested.

Note 2: All voltages referenced to ground.

Note 3: SCL only.

Note 4: SDA and SQW/OUT.

Note 5: I_{CCA}—SCL clocking at max frequency = 400kHz.

Note 6: Specified with the I^2C bus inactive.

Note 7: Measured with a 32.768kHz crystal on X1 and X2.

Note 8: After this period, the first clock pulse is generated.

Note 9: A device must internally provide a hold time of at least 300ns for the SDA signal (referred to the V_{IHMIN} of the SCL signal) to bridge the undefined region of the falling edge of SCL.

Note 10: The maximum $t_{HD:DAT}$ need only be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal.

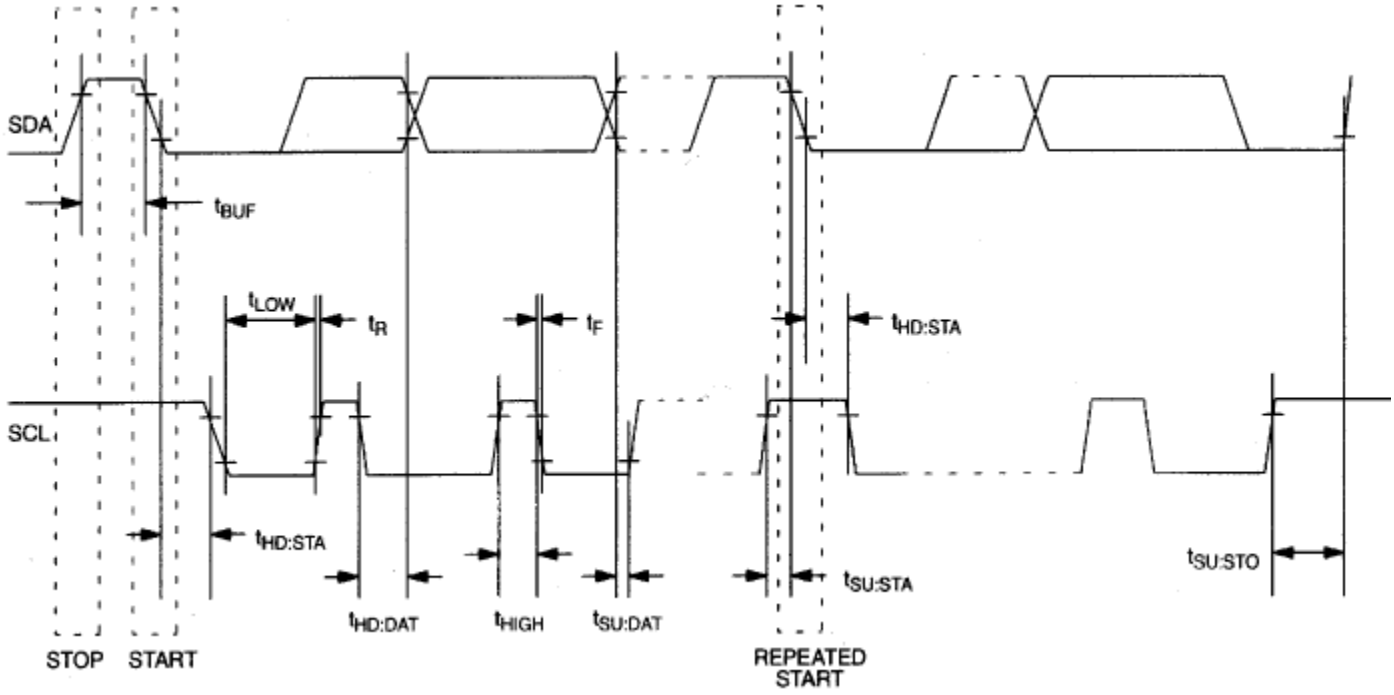
Note 11: A fast-mode device can be used in a standard-mode system, but the requirement $t_{SU:DAT} \geq$ to 250ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{R(MAX)} + t_{SU:DAT} = 1000 + 250 = 1250$ ns before the SCL line is released.

Note 12: C_B—total capacitance of one bus line in pF.

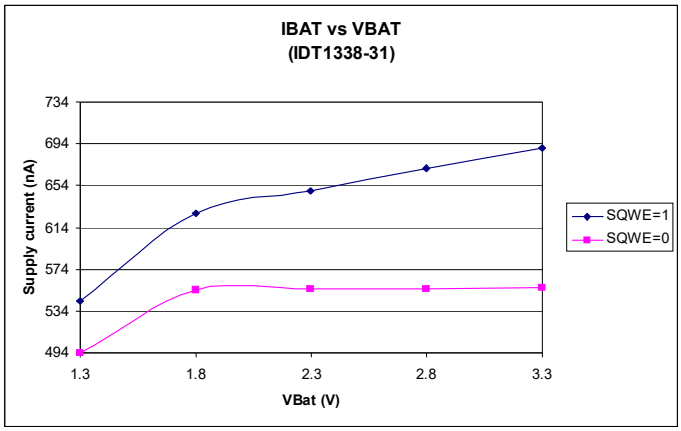
Note 13: Guaranteed by design. Not production tested.

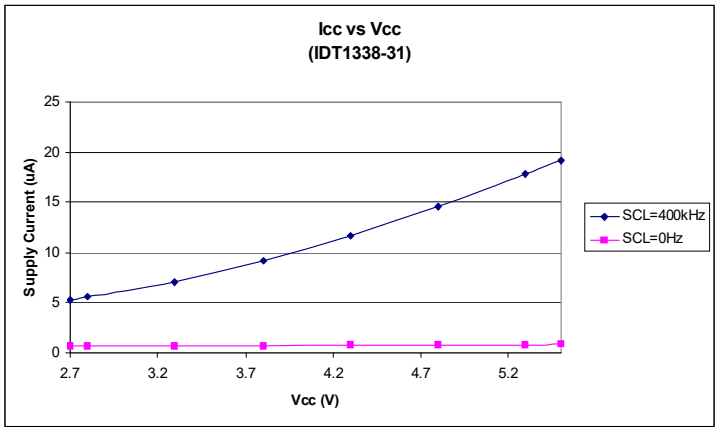
Note 14: The parameter t_{OSF} is the period of time the oscillator must be stopped for the OSF flag to be set over the voltage range of $0.0V \leq V_{CC} \leq V_{CC}MAX$ and $1.3V \leq V_{BACKUP} \leq 3.7V$.

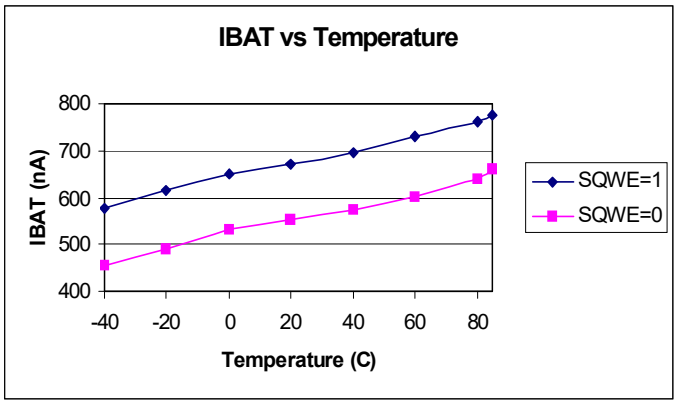
Timing Diagram

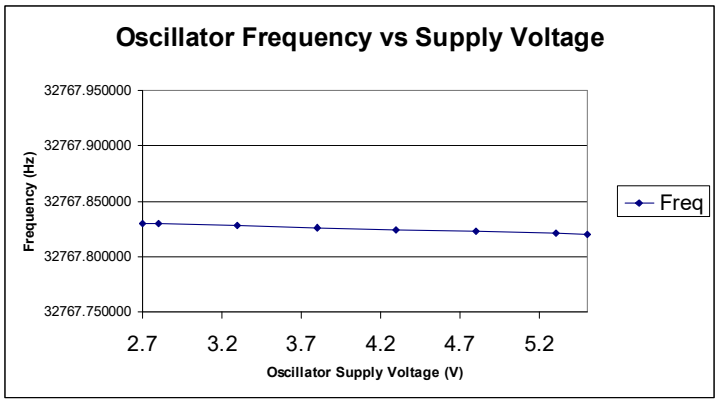


Typical Operating Characteristics









Thermal Characteristics for 8MSOP

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Thermal Resistance Junction to Ambient	θ_{JA}	Still air		95		°C/W
Thermal Resistance Junction to Case	θ_{JC}			48		°C/W

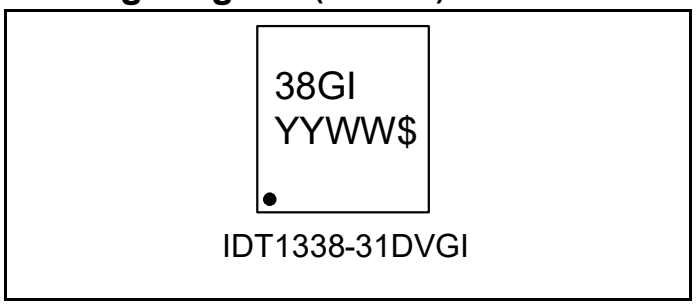
Thermal Characteristics for 8SOIC

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Thermal Resistance Junction to Ambient	θ_{JA}	Still air		150		°C/W
	θ_{JA}	1 m/s air flow		140		°C/W
	θ_{JA}	3 m/s air flow		120		°C/W
Thermal Resistance Junction to Case	θ_{JC}			40		°C/W

Thermal Characteristics for 16SOIC

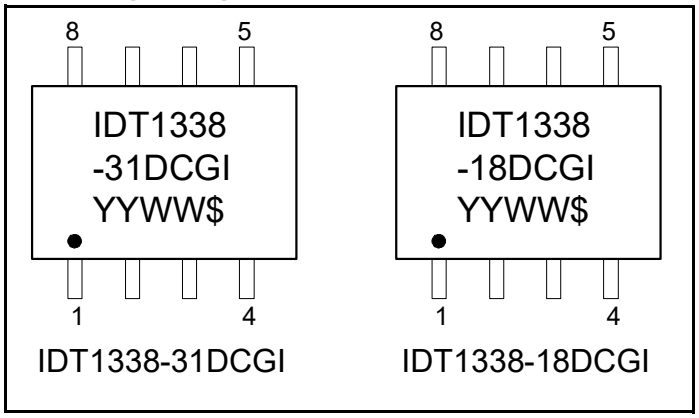
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Thermal Resistance Junction to Ambient	θ_{JA}	Still air		120		°C/W
	θ_{JA}	1 m/s air flow		115		°C/W
	θ_{JA}	3 m/s air flow		105		°C/W
Thermal Resistance Junction to Case	θ_{JC}			58		°C/W

Marking Diagram (8MSOP)



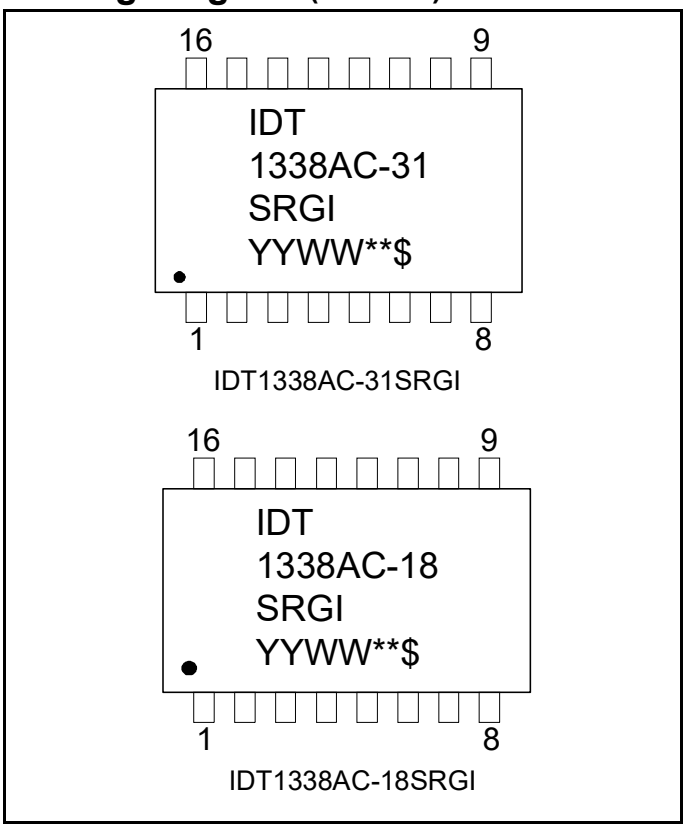
IDT1338-31DVGI

Marking Diagram (8SOIC)



IDT1338-31DCGI IDT1338-18DCGI

Marking Diagram (16SOIC)



IDT1338AC-31SRGI

IDT1338AC-18SRGI

Notes:

1. '$' is the assembly mark code.
2. '**' is the lot sequence.
3. 'YYWW' is the last two digits of the year and week that the part was assembled.
4. "G" denotes RoHS compliant package.
5. "I" denotes industrial grade.
6. Bottom marking: Lot number.

Package Outline Drawings

The package outline drawings are appended at the end of this document and are accessible from the link below. The package information is the most current data available.

8MSOP (TSSOP)
www.idt.com/us/en/document/psc/dvdvg-package-outline-30-x-30-mm-body-tssop

8SOIC
www.idt.com/us/en/document/psc/8-soic-package-outline-drawing-0150-body-width-0050-pitch-dcg8d1

16SOIC
www.idt.com/us/en/document/cpt/pspsgpipig-package-outline-300-body-width-soic-050-pitch

Ordering Information

Part / Order Number	Shipping Packaging	Package	Temperature
1338-18DCGI	Tubes	8-pin SOIC	-40 to +85° C
1338-18DCGI8	Tape and Reel	8-pin SOIC	-40 to +85° C
1338AC-18SRGI	Tubes	16-pin SOIC	-40 to +85° C
1338AC-18SRGI8	Tape and Reel	16-pin SOIC	-40 to +85° C
1338-31DVGI	Tubes	8-pin MSOP	-40 to +85° C
1338-31DVGI8	Tape and Reel	8-pin MSOP	-40 to +85° C
1338-31DCGI	Tubes	8-pin SOIC	-40 to +85° C
1338-31DCGI8	Tape and Reel	8-pin SOIC	-40 to +85° C
1338AC-31SRGI	Tubes	16-pin SOIC	-40 to +85° C
1338AC-31SRGI8	Tape and Reel	16-pin SOIC	-40 to +85° C

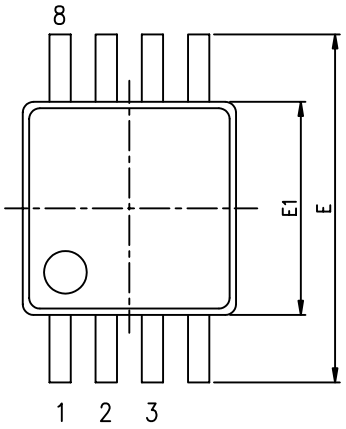
The 1338 packages are RoHS compliant. Packages without the integrated crystal are Pb-free; packages that include the integrated crystal (as designated with a "C" before the dash number) may include lead that is exempt under RoHS requirements. The lead finish is JESD91 category e3.

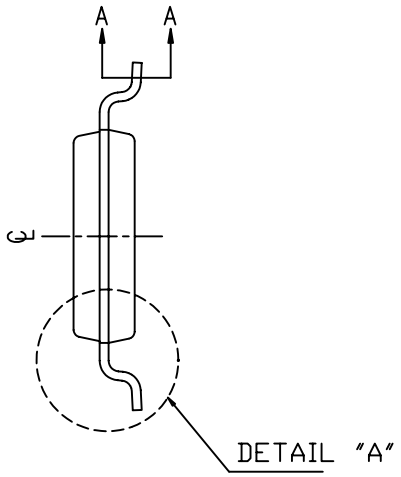
"A" is the device revision designator and will not correlate to the datasheet revision.

Revision History

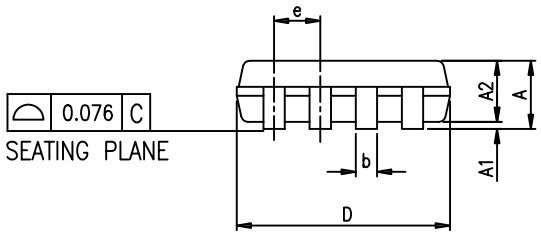
Date	Description of Change
September 30, 2020	• Updated Effective Load Capacitance section; added last sentence of “Cex1...of 12.5pF”. • Rebranded/reformatted datasheet to Renesas.
November 12, 2014	Updated device markings.
March 10, 2014	Changed tVCCF min value from 300µs to 3ms. Added associated note.
February 07, 2013	1. Changed the Vih Min value to 0.8Vcc and the Vil Max value to +0.2Vcc on page 11. This is based on new data taken on TSMC samples (old data was from Fab 4). 2. The IBATDAT current on page 12 should change from 10nA to 120nA (Typ) and from 100nA to 300nA (Max) per latest Characterization data from TSMC.
December 10, 2012	Updated orderable parts - added “G” to 16-pin SOIC parts with SRI/SRI8. New part numbers for 16-pin SOIC will read as SRGI and SRGI8.
September 20, 2012	1. Moved all from Fab4 to TSMC. QA requested change in the marking of only the 16-pin SOIC device with internal crystal to add “A” due to the fact that TSMC uses a different crystal than Fab4. Notification of a change in orderables was initiated with PCN A1208-06. 2. Updated 16-pin SOIC marking diagram and ordering information to include “A”.
October 17, 2011	Added separate item for tVCCF in “Power-up/Down Conditions” table for 1338-31; 300µs min.
September 22, 2011	Changed “V_{CC} Fall Time; $V_{PF(MAX)}$ to $V_{PF(MIN)}$” spec from 300µs Min. to 1ms Min. (Table 2, “Power-Up/Down Characteristics).
April 13, 2011	Updated Supply Current specifications.
March 29, 2010	Added “Timeout” paragraph on page 8.
November 10, 2009	Added “Handling, PCB Layout, and Assembly” section.
December 02, 2008	Updated Typical Operating Characteristics graphs; added marking diagrams.
November 13, 2008	Updated graphs in “Typical Operating Characteristics; added “Typical Operating Circuit” diagram.
November 10, 2008	Updated Block Diagram; Typical Operating Characteristics charts.
May 9, 2008	The part number for 16pin RoHS complaint part has now changed from 1338C-31SOGI to 1338C-31SRI and the 1338C-18SOGI changed to 1338C-18SRI.
April 03, 2004	Combined -3 and -33 parts to -31.
March 28, 2008	Added new note to Part Ordering information pertaining to RoHS compliance and Pb-free devices.
January 29, 2008	New device. Preliminary release.

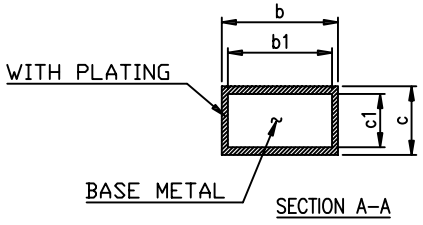
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
00	INITIAL RELEASE	8/29/08	RT
01	UPDATE DIM TO BE JEDEC COMPLIANT	7/31/12	R. Tanh
02	COMBINE POD & LAND PATTERN	7/23/13	KS



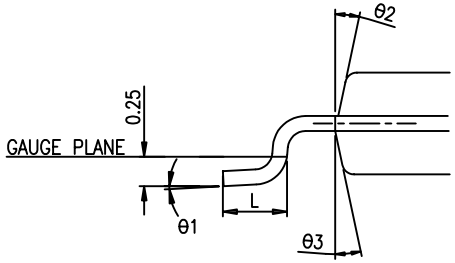


SYMBOL	DIMENSION IN MM		
	MIN.	NOM.	MAX.
A	---	---	1.10
A1	0.00	---	0.15
A2	0.75	0.85	0.95
c	0.08	---	0.23
c1	0.08	---	0.18
D	2.80	3.00	3.20
E1	2.80	3.00	3.20
E	4.90 BSC		
L	0.400	0.600	0.800
θ1	0°		8°





SYMBOL	8L			10L		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
b	0.22	---	0.38	0.17	---	0.27
b1	0.22	0.30	0.33	0.17	0.20	0.23
e	0.65 BSC			0.50 BSC		
JEDEC	MO-187AA			MO-187		



DETAIL "A"
SCALE 25:1

TOLERANCES UNLESS SPECIFIED
DIMENSIONS ARE IN INCHES(METRIC
DIMENSIONS APPLY AFTER FINISH.
TOLERANCES ARE:
DECIMALS ANGLES
.XX±.01 .XXX±.005 .±1°
SURFACE ROUGHNESS= 32
BREAK EDGES: .010 MAX.
SURFACES TO BE FREE OF BURRS,
SCARTCHES, CHIPS, AND DENTS.
THIRD ANGLE PROJECTION

APPROVALS	DATE
DRAWN RAC	08/29/08
CHECKED	

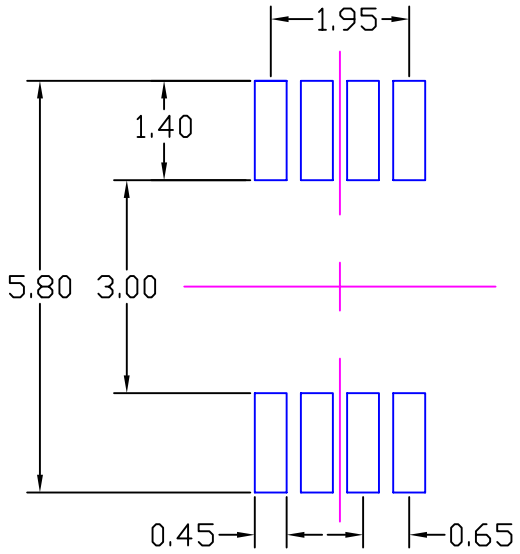
IDT™
www.IDT.com
6024 Silver Creek Valley Road
San Jose CA 95138
PHONE: (408) 284-8200
FAX: (408) 284-8591

TITLE DV/DVG PACKAGE OUTLINE
3.0 x 3.0 mm BODY
TSSOP

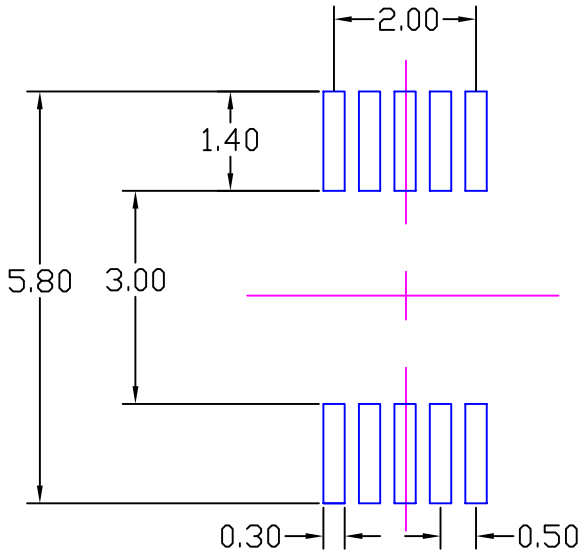
SIZE	DRAWING No.	REV
C	PSC-4163	02

DO NOT SCALE DRAWING | SHEET 1 OF 2

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
00	INITIAL RELEASE	8/29/08	RT
01	UPDATE DIM TO BE JEDEC COMPLIANT	7/31/12	R. Tanh
02	COMBINE POD & LAND PATTERN	7/23/13	KS



N=8



N=10

RECOMMENDED LAND PATTERN

NOTES:

1. ALL DIMENSION ARE IN mm. ANGLES IN DEGREES.
2. TOP DOWN VIEW. AS VIEWED ON PCB.
3. LAND PATTERN IN BLUE. NSMD PATTERN ASSUMED.
4. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

TOLERANCES UNLESS SPECIFIED
DIMENSIONS ARE IN INCHES(METRIC DIMENSIONS APPLY AFTER FINISH.
TOLERANCES ARE:
DECIMALS .XX±.01 .XXX±.005
ANGLES .±1°
SURFACE ROUGHNESS= 32√
BREAK EDGES: .010 MAX.
SURFACES TO BE FREE OF BURRS, SCARTCHES, CHIPS, AND DENTS.
THIRD ANGLE PROJECTION

APPROVALS	DATE
DRAWN RAC	08/29/08
CHECKED	

IDT™
www.IDT.com
6024 Silver Creek Valley Road
San Jose CA 95138
PHONE: (408) 284-8200
FAX: (408) 284-8591

TITLE DV/DVG PACKAGE OUTLINE
3.0 x 3.0 mm BODY
TSSOP

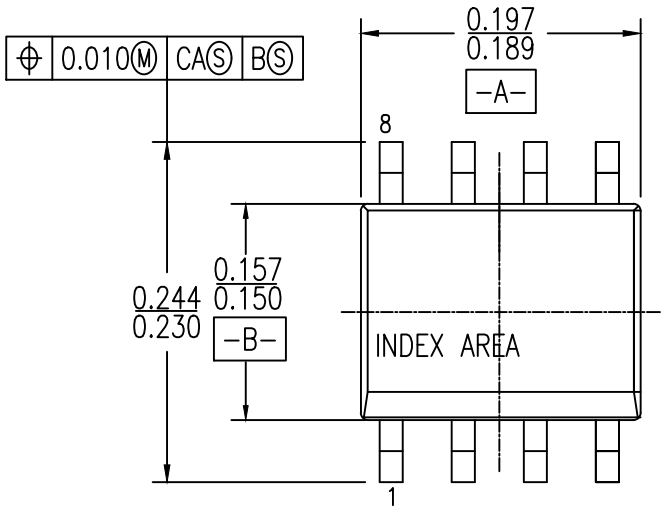
SIZE	DRAWING No.	REV
C	PSC-4163	02

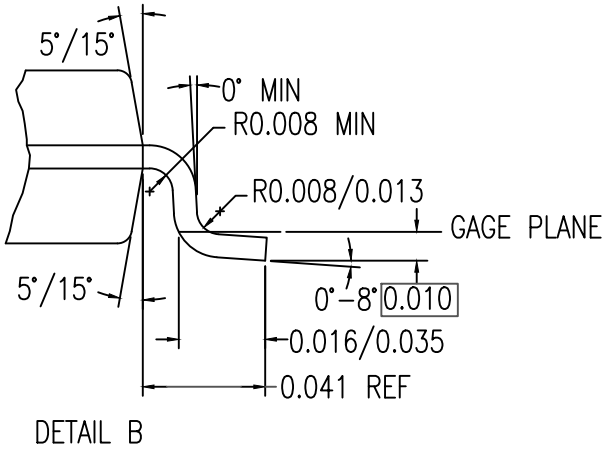
DO NOT SCALE DRAWING | SHEET 2 OF 2

8-SOIC Package Outline Drawing

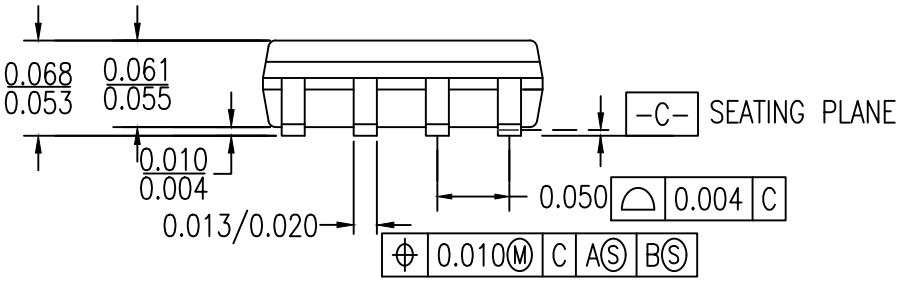
0.150" Body Width, 0.050" Pitch

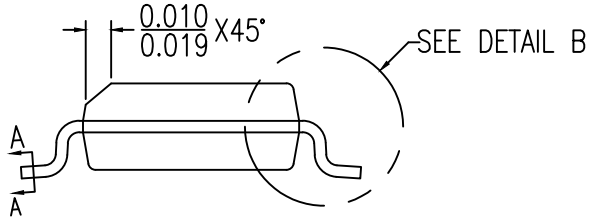
DCG8D1, PSC-4068-01, Rev 01, Page 1

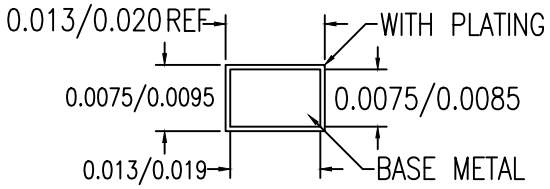




DETAIL B





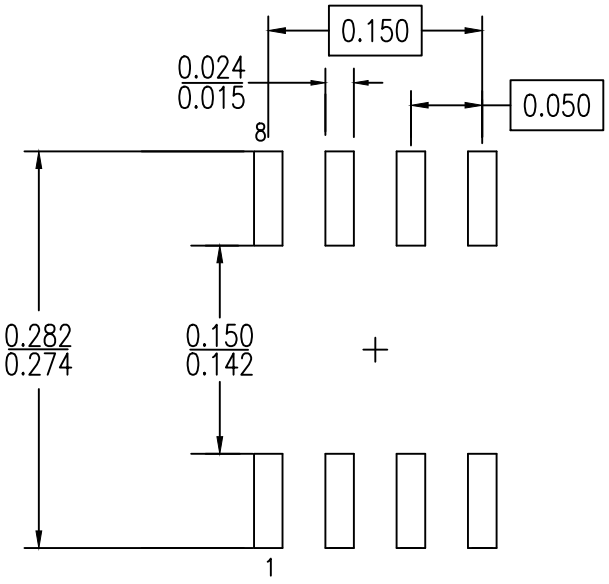


SECTION A-A

NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982
2. ALL DIMENSIONS ARE IN INCHES

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RECOMMENDED LAND PATTERN DIMENSION

NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M–1982
2. ALL DIMENSIONS ARE IN INCHES

Package Revision History		
Date Created	Rev No.	Description
July 27, 2018	Rev 01	Dedicate to Package DCG8 Only
Feb 24, 2016	Rev 00	Initial Release

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(Rev.1.0 Mar 2020)

Corporate Headquarters

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Koto-ku, Tokyo 135-0061, Japan
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