# PECL/CMOS TO CMOS CLOCK DRIVER

# ICS558-01

## Description

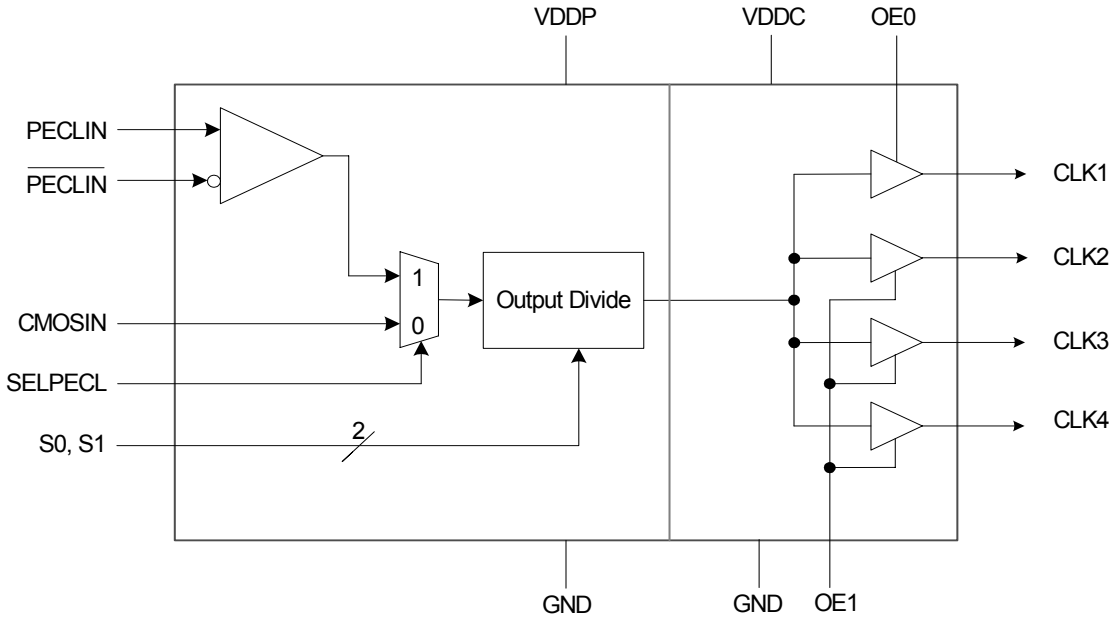
The ICS558-01 accepts a high speed input of either PECL or CMOS, integrates a divider of 1, 2, 3, or 4, and provides four CMOS low skew outputs. The chip also has output enables so that one, three, or all four outputs can be tri-stated.

The ICS558-01 is a member of the IDT Clock Blocks™ family of clock generation, synchronization, and distribution devices.

## Features

- 16-pin TSSOP package
- Pb (lead) free package
- Selectable PECL or CMOS inputs
- Operates up to 250 MHz
- Works as a voltage translator
- Four low skew (<250 ps) outputs
- Selectable internal divider
- Operating input voltages of 3.3 V or 5.0 V
- Operating output voltages of 2.5 V, 3.3 V or 5.0 V
- Ideal for IA64 designs

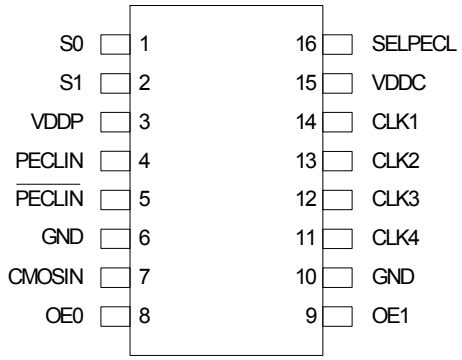
## Block Diagram






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## Pin Assignment




16-pin 173 Mil (0.65mm) TSSOP

### Input Clock Selection

| SELPECL | Input |
|---|---|
| 0 | CMOSIN |
| 1 | PECLIN |

### Tri-State Table

| OE1 | OE0 | CLK 1 | CLK 2, 3, 4 |
|---|---|---|---|
| 0 | 0 | Tri-state | Tri-state |
| 0 | 1 | Clock ON | Tri-state |
| 1 | 0 | Tri-state | Clock ON |
| 1 | 1 | Clock ON | Clock ON |

### Output Divide Selection

| S1 | S0 | Output Divide |
|---|---|---|
| 0 | 0 | /1 |
| 0 | 1 | /2 |
| 1 | 0 | /3 |
| 1 | 1 | /4 |

## Pin Descriptions

| Pin Number | Pin Name | Pin Type | Pin Description |
|---|---|---|---|
| 1 | S0 | Input | Select 0 for output divider. See table above. Internal pull-up to VDDP. |
| 2 | S1 | Input | Select 1 for output divider. See table above. Internal pull-up to VDDP. |
| 3 | VDDP | Power | Connect to +3.3 V or +5 V. Decouple to pin 6. |
| 4 | PECLIN | Clock Input | PECL input. Connect to ground if not used. |
| 5 | PECLIN | Clock Input | Complimentary PECL input. Connect to ground if not used. |
| 6 | GND | Power | Connect to ground. |
| 7 | CMOSIN | Clock Input | CMOS input. Connect to ground if not used. |
| 8 | OE0 | Input | Output Enable 0. See table above. Internal pull-up to VDDP. |
| 9 | OE1 | Input | Output Enable 1. See table above. Internal pull-up to VDDP. |
| 10 | GND | Power | Connect to ground. |
| 11 | CLK4 | Output | Low skew clock output. |
| 12 | CLK3 | Output | Low skew clock output. |
| 13 | CLK2 | Output | Low skew clock output. |
| 14 | CLK1 | Output | Low skew clock output. |
| 15 | VDDC | Power | Connect to +2.5 V, +3.3 V, or +5 V. Decouple to pin 10. |
| 16 | SELPECL | Input | Selects PECL or CMOS input. See table above. Internal pull-up to VDDP. |



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## External Components

The ICS558-01 requires two 0.01 µF capacitors between VDDP and GND, and VDDC and GND—one on each side of the chip. These must be close to the chip to minimize lead inductance. Series termination resistors of 33Ω can be used on the outputs (these also must be close to the chip).

## Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the ICS558-01. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

| Item | Rating |
|---|---|
| Supply Voltage; VDDP, VDDC (referenced to ground) | 7.0 V |
| Inputs and Clock Outputs (referenced to ground) | -0.5 V to VDD+0.5 V |
| Ambient Operating Temperature | 0 to +70 °C |
| Storage Temperature | -65 to +150 °C |
| Soldering Temperature (maximum of 10 seconds) | 260 °C |

## DC Electrical Characteristics

**VDDP = VDDC = 3.3V** (unless stated otherwise), Ambient temperature 0 to +70 °C

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| Operating Voltage, VDDP | | VDDP ≥ VDDC | 3.0 | | 5.5 | V |
| Operating Voltage, VDDC | | VDDP ≥ VDDC | 2.375 | | VDDP | V |
| Input High Voltage, CMOSIN | $V_{IH}$ | | (VDDP/2)+1 | | | V |
| Input Low Voltage, CMOSIN | $V_{IL}$ | | | | (VDDP/2)-1 | V |
| Input High Voltage | $V_{IH}$ | non-clock pins | VDDP-0.5 | | VDDP | V |
| Input Low Voltage | $V_{IL}$ | non-clock pins | | | 0.5 | V |
| Common Mode Range, PECLIN | | VDDP=5 V | VDDP-3.7 | | VDDP-0.6 | V |
| Common Mode Range, PECLIN | | VDDP=3.3 V | VDDP-2.0 | | VDDP-0.6 | V |
| Peak-to-Peak Input Voltage, PECLIN | | | 0.3 | | 1.0 | V |
| Output High Voltage | $V_{OH}$ | VDDC = 5 V, $I_{OH}$ = -24 mA | VDDC-0.4 | | | V |
| Output Low Voltage | $V_{OL}$ | VDDC = 5 V, $I_{OL}$ = 24 mA | | | 0.4 | V |
| Output High Voltage | $V_{OH}$ | VDDC = 3.3 V, $I_{OH}$ = -18 mA | VDDC-0.4 | | | V |
| Output Low Voltage | $V_{OL}$ | VDDC = 3.3 V, $I_{OL}$ = 18 mA | | | 0.4 | V |



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| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| Output High Voltage | $V_{OH}$ | VDDC = 2.5 V, $I_{OH}$ = -8 mA | VDDC-0.4 | | | V |
| Output Low Voltage | $V_{OL}$ | VDDC = 2.5 V $I_{OL}$ = 8 mA | | | 0.4 | V |
| Operating Supply Current | IDDP | No load, 100 MHz input | | 22 | | mA |
| Operating Supply Current | IDDC | No load, 100 MHz input | | 18 | | mA |
| Short Circuit Current | | | | +70 | | mA |
| On-chip pull-up resistor | $R_{PU}$ | | | 250 | | kΩ |
| Input Capacitance | $C_{IN}$ | | | 4 | | pF |

## AC Electrical Characteristics

**VDDP = VDDC = 3.3 V** (unless stated otherwise), Ambient Temperature 0 to +70 °C

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| Input Frequency | | | 0 | | 250 | MHz |
| Output Rise Time | $t_{OR}$ | | | | 800 | ps |
| Output Fall Time | $t_{OF}$ | | | | 750 | ps |
| Skew, between any output clocks | | (Assumes identically loaded outputs with identical rise times, measured at VDDC/2) | | 0 | 250 | ps |
| Propagation Delay | | /1 | | 5.0 | | ns |
| | | /2 | | 6.0 | | ns |
| | | /3 | | | | ns |
| | | /4 | | 7.0 | | ns |
| Output Clock Duty Cycle for /2 and /4 | | | 45 | 50 | 55 | % |
| Output Clock Duty Cycle for /1 and /3 | | | 45 | 50 | 55 | % |

## Thermal Characteristics (16-pin TSSOP)

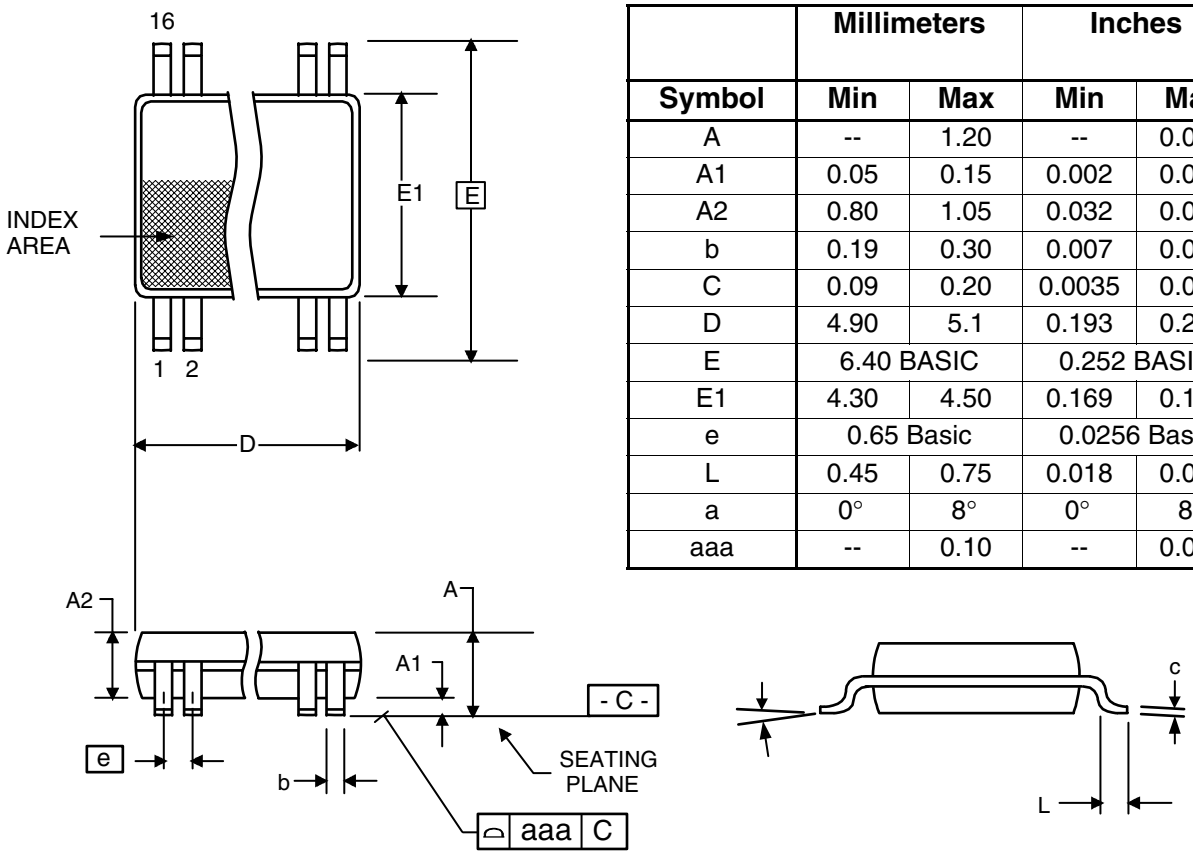
| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| Thermal Resistance Junction to Ambient | $\theta_{JA}$ | Still air | | 78 | | °C/W |
| | $\theta_{JA}$ | 1 m/s air flow | | 70 | | °C/W |
| | $\theta_{JA}$ | 3 m/s air flow | | 68 | | °C/W |
| Thermal Resistance Junction to Case | $\theta_{JC}$ | | | 37 | | °C/W |



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## Package Outline and Package Dimensions (16-pin TSSOP, 4.40 mm Body, 0.65 mm Pitch)

Package dimensions are kept current with JEDEC Publication No. 95, MO-153




| | Millimeters | | Inches | |
|---|---|---|---|---|
| Symbol | Min | Max | Min | Max |
| A | -- | 1.20 | -- | 0.047 |
| A1 | 0.05 | 0.15 | 0.002 | 0.006 |
| A2 | 0.80 | 1.05 | 0.032 | 0.041 |
| b | 0.19 | 0.30 | 0.007 | 0.012 |
| C | 0.09 | 0.20 | 0.0035 | 0.008 |
| D | 4.90 | 5.1 | 0.193 | 0.201 |
| E | 6.40 BASIC | | 0.252 BASIC | |
| E1 | 4.30 | 4.50 | 0.169 | 0.177 |
| e | 0.65 Basic | | 0.0256 Basic | |
| L | 0.45 | 0.75 | 0.018 | 0.030 |
| a | 0° | 8° | 0° | 8° |
| aaa | -- | 0.10 | -- | 0.004 |

## Ordering Information

| Part / Order Number | Marking | Shipping Packaging | Package | Temperature |
|---|---|---|---|---|
| 558G-01LF | 558G-01LF | Tubes | 16-pin TSSOP | 0 to +70° C |
| 558G-01LFT | 558G-01LF | Tape and Reel | 16-pin TSSOP | 0 to +70° C |

**"LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.**

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