GLITCH-FREE CLOCK MULITPLEXER ICS580-01

Description

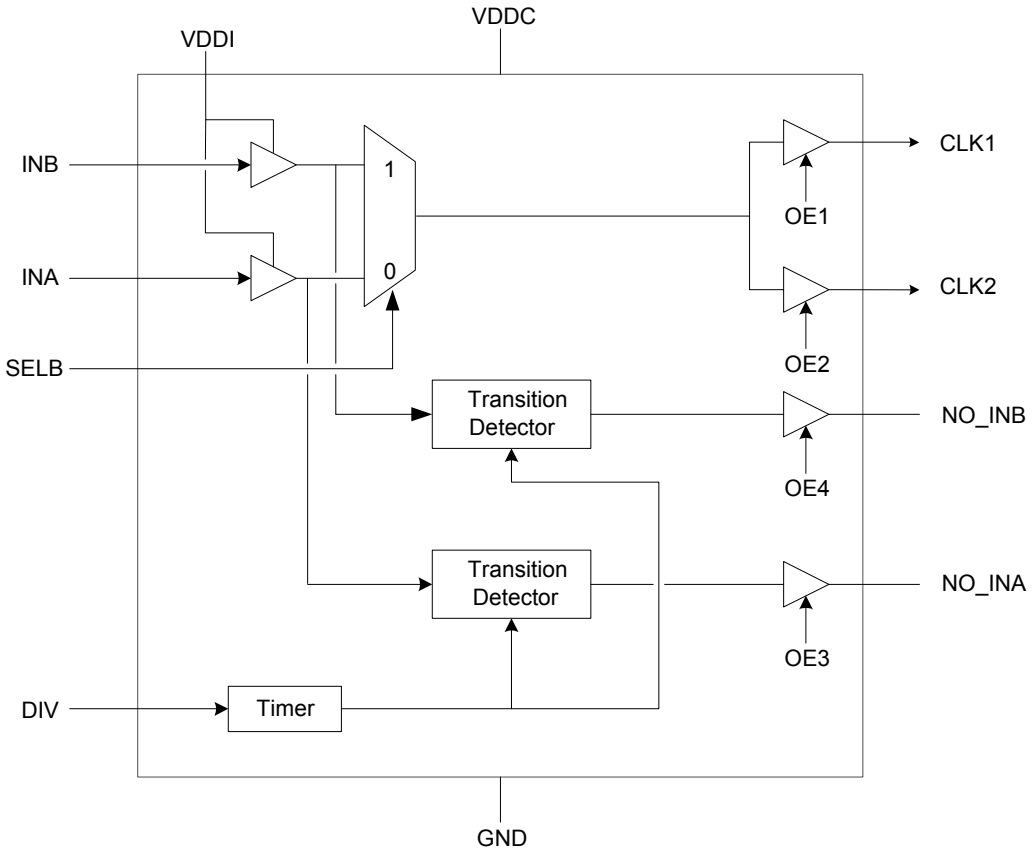
The ICS580-01 is a clock multiplexer (mux) designed to switch between two clock sources with no glitches or short pulses. The operation of the mux is controlled by an input pin but the part can also be configured to switch automatically if one of the input clocks stops. The part also provides clock detection by reporting when an input clock has stopped.

For a clock mux with zero delay and smooth switching, see either the ICS581-01 or the ICS581-02.

Features

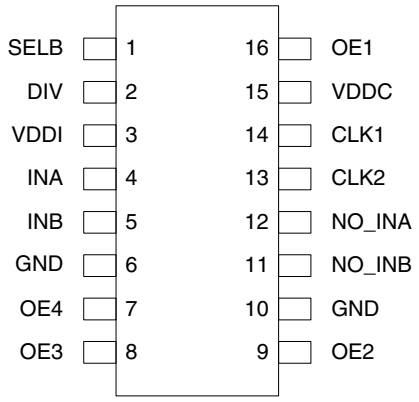
- 16-pin SOIC and 16-pin TSSOP packages available
- Pb (lead) free package
- No short pulses or glitches on output
- Operates from 2 to 220 MHz
- Low skew outputs
- Clock detect feature
- Ideal for systems with back-up or redundant clocks
- Selectable timeouts for clock detection
- Separate supply voltages allow power supply voltage translation
- Operates from 2.5 V to 5 V

Block Diagram

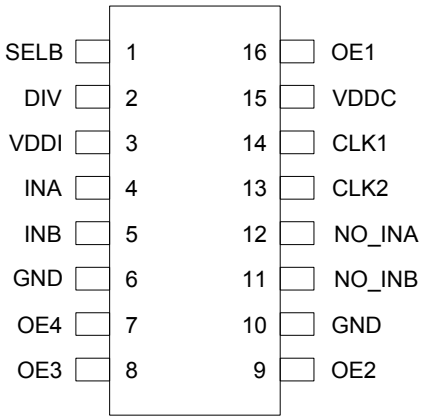


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Pin Assignment



16 pin (150 mil) SOIC



16-pin TSSOP

Timeout Selection

DIV	Nominal Timeout
0	600 ns
1	75 ns

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Pin Descriptions

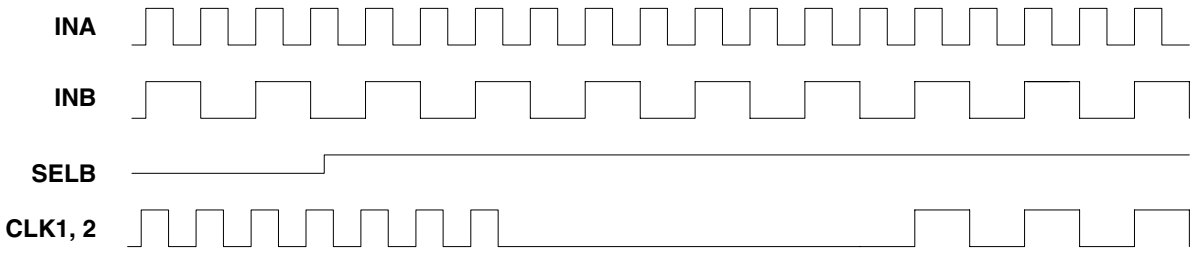
Pin Number	Pin Name	Pin Type	Pin Description
1	SELB	Input	Mux select. Selects INB when high. Internal pull-up.
2	DIV	Input	Time out select. See table above. Internal pull-up.
3	VDDI	Power	Supply for input clocks only. Can be higher than VDDC.
4	INA	Input	Input Clock A.
5	INB	Input	Input Clock B.
6	GND	Power	Connect to ground.
7	OE4	Input	Output enable. Tri-states NO_INB when low. Internal pull-up.
8	OE3	Input	Output enable. Tri-states NO_INA when low. Internal pull-up.
9	OE2	Input	Output enable. Tri-states CLK2 when low. Internal pull-up.
10	GND	Power	Connect to ground.
11	NO_INB	Output	Goes high when clock on INB stops.
12	NO_INA	Output	Goes high when clock on INA stops.
13	CLK2	Output	Clock 2 output. Low skew compared to CLK1.
14	CLK1	Output	Clock 1 output. Low skew compared to CLK2.
15	VDDC	Power	Main chip supply. Output clocks amplitude will match this VDD.
16	OE1	Input	Output enable. Tri-states CLK1 when low. Internal pull-up.

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Device Operation

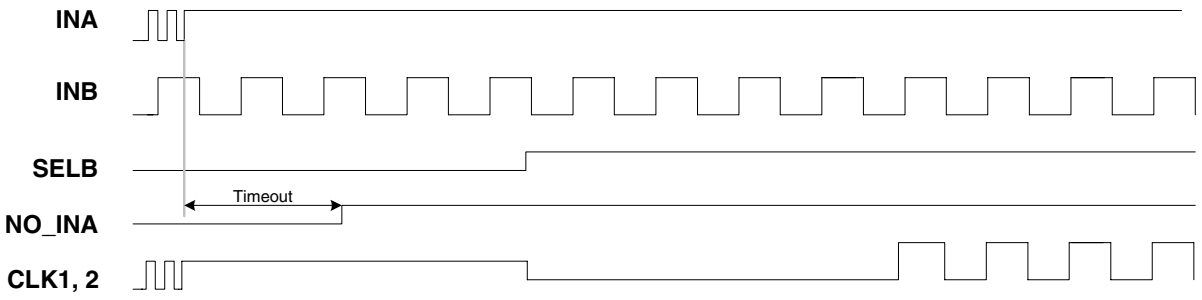
The ICS580-01 consists of a glitch free mux between INA and INB controlled by SELB. The device is designed to switch between two clocks, whether running or not. In the first example, clocks are running on both INA and INB. When SELB changes, the output clock goes low after three cycles of the output clock (nominally). The output then stays low for three cycles of the new input clock (nominally) and then starts with the new input clock. This is shown in Figure 1.

Figure 1



In the second example, one of the inputs was selected and running but has since stopped (either high or low). This is indicated by either NO_INA or NO_INB going high depending on whether INA or INB has stopped. These signals go high following a selectable time-out period after the clock has stopped. The timeout period is determined by the DIV input in. The SELB pin is now changed to select the new input clock which is running. The output clock immediately goes low and stays low for three cycles of the new input clock and then starts with the new input clock. Figure 2 shows an example of this

Figure 2

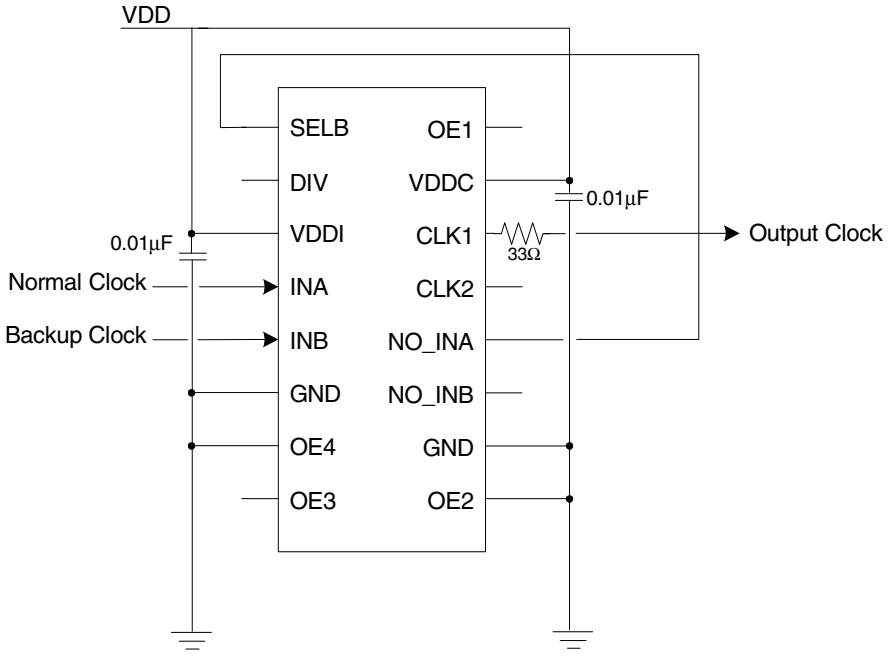


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Application Example

In the third example, the ICS580-01 is configured to automatically switch clocks when an input stops. The clock that could stop is connected to INA while the backup clock (always running) is connected to INB. The output NO_INA is connected to SELB. This means that when the clock on INA stops, NO_INA goes high selecting the clock on INB which is muxed to the output after three cycles. When the clock on INA restarts, NO_INA immediately goes low, selecting the clock on INA. The output then switches in the manner described in the first example.

The circuit diagram in Figure 3 shows a typical connection for this example. Note that CLK2 and NO_INB are unused and are disabled by grounding OE2 and OE4. A 33Ω series termination resistor is used on the clock output and two decoupling capacitors of 0.01µF are used. All other inputs are left floating and are therefore pulled high by the on-chip pull-ups.



Output Enable

Each output has a dedicated output enable pin. If an output is unused, it should be tri-stated by tying the appropriate output enable pin to ground.

External Components

The ICS580-01 requires two 0.01µF decoupling capacitors, one between VDDI and GND and one between VDDC and GND. Series termination resistors of 33Ω can be used on CLK1 and CLK2.

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Split Power Supplies

The VDDI pin provides the power for the INA and INB input buffers only. All the other inputs and the rest of the chip are connected to VDDC. This allows for supply voltage translation. For example, INA and INB could be 5V clocks (VDDI = 5V) and the rest of the chip could use a 3.3V supply on VDDC giving 3.3V output clocks. For correct operation VDDI must always be greater than or equal to VDDC.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the ICS580-01. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
Supply Voltage, VDD	7V
All Inputs and Outputs	-0.5V to VDD+0.5V
Ambient Operating Temperature	0 to +70° C
Ambient Operating Temperature	-40 to +85° C
Storage Temperature	-65 to +150° C
Junction Temperature	125° C
Soldering Temperature	260° C

Recommended Operation Conditions

Parameter	Min.	Typ.	Max.	Units
Ambient Operating Temperature	0		+70	° C
Ambient Operating Temperature	-40		+85	° C
Power Supply Voltage (measured in respect to GND)	+2.5		+5.5	V

DC Electrical Characteristics

Unless stated otherwise, VDD = 3.3V ±5%, Ambient Temperature -40 to +85° C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDDC		2.5		5.5	V
	VDDI		VDDC		5.5	V
Supply Current	IDD	50 MHz, no load		6		mA
Input High Voltage	V_{IH}	Non-clock inputs	2		VDDC	V
Input Low Voltage	V_{IL}	Non-clock inputs			0.8	V
Input High Voltage	V_{IH}	INA and INB only Note 3	(VDDC/2)+1		VDDI	V

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Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Low Voltage	V_{IL}	INA and INB only Note 3			(VDDC/2)-1	V
Input Capacitance	C_{IN}			4		pF
Output High Voltage	V_{OH}	I_{OH} = -12 mA	VDDC-0.5			V
Output Low Voltage	V_{OL}	I_{OL} = 12 mA			0.5	V
Short Circuit Current	I_{OS}			±70		mA
On-chip pull-up Resistor	R_{PU}	Non-clock inputs Pull-up to VDDC		250		kΩ

AC Electrical Characteristics

Unless stated otherwise, VDD = 3.3V ±5%, Ambient Temperature -40 to +85° C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Frequency INA and INB, Note 1	f_{IN}	VDDC = 5V	1/timeout		270	MHz
		VDDC = 3.3V	1/timeout		220	MHz
		VDDC = 2.7V	1/timeout		180	MHz
Propagation Delay INA or INB to output		VDDC = 5V		4	8	ns
		VDDC = 3.3V		5	10	ns
		VDDC = 2.7V		6	12	ns
Transition Detector Timeout, DIV = 0		VDDI = 5V	175	350	750	ns
		VDDI = 3.3V	500	1000	2000	ns
		VDDI = 2.7V	750	1500	3000	ns
Transition Detector Timeout, DIV = 1		VDDI = 5V	20	40	80	ns
		VDDI = 3.3V	55	110	210	ns
		VDDI = 2.7V	100	200	400	ns
Output Clock Rise Time					1.5	ns
Output Clock Fall Time					1.5	ns
Output Clock Skew		CLK1 to CLK2 Note 2	-250	0	250	ps

Note 1. Frequencies less than the minimum may cause a timeout which will not guarantee glitch-free switching unless the clock is actually stopped.

Note 2: Assumes identically loaded outputs with identical rise times, measured at VDD/2.

Note 3: Output duty cycle is set by duty cycle of input clock at VDDC/2.

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Thermal Characteristics (16-pin SOIC)

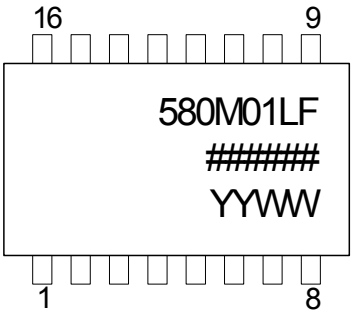
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Thermal Resistance Junction to Ambient	θ_{JA}	Still air		120		°C/W
	θ_{JA}	1 m/s air flow		115		°C/W
	θ_{JA}	3 m/s air flow		105		°C/W
Thermal Resistance Junction to Case	θ_{JC}			58		°C/W

Thermal Characteristics (16-pin TSSOP)

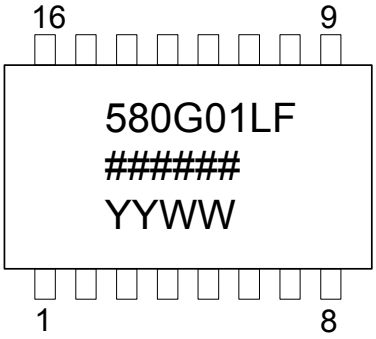
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Thermal Resistance Junction to Ambient	θ_{JA}	Still air		78		°C/W
	θ_{JA}	1 m/s air flow		70		°C/W
	θ_{JA}	3 m/s air flow		68		°C/W
Thermal Resistance Junction to Case	θ_{JC}			37		°C/W

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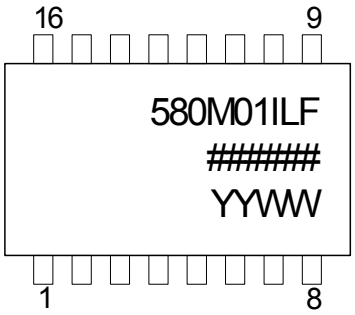
Marking Diagram (ICS580M-01LF)



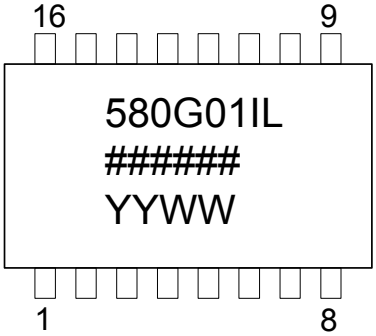
Marking Diagram (ICS580G-01LF)



Marking Diagram (ICS580M-01ILF)



Marking Diagram (ICS580G-01ILF)



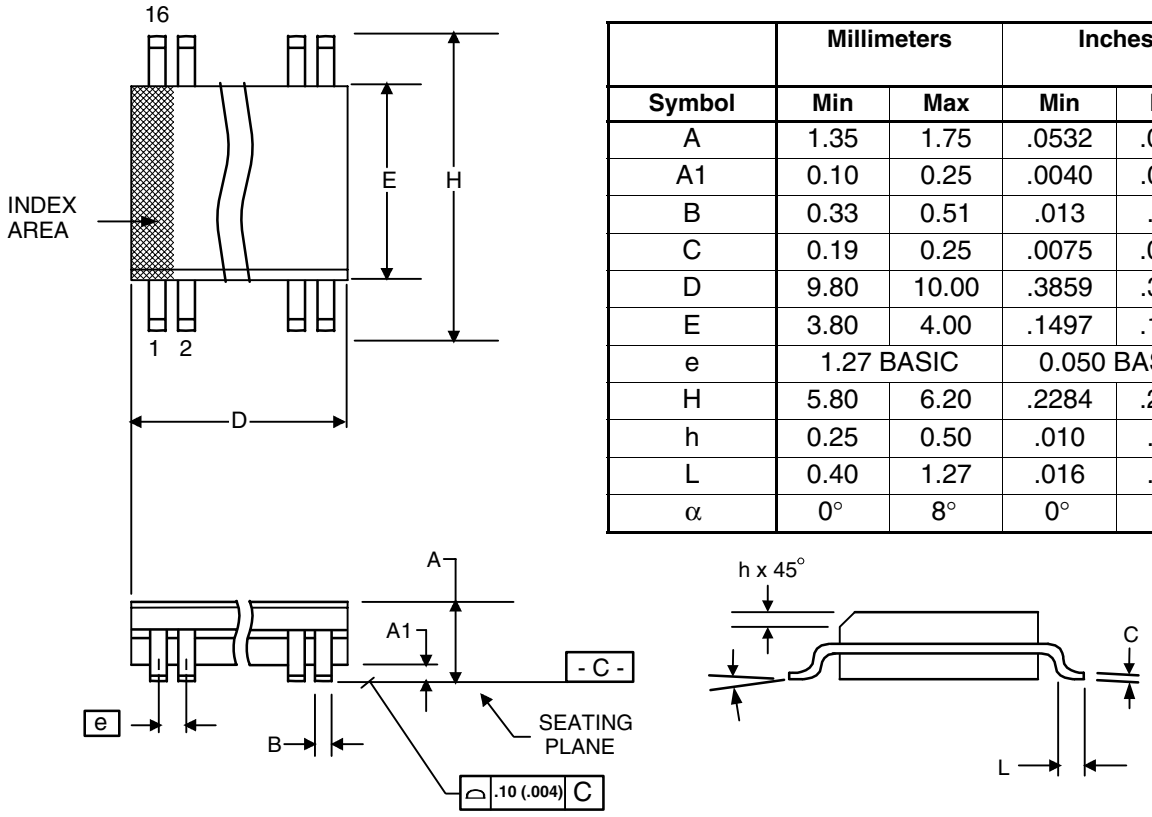
Notes:

1. ###### is the lot number.
2. YYWW is the last two digits of the year and week that the part was assembled.
3. “LF” or “L” denotes Pb (lead) free package.
4. “I” indicates industrial grade.
4. Bottom marking: country of origin if not USA.

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Package Outline and Package Dimensions (16-pin SOIC, 150 Mil. Narrow Body)

Package dimensions are kept current with JEDEC Publication No. 95

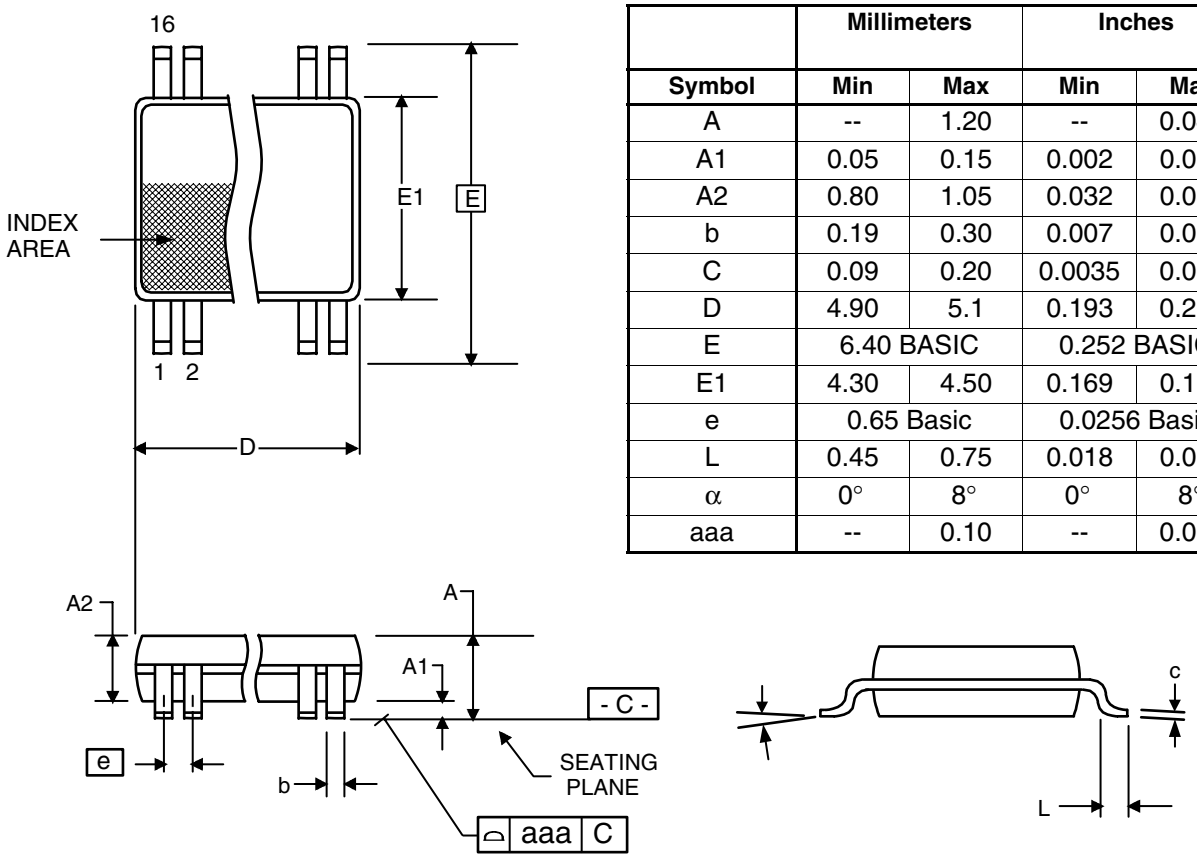


	Millimeters		Inches	
Symbol	**Min**	**Max**	**Min**	**Max**
A	1.35	1.75	.0532	.0688
A1	0.10	0.25	.0040	.0098
B	0.33	0.51	.013	.020
C	0.19	0.25	.0075	.0098
D	9.80	10.00	.3859	.3937
E	3.80	4.00	.1497	.1574
e	1.27 BASIC		0.050 BASIC	
H	5.80	6.20	.2284	.2440
h	0.25	0.50	.010	.020
L	0.40	1.27	.016	.050
α	0°	8°	0°	8°

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Package Outline and Package Dimensions (16-pin TSSOP, 173 Mil. Body)

Package dimensions are kept current with JEDEC Publication No. 95



	Millimeters		Inches	
Symbol	**Min**	**Max**	**Min**	**Max**
A	--	1.20	--	0.047
A1	0.05	0.15	0.002	0.006
A2	0.80	1.05	0.032	0.041
b	0.19	0.30	0.007	0.012
C	0.09	0.20	0.0035	0.008
D	4.90	5.1	0.193	0.201
E	6.40 BASIC		0.252 BASIC	
E1	4.30	4.50	0.169	0.177
e	0.65 Basic		0.0256 Basic	
L	0.45	0.75	0.018	0.030
α	0°	8°	0°	8°
aaa	--	0.10	--	0.004

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Ordering Information

Part / Order Number	Marking	Shipping Packaging	Package	Temperature
580M-01LF	see page 9	Tubes	16-pin SOIC	0 to +70° C
580M-01LFT		Tape and Reel	16-pin SOIC	0 to +70° C
580M-01ILF		Tubes	16-pin SOIC	-40 to +85° C
580M-01ILFT		Tape and Reel	16-pin SOIC	-40 to +85° C
580G-01LF	see page 9	Tubes	16-pin TSSOP	0 to +70° C
580G-01LFT		Tape and Reel	16-pin TSSOP	0 to +70° C
580G-01ILF		Tubes	16-pin TSSOP	-40 to +85° C
580G-01ILFT		Tape and Reel	16-pin TSSOP	-40 to +85° C

"LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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