# SNx4AHCT240 Octal Inverting Buffers/Drivers With Tri-State Outputs

## 1 Features

- Inputs are TTL-Voltage Compatible
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- On Products Compliant to MIL-PRF-38535, All Parameters Are Tested Unless Otherwise Noted. On All Other Products, Production Processing Does Not Necessarily Include Testing of All Parameters.

## 2 Applications

- Network Switches
- Health and Fitness
- Televisions
- Power Infrastructures

## 3 Description

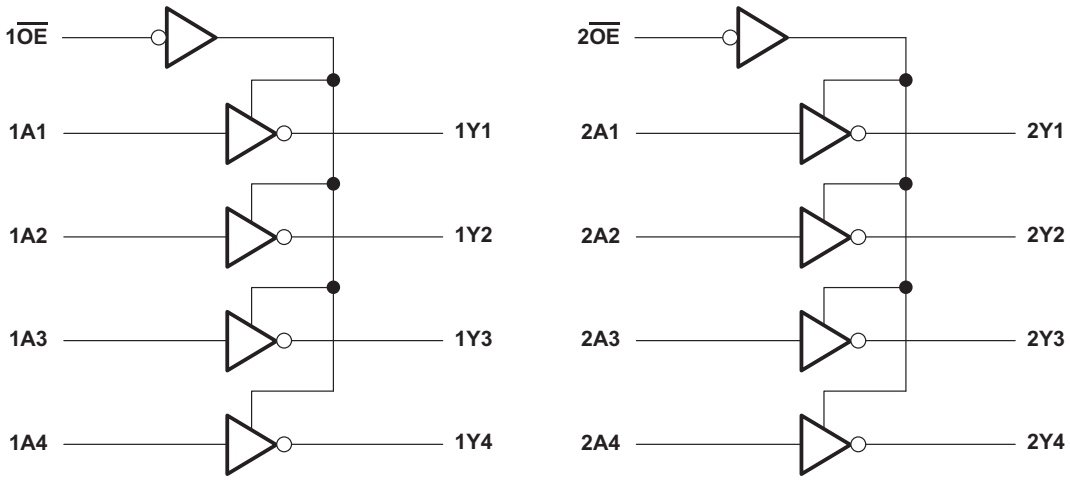
The SNx4AHCT240 octal buffers/drivers are designed specifically to improve both the performance and density of tri-state memory-address drivers, clock drivers, and bus-oriented receivers and transmitters.

**Device Information(1)**

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| SN74AHCT240DB | SSOP (20) | 7.50 mm × 5.30 mm |
| SN74AHCT240NS | SO (20) | 12.60 mm × 5.30 mm |
| SN74AHCT240PW | TSSOP (20) | 6.50 mm × 4.40 mm |
| SN74AHCT240DW | SOIC (20) | 12.80 mm × 7.50 mm |
| SN74AHCT240N | PDIP (20) | 25.40 mm × 6.35 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

**Simplified Schematic**




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An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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# 4 Revision History

**Changes from Revision M (April 2016) to Revision N** — **Page**

- Added junction temperature to *Absolute Maximum Ratings* table ... 4
- Moved storage temperature from *ESD Ratings* table to *Absolute Maximum Ratings* table ... 4
- Changed the *Function* table layout ... 10

**Changes from Revision L (October 2014) to Revision M** — **Page**

- Changed *Handling Ratings* table title to *ESD Ratings* ... 4
- Added –40°C to 85°C to SN74AHCT240 header in *Electrical Characteristics* table ... 5
- Added –40°C to 85°C to SN74AHCT240 header in *Switching Characteristics* table ... 6

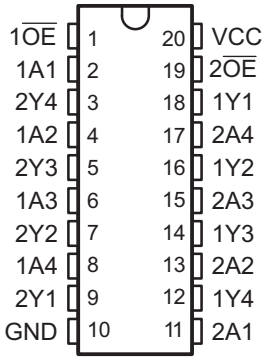
**Changes from Revision K (July 2003) to Revision L** — **Page**

- Updated document to new TI data sheet format. ... 1
- Deleted Ordering Information table. ... 1
- Added Military Disclaimer to Features list. ... 1
- Added Applications. ... 1
- Extended operating temperature range to 125°C ... 5
- Added *Thermal Information* table ... 5
- Added –40°C to 125°C for SN74AHCT240 in the Electrical Specifications table. ... 5
- Added –40°C to 125°C for SN74AHCT240 in the Switching Characteristics table. ... 6
- Added Detailed Description section ... 10
- Added *Application and Implementation* section ... 11
- Added Power Supply Recommendations and Layout sections. ... 12

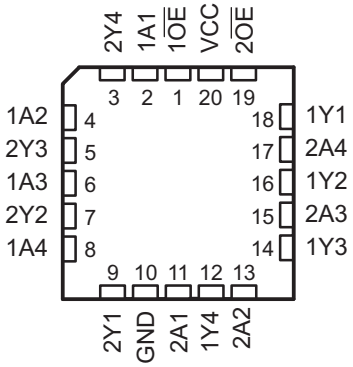

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# 5 Pin Configuration and Functions

**SN54AHCT240, J or W Package**
**SN74AHCT240, DB, DGV, DW, N, NS, or PW Package (20) Pin**
**Top View**




**SN54AHCT240 FK Package (20) Pin**
**Top View**




**Pin Functions**

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| 1$\overline{OE}$ | 1 | I | Output Enable 1 |
| 1A1 | 2 | I | 1A1 Input |
| 2Y4 | 3 | O | 2Y4 Output |
| 1A2 | 4 | I | 1A2 Input |
| 2Y3 | 5 | O | 2Y3 Output |
| 1A3 | 6 | I | 1A3 Input |
| 2Y2 | 7 | O | 2Y2 Output |
| 1A4 | 8 | I | 1A4 Input |
| 2Y1 | 9 | O | 2Y1 Output |
| GND | 10 | — | Ground Pin |
| 2A1 | 11 | I | 2A1 Input |
| 1Y4 | 12 | O | 1Y4 Output |
| 2A2 | 13 | I | 2A2 Input |
| 1Y3 | 14 | O | 1Y3 Output |
| 2A3 | 15 | I | 2A3 Input |
| 1Y2 | 16 | O | 1Y2 Output |
| 2A4 | 17 | I | 2A4 Input |
| 1Y1 | 18 | O | 1Y1 Output |
| 2$\overline{OE}$ | 19 | I | Output Enable 2 |
| VCC | 20 | — | Power Pin |

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# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Supply voltage, $V_{CC}$ | | –0.5 | 7 | V |
| Input voltage, $V_I$(2) | | –0.5 | 7 | V |
| Output voltage, $V_O$(2) | | –0.5 | $V_{CC}$ + 0.5 | V |
| Input clamp current, $I_{IK}$ | $V_I$ < 0 | | –20 | mA |
| Output clamp current, $I_{OK}$ | $V_O$ < 0 or $V_O$ > $V_{CC}$ | | ±20 | mA |
| Continuous output current, $I_O$ | $V_O$ = 0 to $V_{CC}$ | | ±25 | mA |
| Continuous current through $V_{CC}$ or GND | | | ±75 | mA |
| Junction temperature, $T_J$ | | | 150 | °C |
| Storage temperature, $T_{stg}$ | | –65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

## 6.2 ESD Ratings

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1) | 0 | 1000 | V |
| | | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2) | 0 | 2000 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.


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## 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

| | | SN54AHCT240 | | SN74AHCT240 | | UNIT |
|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | 4.5 | 5.5 | 4.5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | 2 | | V |
| $V_{IL}$ | Low-level Input voltage | | 0.8 | | 0.8 | V |
| $V_I$ | Input voltage | 0 | 5.5 | 0 | 5.5 | V |
| $V_O$ | Output voltage | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | | –8 | | –8 | mA |
| $I_{OL}$ | Low-level output current | | 8 | | 8 | mA |
| $T_A$ | Operating free-air temperature | –55 | 125 | –40 | 125 | °C |

(1) All unused inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. See the *Implications of Slow or Floating CMOS Inputs* application report.

## 6.4 Thermal Information

| THERMAL METRIC(1) | | SN74AHCT240 | | | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | DW | DB | N | NS | PW | |
| | | 20 PINS | 20 PINS | 20 PINS | 20 PINS | 20 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 83.0 | 99.9 | 54.9 | 80.4 | 105.4 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 48.9 | 61.7 | 41.7 | 46.9 | 39.5 | |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 50.5 | 55.2 | 35.8 | 47.9 | 56.4 | |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 21.1 | 22.6 | 27.9 | 19.9 | 3.1 | |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 50.1 | 54.8 | 35.7 | 47.5 | 55.8 | |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report.

## 6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $T_A$ = 25°C | | | SN54AHCT240 | | –40°C to 85°C SN74AHCT240 | | –40°C to 125°C SN74AHCT240 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $V_{OH}$ | High-level output voltage | $I_{OH}$ = –50 µA, $V_{CC}$ = 4.5 V | 4.4 | 4.5 | | 4.4 | | 4.4 | | 4.4 | | V |
| | | $I_{OH}$ = –8 mA, $V_{CC}$ = 4.5 V | 3.94 | | | 3.8 | | 3.8 | | 3.8 | | |
| $V_{OL}$ | Low-level output voltage | $I_{OL}$ = 50 µA, $V_{CC}$ = 4.5 V | | | 0.1 | | 0.1 | | 0.1 | | 0.1 | V |
| | | $I_{OL}$ = 8 mA, $V_{CC}$ = 4.5 V | | | 0.36 | | 0.44 | | 0.44 | | 0.44 | |
| $I_{OZ}$ | High-impedance-state output current | $V_O$ = $V_{CC}$ or GND<br>$V_{CC}$ = 5.5 V | | | ±0.25 | | ±2.5 | | ±2.5 | | ±2.5 | µA |
| $I_I$ | Inflection-point current | $V_I$ = 5.5 V or GND<br>$V_{CC}$ = 0 V to 5.5 V | | | ±0.1 | | ±1(1) | | ±1 | | ±1 | µA |
| $I_{CC}$ | Supply current | $V_I$ = $V_{CC}$ or GND<br>$I_O$ = 0,$V_{CC}$ = 5.5 V | | | 4 | | 40 | | 40 | | 40 | µA |
| $\Delta I_{CC}$(2) | Supply current change | One input at 3.4 V other inputs at $V_{CC}$ or GND<br>$V_{CC}$ = 5.5 V | | | 1.35 | | 1.5 | | 1.5 | | 1.5 | mA |
| $C_i$ | Input capacitance | $V_I$ = $V_{CC}$ or GND<br>$V_{CC}$ = 5.5 V | | 2.5 | 10 | | | | 10 | | 10 | pF |
| $C_o$ | Output capacitance | $V_O$ = $V_{CC}$ or GND<br>$V_{CC}$ = 5.5 V | | 3 | | | | | | | | pF |

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested at $V_{CC}$ = 0 V.
(2) This is the increase in supply current for each input at one of the specified TTL voltage levels, rather than 0 V or $V_{CC}$.

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## 6.6 Switching Characteristics

over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see *Parameter Measurement Information* section)

| PARAMETER | | TEST CONDITIONS | | $T_A$ = 25°C | | SN54AHCT240 | | –40°C to 85°C SN74AHCT240 | | –40°C to 125°C SN74AHCT240 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | TYP | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_{PLH}$ | Propagation delay time (low-to-high output) | A-to-Y | $C_L$ = 15 pF | 5.4(1) | 7.4(1) | 1(1) | 8.5(1) | 1 | 8.5 | 1 | 9.5 | ns |
| $t_{PHL}$ | Propagation delay time (high-to-low output) | | | 5.4(1) | 7.4(1) | 1(1) | 8.5(1) | 1 | 8.5 | 1 | 9.5 | |
| $t_{PZH}$ | Enable time (to the high level) | $\overline{OE}$-to-Y | $C_L$ = 15 pF | 7.7(1) | 10.4(1) | 1(1) | 12(1) | 1 | 12 | 1 | 13 | ns |
| $t_{PZL}$ | Enable time (to the low level) | | | 7.7(1) | 10.4(1) | 1(1) | 12(1) | 1 | 12 | 1 | 13 | |
| $t_{PHZ}$ | Disable time (from high level) | $\overline{OE}$-to-Y | $C_L$ = 15 pF | 8.3(1) | 10.4(1) | 1(1) | 12(1) | 1 | 12 | 1 | 13 | ns |
| $t_{PLZ}$ | Disable time (from low level) | | | 8.3(1) | 10.4(1) | 1(1) | 12(1) | 1 | 12 | 1 | 13 | |
| $t_{PLH}$ | Propagation delay time (low-to-high output) | A-to-Y | $C_L$ = 50 pF | 5.9 | 8.4 | 1 | 9.5 | 1 | 9.5 | 1 | 10.5 | ns |
| $t_{PHL}$ | Propagation delay time (high-to-low output) | | | 5.9 | 8.4 | 1 | 9.5 | 1 | 9.5 | 1 | 10.5 | |
| $t_{PZH}$ | Enable time (to the high level) | $\overline{OE}$-to-Y | $C_L$ = 50 pF | 8.2 | 11.4 | 1 | 13 | 1 | 13 | 1 | 14 | ns |
| $t_{PZL}$ | Enable time (to the low level) | | | 8.2 | 11.4 | 1 | 13 | 1 | 13 | 1 | 14 | |
| $t_{PHZ}$ | Disable time (from high level) | $\overline{OE}$-to-Y | $C_L$ = 50 pF | 8.8 | 11.4 | 1 | 13 | 1 | 13 | 1 | 14 | ns |
| $t_{PLZ}$ | Disable time (from low level) | | | 8.8 | 11.4 | 1 | 13 | 1 | 13 | 1 | 14 | |
| $t_{sk(o)}$ | Skew (time), output | | $C_L$ = 50 pF | | 1(2) | | 1 | | 1 | | 1 | ns |

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.
(2) On products compliant to MIL-PRF-38535, this parameter does not apply.

## 6.7 Noise Characteristics

$V_{CC}$ = 5 V, $C_L$ = 50 pF, $T_A$ = 25°C(1)

| PARAMETER | | SN74AHCT240 | | | UNIT |
|---|---|---|---|---|---|
| | | MIN | TYP | MAX | |
| $V_{OH(V)}$ | Quiet output, minimum dynamic $V_{OH}$ | | 4.1 | | V |
| $V_{IH(D)}$ | High-level dynamic input voltage | 2 | | | V |
| $V_{IL(D)}$ | Low-level dynamic input voltage | | | 0.8 | V |

(1) Characteristics are for surface-mount packages only.

## 6.8 Operating Characteristics

$V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | TYP | UNIT |
|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | No load, f = 1 MHz | 10 | pF |


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# 7 Typical Characteristics

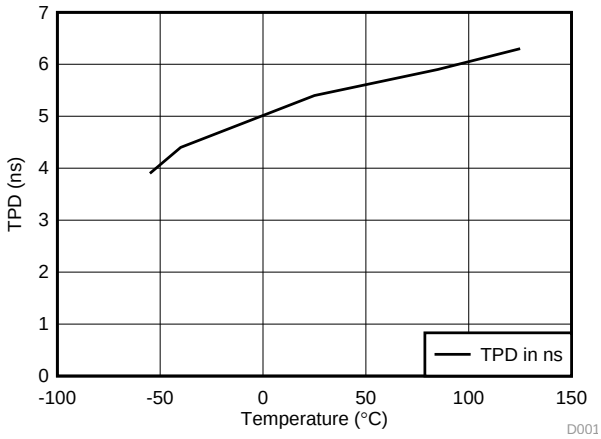



**Figure 1. TPD vs Temperature**

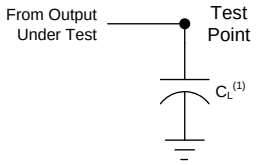
## 8 Parameter Measurement Information

Unless otherwise noted, all input pulses are supplied by generators having the following characteristics:

- PRR ≤ 1 MHz
- $Z_O$ = 50 Ω
- $t_r$ ≤ 3 ns
- $t_f$ ≤ 3 ns

**NOTE**

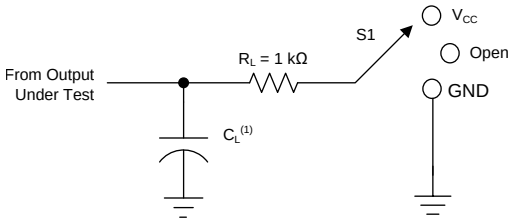
All parameters and waveforms are not applicable to all devices.




(1) $C_L$ includes probe and jig capacitance.

(2) The outputs are measured one at a time, with one transition per measurement.

**Figure 2. Load Circuit For Totem-Pole Outputs**




(1) $C_L$ includes probe and jig capacitance.

(2) The outputs are measured one at a time, with one transition per measurement.

**Figure 3. Load Circuit For Tri-State And Open-Drain Outputs**

**Table 1. Loading Conditions For Parameter**

| TEST | S1 |
|---|---|
| $t_{PLH}$(1), $t_{PHL}$(1) | Open |
| $t_{PLZ}$(2), $t_{PZL}$(3) | $V_{CC}$ |
| $t_{PHZ}$(2), $t_{PZH}$(3) | GND |
| Open drain | $V_{CC}$ |

(1) $t_{PLH}$ and $t_{PHL}$ are the same as $t_{pd}$.
(2) $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{dis}$.
(3) $t_{PZL}$ and $t_{PZH}$ are the same as $t_{en}$.

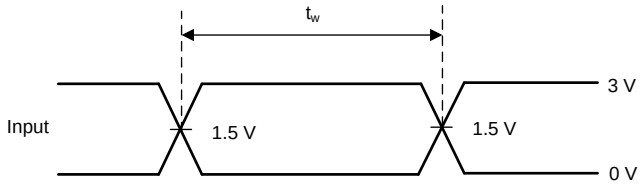
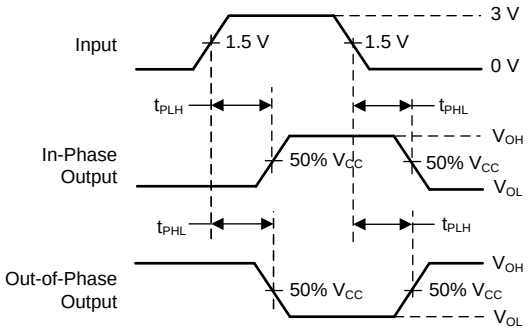



**Figure 4. Voltage Waveforms Pulse Durations**


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(1) The outputs are measured one at a time, with one transition per measurement.

**Figure 5. Voltage Waveforms Propagation Delay Times Inverting and Noninverting Outputs**

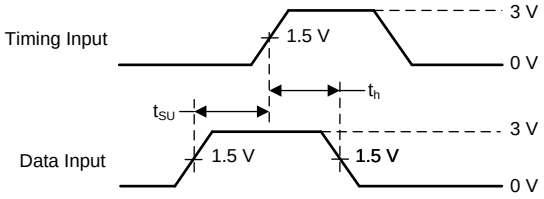
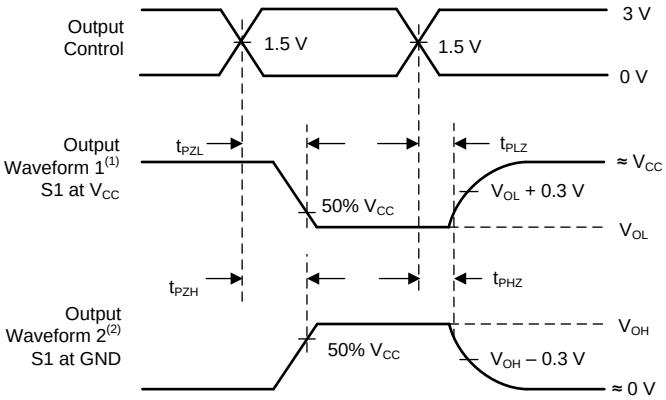



**Figure 6. Voltage Waveforms Setup And Hold Times**




(1) Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control.

(2) Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.

(3) The outputs are measured one at a time, with one transition per measurement.

**Figure 7. Votlage Waveforms Enable And Disable Times Low- and High-Level Enabling**

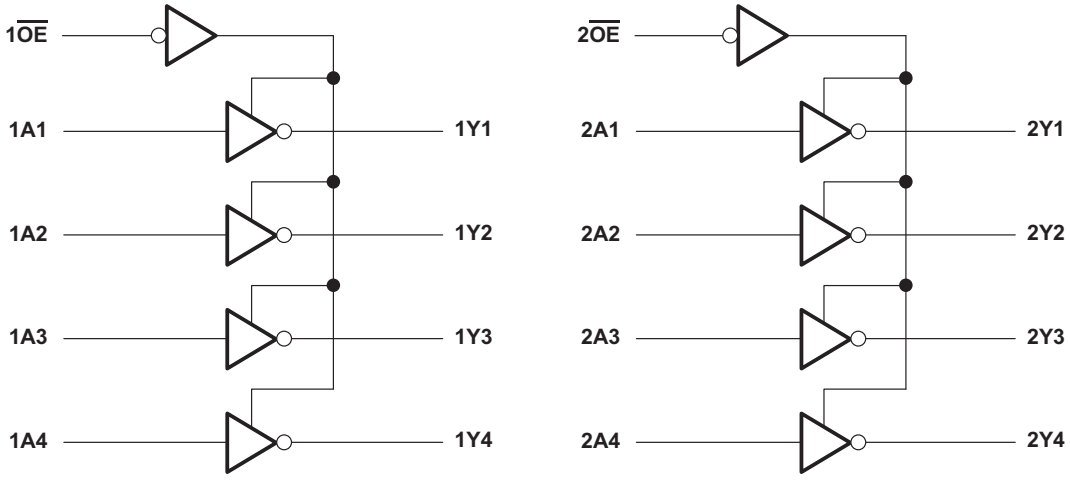
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# 9 Detailed Description

## 9.1 Overview

The SN74AHCT240 devices are organized as two 4-bit buffers/line drivers with separate output-enable ($\overline{OE}$) inputs. When $\overline{OE}$ is low, the device passes inverted data from the A inputs to the Y outputs. When $\overline{OE}$ is high, the outputs are in the high-impedance state. To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to $V_{CC}$ through a pull-up resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

## 9.2 Functional Block Diagram




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## 9.3 Feature Description

- $V_{CC}$ is optimized at 5 V
- Allows up-voltage translation from 3.3 V to 5 V
  - Inputs accept $V_{IH}$ levels of 2 V
- Slow edge rates minimize output ringing
- Inputs are TTL-voltage compatible

## 9.4 Device Functional Modes

**Table 2. Function Table (Each 4-bit Inverting Buffer/Driver)**

| INPUTS | | OUTPUT |
|---|---|---|
| $\overline{OE}$ | A | Y |
| L | H | L |
| L | L | H |
| H | X | Z |


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# 10 Application and Implementation

**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 10.1 Application Information

The SNx4AHCT240 device is a low-drive CMOS device that may be used for a multitude of bus interface type applications where output ringing is a concern. The low drive and slow edge rates will minimize overshoot and undershoot on the outputs. The input switching levels have been lowered to accommodate TTL inputs of 0.8-V $V_{IL}$ and 2-V $V_{IH}$. This feature makes the SNx4AHCT240 device ideal for translating up from 3.3 V to 5 V. Figure 8 shows this type of translation.

## 10.2 Typical Application

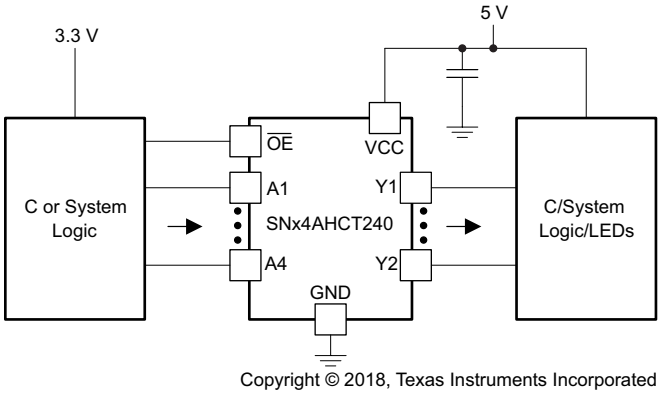



**Figure 8. Application Diagram**

### 10.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads; therefore, routing and load conditions should be considered to prevent ringing.

### 10.2.2 Detailed Design Procedure

1. Recommended Input Conditions:
   - For rise time and fall time specifications, see $\Delta t/\Delta V$ in the *Recommended Operating Conditions* table.
   - For specified high and low levels, see $V_{IH}$ and $V_{IL}$ in the *Recommended Operating Conditions* table.
   - Inputs are overvoltage tolerant, allowing them to go as high as 5.5 V at any valid $V_{CC}$.
2. Recommend Output Conditions:
   - Load currents should not exceed 25 mA per output and 75 mA total for the part.
   - Outputs should not be pulled above $V_{CC}$.

## Typical Application (continued)

### 10.2.3 Application Curves

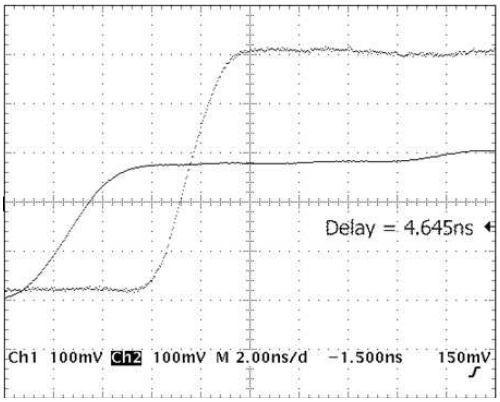



**Figure 9. Application Scope Capture**

## 11 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the *Recommended Operating Conditions*.

Each $V_{CC}$ terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1 μF capacitor is recommended. If there are multiple $V_{CC}$ terminals then 0.01 μF or 0.022 μF capacitors are recommended for each power terminal. It is ok to parallel multiple bypass capacitors to reject different frequencies of noise. 0.1 μF and 1.0 μF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for the best results.

## 12 Layout

### 12.1 Layout Guidelines

When using multiple bit logic devices, inputs should not float. In many cases, functions or parts of functions of digital logic devices are unused. Such examples are when only two inputs of a triple-input AND gate are used, or only 3 of the 4-buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states.

Specified in Figure 10 are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or $V_{CC}$, whichever makes more sense or is more convenient. It is acceptable to float outputs unless the part is a transceiver. If the transceiver has an output enable pin, it will disable the outputs section of the part when asserted. This will not disable the input section of the I/Os so they also cannot float when disabled.

### 12.2 Layout Example

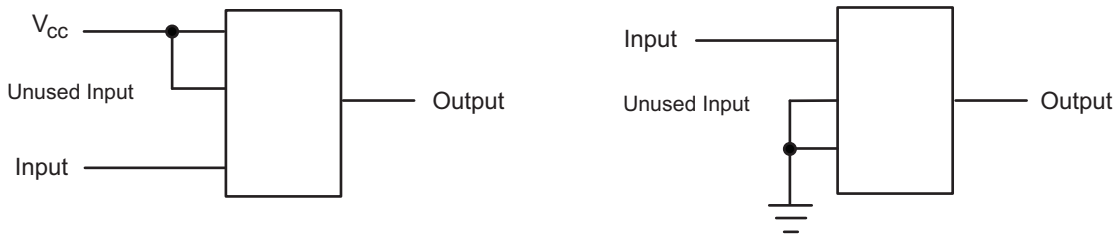



**Figure 10. Layout Diagram**


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# 13 Device and Documentation Support

## 13.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

**TI E2E™ Online Community** ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

## 13.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**Table 3. Related Links**

| PARTS | PRODUCT FOLDER | SAMPLE & BUY | TECHNICAL DOCUMENTS | TOOLS & SOFTWARE | SUPPORT & COMMUNITY |
|---|---|---|---|---|---|
| SN54AHCT240 | Click here | Click here | Click here | Click here | Click here |
| SN74AHCT240 | Click here | Click here | Click here | Click here | Click here |

## 13.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

## 13.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## 13.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

# 14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 5962-9680601Q2A | ACTIVE | LCCC | FK | 20 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-9680601Q2A SNJ54AHCT240FK | Samples |
| 5962-9680601QRA | ACTIVE | CDIP | J | 20 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-9680601QRA SNJ54AHCT240J | Samples |
| 5962-9680601QSA | ACTIVE | CFP | W | 20 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-9680601QSA SNJ54AHCT240W | Samples |
| SN74AHCT240DBR | ACTIVE | SSOP | DB | 20 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | HB240 | Samples |
| SN74AHCT240DW | ACTIVE | SOIC | DW | 20 | 25 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | AHCT240 | Samples |
| SN74AHCT240DWR | ACTIVE | SOIC | DW | 20 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | AHCT240 | Samples |
| SN74AHCT240N | ACTIVE | PDIP | N | 20 | 20 | RoHS & Non-Green | NIPDAU | N / A for Pkg Type | -40 to 125 | SN74AHCT240N | Samples |
| SN74AHCT240NSR | ACTIVE | SO | NS | 20 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | AHCT240 | Samples |
| SN74AHCT240PW | ACTIVE | TSSOP | PW | 20 | 70 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | HB240 | Samples |
| SN74AHCT240PWR | ACTIVE | TSSOP | PW | 20 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | HB240 | Samples |
| SN74AHCT240PWRG4 | ACTIVE | TSSOP | PW | 20 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | HB240 | Samples |
| SNJ54AHCT240FK | ACTIVE | LCCC | FK | 20 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-9680601Q2A SNJ54AHCT240FK | Samples |
| SNJ54AHCT240J | ACTIVE | CDIP | J | 20 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-9680601QRA SNJ54AHCT240J | Samples |
| SNJ54AHCT240W | ACTIVE | CFP | W | 20 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-9680601QSA SNJ54AHCT240W | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN54AHCT240, SN74AHCT240 :**

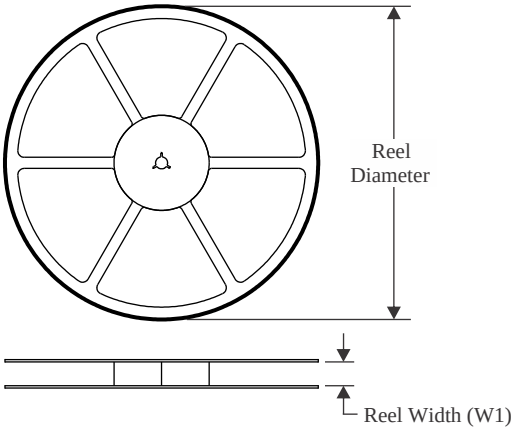
- Catalog : SN74AHCT240
- Automotive : SN74AHCT240-Q1, SN74AHCT240-Q1
- Military : SN54AHCT240

NOTE: Qualified Version Definitions:

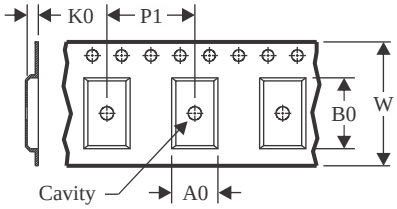
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Military - QML certified for Military and Defense Applications

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

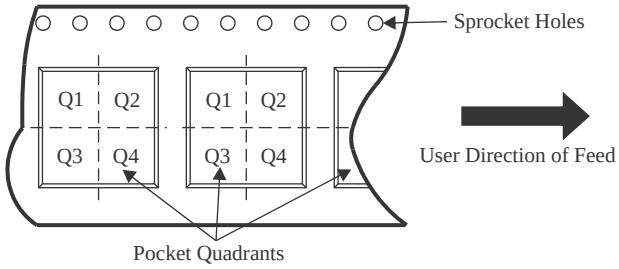



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

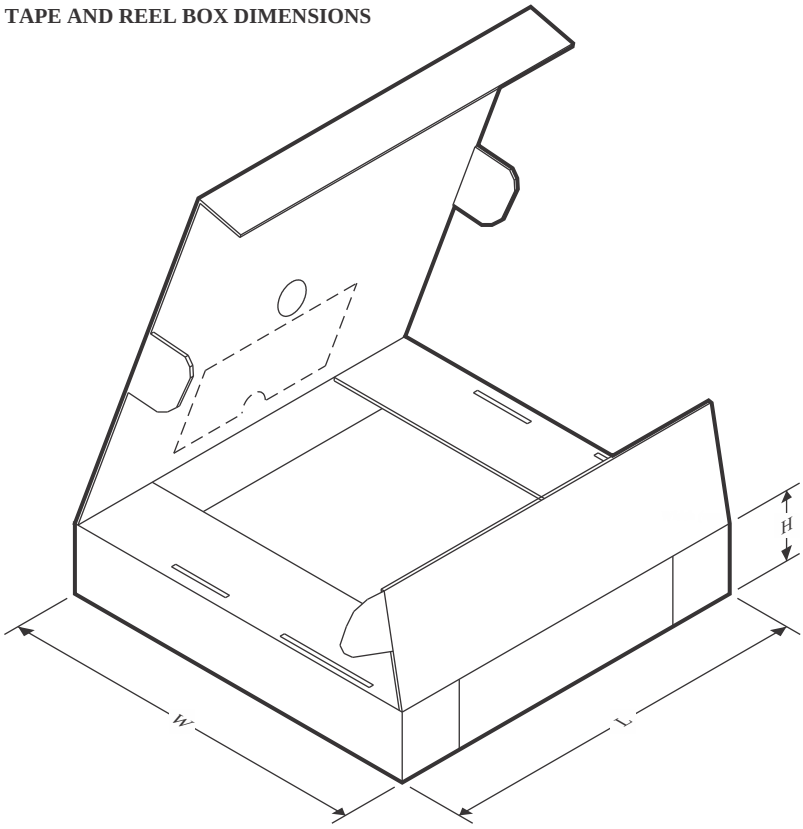
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74AHCT240DBR | SSOP | DB | 20 | 2000 | 330.0 | 16.4 | 8.2 | 7.5 | 2.5 | 12.0 | 16.0 | Q1 |
| SN74AHCT240DWR | SOIC | DW | 20 | 2000 | 330.0 | 24.4 | 10.8 | 13.3 | 2.7 | 12.0 | 24.0 | Q1 |
| SN74AHCT240NSR | SO | NS | 20 | 2000 | 330.0 | 24.4 | 8.4 | 13.0 | 2.5 | 12.0 | 24.0 | Q1 |
| SN74AHCT240PWR | TSSOP | PW | 20 | 2000 | 330.0 | 16.4 | 6.95 | 7.0 | 1.4 | 8.0 | 16.0 | Q1 |

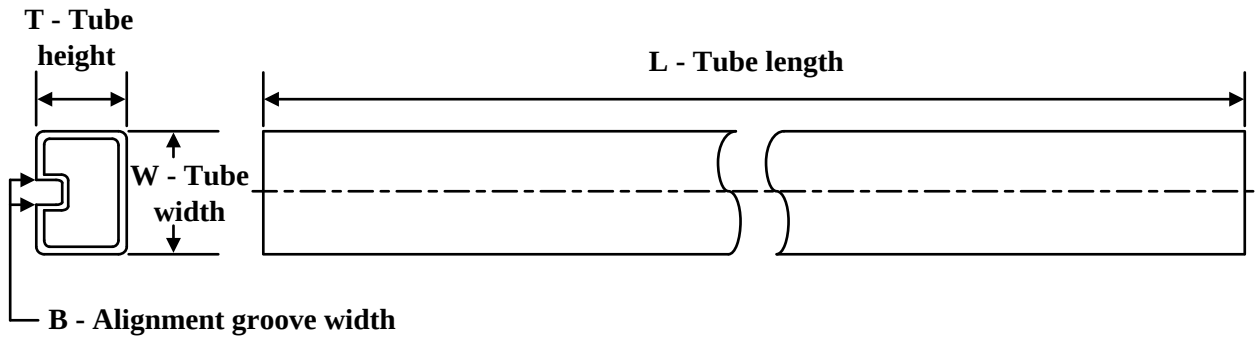
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SN74AHCT240DBR | SSOP | DB | 20 | 2000 | 356.0 | 356.0 | 35.0 |
| SN74AHCT240DWR | SOIC | DW | 20 | 2000 | 367.0 | 367.0 | 45.0 |
| SN74AHCT240NSR | SO | NS | 20 | 2000 | 367.0 | 367.0 | 45.0 |
| SN74AHCT240PWR | TSSOP | PW | 20 | 2000 | 356.0 | 356.0 | 35.0 |

## TUBE



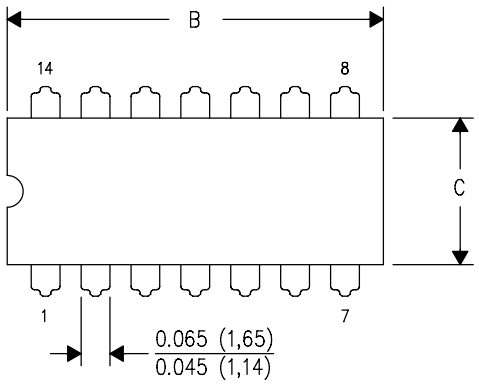

*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| 5962-9680601Q2A | FK | LCCC | 20 | 1 | 506.98 | 12.06 | 2030 | NA |
| 5962-9680601QSA | W | CFP | 20 | 1 | 506.98 | 26.16 | 6220 | NA |
| SN74AHCT240DW | DW | SOIC | 20 | 25 | 507 | 12.83 | 5080 | 6.6 |
| SN74AHCT240N | N | PDIP | 20 | 20 | 506 | 13.97 | 11230 | 4.32 |
| SN74AHCT240PW | PW | TSSOP | 20 | 70 | 530 | 10.2 | 3600 | 3.5 |
| SNJ54AHCT240FK | FK | LCCC | 20 | 1 | 506.98 | 12.06 | 2030 | NA |
| SNJ54AHCT240W | W | CFP | 20 | 1 | 506.98 | 26.16 | 6220 | NA |

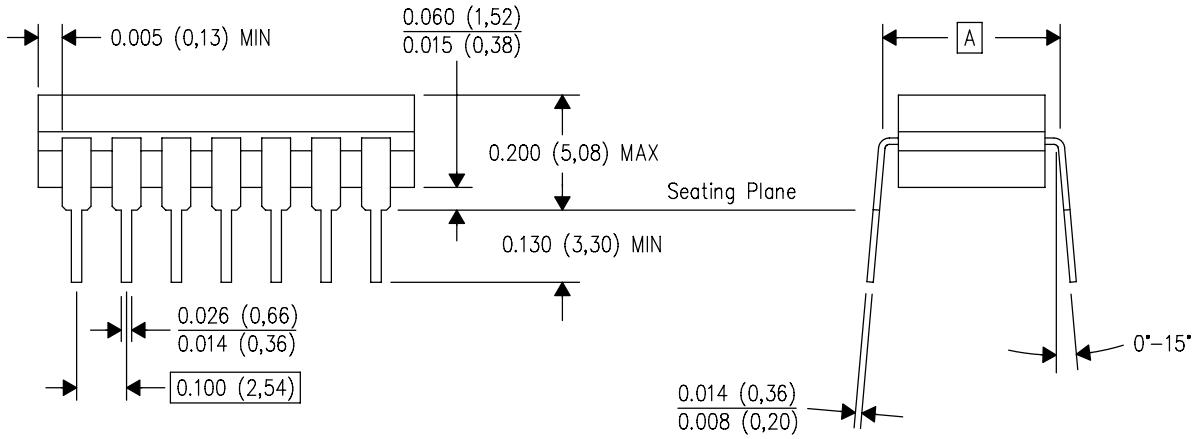
J (R–GDIP–T**)

14 LEADS SHOWN

# CERAMIC DUAL IN–LINE PACKAGE




| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |




4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

# GENERIC PACKAGE VIEW

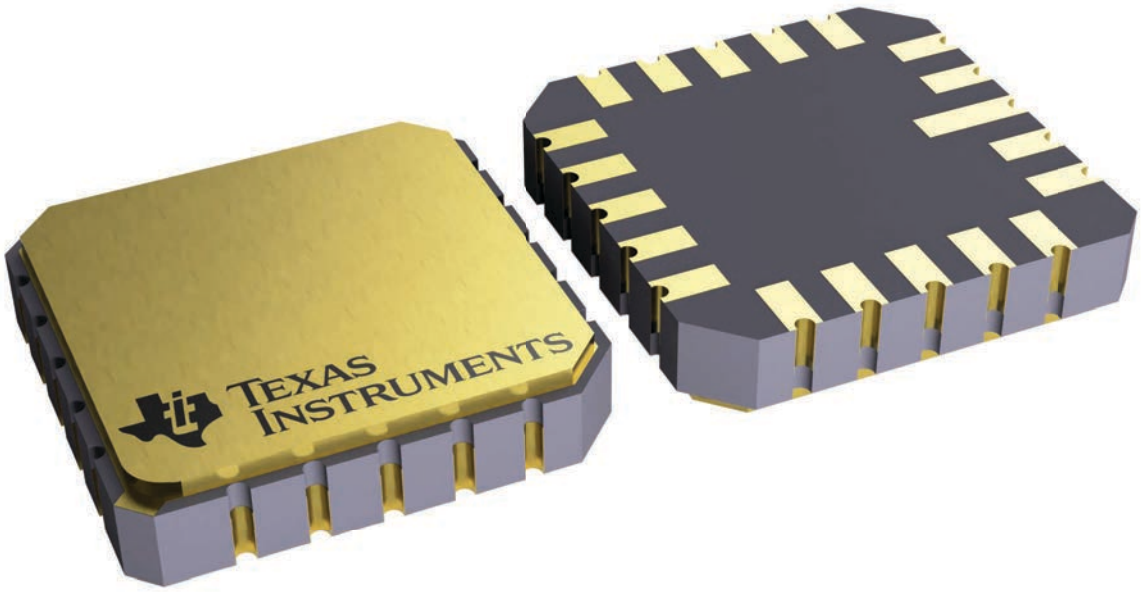
## FK 20

## LCCC - 2.03 mm max height

**8.89 x 8.89, 1.27 mm pitch**

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

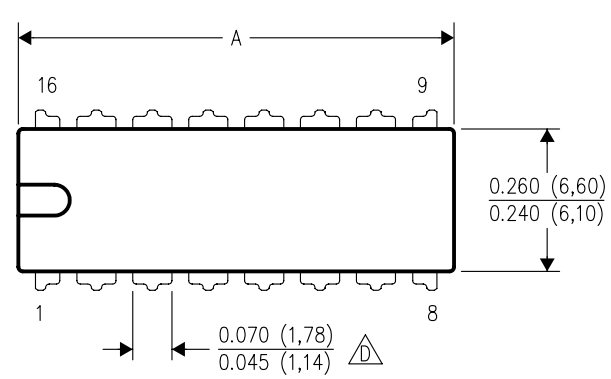



4229370VA\

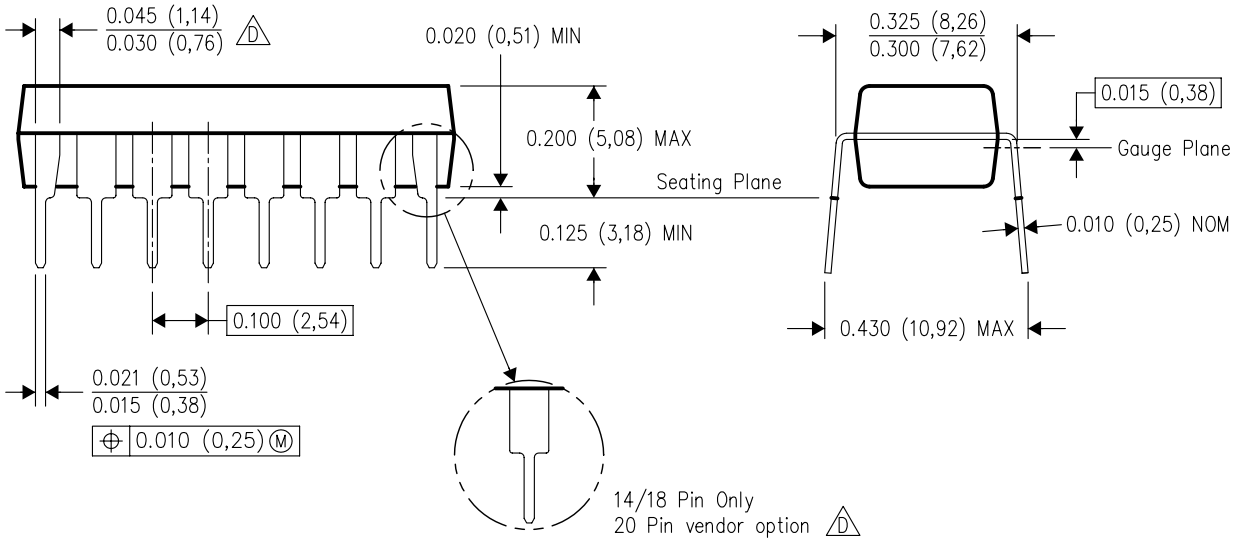
## N (R–PDIP–T**)

## PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN

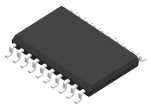



| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A MAX | 0.775 (19,69) | 0.775 (19,69) | 0.920 (23,37) | 1.060 (26,92) |
| A MIN | 0.745 (18,92) | 0.745 (18,92) | 0.850 (21,59) | 0.940 (23,88) |
| MS–001 VARIATION (C) | AA | BB | AC | AD |




4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

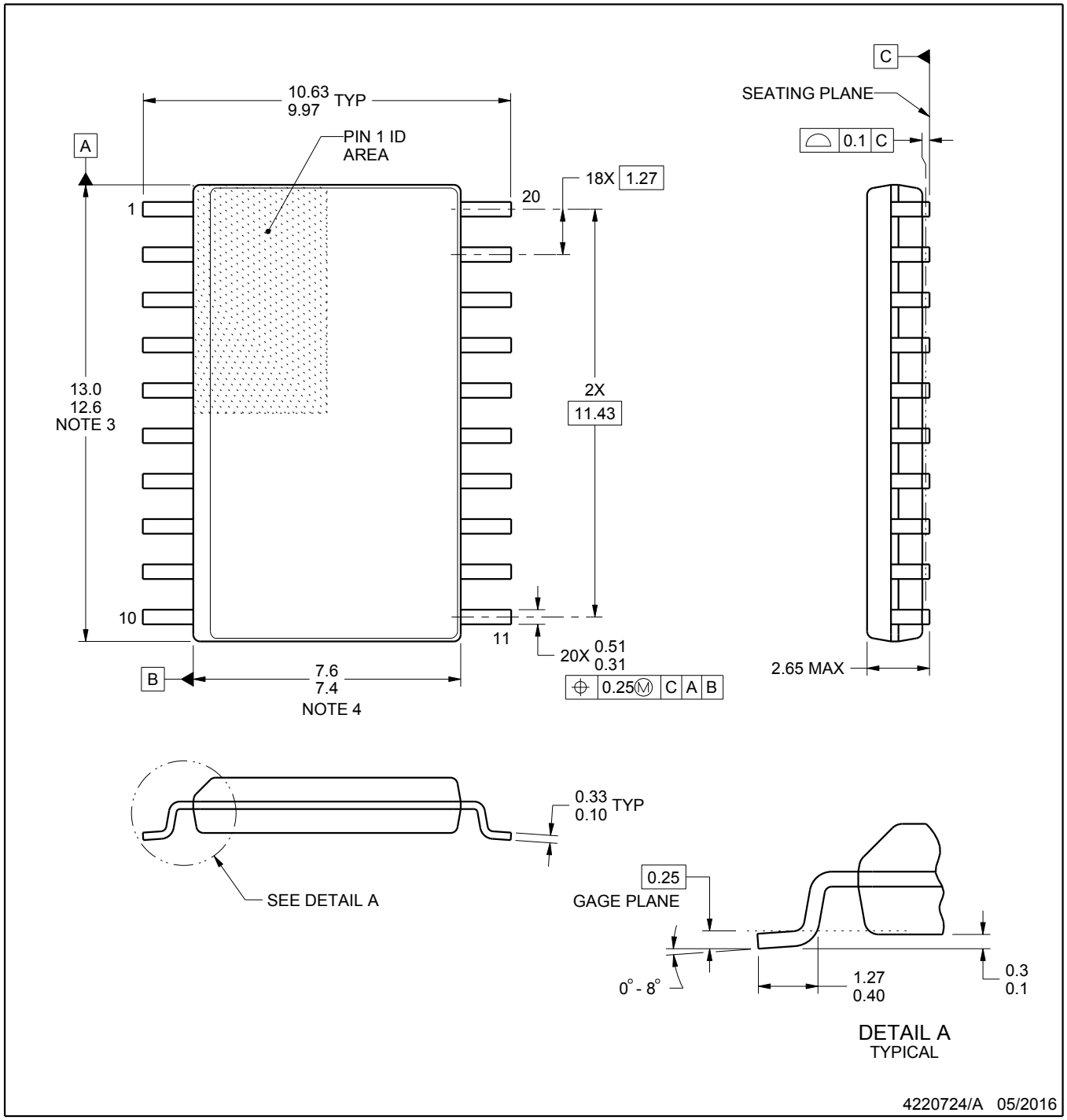


# PACKAGE OUTLINE

## DW0020A

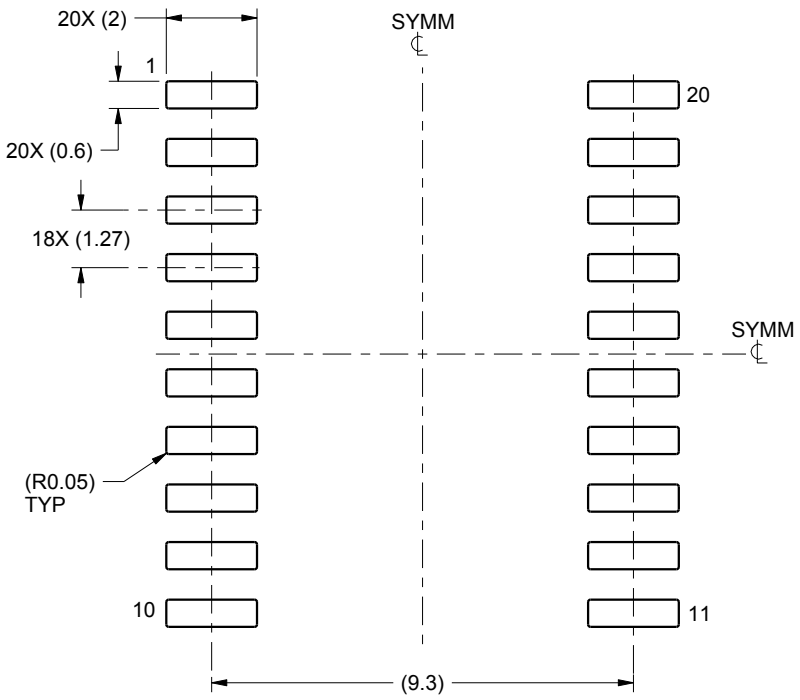
## SOIC - 2.65 mm max height

SOIC

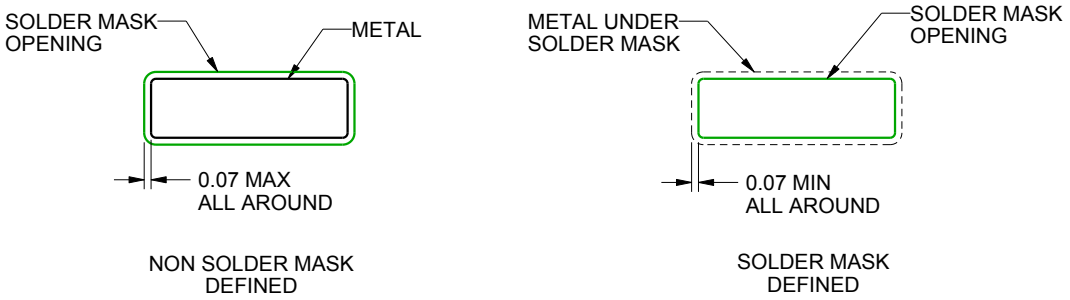



NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.




LAND PATTERN EXAMPLE
SCALE:6X

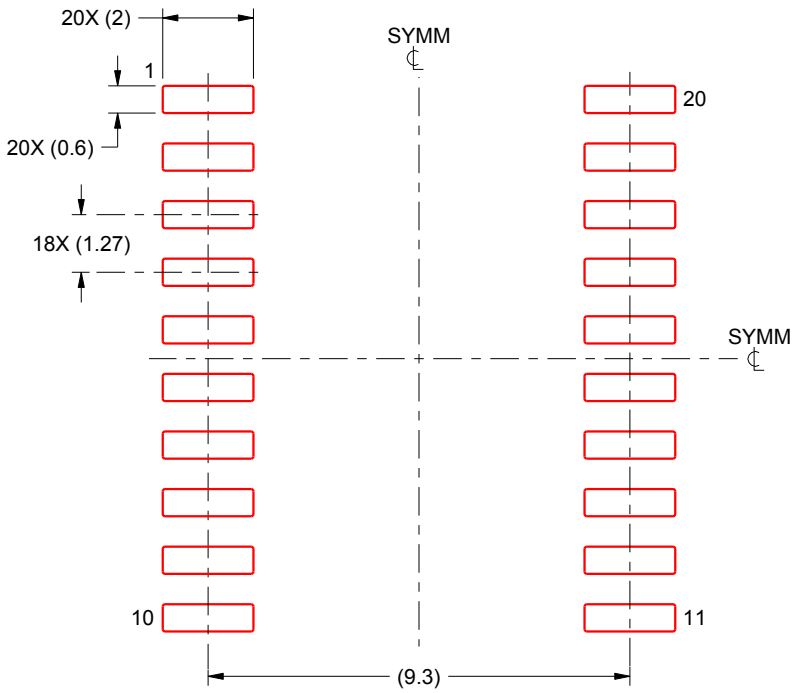



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



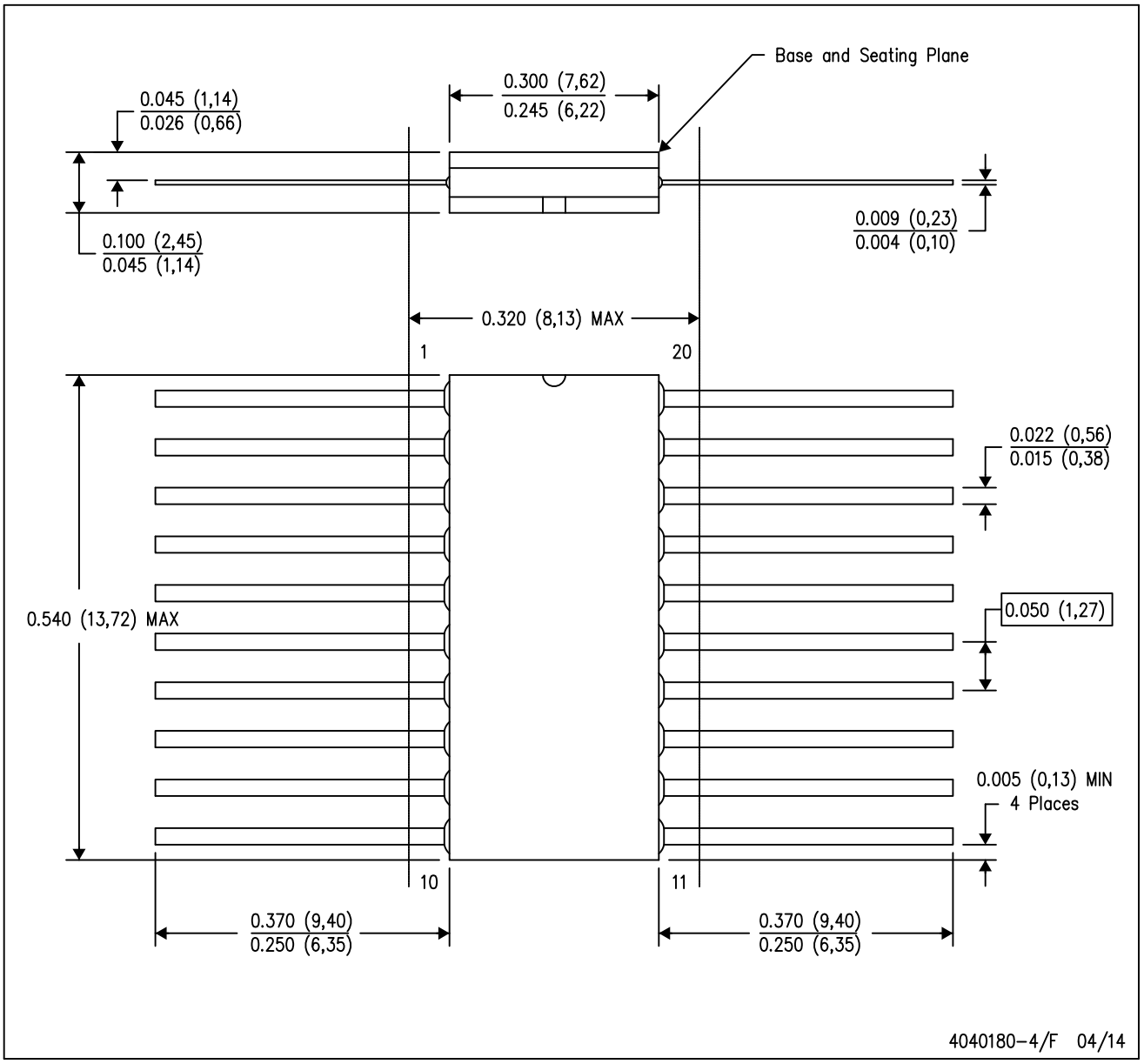

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

W (R–GDFP–F20) CERAMIC DUAL FLATPACK



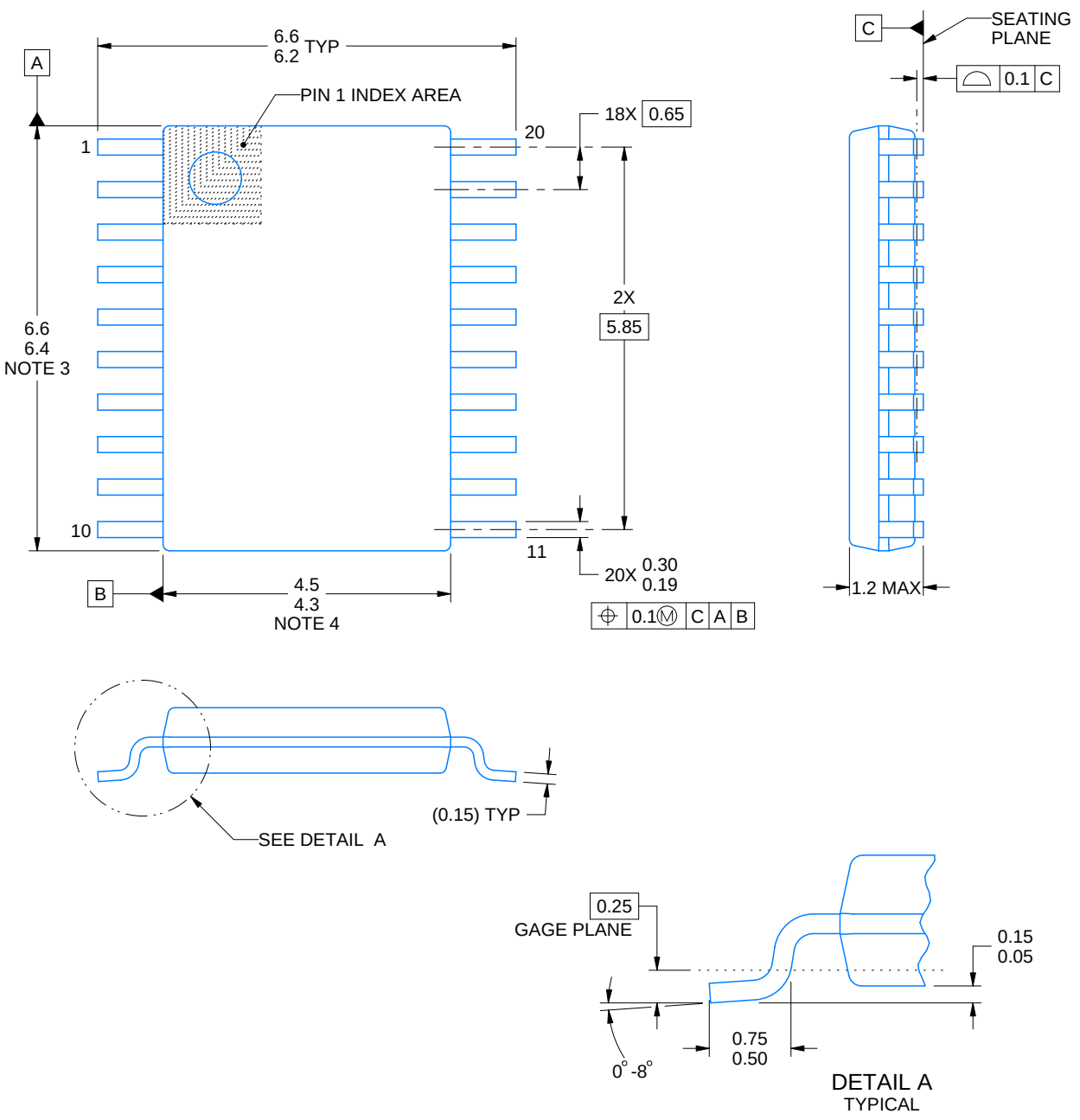

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within Mil–Std 1835 GDFP2–F20

# PACKAGE OUTLINE

## PW0020A

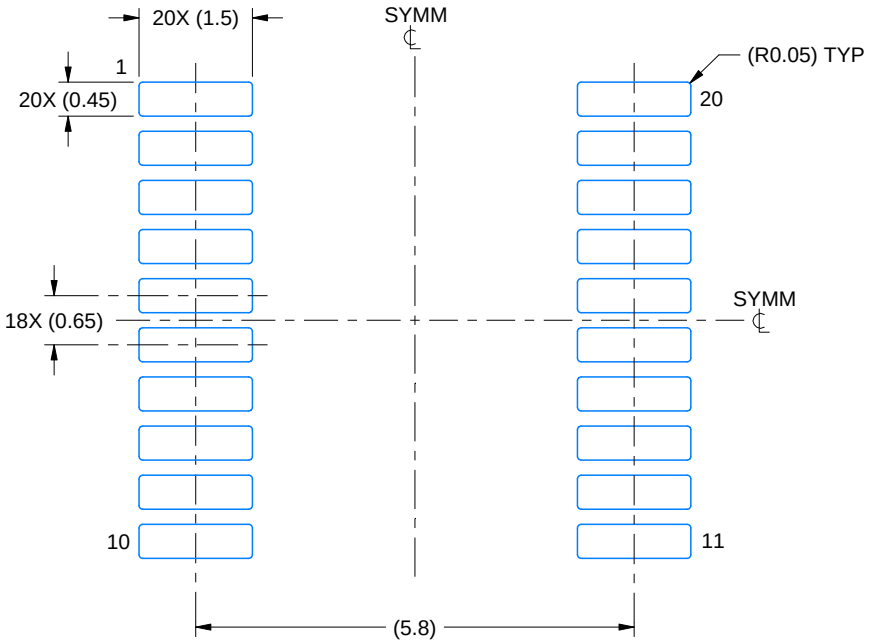
## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE




NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

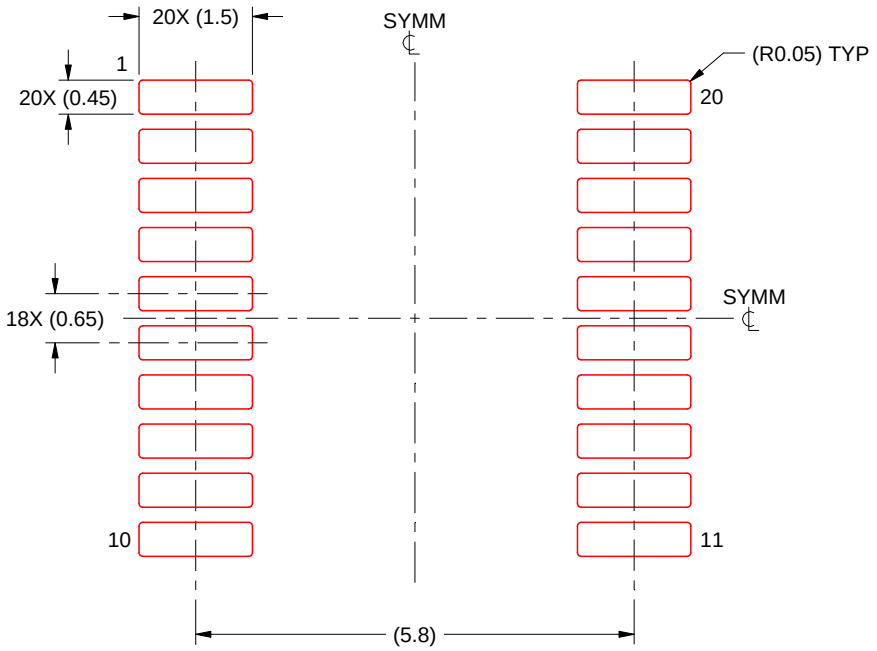



SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



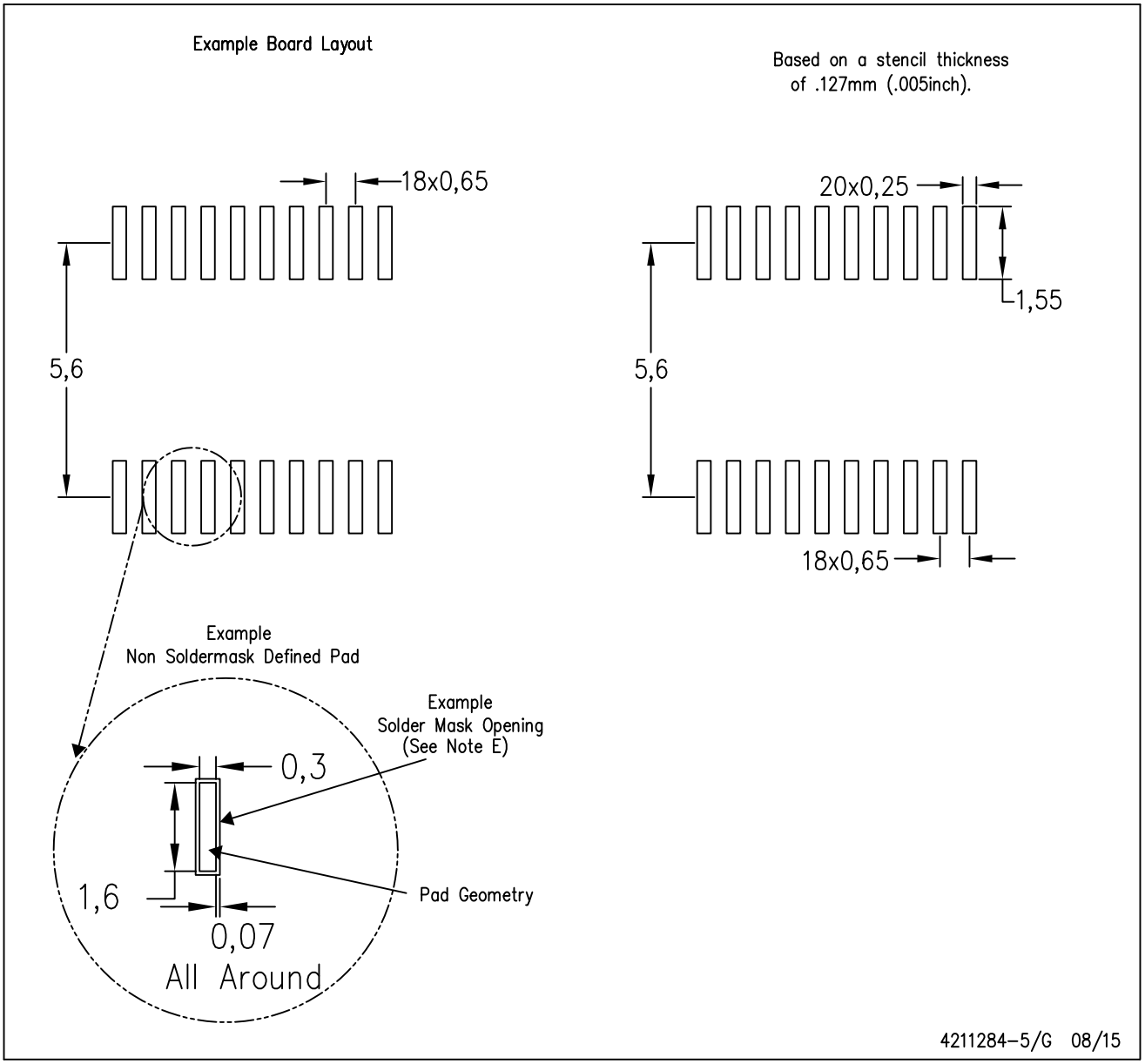

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PW (R–PDSO–G20) PLASTIC SMALL OUTLINE



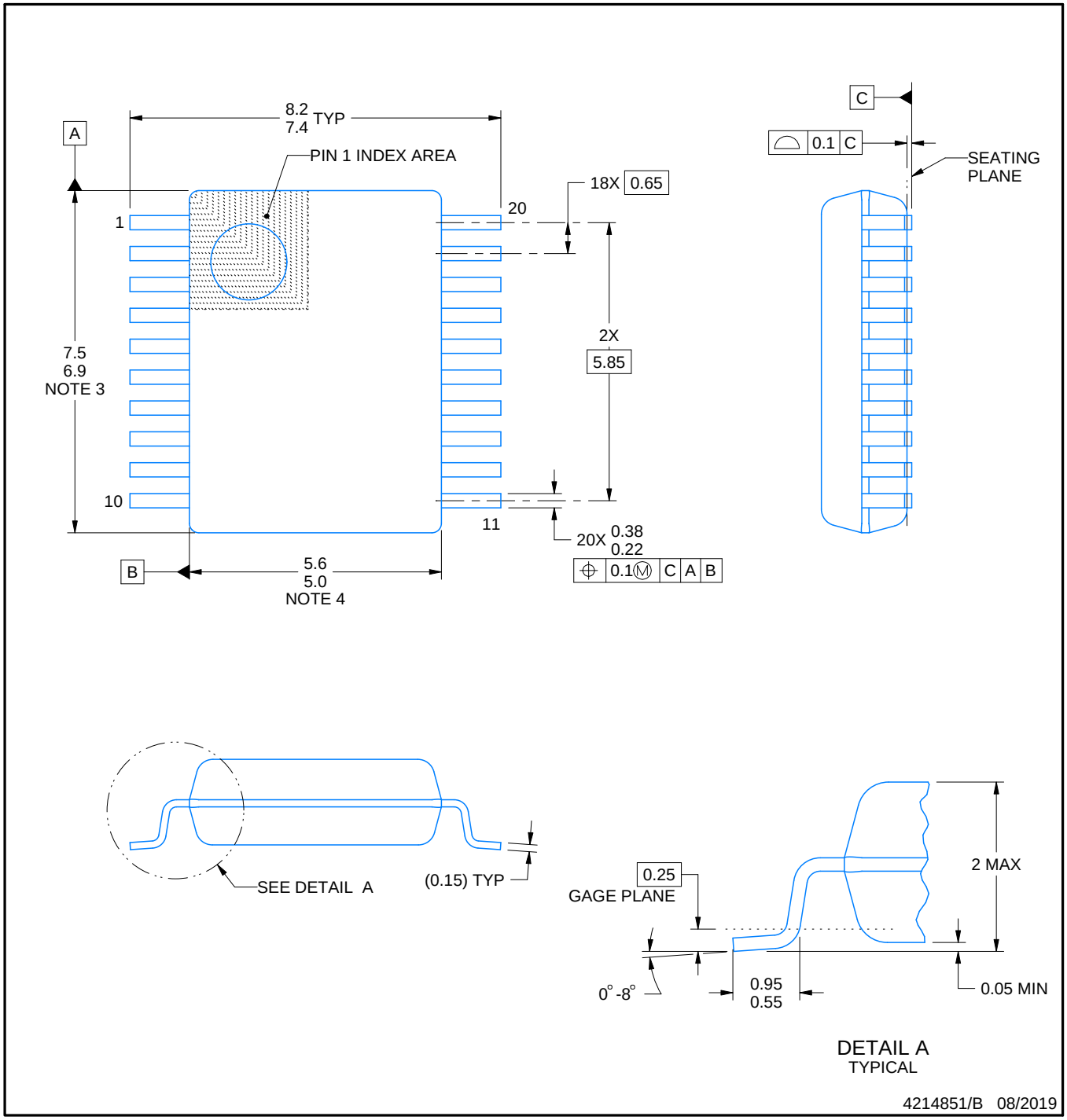

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

# PACKAGE OUTLINE

## DB0020A

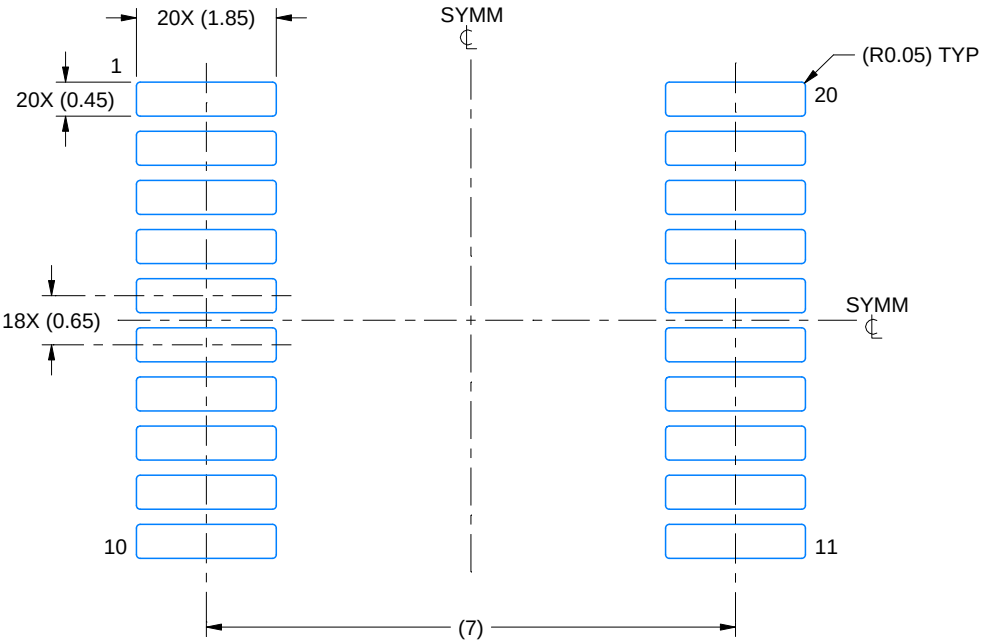
## SSOP - 2 mm max height

SMALL OUTLINE PACKAGE

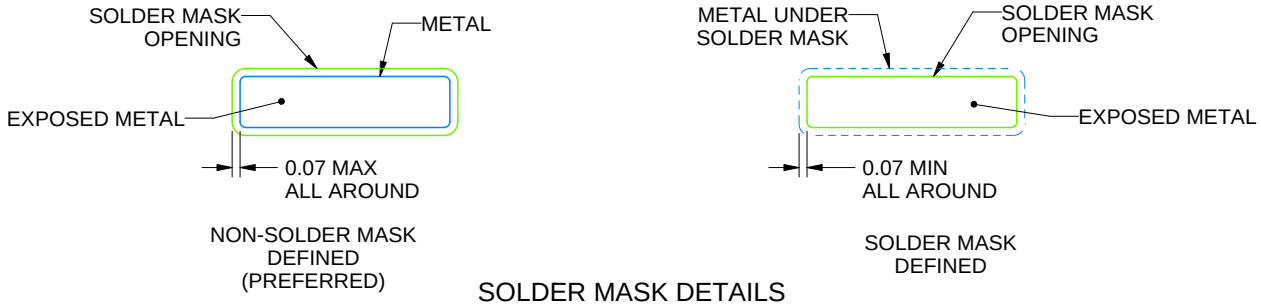



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X




SOLDER MASK DETAILS

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NOTES: (continued)

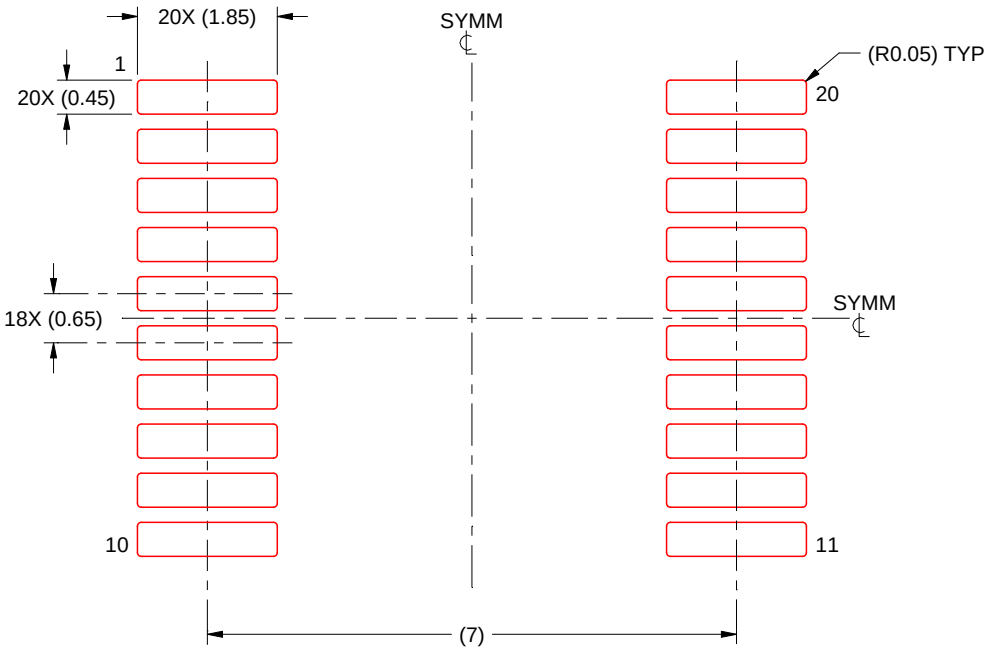
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

## DB0020A

## SSOP - 2 mm max height

SMALL OUTLINE PACKAGE




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

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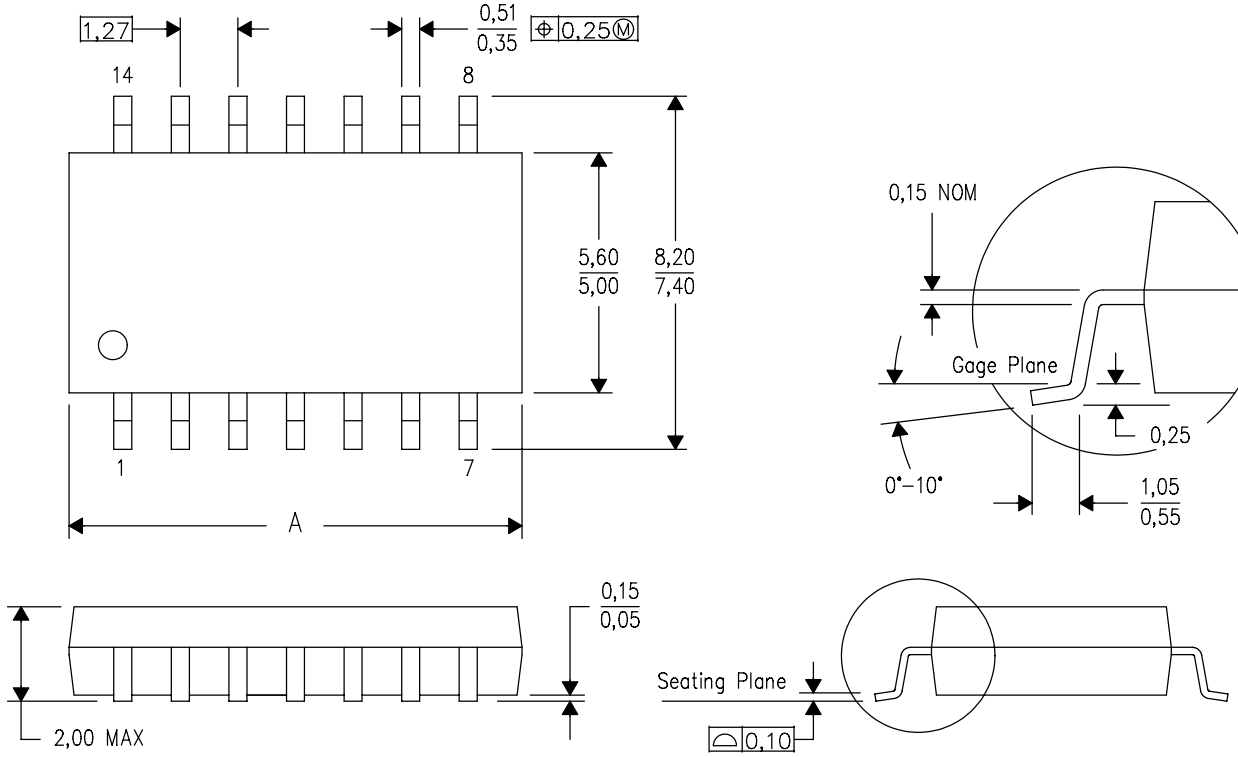
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## MECHANICAL DATA

**NS (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE PACKAGE**

**14-PINS SHOWN**




| DIM \ PINS ** | 14 | 16 | 20 | 24 |
|---|---|---|---|---|
| A MAX | 10,50 | 10,50 | 12,90 | 15,30 |
| A MIN | 9,90 | 9,90 | 12,30 | 14,70 |

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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