1 OUTPUT PCIE GEN1/2 SYNTHESIZER

IDT5V41064

Recommended Applications

One output synthesizer for PCIe Gen1/2

General Description

The IDT5V41064 is a PCIe Gen2 compliant spread spectrum capable clock generator. The device has 1 differential HCSL output and can be used in communication or embedded systems to substantially reduce electro-magnetic interference (EMI). Spread spectrum can be enabled via a select pin.

Output Features

- 1 - 0.7V current mode differential HCSL output pairs

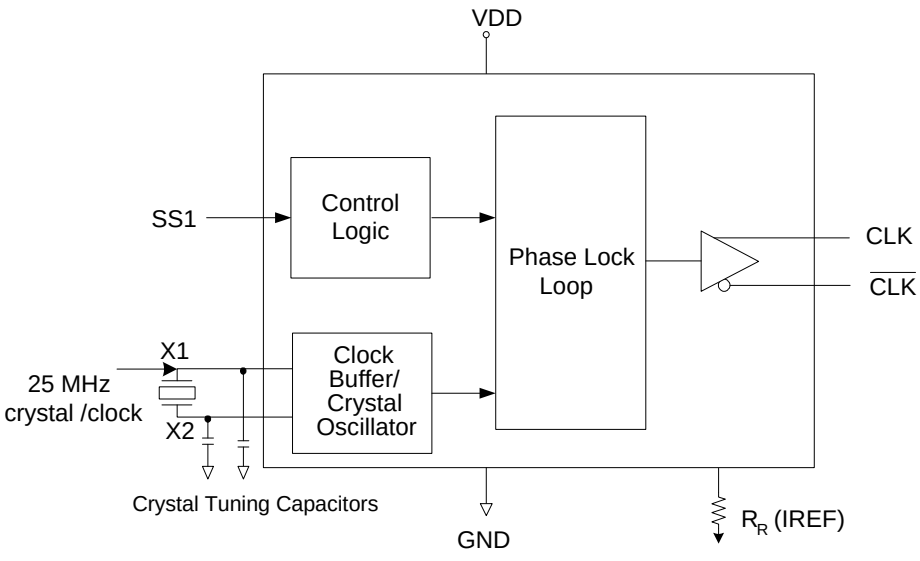
Features/Benefits

- 16-pin QFN package; very small board footprint
- Spread-spectrum capable; reduces EMI
- Outputs can be terminated to LVDS; can drive a wider variety of devices
- Spread enable via pin selection; no software required to configure device
- Industrial temperature range available; supports demanding embedded applications
- **For PCIe Gen3 applications, see the 5V41234**

Key Specifications

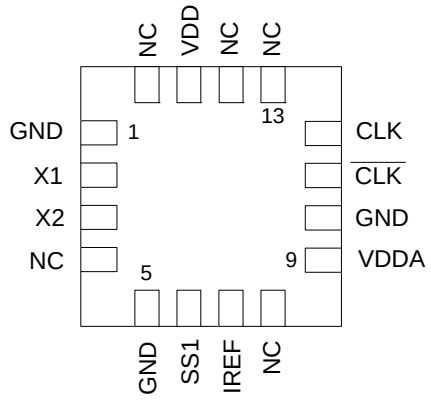
- Cycle-to-cycle jitter < 100 ps
- PCIe Gen2 phase jitter < 3.0ps RMS

Block Diagram



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Pin Assignment



16-pin QFN

Spread Spectrum Select Table

SS1	Spread%
0	-0.5% down
1	No spread

Pin Descriptions

Pin Number	Pin Name	Pin Type	Pin Description
1	GND	Power	Connect to ground.
2	X1	XI	Crystal or clock input. Connect to 25 MHz crystal or single-ended clock.
3	X2	XO	Crystal connection. Connect to parallel mode crystal. Leave floating if X1 is driven by single-ended clock.
4	NC	–	No connect.
5	GND	Power	Connect to ground.
6	SS1	Input	Spread Select 1. See table above. Internal pull-up resistor.
7	IREF	Output	475Ω precision resistor must be attached to this pin, which is connected to internal current source.
8	NC	–	No connect.
9	VDDA	Power	Connect to 3.3V and filter as analog supply.
10	GND	Power	Connect to ground.
11	$\overline{\text{CLK}}$	Output	HCSL complementary output clock.
12	CLK	Output	HCSL true output clock.
13	NC	–	No connect.
14	NC	–	No connect.
15	VDD	Power	Connect to 3.3 V for OSC and digital circuits.
16	NC	–	No connect.

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Applications Information

External Components

A minimum number of external components are required for proper operation.

Decoupling Capacitors

Decoupling capacitors of 0.01 μF should be connected between VDD and the ground plane (pin 4) as close to the VDD pin as possible. Do not share ground vias between components. Route power from power source through the capacitor pad and then into IDT pin.

Crystal

A 25 MHz fundamental mode parallel resonant crystal with C_L = 16 pF should be used. This crystal must have less than 300 ppm of error across temperature in order for the IDT5V41064 to meet PCI Express specifications.

Crystal Capacitors

Crystal capacitors are connected from pins X1 to ground and X2 to ground to optimize the accuracy of the output frequency.

C_L= Crystal's load capacitance in pF

Crystal Capacitors (pF) = (C_L- 8) * 2

For example, for a crystal with a 16 pF load cap, each external crystal cap would be 16 pF. (16-8)*2=16.

Current Source (Iref) Reference Resistor - R_R

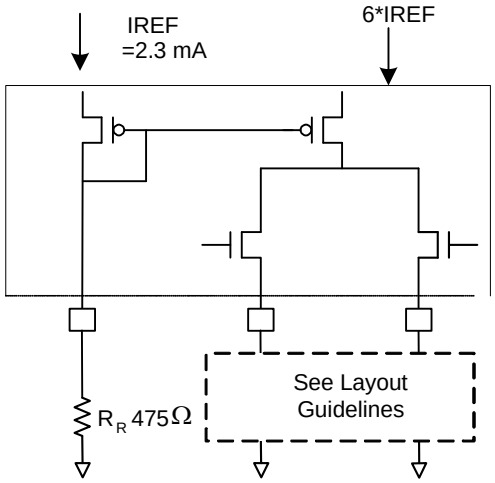
If board target trace impedance (Z) is 50Ω, then R_R = 475Ω (1%), providing IREF of 2.32 mA. The output current (I_{OH}) is equal to 6*IREF.

Output Termination

The PCI-Express differential clock outputs of the IDT5V41064 are open source drivers and require an external series resistor and a resistor to ground. These resistor values and their allowable locations are shown in detail in the **PCI-Express Layout Guidelines** section.

The IDT5V41064 can also be terminated to LVDS compatible voltage levels. See Layout Guidelines section.

Output Structures



General PCB Layout Recommendations

For optimum device performance and lowest output phase noise, the following guidelines should be observed.

1. Each 0.01μF decoupling capacitor should be mounted on the component side of the board as close to the VDD pin as possible.

2. No vias should be used between decoupling capacitor and VDD pin.

3. The PCB trace to VDD pin should be kept as short as possible, as should the PCB trace to the ground via. Distance of the ferrite bead and bulk decoupling from the device is less critical.

4. An optimum layout is one with all components on the same side of the board, minimizing vias through other signal layers (any ferrite beads and bulk decoupling capacitors can be mounted on the back). Other signal traces should be routed away from the IDT5V41064.This includes signal traces just underneath the device, or on layers adjacent to the ground plane layer used by the device.

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Layout Guidelines for PCI Express

PCIe Reference Clock			
Common Recommendations for Differential Routing	Dimension or Value	Unit	Figure
L1 length, route as non-coupled 50ohm trace	0.5 max	inch	1
L2 length, route as non-coupled 50ohm trace	0.2 max	inch	1
L3 length, route as non-coupled 50ohm trace	0.2 max	inch	1
Rs	33	ohm	1
Rt	49.9	ohm	1

Down Device Differential Routing			
L4 length, route as coupled microstrip 100ohm differential trace	2 min to 16 max	inch	1
L4 length, route as coupled stripline 100ohm differential trace	1.8 min to 14.4 max	inch	1

Differential Routing to PCI Express Connector			
L4 length, route as coupled microstrip 100ohm differential trace	0.25 to 14 max	inch	2
L4 length, route as coupled stripline 100ohm differential trace	0.225 min to 12.6 max	inch	2

Figure 1: Down Device Routing

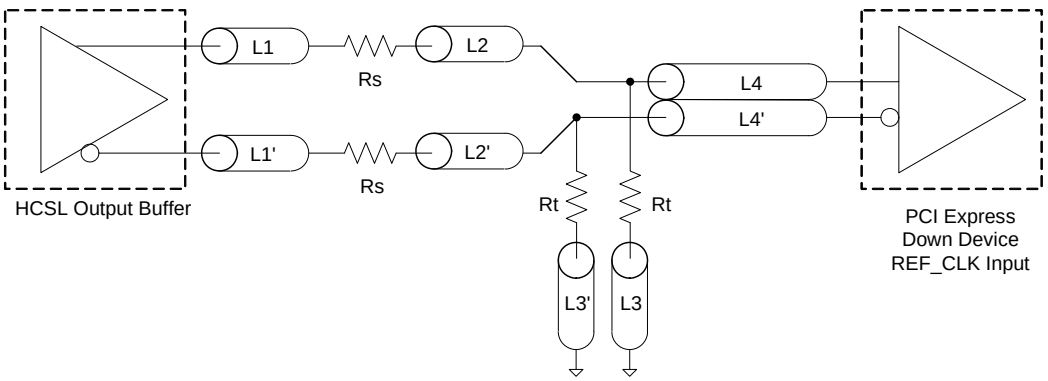
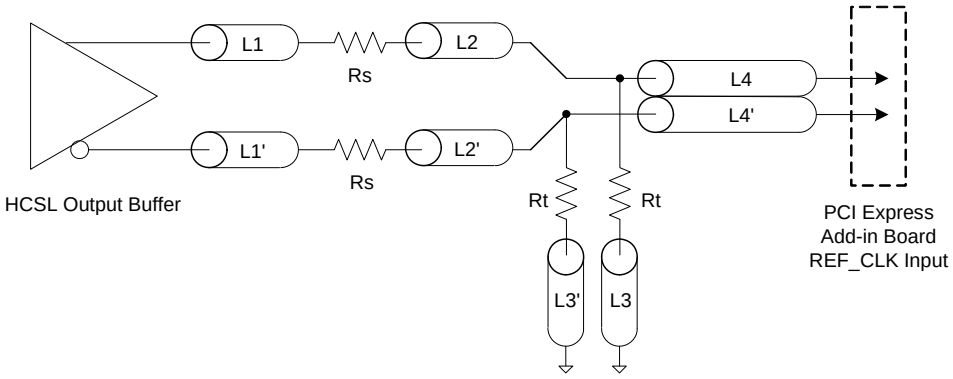


Figure 2: PCI Express Connector Routing



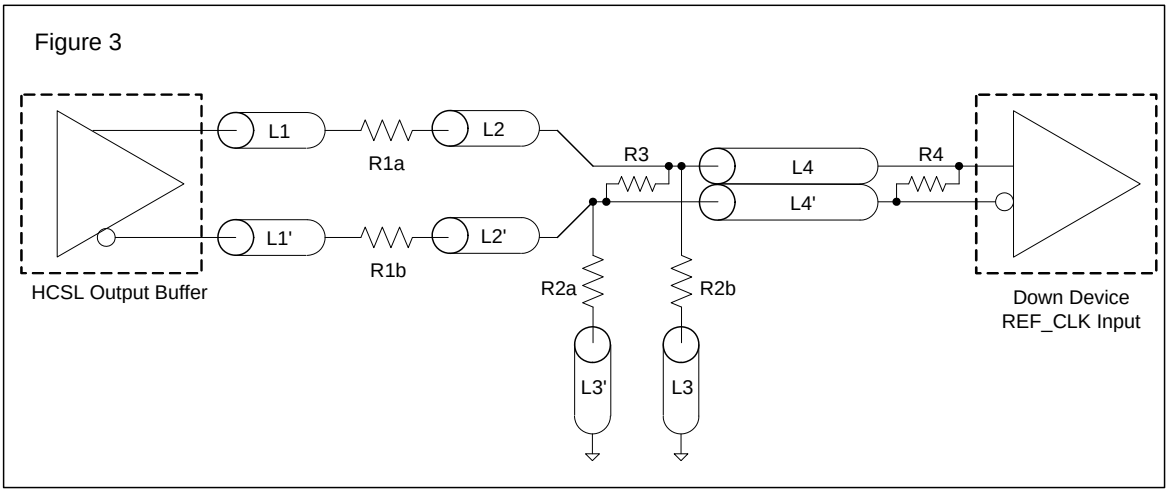
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Layout Guidelines for LVDS and Other Applications

Alternative Termination for LVDS and other Common Differential Signals (figure 3)							
Vdiff	Vp-p	Vcm	R1	R2	R3	R4	Note
0.45v	0.22v	1.08	33	150	100	100	
0.58	0.28	0.6	33	78.7	137	100	
0.80	0.40	0.6	33	78.7	none	100	ICS874003i-02 input compatible
0.60	0.3	1.2	33	174	140	100	Standard LVDS

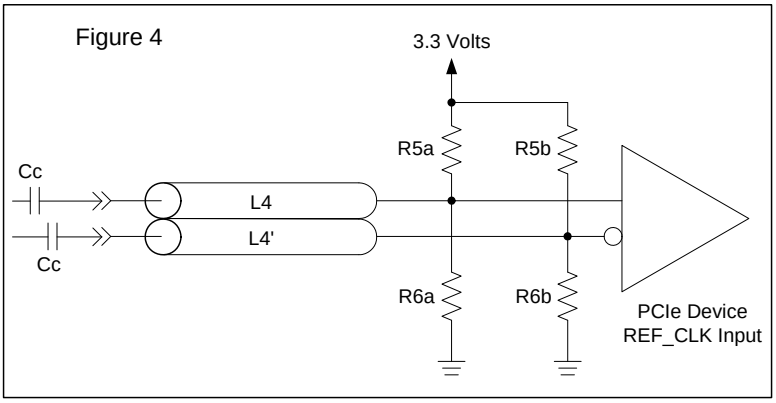
R1a = R1b = R1
R2a = R2b = R2

Figure 3



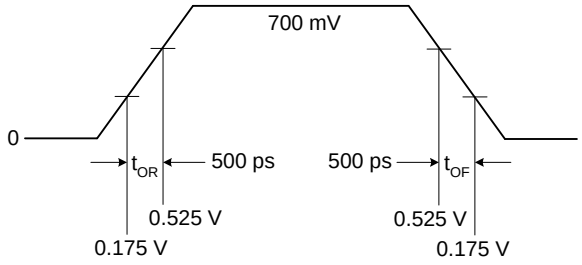
Cable Connected AC Coupled Application (figure 4)		
Component	Value	Note
R5a, R5b	8.2K 5%	
R6a, R6b	1K 5%	
Cc	0.1 µF	
Vcm	0.350 volts	

Figure 4

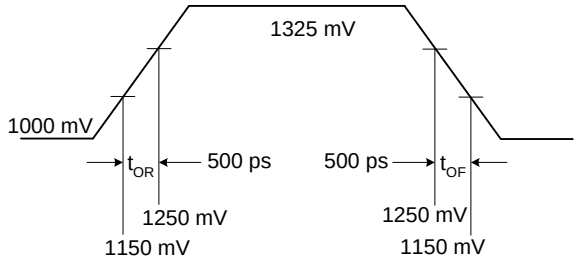


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Typical PCI-Express (HCSL) Waveform



Typical LVDS Waveform



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Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the IDT5V41064. These ratings are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
Supply Voltage, VDD, VDDA	5.5 V
All Inputs and Outputs	-0.5 V to VDD+0.5 V
Ambient Operating Temperature (commercial)	0 to +70°C
Ambient Operating Temperature (industrial)	-40 to +85°C
Storage Temperature	-65 to +150°C
Junction Temperature	125°C
Soldering Temperature	260°C
ESD Protection (Input)	2000 V min. (HBM)

DC Electrical Characteristics

Unless stated otherwise, **VDD = 3.3 V ±5%**, Ambient Temperature -40 to +85°C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Supply Voltage	V		3.135		3.465	
Input High Voltage[1]	V_{IH}		2.2		VDD +0.3	V
Input Low Voltage[1]	V_{IL}		VSS-0.3		0.8	V
Input Leakage Current[2]	I_{IL}	0 < Vin < VDD	-5		5	µA
Operating Supply Current	I_{DD}	2 pF load			70	mA
Input Capacitance	C_{IN}	Input pin capacitance			7	pF
Output Capacitance	C_{OUT}	Output pin capacitance			6	pF
Pin Inductance	L_{PIN}				5	nH
Output Resistance	Rout	CLK outputs	3.0			kΩ
Pull-up Resistor	R_{PUP}	SS1		100		kΩ

1 Single edge is monotonic when transitioning through region.

2 Inputs with pull-ups/-downs are not included.

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AC Electrical Characteristics - CLK/$\overline{CLK}$

Unless stated otherwise, **VDD=3.3 V ±5%**, Ambient Temperature -40 to +85°C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Frequency				25		MHz
Output Frequency				100		MHz
Output High Voltage[1,2]	V_{OH}		660	700	850	mV
Output Low Voltage[1,2]	V_{OL}		-150	27	150	mV
Crossing Point Voltage[1,2]		Absolute	250	350	550	mV
Crossing Point Voltage[1,2,4]		Variation over all edges		40	140	mV
Jitter, Cycle-to-Cycle[1,3]				25	100	ps
Rise Time[1,2]	t_{OR}	From 0.175 V to 0.525 V	175	332	700	ps
Fall Time[1,2]	t_{OF}	From 0.525 V to 0.175 V	175	344	700	ps
Rise/Fall Time Variation[1,2]				75	125	ps
Duty Cycle[1,3]			45	51	55	%
Stabilization Time	t_{STABLE}	From power-up VDD=3.3 V		1.2	3.0	ms
Spread Change Time	t_{SPREAD}	Settling period after spread change		3.0		ms

[1] Test setup is R_S=33 ohms R_P=50 ohms with 2 pF, R_R = 475Ω (1%).

[2] Measurement taken from a single-ended waveform.

[3] Measurement taken from a differential waveform.

[4] Measured at the crossing point where instantaneous voltages of both CLK and $\overline{CLK}$ are equal.

Electrical Characteristics - Differential Phase Jitter

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Jitter, Phase	$t_{jphasePLL}$	PCIe Gen1		30	86	ps (p-p)	1,2,3
	$t_{jphaseLO}$	PCIe Gen2, 10 kHz < f < 1.5 MHz		1.2	3	ps (RMS)	1,2,3
	$t_{jphaseHIGH}$	PCIe Gen2, 1.5 MHz < f < Nyquist (50 MHz)		1.9	3.1	ps (RMS)	1,2,3

Note 1. Guaranteed by design and characterization, not 100% tested in production.

Note 2. See http://www.pcisig.com for complete specs.

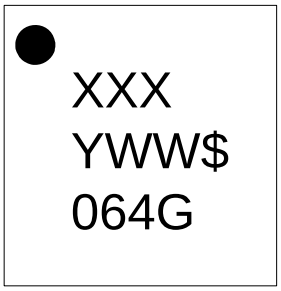
Note 3: Applies to 100MHz, spread off and 0.5% down spread only.

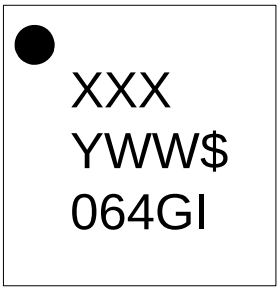
Thermal Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Thermal Resistance Junction to Ambient	θ_{JA}	Still air		63.2		°C/W
	θ_{JA}	1 m/s air flow		55.9		°C/W
	θ_{JA}	2 m/s air flow		53.1		°C/W
	θ_{JA}	3 m/s air flow		51.4		°C/W
Thermal Resistance Junction to Case	θ_{JC}			65.8		°C/W

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Marking Diagrams

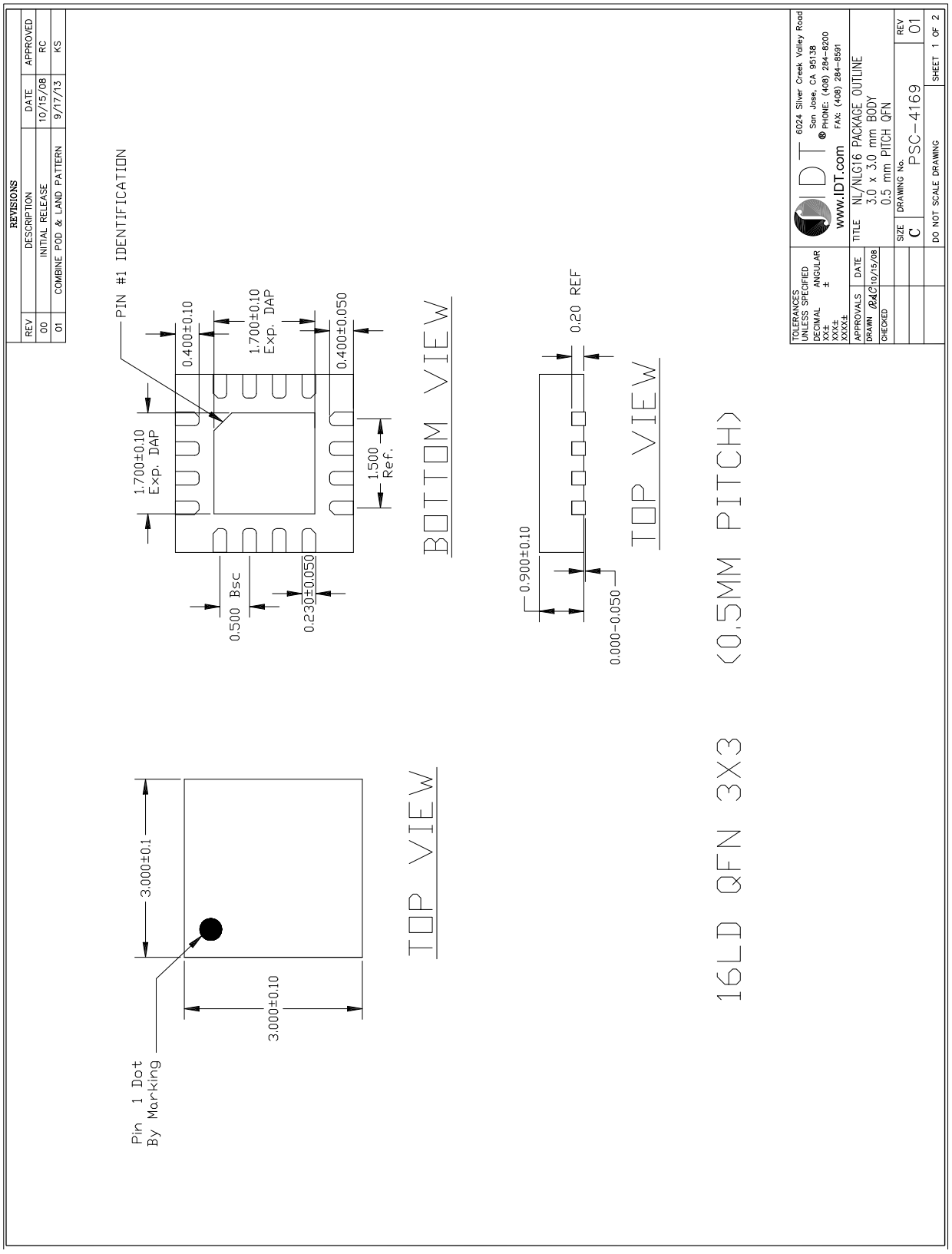




Notes:
1. Line 1: ‘XXX’ is the lot traceability (last numeric character of the assembly lot number).
2. Line 2: ‘YYW’ – Date code; $ – Assembly location.
3. Line 3: truncated IDT part number.
4. “G” designates RoHS compliant package.
5. “I” within the part number indicates industrial temperature range.

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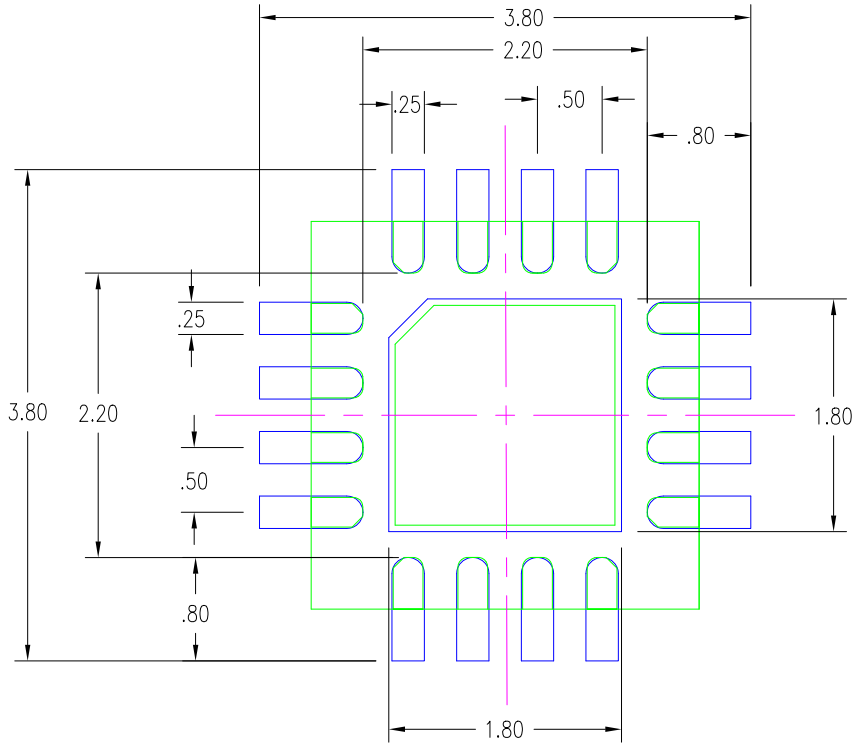
Package Outline and Package Dimensions (16-pin QFN)



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Package Outline and Package Dimensions (16-pin QFN), cont.

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
00	INITIAL RELEASE	10/15/08	RC
01	COMBINE POD & LAND PATTERN	9/17/13	KS



NOTES:
1. ALL DIMENSION ARE IN mm. ANGLES IN DEGREES.
2. TOP DOWN VIEW. AS VIEWED ON PCB.
3. COMPONENT OUTLINE SHOW FOR REFERENCE IN GREEN.
4. LAND PATTERN IN BLUE. NSMD PATTERN ASSUMED.
5. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

TOLERANCES UNLESS SPECIFIED DECIMAL ANGULAR XX± ± XXX± XXXX±	IDT 6024 Silver Creek Valley Road San Jose, CA 95138 PHONE: (408) 284-8200 FAX: (408) 284-8591 www.IDT.com	
APPROVALS DATE DRAWN RAC 10/15/08 CHECKED	TITLE NL/NLG16 PACKAGE OUTLINE 3.0 x 3.0 mm BODY 0.5 mm PITCH QFN	
	SIZE C	DRAWING No. PSC-4169 REV 01
	DO NOT SCALE DRAWING	SHEET 2 OF 2

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Ordering Information

Part / Order Number	Marking	Shipping Packaging	Package	Temperature
5V41064NLG	See Page 9	Trays	16-pin QFN	0 to +70° C
5V41064NLG8		Tape and Reel	16-pin QFN	0 to +70° C
5V41064NLGI		Trays	16-pin QFN	-40 to +85° C
5V41064NLGI8		Tape and Reel	16-pin QFN	-40 to +85° C

"G" after the two-letter package code are the Pb-Free configuration and are RoHS compliant.

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Revision History

Rev.	Originator	Date	Description of Change
A		04/01/08	Initial release - preliminary.
B	RW	03/02/10	1. Updated Title and Features bullets 2. Added Differential Phase Jitter table 3. Updated Cycle-to-cycle Jitter spec from 80ps to 125ps
C	RDW	06/18/10	1. Updated package and pinout to 16QFN. 2. Added Spread Spectrum.
D	RDW	07/19/10	1. Updated title and general description 2. Updated cycle-to-cycle jitter spec from 125 to 100 ps
E	RDW	12/21/10	1. Minor corrections 2. Updated with Typical data 3. Released to final
F	RDW	10/28/11	Updated Thermal char data
G	RDW	11/21/11	1. Changed title to "1 Output PCIe GEN1/2 Synthesizer" 2. Added note to Features section: "For PCIe Gen3 applications, see 5V41234" 3. Updated Differential Phase Jitter table.
H	RDW	10/07/13	Updated VOH min and VOL max values in AC Char table.
J	C.P.	04/17/17	Replaced package outline drawings with latest NLG16 drawings.

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