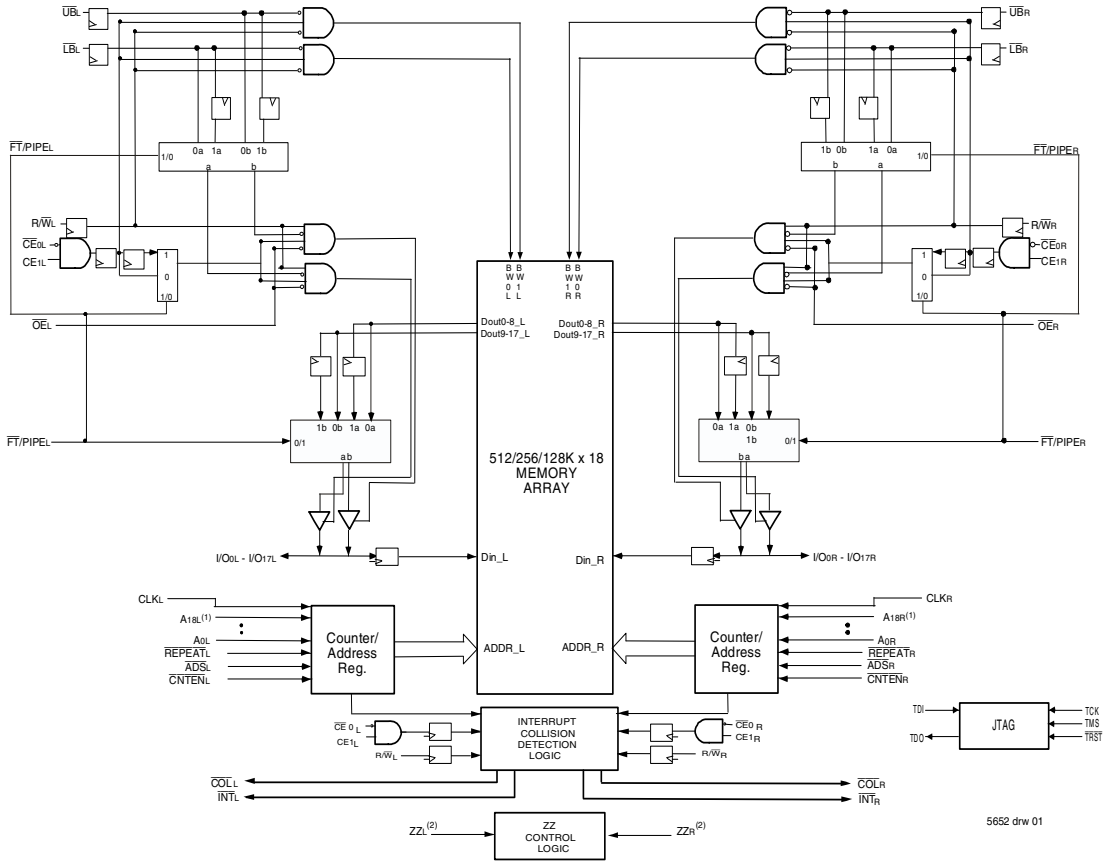
# HIGH-SPEED 2.5V 512/256/128K X 18 SYNCHRONOUS DUAL-PORT STATIC RAM WITH 3.3V OR 2.5V INTERFACE

**70T3339/19/99S**

## Features:

- **True Dual-Port memory cells which allow simultaneous access of the same memory location**
- **High-speed data access**
  - *Commercial: 3.4 (200MHz)/3.6ns (166MHz)/ 4.2ns (133MHz)(max.)*
  - *Industrial: 4.2ns (133MHz) (max.)*
- **Selectable Pipelined or Flow-Through output mode**
- **Counter enable and repeat features**
- **Dual chip enables allow for depth expansion without additional logic**
- **Interrupt and Collision Detection Flags**
- **Full synchronous operation on both ports**
  - *5ns cycle time, 200MHz operation (14Gbps bandwidth)*
  - *Fast 3.4ns clock to data out*
  - *Data input, address, byte enable and control registers*
  - *1.5ns setup to clock and 0.5ns hold on all control, data, and address inputs @ 200MHz*
  - *Self-timed write allows fast cycle time*
- **Separate byte controls for multiplexed bus and bus matching compatibility**
- **Dual Cycle Deselect (DCD) for Pipelined Output Mode**
- **2.5V (±100mV) power supply for core**
- **LVTTL compatible, selectable 3.3V (±150mV) or 2.5V (±100mV) power supply for I/Os and control signals on each port**
- **Industrial temperature range (-40°C to +85°C) is available at 133MHz**
- **Available in a 256-pin Ball Grid Array (BGA) and 208-pin fine pitch Ball Grid Array (fpBGA)**
- **Supports JTAG features compliant with IEEE 1149.1**
- **Green parts available, see ordering information**

## Functional Block Diagram




**NOTES:**

1. Address A18 is a NC for the IDT70T3319. Also, Addresses A18 and A17 are NC's for the IDT70T3399.
2. The sleep mode pin shuts off all dynamic inputs, except JTAG inputs, when asserted. All static inputs, i.e., PL/$\overline{FT}$x and OPTx and the sleep mode pins themselves (ZZx) are not affected during sleep mode.

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DSC-5652/11

## Description:

The IDT70T3339/19/99 is a high-speed 512/256/128k x 18 bit synchronous Dual-Port RAM. The memory array utilizes Dual-Port memory cells to allow simultaneous access of any address from both ports. Registers on control, data, and address inputs provide minimal setup and hold times. The timing latitude provided by this approach allows systems to be designed with very short cycle times. With an input data register, the IDT70T3339/19/99 has been optimized for applications having unidirectional or bidirectional data flow in bursts. An automatic power down feature, controlled by $\overline{CE}_0$ and $CE_1$, permits the on-chip circuitry of each port to enter a very low standby power mode.

The IDT70T3339/19/99 can support an operating voltage of either 3.3V or 2.5V on one or both ports, controllable by the OPT pins. The power supply for the core of the device ($V_{DD}$) is at 2.5V.



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## Pin Configuration (3,4,5,6)

70T3339/19/99
BC256(8)
BCG256(8)
256-Pin BGA
Top View

| | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A1 NC | A2 TDI | A3 NC | A4 $A_{17L}$(2) | A5 $A_{14L}$ | A6 $A_{11L}$ | A7 $A_{8L}$ | A8 NC | A9 $CE_{1L}$ | A10 $\overline{OE}_L$ | A11 $\overline{CNTEN}_L$ | A12 $A_{5L}$ | A13 $A_{2L}$ | A14 $A_{0L}$ | A15 NC | A16 NC |
| B1 $\overline{INT}_L$ | B2 NC | B3 TDO | B4 $A_{18L}$(1) | B5 $A_{15L}$ | B6 $A_{12L}$ | B7 $A_{9L}$ | B8 $\overline{UB}_L$ | B9 $\overline{CE}_{0L}$ | B10 $R/\overline{W}_L$ | B11 $\overline{REPEAT}_L$ | B12 $A_{4L}$ | B13 $A_{1L}$ | B14 $V_{DD}$ | B15 NC | B16 NC |
| C1 $\overline{COL}_L$ | C2 $I/O_{9L}$ | C3 $V_{SS}$ | C4 $A_{16L}$ | C5 $A_{13L}$ | C6 $A_{10L}$ | C7 $A_{7L}$ | C8 NC | C9 $\overline{LB}_L$ | C10 $CLK_L$ | C11 $\overline{ADS}_L$ | C12 $A_{6L}$ | C13 $A_{3L}$ | C14 $OPT_L$ | C15 NC | C16 $I/O_{8L}$ |
| D1 NC | D2 $I/O_{9R}$ | D3 NC | D4 $PIPE/\overline{FT}_L$ | D5 $V_{DDQL}$ | D6 $V_{DDQL}$ | D7 $V_{DDQR}$ | D8 $V_{DDQR}$ | D9 $V_{DDQL}$ | D10 $V_{DDQL}$ | D11 $V_{DDQR}$ | D12 $V_{DDQR}$ | D13 $V_{DD}$ | D14 NC | D15 NC | D16 $I/O_{8R}$ |
| E1 $I/O_{10R}$ | E2 $I/O_{10L}$ | E3 NC | E4 $V_{DDQL}$ | E5 $V_{DD}$ | E6 $V_{DD}$ | E7 NC | E8 $V_{SS}$ | E9 $V_{SS}$ | E10 $V_{SS}$ | E11 $V_{DD}$ | E12 $V_{DD}$ | E13 $V_{DDQR}$ | E14 NC | E15 $I/O_{7L}$ | E16 $I/O_{7R}$ |
| F1 $I/O_{11L}$ | F2 NC | F3 $I/O_{11R}$ | F4 $V_{DDQL}$ | F5 $V_{DD}$ | F6 NC | F7 NC | F8 $V_{SS}$ | F9 $V_{SS}$ | F10 $V_{SS}$ | F11 $V_{SS}$ | F12 $V_{DD}$ | F13 $V_{DDQR}$ | F14 $I/O_{6R}$ | F15 NC | F16 $I/O_{6L}$ |
| G1 NC | G2 NC | G3 $I/O_{12L}$ | G4 $V_{DDQR}$ | G5 $V_{SS}$ | G6 $V_{SS}$ | G7 $V_{SS}$ | G8 $V_{SS}$ | G9 $V_{SS}$ | G10 $V_{SS}$ | G11 $V_{SS}$ | G12 $V_{SS}$ | G13 $V_{DDQL}$ | G14 $I/O_{5L}$ | G15 NC | G16 NC |
| H1 NC | H2 $I/O_{12R}$ | H3 NC | H4 $V_{DDQR}$ | H5 $V_{SS}$ | H6 $V_{SS}$ | H7 $V_{SS}$ | H8 $V_{SS}$ | H9 $V_{SS}$ | H10 $V_{SS}$ | H11 $V_{SS}$ | H12 $V_{SS}$ | H13 $V_{DDQL}$ | H14 NC | H15 NC | H16 $I/O_{5R}$ |
| J1 $I/O_{13L}$ | J2 $I/O_{14R}$ | J3 $I/O_{13R}$ | J4 $V_{DDQL}$ | J5 $ZZ_R$ | J6 $V_{SS}$ | J7 $V_{SS}$ | J8 $V_{SS}$ | J9 $V_{SS}$ | J10 $V_{SS}$ | J11 $V_{SS}$ | J12 $ZZ_L$ | J13 $V_{DDQR}$ | J14 $I/O_{4R}$ | J15 $I/O_{3R}$ | J16 $I/O_{4L}$ |
| K1 NC | K2 NC | K3 $I/O_{14L}$ | K4 $V_{DDQL}$ | K5 $V_{SS}$ | K6 $V_{SS}$ | K7 $V_{SS}$ | K8 $V_{SS}$ | K9 $V_{SS}$ | K10 $V_{SS}$ | K11 $V_{SS}$ | K12 $V_{SS}$ | K13 $V_{DDQR}$ | K14 NC | K15 NC | K16 $I/O_{3L}$ |
| L1 $I/O_{15L}$ | L2 NC | L3 $I/O_{15R}$ | L4 $V_{DDQR}$ | L5 $V_{DD}$ | L6 NC | L7 NC | L8 $V_{SS}$ | L9 $V_{SS}$ | L10 $V_{SS}$ | L11 $V_{SS}$ | L12 $V_{DD}$ | L13 $V_{DDQL}$ | L14 $I/O_{2L}$ | L15 NC | L16 $I/O_{2R}$ |
| M1 $I/O_{16R}$ | M2 $I/O_{16L}$ | M3 NC | M4 $V_{DDQR}$ | M5 $V_{DD}$ | M6 $V_{DD}$ | M7 NC | M8 $V_{SS}$ | M9 $V_{SS}$ | M10 $V_{SS}$ | M11 $V_{DD}$ | M12 $V_{DD}$ | M13 $V_{DDQL}$ | M14 $I/O_{1R}$ | M15 $I/O_{1L}$ | M16 NC |
| N1 NC | N2 $I/O_{17R}$ | N3 NC | N4 $PIPE/\overline{FT}_R$ | N5 $V_{DDQR}$ | N6 $V_{DDQR}$ | N7 $V_{DDQL}$ | N8 $V_{DDQL}$ | N9 $V_{DDQR}$ | N10 $V_{DDQR}$ | N11 $V_{DDQL}$ | N12 $V_{DDQL}$ | N13 $V_{DD}$ | N14 NC | N15 $I/O_{0R}$ | N16 NC |
| P1 $\overline{COL}_R$ | P2 $I/O_{17L}$ | P3 TMS | P4 $A_{16R}$ | P5 $A_{13R}$ | P6 $A_{10R}$ | P7 $A_{7R}$ | P8 NC | P9 $\overline{LB}_R$ | P10 $CLK_R$ | P11 $\overline{ADS}_R$ | P12 $A_{6R}$ | P13 $A_{3R}$ | P14 NC | P15 NC | P16 $I/O_{0L}$ |
| R1 $\overline{INT}_R$ | R2 NC | R3 $\overline{TRST}$ | R4 $A_{18R}$(1) | R5 $A_{15R}$ | R6 $A_{12R}$ | R7 $A_{9R}$ | R8 $\overline{UB}_R$ | R9 $\overline{CE}_{0R}$ | R10 $R/\overline{W}_R$ | R11 $\overline{REPEAT}_R$ | R12 $A_{4R}$ | R13 $A_{1R}$ | R14 $OPT_R$ | R15 NC | R16 NC |
| T1 NC | T2 TCK | T3 NC | T4 $A_{17R}$(2) | T5 $A_{14R}$ | T6 $A_{11R}$ | T7 $A_{8R}$ | T8 NC | T9 $CE_{1R}$ | T10 $\overline{OE}_R$ | T11 $\overline{CNTEN}_R$ | T12 $A_{5R}$ | T13 $A_{2R}$ | T14 $A_{0R}$ | T15 NC | T16 NC |

5652 drw 02d

**NOTES:**
1. Pin is a NC for IDT70T3319 and IDT70T3399.
2. Pin is a NC for IDT70T3399.
3. All $V_{DD}$ pins must be connected to 2.5V power supply.
4. All $V_{DDQ}$ pins must be connected to appropriate power supply: 3.3V if OPT pin for that port is set to $V_{DD}$ (2.5V), and 2.5V if OPT pin for that port is set to $V_{SS}$ (0V).
5. All $V_{SS}$ pins must be connected to ground supply.
6. Package body is approximately 17mm x 17mm x 1.4mm, with 1.0mm ball-pitch.
7. This package code is used to reference the package diagram.
8. This text does not indicate orientation of the actual part-marking.



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## Pin Configurations(con't)[3,4,5,6]

| 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $I/O_{9L}$ | $\overline{INT}_L$ | $V_{SS}$ | TDO | NC | $A_{16L}$ | $A_{12L}$ | $A_{8L}$ | NC | $V_{DD}$ | $CLK_L$ | $\overline{CNTEN}_L$ | $A_{4L}$ | $A_{0L}$ | $OPT_L$ | NC | $V_{SS}$ | A |
| NC | $V_{SS}$ | $\overline{COL}_L$ | TDI | $A_{17L}$(2) | $A_{13L}$ | $A_{9L}$ | NC | $\overline{CE}_{0L}$ | $V_{SS}$ | $\overline{ADS}_L$ | $A_{5L}$ | $A_{1L}$ | NC | $V_{DDQR}$ | $I/O_{8L}$ | NC | B |
| $V_{DDQL}$ | $I/O_{9R}$ | $V_{DDQR}$ | PIPE/$\overline{FT}_L$ | $A_{18L}$(1) | $A_{14L}$ | $A_{10L}$ | $\overline{UB}_L$ | $CE_{1L}$ | $V_{SS}$ | $R/\overline{W}_L$ | $A_{6L}$ | $A_{2L}$ | $V_{DD}$ | $I/O_{8R}$ | NC | $V_{SS}$ | C |
| NC | $V_{SS}$ | $I/O_{10L}$ | NC | $A_{15L}$ | $A_{11L}$ | $A_{7L}$ | $\overline{LB}_L$ | $V_{DD}$ | $\overline{OE}_L$ | $\overline{REPEAT}_L$ | $A_{3L}$ | $V_{DD}$ | NC | $V_{DDQL}$ | $I/O_{7L}$ | $I/O_{7R}$ | D |
| $I/O_{11L}$ | NC | $V_{DDQR}$ | $I/O_{10R}$ | | | | | | | | | | $I/O_{6L}$ | NC | $V_{SS}$ | NC | E |
| $V_{DDQL}$ | $I/O_{11R}$ | NC | $V_{SS}$ | | | | | | | | | | $V_{SS}$ | $I/O_{6R}$ | NC | $V_{DDQR}$ | F |
| NC | $V_{SS}$ | $I/O_{12L}$ | NC | | | | | | | | | | NC | $V_{DDQL}$ | $I/O_{5L}$ | NC | G |
| $V_{DD}$ | NC | $V_{DDQR}$ | $I/O_{12R}$ | | | | | | | | | | $V_{DD}$ | NC | $V_{SS}$ | $I/O_{5R}$ | H |
| $V_{DDQL}$ | $V_{DD}$ | $V_{SS}$ | $ZZ_R$ | | | | | | | | | | $ZZ_L$ | $V_{DD}$ | $V_{SS}$ | $V_{DDQR}$ | J |
| $I/O_{14R}$ | $V_{SS}$ | $I/O_{13R}$ | $V_{SS}$ | | | | | | | | | | $I/O_{3R}$ | $V_{DDQL}$ | $I/O_{4R}$ | $V_{SS}$ | K |
| NC | $I/O_{14L}$ | $V_{DDQR}$ | $I/O_{13L}$ | | | | | | | | | | NC | $I/O_{3L}$ | $V_{SS}$ | $I/O_{4L}$ | L |
| $V_{DDQL}$ | NC | $I/O_{15R}$ | $V_{SS}$ | | | | | | | | | | $V_{SS}$ | NC | $I/O_{2R}$ | $V_{DDQR}$ | M |
| NC | $V_{SS}$ | NC | $I/O_{15L}$ | | | | | | | | | | $I/O_{1R}$ | $V_{DDQL}$ | NC | $I/O_{2L}$ | N |
| $I/O_{16R}$ | $I/O_{16L}$ | $V_{DDQR}$ | $\overline{COL}_R$ | $\overline{TRST}$ | $A_{16R}$ | $A_{12R}$ | $A_{8R}$ | NC | $V_{DD}$ | $CLK_R$ | $\overline{CNTEN}_R$ | $A_{4R}$ | NC | $I/O_{1L}$ | $V_{SS}$ | NC | P |
| $V_{SS}$ | NC | $I/O_{17R}$ | TCK | $A_{17R}$(2) | $A_{13R}$ | $A_{9R}$ | NC | $\overline{CE}_{0R}$ | $V_{SS}$ | $\overline{ADS}_R$ | $A_{5R}$ | $A_{1R}$ | NC | $V_{DDQL}$ | $I/O_{0R}$ | $V_{DDQR}$ | R |
| NC | $I/O_{17L}$ | $V_{DDQL}$ | TMS | $A_{18R}$(1) | $A_{14R}$ | $A_{10R}$ | $\overline{UB}_R$ | $CE_{1R}$ | $V_{SS}$ | $R/\overline{W}_R$ | $A_{6R}$ | $A_{2R}$ | $V_{SS}$ | NC | $V_{SS}$ | NC | T |
| $V_{SS}$ | $\overline{INT}_R$ | PIPE/$\overline{FT}_R$ | NC | $A_{15R}$ | $A_{11R}$ | $A_{7R}$ | $\overline{LB}_R$ | $V_{DD}$ | $\overline{OE}_R$ | $\overline{REPEAT}_R$ | $A_{3R}$ | $A_{0R}$ | $V_{DD}$ | $OPT_R$ | NC | $I/O_{0L}$ | U |

70T3339/19/99
BF208[7]
BFG208[7]
208-Pin fpBGA
Top View[8]

5652 drw 02c

**NOTES:**
1. Pin is a NC for IDT70T3319 and IDT70T3399.
2. Pin is a NC for IDT70T3399.
3. All $V_{DD}$ pins must be connected to 2.5V power supply.
4. All $V_{DDQ}$ pins must be connected to appropriate power supply: 3.3V if OPT pin for that port is set to $V_{DD}$ (2.5V), and 2.5V if OPT pin for that port is set to $V_{SS}$ (0V).
5. All $V_{SS}$ pins must be connected to ground supply.
6. Package body is approximately 15mm x 15mm x 1.4mm with 0.8mm ball pitch.
7. This package code is used to reference the package diagram.
8. This text does not indicate orientation of the actual part-marking.



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## Pin Names

| Left Port | Right Port | Names |
|---|---|---|
| $\overline{CE}_{0L}$, $CE_{1L}$ | $\overline{CE}_{0R}$, $CE_{1R}$ | Chip Enables (Input)[6] |
| R/$\overline{W}_L$ | R/$\overline{W}_R$ | Read/Write Enable (Input) |
| $\overline{OE}_L$ | $\overline{OE}_R$ | Output Enable (Input) |
| $A_{0L}$ - $A_{18L}$[5] | $A_{0R}$ - $A_{18R}$[5] | Address (Input) |
| $I/O_{0L}$ - $I/O_{17L}$ | $I/O_{0R}$ - $I/O_{17R}$ | Data Input/Output |
| $CLK_L$ | $CLK_R$ | Clock (Input) |
| PL/$\overline{FT}_L$ | PL/$\overline{FT}_R$ | Pipeline/Flow-Through (Input) |
| $\overline{ADS}_L$ | $\overline{ADS}_R$ | Address Strobe Enable (Input) |
| $\overline{CNTEN}_L$ | $\overline{CNTEN}_R$ | Counter Enable (Input) |
| $\overline{REPEAT}_L$ | $\overline{REPEAT}_R$ | Counter Repeat[3] |
| $\overline{UB}_L$ | $\overline{UB}_R$ | Upper Byte Enable ($I/O_9$ - $I/O_{17}$)[6] |
| $\overline{LB}_L$ | $\overline{LB}_R$ | Lower Byte Enable ($I/O_0$ - $I/O_8$)[6] |
| $V_{DDQL}$ | $V_{DDQR}$ | Power (I/O Bus) (3.3V or 2.5V)[1] (Input) |
| $OPT_L$ | $OPT_R$ | Option for selecting $V_{DDQX}$[1,2] (Input) |
| $ZZ_L$ | $ZZ_R$ | Sleep Mode pin[4] (Input) |
| $V_{DD}$ | | Power (2.5V)[1] (Input) |
| $V_{SS}$ | | Ground (0V) (Input) |
| TDI | | Test Data Input |
| TDI | | Test Data Output |
| TCK | | Test Logic Clock (10MHz) (Input) |
| TMS | | Test Mode Select (Input) |
| $\overline{TRST}$ | | Reset (Initialize TAP Controller) (Input) |
| $\overline{INT}_L$ | $\overline{INT}_R$ | Interrupt Flag (Output) |
| $\overline{COL}_L$ | $\overline{COL}_R$ | Collision Alert (Output) |

5652 tbl 01

**NOTES:**

1. $V_{DD}$, $OPT_X$, and $V_{DDQX}$ must be set to appropriate operating levels prior to applying inputs on the I/Os and controls for that port.
2. $OPT_X$ selects the operating voltage levels for the I/Os and controls on that port. If $OPT_X$ is set to $V_{DD}$ (2.5V), then that port's I/Os and controls will operate at 3.3V levels and $V_{DDQX}$ must be supplied at 3.3V. If $OPT_X$ is set to $V_{SS}$ (0V), then that port's I/Os and address controls will operate at 2.5V levels and $V_{DDQX}$ must be supplied at 2.5V. The OPT pins are independent of one another—both ports can operate at 3.3V levels, both can operate at 2.5V levels, or either can operate at 3.3V with the other at 2.5V.
3. When $\overline{REPEAT}_X$ is asserted, the counter will reset to the last valid address loaded via $\overline{ADS}_X$.
4. The sleep mode pin shuts off all dynamic inputs, except JTAG inputs, when asserted. All static inputs, i.e., PL/$\overline{FT}_X$ and $OPT_X$ and the sleep mode pins themselves ($ZZ_X$) are not affected during sleep mode. It is recommended that boundary scan not be operated during sleep mode.
5. Address $A_{18X}$ is a NC for the IDT70T3319. Also, Addresses $A_{18X}$ and $A_{17X}$ are NC's for the IDT70T3399.
6. Chip Enables and Byte Enables are double buffered when PL/$\overline{FT}$ = $V_{IH}$, i.e., the signals take two cycles to deselect.



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## Truth Table I—Read/Write and Enable Control (1,2,3,4)

| $\overline{OE}$ | CLK | $\overline{CE_0}$ | $CE_1$ | $\overline{UB}$ | $\overline{LB}$ | R/$\overline{W}$ | ZZ | Upper Byte $I/O_{9-17}$ | Lower Byte $I/O_{0-8}$ | MODE |
|---|---|---|---|---|---|---|---|---|---|---|
| X | ↑ | H | X | X | X | X | L | High-Z | High-Z | Deselected–Power Down |
| X | ↑ | X | L | X | X | X | L | High-Z | High-Z | Deselected–Power Down |
| X | ↑ | L | H | H | H | X | L | High-Z | High-Z | Both Bytes Deselected |
| X | ↑ | L | H | H | L | L | L | High-Z | $D_{IN}$ | Write to Lower Byte Only |
| X | ↑ | L | H | L | H | L | L | $D_{IN}$ | High-Z | Write to Upper Byte Only |
| X | ↑ | L | H | L | L | L | L | $D_{IN}$ | $D_{IN}$ | Write to Both Bytes |
| L | ↑ | L | H | H | L | H | L | High-Z | $D_{OUT}$ | Read Lower Byte Only |
| L | ↑ | L | H | L | H | H | L | $D_{OUT}$ | High-Z | Read Upper Byte Only |
| L | ↑ | L | H | L | L | H | L | $D_{OUT}$ | $D_{OUT}$ | Read Both Bytes |
| H | ↑ | L | H | L | L | X | L | High-Z | High-Z | Outputs Disabled |
| X | X | X | X | X | X | X | H | High-Z | High-Z | Sleep Mode |

5652 tbl 02

**NOTES:**
1. "H" = $V_{IH}$, "L" = $V_{IL}$, "X" = Don't Care.
2. $\overline{ADS}$, $\overline{CNTEN}$, $\overline{REPEAT}$ = X.
3. $\overline{OE}$ and ZZ are asynchronous input signals.
4. It is possible to read or write any combination of bytes during a given access. A few representative samples have been illustrated here.

## Truth Table II—Address Counter Control (1,2)

| Address | Previous Internal Address | Internal Address Used | CLK | $\overline{ADS}$ | $\overline{CNTEN}$ | $\overline{REPEAT}$[6] | I/O[3] | MODE |
|---|---|---|---|---|---|---|---|---|
| An | X | An | ↑ | L[4] | X | H | $D_{I/O}$ (n) | External Address Used |
| X | An | An + 1 | ↑ | H | L[5] | H | $D_{I/O}$(n+1) | Counter Enabled—Internal Address generation |
| X | An + 1 | An + 1 | ↑ | H | H | H | $D_{I/O}$(n+1) | External Address Blocked—Counter disabled (An + 1 reused) |
| X | X | An | ↑ | X | X | L[4] | $D_{I/O}$(n) | Counter Set to last valid $\overline{ADS}$ load |

5652 tbl 03

**NOTES:**
1. "H" = $V_{IH}$, "L" = $V_{IL}$, "X" = Don't Care.
2. Read and write operations are controlled by the appropriate setting of R/$\overline{W}$, $\overline{CE_0}$, $CE_1$, $\overline{UB}$, $\overline{LB}$ and $\overline{OE}$.
3. Outputs configured in flow-through output mode: if outputs are in pipelined mode the data out will be delayed by one cycle.
4. $\overline{ADS}$ and $\overline{REPEAT}$ are independent of all other memory control signals including $\overline{CE_0}$, $CE_1$, $\overline{UB}$ and $\overline{LB}$.
5. The address counter advances if $\overline{CNTEN}$ = $V_{IL}$ on the rising edge of CLK, regardless of all other memory control signals including $\overline{CE_0}$, $CE_1$, $\overline{UB}$ and $\overline{LB}$.
6. When $\overline{REPEAT}$ is asserted, the counter will reset to the last valid address loaded via $\overline{ADS}$. This value is not set at power-up: a known location should be loaded via $\overline{ADS}$ during initialization if desired. Any subsequent $\overline{ADS}$ access during operations will update the $\overline{REPEAT}$ address location.



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## Maximum Operating Temperature and Supply Voltage(1)

| Grade | Ambient Temperature | GND | $V_{DD}$ |
|---|---|---|---|
| Commercial | 0°C to +70°C | 0V | 2.5V ± 100mV |
| Industrial | -40°C to +85°C | 0V | 2.5V ± 100mV |

5652 tbl 04

**NOTE:**
1. This is the parameter TA. This is the "instant on" case temperature.

## Recommended DC Operating Conditions with $V_{DDQ}$ at 2.5V

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{DD}$ | Core Supply Voltage | 2.4 | 2.5 | 2.6 | V |
| $V_{DDQ}$ | I/O Supply Voltage(3) | 2.4 | 2.5 | 2.6 | V |
| $V_{SS}$ | Ground | 0 | 0 | 0 | V |
| $V_{IH}$ | Input High Volltage (Address, Control & Data I/O Inputs)(3) | 1.7 | — | $V_{DDQ}$ + 100mV(2) | V |
| $V_{IH}$ | Input High Voltage – JTAG | 1.7 | — | $V_{DD}$ + 100mV(2) | V |
| $V_{IH}$ | Input High Voltage - ZZ, OPT, PIPE/$\overline{FT}$ | $V_{DD}$ - 0.2V | — | $V_{DD}$ + 100mV(2) | V |
| $V_{IL}$ | Input Low Voltage | -0.3(1) | — | 0.7 | V |
| $V_{IL}$ | Input Low Voltage - ZZ, OPT, PIPE/$\overline{FT}$ | -0.3(1) | — | 0.2 | V |

5652 tbl 05a

**NOTES:**
1. $V_{IL}$ (min.) = -1.0V for pulse width less than $t_{CYC}$/2 or 5ns, whichever is less.
2. $V_{IH}$ (max.) = $V_{DDQ}$ + 1.0V for pulse width less than $t_{CYC}$/2 or 5ns, whichever is less.
3. To select operation at 2.5V levels on the I/Os and controls of a given port, the OPT pin for that port must be set to $V_{SS}$(0V), and $V_{DDQX}$ for that port must be supplied as indicated above.

## Recommended DC Operating Conditions with $V_{DDQ}$ at 3.3V

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{DD}$ | Core Supply Voltage | 2.4 | 2.5 | 2.6 | V |
| $V_{DDQ}$ | I/O Supply Voltage(3) | 3.15 | 3.3 | 3.45 | V |
| $V_{SS}$ | Ground | 0 | 0 | 0 | V |
| $V_{IH}$ | Input High Voltage (Address, Control &Data I/O Inputs)(3) | 2.0 | — | $V_{DDQ}$ + 150mV(2) | V |
| $V_{IH}$ | Input High Voltage – JTAG | 1.7 | — | $V_{DD}$ + 100mV(2) | V |
| $V_{IH}$ | Input High Voltage - ZZ, OPT, PIPE/$\overline{FT}$ | $V_{DD}$ - 0.2V | — | $V_{DD}$ + 100mV(2) | V |
| $V_{IL}$ | Input Low Voltage | -0.3(1) | — | 0.8 | V |
| $V_{IL}$ | Input Low Voltage - ZZ, OPT, PIPE/$\overline{FT}$ | -0.3(1) | — | 0.2 | V |

5652 tbl 05b

**NOTES:**
1. $V_{IL}$ (min.) = -1.0V for pulse width less than $t_{CYC}$/2, or 5ns, whichever is less.
2. $V_{IH}$ (max.) = $V_{DDQ}$ + 1.0V for pulse width less than $t_{CYC}$/2 or 5ns, whichever is less.
3. To select operation at 3.3V levels on the I/Os and controls of a given port, the OPT pin for that port must be set to $V_{DD}$ (2.5V), and $V_{DDQX}$ for that port must be supplied as indicated above.



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## Absolute Maximum Ratings(1)

| Symbol | Rating | Commercial & Industrial | Unit |
|---|---|---|---|
| $V_{TERM}$ ($V_{DD}$) | $V_{DD}$ Terminal Voltage with Respect to GND | -0.5 to 3.6 | V |
| $V_{TERM}$(2) ($V_{DDQ}$) | $V_{DDQ}$ Terminal Voltage with Respect to GND | -0.3 to $V_{DDQ}$ + 0.3 | V |
| $V_{TERM}$(2) (INPUTS and I/O's) | Input and I/O Terminal Voltage with Respect to GND | -0.3 to $V_{DDQ}$ + 0.3 | V |
| $T_{BIAS}$(3) | Temperature Under Bias | -55 to +125 | °C |
| $T_{STG}$ | Storage Temperature | -65 to +150 | °C |
| $T_{JN}$ | Junction Temperature | +150 | °C |
| $I_{OUT}$(For $V_{DDQ}$ = 3.3V) | DC Output Current | 50 | mA |
| $I_{OUT}$(For $V_{DDQ}$ = 2.5V) | DC Output Current | 40 | mA |

5652 tbl 06

**NOTES:**
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. This is a steady-state DC parameter that applies after the power supply has reached its nominal operating value. Power sequencing is not necessary; however, the voltage on any Input or I/O pin cannot exceed $V_{DDQ}$ during power supply ramp up.
3. Ambient Temperature under DC Bias. No AC Conditions. Chip Deselected.

## Capacitance(1)

($T_A$ = +25°C, f = 1.0MHz) PQFP ONLY

| Symbol | Parameter | Conditions(2) | Max. | Unit |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $V_{IN}$ = 3dV | 8 | pF |
| $C_{OUT}$(3) | Output Capacitance | $V_{OUT}$ = 3dV | 10.5 | pF |

5652 tbl 07

**NOTES:**
1. These parameters are determined by device characterization, but are not production tested.
2. 3dV references the interpolated capacitance when the input and output switch from 0V to 3V or from 3V to 0V.
3. $C_{OUT}$ also references $C_{I/O}$.

## DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range ($V_{DD}$ = 2.5V ± 100mV)

| Symbol | Parameter | Test Conditions | 70T3339/19/99S Min. | 70T3339/19/99S Max. | Unit |
|---|---|---|---|---|---|
| $\|I_{LI}\|$ | Input Leakage Current(1) | $V_{DDQ}$ = Max., $V_{IN}$ = 0V to $V_{DDQ}$ | — | 10 | µA |
| $\|I_{LI}\|$ | JTAG & ZZ Input Leakage Current(1,2) | $V_{DD}$ = Max., $V_{IN}$ = 0V to $V_{DD}$ | — | ±30 | µA |
| $\|I_{LO}\|$ | Output Leakage Current(1,3) | $\overline{CE}_0$ = $V_{IH}$ or $CE_1$ = $V_{IL}$, $V_{OUT}$ = 0V to $V_{DDQ}$ | — | 10 | µA |
| $V_{OL}$ (3.3V) | Output Low Voltage(1) | $I_{OL}$ = +4mA, $V_{DDQ}$ = Min. | — | 0.4 | V |
| $V_{OH}$ (3.3V) | Output High Voltage(1) | $I_{OH}$ = -4mA, $V_{DDQ}$ = Min. | 2.4 | — | V |
| $V_{OL}$ (2.5V) | Output Low Voltage(1) | $I_{OL}$ = +2mA, $V_{DDQ}$ = Min. | — | 0.4 | V |
| $V_{OH}$ (2.5V) | Output High Voltage(1) | $I_{OH}$ = -2mA, $V_{DDQ}$ = Min. | 2.0 | — | V |

5652 tbl 08

**NOTES:**
1. $V_{DDQ}$ is selectable (3.3V/2.5V) via OPT pins. Refer to p.6 for details.
2. Applicable only for TMS, TDI and $\overline{TRST}$ inputs.
3. Outputs tested in tri-state mode.



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## DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range (3) ($V_{DD}$ = 2.5V ± 100mV)

| Symbol | Parameter | Test Condition | Version | | 70T3339/19/99 S200 Com'l Only(7) Typ.(4) | 70T3339/19/99 S200 Com'l Only(7) Max. | 70T3339/19/99 S166 Com'l & Ind Typ.(4) | 70T3339/19/99 S166 Com'l & Ind Max. | 70T3339/19/99 S133 Com'l & Ind Typ.(4) | 70T3339/19/99 S133 Com'l & Ind Max. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| $I_{DD}$ | Dynamic Operating Current (Both Ports Active) | $\overline{CE}_L$ and $\overline{CE}_R$= $V_{IL}$, Outputs Disabled, f = $f_{MAX}$(1) | COM'L | S | 375 | 525 | 320 | 450 | 260 | 370 | mA |
| | | | IND | S | — | — | 320 | 510 | 260 | 450 | |
| $I_{SB1}$(6) | Standby Current (Both Ports - TTL Level Inputs) | $\overline{CE}_L$ = $\overline{CE}_R$ = $V_{IH}$ f = $f_{MAX}$(1) | COM'L | S | 205 | 270 | 175 | 230 | 140 | 190 | mA |
| | | | IND | S | — | — | 175 | 275 | 140 | 235 | |
| $I_{SB2}$(6) | Standby Current (One Port - TTL Level Inputs) | $\overline{CE}_{"A"}$ = $V_{IL}$ and $\overline{CE}_{"B"}$ = $V_{IH}$(5) Active Port Outputs Disabled, f=$f_{MAX}$(1) | COM'L | S | 300 | 375 | 250 | 325 | 200 | 250 | mA |
| | | | IND | S | — | — | 250 | 365 | 200 | 310 | |
| $I_{SB3}$ | Full Standby Current (Both Ports - CMOS Level Inputs) | Both Ports $\overline{CE}_L$ and $\overline{CE}_R$ ≥ $V_{DDQ}$ - 0.2V, $V_{IN}$ ≥ $V_{DDQ}$ - 0.2V or $V_{IN}$ ≤ 0.2V, f = 0(2) | COM'L | S | 5 | 15 | 5 | 15 | 5 | 15 | mA |
| | | | IND | S | — | — | 5 | 20 | 5 | 20 | |
| $I_{SB4}$(6) | Full Standby Current (One Port - CMOS Level Inputs) | $\overline{CE}_{"A"}$ ≤ 0.2V and $\overline{CE}_{"B"}$ ≥ $V_{DDQ}$ - 0.2V(5) $V_{IN}$ ≥ $V_{DDQ}$ - 0.2V or $V_{IN}$ ≤ 0.2V Active Port, Outputs Disabled, f = $f_{MAX}$(1) | COM'L | S | 300 | 375 | 250 | 325 | 200 | 250 | mA |
| | | | IND | S | — | — | 250 | 365 | 200 | 310 | |
| $I_{ZZ}$ | Sleep Mode Current (Both Ports - TTL Level Inputs) | $ZZ_L$ = $ZZ_R$ = $V_{IH}$ f=$f_{MAX}$(1) | COM'L | S | 5 | 15 | 5 | 15 | 5 | 15 | mA |
| | | | IND | S | — | — | 5 | 20 | 5 | 20 | |

5652 tbl 09

**NOTES:**

1. At f = $f_{MAX}$, address and control lines (except Output Enable) are cycling at the maximum frequency clock cycle of 1/$t_{CYC}$, using "AC TEST CONDITIONS".
2. f = 0 means no address, clock, or control lines change. Applies only to input at CMOS level standby.
3. Port "A" may be either left or right port. Port "B" is the opposite from port "A".
4. $V_{DD}$ = 2.5V, $T_A$ = 25°C for Typ, and are not production tested. $I_{DD\,DC}$(f=0) = 15mA (Typ).
5. $\overline{CE}_X$ = $V_{IL}$ means $\overline{CE}_{0X}$ = $V_{IL}$ and $CE_{1X}$ = $V_{IH}$
   $\overline{CE}_X$ = $V_{IH}$ means $\overline{CE}_{0X}$ = $V_{IH}$ or $CE_{1X}$ = $V_{IL}$
   $\overline{CE}_X$ ≤ 0.2V means $\overline{CE}_{0X}$ ≤ 0.2V and $CE_{1X}$ ≥ $V_{DDQ}$ - 0.2V
   $\overline{CE}_X$ ≥ $V_{DDQ}$ - 0.2V means $\overline{CE}_{0X}$ ≥ $V_{DDQ}$ - 0.2V or $CE_{1X}$ - 0.2V
   "X" represents "L" for left port or "R" for right port.
6. $I_{SB1}$, $I_{SB2}$ and $I_{SB4}$ will all reach full standby levels ($I_{SB3}$) on the appropriate port(s) if $ZZ_L$ and/or $ZZ_R$ = $V_{IH}$.
7. 200Mhz is not available in the BF-208 package.



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## AC Test Conditions ($V_{DDQ}$ - 3.3V/2.5V)

| | |
|---|---|
| Input Pulse Levels (Address & Controls) | GND to 3.0V/GND to 2.4V |
| Input Pulse Levels (I/Os) | GND to 3.0V/GND to 2.4V |
| Input Rise/Fall Times | 2ns |
| Input Timing Reference Levels | 1.5V/1.25V |
| Output Reference Levels | 1.5V/1.25V |
| Output Load | Figures 1 and 2 |

5652 tbl 10

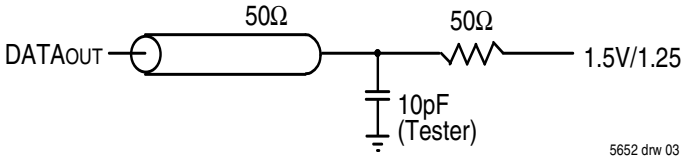
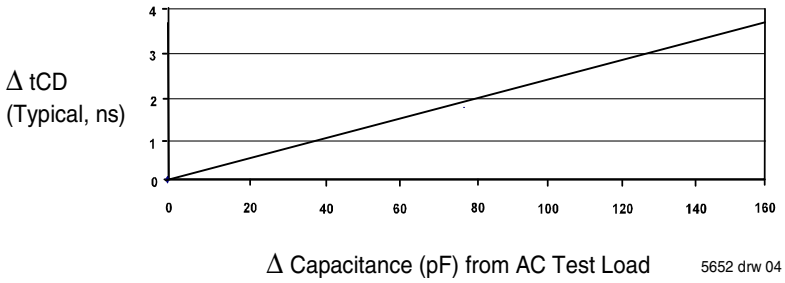



**Figure 1. AC Output Test load.**






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# AC Electrical Characteristics Over the Operating Temperature Range (Read and Write Cycle Timing) [2,3] ($V_{DD}$ = 2.5V ± 100mV, $T_A$ = 0°C to +70°C)

| | | 70T3339/19/99 S200 Com'l Only[4] | | 70T3339/19/99 S166 Com'l & Ind | | 70T3339/19/99 S133 Com'l & Ind | | |
|---|---|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Unit** |
| $t_{CYC1}$ | Clock Cycle Time (Flow-Through)[1] | 15 | — | 20 | — | 25 | — | ns |
| $t_{CYC2}$ | Clock Cycle Time (Pipelined)[1] | 5 | — | 6 | — | 7.5 | — | ns |
| $t_{CH1}$ | Clock High Time (Flow-Through)[1] | 6 | — | 8 | — | 10 | — | ns |
| $t_{CL1}$ | Clock Low Time (Flow-Through)[1] | 6 | — | 8 | — | 10 | — | ns |
| $t_{CH2}$ | Clock High Time (Pipelined)[2] | 2 | — | 2.4 | — | 3 | — | ns |
| $t_{CL2}$ | Clock Low Time (Pipelined)[1] | 2 | — | 2.4 | — | 3 | — | ns |
| $t_{SA}$ | Address Setup Time | 1.5 | — | 1.7 | — | 1.8 | — | ns |
| $t_{HA}$ | Address Hold Time | 0.5 | — | 0.5 | — | 0.5 | — | ns |
| $t_{SC}$ | Chip Enable Setup Time | 1.5 | — | 1.7 | — | 1.8 | — | ns |
| $t_{HC}$ | Chip Enable Hold Time | 0.5 | — | 0.5 | — | 0.5 | — | ns |
| $t_{SB}$ | Byte Enable Setup Time | 1.5 | — | 1.7 | — | 1.8 | — | ns |
| $t_{HB}$ | Byte Enable Hold Time | 0.5 | — | 0.5 | — | 0.5 | — | ns |
| $t_{SW}$ | R/W Setup Time | 1.5 | — | 1.7 | — | 1.8 | — | ns |
| $t_{HW}$ | R/W Hold Time | 0.5 | — | 0.5 | — | 0.5 | — | ns |
| $t_{SD}$ | Input Data Setup Time | 1.5 | — | 1.7 | — | 1.8 | — | ns |
| $t_{HD}$ | Input Data Hold Time | 0.5 | — | 0.5 | — | 0.5 | — | ns |
| $t_{SAD}$ | $\overline{ADS}$ Setup Time | 1.5 | — | 1.7 | — | 1.8 | — | ns |
| $t_{HAD}$ | $\overline{ADS}$ Hold Time | 0.5 | — | 0.5 | — | 0.5 | — | ns |
| $t_{SCN}$ | $\overline{CNTEN}$ Setup Time | 1.5 | — | 1.7 | — | 1.8 | — | ns |
| $t_{HCN}$ | $\overline{CNTEN}$ Hold Time | 0.5 | — | 0.5 | — | 0.5 | — | ns |
| $t_{SRPT}$ | $\overline{REPEAT}$ Setup Time | 1.5 | — | 1.7 | — | 1.8 | — | ns |
| $t_{HRPT}$ | $\overline{REPEAT}$ Hold Time | 0.5 | — | 0.5 | — | 0.5 | — | ns |
| $t_{OE}$ | Output Enable to Data Valid | — | 4.4 | — | 4.4 | — | 4.6 | ns |
| $t_{OLZ}$[5] | Output Enable to Output Low-Z | 1 | — | 1 | — | 1 | — | ns |
| $t_{OHZ}$[5] | Output Enable to Output High-Z | 1 | 3.4 | 1 | 3.6 | 1 | 4.2 | ns |
| $t_{CD1}$ | Clock to Data Valid (Flow-Through)[1] | — | 10 | — | 12 | — | 15 | ns |
| $t_{CD2}$ | Clock to Data Valid (Pipelined)[1] | — | 3.4 | — | 3.6 | — | 4.2 | ns |
| $t_{DC}$ | Data Output Hold After Clock High | 1 | — | 1 | — | 1 | — | ns |
| $t_{CKHZ}$[5] | Clock High to Output High-Z | 1 | 3.4 | 1 | 3.6 | 1 | 4.2 | ns |
| $t_{CKLZ}$[5] | Clock High to Output Low-Z | 1 | — | 1 | — | 1 | — | ns |
| $t_{INS}$ | Interrupt Flag Set Time | — | 7 | — | 7 | — | 7 | ns |
| $t_{INR}$ | Interrupt Flag Reset Time | — | 7 | — | 7 | — | 7 | ns |
| $t_{COLS}$ | Collision Flag Set Time | — | 3.4 | — | 3.6 | — | 4.2 | ns |
| $t_{COLR}$ | Collision Flag Reset Time | — | 3.4 | — | 3.6 | — | 4.2 | ns |
| $t_{ZZSC}$ | Sleep Mode Set Cycles | 2 | — | 2 | — | 2 | — | cycles |
| $t_{ZZRC}$ | Sleep Mode Recovery Cycles | 3 | — | 3 | — | 3 | — | cycles |
| **Port-to-Port Delay** | | | | | | | | |
| $t_{CO}$ | Clock-to-Clock Offset | 4 | — | 5 | — | 6 | — | ns |
| $t_{OFS}$ | Clock-to-Clock Offset for Collision Detection | Please refer to Collision Detection Timing Table on Page 20 | | | | | | |

5652 tbl 11

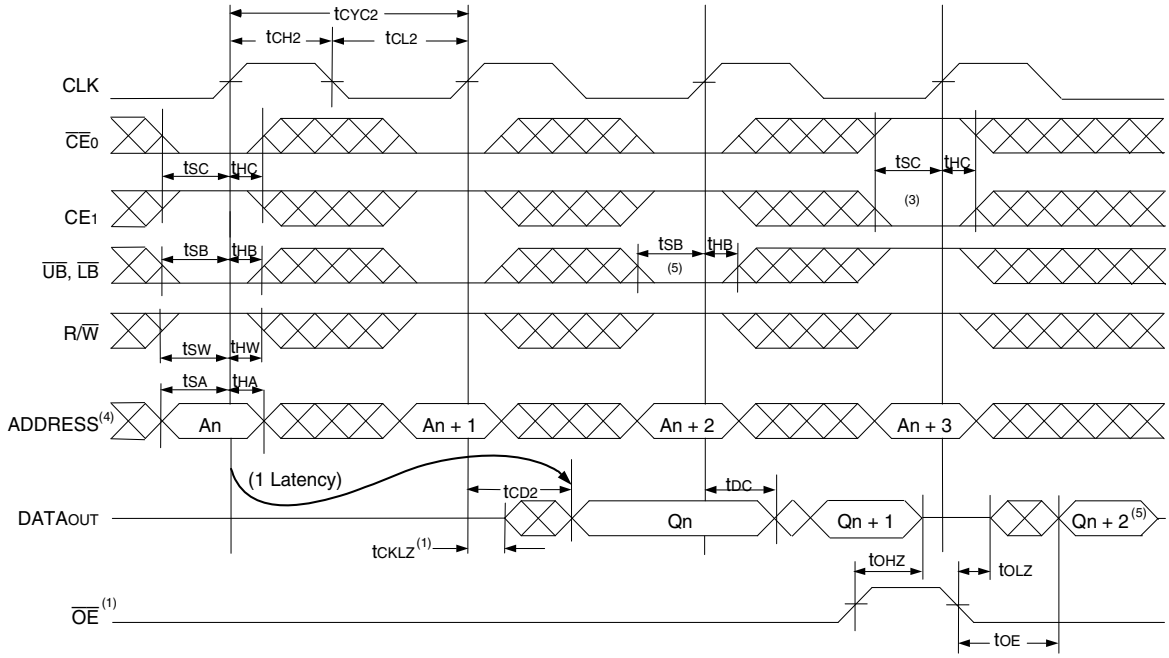
**NOTES:**

1. The Pipelined output parameters ($t_{CYC2}$, $t_{CD2}$) apply to either or both left and right ports when $\overline{FT}$/PIPEX = $V_{DD}$ (2.5V). Flow-through parameters ($t_{CYC1}$, $t_{CD1}$) apply when $\overline{FT}$/PIPE = $V_{SS}$ (0V) for that port.
2. All input signals are synchronous with respect to the clock except for the asynchronous Output Enable ($\overline{OE}$), $\overline{FT}$/PIPE and OPT. $\overline{FT}$/PIPE and OPT should be treated as DC signals, i.e. steady state during operation.
3. These values are valid for either level of $V_{DDQ}$ (3.3V/2.5V). See page 5 for details on selecting the desired operating voltage levels for each port.
4. 200Mhz is not available in BF-208 package.
5. Guaranteed by design (not production tested).



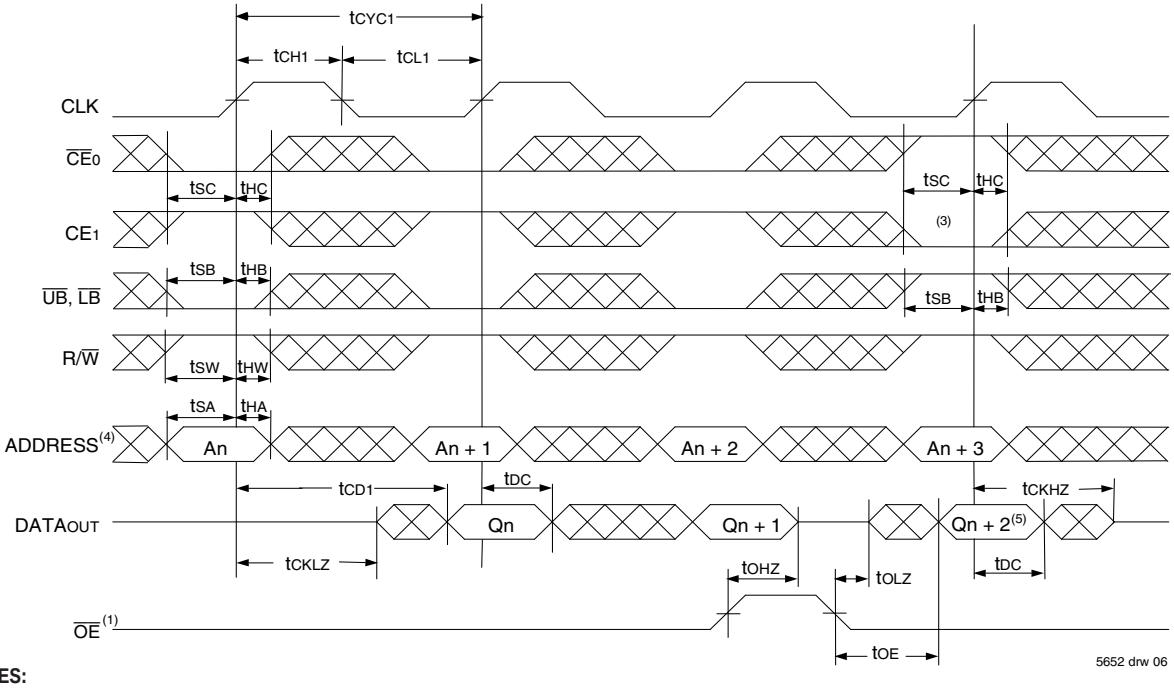
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## Timing Waveform of Read Cycle for Pipelined Operation ($\overline{FT}$/PIPE'X' = $V_{IH}$)(2)




5652 drw 05

## Timing Waveform of Read Cycle for Flow-through Output ($\overline{FT}$/PIPE"X" = $V_{IL}$)(2,6)



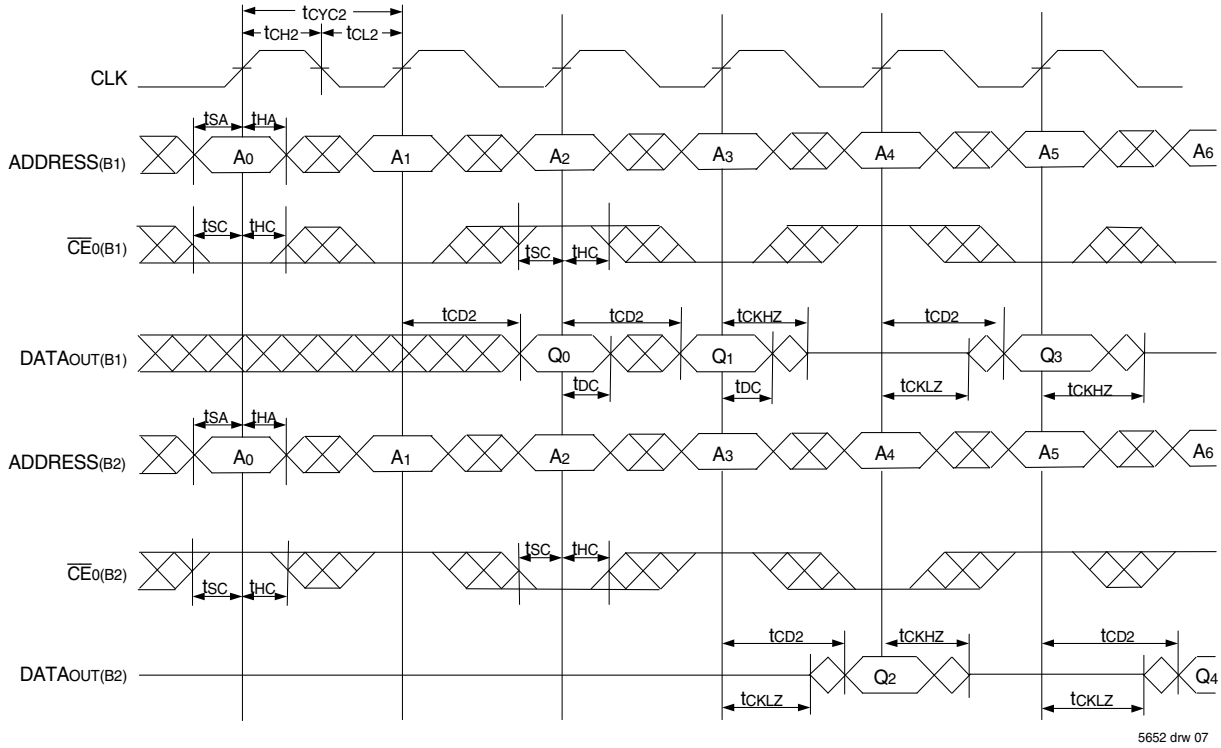

5652 drw 06

**NOTES:**
1. $\overline{OE}$ is asynchronously controlled; all other inputs depicted in the above waveforms are synchronous to the rising clock edge.
2. $\overline{ADS}$ = $V_{IL}$, $\overline{CNTEN}$ and $\overline{REPEAT}$ = $V_{IH}$.
3. The output is disabled (High-Impedance state) by $\overline{CE}_0$ = $V_{IH}$, $CE_1$ = $V_{IL}$, $\overline{UB}$, $\overline{LB}$ = $V_{IH}$ following the next rising edge of the clock. Refer to Truth Table 1.
4. Addresses do not have to be accessed sequentially since $\overline{ADS}$ = $V_{IL}$ constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
5. If $\overline{UB}$, $\overline{LB}$ was HIGH, then the appropriate Byte of $DATA_{OUT}$ for Qn + 2 would be disabled (High-Impedance state).
6. "x" denotes Left or Right port. The diagram is with respect to that port.

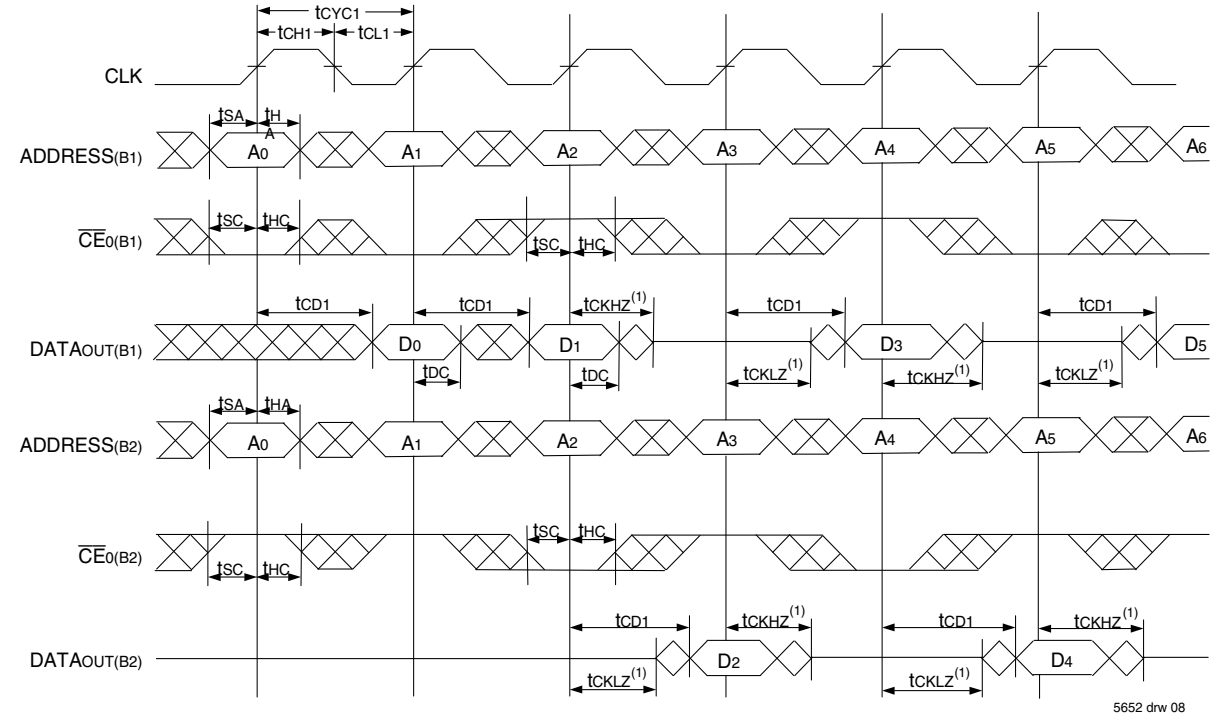


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## Timing Waveform of a Multi-Device Pipelined Read(1,2)




## Timing Waveform of a Multi-Device Flow-Through Read(1,2)



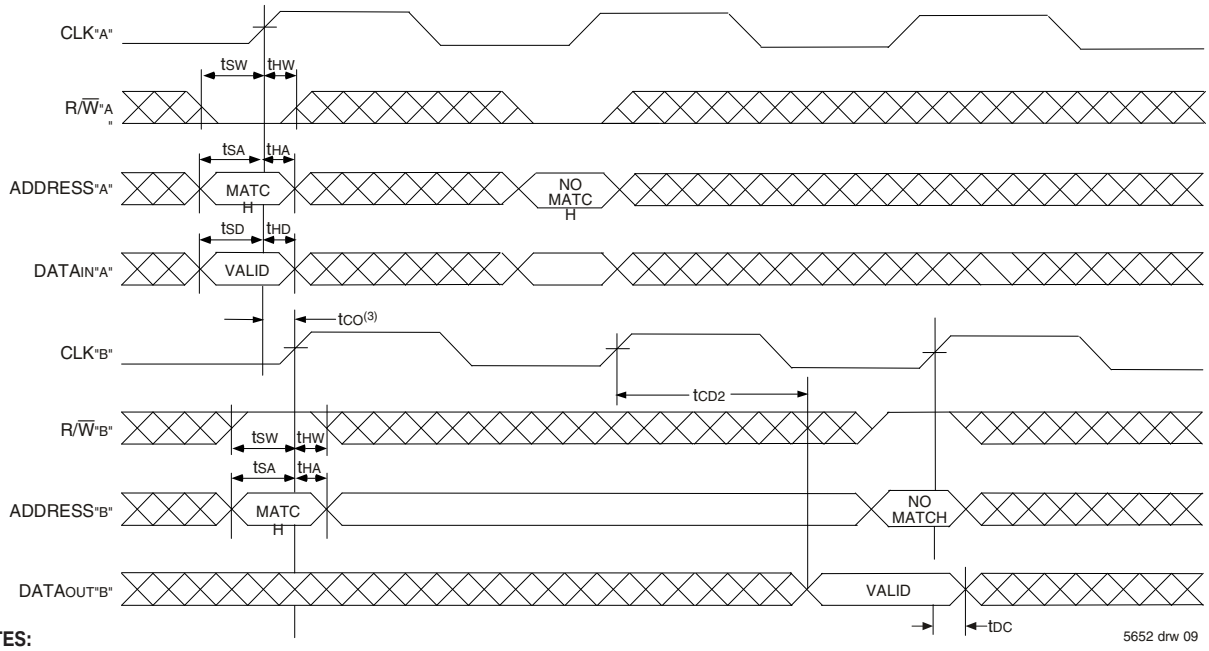

**NOTES:**

1. B1 Represents Device #1; B2 Represents Device #2. Each Device consists of one IDT70T3339/19/99 for this waveform, and are setup for depth expansion in this example. $\overline{ADDRESS}_{(B1)}$ = $\overline{ADDRESS}_{(B2)}$ in this situation.
2. $\overline{UB}$, $\overline{LB}$, $\overline{OE}$, and $\overline{ADS}$ = $V_{IL}$; $CE_{1(B1)}$, $CE_{1(B2)}$, R/$\overline{W}$, $\overline{CNTEN}$, and $\overline{REPEAT}$ = $V_{IH}$.



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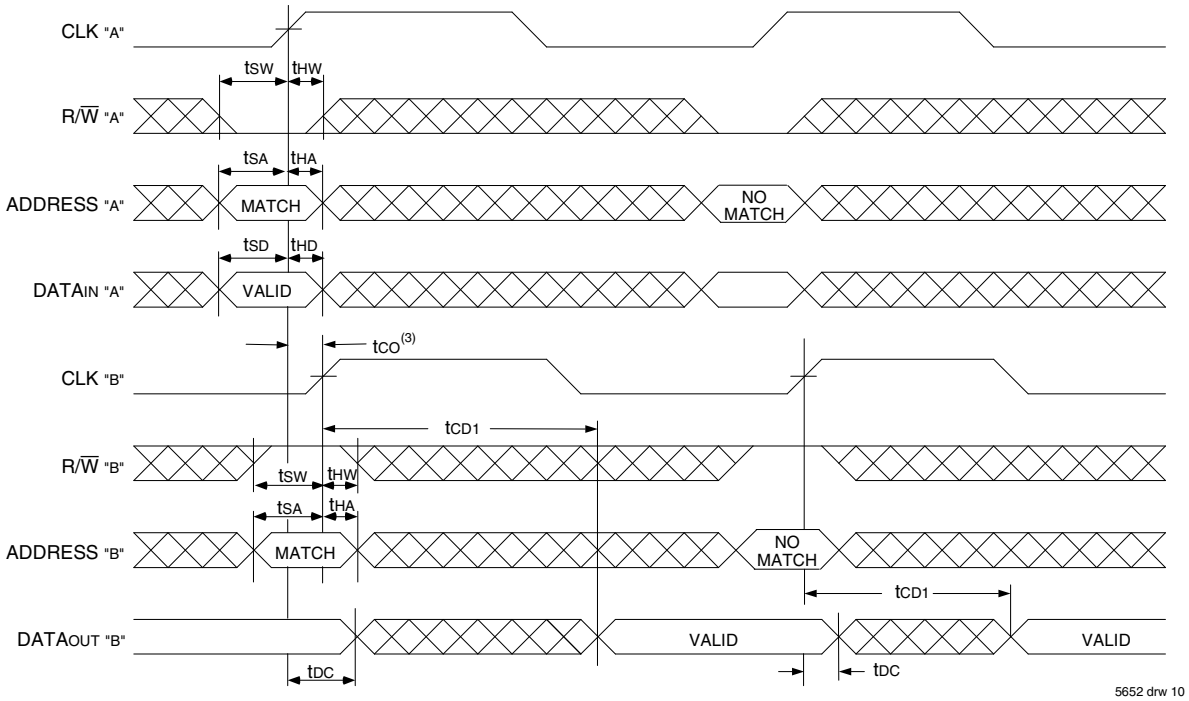
## Timing Waveform of Left Port Write to Pipelined Right Port Read(1,2,4)




**NOTES:**

1. $\overline{CE_0}$, $\overline{UB}$, $\overline{LB}$, and $\overline{ADS}$ = $V_{IL}$; $CE_1$, $\overline{CNTEN}$, and $\overline{REPEAT}$ = $V_{IH}$.
2. $\overline{OE}$ = $V_{IL}$ for Port "B", which is being read from. $\overline{OE}$ = $V_{IH}$ for Port "A", which is being written to.
3. If $t_{CO} \leq$ minimum specified, then data from Port "B" read is not valid until following Port "B" clock cycle (ie, time from write to valid read on opposite port will be $t_{CO} + 2\ t_{CYC2} + t_{CD2}$). If $t_{CO}$ > minimum, then data from Port "B" read is available on first Port "B" clock cycle (ie, time from write to valid read on opposite port will be $t_{CO} + t_{CYC2} + t_{CD2}$).
4. All timing is the same for Left and Right ports. Port "A" may be either Left or Right port. Port "B" is the opposite of Port "A"

## Timing Waveform with Port-to-Port Flow-Through Read(1,2,4)



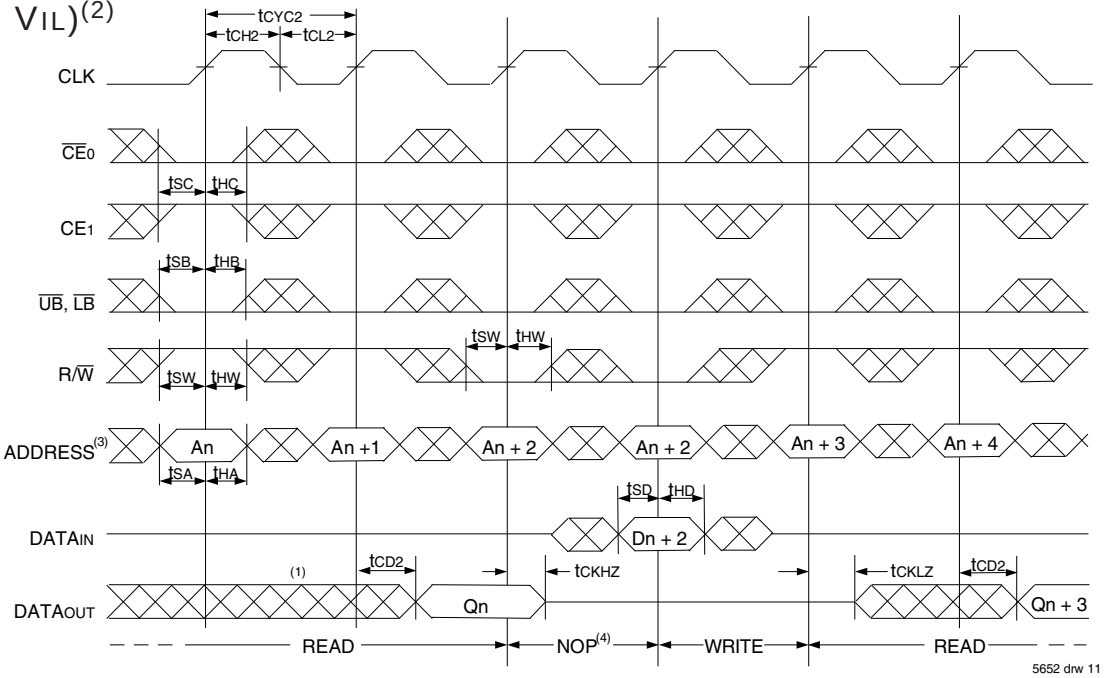

**NOTES:**

1. $\overline{CE_0}$, $\overline{UB}$, $\overline{LB}$, and $\overline{ADS}$ = $V_{IL}$; $CE_1$, $\overline{CNTEN}$, and $\overline{REPEAT}$ = $V_{IH}$.
2. $\overline{OE}$ = $V_{IL}$ for the Right Port, which is being read from. $\overline{OE}$ = $V_{IH}$ for the Left Port, which is being written to.
3. If $t_{CO} \leq$ minimum specified, then data from Port "B" read is not valid until following Port "B" clock cycle (i.e., time from write to valid read on opposite port will be $t_{CO} + t_{CYC} + t_{CD1}$). If $t_{CO}$ > minimum, then data from Port "B" read is available on first Port "B" clock cycle (i.e., time from write to valid read on opposite port will be $t_{CO} + t_{CD1}$).
4. All timing is the same for both left and right ports. Port "A" may be either left or right port. Port "B" is the opposite of Port "A".



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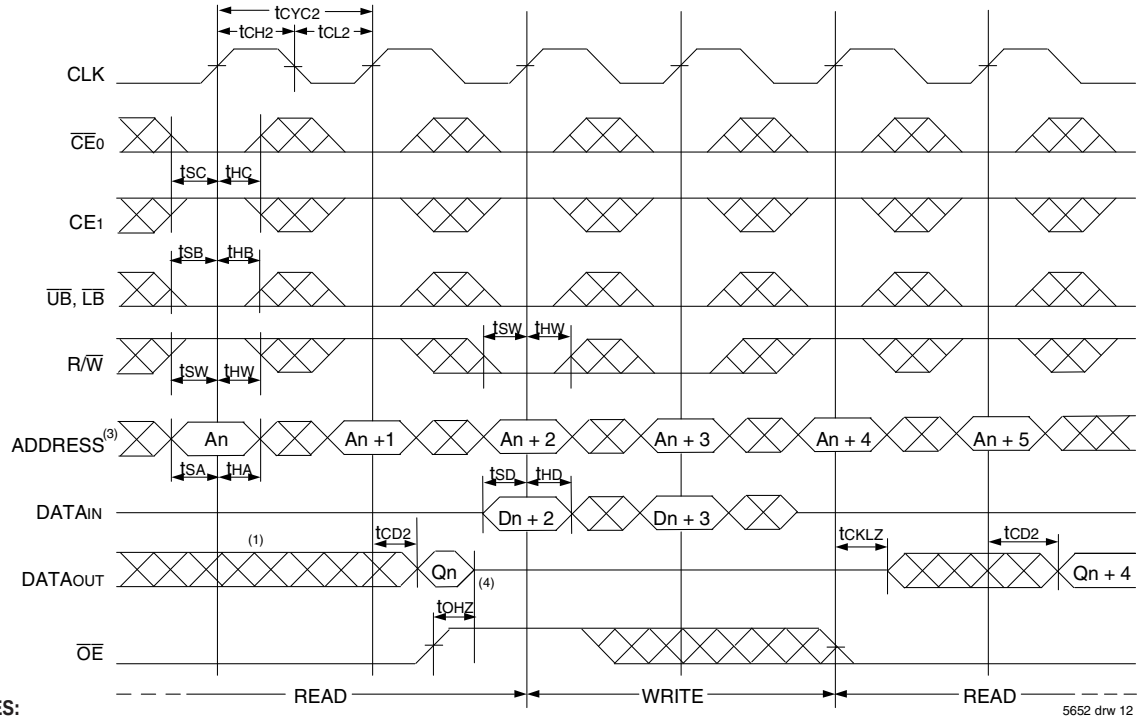
## Timing Waveform of Pipelined Read-to-Write-to-Read ($\overline{OE}$ = VIL)(2)




**NOTES:**

1. Output state (High, Low, or High-impedance) is determined by the previous cycle control signals.
2. $\overline{CE}_0$, $\overline{UB}$, $\overline{LB}$, and $\overline{ADS}$ = VIL; CE1, $\overline{CNTEN}$, and $\overline{REPEAT}$ = VIH. "NOP" is "No Operation".
3. Addresses do not have to be accessed sequentially since $\overline{ADS}$ = VIL constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
4. "NOP" is "No Operation." Data in memory at the selected address may be corrupted and should be rewritten to guarantee data integrity.

## Timing Waveform of Pipelined Read-to-Write-to-Read ($\overline{OE}$ Controlled)(2)



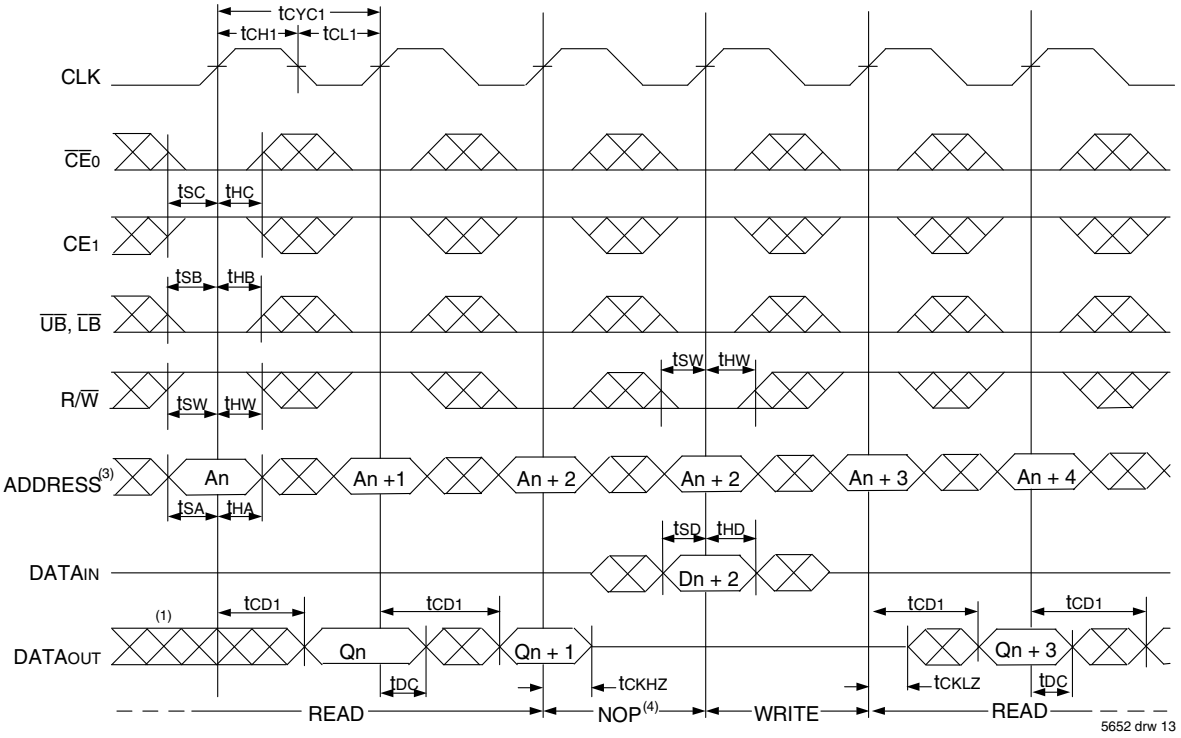

**NOTES:**

1. Output state (High, Low, or High-impedance) is determined by the previous cycle control signals.
2. $\overline{CE}_0$, $\overline{UB}$, $\overline{LB}$, and $\overline{ADS}$ = VIL; CE1, $\overline{CNTEN}$, and $\overline{REPEAT}$ = VIH.
3. Addresses do not have to be accessed sequentially since $\overline{ADS}$ = VIL constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
4. This timing does not meet requirements for fastest speed grade. This waveform indicates how logically it could be done if timing so allows.

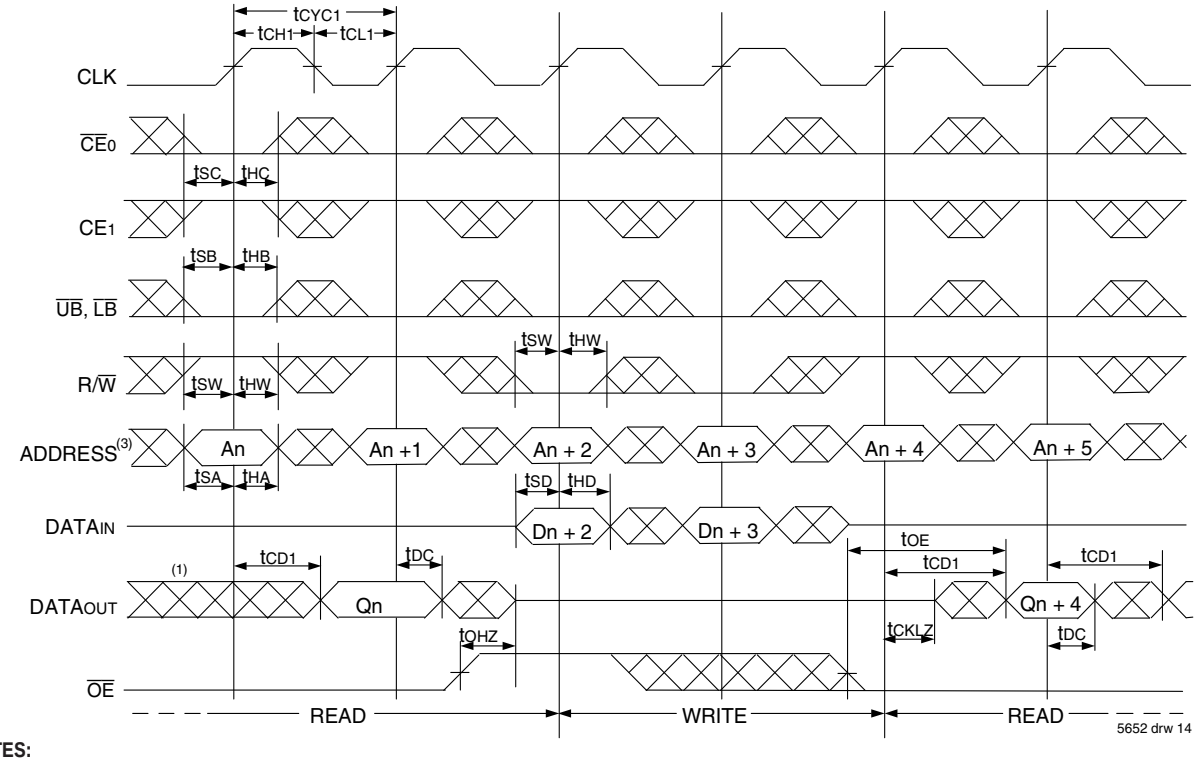


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## Timing Waveform of Flow-Through Read-to-Write-to-Read ($\overline{OE}$ = VIL)(2)




## Timing Waveform of Flow-Through Read-to-Write-to-Read ($\overline{OE}$ Controlled)(2)



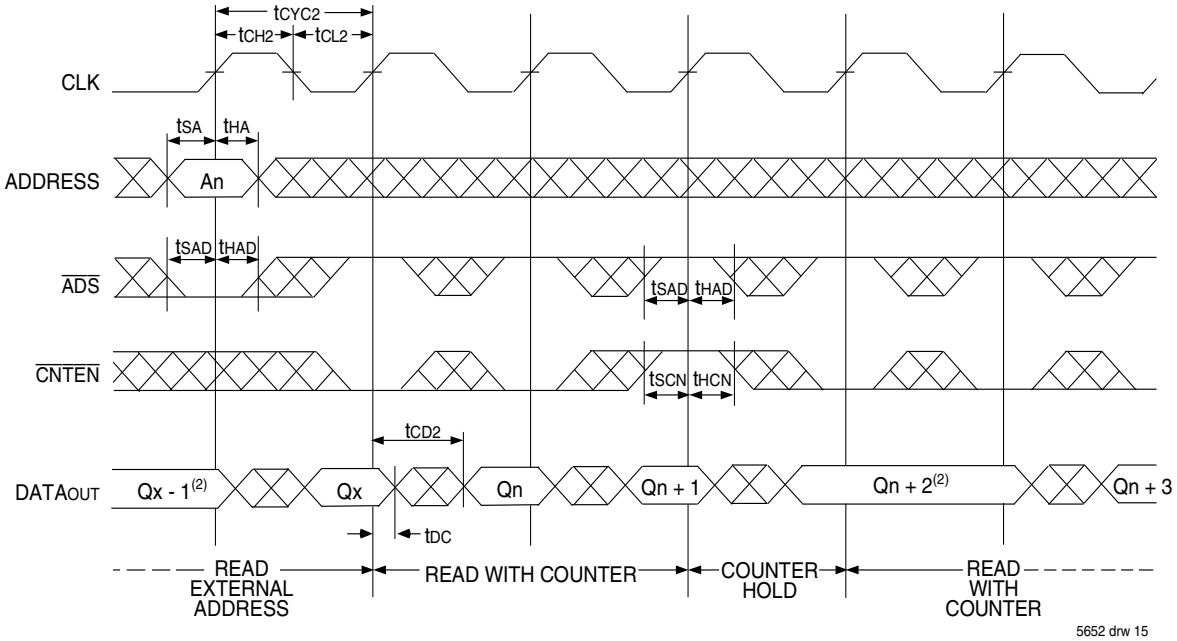

**NOTES:**

1. Output state (High, Low, or High-impedance) is determined by the previous cycle control signals.
2. $\overline{CE_0}$, $\overline{UB}$, $\overline{LB}$, and $\overline{ADS}$ = $V_{IL}$; $CE_1$, $\overline{CNTEN}$, and $\overline{REPEAT}$ = $V_{IH}$.
3. Addresses do not have to be accessed sequentially since $\overline{ADS}$ = $V_{IL}$ constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
4. "NOP" is "No Operation." Data in memory at the selected address may be corrupted and should be rewritten to guarantee data integrity.

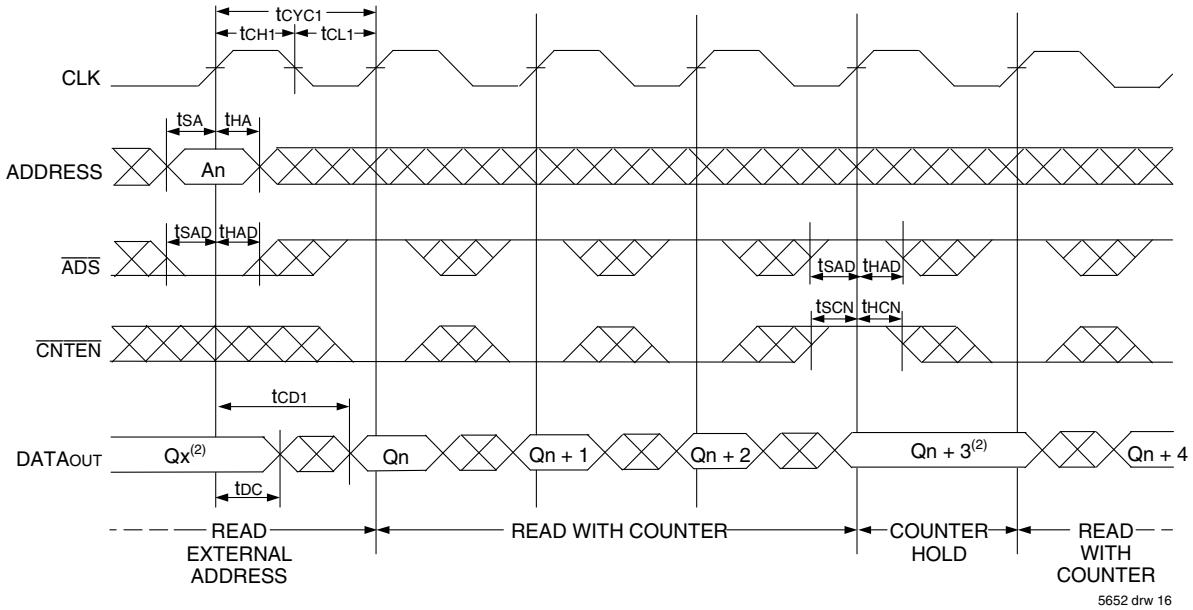


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## Timing Waveform of Pipelined Read with Address Counter Advance(1)




## Timing Waveform of Flow-Through Read with Address Counter Advance(1)

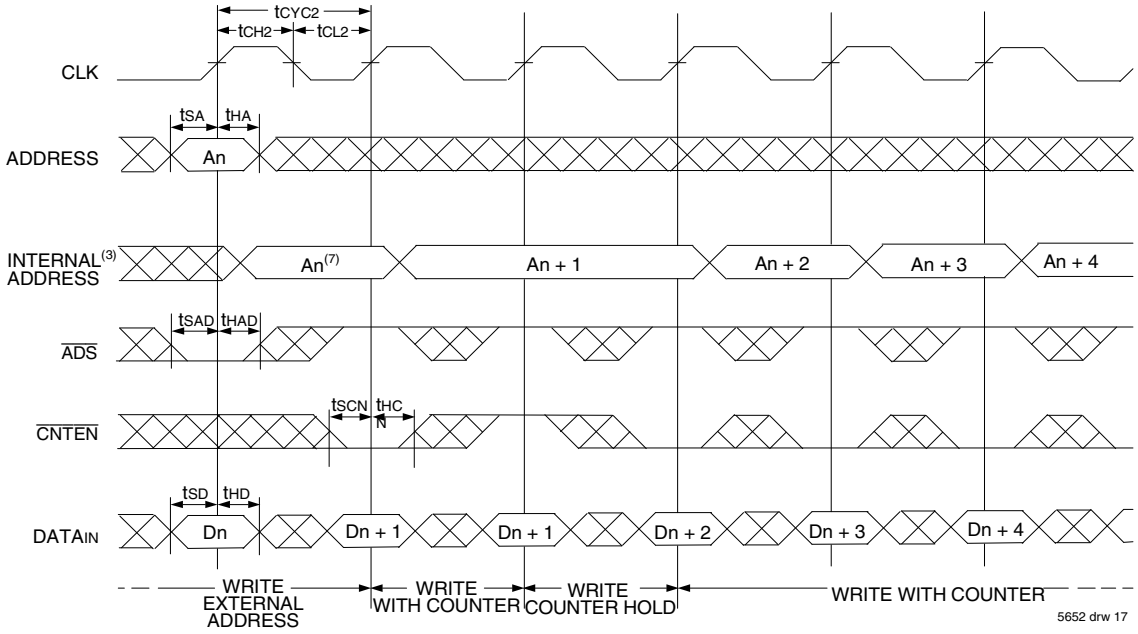



**NOTES:**
1. $\overline{CE_0}$, $\overline{OE}$, $\overline{UB}$, $\overline{LB}$ = $V_{IL}$; $CE_1$, R/$\overline{W}$, and $\overline{REPEAT}$ = $V_{IH}$.
2. If there is no address change via $\overline{ADS}$ = $V_{IL}$ (loading a new address) or $\overline{CNTEN}$ = $V_{IL}$ (advancing the address), i.e. $\overline{ADS}$ = $V_{IH}$ and $\overline{CNTEN}$ = $V_{IH}$, then the data output remains constant for subsequent clocks.

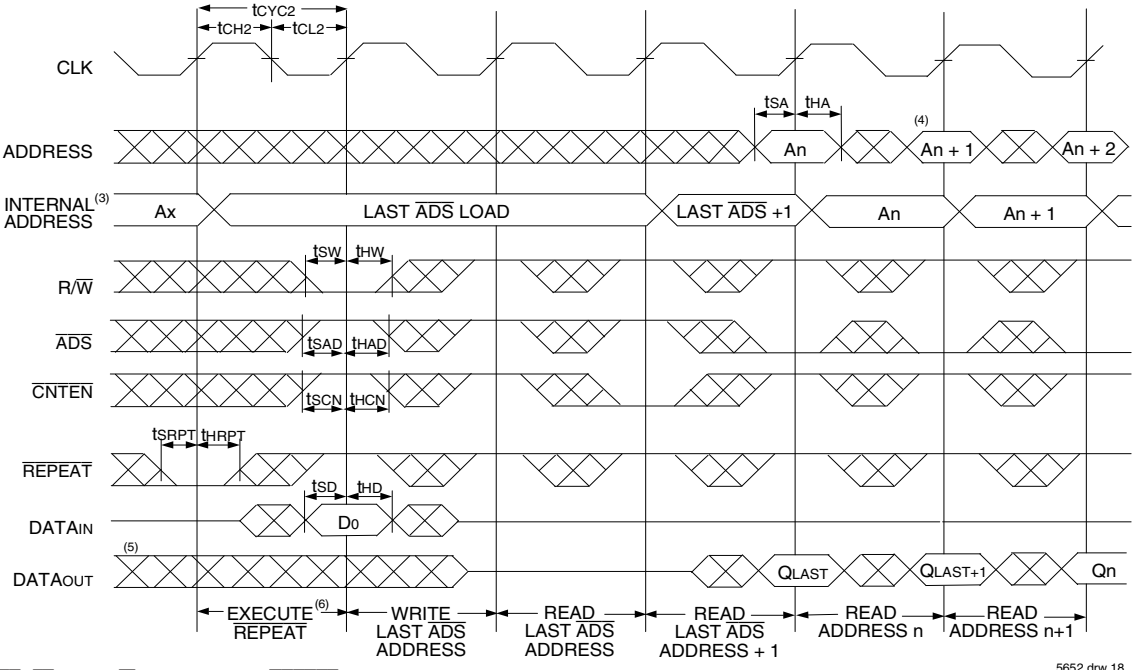


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## Timing Waveform of Write with Address Counter Advance (Flow-through or Pipelined Inputs)(1)




## Timing Waveform of Counter Repeat(2)



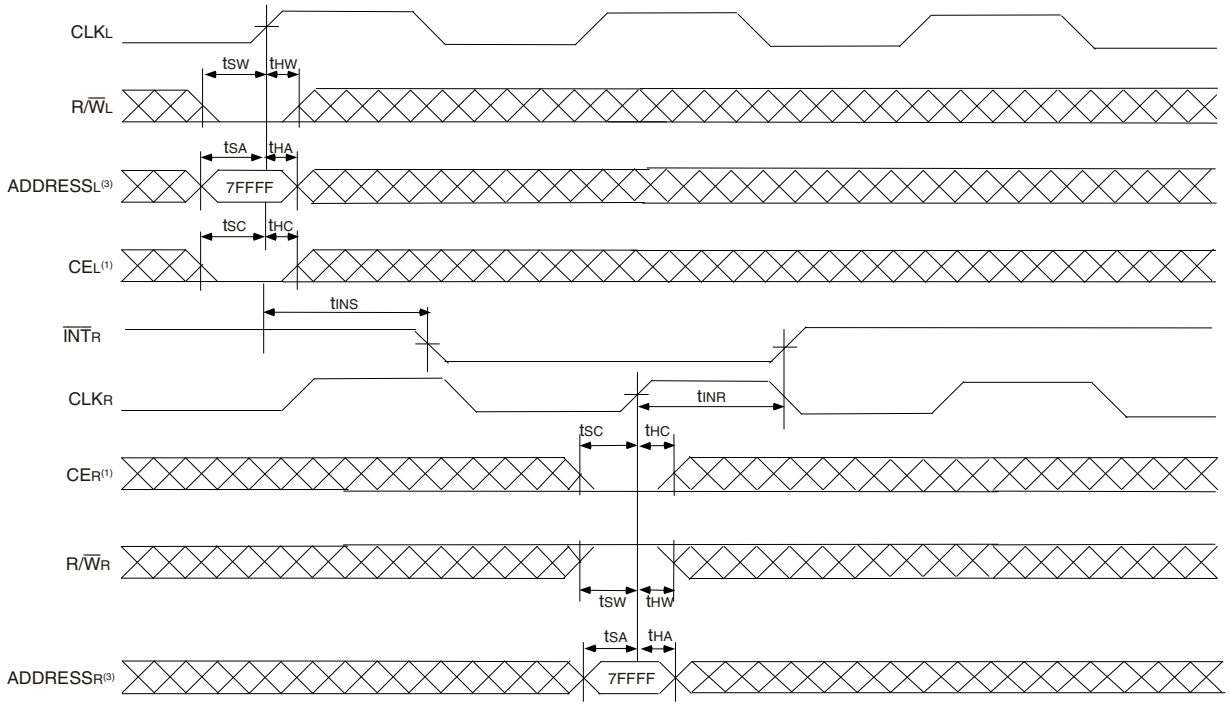

**NOTES:**

1. $\overline{CE_0}$, $\overline{UB}$, $\overline{LB}$, and R/$\overline{W}$ = $V_{IL}$; $CE_1$ and $\overline{REPEAT}$ = $V_{IH}$.
2. $\overline{CE_0}$, $\overline{UB}$, $\overline{LB}$ = $V_{IL}$; $CE_1$ = $V_{IH}$.
3. The "Internal Address" is equal to the "External Address" when $\overline{ADS}$ = $V_{IL}$ and equals the counter output when $\overline{ADS}$ = $V_{IH}$.
4. Addresses do not have to be accessed sequentially since $\overline{ADS}$ = $V_{IL}$ constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
5. Output state (High, Low, or High-impedance) is determined by the previous cycle control signals.
6. No dead cycle exists during $\overline{REPEAT}$ operation. A READ or WRITE cycle may be coincidental with the counter $\overline{REPEAT}$ cycle: Address loaded by last valid $\overline{ADS}$ load will be accessed. Extra cycles are shown here simply for clarification. For more information on $\overline{REPEAT}$ function refer to Truth Table II.
7. $\overline{CNTEN}$ = $V_{IL}$ advances Internal Address from 'An' to 'An +1'. The transition shown indicates the time required for the counter to advance. The 'An +1'Address is written to during this cycle.



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## Waveform of Interrupt Timing (2)




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**NOTES:**
1. $\overline{CE_0}$ = $V_{IL}$ and $CE_1$ = $V_{IH}$
2. All timing is the same for Left and Right ports.
3. Address is for internal register, not the external bus, i.e., address needs to be qualified by one of the Address counter control signals.

## Truth Table III — Interrupt Flag (1)

| Left Port | | | | | Right Port | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| $CLK_L$ | $R/\overline{W}_L$(2) | $CE_L$(2) | $A_{18L}$-$A_{0L}$(3,4,5) | $\overline{INT}_L$ | $CLK_R$ | $R/\overline{W}_R$(2) | $CE_R$(2) | $A_{18R}$-$A_{0R}$(3,4,5) | $\overline{INT}_R$ | Function |
| ↑ | L | L | 7FFFF | X | ↑ | X | X | X | L | Set Right $\overline{INT}_R$ Flag |
| ↑ | X | X | X | X | ↑ | H | L | 7FFFF | H | Reset Right $\overline{INT}_R$ Flag |
| ↑ | X | X | X | L | ↑ | L | L | 7FFFE | X | Set Left $\overline{INT}_L$ Flag |
| ↑ | H | L | 7FFFE | H | ↑ | X | X | X | X | Reset Left $\overline{INT}_L$ Flag |

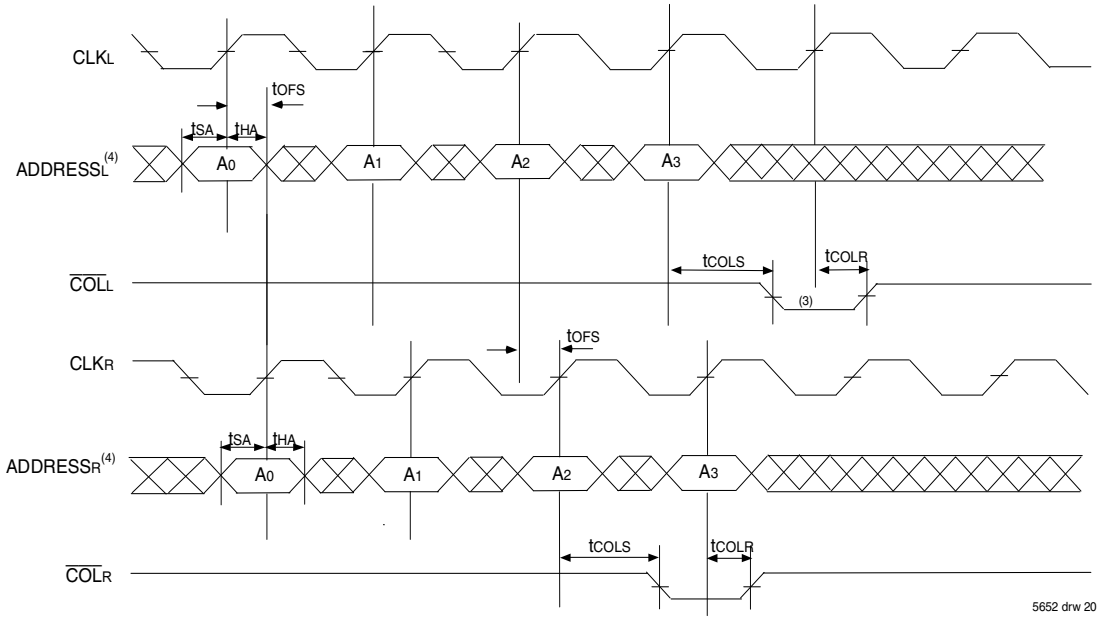
5652 tbl 12

**NOTES:**
1. $\overline{INT}_L$ and $\overline{INT}_R$ must be initialized at power-up by Resetting the flags.
2. $\overline{CE_0}$ = $V_{IL}$ and $CE_1$ = $V_{IH}$. $R/\overline{W}$ and CE are synchronous with respect to the clock and need valid set-up and hold times.
3. A18x is a NC for IDT70T3319, therefore Interrupt Addresses are 3FFFF and 3FFFE.
4. A18x and A17x are NC's for IDT70T3399, therefore Interrupt Addresses are 1FFFF and 1FFFE.
5. Address is for internal register, not the external bus, i.e., address needs to be qualified by one of the Address counter control signals.



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## Waveform of Collision Timing (1,2)
## Both Ports Writing with Left Port Clock Leading




**NOTES:**
1. $\overline{CE_0}$ = $V_{IL}$, $CE_1$ = $V_{IH}$.
2. For reading port, $\overline{OE}$ is a Don't care on the Collision Detection Logic. Please refer to Truth Table IV for specific cases.
3. Leading Port Output flag might output $3t_{CYC2} + t_{COLS}$ after Address match.
4. Address is for internal register, not the external bus, i.e., address needs to be qualified by one of the Address counter control signals.

## Collision Detection Timing(3,4)

| Cycle Time | $t_{OFS}$ (ns) | |
|---|---|---|
| | Region 1 (ns) (1) | Region 2 (ns) (2) |
| 5ns | 0 - 2.8 | 2.81 - 4.6 |
| 6ns | 0 - 3.8 | 3.81 - 5.6 |
| 7.5ns | 0 - 5.3 | 5.31 - 7.1 |

5652 tbl 13

**NOTES:**
1. Region 1
   Both ports show collision after 2nd cycle for Addresses 0, 2, 4 etc.
2. Region 2
   Leading port shows collision after 3rd cycle for addresses 0, 3, 6, etc. while trailing port shows collision after 2nd cycle for addresses 0, 2, 4 etc.
3. All the production units are tested to midpoint of each region.
4. These ranges are based on characterization of a typical device.

## Truth Table IV — Collision Detection Flag

| Left Port | | | | | Right Port | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| $CLK_L$ | $R/\overline{W}_L$(1) | $CE_L$(1) | $A_{18L}$-$A_{0L}$(2) | $\overline{COL}_L$ | $CLK_R$ | $R/\overline{W}_R$(1) | $CE_R$(1) | $A_{18R}$-$A_{0R}$(2) | $\overline{COL}_R$ | Function |
| ↑ | H | L | MATCH | H | ↑ | H | L | MATCH | H | Both ports reading. Not a valid collision. No flag output on either port. |
| ↑ | H | L | MATCH | L | ↑ | L | L | MATCH | H | Left port reading, Right port writing. Valid collision, flag output on Left port. |
| ↑ | L | L | MATCH | H | ↑ | H | L | MATCH | L | Right port reading, Left port writing. Valid collision, flag output on Right port. |
| ↑ | L | L | MATCH | L | ↑ | L | L | MATCH | L | Both ports writing. Valid collision. Flag output on both ports. |

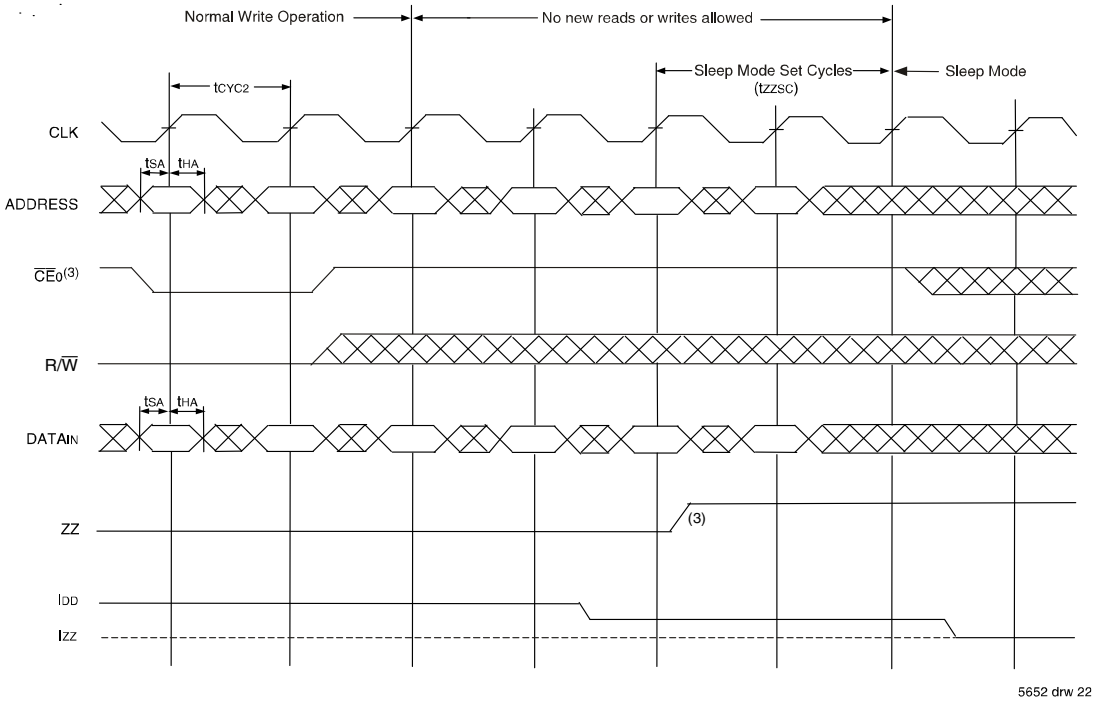
5652 tbl 14

**NOTES:**
1. $\overline{CE_0}$ = $V_{IL}$ and $CE_1$ = $V_{IH}$. $R/\overline{W}$ and CE are synchronous with respect to the clock and need valid set-up and hold times.
2. Address is for internal register, not the external bus, i.e., address needs to be qualified by one of the Address counter control signals.

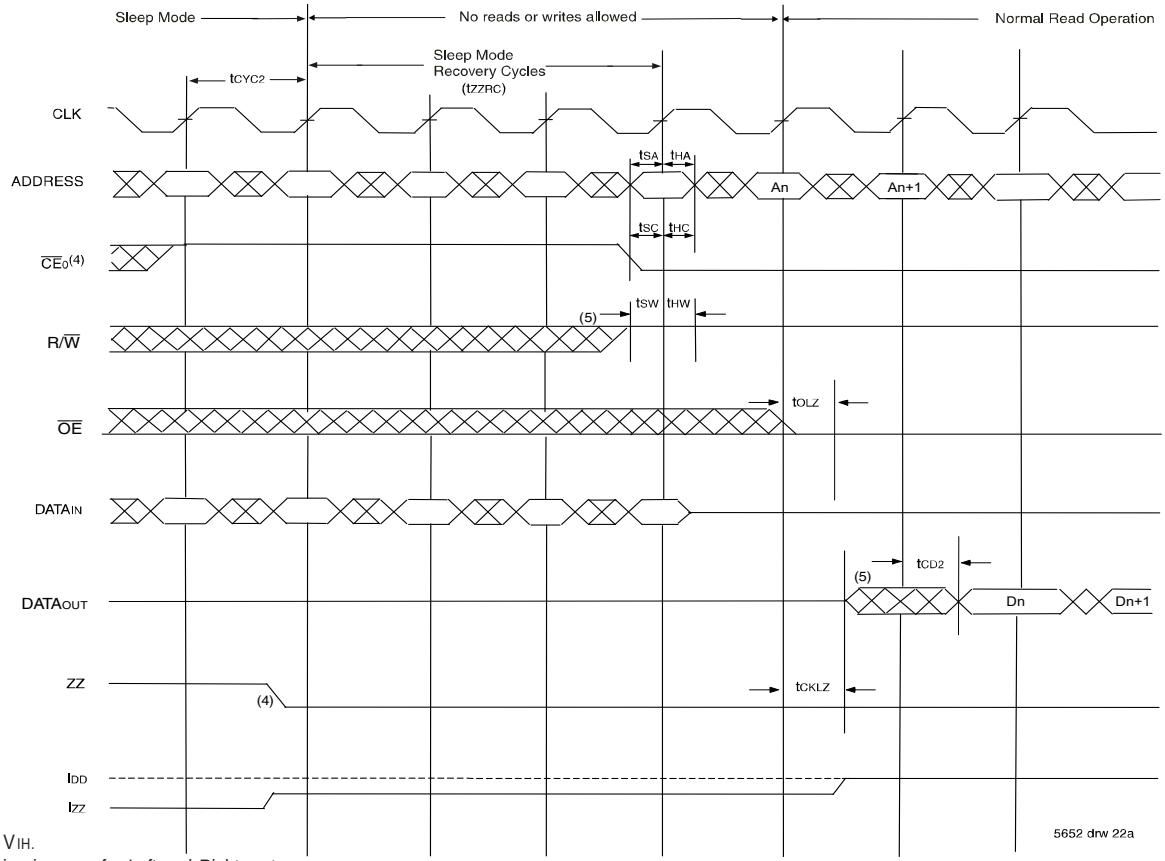


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## Timing Waveform - Entering Sleep Mode (1,2)




## Timing Waveform - Exiting Sleep Mode (1,2)




**NOTES:**

1. CE1 = VIH.
2. All timing is same for Left and Right ports.
3. $\overline{CE}_0$ has to be deactivated ($\overline{CE}_0$ = VIH) three cycles prior to asserting ZZ (ZZx = VIH) and held for two cycles after asserting ZZ (ZZx = VIH).
4. $\overline{CE}_0$ has to be deactivated ($\overline{CE}_0$ = VIH) one cycle prior to de-asserting ZZ (ZZx = VIL) and held for three cycles after de-asserting ZZ (ZZx = VIL).
5. The device must be in Read Mode (R/$\overline{W}$ High) when exiting sleep mode. Outputs are active but data is not valid until the following cycle.



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## Functional Description

The IDT70T3339/19/99 provides a true synchronous Dual-Port Static RAM interface. Registered inputs provide minimal set-up and hold times on address, data, and all critical control inputs. All internal registers are clocked on the rising edge of the clock signal, however, the self-timed internal write pulse width is independent of the cycle time.

An asynchronous output enable is provided to ease asynchronous bus interfacing. Counter enable inputs are also provided to stall the operation of the address counters for fast interleaved memory applications.

A HIGH on $\overline{CE}_0$ or a LOW on $CE_1$ for one clock cycle will power down the internal circuitry to reduce static power consumption. Multiple chip enables allow easier banking of multiple IDT70T3339/19/99s for depth expansion configurations. Two cycles are required with $\overline{CE}_0$ LOW and $CE_1$ HIGH to reactivate the outputs.

## Interrupts

If the user chooses the interrupt function, a memory location (mail box or message center) is assigned to each port. The left port interrupt flag ($\overline{INT}_L$) is asserted when the right port writes to memory location 7FFFE (HEX), where a write is defined as $\overline{CE}_R$ = R/$\overline{W}_R$ = $V_{IL}$ per the Truth Table. The left port clears the interrupt through access of address location 7FFFE when $\overline{CE}_L$ = $V_{IL}$ and R/$\overline{W}_L$ = $V_{IH}$. Likewise, the right port interrupt flag ($\overline{INT}_R$) is asserted when the left port writes to memory location 7FFFF (HEX) and to clear the interrupt flag ($\overline{INT}_R$), the right port must read the memory location 7FFFF (3FFFF or 3FFFE for IDT70T3319 and 1FFFF or 1FFFE for IDT70T3399). The message (18 bits) at 7FFFE or 7FFFF (3FFFF or 3FFFE for IDT70T3319 and 1FFFF or 1FFFE for IDT70T3399) is user-defined since it is an addressable SRAM location. If the interrupt function is not used, address locations 7FFFE and 7FFFF (3FFFF or 3FFFE for IDT70T3319 and 1FFFF or 1FFFE for IDT70T3399) are not used as mail boxes, but as part of the random access memory. Refer to Truth Table III for the interrupt operation.

## Collision Detection

Collision is defined as an overlap in access between the two ports resulting in the potential for either reading or writing incorrect data to a specific address. For the specific cases: (a) Both ports reading - no data is corrupted, lost, or incorrectly output, so no collision flag is output on either port. (b) One port writing, the other port reading - the end result of the write will still be valid. However, the reading port might capture data that is in a state of transition and hence the reading port's collision flag is output. (c) Both ports writing - there is a risk that the two ports will interfere with each other, and the data stored in memory will not be a valid write from either port (it may essentially be a random combination of the two). Therefore, the collision flag is output on both ports. Please refer to Truth Table IV for all of the above cases.

The alert flag ($COL_X$) is asserted on the 2nd or 3rd rising clock edge of the affected port following the collision, and remains low for one cycle. Please refer to Collision Detection Timing table on page 20. During that next cycle, the internal arbitration is engaged in resetting the alert flag (this avoids a specific requirement on the part of the user to reset the alert flag). If two collisions occur on subsequent clock cycles, the second collision may not generate the appropriate alert flag. A third collision will generate the alert flag as appropriate. In the event that a user initiates a burst access on both ports with the same starting address on both ports and one or both ports writing during each access (i.e., imposes a long string of collisions on contiguous clock cycles), the alert flag will be asserted and cleared every other cycle. Please refer to the Collision Detection Timing waveform on page 20.

Collision detection on the IDT70T3339/19/99 represents a significant advance in functionality over current sync multi-ports, which have no such capability. In addition to this functionality the IDT70T3339/19/99 sustains the key features of bandwidth and flexibility. The collision detection function is very useful in the case of bursting data, or a string of accesses made to sequential addresses, in that it indicates a problem within the burst, giving the user the option of either repeating the burst or continuing to watch the alert flag to see whether the number of collisions increases above an acceptable threshold value. Offering this function on chip also allows users to reduce their need for arbitration circuits, typically done in CPLD's or FPGA's. This reduces board space and design complexity, and gives the user more flexibility in developing a solution.

## Sleep Mode

The IDT70T3339/19/99 is equipped with an optional sleep or low power mode on both ports. The sleep mode pin on both ports is asynchronous and active high. During normal operation, the ZZ pin is pulled low. When ZZ is pulled high, the port will enter sleep mode where it will meet lowest possible power conditions. The sleep mode timing diagram shows the modes of operation: Normal Operation, No Read/Write Allowed and Sleep Mode.

For normal operation all inputs must meet setup and hold times prior to sleep and after recovering from sleep. Clocks must also meet cycle high and low times during these periods. Three cycles prior to asserting ZZ (ZZx = $V_{IH}$) and three cycles after de-asserting ZZ (ZZx = $V_{IL}$), the device must be disabled via the chip enable pins. If a write or read operation occurs during these periods, the memory array may be corrupted. Validity of data out from the RAM cannot be guaranteed immediately after ZZ is asserted (prior to being in sleep). When exiting sleep mode, the device must be in Read mode (R/$\overline{W}$x = $V_{IH}$)when chip enable is asserted, and the chip enable must be valid for one full cycle before a read will result in the output of valid data.

During sleep mode the RAM automatically deselects itself. The RAM disconnects its internal clock buffer. The external clock may continue to run without impacting the RAMs sleep current ($I_{ZZ}$). All outputs will remain in high-Z state while in sleep mode. All inputs are allowed to toggle. The RAM will not be selected and will not perform any reads or writes.



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## Depth and Width Expansion

The IDT70T3339/19/99 features dual chip enables (refer to Truth Table I) in order to facilitate rapid and simple depth expansion with no requirements for external logic. Figure 4 illustrates how to control the various chip enables in order to expand two devices in depth.

The IDT70T3339/19/99 can also be used in applications requiring expanded width, as indicated in Figure 4. Through combining the control signals, the devices can be grouped as necessary to accommodate applications needing 36-bits or wider.

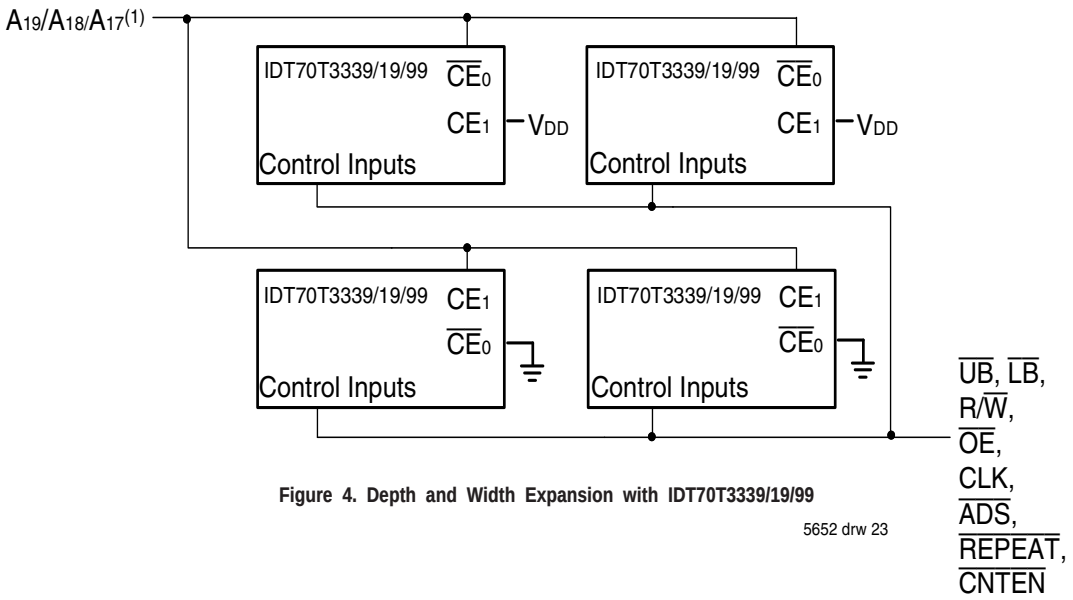



**Figure 4. Depth and Width Expansion with IDT70T3339/19/99**

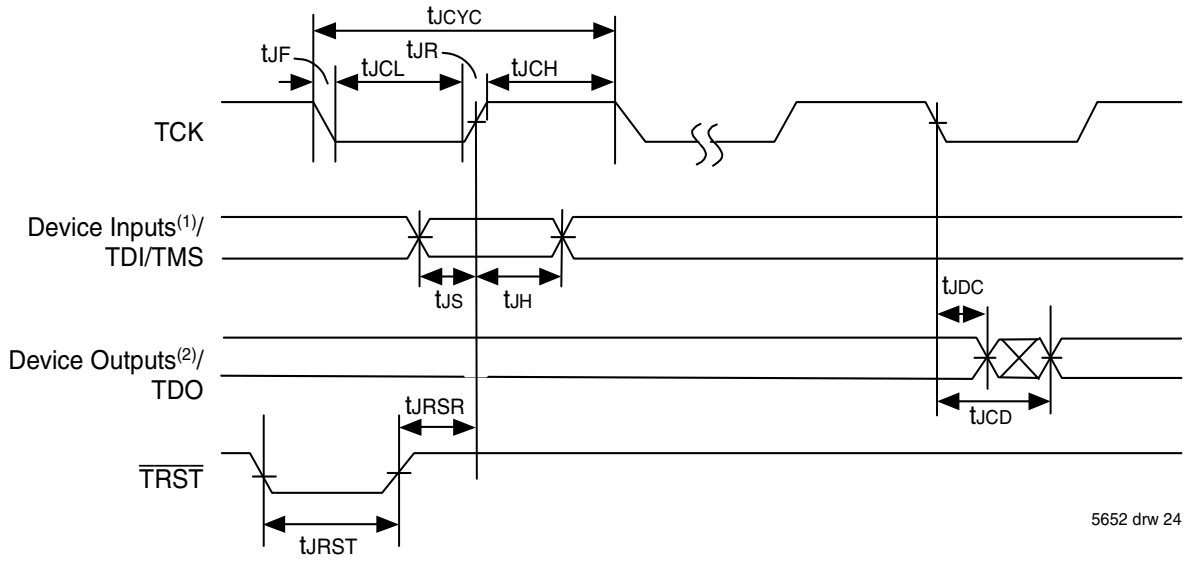
5652 drw 23

**NOTE:**
1. $A_{19}$ is for IDT70T3339, $A_{18}$ is for IDT70T3319, $A_{17}$ is for IDT70T3399.



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## JTAG Timing Specifications




**NOTES:**
1. Device inputs = All device inputs except TDI, TMS, and TRST.
2. Device outputs = All device outputs except TDO.

## JTAG AC Electrical Characteristics (1,2,3,4)

| Symbol | Parameter | 70T3339/19/99 | | |
|---|---|---|---|---|
| | | Min. | Max. | Units |
| tJCYC | JTAG Clock Input Period | 100 | — | ns |
| tJCH | JTAG Clock HIGH | 40 | — | ns |
| tJCL | JTAG Clock Low | 40 | — | ns |
| tJR | JTAG Clock Rise Time | — | 3(1) | ns |
| tJF | JTAG Clock Fall Time | — | 3(1) | ns |
| tJRST | JTAG Reset | 50 | — | ns |
| tJRSR | JTAG Reset Recovery | 50 | — | ns |
| tJCD | JTAG Data Output | — | 25 | ns |
| tJDC | JTAG Data Output Hold | 0 | — | ns |
| tJS | JTAG Setup | 15 | — | ns |
| tJH | JTAG Hold | 15 | — | ns |

5652 tbl 15

**NOTES:**
1. Guaranteed by design.
2. 30pF loading on external output signals.
3. Refer to AC Electrical Test Conditions stated earlier in this document.
4. JTAG operations occur at one speed (10MHz). The base device may run at any speed specified in this datasheet.



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## Identification Register Definitions

| Instruction Field | Value | Description |
|---|---|---|
| Revision Number (31:28) | 0x0 | Reserved for version number |
| IDT Device ID (27:12) | 0x333(1) | Defines IDT part number |
| IDT JEDEC ID (11:1) | 0x33 | Allows unique identification of device vendor as IDT |
| ID Register Indicator Bit (Bit 0) | 1 | Indicates the presence of an ID register |

5652 tbl 16

**NOTE:**
1. Device ID for IDT70T3319 is 0x334. Device ID for IDT70T3399 is 0x335.

## Scan Register Sizes

| Register Name | Bit Size |
|---|---|
| Instruction (IR) | 4 |
| Bypass (BYR) | 1 |
| Identification (IDR) | 32 |
| Boundary Scan (BSR) | Note (3) |

5652 tbl 17

## System Interface Parameters

| Instruction | Code | Description |
|---|---|---|
| EXTEST | 0000 | Forces contents of the boundary scan cells onto the device outputs(1). Places the boundary scan register (BSR) between TDI and TDO. |
| BYPASS | 1111 | Places the bypass register (BYR) between TDI and TDO. |
| IDCODE | 0010 | Loads the ID register (IDR) with the vendor ID code and places the register between TDI and TDO. |
| HIGHZ | 0100 | Places the bypass register (BYR) between TDI and TDO. Forces all device output drivers to a High-Z state except $\overline{COL}$x & $\overline{INT}$x outputs. |
| CLAMP | 0011 | Uses BYR. Forces contents of the boundary scan cells onto the device outputs. Places the bypass register (BYR) between TDI and TDO. |
| SAMPLE/PRELOAD | 0001 | Places the boundary scan register (BSR) between TDI and TDO. SAMPLE allows data from device inputs(2) to be captured in the boundary scan cells and shifted serially through TDO. PRELOAD allows data to be input serially into the boundary scan cells via the TDI. |
| RESERVED | 0101, 0111, 1000, 1001, 1010, 1011, 1100 | Several combinations are reserved. Do not use codes other than those identified above. |
| PRIVATE | 0110,1110,1101 | For internal use only. |

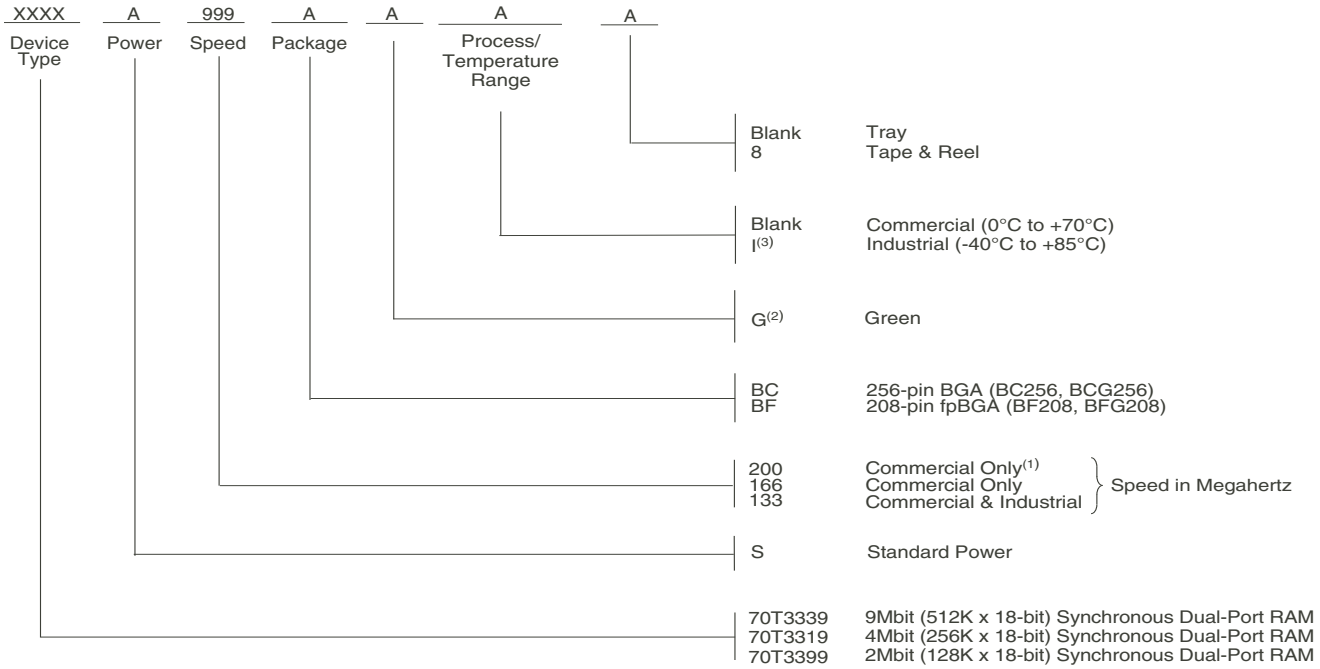
5652 tbl 18

**NOTES:**
1. Device outputs = All device outputs except TDO.
2. Device inputs = All device inputs except TDI, TMS, and $\overline{TRST}$.
3. The Boundary Scan Descriptive Language (BSDL) file for this device is available on the IDT website (www.idt.com), or by contacting your local IDT sales representative.



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## Ordering Information




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**NOTES:**
1. 200Mhz is not available in the BF-208 package.
2. Green parts available. For specific speeds, packages and powers contact your local sales office.
3. Contact your local sales office for industrial temp range for other speeds, packages and powers.
   Note that information regarding recently obsoleted parts are included in this datasheet for customer convenience.

## Orderable Part Information

| Speed (MHz) | Orderable Part ID | Pkg. Code | Pkg. Type | Temp. Grade |
|---|---|---|---|---|
| 133 | 70T3319S133BC | BC256 | CABGA | C |
| | 70T3319S133BC8 | BC256 | CABGA | C |
| | 70T3319S133BF | BF208 | CABGA | C |
| | 70T3319S133BF8 | BF208 | CABGA | C |
| | 70T3319S133BFGI | BFG208 | CABGA | I |
| | 70T3319S133BFGI8 | BFG208 | CABGA | I |
| | 70T3319S133BFI | BF208 | CABGA | I |
| | 70T3319S133BFI8 | BF208 | CABGA | I |
| 166 | 70T3319S166BC | BC256 | CABGA | C |
| | 70T3319S166BC8 | BC256 | CABGA | C |
| | 70T3319S166BF | BF208 | CABGA | C |
| | 70T3319S166BF8 | BF208 | CABGA | C |
| | 70T3319S166BFG | BFG208 | CABGA | C |
| | 70T3319S166BFG8 | BFG208 | CABGA | C |
| 200 | 70T3319S200BC | BC256 | CABGA | C |
| | 70T3319S200BC8 | BC256 | CABGA | C |

| Speed (MHz) | Orderable Part ID | Pkg. Code | Pkg. Type | Temp. Grade |
|---|---|---|---|---|
| 133 | 70T3339S133BC | BC256 | CABGA | C |
| | 70T3339S133BC8 | BC256 | CABGA | C |
| | 70T3339S133BCI | BC256 | CABGA | I |
| | 70T3339S133BCI8 | BC256 | CABGA | I |
| | 70T3339S133BF | BF208 | CABGA | C |
| | 70T3339S133BF8 | BF208 | CABGA | C |
| | 70T3339S133BFGI | BFG208 | CABGA | I |
| | 70T3339S133BFI | BF208 | CABGA | I |
| | 70T3339S133BFI8 | BF208 | CABGA | I |
| 166 | 70T3339S166BC | BC256 | CABGA | C |
| | 70T3339S166BC8 | BC256 | CABGA | C |
| | 70T3339S166BF | BF208 | CABGA | C |
| | 70T3339S166BF8 | BF208 | CABGA | C |
| 200 | 70T3339S200BC | BC256 | CABGA | C |
| | 70T3339S200BC8 | BC256 | CABGA | C |
| | 70T3339S200BCG | BCG256 | CABGA | C |



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## Orderable Part Information (con't)

| Speed (MHz) | Orderable Part ID | Pkg. Code | Pkg. Type | Temp. Grade |
|---|---|---|---|---|
| 133 | 70T3399S133BC | BC256 | CABGA | C |
| | 70T3399S133BC8 | BC256 | CABGA | C |
| | 70T3399S133BFI | BF208 | CABGA | I |
| | 70T3399S133BFI8 | BF208 | CABGA | I |
| 166 | 70T3399S166BC | BC256 | CABGA | C |
| | 70T3399S166BC8 | BC256 | CABGA | C |
| 200 | 70T3399S200BC | BC256 | CABGA | C |
| | 70T3399S200BC8 | BC256 | CABGA | C |

## Datasheet Document History

01/20/03: Initial Datasheet

04/25/03: Page 11 Added Capacitance Derating drawing
Page 12 Changed $t_{INS}$ and $t_{INR}$ specs in AC Electrical Characteristics table

11/11/03: Page 10 Updated power numbers in DC Electrical Characteristics table
Page 12 Added $t_{OFS}$ symbol and parameter to AC Electrical Characteristics table
Page 21 Updated Collision Timing waveform
Page 22 Added Collision Detection Timing table and footnotes
Page 26 Updated HIGHZ function in System Interface Parameters table
Page 27 Added IDT Clock Solution table

04/08/04: Page 22 & 23 Clarified Sleep Mode Text and Waveforms
Page 1 & 28 Removed Preliminary status
Page 6 Added another sentence to footnote 4 to recommend that boundary scan not be operated during sleep mode

02/07/06: Page 1 Added green availability to features
Page 7 Changed footnote 2 for Truth Table I from $\overline{ADS}$, $\overline{CNTEN}$, $\overline{REPEAT}$ = $V_{IH}$ to $\overline{ADS}$, $\overline{CNTEN}$, $\overline{REPEAT}$ = X
Page 27 Added green indicator to ordering information

07/28/08: Page 10 Corrected a typo in the DC Chars table footnotes

01/19/09: Page 28 Removed "IDT" from orderable part number

04/20/10: Removed the DD 144-pin TQFP (DD-144) Thin Quad Flatpack per PDN: F-08-01

06/10/15: Page 3 & 4 Removed the date from all of the pin configurations BC256 & BF208
Page 26 Added T&R indicator and industrial temp footnote to Ordering Information

02/08/18: Product Discontinuation Notice - PDN# SP-17-02
Last time buy expires June 15, 2018

08/19/19: Page 2 & 3 Updated package codes BC-256 to BC256, BCG256 and BF-208 to BF208, BFG208
Page 1, 9 , 11 & 26 Removed 166MHz Industrial temp offering
Page 26 Removed IDT Clock Solution table
Page 26 & 27 Added Orderable Part Information tables

11/06/19: Page 26 & 27 Corrected "ns" to "MHz" in the header of the Orderable Part Information tables

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