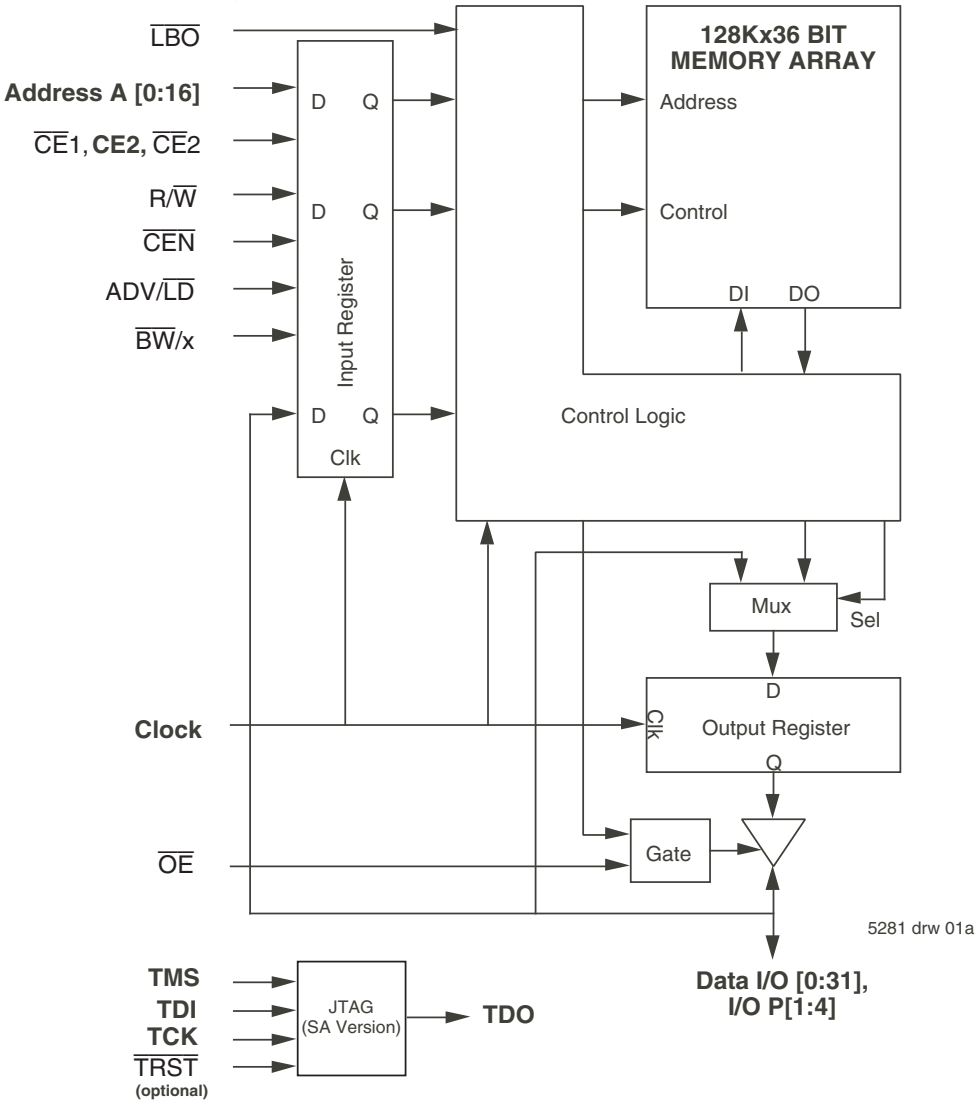
128K x 36, 256K x 18
3.3V Synchronous ZBT SRAMs
3.3V I/O, Burst Counter
Pipelined Outputs

71V3556S
71V3558S
71V3556SA
71V3558SA

Features

- 128K x 36, 256K x 18 memory configurations
- Supports high performance system speed - 166 MHz (x36) (3.5 ns Clock-to-Data Access)
- ZBT™ Feature - No dead cycles between write and read cycles
- Internally synchronized output buffer enable eliminates the need to control $\overline{OE}$
- Positive clock-edge triggered address, data, and control signal registers for fully pipelined applications
- Positive clock-edge triggered address, data, and control signal registers for fully pipelined applications
- Single R/$\overline{W}$ (READ/WRITE) control pin
- 4-word burst capability (interleaved or linear)
- Individual byte write ($\overline{BW}_1$ - $\overline{BW}_4$) control (May tie active)
- Three chip enables for simple depth expansion
- 3.3V power supply (±5%), 3.3V I/O Supply (V_{DDQ})
- Optional- Boundary Scan JTAG Interface (IEEE 1149.1 compliant)
- Packaged in a JEDEC standard 100-pin plastic thin quad flatpack (TQFP), 119 ball grid array (BGA) and 165 fine pitch ball grid array (fBGA)
- Industrial temperature range (–40°C to +85°C) is available for selected speeds
- Green parts available, see ordering information

Functional Block Diagram



ZBT® and Zero Bus Turnaround are trademarks of Renesas and the architecture is supported by Micron Technology and Motorola Inc.

Description

The IDT71V3556/58 are 3.3V high-speed 4,718,592-bit (4.5 Megabit) synchronous SRAMS. They are designed to eliminate dead bus cycles when turning the bus around between reads and writes, or writes and reads. Thus, they have been given the name ZBT™, or Zero Bus Turnaround.

Address and control signals are applied to the SRAM during one clock cycle, and two cycles later the associated data cycle occurs, be it read or write.

The IDT71V3556/58 contain data I/O, address and control signal registers. Output enable is the only asynchronous signal and can be used to disable the outputs at any given time.

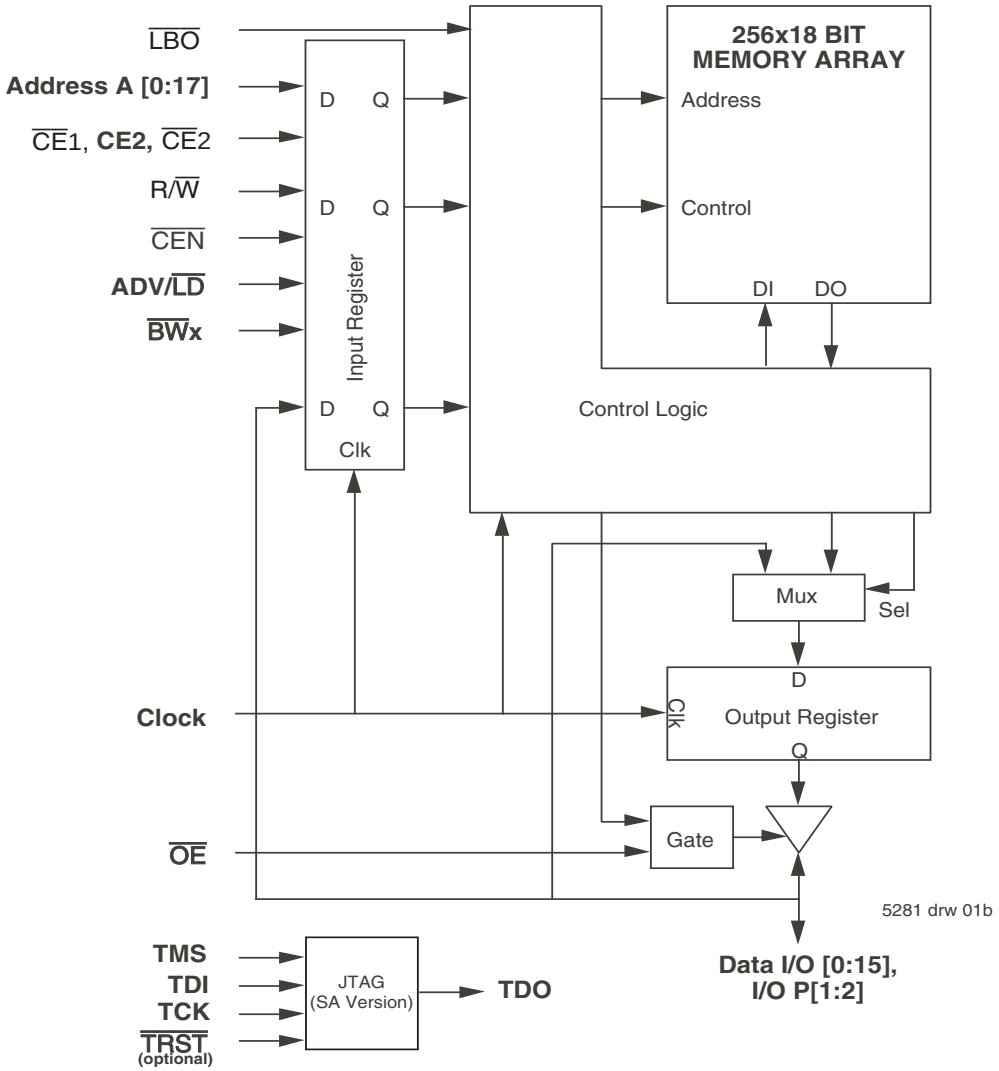
A Clock Enable ($\overline{CEN}$) pin allows operation of the IDT71V3556/58 to be suspended as long as necessary. All synchronous inputs are ignored when ($\overline{CEN}$) is high and the internal device registers will hold their previous values.

There are three chip enable pins ($\overline{CE}_1$, CE_2, $\overline{CE}_2$) that allow the user to deselect the device when desired. If any one of these three are not asserted when ADV/$\overline{LD}$ is low, no new memory operation can be initiated. However, any pending data transfers (reads or writes) will be completed. The data bus will tri-state two cycles after chip is deselected or a write is initiated.

The IDT71V3556/58 has an on-chip burst counter. In the burst mode, the IDT71V3556/58 can provide four cycles of data for a single address presented to the SRAM. The order of the burst sequence is defined by the $\overline{LBO}$ input pin. The $\overline{LBO}$ pin selects between linear and interleaved burst sequence. The ADV/$\overline{LD}$ signal is used to load a new external address (ADV/$\overline{LD}$ = LOW) or increment the internal burst counter (ADV/$\overline{LD}$ = HIGH).

The IDT71V3556/58 SRAMs utilize a high-performance CMOS process and are packaged in a JEDEC standard 14mm x 20mm 100-pin thin plastic quad flatpack (TQFP) as well as a 119 ball grid array (BGA) and a 165 fine pitch ball grid array (fBGA).

Functional Block Diagram



Pin Description Summary

A_0-A_{17}	Address Inputs	Input	Synchronous
$\overline{CE}_1$, CE_2, $\overline{CE}_2$	Chip Enables	Input	Synchronous
$\overline{OE}$	Output Enable	Input	Asynchronous
R/$\overline{W}$	Read/Write Signal	Input	Synchronous
$\overline{CEN}$	Clock Enable	Input	Synchronous
$\overline{BW}_1$, $\overline{BW}_2$, $\overline{BW}_3$, $\overline{BW}_4$	Individual Byte Write Selects	Input	Synchronous
CLK	Clock	Input	N/A
ADV/$\overline{LD}$	Advance burst address / Load new address	Input	Synchronous
$\overline{LBO}$	Linear / Interleaved Burst Order	Input	Static
TMS	Test Mode Select	Input	Synchronous
TDI	Test Data Input	Input	Synchronous
TCK	Test Clock	Input	N/A
TDO	Test Data Output	Output	Synchronous
$\overline{TRST}$	JTAG Reset (Optional)	Input	Asynchronous
ZZ	Sleep Mode	Input	Synchronous
I/O_0-I/O_{31}, I/O_{P1}-I/O_{P4}	Data Input / Output	I/O	Synchronous
V_{DD}, V_{DDQ}	Core Power, I/O Power	Supply	Static
V_{SS}	Ground	Supply	Static

5281 tbl 01

Pin Definition(1)

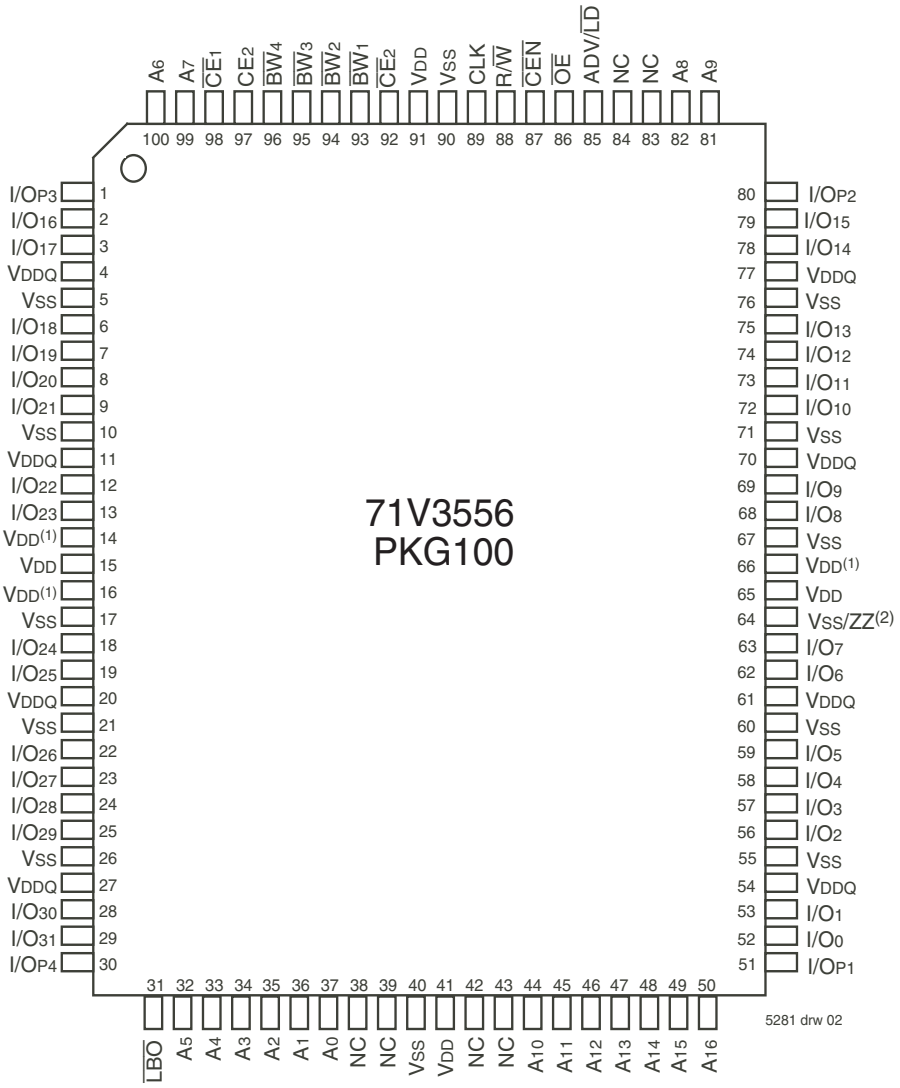
Symbol	Pin Function	I/O	Active	Description
A_0-A_{17}	Address Inputs	I	N/A	Synchronous Address inputs. The address register is triggered by a combination of the rising edge of CLK, ADV/$\overline{LD}$ low, $\overline{CEN}$ low, and true chip enables.
ADV/$\overline{LD}$	Advance / Load	I	N/A	ADV/$\overline{LD}$ is a synchronous input that is used to load the internal registers with new address and control when it is sampled low at the rising edge of clock with the chip selected. When ADV/$\overline{LD}$ is low with the chip deselected, any burst in progress is terminated. When ADV/$\overline{LD}$ is sampled high then the internal burst counter is advanced for any burst that was in progress. The external addresses are ignored when ADV/$\overline{LD}$ is sampled high.
R/$\overline{W}$	Read / Write	I	N/A	R/$\overline{W}$ signal is a synchronous input that identifies whether the current load cycle initiated is a Read or Write access to the memory array. The data bus activity for the current cycle takes place two clock cycles later.
$\overline{CEN}$	Clock Enable	I	LOW	Synchronous Clock Enable Input. When $\overline{CEN}$ is sampled high, all other synchronous inputs, including clock are ignored and outputs remain unchanged. The effect of $\overline{CEN}$ sampled high on the device outputs is as if the low to high clock transition did not occur. For normal operation, $\overline{CEN}$ must be sampled low at rising edge of clock.
$\overline{BW_1}$-$\overline{BW_4}$	Individual Byte Write Enables	I	LOW	Synchronous byte write enables. Each 9-bit byte has its own active low byte write enable. On load write cycles (When R/$\overline{W}$ and ADV/$\overline{LD}$ are sampled low) the appropriate byte write signal ($\overline{BW_1}$-$\overline{BW_4}$) must be valid. The byte write signal must also be valid on each cycle of a burst write. Byte Write signals are ignored when R/$\overline{W}$ is sampled high. The appropriate byte(s) of data are written into the device two cycles later. $\overline{BW_1}$-$\overline{BW_4}$ can all be tied low if always doing write to the entire 36-bit word.
$\overline{CE_1}$, $\overline{CE_2}$	Chip Enables	I	LOW	Synchronous active low chip enable. $\overline{CE_1}$ and $\overline{CE_2}$ are used with CE_2 to enable the IDT71V3556/58. ($\overline{CE_1}$ or $\overline{CE_2}$ sampled high or CE_2 sampled low) and ADV/$\overline{LD}$ low at the rising edge of clock, initiates a deselect cycle. The ZBT™ has a two cycle deselect, i.e., the data bus will tri-state two clock cycles after deselect is initiated.
CE_2	Chip Enable	I	HIGH	Synchronous active high chip enable. CE_2 is used with $\overline{CE_1}$ and $\overline{CE_2}$ to enable the chip. CE_2 has inverted polarity but otherwise identical to $\overline{CE_1}$ and $\overline{CE_2}$.
CLK	Clock	I	N/A	This is the clock input to the IDT71V3556/58. Except for $\overline{OE}$, all timing references for the device are made with respect to the rising edge of CLK.
I/O_0-I/O_{31} I/O_{P1}-I/O_{P4}	Data Input/Output	I/O	N/A	Synchronous data input/output (I/O) pins. Both the data input path and data output path are registered and triggered by the rising edge of CLK.
$\overline{LBO}$	Linear Burst Order	I	LOW	Burst order selection input. When $\overline{LBO}$ is high the Interleaved burst sequence is selected. When $\overline{LBO}$ is low the Linear burst sequence is selected. $\overline{LBO}$ is a static input and it must not change during device operation.
$\overline{OE}$	Output Enable	I	LOW	Asynchronous output enable. $\overline{OE}$ must be low to read data from the 71V3556/58. When $\overline{OE}$ is high the I/O pins are in a high-impedance state. $\overline{OE}$ does not need to be actively controlled for read and write cycles. In normal operation, $\overline{OE}$ can be tied low.
TMS	Test Mode Select	I	N/A	Gives input command for TAP controller. Sampled on rising edge of TDK. This pin has an internal pullup.
TDI	Test Data Input	I	N/A	Serial input of registers placed between TDI and TDO. Sampled on rising edge of TCK. This pin has an internal pullup.
TCK	Test Clock	I	N/A	Clock input of TAP controller. Each TAP event is clocked. Test inputs are captured on rising edge of TCK, while test outputs are driven from the falling edge of TCK. This pin has an internal pullup.
TDO	Test Data Output	O	N/A	Serial output of registers placed between TDI and TDO. This output is active depending on the state of the TAP controller.
$\overline{TRST}$	JTAG Reset (Optional)	I	LOW	Optional Asynchronous JTAG reset. Can be used to reset the TAP controller, but not required. JTAG reset occurs automatically at power up and also resets using TMS and TCK per IEEE 1149.1. If not used $\overline{TRST}$ can be left floating. This pin has an internal pullup. Only available in BGA package.
ZZ	Sleep Mode	I	HIGH	Synchronous sleep mode input. ZZ HIGH will gate the CLK internally and power down the IDT71V3556/3558 to its lowest power consumption level. Data retention is guaranteed in Sleep Mode. This pin has an internal pulldown.
V_{DD}	Power Supply	N/A	N/A	3.3V core power supply.
V_{DDQ}	Power Supply	N/A	N/A	3.3V I/O Supply.
V_{SS}	Ground	N/A	N/A	Ground.

5281 tbl 02

NOTE:

1. All synchronous inputs must meet specified setup and hold times with respect to CLK.

Pin Configuration - 128K x 36, PKG100(3)

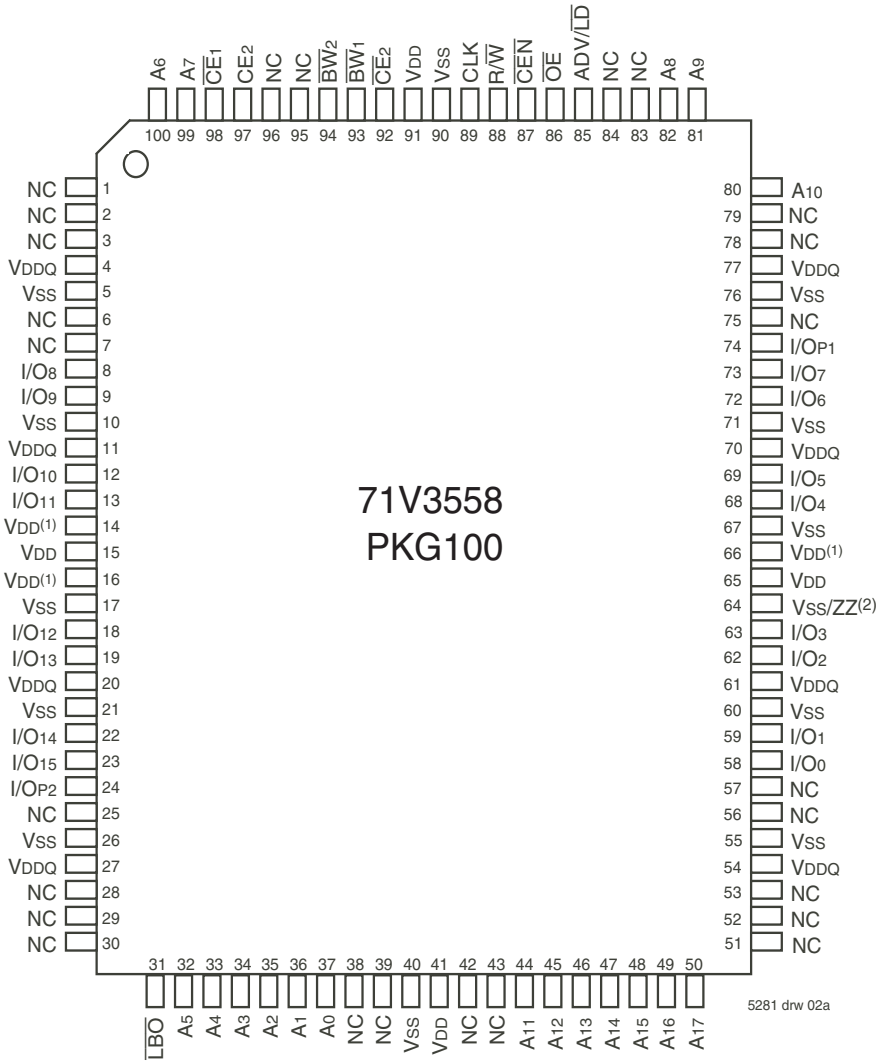


Top View
100 TQFP

NOTES:

1. Pins 14, 16 and 66 do not have to be connected directly to V_{DD} as long as the input voltage is ≥ V_{IH}.
2. Pin 64 does not have to be connected directly to V_{SS} as long as the input voltage is ≤ V_{IL}; on the latest die revision this pin supports ZZ (sleep mode).
3. This text does not indicate orientation of actual part-marking.

Pin Configuration - 256K x 18, PKG100(3)



Top View
100 TQFP

NOTES:

1. Pins 14, 16 and 66 do not have to be connected directly to V_{DD} as long as the input voltage is $\geq V_{IH}$.
2. Pin 64 does not have to be connected directly to V_{SS} as long as the input voltage is $\leq V_{IL}$; on the latest die revision this pin supports ZZ (sleep mode).
3. This text does not indicate orientation of actual part-marking.

Pin Configuration - 128K x 36, BG119, BGG119(5)

	1	2	3	4	5	6	7
A	VDDQ	A6	A4	NC	A8	A16	VDDQ
B	NC	CE2	A3	ADV/LD	A9	CE2	NC
C	NC	A7	A2	VDD	A12	A15	NC
D	I/O16	I/OP3	VSS	NC	VSS	I/OP2	I/O15
E	I/O17	I/O18	VSS	CE1	VSS	I/O13	I/O14
F	VDDQ	I/O19	VSS	OE	VSS	I/O12	VDDQ
G	I/O20	I/O21	BW3	NC	BW2	I/O11	I/O10
H	I/O22	I/O23	VSS	R/W	VSS	I/O9	I/O8
J	VDDQ	VDD	VDD(1)	VDD	VDD(1)	VDD	VDDQ
K	I/O24	I/O26	VSS	CLK	VSS	I/O6	I/O7
L	I/O25	I/O27	BW4	NC	BW1	I/O4	I/O5
M	VDDQ	I/O28	VSS	CEN	VSS	I/O3	VDDQ
N	I/O29	I/O30	VSS	A1	VSS	I/O2	I/O1
P	I/O31	I/OP4	VSS	A0	VSS	I/OP1	I/O0
R	NC	A5	LBO	VDD	VDD(1)	A13	NC
T	NC	NC	A10	A11	A14	NC	NC/ZZ(4)
U	VDDQ	NC/TMS(2)	NC/TDI(2)	NC/TCK(2)	NC/TDO(2)	NC/TRST(2,3)	VDDQ

5281 drw 13A

Top View

Pin Configuration - 256K x 18, BG119, BGG119(5)

	1	2	3	4	5	6	7
A	VDDQ	A6	A4	NC	A8	A16	VDDQ
B	NC	CE2	A3	ADV/LD	A9	CE2	NC
C	NC	A7	A2	VDD	A13	A17	NC
D	I/O8	NC	VSS	NC	VSS	I/OP1	NC
E	NC	I/O9	VSS	CE1	VSS	NC	I/O7
F	VDDQ	NC	VSS	OE	VSS	I/O6	VDDQ
G	NC	I/O10	BW2	NC	VSS	NC	I/O5
H	I/O11	NC	VSS	R/W	VSS	I/O4	NC
J	VDDQ	VDD	VDD(1)	VDD	VDD(1)	VDD	VDDQ
K	NC	I/O12	VSS	CLK	VSS	NC	I/O3
L	I/O13	NC	VSS	NC	BW1	I/O2	NC
M	VDDQ	I/O14	VSS	CEN	VSS	NC	VDDQ
N	I/O15	NC	VSS	A1	VSS	I/O1	NC
P	NC	I/OP2	VSS	A0	VSS	NC	I/O0
R	NC	A5	LBO	VDD	VDD(1)	A12	NC
T	NC	A10	A15	NC	A14	A11	NC/ZZ(4)
U	VDDQ	NC/TMS(2)	NC/TDI(2)	NC/TCK(2)	NC/TDO(2)	NC/TRST(2,3)	VDDQ

5281drw 13B

Top View

NOTES:
1. J3, J5, and R5 do not have to be directly connected to V_{DD} as long as the input voltage is $\geq V_{IH}$.
2. These pins are NC for the "S" version or the JTAG signal listed for the "SA" version.
3. $\overline{TRST}$ is offered as an optional JTAG reset if required in the application. If not needed, can be left floating and will internally be pulled to V_{DD}.
4. Pin T7 does not have to be connected directly to V_{SS} as long as the input voltage is $\leq V_{IL}$; on the latest die revision this pin supports ZZ (sleep mode).
5. This text does not indicate the orientation of actual part-marking.

Pin Configuration - 128K x 36, BQ165, BQG165(5)

	1	2	3	4	5	6	7	8	9	10	11
A	NC	A7	$\overline{CE_1}$	$\overline{BW_3}$	$\overline{BW_2}$	$\overline{CE_2}$	$\overline{CEN}$	ADV/$\overline{LD}$	NC	A8	NC
B	NC	A6	CE2	$\overline{BW_4}$	$\overline{BW_1}$	CLK	R/$\overline{W}$	$\overline{OE}$	NC	A9	NC
C	I/OP3	NC	VDDQ	VSS	VSS	VSS	VSS	VSS	VDDQ	NC	I/OP2
D	I/O17	I/O16	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	I/O15	I/O14
E	I/O19	I/O18	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	I/O13	I/O12
F	I/O21	I/O20	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	I/O11	I/O10
G	I/O23	I/O22	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	I/O9	I/O8
H	VDD(1)	VDD(1)	NC	VDD	VSS	VSS	VSS	VDD	NC	NC	NC/ZZ(4)
J	I/O25	I/O24	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	I/O7	I/O6
K	I/O27	I/O26	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	I/O5	I/O4
L	I/O29	I/O28	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	I/O3	I/O2
M	I/O31	I/O30	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	I/O1	I/O0
N	I/OP4	NC	VDDQ	VSS	NC/$\overline{TRST}$(2,3)	NC	VDD(1)	VSS	VDDQ	NC	I/OP1
P	NC	NC	A5	A2	NC/TDI(2)	A1	NC/TDO(2)	A10	A13	A14	NC
R	$\overline{LBO}$	NC	A4	A3	NC/TMS(2)	A0	NC/TCK(2)	A11	A12	A15	A16

5281 tbl 25

Pin Configuration - 256K x 18, BQ165, BQG165(5)

	1	2	3	4	5	6	7	8	9	10	11
A	NC	A7	$\overline{CE_1}$	$\overline{BW_2}$	NC	$\overline{CE_2}$	$\overline{CEN}$	ADV/$\overline{LD}$	NC	A8	A10
B	NC	A6	CE2	NC	$\overline{BW_1}$	CLK	R/$\overline{W}$	$\overline{OE}$	NC	A9	NC
C	NC	NC	VDDQ	VSS	VSS	VSS	VSS	VSS	VDDQ	NC	I/OP1
D	NC	I/O8	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	NC	I/O7
E	NC	I/O9	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	NC	I/O6
F	NC	I/O10	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	NC	I/O5
G	NC	I/O11	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	NC	I/O4
H	VDD(1)	VDD(1)	NC	VDD	VSS	VSS	VSS	VDD	NC	NC	NC/ZZ(4)
J	I/O12	NC	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	I/O3	NC
K	I/O13	NC	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	I/O2	NC
L	I/O14	NC	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	I/O1	NC
M	I/O15	NC	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	I/O0	NC
N	I/OP2	NC	VDDQ	VSS	NC/$\overline{TRST}$(2,3)	NC	VDD(1)	VSS	VDDQ	NC	NC
P	NC	NC	A5	A2	NC/TDI(2)	A1	NC/TDO(2)	A11	A14	A15	NC
R	$\overline{LBO}$	NC	A4	A3	NC/TMS(2)	A0	NC/TCK(2)	A12	A13	A16	A17

5281 tbl 25a

NOTES:
1. H1, H2, and N7 do not have to be directly connected to VDD as long as the input voltage is ≥ VIH.
2. These pins are NC for the "S" version or the JTAG signal listed for the "SA" version.
3. $\overline{TRST}$ is offered as an optional JTAG reset if required in the application. If not needed, can be left floating and will internally be pulled to VDD.
4. Pin H11 does not have to be connected directly to VSS as long as the input voltage is ≤ VIL; on the latest die revision this pin supports ZZ (sleep mode).
5. This text does not indicate the orientation of the actual part-marking.

Absolute Maximum Ratings (1)

Symbol	Rating	Commercial & Industrial Values	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	-0.5 to +4.6	V
V_{TERM}(3,6)	Terminal Voltage with Respect to GND	-0.5 to V_{DD}	V
V_{TERM}(4,6)	Terminal Voltage with Respect to GND	-0.5 to V_{DD} +0.5	V
V_{TERM}(5,6)	Terminal Voltage with Respect to GND	-0.5 to V_{DDQ} +0.5	V
T_A(7)	**Commercial** Operating Temperature	-0 to +70	°C
	Industrial Operating Temperature	-40 to +85	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	°C
T_{STG}	Storage Temperature	-55 to +125	°C
P_T	Power Dissipation	2.0	W
I_{OUT}	DC Output Current	50	mA

5281 tbl 06

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{DD} terminals only.
3. V_{DDQ} terminals only.
4. Input terminals only.
5. I/O terminals only.
6. This is a steady-state DC parameter that applies after the power supply has reached its nominal operating value. Power sequencing is not necessary; however, the voltage on any input or I/O pin cannot exceed V_{DDQ} during power supply ramp up.
7. T_A is the "instant on" case temperature.

Recommended Operating Temperature and Supply Voltage

Grade	Temperature(1)	V_{SS}	V_{DD}	V_{DDQ}
Commercial	0°C to +70°C	0V	3.3V±5%	3.3V±5%
Industrial	-40°C to +85°C	0V	3.3V±5%	3.3V±5%

5281 tbl 05

NOTES:
1. T_A is the "instant on" case temperature.

Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{DD}	Core Supply Voltage	3.135	3.3	3.465	V
V_{DDQ}	I/O Supply Voltage	3.135	3.3	3.465	V
V_{SS}	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage - Inputs	2.0	—	V_{DD} +0.3	V
V_{IH}	Input High Voltage - I/O	2.0	—	V_{DDQ} +0.3(2)	V
V_{IL}	Input Low Voltage	-0.3(1)	—	0.8	V

5281 tbl 04

NOTES:
1. V_{IL} (min.) = –1.0V for pulse width less than t_{CYC}/2, once per cycle.
2. V_{IH} (max.) = +6.0V for pulse width less than t_{CYC}/2, once per cycle.

100 Pin TQFP Capacitance(1)
(T_A = +25° C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 3dV	5	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 3dV	7	pF

5281 tbl 07

119 BGA Capacitance(1)
(T_A = +25° C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 3dV	7	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 3dV	7	pF

5281 tbl 07a

165 fBGA Capacitance(1)
(T_A = +25° C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 3dV	TBD	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 3dV	TBD	pF

5281 tbl 07b

NOTE:
1. This parameter is guaranteed by device characterization, but not production tested.

Synchronous Truth Table (1)

$\overline{CEN}$	R/$\overline{W}$	Chip[5] Enable	ADV/$\overline{LD}$	$\overline{BW}$x	ADDRESS USED	PREVIOUS CYCLE	CURRENT CYCLE	I/O (2 cycles later)
L	L	Select	L	Valid	External	X	LOAD WRITE	D[7]
L	H	Select	L	X	External	X	LOAD READ	Q[7]
L	X	X	H	Valid	Internal	LOAD WRITE / BURST WRITE	BURST WRITE (Advance burst counter)[2]	D[7]
L	X	X	H	X	Internal	LOAD READ / BURST READ	BURST READ (Advance burst counter)[2]	Q[7]
L	X	Deselect	L	X	X	X	DESELECT or STOP[3]	HiZ
L	X	X	H	X	X	DESELECT / NOOP	NOOP	HiZ
H	X	X	X	X	X	X	SUSPEND[4]	Previous Value

5281 tbl 08

NOTES:
1. L = V_{IL}, H = V_{IH}, X = Don't Care.
2. When ADV/$\overline{LD}$ signal is sampled high, the internal burst counter is incremented. The R/$\overline{W}$ signal is ignored when the counter is advanced. Therefore the nature of the burst cycle (Read or Write) is determined by the status of the R/$\overline{W}$ signal when the first address is loaded at the beginning of the burst cycle.
3. Deselect cycle is initiated when either ($\overline{CE}_1$, or $\overline{CE}_2$ is sampled high or CE_2 is sampled low) and ADV/$\overline{LD}$ is sampled low at rising edge of clock. The data bus will tri-state two cycles after deselect is initiated.
4. When $\overline{CEN}$ is sampled high at the rising edge of clock, that clock edge is blocked from propagating through the part. The state of all the internal registers and the I/Os remains unchanged.
5. To select the chip requires $\overline{CE}_1$ = L, $\overline{CE}_2$ = L, CE_2 = H on these chip enables. Chip is deselected if any one of the chip enables is false.
6. Device Outputs are ensured to be in High-Z after the first rising edge of clock upon power-up.
7. Q - Data read from the device, D - data written to the device.

Partial Truth Table for Writes (1)

OPERATION	R/$\overline{W}$	$\overline{BW}_1$	$\overline{BW}_2$	$\overline{BW}_3$[3]	$\overline{BW}_4$[3]
READ	H	X	X	X	X
WRITE ALL BYTES	L	L	L	L	L
WRITE BYTE 1 (I/O[0:7], I/O_{P1})[2]	L	L	H	H	H
WRITE BYTE 2 (I/O[8:15], I/O_{P2})[2]	L	H	L	H	H
WRITE BYTE 3 (I/O[16:23], I/O_{P3})[2,3]	L	H	H	L	H
WRITE BYTE 4 (I/O[24:31], I/O_{P4})[2,3]	L	H	H	H	L
NO WRITE	L	H	H	H	H

5281 tbl 09

NOTES:
1. L = V_{IL}, H = V_{IH}, X = Don't Care.
2. Multiple bytes may be selected during the same cycle.
3. N/A for X18 configuration.

Interleaved Burst Sequence Table ($\overline{LBO}$=VDD)

	Sequence 1		Sequence 2		Sequence 3		Sequence 4	
	A1	A0	A1	A0	A1	A0	A1	A0
First Address	0	0	0	1	1	0	1	1
Second Address	0	1	0	0	1	1	1	0
Third Address	1	0	1	1	0	0	0	1
Fourth Address(1)	1	1	1	0	0	1	0	0

5281 tbl 10

NOTE:
1. Upon completion of the Burst sequence the counter wraps around to its initial state and continues counting.

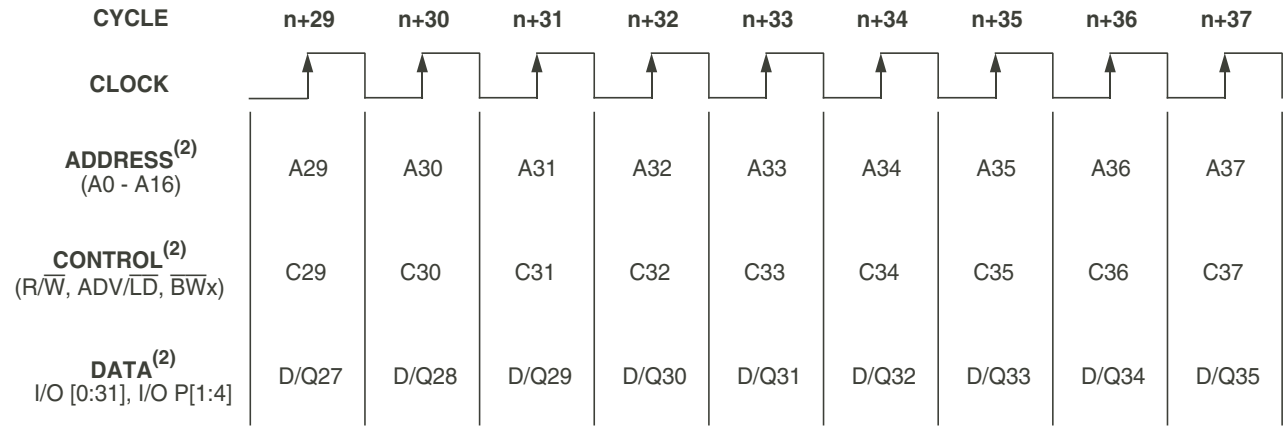
Linear Burst Sequence Table ($\overline{LBO}$=Vss)

	Sequence 1		Sequence 2		Sequence 3		Sequence 4	
	A1	A0	A1	A0	A1	A0	A1	A0
First Address	0	0	0	1	1	0	1	1
Second Address	0	1	1	0	1	1	0	0
Third Address	1	0	1	1	0	0	0	1
Fourth Address(1)	1	1	0	0	0	1	1	0

5281 tbl 11

NOTE:
1. Upon completion of the Burst sequence the counter wraps around to its initial state and continues counting.

Functional Timing Diagram (1)



5281 drw 03

NOTES:
1. This assumes $\overline{CEN}$, $\overline{CE}_1$, CE_2, $\overline{CE}_2$ are all true.
2. All Address, Control and Data_In are only required to meet set-up and hold time with respect to the rising edge of clock. Data_Out is valid after a clock-to-data delay from the rising edge of clock.

Device Operation - Showing Mixed Load, Burst, Deselect and NOOP Cycles (2)

Cycle	Address	R/$\overline{W}$	ADV/$\overline{LD}$	$\overline{CE}$(1)	$\overline{CEN}$	$\overline{BW}$x	$\overline{OE}$	I/O	Comments
n	A_0	H	L	L	L	X	X	X	Load read
n+1	X	X	H	X	L	X	X	X	Burst read
n+2	A_1	H	L	L	L	X	L	Q_0	Load read
n+3	X	X	L	H	L	X	L	Q_{0+1}	Deselect or STOP
n+4	X	X	H	X	L	X	L	Q_1	NOOP
n+5	A_2	H	L	L	L	X	X	Z	Load read
n+6	X	X	H	X	L	X	X	Z	Burst read
n+7	X	X	L	H	L	X	L	Q_2	Deselect or STOP
n+8	A_3	L	L	L	L	L	L	Q_{2+1}	Load write
n+9	X	X	H	X	L	L	X	Z	Burst write
n+10	A_4	L	L	L	L	L	X	D_3	Load write
n+11	X	X	L	H	L	X	X	D_{3+1}	Deselect or STOP
n+12	X	X	H	X	L	X	X	D_4	NOOP
n+13	A_5	L	L	L	L	L	X	Z	Load write
n+14	A_6	H	L	L	L	X	X	Z	Load read
n+15	A_7	L	L	L	L	L	X	D_5	Load write
n+16	X	X	H	X	L	L	L	Q_6	Burst write
n+17	A_8	H	L	L	L	X	X	D_7	Load read
n+18	X	X	H	X	L	X	X	D_{7+1}	Burst read
n+19	A_9	L	L	L	L	L	L	Q_8	Load write

5281 tbl 12

NOTES:
1. $\overline{CE}$ = L is defined as $\overline{CE}_1$ = L, $\overline{CE}_2$ = L and CE_2 = H. $\overline{CE}$ = H is defined as $\overline{CE}_1$ = H, $\overline{CE}_2$ = H or CE_2 = L.
2. H = High; L = Low; X = Don't Care; Z = High Impedance.

Read Operation (1)

Cycle	Address	R/$\overline{W}$	ADV/$\overline{LD}$	$\overline{CE}$(2)	$\overline{CEN}$	$\overline{BW}$x	$\overline{OE}$	I/O	Comments
n	A_0	H	L	L	L	X	X	X	Address and Control meet setup
n+1	X	X	X	X	L	X	X	X	Clock Setup Valid
n+2	X	X	X	X	X	X	L	Q_0	Contents of Address A_0 Read Out

5281 tbl 13

NOTES:
1. H = High; L = Low; X = Don't Care; Z = High Impedance.
2. $\overline{CE}$ = L is defined as $\overline{CE}_1$ = L, $\overline{CE}_2$ = L and CE_2 = H. $\overline{CE}$ = H is defined as $\overline{CE}_1$ = H, $\overline{CE}_2$ = H or CE_2 = L.

Burst Read Operation (1)

Cycle	Address	R/$\overline{W}$	ADV/$\overline{LD}$	$\overline{CE}$(2)	$\overline{CEN}$	$\overline{BW}$x	$\overline{OE}$	I/O	Comments
n	A_0	H	L	L	L	X	X	X	Address and Control meet setup
n+1	X	X	H	X	L	X	X	X	Clock Setup Valid, Advance Counter
n+2	X	X	H	X	L	X	L	Q_0	Address A_0 Read Out, Inc. Count
n+3	X	X	H	X	L	X	L	Q_{0+1}	Address A_{0+1} Read Out, Inc. Count
n+4	X	X	H	X	L	X	L	Q_{0+2}	Address A_{0+2} Read Out, Inc. Count
n+5	A_1	H	L	L	L	X	L	Q_{0+3}	Address A_{0+3} Read Out, Load A_1
n+6	X	X	H	X	L	X	L	Q_0	Address A_0 Read Out, Inc. Count
n+7	X	X	H	X	L	X	L	Q_1	Address A_1 Read Out, Inc. Count
n+8	A_2	H	L	L	L	X	L	Q_{1+1}	Address A_{1+1} Read Out, Load A_2

5281 tbl 14

NOTES:
1. H = High; L = Low; X = Don't Care; Z = High Impedance..
2. $\overline{CE}$ = L is defined as $\overline{CE}_1$ = L, $\overline{CE}_2$ = L and CE_2 = H. $\overline{CE}$ = H is defined as $\overline{CE}_1$ = H, $\overline{CE}_2$ = H or CE_2 = L.

Write Operation (1)

Cycle	Address	R/$\overline{W}$	ADV/$\overline{LD}$	$\overline{CE}$(2)	$\overline{CEN}$	$\overline{BW}$x	$\overline{OE}$	I/O	Comments
n	A_0	L	L	L	L	L	X	X	Address and Control meet setup
n+1	X	X	X	X	L	X	X	X	Clock Setup Valid
n+2	X	X	X	X	L	X	X	D_0	Write to Address A_0

5281 tbl 15

NOTES:
1. H = High; L = Low; X = Don't Care; Z = High Impedance.
2. $\overline{CE}$ = L is defined as $\overline{CE}_1$ = L, $\overline{CE}_2$ = L and CE_2 = H. $\overline{CE}$ = H is defined as $\overline{CE}_1$ = H, $\overline{CE}_2$ = H or CE_2 = L.

Burst Write Operation (1)

Cycle	Address	R/$\overline{W}$	ADV/$\overline{LD}$	$\overline{CE}$(2)	$\overline{CEN}$	$\overline{BW}$x	$\overline{OE}$	I/O	Comments
n	A_0	L	L	L	L	L	X	X	Address and Control meet setup
n+1	X	X	H	X	L	L	X	X	Clock Setup Valid, Inc. Count
n+2	X	X	H	X	L	L	X	D_0	Address A_0 Write, Inc. Count
n+3	X	X	H	X	L	L	X	D_{0+1}	Address A_{0+1} Write, Inc. Count
n+4	X	X	H	X	L	L	X	D_{0+2}	Address A_{0+2} Write, Inc. Count
n+5	A1	L	L	L	L	L	X	D_{0+3}	Address A_{0+3} Write, Load A_1
n+6	X	X	H	X	L	L	X	D_0	Address A_0 Write, Inc. Count
n+7	X	X	H	X	L	L	X	D_1	Address A_1 Write, Inc. Count
n+8	A_2	L	L	L	L	L	X	D_{1+1}	Address A_{1+1} Write, Load A_2

5281 tbl 16

NOTES:
1. H = High; L = Low; X = Don't Care; ? = Don't Know; Z = High Impedance.
2. $\overline{CE}$ = L is defined as $\overline{CE}_1$ = L, $\overline{CE}_2$ = L and CE_2 = H. $\overline{CE}$ = H is defined as $\overline{CE}_1$ = H, $\overline{CE}_2$ = H or CE_2 = L.

Read Operation with Clock Enable Used (1)

Cycle	Address	R/$\overline{W}$	ADV/$\overline{LD}$	$\overline{CE}$(2)	$\overline{CEN}$	$\overline{BW}$x	$\overline{OE}$	I/O	Comments
n	A_0	H	L	L	L	X	X	X	Address and Control meet setup
n+1	X	X	X	X	H	X	X	X	Clock n+1 Ignored
n+2	A_1	H	L	L	L	X	X	X	Clock Valid
n+3	X	X	X	X	H	X	L	Q_0	Clock Ignored. Data Q_0 is on the bus.
n+4	X	X	X	X	H	X	L	Q_0	Clock Ignored. Data Q_0 is on the bus.
n+5	A_2	H	L	L	L	X	L	Q_0	Address A_0 Read out (bus trans.)
n+6	A_3	H	L	L	L	X	L	Q_1	Address A_1 Read out (bus trans.)
n+7	A_4	H	L	L	L	X	L	Q_2	Address A_2 Read out (bus trans.)

5281 tbl 17

NOTES:
1. H = High; L = Low; X = Don't Care; Z = High Impedance.
2. $\overline{CE}$ = L is defined as $\overline{CE}_1$ = L, $\overline{CE}_2$ = L and CE_2 = H. $\overline{CE}$ = H is defined as $\overline{CE}_1$ = H, $\overline{CE}_2$ = H or CE_2 = L.

Write Operation with Clock Enable Used (1)

Cycle	Address	R/$\overline{W}$	ADV/$\overline{LD}$	$\overline{CE}$(2)	$\overline{CEN}$	$\overline{BW}$x	$\overline{OE}$	I/O	Comments
n	A_0	L	L	L	L	L	X	X	Address and Control meet setup.
n+1	X	X	X	X	H	X	X	X	Clock n+1 Ignored.
n+2	A_1	L	L	L	L	L	X	X	Clock Valid.
n+3	X	X	X	X	H	X	X	X	Clock Ignored.
n+4	X	X	X	X	H	X	X	X	Clock Ignored.
n+5	A_2	L	L	L	L	L	X	D_0	Write Data D_0
n+6	A_3	L	L	L	L	L	X	D_1	Write Data D_1
n+7	A_4	L	L	L	L	L	X	D_2	Write Data D_2

5281 tbl 18

NOTES:
1. H = High; L = Low; X = Don't Care; Z = High Impedance.
2. $\overline{CE}$ = L is defined as $\overline{CE}_1$ = L, $\overline{CE}_2$ = L and CE_2 = H. $\overline{CE}$ = H is defined as $\overline{CE}_1$ = H, $\overline{CE}_2$ = H or CE_2 = L.

Read Operation with CHIP Enable Used (1)

Cycle	Address	R/$\overline{W}$	ADV/$\overline{LD}$	$\overline{CE}$(2)	$\overline{CEN}$	$\overline{BW}$x	$\overline{OE}$	I/O(3)	Comments
n	X	X	L	H	L	X	X	?	Deselected.
n+1	X	X	L	H	L	X	X	?	Deselected.
n+2	A_0	H	L	L	L	X	X	Z	Address and Control meet setup
n+3	X	X	L	H	L	X	X	Z	Deselected or STOP.
n+4	A_1	H	L	L	L	X	L	Q_0	Address A_0 Read out. Load A_1.
n+5	X	X	L	H	L	X	X	Z	Deselected or STOP.
n+6	X	X	L	H	L	X	L	Q_1	Address A_1 Read out. Deselected.
n+7	A_2	H	L	L	L	X	X	Z	Address and control meet setup.
n+8	X	X	L	H	L	X	X	Z	Deselected or STOP.
n+9	X	X	L	H	L	X	L	Q_2	Address A_2 Read out. Deselected.

5281 tbl 19

NOTES:
1. H = High; L = Low; X = Don't Care; ? = Don't Know; Z = High Impedance.
2. $\overline{CE}$ = L is defined as $\overline{CE}_1$ = L, $\overline{CE}_2$ = L and CE_2 = H. $\overline{CE}$ = H is defined as $\overline{CE}_1$ = H, $\overline{CE}_2$ = H or CE_2 = L.
3. Device Outputs are ensured to be in High-Z after the first rising edge of clock upon power-up.

Write Operation with Chip Enable Used (1)

Cycle	Address	R/$\overline{W}$	ADV/$\overline{LD}$	$\overline{CE}$(2)	$\overline{CEN}$	$\overline{BW}$x	$\overline{OE}$	I/O(3)	Comments
n	X	X	L	H	L	X	X	?	Deselected.
n+1	X	X	L	H	L	X	X	?	Deselected.
n+2	A_0	L	L	L	L	L	X	Z	Address and Control meet setup
n+3	X	X	L	H	L	X	X	Z	Deselected or STOP.
n+4	A_1	L	L	L	L	L	X	D_0	Address D_0 Write in. Load A_1.
n+5	X	X	L	H	L	X	X	Z	Deselected or STOP.
n+6	X	X	L	H	L	X	X	D_1	Address D_1 Write in. Deselected.
n+7	A_2	L	L	L	L	L	X	Z	Address and control meet setup.
n+8	X	X	L	H	L	X	X	Z	Deselected or STOP.
n+9	X	X	L	H	L	X	X	D_2	Address D_2 Write in. Deselected.

5281 tbl 20

NOTES:
1. H = High; L = Low; X = Don't Care; ? = Don't Know; Z = High Impedance.
2. $\overline{CE}$ = L is defined as $\overline{CE}_1$ = L, $\overline{CE}_2$ = L and CE_2 = H. $\overline{CE}$ = H is defined as $\overline{CE}_1$ = H, $\overline{CE}_2$ = H or CE_2 = L.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range (V_{DD} = 3.3V +/-5%)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
$\|I_{LI}\|$	Input Leakage Current	V_{DD} = Max., V_{IN} = 0V to V_{DD}	—	5	µA
$\|I_{LI}\|$	LBO, JTAG and ZZ Input Leakage Current(1)	V_{DD} = Max., V_{IN} = 0V to V_{DD}	—	30	µA
$\|I_{LO}\|$	Output Leakage Current	V_{OUT} = 0V to V_{DDQ}, Device Deselected	—	5	µA
V_{OL}	Output Low Voltage	I_{OL} = +8mA, V_{DD} = Min.	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -8mA, V_{DD} = Min.	2.4	—	V

5281 tbl 21

NOTE:
1. The $\overline{LBO}$, TMS, TDI, TCK and $\overline{TRST}$ pins will be internally pulled to V_{DD} and ZZ will be internally pulled if they are not actively driven in the application.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range (1) (V_{DD} = 3.3V +/-5%)

Symbol	Parameter	Test Conditions	200MHz(4)	166MHz		133MHz		100MHz		Unit
			Com'l Only	Com'l	Ind	Com'l	Ind	Com'l	Ind	
I_{DD}	Operating Power Supply Current	Device Selected, Outputs Open, ADV/LD = X, V_{DD} = Max., $V_{IN} \geq V_{IH}$ or $\leq V_{IL}$, f = f_{MAX}(2)	400	350	360	300	310	250	255	mA
I_{SB1}	CMOS Standby Power Supply Current	Device Deselected, Outputs Open, V_{DD} = Max., $V_{IN} \geq V_{HD}$ or $\leq V_{LD}$, f = 0(2,3)	40	40	45	40	45	40	45	mA
I_{SB2}	Clock Running Power Supply Current	Device Deselected, Outputs Open, V_{DD} = Max., $V_{IN} \geq V_{HD}$ or < V_{LD}, f = f_{MAX}(2.3)	130	120	130	110	120	100	110	mA
I_{SB3}	Idle Power Supply Current	Device Selected, Outputs Open, CEN $\geq V_{IH}$, V_{DD} = Max., $V_{IN} \geq V_{HD}$ or $\leq V_{LD}$, f = f_{MAX}(2,3)	40	40	45	40	45	40	45	mA

NOTES:
5281 tbl 22
1. All values are maximum guaranteed values.
2. At f = f_{MAX}, inputs are cycling at the maximum frequency of read cycles of 1/t_{CYC}; f=0 means no input lines are changing.
3. For I/Os V_{HD} = V_{DDQ} – 0.2V, V_{LD} = 0.2V. For other inputs V_{HD} = V_{DD} – 0.2V, V_{LD} = 0.2V.
4. Only available in 256K x 18 configuration.

AC Test Loads

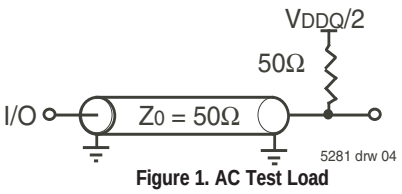


Figure 1. AC Test Load

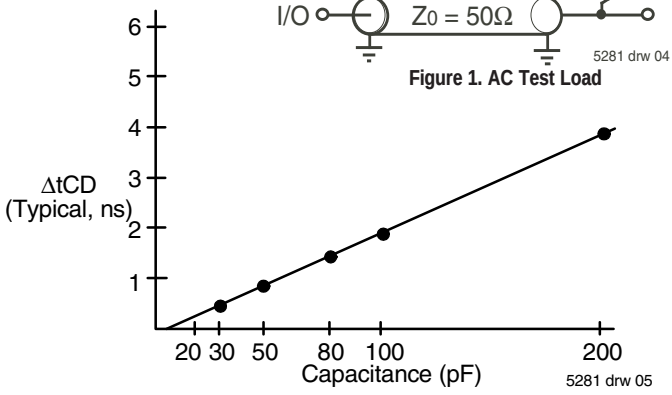


Figure 2. Lumped Capacitive Load, Typical Derating

AC Test Conditions (V_{DDQ} = 3.3V)

Input Pulse Levels	0 to 3V
Input Rise/Fall Times	2ns
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
AC Test Load	See Figure 1

5281 tbl 23

AC Electrical Characteristics

(VDD = 3.3V +/-5%, Commercial and Industrial Temperature Ranges)

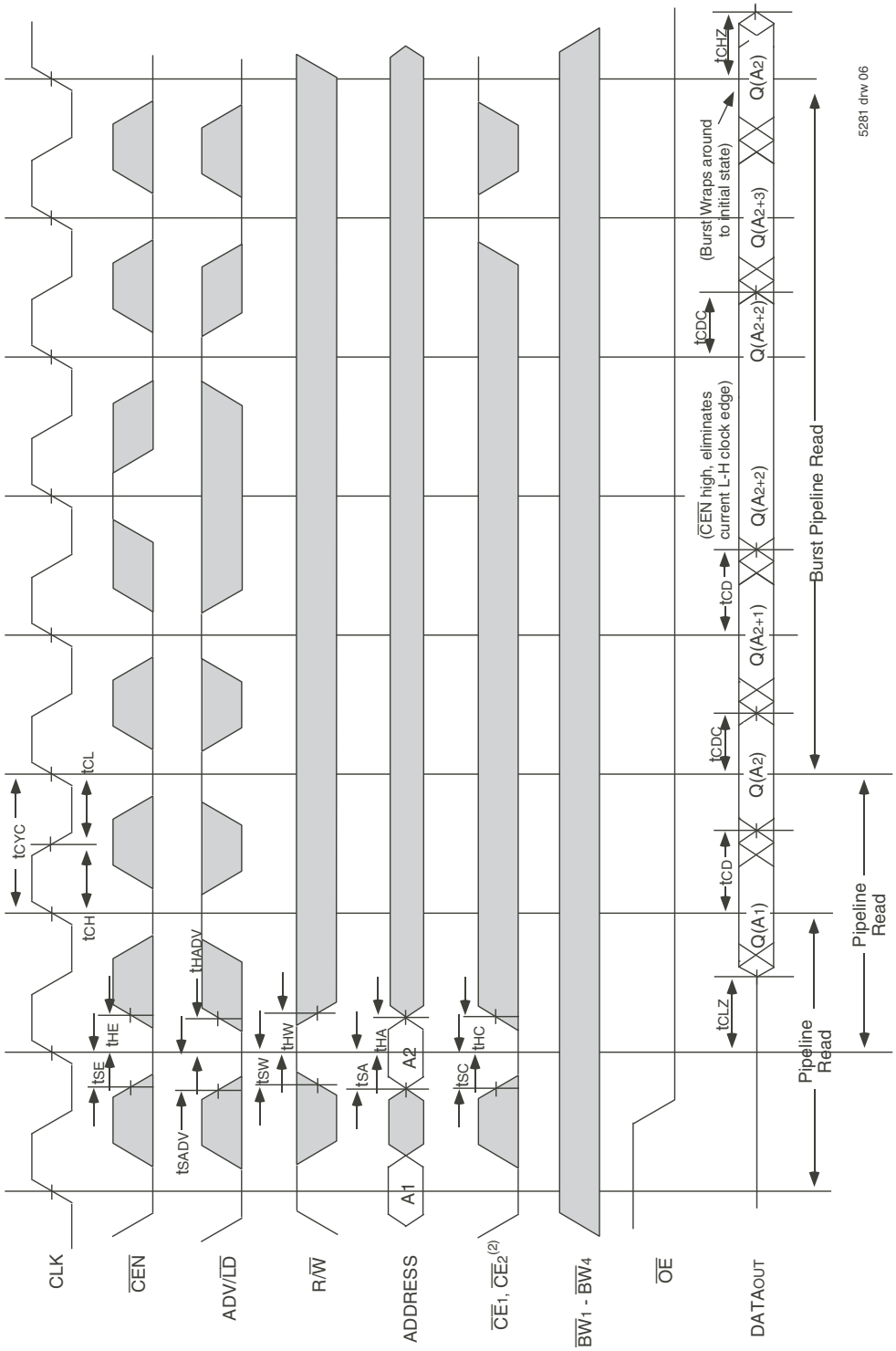
Symbol	Parameter	200MHz[6]		166MHz		133MHz		100MHz		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{CYC}	Clock Cycle Time	5	—	6	—	7.5	—	10	—	ns
t_F[1]	Clock Frequence	—	200	—	166	—	133	—	100	MHz
t_{CH}[2]	Clock High Pulse Width	1.8	—	1.8	—	2.2	—	3.2	—	ns
t_{CL}[2]	Clock Low Pulse Width	1.8	—	1.8	—	2.2	—	3.2	—	ns
Output Parameters										
t_{CD}	Clock High to Valid Data	—	3.2	—	3.5	—	4.2	—	5	ns
t_{CDC}	Clock High to Data Change	1	—	1	—	1	—	1	—	ns
t_{CLZ}[3,4,5]	Clock High to Output Active	1	—	1	—	1	—	1	—	ns
t_{CHZ}[3,4,5]	Clock High to Data High-Z	1	3	1	3	1	3	1	3.3	ns
t_{OE}	Output Enable Access Time	—	3.2	—	3.5	—	4.2	—	5	ns
t_{OLZ}[3,4]	Output Enable Low to Data Active	0	—	0	—	0	—	0	—	ns
t_{OHZ}[3,4]	Output Enable High to Data High-Z	—	3.5	—	3.5	—	4.2	—	5	ns
Set Up Times										
t_{SE}	Clock Enable Setup Time	1.5	—	1.5	—	1.7	—	2.0	—	ns
t_{SA}	Address Setup Time	1.5	—	1.5	—	1.7	—	2.0	—	ns
t_{SD}	Data In Setup Time	1.5	—	1.5	—	1.7	—	2.0	—	ns
t_{SW}	Read/Write (R/$\overline{W}$) Setup Time	1.5	—	1.5	—	1.7	—	2.0	—	ns
t_{SADV}	Advance/Load (ADV/$\overline{LD}$) Setup Time	1.5	—	1.5	—	1.7	—	2.0	—	ns
t_{SC}	Chip Enable/Select Setup Time	1.5	—	1.5	—	1.7	—	2.0	—	ns
t_{SB}	Byte Write Enable ($\overline{BW}$x) Setup Time	1.5	—	1.5	—	1.7	—	2.0	—	ns
Hold Times										
t_{HE}	Clock Enable Hold Time	0.5	—	0.5	—	0.5	—	0.5	—	ns
t_{HA}	Address Hold Time	0.5	—	0.5	—	0.5	—	0.5	—	ns
t_{HD}	Data In Hold Time	0.5	—	0.5	—	0.5	—	0.5	—	ns
t_{HW}	Read/Write (R/$\overline{W}$) Hold Time	0.5	—	0.5	—	0.5	—	0.5	—	ns
t_{HADV}	Advance/Load (ADV/$\overline{LD}$) Hold Time	0.5	—	0.5	—	0.5	—	0.5	—	ns
t_{HC}	Chip Enable/Select Hold Time	0.5	—	0.5	—	0.5	—	0.5	—	ns
t_{HB}	Byte Write Enable ($\overline{BW}$x) Hold Time	0.5	—	0.5	—	0.5	—	0.5	—	ns

5281 tbl 24

NOTES:

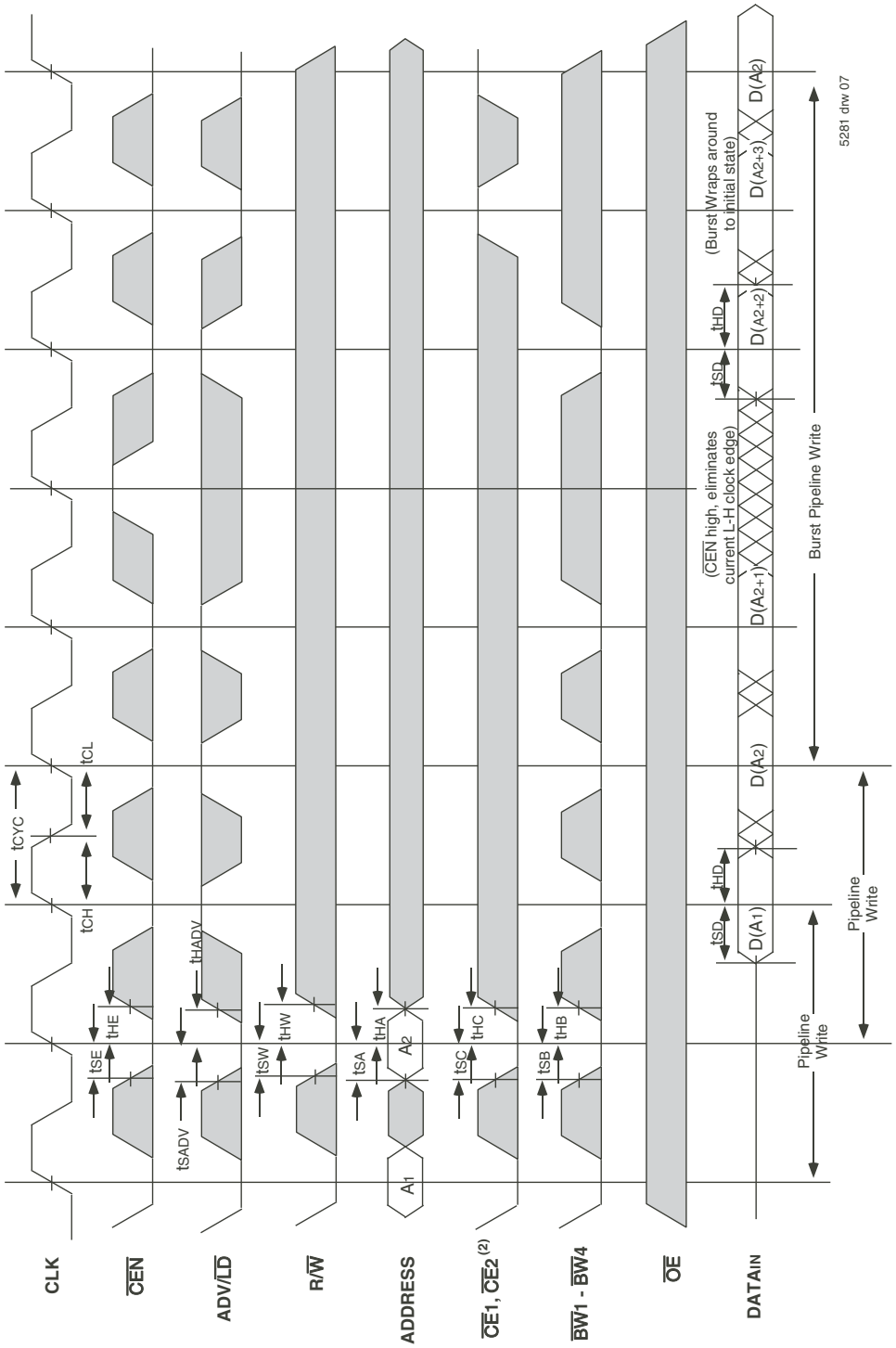
1. $t_F = 1/t_{CYC}$.
2. Measured as HIGH above 0.6VDDQ and LOW below 0.4VDDQ.
3. Transition is measured ±200mV from steady-state.
4. These parameters are guaranteed with the AC load (Figure 1) by device characterization. They are not production tested.
5. To avoid bus contention, the output buffers are designed such that t_{CHZ} (device turn-off) is about 1ns faster than t_{CLZ} (device turn-on) at a given temperature and voltage. The specs as shown do not imply bus contention because t_{CLZ} is a Min. parameter that is worse case at totally different test conditions (0 deg. C, 3.465V) than t_{CHZ}, which is a Max. parameter (worse case at 70 deg. C, 3.135V).
6. Commercial temperature range only. Only available in 256K x 18 configuration.

Timing Waveform of Read Cycle (1,2,3,4)



NOTES:
1. Q (A1) represents the first output from the external address A1. Q (A2) represents the first output from the external address A2; Q (A2+1) represents the next output data in the burst sequence of the base address A2, etc. where address bits A0 and A1 are advancing for the four word burst in the sequence defined by the state of the LBO input.
2. CE2 timing transitions are identical but inverted to the CE1 and CE2 signals. For example, when CE1 and CE2 are LOW on this waveform, CE2 is HIGH.
3. Burst ends when new address and control are loaded into the SRAM by sampling ADV/LD LOW.
4. R/W is don't care when the SRAM is bursting (ADV/LD sampled HIGH). The nature of the burst access (Read or Write) is fixed by the state of the R/W signal when new address and control are loaded into the SRAM.

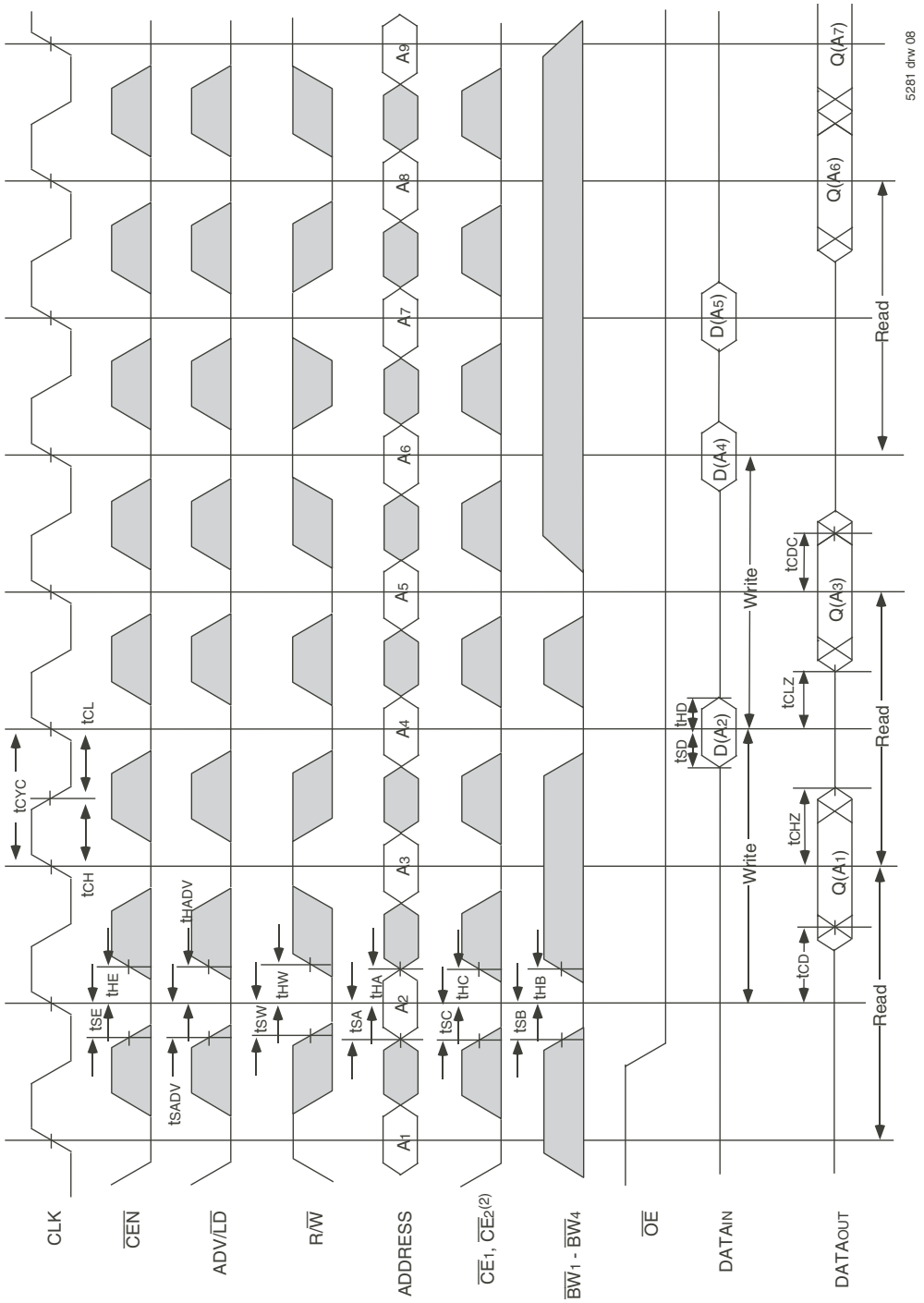
Timing Waveform of Write Cycles (1,2,3,4,5)



NOTES:

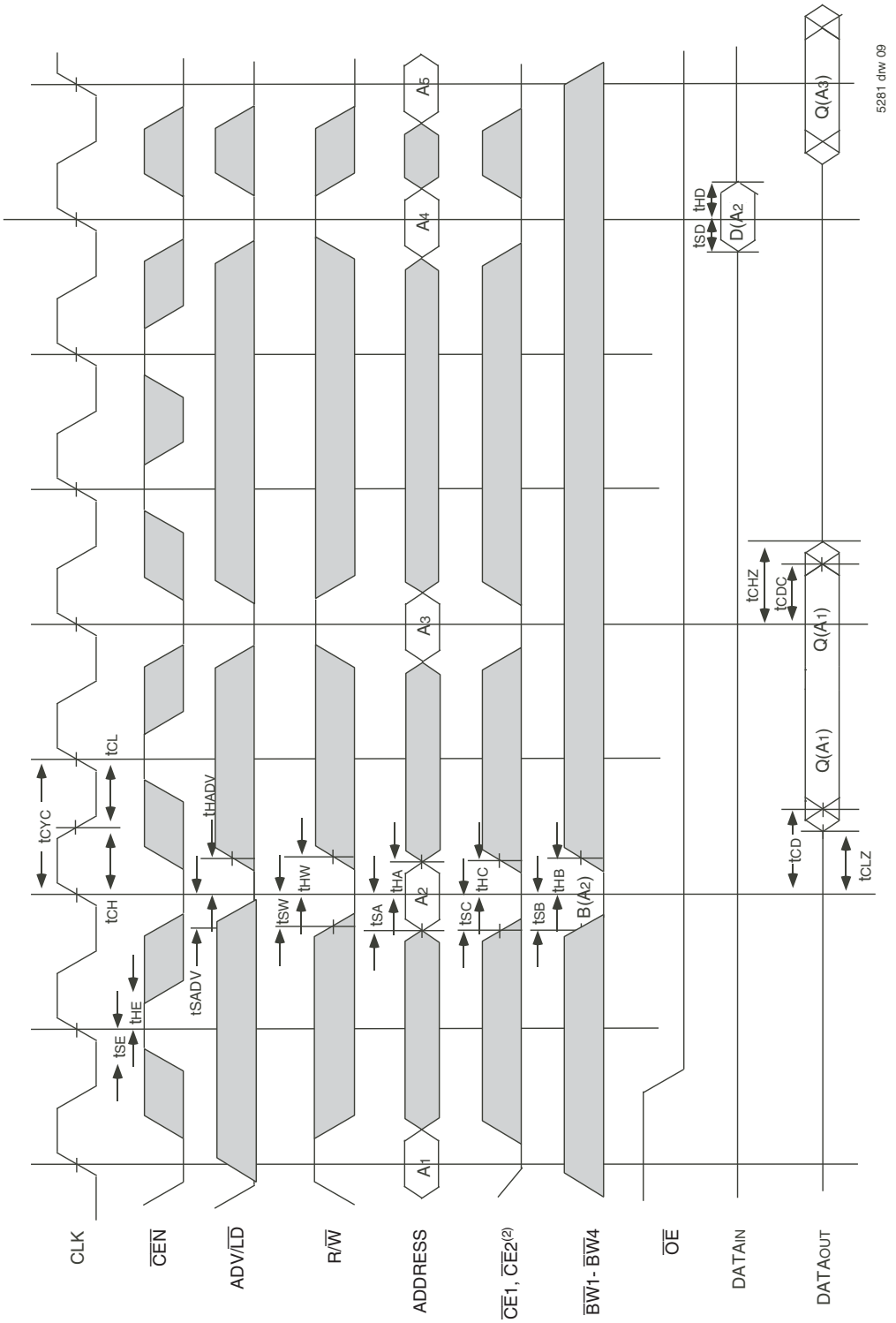
1. D (A_1) represents the first input to the external address A_1. D (A_2) represents the first input to the external address A_2; D (A_{2+1}) represents the next input data in the burst sequence of the base address A_2, etc. where address bits A_0 and A_1 are advancing for the four word burst in the sequence defined by the state of the $\overline{LBO}$ input.
2. CE_2 timing transitions are identical but inverted to the $\overline{CE}_1$ and $\overline{CE}_2$ signals. For example, when $\overline{CE}_1$ and $\overline{CE}_2$ are LOW on this waveform, CE2 is HIGH.
3. Burst ends when new address and control are loaded into the SRAM by sampling ADV/$\overline{LD}$ LOW.
4. R/$\overline{W}$ is don't care when the SRAM is bursting (ADV/$\overline{LD}$ sampled HIGH). The nature of the burst access (Read or Write) is fixed by the state of the R/$\overline{W}$ signal when new address and control are loaded into the SRAM.
5. Individual Byte Write signals ($\overline{BW}x$) must be valid on all write and burst-write cycles. A write cycle is initiated when R/$\overline{W}$ signal is sampled LOW. The byte write information comes in two cycles before the actual data is presented to the SRAM.

Timing Waveform of Combined Read and Write Cycles (1,2,3)



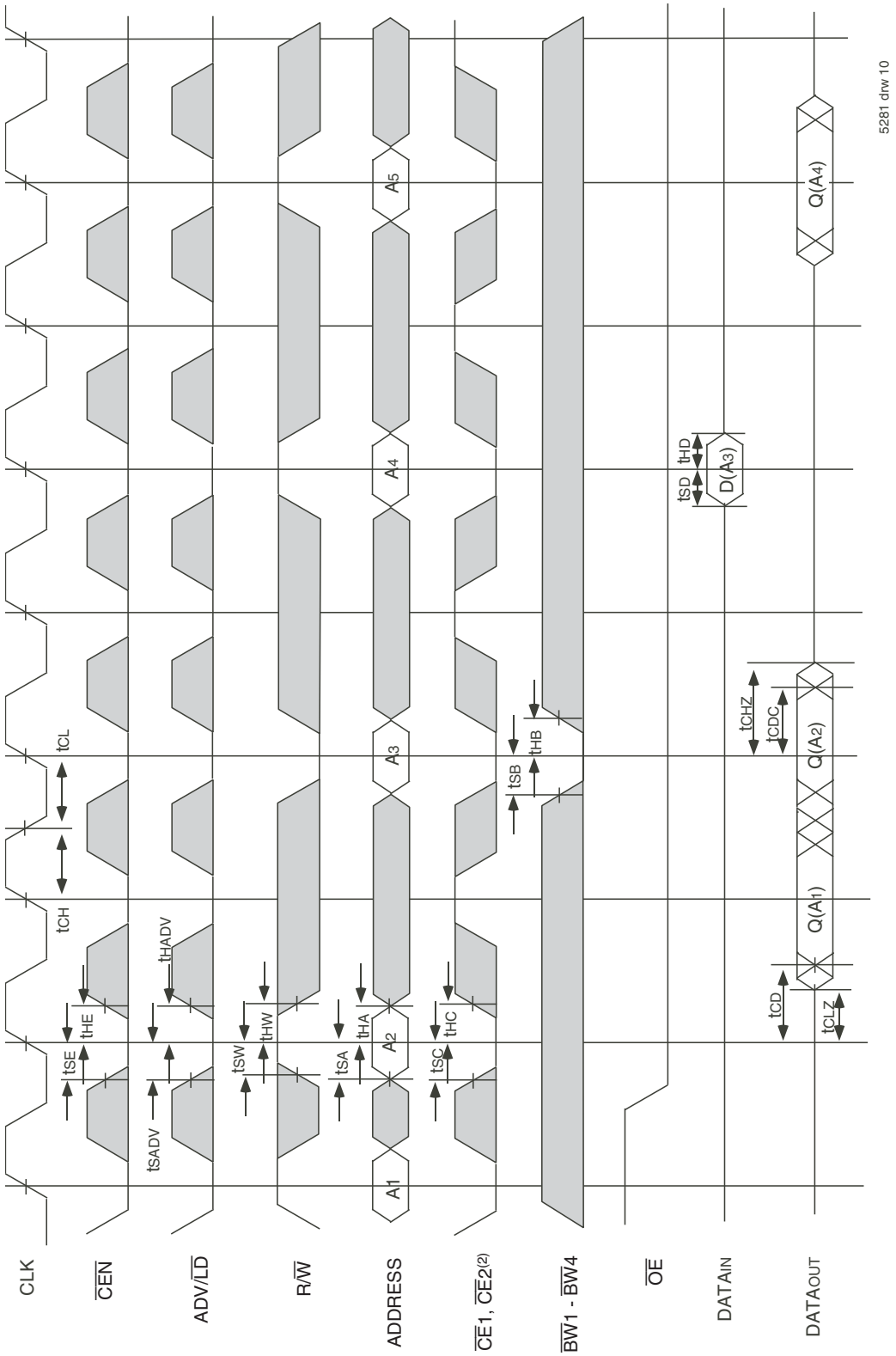
NOTES:
1. Q (A1) represents the first output from the external address A1. D (A2) represents the input data to the SRAM corresponding to address A2.
2. CE2 timing transitions are identical but inverted to the $\overline{CE}_1$ and $\overline{CE}_2$ signals. For example, when $\overline{CE}_1$ and $\overline{CE}_2$ are LOW on this waveform, CE2 is HIGH.
3. Individual Byte Write signals ($\overline{BW}x$) must be valid on all write and burst-write cycles. A write cycle is initiated when R/$\overline{W}$ signal is sampled LOW. The byte write information comes in two cycles before the actual data is presented to the SRAM.

Timing Waveform of $\overline{CEN}$ Operation (1,2,3,4)



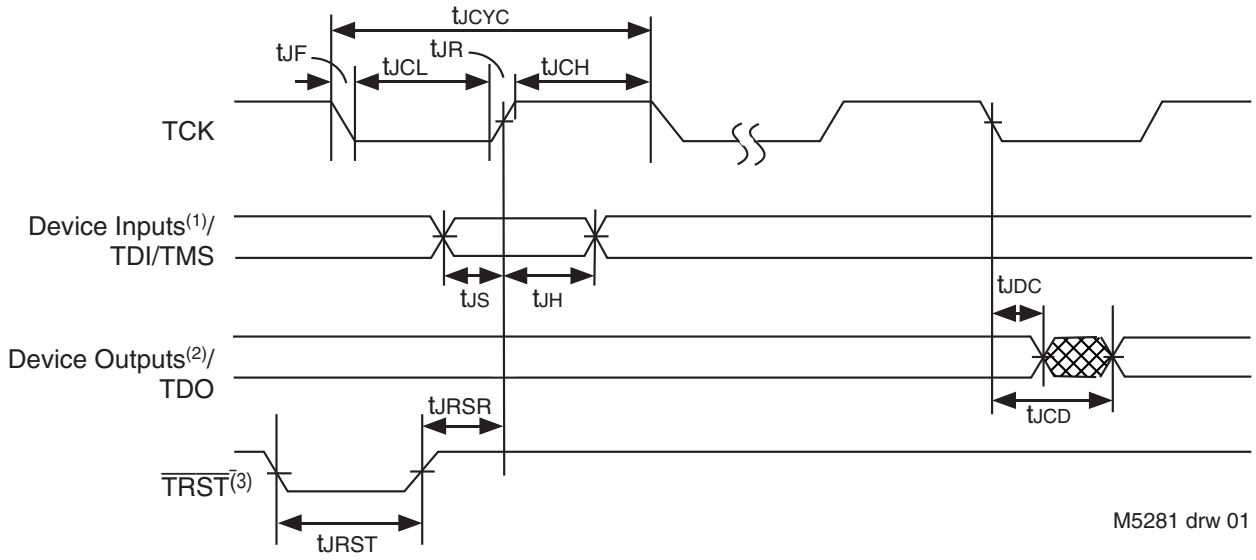
NOTES:
1. Q (A_1) represents the first output from the external address A_1. D (A_2) represents the input data to the SRAM corresponding to address A_2.
2. CE_2 timing transitions are identical but inverted to the $\overline{CE}_1$ and $\overline{CE}_2$ signals. For example, when $\overline{CE}_1$ and $\overline{CE}_2$ are LOW on this waveform, CE_2 is HIGH.
3. $\overline{CEN}$ when sampled high on the rising edge of clock will block that L-H transition of the clock from propagating into the SRAM. The part will behave as if the L-H clock transition did not occur. All internal registers in the SRAM will retain their previous state.
4. Individual Byte Write signals ($\overline{BW}x$) must be valid on all write and burst-write cycles. A write cycle is initiated when R/$\overline{W}$ signal is sampled LOW. The byte write information comes in two cycles before the actual data is presented to the SRAM.

Timing Waveform of $\overline{CS}$ Operation (1,2,3,4)



NOTES:
1. Q (A1) represents the first output from the external address A1. D (A3) represents the input data to the SRAM corresponding to address A3.
2. $\overline{CE}_2$ timing transitions are identical but inverted to the $\overline{CE}_1$ and $\overline{CE}_2$ signals. For example, when $\overline{CE}_1$ and $\overline{CE}_2$ are LOW on this waveform, CE_2 is HIGH.
3. $\overline{CEN}$ when sampled high on the rising edge of clock will block that L-H transition of the clock from propagating into the SRAM. The part will behave as if the L-H clock transition did not occur. All internal registers in the SRAM will retain their previous state.
4. Individual Byte Write signals ($\overline{BW}x$) must be valid on all write and burst-write cycles. A write cycle is initiated when R/$\overline{W}$ signal is sampled LOW. The byte write information comes in two cycles before the actual data is presented to the SRAM.

JTAG Interface Specification (SA Version only)



NOTES:
1. Device inputs = All device inputs except TDI, TMS and $\overline{\text{TRST}}$.
2. Device outputs = All device outputs except TDO.
3. During power up, $\overline{\text{TRST}}$ could be driven low or not be used since the JTAG circuit resets automatically. $\overline{\text{TRST}}$ is an optional JTAG reset.

JTAG AC Electrical Characteristics(1,2,3,4)

Symbol	Parameter	Min.	Max.	Units
t_{JCYC}	JTAG Clock Input Period	100	—	ns
t_{JCH}	JTAG Clock HIGH	40	—	ns
t_{JCL}	JTAG Clock Low	40	—	ns
t_{JR}	JTAG Clock Rise Time	—	5(1)	ns
t_{JF}	JTAG Clock Fall Time	—	5(1)	ns
t_{JRST}	JTAG Reset	50	—	ns
t_{JRSR}	JTAG Reset Recovery	50	—	ns
t_{JCD}	JTAG Data Output	—	20	ns
t_{JDC}	JTAG Data Output Hold	0	—	ns
t_{JS}	JTAG Setup	25	—	ns
t_{JH}	JTAG Hold	25	—	ns

5281 tbl 01

NOTES:
1. Guaranteed by design.
2. AC Test Load (Fig. 1) on external output signals.
3. Refer to AC Test Conditions stated earlier in this document.
4. JTAG operations occur at one speed (10MHz). The base device may run at any speed specified in this datasheet.

Scan Register Sizes

Register Name	Bit Size
Instruction (IR)	4
Bypass (BYR)	1
JTAG Identification (JIDR)	32
Boundary Scan (BSR)	Note (1)

5281 tbl 03

NOTE:
1. The Boundary Scan Descriptive Language (BSDL) file for this device is available by contacting your local IDT sales representative.

JTAG Identification Register Definitions (SA Version only)

Instruction Field	Value	Description
Revision Number (31:28)	0x2	Reserved for version number.
IDT Device ID (27:12)	0x208, 0x20A	Defines IDT part number 71V3556SA and 71V3558SA, respectively.
IDT JEDEC ID (11:1)	0x33	Allows unique identification of device vendor as IDT.
ID Register Indicator Bit (Bit 0)	1	Indicates the presence of an ID register.

I5281 tbl 02

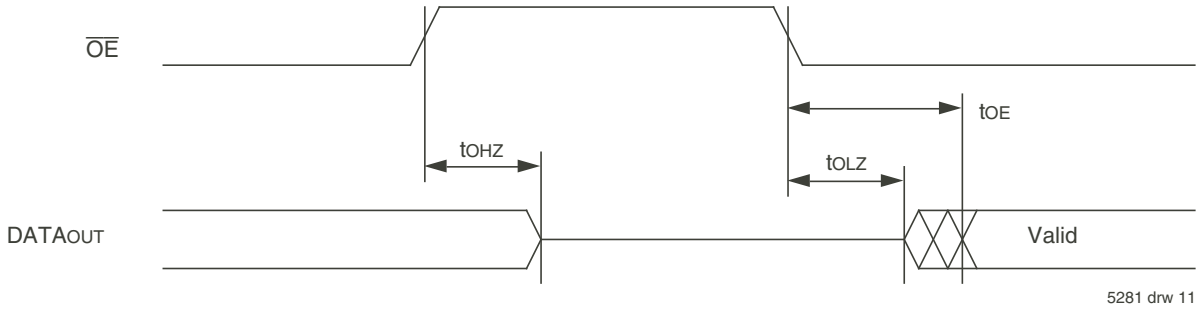
Available JTAG Instructions

Instruction	Description	OPCODE
EXTEST	Forces contents of the boundary scan cells onto the device outputs[1]. Places the boundary scan register (BSR) between TDI and TDO.	0000
SAMPLE/PRELOAD	Places the boundary scan register (BSR) between TDI and TDO. SAMPLE allows data from device inputs[2] and outputs[1] to be captured in the boundary scan cells and shifted serially through TDO. PRELOAD allows data to be input serially into the boundary scan cells via the TDI.	0001
DEVICE_ID	Loads the JTAG ID register (JIDR) with the vendor ID code and places the register between TDI and TDO.	0010
HIGHZ	Places the bypass register (BYR) between TDI and TDO. Forces all device output drivers to a High-Z state.	0011
RESERVED	Several combinations are reserved. Do not use codes other than those identified for EXTEST, SAMPLE/PRELOAD, DEVICE_ID, HIGHZ, CLAMP, VALIDATE and BYPASS instructions.	0100
RESERVED		0101
RESERVED		0110
RESERVED		0111
CLAMP	Uses BYR. Forces contents of the boundary scan cells onto the device outputs. Places the bypass register (BYR) between TDI and TDO.	1000
RESERVED	Same as above.	1001
RESERVED		1010
RESERVED		1011
RESERVED		1100
VALIDATE	Automatically loaded into the instruction register whenever the TAP controller passes through the CAPTURE-IR state. The lower two bits '01' are mandated by the IEEE std. 1149.1 specification.	1101
RESERVED	Same as above.	1110
BYPASS	The BYPASS instruction is used to truncate the boundary scan register as a single bit in length.	1111

I5281 tbl 04

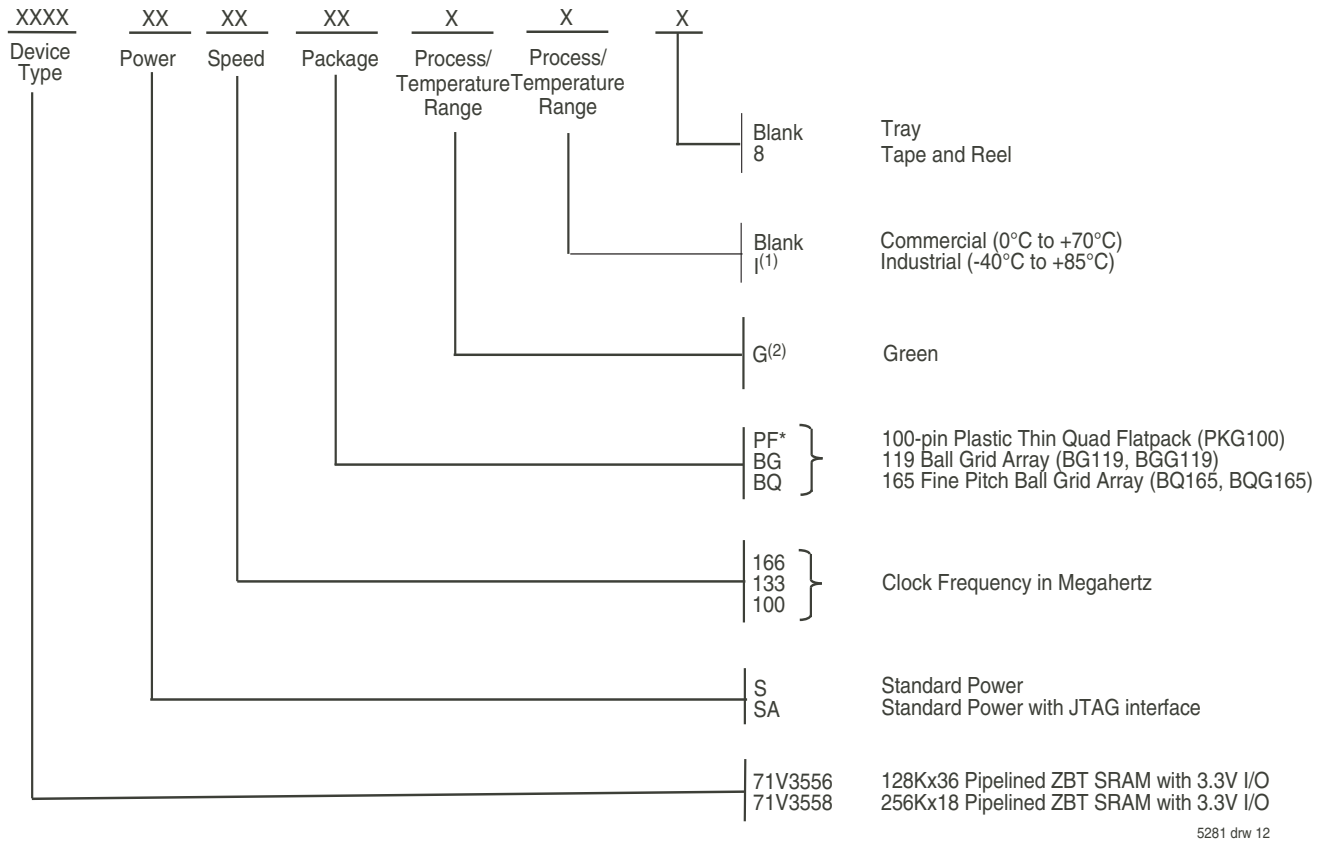
NOTES:
1. Device outputs = All device outputs except TDO.
2. Device inputs = All device inputs except TDI, TMS, and $\overline{\text{TRST}}$.

Timing Waveform of $\overline{OE}$ Operation (1)



NOTE:
1. A read operation is assumed to be in progress.

Ordering Information



* JTAG (SA Version) is not available with 100-pin TQFP package

NOTES:
1. Contact your local sales office for Industrial temp range for other speeds, packages and powers.
2. Green parts available. For specific speeds, packages and powers contact your local sales office.

Orderable Part Information

Speed (MHz)	Orderable Part ID	Pkg. Code	Pkg. Type	Temp. Grade
100	71V3556S100PFG	PKG100	TQFP	C
	71V3556S100PFG8	PKG100	TQFP	C
	71V3556S100PFGI	PKG100	TQFP	I
	71V3556S100PFGI8	PKG100	TQFP	I
133	71V3556S133PFG	PKG100	TQFP	C
	71V3556S133PFG8	PKG100	TQFP	C
	71V3556S133PFGI	PKG100	TQFP	I
	71V3556S133PFGI8	PKG100	TQFP	I
166	71V3556S166PFG	PKG100	TQFP	C
	71V3556S166PFG8	PKG100	TQFP	C
	71V3556S166PFGI	PKG100	TQFP	I
	71V3556S166PFGI8	PKG100	TQFP	I

Speed (MHz)	Orderable Part ID	Pkg. Code	Pkg. Type	Temp. Grade
100	71V3556SA100BG	BG119	PBGA	C
	71V3556SA100BG8	BG119	PBGA	C
	71V3556SA100BGG	BGG119	PBGA	C
	71V3556SA100BGG8	BGG119	PBGA	C
	71V3556SA100BGGI	BGG119	PBGA	I
	71V3556SA100BGGI8	BGG119	PBGA	I
	71V3556SA100BGI	BG119	PBGA	I
	71V3556SA100BGI8	BG119	PBGA	I
	71V3556SA100BQ	BQ165	CABGA	C
	71V3556SA100BQ8	BQ165	CABGA	C
	71V3556SA100BQG	BQG165	CABGA	C
	71V3556SA100BQG8	BQG165	CABGA	C
	71V3556SA100BQGI	BQG165	CABGA	I
	71V3556SA100BQGI8	BQG165	CABGA	I
	71V3556SA100BQI	BQ165	CABGA	I
	71V3556SA100BQI8	BQ165	CABGA	I

Speed (MHz)	Orderable Part ID	Pkg. Code	Pkg. Type	Temp. Grade
133	71V3556SA133BG	BG119	PBGA	C
	71V3556SA133BG8	BG119	PBGA	C
	71V3556SA133BGG	BGG119	PBGA	C
	71V3556SA133BGG8	BGG119	PBGA	C
	71V3556SA133BGGI	BGG119	PBGA	I
	71V3556SA133BGGI8	BGG119	PBGA	I
	71V3556SA133BGI	BG119	PBGA	I
	71V3556SA133BGI8	BG119	PBGA	I
	71V3556SA133BQ	BQ165	CABGA	C
	71V3556SA133BQ8	BQ165	CABGA	C
	71V3556SA133BQG	BQG165	CABGA	C
	71V3556SA133BQG8	BQG165	CABGA	C
	71V3556SA133BQGI	BQG165	CABGA	I
	71V3556SA133BQGI8	BQG165	CABGA	I
	71V3556SA133BQI	BQ165	CABGA	I
	71V3556SA133BQI8	BQ165	CABGA	I
150	71V3556SA150BG	BG119	PBGA	C
	71V3556SA150BG8	BG119	PBGA	C
	71V3556SA150BGG	BGG119	PBGA	C
	71V3556SA150BGG8	BGG119	PBGA	C
	71V3556SA150BGGI	BGG119	PBGA	I
	71V3556SA150BGGI8	BGG119	PBGA	I
	71V3556SA150BQ	BQ165	CABGA	C
	71V3556SA150BQ8	BQ165	CABGA	C
166	71V3556SA166BG	BG119	PBGA	C
	71V3556SA166BG8	BG119	PBGA	C
	71V3556SA166BGG	BGG119	PBGA	C
	71V3556SA166BGG8	BGG119	PBGA	C
	71V3556SA166BGGI	BGG119	PBGA	I
	71V3556SA166BGGI8	BGG119	PBGA	I
	71V3556SA166BGI	BG119	PBGA	I
	71V3556SA166BGI8	BG119	PBGA	I
	71V3556SA166BQ	BQ165	CABGA	C
	71V3556SA166BQ8	BQ165	CABGA	C
	71V3556SA166BQG	BQG165	CABGA	C
	71V3556SA166BQG8	BQG165	CABGA	C
	71V3556SA166BQGI	BQG165	CABGA	I
	71V3556SA166BQGI8	BQG165	CABGA	I

Orderable Part Information (con't)

Speed (MHz)	Orderable Part ID	Pkg. Code	Pkg. Type	Temp. Grade
100	71V3558S100PFG	PKG100	TQFP	C
	71V3558S100PFG8	PKG100	TQFP	C
	71V3558S100PFGI	PKG100	TQFP	I
	71V3558S100PFGI8	PKG100	TQFP	I
133	71V3558S133PFG	PKG100	TQFP	C
	71V3558S133PFG8	PKG100	TQFP	C
	71V3558S133PFGI	PKG100	TQFP	I
	71V3558S133PFGI8	PKG100	TQFP	I
166	71V3558S166PFG	PKG100	TQFP	C
	71V3558S166PFG8	PKG100	TQFP	C
	71V3558S166PFGI	PKG100	TQFP	I
	71V3558S166PFGI8	PKG100	TQFP	I

Speed (MHz)	Orderable Part ID	Pkg. Code	Pkg. Type	Temp. Grade
100	71V3558SA100BQG	BQG165	CABGA	C
	71V3558SA100BQG8	BQG165	CABGA	C
	71V3558SA100BQGI	BQG165	CABGA	I
	71V3558SA100BQGI8	BQG165	CABGA	I
133	71V3558SA133BQG	BQG165	CABGA	C
	71V3558SA133BQG8	BQG165	CABGA	C
	71V3558SA133BQGI	BQG165	CABGA	I
	71V3558SA133BQGI8	BQG165	CABGA	I
166	71V3558SA166BQG	BQG165	CABGA	C
	71V3558SA166BQG8	BQG165	CABGA	C
	71V3558SA166BQGI	BQG165	CABGA	I
	71V3558SA166BQGI8	BQG165	CABGA	I

Datasheet Document History

06/30/99		Updated to new format
08/23/99		Added Smart ZBT functionality
	Pg. 4, 5	Added Note 4 and changed Pins 38, 42, and 43 to DNU
	Pg. 6	Changed U2–U6 to DNU
	Pg. 14	Added Smart ZBT AC Electrical Characteristics
	Pg. 15	Improved t_{CD} and $t_{OE(MAX)}$ at 166MHz
		Revised $t_{CHZ(MIN)}$ for f ≤ 133 MHz
		Revised t_{OHZ} ($_{MAX}$) for f ≤ 133 MHz
		Improved t_{CH}, t_{CL} for f ≤ 166 MHz
		Improved setup times for 100–200 MHz
	Pg. 22	Added BGA package diagrams
	Pg. 24	Added Datasheet Document History
10/04/99	Pg. 14	Revised AC Electrical Characteristics table
	Pg. 15	Revised t_{CHZ} to match t_{CLZ} and t_{CDC} at 133MHz and 100MHz
12/31/99		Removed Smart functionality
		Added Industrial Temperature range offerings at the 100 to 166MHz speed grades.
04/30/00	Pg. 5, 6	Insert clarification note to Recommended Operating Temperature and Absolute Max Ratings tables
	Pg. 6	Add BGA capacitance table
	Pg. 5,6, 7	Add note to TQFP and BGA Pin Configurations; corrected typo in pinout
	Pg. 21	Add 100pin TQFP package Diagram Outline
05/26/00		Add new package offering, 13 x 15mm 165 fBGA
	Pg. 25	Correct 119BGA Package Diagram Outline
07/26/00	Pg. 5-8	Add ZZ sleep mode reference note to BG119, PK100 and BQ165 pinouts
	Pg. 8	Update BQ165 pinout
	Pg. 23	Update BG119 package diagram outline dimensions
10/25/00		Remove Preliminary status
	Pg. 8	Add note to pin N5 on BQ165, reserved for JTAG $\overline{TRST}$
01/24/02	Pg. 1-8, 15,22,23,27	Added JTAG "SA" version functionality
09/30/04	Pg. 7	Updated pin configuration for the 119 BGA-reordered I/O signals on P6, P7 (128K x 36) and P7, N6, L6, K7, H6, G7, F6, E7, D6 (256K x 18).
	Pg. 27	Adding "Restricted hazardous substance device" to ordering information.
10/18/06	Pg. 1, 26	Added X generation die step to data sheet.
08/11/08	Pg. 1, 15, 16, 27	Remove 200MHz on 128K x 36 configuration.
10/14/10	Pg. 28	Removed IDT from the ordering information
01/20/15	Pg. 24 -26	Removed PSC Package Diagram Outlines. See idt.com for PSC details
08/06/21	Pg. 1 - 29	Rebranded as Renesas datasheet
	Pg. 5-8 & 25	Updated package codes
	Pg. 1 & 25	Updated Industrial temp range and green availability
		Removed 200MHz for 256K x18
		Removed X die stepping from datasheet
	Pg. 25	Removed IDT from the orderable part number in the ordering information
	Pg. 26 & 27	Added Orderable Part Information tables

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