CMOS PARALLEL-TO-SERIAL FIFO 1,024 x 16

IDT72125

FEATURES:

- **25ns parallel port access time, 35ns cycle time**
- **50MHz serial shift frequency**
- **Wide x16 organization offering easy expansion**
- **Low power consumption (50mA typical)**
- **Least/Most Significant Bit first read selected by asserting the $\overline{FL}$/DIR pin**
- **Four memory status flags: Empty, Full, Half-Full, and Almost-Empty/Almost-Full**
- **Dual-Port zero fall-through architecture**
- **Available in 28-pin 300 mil plastic DIP and 28-pin SOIC**
- **Green parts available, see ordering information**

DESCRIPTION:

The IDT72125 is a high-speed, low- power, dedicated, parallel-to-serial FIFO. This FIFO features a 16-bit parallel input port and a serial output port with 1,024 word depths, respectively.

The ability to buffer wide word widths (x16) make these FIFOs ideal for laser printers, FAX machines, local area networks (LANs), video storage and disk/tape controller applications.

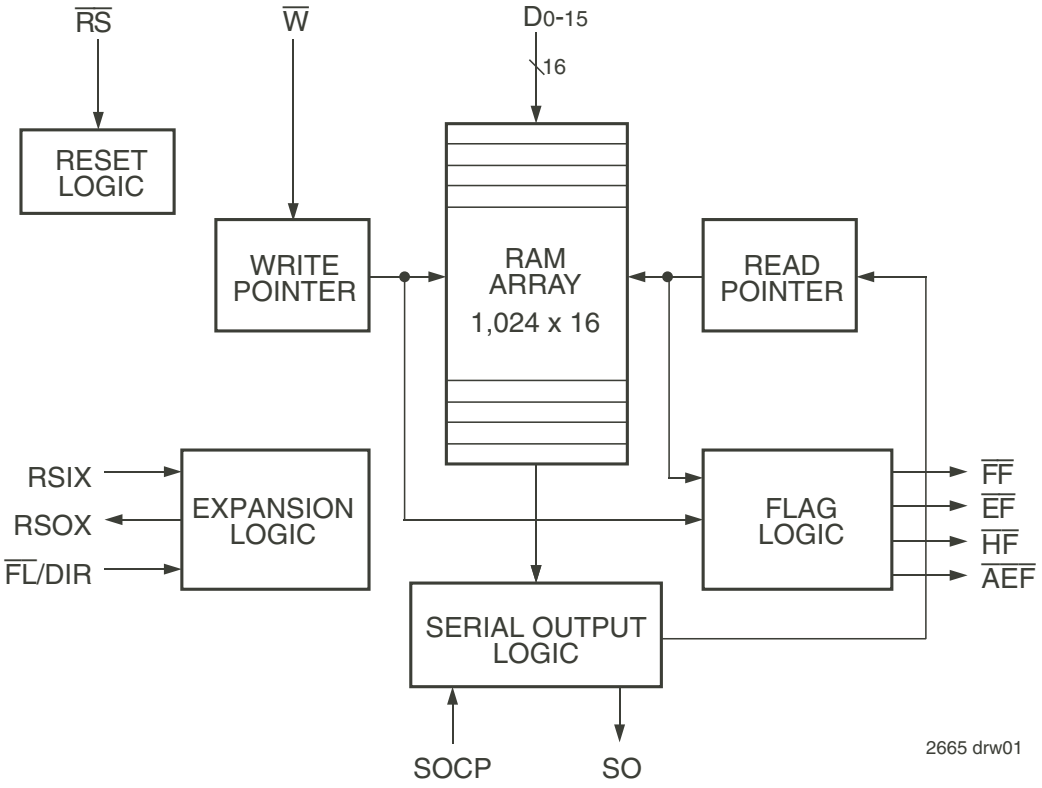
Expansion in width and depth can be achieved using multiple chips. IDT's unique serial expansion logic makes this possible using a minimum of pins.

The unique serial output port is driven by one data pin (SO) and one clock pin (SOCP). The Least Significant or Most Significant Bit can be read first by programming the DIR pin after a reset.

Monitoring the FIFO is eased by the availability of four status flags: Empty, Full, Half-Full and Almost-Empty/Almost-Full. The Full and Empty flags prevent any FIFO data overflow or underflow conditions. The Half-Full Flag is available in both single and expansion mode configurations. The Almost-Empty/Almost-Full Flag is available only in a single device mode.

The IDT72125 is fabricated using submicron CMOS technology.

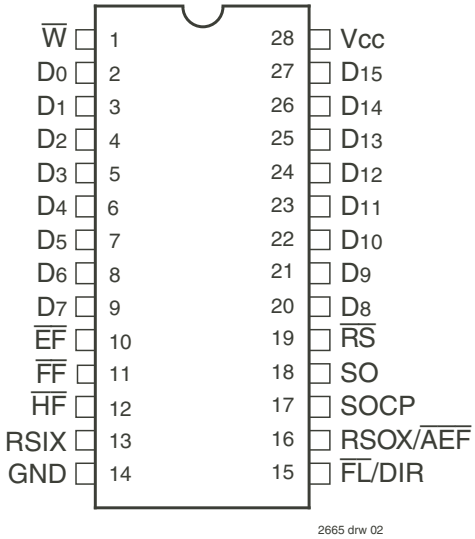
FUNCTIONAL BLOCK DIAGRAM



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PIN CONFIGURATION



PLASTIC THIN DIP (P28, order code: TP)
SOIC (SO28, order code: SO)
TOP VIEW

PIN DESCRIPTIONS

Symbol	Name	I/O	Description
D0–D15	Inputs	I	Data inputs for 16-bit wide data.
$\overline{RS}$	Reset	I	When $\overline{RS}$ is set low, internal READ and WRITE pointers are set to the first location of the RAM array. $\overline{FF}$ and $\overline{HF}$ go HIGH. $\overline{EF}$ and $\overline{AEF}$ go LOW. A reset is required before an initial WRITE after power-up. $\overline{W}$ must be high during the $\overline{RS}$ cycle. Also the First Load pin ($\overline{FL}$) is programmed only during Reset.
$\overline{W}$	Write	I	A write cycle is initiated on the falling edge of WRITE if the Full Flag ($\overline{FF}$) is not set. Data set-up and hold times must be adhered to with respect to the rising edge of WRITE. Data is stored in the RAM array sequentially and independently of any ongoing read operation.
SOCP	Serial Output Clock	I	A serial bit read cycle is initiated on the rising edge of SOCP if the Empty Flag ($\overline{EF}$) is not set. In both Depth and Serial Word Width Expansion modes, all of the SOCP pins are tied together.
$\overline{FL}$/DIR	First Load/Direction	I	This is a dual purpose input used in the width and depth expansion configurations. The First Load ($\overline{FL}$) function is programmed only during Reset ($\overline{RS}$) and a LOW on $\overline{FL}$ indicates the first device to be loaded with a byte of data. All other devices should be programmed HIGH. The Direction (DIR) pin controls shift direction after Reset and tells the device whether to read out the Least Significant or Most Significant bit first.
RSIX	Read Serial In Expansion	I	In the single device configuration, RSIX is set HIGH. In depth expansion or daisy chain expansion, RSIX is connected to RSOX (expansion out) of the previous device.
SO	Serial Output	O	Serial data is output on the Serial Output (SO) pin. Data is clocked out LSB or MSB depending on the Direction pin programming. During Expansion the SO pins are tied together.
$\overline{FF}$	Full Flag	O	When $\overline{FF}$ goes LOW, the device is full and further WRITE operations are inhibited. When $\overline{FF}$ is HIGH, the device is not full.
$\overline{EF}$	Empty Flag	O	When $\overline{EF}$ goes LOW, the device is empty and further READ operations are inhibited. When $\overline{EF}$ is HIGH, the device is not empty.
$\overline{HF}$	Half-Full Flag	O	When $\overline{HF}$ is LOW, the device is more than half-full. When $\overline{HF}$ is HIGH, the device is empty to half-full.
RSOX/$\overline{AEF}$	Read Serial Out Expansion Almost-Empty, Almost-Full Flag	O	This is a dual purpose output. In the single device configuration (RSIX HIGH), this is an $\overline{AEF}$ output pin. When $\overline{AEF}$ is LOW, the device is empty-to-(1/8 full -1) or (7/8 full +1)-to-full. When $\overline{AEF}$ is HIGH, the device is 1/8-full up to 7/8-full. In the Expansion configuration (RSOX connected to RSIX of the next device) a pulse is sent from RSOX to RSIX to coordinate the width, depth or daisy chain expansion.
VCC	Power Supply		Single power supply of 5V.
GND	Ground		Single ground of 0V.

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STATUS FLAGS

Number of Words in FIFO				
IDT72125	$\overline{FF}$	$\overline{AEF}$	$\overline{HF}$	$\overline{EF}$
0	H	L	H	L
1–127	H	L	H	H
128–512	H	H	H	H
513–896	H	H	L	H
897–1023	H	L	L	H
1024	L	L	L	H

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Description	Max	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
T_{STG}	Storage Temperature	–55 to +125	°C
I_{OUT}	DC Output Current	–50 to +50	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input HIGH Voltage	2	—	—	V
V_{IL}(1)	Input LOW Voltage	—	—	0.8	V
T_A	Operating Temperature	0	—	+70	°C

NOTE:
1. 1.5V undershoots are allowed for 10ns once per cycle.

DC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5V ± 10%, T_A = 0°C to +70°C)

Symbol	Parameter	IDT72125 Commercial			Unit
		Min.	Typ.	Max.	
I_{LI} (1)	Input Leakage Current (Any Input)	–1	—	1	µA
I_{LO}(2)	Output Leakage Current	–10	—	10	µA
V_{OH}	Output Logic "1" Voltage IOUT = –2mA(3)	2.4	—	—	V
V_{OL}	Output Logic "0" Voltage IOUT = 8mA(4)	—	—	0.4	V
I_{CC1}(5)	Active Power Supply Current	—	50	100	mA
I_{CC2}(5,6,7)	Standby Current ($\overline{W}$ = $\overline{RS}$ = $\overline{FL}$/DIR = VIH; SOCP = VIL)	—	4	8	mA
I_{CC3}(5,6,7)	Power Down Current	—	1	6	mA

NOTES:
1. Measurements with 0.4V ≤ V_{IN} ≤ V_{CC}.
2. SOCP = V_{IL}, 0.4 ≤ V_{OUT} ≤ V_{CC}.
3. For SO, I_{OUT} = -4mA.
4. For SO, I_{OUT} = 16mA.
5. Tested with outputs open (I_{OUT} = 0).
6. $\overline{RS}$ = $\overline{FL}$/DIR = $\overline{W}$ = V_{CC} - 0.2V; SOCP = 0.2V; all other inputs - V_{CC} - 0.2.
7. Measurements are made after reset.

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AC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5V ± 10%, T_A = 0°C to +70°C)

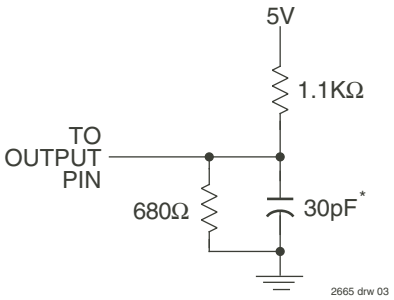
Symbol	Parameter	Figure	Commercial IDT72125L25 Min.	Commercial IDT72125L25 Max.	Unit
t_S	Parallel Shift Frequency	—	—	28.5	MHz
t_{SOCP}	Serial Shift Frequency	—	—	50	MHz
PARALLEL INPUT TIMINGS					
t_{WC}	Write Cycle Time	2	35	—	ns
t_{WPW}	Write Pulse Width	2	25	—	ns
t_{WR}	Write Recovery Time	2	10	—	ns
t_{DS}	Data Set-up Time	2	12	—	ns
t_{DH}	Data Hold Time	2	0	—	ns
t_{WEF}	Write High to $\overline{EF}$ HIGH	5, 6	—	35	ns
t_{WFF}	Write Low to $\overline{FF}$ LOW	4, 7	—	35	ns
t_{WF}	Write Low to Transitioning $\overline{HF}$, $\overline{AEF}$	8	—	35	ns
t_{WPF}	Write Pulse Width After $\overline{FF}$ HIGH	7	25	—	ns
SERIAL OUTPUT TIMINGS					
t_{SOCP}	Serial Clock Cycle Time	3	20	—	ns
t_{SOCW}	Serial Clock Width HIGH/LOW	3	8	—	ns
t_{SOPD}	SOCP Rising Edge to SO Valid Data	3	—	14	ns
t_{SOHZ}	SOCP Rising Edge to SO at High-Z(1)	3	3	14	ns
t_{SOLZ}	SOCP Rising Edge to SO at Low-Z(1)	3	3	14	ns
t_{SOCEF}	SOCP Rising Edge to $\overline{EF}$ LOW	5, 6	—	35	ns
t_{SOCFF}	SOCP Rising Edge to $\overline{FF}$ HIGH	4, 7	—	35	ns
t_{SOCF}	SOCP Rising Edge to Transitioning $\overline{HF}$, $\overline{AEF}$	8	—	35	ns
t_{REFSO}	SOCP Delay After $\overline{EF}$ HIGH	6	35	—	ns
RESET TIMINGS					
t_{RSC}	Reset Cycle Time	1	35	—	ns
t_{RS}	Reset Pulse Width	1	25	—	ns
t_{RSS}	Reset Set-up Time	1	25	—	ns
t_{RSR}	Reset Recovery Time	1	10	—	ns
EXPANSION MODE TIMINGS					
t_{FLS}	$\overline{FL}$ Set-up Time to $\overline{RS}$ Rising Edge	9	7	—	ns
t_{FLH}	$\overline{FL}$ Hold Time to $\overline{RS}$ Rising Edge	9	0	—	ns
t_{DIRS}	DIR Set-up Time to SOCP Rising Edge	9	10	—	ns
t_{DIRH}	DIR Hold Time from SOCP Rising Edge	9	5	—	ns
t_{SOXD1}	SOCP Rising Edge to RSOX Rising Edge	9	—	15	ns
t_{SOXD2}	SOCP Rising Edge to RSOX Falling Edge	9	—	15	ns
t_{SIXS}	RSIX Set-up Time to SOCP Rising Edge	9	5	—	ns
t_{SIXPW}	RSIX Pulse Width	9	10	—	ns

NOTE:
1. Values guaranteed by design.

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AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure A



or equivalent circuit

Figure A. Output Load

* Includes scope and jig capacitances.

CAPACITANCE (T_A = +25°C, f = 1.0 MHz)

Symbol	Parameter[1]	Condition	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	12	pF

NOTE:
1. Characterized values, not currently tested.

FUNCTIONAL DESCRIPTION

PARALLEL DATA INPUT

The device must be reset before beginning operation so that all flags are set to their initial state. In width or depth expansion the First Load pin ($\overline{FL}$) must be programmed to indicate the first device.

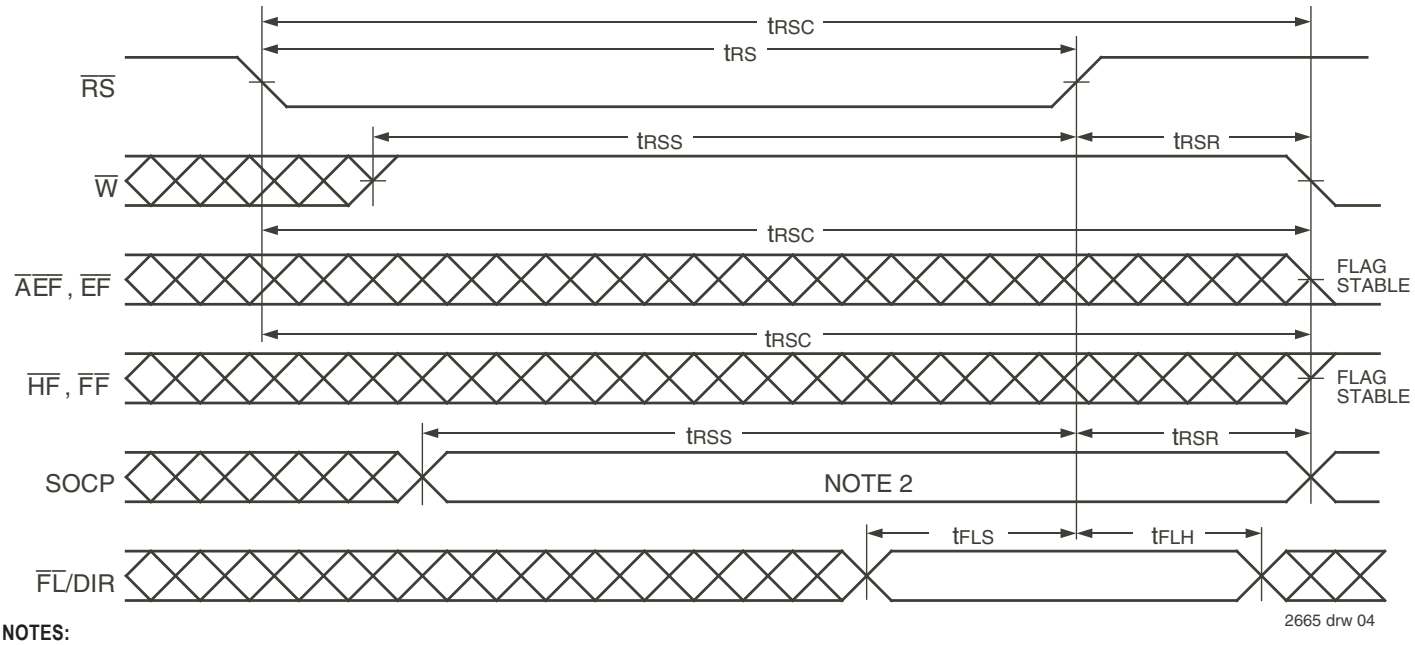
The data is written into the FIFO in parallel through the D0–D15 input data lines. A write cycle is initiated on the falling edge of the Write ($\overline{W}$) signal provided the Full Flag ($\overline{FF}$) is not asserted. If the $\overline{W}$ signal changes from HIGH-to-LOW and the Full Flag ($\overline{FF}$) is already set, the write line is internally inhibited internally from incrementing the write pointer and no write operation occurs.

Data set-up and hold times must be met with respect to the rising edge of Write. On the rising edge of $\overline{W}$, the write pointer is incremented. Write operations can occur simultaneously or asynchronously with read operations.

SERIAL DATA OUTPUT

The serial data is output on the SO pin. The data is clocked out on the rising edge of SOCP providing the Empty Flag ($\overline{EF}$) is not asserted. If the Empty Flag is asserted then the next data word is inhibited from moving to the output register and being clocked out by SOCP.

The serial word is shifted out Least Significant Bit or Most Significant Bit first, depending on the $\overline{FL}$/DIR level during operation. A LOW on DIR will cause the Least Significant Bit to be read out first. A HIGH on DIR will cause the Most Significant Bit to be read out first.



NOTES:
1. $\overline{EF}$, $\overline{FF}$, $\overline{HF}$ and $\overline{AEF}$ may change status during Reset, but flags will be valid at t_{RSC}.
2. SOCP should be in the steady LOW or HIGH during t_{RSS}. The first LOW-HIGH (or HIGH-LOW) transition can begin after t_{RSR}.

Figure 1. Reset

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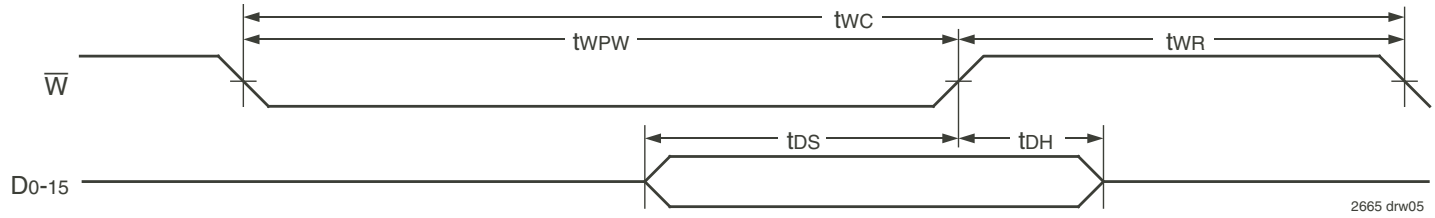
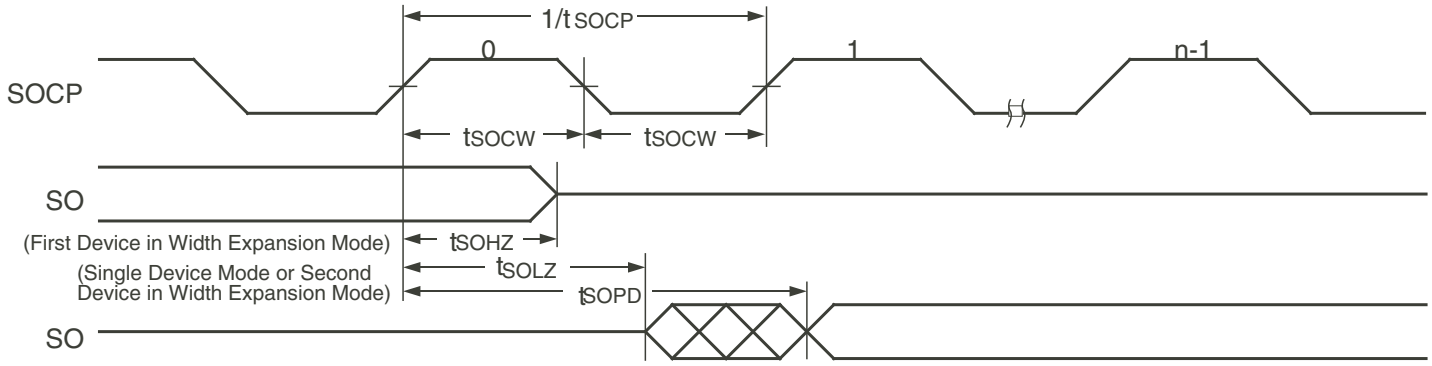


Figure 2. Write Operation



NOTE:
1. In Single Device Mode, SO will not tri-state except after reset.

Figure 3. Read Operation

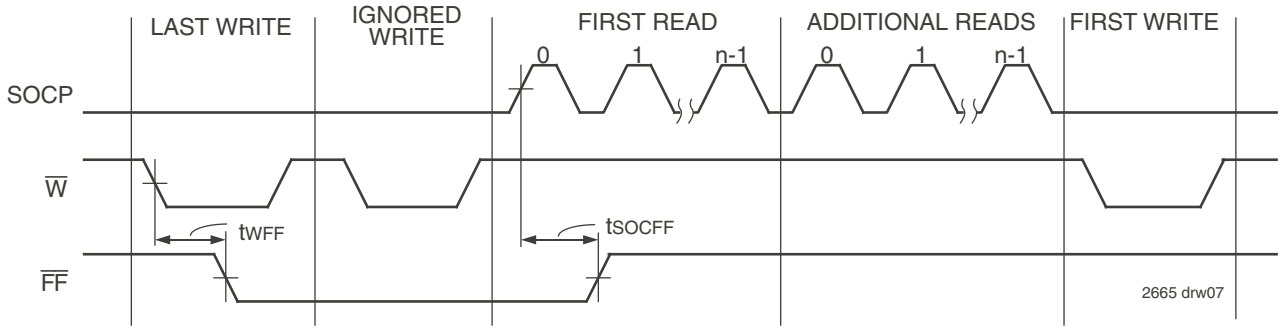
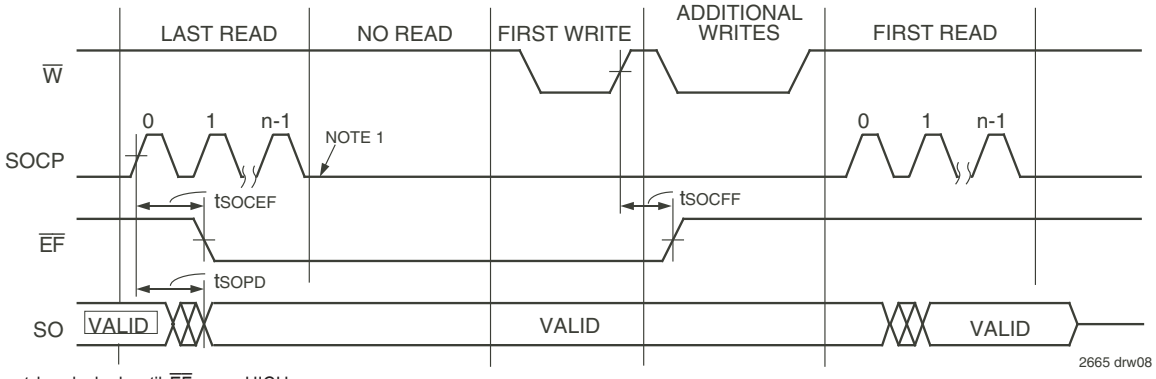


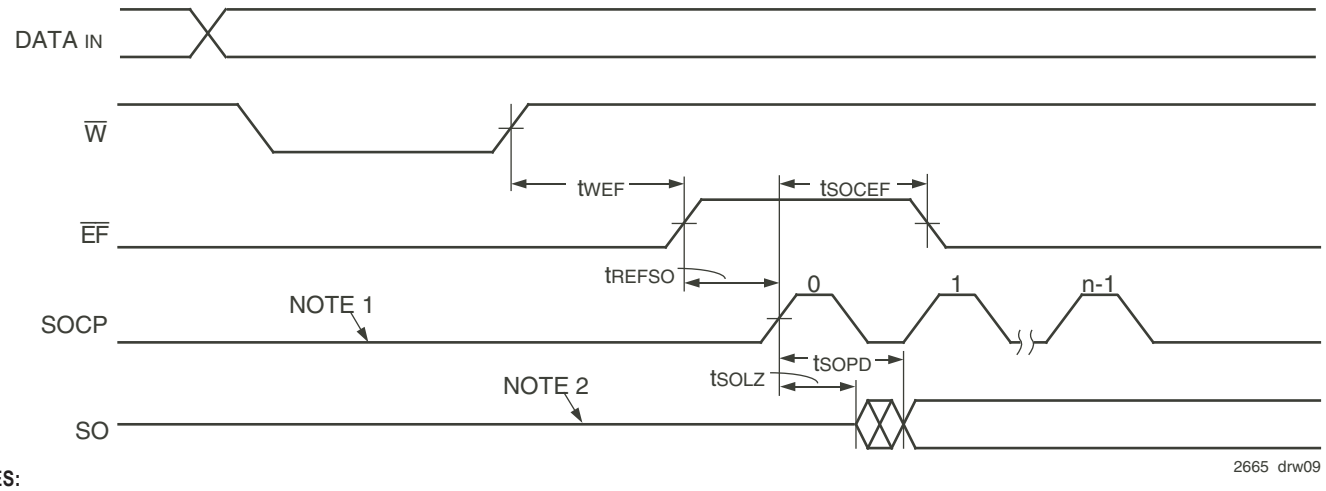
Figure 4. Full Flag from Last Write to First Read



NOTE:
1. SOCP should not be clocked until $\overline{EF}$ goes HIGH.

Figure 5. Empty Flag from Last Read to First Write

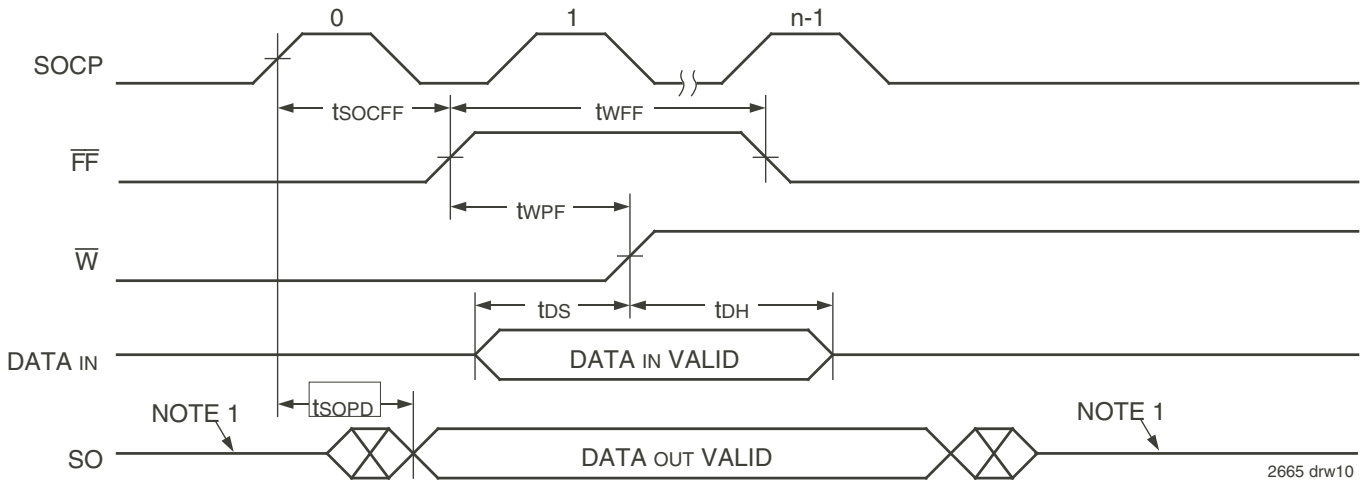
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NOTES:

1. Once $\overline{EF}$ has gone LOW and the last bit of the final word has been shifted out, SOCP should not be clocked until $\overline{EF}$ goes HIGH.
2. In Single Device Mode, SO will not tri-state except after Reset. It will retain the last valid data.

Figure 6. Empty Boundary Condition Timing



NOTE:

1. Single Device Mode will not tri-state but will retain the last valid data.

Figure 7. Full Boundary Condition Timing

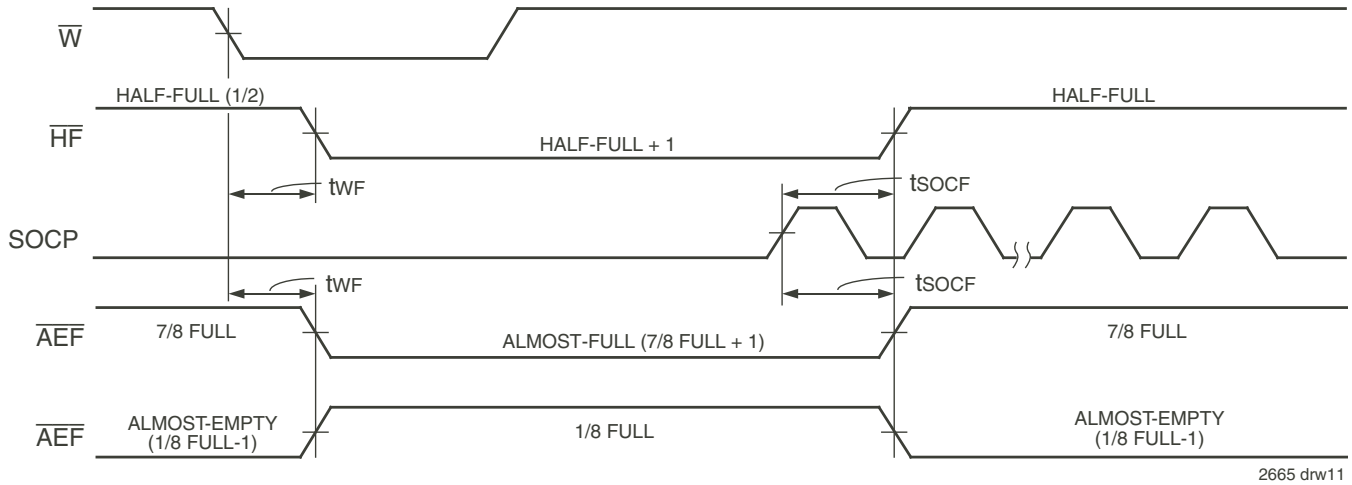


Figure 8. Half-Full, Almost-Full and Almost-Empty Timings

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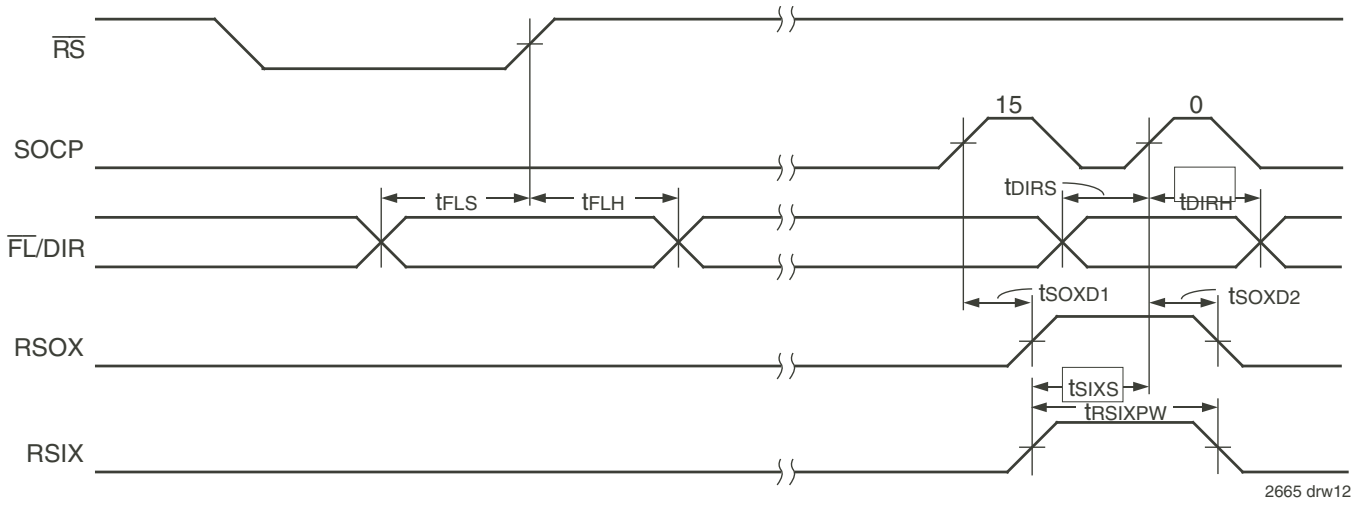


Figure 9. Serial Read Expansion

OPERATING CONFIGURATIONS

SINGLE DEVICE MODE

The device must be reset before beginning operation so that all flags are set to location zero. In the standalone case, the RSIX line is tied HIGH and indicates single device operation to the device. The RSOX/$\overline{AEF}$ pin defaults to $\overline{AEF}$ and outputs the Almost-Empty and Almost-Full Flag.

WIDTH EXPANSION MODE

In the cascaded case, word widths of more than 16 bits can be achieved by using more than one device. By tying the RSOX and RSIX pins together, as shown in Figure 11, and programming which is the Least Significant Device, a cascaded serial word is achieved. The Least Significant Device is programmed by a LOW on the $\overline{FL}$/DIR pin during reset. All other devices should be programmed HIGH on the $\overline{FL}$/DIR pin at reset.

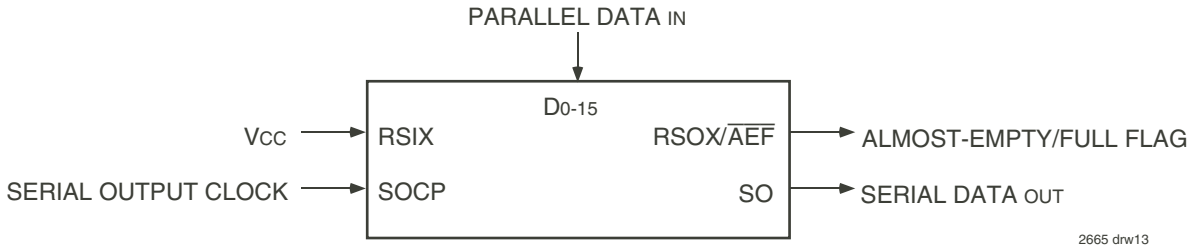


Figure 10. Single Device Configuration

TABLE 1 — RESET AND FIRST LOAD TRUTH TABLE-SINGLE DEVICE CONFIGURATION

Mode	Inputs			Internal Status		Outputs		
	$\overline{RS}$	$\overline{FL}$	DIR	Read Pointer	Write Pointer	$\overline{AEF}$, $\overline{EF}$	$\overline{FF}$	$\overline{HF}$
Reset	0	X	X	Location Zero	Location Zero	0	1	1
Read/Write	1	X	0,1	Increment[1]	Increment[1]	X	X	X

NOTE:
1. Pointer will increment if appropriate flag is HIGH

The Serial Data Output (SO) of each device in the serial word must be tied together. Since the SO pin is three stated, only the device which is currently shifting out is enabled and driving the 1-bit bus. NOTE: After reset, the level on the $\overline{FL}$/DIR pin decides if the Least Significant or Most Significant Bit is read first out of each device.

The three flag outputs, Empty ($\overline{EF}$), Half-Full ($\overline{HF}$) and Full ($\overline{FF}$), should be taken from the Most Significant Device (in the example, FIFO #2). The Almost-Empty/Almost-Full flag is not available. The RSOX pin is used for expansion.

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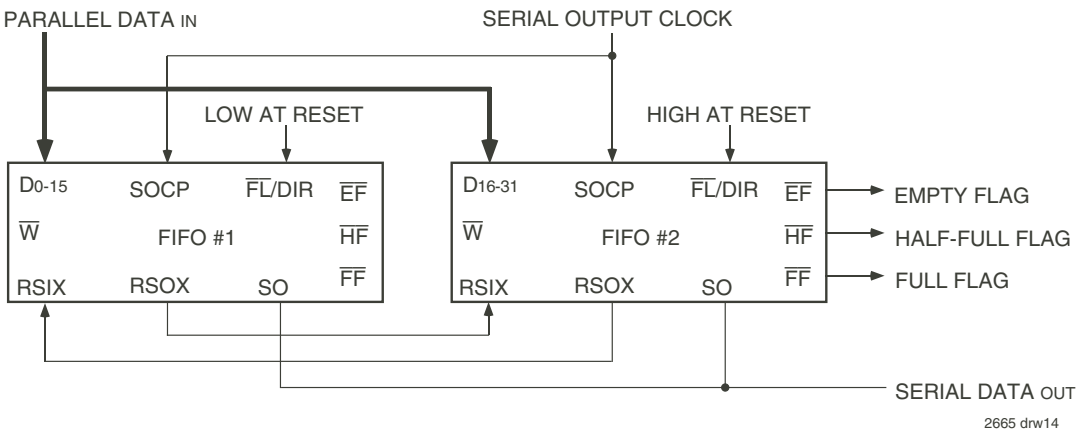


Figure 11. Width Expansion for 32-bit Parallel Data In

OPERATING CONFIGURATIONS

SINGLE DEVICE MODE

The IDT72125 can easily be adapted to applications requiring greater than 1,024 words. Figure 12 demonstrates Depth Expansion using three IDT72125s and an 74FCT138 Address Decoder. Any depth can be attained by adding additional devices. The Address Decoder is necessary to determine which FIFO is being written. A word of data must be written sequentially into each FIFO so that the data will be read in the correct sequence. These devices operate in the Depth Expansion Mode when the following conditions are met:

1. The first device must be programmed by holding $\overline{FL}$ LOW at Reset. All other devices must be programmed by holding $\overline{FL}$ HIGH at reset.
2. The Read Serial Out Expansion pin (RSOX) of each device must be tied to the Read Serial In Expansion pin (RSIX) of the next device (see Figure 12).
3. External logic is needed to generate composite Empty, Half-Full and Full Flags. This requires the ORing of all $\overline{EF}$, $\overline{HF}$ and $\overline{FF}$ Flags.
4. The Almost-Empty and Almost-Full Flag is not available due to using the RSOX pin for expansion.

COMPOUND EXPANSION (DAISY CHAIN) MODE

These FIFOs can be expanded in both depth and width as Figure 13 indicates:

1. The RSOX-to-RSIX expansion signals are wrapped around sequentially.
2. The write ($\overline{W}$) signal is expanded in width.
3. Flag signals are only taken from the Most Significant Devices.
4. The Least Significant Device in the array must be programmed with a LOW on $\overline{FL}$/DIR during reset.

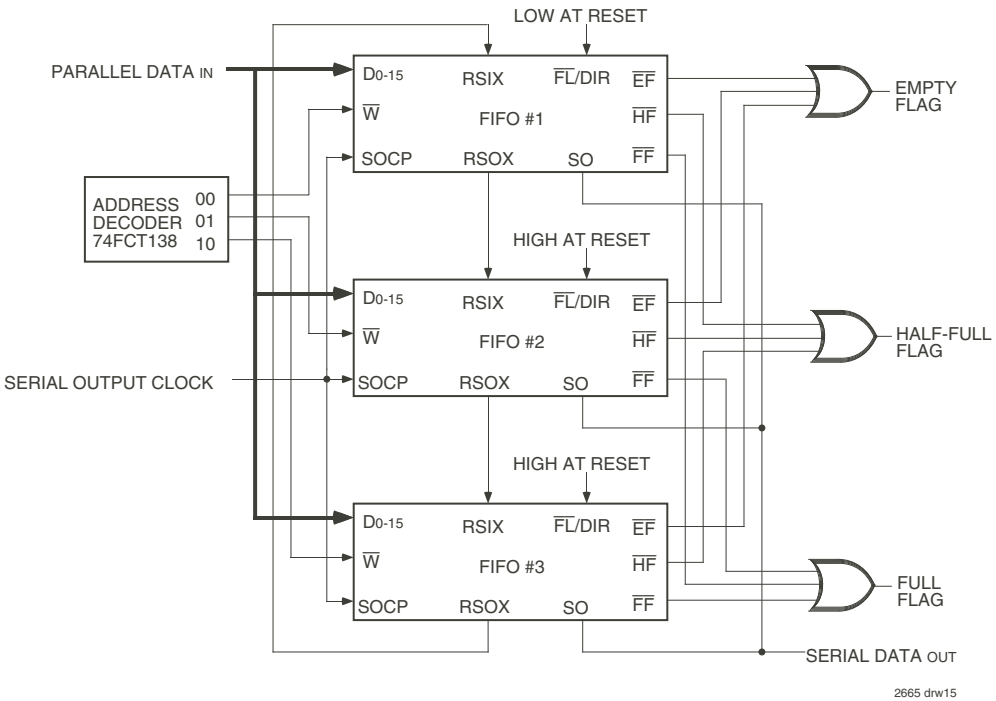


Figure 12. A 3K x 16 Parallel-to-Serial FIFO using the IDT72125

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TABLE 2 — RESET AND FIRST LOAD TRUTH TABLE-WIDTH/DEPTH COMPOUND EXPANSION MODE

Mode	Inputs			Internal Status		Outputs	
	$\overline{RS}$	$\overline{FL}$	DIR	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{HF}$, $\overline{FF}$
Reset-First Device	0	0	X	Location Zero	Location Zero	0	1
Reset All Other Devices	0	1	X	Location Zero	Location Zero	0	1
Read/Write	1	X	0,1	X	X	X	X

NOTE:
1. $\overline{RS}$ = Reset Input, $\overline{FL}$/FIR = First Load/Direction, $\overline{EF}$ = Empty Flag Output, $\overline{HF}$ = Half-Full Flag Output, $\overline{FF}$ = Full Flag Output.

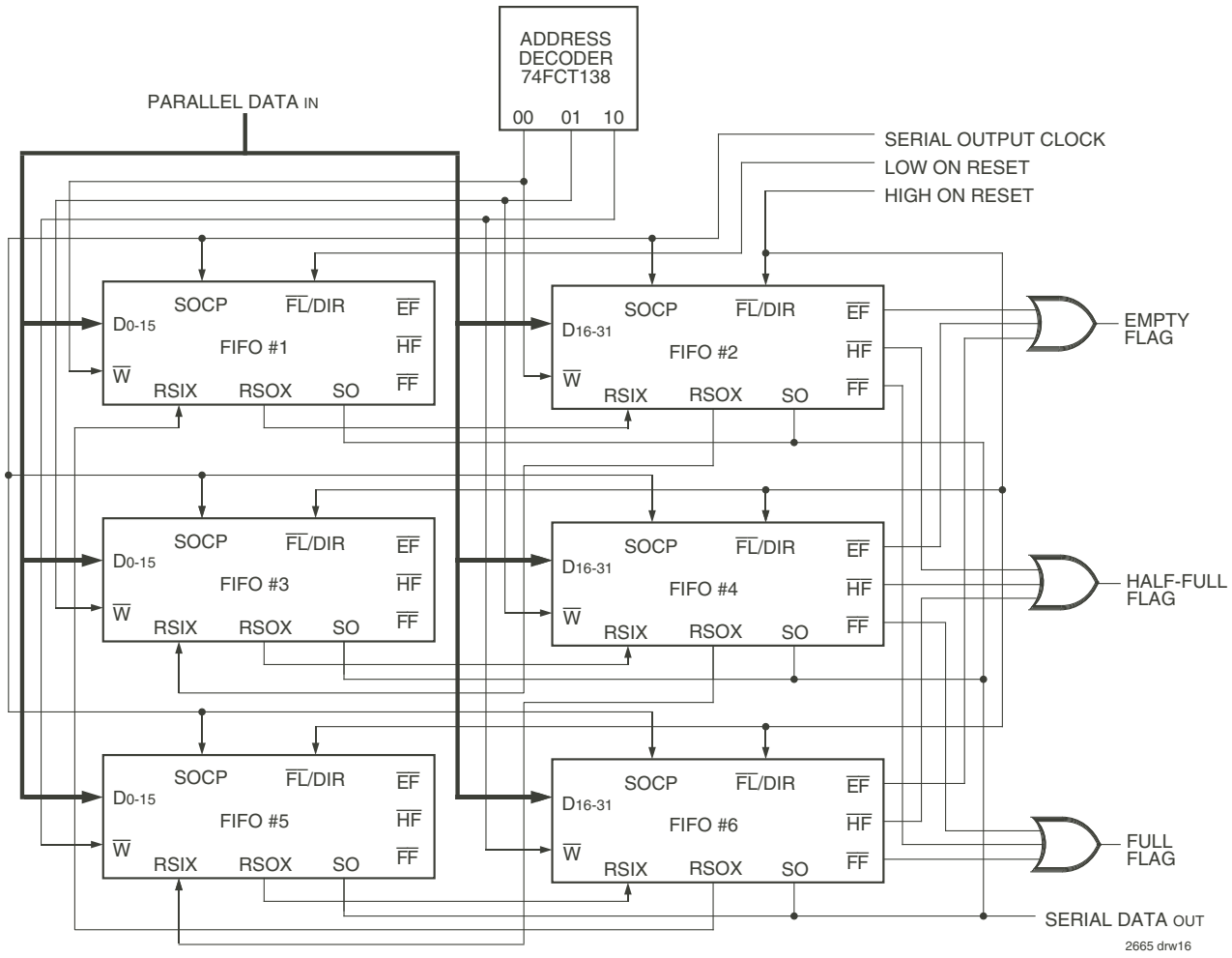
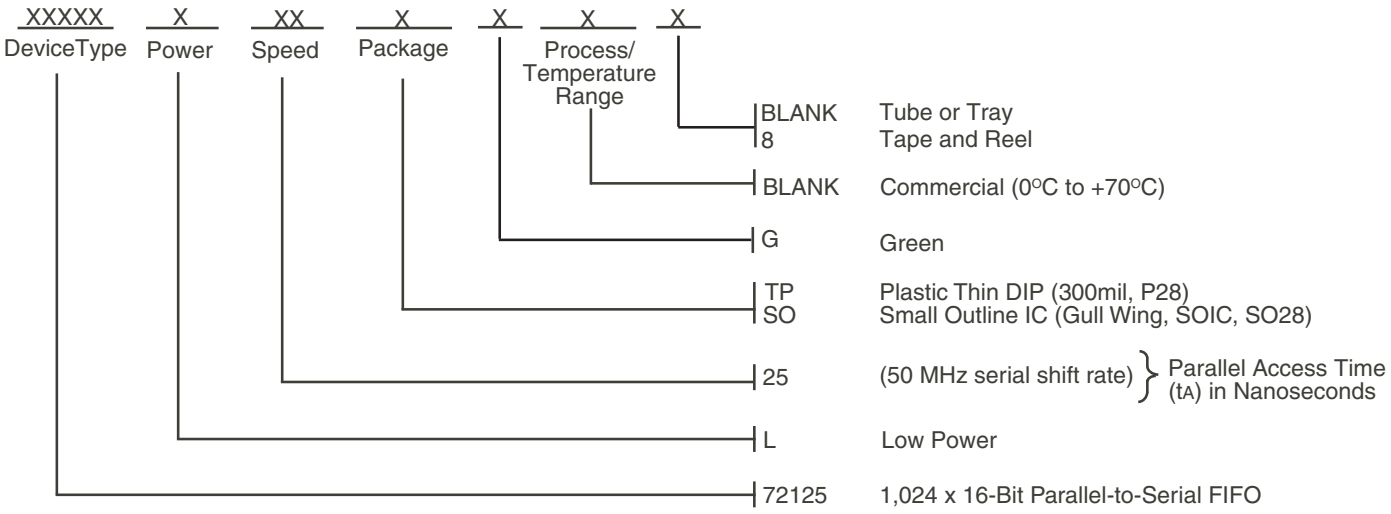


Figure 13. A 3K x 32 Parallel-to-Serial FIFO using the IDT72125

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