CMOS TRIPLE BUS SyncFIFO™ WITH BUS-MATCHING AND BYTE SWAPPING 64 x 36 x 2

IDT723616
OBSOLETE PART

OBSOLETE PART
NOT RECOMMENDED FOR
NEW DESIGNS

FEATURES:

- **Two independent FIFOs (64 X 36 storage capacity each) buffer data between bidirectional 36-bit port A and two unidirectional 18/9-bit ports (Port B transmits, Port C receives)**
- **Clock frequencies up to 67 MHz (10 ns access time)**
  Free-running clock lines for each port: CLKA, CLKB and CLKC, may be asynchronous or coincident (simultaneous reading and writing of data is permitted)
- **IDT Standard timing**
- **Empty flag functions: $\overline{EFA}$ (synchronized by CLKA) and $\overline{EFB}$ (synchronized by CLKB)**
- **Full flag functions: $\overline{FFA}$ (synchronized by CLKA) and $\overline{FFC}$ (synchronized by CLKC)**
- **Programmable Almost-Empty and Almost-Full flags; each has four default offsets (4, 8, 12 and 16)**
- **Bus sizing of 18-bits (word) and 9-bits (byte) for ports B and C**
- **Byte order swapping on ports B and C**
- **Passive parity checking on ports A and C**
- **Parity generation can be selected for ports A and B**
- **Master Reset clears data and configures FIFO**
- **Width can be easily expanded by adding FIFOs**
- **Auto power down minimizes power dissipation**
- **Available in a space-saving 128-pin Thin Quad Flatpack (TQFP)**
- **High performance sub-micron CMOS technology**
- **Industrial temperature range (–40°C to +85°C) is available**
- **Green parts available, see ordering information**

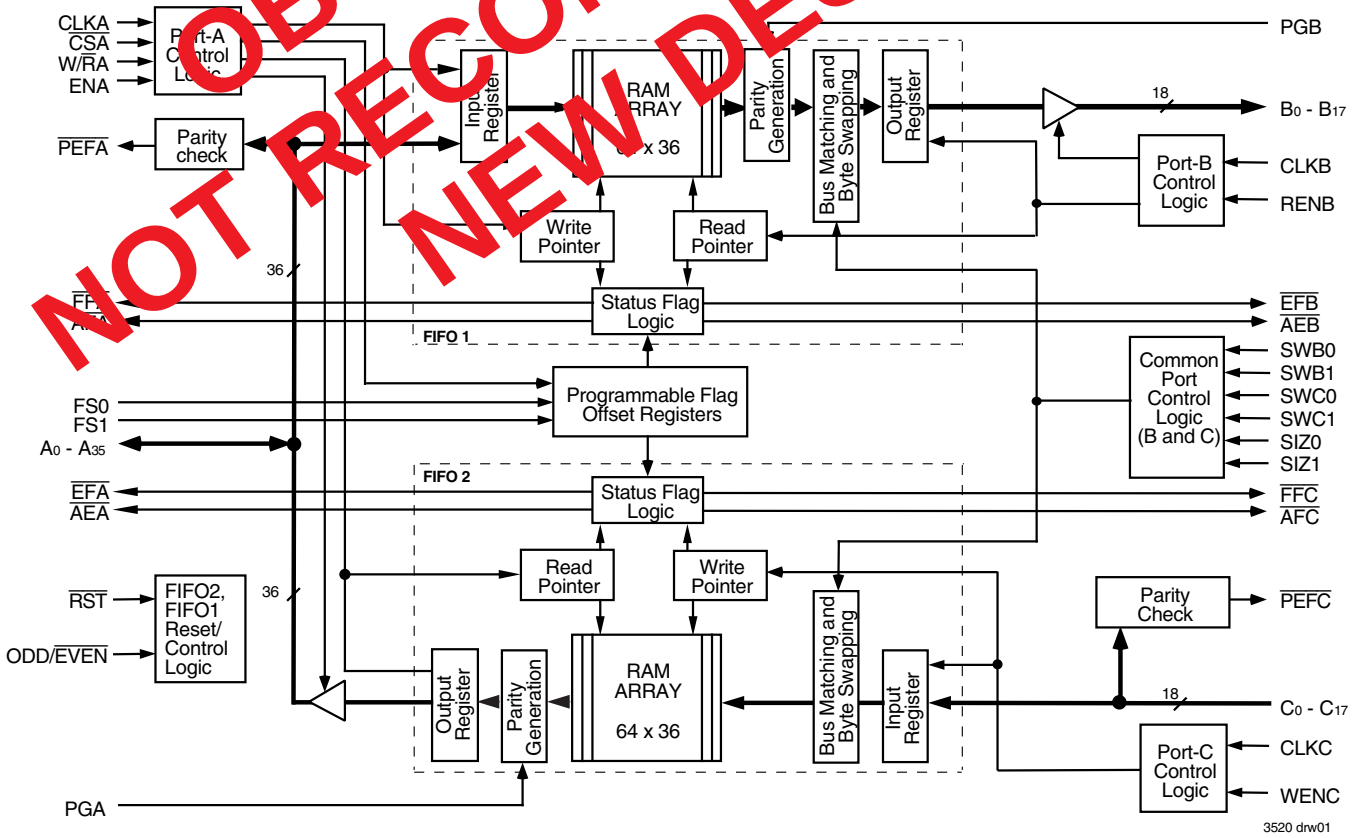
DESCRIPTION:

The IDT723616 is a monolithic, high-speed, low-power, CMOS Triple Bus SyncFIFO™ (clocked) memory which supports clock frequencies up to 67 MHz and has read access times as fast as 10 ns. Two independent 64 x 36 dual-port SRAM FIFOs on board each chip buffer data between a bidirectional 36-bit bus (Port A) and two unidirectional 18-bit buses (Port B transmits data, Port C receives data.) FIFO data can be read out of ports B and written into port A using either 18-bit or 9-bit formats.

Reset ($\overline{RST}$) initializes the read and write pointers to the first location of the memory array and selects one of four possible default flag offset settings: 4, 8, 12 or 16.

Each FIFO has flags to indicate empty and full conditions and two programmable flags (Almost-Full and Almost-Empty) to indicate when a selected

FUNCTIONAL BLOCK DIAGRAM



IDT and the IDT logo are registered trademarks of Integrated Device Technology, Inc. SyncFIFO is a trademark of Integrated Device Technology, Inc.

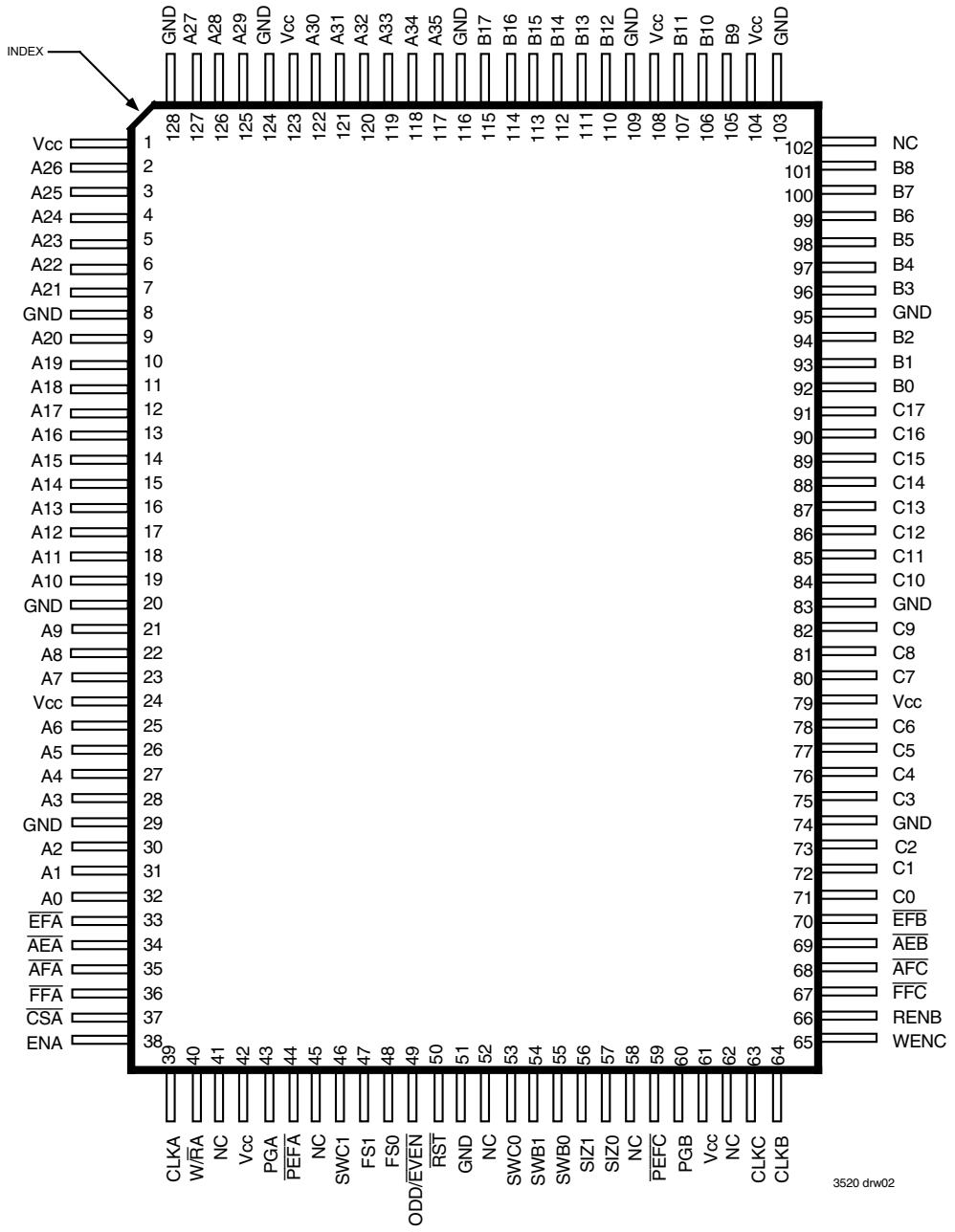
© 2019 Renesas Electronics Corporation

DESCRIPTION (CONTINUED)

number of words is stored in memory. Data on Port B can be accessed in 18-bit and 9-bit formats. FIFO Data on Port C can be input in 18-bit and 9-bit formats. Byte-order swapping on ports B and C is possible with any bus size selection. Parity is checked passively on ports A and C and may be ignored if not desired. Parity generation can be selected for data read from ports A and B. Two or more devices can be used in parallel to create wider or deeper FIFO configurations.

This device is a clocked FIFO, which means each port employs a synchronous interface. All data transfers through a port are gated to the LOW-to-HIGH transition of a continuous (free-running) port clock by enable signals. The clocks for each port are independent of one another and can be asynchronous or coincident. The enables for each port are arranged to provide a simple bidirectional interface between microprocessors and/or buses controlled by a synchronous interface.

PIN CONFIGURATION



TQFP (PK128-1, ORDER CODE: PF)
TOP VIEW

NOTE:
1. NC - No internal connection.

© 2019 Renesas Electronics Corporation

This FIFO employs IDT Standard Mode timing; that is to say, the first word written to an empty FIFO is deposited into the memory array. A read operation is required to access that word (along with all other words residing in memory).

Each FIFO has an Empty Flag ($\overline{EFA}$ and $\overline{EFB}$) and a Full Flag ($\overline{FFA}$ and $\overline{FFC}$). $\overline{EF}$ indicates whether or not the FIFO memory is empty. $\overline{FF}$ shows whether the memory is full or not.

Each FIFO has a programmable Almost-Empty flag ($\overline{AEA}$ and $\overline{AEB}$) and a programmable Almost-Full flag ($\overline{AFA}$ and $\overline{AFC}$). $\overline{AEA}$ and $\overline{AEB}$ indicate when a selected number of words written to FIFO memory achieve a predetermined "almost-empty state". $\overline{AFA}$ and $\overline{AFC}$ indicate when a selected number of words written to the memory achieve a predetermined "almost-full state".

$\overline{FFA}$, $\overline{FFC}$, $\overline{AFA}$ and $\overline{AFC}$ are two-stage synchronized to the port clock that writes data into its array. $\overline{EFA}$, $\overline{EFB}$, $\overline{AEA}$, and $\overline{AEB}$ are two-stage synchronized to the port clock that reads data from its array. Four default offset settings are also provided. The $\overline{AEA}$ and $\overline{AEB}$ threshold can be set at 4, 8, 12 or 16 locations from the empty boundary and the $\overline{AFA}$ and $\overline{AFC}$ threshold can be set at 4, 8, 12 or 16 locations from the full boundary. All these choices are made using the FS0 and FS1 inputs during Reset.

Two or more FIFOs may be used in parallel to create wider data paths. Such a width expansion requires no additional, external components.

If, at any time, the FIFO is not actively performing a function, the chip will automatically power down. During the power down state, supply current consumption (ICC) is at a minimum. Initiating any operation (by activating control inputs) will immediately take the device out of the Power Down state.

The IDT723616 are characterized for operation from 0°C to 70°C. They are fabricated using IDT's high speed, submicron CMOS technology.

© 2019 Renesas Electronics Corporation

PIN DESCRIPTION

Symbol	Name	I/O	Description
A0-A35	Port A Data	I/O	36-bit bidirectional data port for side A.
$\overline{AEA}$	Port A Almost-Empty Flag	O	Programmable Almost-Empty flag synchronized to CLKA. It is LOW when the number of 36-bit words in FIFO2 is less than or equal to the value in the offset register, X.
$\overline{AEB}$	Port B Almost-Empty Flag	O	Programmable Almost-Empty flag synchronized to CLKB. It is LOW when the number of 36-bit words in FIFO1 is less than or equal to the value in the offset register, X.
$\overline{AFA}$	Port A Almost-Full Flag	O	Programmable Almost-Full flag synchronized to CLKA. It is LOW when the number of 36-bit empty locations in FIFO1 is less than or equal to the value in the offset register, X.
$\overline{AFC}$	Port C Almost-Full Flag	O	Programmable Almost-Full flag synchronized to CLKC. It is LOW when the number of 36-bit empty locations in FIFO2 is less than or equal to the value in the offset register, X.
B0-B17	Port B Data.	O	18-bit output data port for side B.
C0-C17	Port-C Data	I	18-bit input data port for side C.
CLKA	Port A Clock	I	CLKA is a continuous clock that synchronizes all data transfers through port A and can be asynchronous or coincident to CLKB and CLKC. $\overline{EFA}$, $\overline{FFA}$, $\overline{AFA}$, and $\overline{AEA}$ are synchronized to the LOW-to-HIGH transition of CLKA.
CLKB	Port B Clock	I	CLKB is a continuous clock that synchronizes all data read from port B and can be asynchronous or coincident to CLKA and CLKC. Port B byte swapping and data port sizing operations are also synchronous to the LOW-to-HIGH transition of CLKB. $\overline{EFB}$ and $\overline{AEB}$ are synchronized to the LOW-to-HIGH transition of CLKB.
CLKC	Port-C Clock	I	CLKC is a continuous clock that synchronizes all data written to port C and can be asynchronous or coincident to CLKA and CLKC. $\overline{FFC}$ and $\overline{AFC}$ are synchronized to the LOW-to-HIGH transition of CLKC.
$\overline{CSA}$	Port A Chip Select	I	$\overline{CSA}$ must be LOW to enable a LOW-to-HIGH transition of CLKA to read or write data on port A. The A0-A35 outputs are in the high-impedance state when $\overline{CSA}$ is HIGH.
$\overline{EFA}$	Port A Empty Flag	O	$\overline{EFA}$ is synchronized to the LOW-to-HIGH transition of CLKA. When $\overline{EFA}$ is LOW, FIFO2 is empty, and reads from its memory are disabled. Data can be read from FIFO2 to the output register when $\overline{EFA}$ is HIGH. $\overline{EFA}$ is forced LOW when the device is reset and is set HIGH by the second LOW-to-HIGH transition of CLKA after data is loaded into empty FIFO2 memory.
$\overline{EFB}$	Port B Empty Flag	O	$\overline{EFB}$ is synchronized to the LOW-to-HIGH transition of CLKB. When $\overline{EFB}$ is LOW, the FIFO1 is empty, and reads from its memory are disabled. Data can be read from FIFO1 to the output register when $\overline{EFB}$ is HIGH. $\overline{EFB}$ is forced LOW when the device is reset and is set HIGH by the second LOW-to-HIGH transition of CLKB after data is loaded into empty FIFO1 memory.
ENA	Port A Enable	I	ENA must be HIGH to enable a LOW-to-HIGH transition of CLKA to read or write data on port A.
$\overline{FFA}$	Port A Full Flag	O	$\overline{FFA}$ is synchronized to the LOW-to-HIGH transition of CLKA. When $\overline{FFA}$ is LOW, FIFO1 is full, and writes to its memory are disabled. $\overline{FFA}$ is forced LOW when the device is reset and is set HIGH by the second LOW-to-HIGH transition of CLKA after reset.
$\overline{FFC}$	Port C Full Flag	O	$\overline{FFC}$ is synchronized to the LOW-to-HIGH transition of CLKC. When $\overline{FFC}$ is LOW, FIFO2 is full, and writes to its memory are disabled. $\overline{FFC}$ is forced LOW when the device is reset and is set HIGH by the second LOW-to-HIGH transition of CLKC after reset.
FS1, FS0	Flag-Offset Selects	I	The LOW-to-HIGH transition of $\overline{RST}$ latches the values of FS0 and FS1, which selects one of four preset values for the Almost-Full flag and Almost-Empty flag offset.
ODD/$\overline{EVEN}$	Odd/Even Parity Select	I	Odd parity is checked on each port when ODD/$\overline{EVEN}$ is HIGH, and even parity is checked when ODD/$\overline{EVEN}$ is LOW. ODD/$\overline{EVEN}$ also selects the type of parity generated for each port if parity generation is enabled for a read operation.
$\overline{PEFA}$	Port A Parity Error Flag	O	When any byte applied to terminals A0-A35 fails parity, $\overline{PEFA}$ is LOW. Bytes are organized as A0-A8, A9-A17, A18-A26, and A27-A35, with the most significant bit of each byte serving as the parity bit. The type of parity checked is determined by the state of the ODD/$\overline{EVEN}$ input. The parity trees used to check the A0-A35 inputs are shared by the mail2 register to generate parity if parity generation is selected by PGA. Therefore, if a mail2 read parity generation is setup by having W/$\overline{RA}$ LOW, and PGA HIGH, the $\overline{PEFA}$ flag is forced HIGH regardless of the A0-A35 inputs.

© 2019 Renesas Electronics Corporation

PIN DESCRIPTION (CONTINUED)

Symbol	Name	I/O	Description
$\overline{PEFC}$	Port C Parity Error Flag	O	When any valid byte applied to terminals B0-B17 fails parity, $\overline{PEFC}$ is LOW. Bytes are organized as B0-B8 and B9-B17 with the most significant bit of each byte serving as the parity bit. A byte is valid when it is used by the bus size selected for Port C. The type of parity checked is determined by the state of the ODD/ $\overline{EVEN}$ input. The parity trees used to check the B0-B17 inputs are shared by the mail 1 register to generate parity if parity generation is selected by PGB. Therefore, if a mail1 read with parity generation is setup by having WENC LOW, SIZ1 and SIZ0 HIGH, and PGB HIGH, the $\overline{PEFC}$ flag is forced HIGH regardless of the state of the B0-B17 inputs.
PGA	Port A Parity Generation	I	Parity is generated for data reads from port A when PGA is HIGH. The type of parity generated is selected by the state of the ODD/$\overline{EVEN}$ input. Bytes are organized as A0-A8, A9-A17, A18-A26, and A27-A35. The generated parity bits are output in the most significant bit of each byte.
PGB	Port B Parity Generation	I	Parity is generated for data reads from port B when PGB is HIGH. The type of parity generated is selected by the state of the ODD/$\overline{EVEN}$ input. Bytes are organized as B0-B8 and B9-B17. The generated parity bits are output in the most significant bit of each byte.
RENB	Port B Read Enable	I	RENB must be HIGH to enable a LOW-to-HIGH transition of CLKB to read data on port B.
$\overline{RST}$	Reset	I	To reset the device, four LOW-to-HIGH transitions of CLKA, four LOW-to-HIGH transitions of CLKB, and four LOW-to-HIGH transitions of CLKC must occur while $\overline{RST}$ is LOW. This sets the $\overline{AFA}$ and $\overline{AFC}$ flags HIGH and the $\overline{EFA}$, $\overline{EFB}$, $\overline{AEA}$, $\overline{AEB}$, $\overline{FFA}$, and $\overline{FFC}$ flags LOW. The LOW-to-HIGH transition of $\overline{RST}$ latches the status of the FS1 and FS0 inputs to select Almost-Full and Almost-Empty flag offsets.
SIZ0, SIZ1	Bus Size Select (Ports B and C)	I	The levels on these inputs determine the bus size for ports B and C . These levels must be stable before Master Reset and must remain static for the duration of FIFO operation. Either a word or a byte size may be selected for both ports B and C together; the ports cannot be configured independently.
SWB0 SWB1	Port B Byte Swap	I	The levels on these inputs select one of four modes of byte-order swapping for Port B. These levels must be stable before Master Reset and must remain static for the duration of FIFO operation. The four modes are no swap, byte swap, word swap, and byte-word swap. Byte-order swapping is possible with any bus size selection.
SWC0	Port C Byte Swap	I	The levels on these inputs select one of four modes of byte-order swapping for Port C. These levels must be stable before Master Reset and must remain static for the duration of FIFO operation. The four modes are no swap, byte swap, word swap, and byte-word swap. Byte-order swapping is possible with any bus size selection.
W/$\overline{R}$A	Port A Write/Read Select	I	A HIGH selects a write operation and a LOW selects a read operation on port A for a LOW-to-HIGH transition of CLKA. The A0-A35 outputs are in the high-impedance state when W/$\overline{R}$A is HIGH.
WENC	Port C Write Enable	I	A HIGH selects a Port C write operation for a LOW-to-HIGH transition of CLKC.

© 2019 Renesas Electronics Corporation

ABSOLUTE MAXIMUM RATINGS OVER OPERATING FREE-AIR TEMPERATURE RANGE (UNLESS OTHERWISE NOTED)(1)

Symbol	Rating	Commercial	Unit
V_{CC}	Supply Voltage Range	–0.5 to 7	V
V_I(2)	Input Voltage Range	–0.5 to V_{CC}+0.5	V
V_O(2)	Output Voltage Range	–0.5 to V_{CC}+0.5	V
I_{IK}	Input Clamp Current, (V_I < 0 or V_I > V_{CC})	±20	mA
I_{OK}	Output Clamp Current, (V_O < 0 or V_O > V_{CC})	±50	mA
I_{OUT}	Continuous Output Current, (V_O = 0 to V_{CC})	±50	mA
I_{CC}, I_{GND}	Continuous Current Through V_{CC} or GND	±500	mA
T_{STG}	Storage Temperature Range	–65 to 150	°C

NOTES:
1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "Recommended Operating Conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded provided the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.5	V
V_{IH}	HIGH Level Input Voltage	2	—	V
V_{IL}	LOW-Level Input Voltage	—	0.8	V
I_{OH}	HIGH-Level Output Current	—	–4	mA
I_{OL}	LOW-Level Output Current	—	8	mA
T_A	Operating Free-air Temperature	0	70	°C

ELECTRICAL CHARACTERISTICS OVER RECOMMENDED OPERATING FREE-AIR TEMPERATURE RANGE (UNLESS OTHERWISE NOTED)

		IDT723616 Commercial & Industrial(1) t_A = 15, 20 ns			
Parameter	Test Conditions	Min.	Typ.(1)	Max.	Unit
V_{OH}	V_{CC} = 4.5V, I_{OH} = –4 mA	2.4	—	—	V
V_{OL}	V_{CC} = 4.5 V, I_{OL} = 8 mA	—	—	0.5	V
I_I	V_{CC} = 5.5 V, V_I = V_{CC} or 0	—	—	±50	µA
I_{OZ}	V_{CC} = 5.5 V, V_O = V_{CC} or 0	—	—	±50	µA
I_{CC}(3)	V_{CC} = 5.5 V, I_O = 0 mA, V_I = V_{CC} or GND	—	—	1	mA
C_{IN}	V_I = 0, f = 1 MHz	—	4	—	pF
C_{OUT}	V_O = 0, f = 1 MHz	—	8	—	pF

NOTES:
1. Industrial temperature range product for 20ns speed grade is available as a standard device. All other speed grades are available by special order.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3 For additional ICC information, see following page.

© 2019 Renesas Electronics Corporation

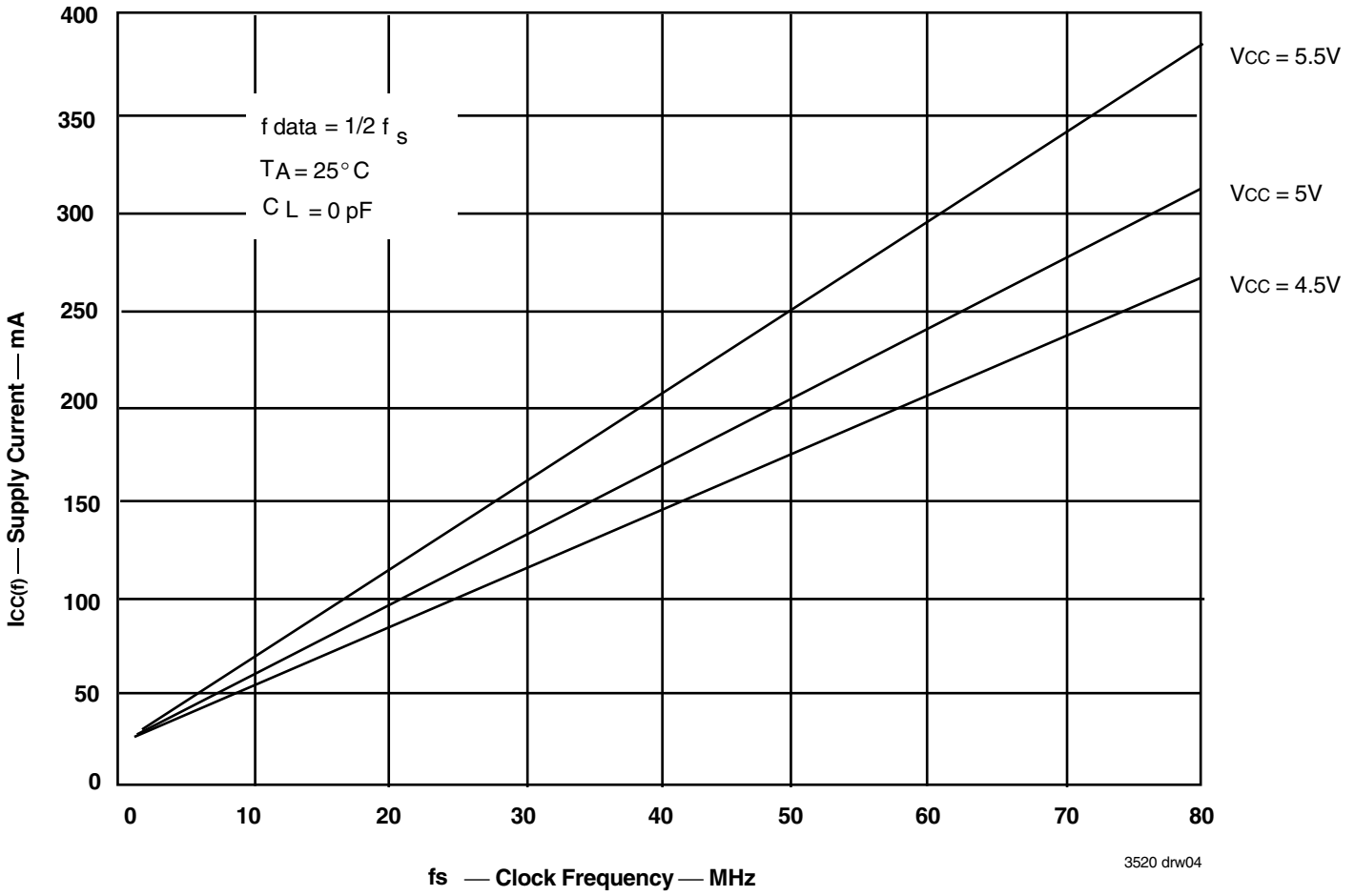


Figure 1. Typical Characteristics: Supply Current vs Clock Frequency

CALCULATING POWER DISSIPATION

The $I_{CC(f)}$ current for the graph in Figure 1 was taken while simultaneously reading and writing the FIFO on the IDT723616 with CLKA and CLKB set to fs. All data inputs and data outputs change state during each clock cycle to consume the highest supply current. Data outputs were disconnected to normalize the graph to a zero-capacitance load. Once the capacitive lead per data-output channel is known, the power dissipation can be calculated with the equation below.

With $I_{CC(f)}$ taken from Figure 1, the maximum power dissipation (P_T) of the IDT723616 can be calculated by:

$$P_T = V_{CC} \times I_{CC(f)} + \Sigma(C_L \times V_{OH}^2 \times f_o)$$

where:

C_L = output capacitance load
f_o = switching frequency of an output
V_{OH} = output high level voltage

When no reads or writes are occurring on the IDT723616, the power dissipated by a single clock (CLKA or CLKB) input running at frequency fs is calculated by:

$$P_T = V_{CC} \times f_S \times 0.290\ mA/MHz$$

© 2019 Renesas Electronics Corporation

SWITCHING CHARACTERISTICS OVER RECOMMENDED RANGES OF SUPPLY VOLTAGE AND OPERATING FREE-AIR TEMPERATURE

(Commercial: V_{CC} = 5.0V ±10%, T_A = 0°C to +70°C; Industrial; V_{CC} = 5.0V ± 10%, T_A = 40°C to +85°C)

Symbol	Parameter	Commercial IDT723616L15 Min.	Commercial IDT723616L15 Max.	Com'l & Ind'l[1] IDT723616L20 Min.	Com'l & Ind'l[1] IDT723616L20 Max.	Unit
f_S	Clock Frequency, CLKA, CLKB, or CLKC	–	66.7	–	50	MHz
t_{CLK}	Clock Cycle Time, CLKA, CLKB, or CLKC	15	–	20	–	ns
t_{CLKH}	Pulse Duration, CLKA, CLKB, and CLKC	6	–	8	–	ns
t_{CLKL}	Pulse Duration, CLKA, CLKB, and CLKC	6	–	8	–	ns
t_{DS}	Setup Time, A0-A35 before CLKA↑ and C0-C17 before CLKC↑	4	–	5	–	ns
t_{ENS}	Setup Time, $\overline{CSA}$, W/$\overline{RA}$, and ENA before CLKA↑; RENB before CLKB↑; WENC before CLKC↑	5	–	5	–	ns
t_{SZS}	Setup Time, SIZ0 and SIZ1 before CLKB↑ and CLKC↑	4	–	5	–	ns
t_{SWS}	Setup Time, SWB0 and SWB1 before CLKB↑, SWCO and SWC1, before CLKC↑	5	–	7	–	ns
t_{PGS}	Setup Time, ODD/$\overline{EVEN}$ and PGA before CLKA↑; ODD/$\overline{EVEN}$ and PGB before CLKB↑[2]	4	–	5	–	ns
t_{RSTS}	Setup Time, $\overline{RST}$ LOW before CLKA↑, CLKB↑, or CLKC↑[3]	5	–	6	–	ns
t_{FSS}	Setup Time, FS0 and FS1 before $\overline{RST}$ HIGH	5	–	6	–	ns
t_{DH}	Hold Time, A0-A35 after CLKA↑ and C0-C17 after CLKC↑	1	–	1	–	ns
t_{ENH}	Hold Time, $\overline{CSA}$, W/$\overline{RA}$, and ENA after CLKA↑; RENB after CLKB↑; WENB after CLKC↑	1	–	1	–	ns
t_{SZH}	Hold Time, SIZ0 and SIZ1 after CLKB↑ and CLKC↑	2	–	2	–	ns
t_{SWH}	Hold Time, SWB0 and SWB1 after CLKB↑, SWC0 and SWC1 after CLKC↑	0	–	0	–	ns
t_{PGH}	Hold Time, ODD/$\overline{EVEN}$ and PGA after CLKA↑; ODD/$\overline{EVEN}$ and PGB after CLKB↑[2]	0	–	0	–	ns
t_{RSTH}	Hold Time, $\overline{RST}$ LOW after CLKA↑, CLKB↑ or CLKC↑[2]	5	–	6	–	ns
t_{FSH}	Hold Time, FS0 and FS1 after $\overline{RST}$ HIGH	4	–	4	–	ns
t_{SKEW1}[4]	Skew Time, between CLKA↑ and CLKB↑ for $\overline{EFB}$ and $\overline{FFA}$; between CLKC↑ and CLKA↑ for $\overline{EFA}$ and $\overline{FFC}$	8	–	8	–	ns
t_{SKEW2}[4]	Skew Time, between CLKA↑ and CLKB↑ for $\overline{AEB}$ and $\overline{AFA}$; between CLKC↑ and CLKA↑ for $\overline{AEA}$ and $\overline{AFC}$	14	–	16	–	ns

NOTES:
1. Industrial temperature range product for 20ns speed grade is available as a standard device. All other speed grades are available by special order.
2. Only applies for a clock edge that does a FIFO read.
3. Requirement to count the clock edge as one of at least four needed to reset a FIFO.
4. Skew time is not a timing constraint for proper device operation and is only included to illustrate the timing relationships among CLKA cycle, CLKB cycle and CLKC.

© 2019 Renesas Electronics Corporation

SWITCHING CHARACTERISTICS OVER RECOMMENDED RANGES OF SUPPLY VOLTAGE AND OPERATING FREE-AIR TEMPERATURE, CL = 30pF

(Commercial: V_{CC} = 5.0V ±10%, T_A = 0°C to +70°C; Industrial; V_{CC} = 5.0V ± 10%, T_A = 40°C to +85°C)

Symbol	Parameter	Commercial IDT723616L15 Min.	Commercial IDT723616L15 Max.	Com'l & Ind'l[1] IDT723616L20 Min.	Com'l & Ind'l[1] IDT723616L20 Max.	Unit
t_A	Access Time, CLKA↑ to A0-A35 and CLKB↑ to B0-B17	2	10	2	12	ns
t_{WFF}	Propagation Delay Time, CLKA↑ to $\overline{FFA}$ and CLKC↑ to $\overline{FFC}$	2	10	2	12	ns
t_{REF}	Propagation Delay Time, CLKA↑ to $\overline{EFA}$ and CLKB↑ to $\overline{EFB}$	2	10	2	12	ns
t_{PAE}	Propagation Delay Time, CLKA↑ to $\overline{AEA}$ and CLKB↑ to $\overline{AEB}$	2	10	2	12	ns
t_{PAF}	Propagation Delay Time, CLKA↑ to $\overline{AFA}$ and CLKC↑ to $\overline{AFC}$	2	10	2	12	ns
t_{PPE}[2]	Propagation delay time, CLKB↑ to $\overline{PEFB}$	2	10	2	12	ns
t_{PDPE}	Propagation Delay Time, A0-A35 valid to $\overline{PEFA}$ valid; C0-C17 valid to $\overline{PEFC}$ valid	2	10	2	11	ns
t_{POPE}	Propagation Delay Time, ODD/$\overline{EVEN}$ to $\overline{PEFA}$ and $\overline{PEFC}$	2	10	2	12	ns
t_{PEPE}	Propagation Delay Time, W/$\overline{R}$A or PGA to $\overline{PEFA}$	1	10	1	12	ns
t_{EN}	Enable Time, $\overline{CSA}$ and W/$\overline{R}$A LOW to A0-A35 active and RENB HIGH to B0-B17 active	2	10	2	12	ns
t_{DIS}	Disable Time, $\overline{CSA}$ or W/$\overline{R}$A HIGH to A0-A35 at high-impedance and RENB LOW to B0-B17 at high-impedance	1	8	1	9	ns

NOTE:
1. Industrial temperature range product for 20ns speed grade is available as a standard device. All other speed grades are available by special order.
2. Only applies when a new port B bus size is implemented by the rising CLKB edge.

© 2019 Renesas Electronics Corporation

SIGNAL DESCRIPTIONS

RESET

The IDT723616 is reset by taking the reset ($\overline{RST}$) input LOW for at least four Port A clock (CLKA), four Port B clock (CLKB) and four Port C clock (CLKC) LOW-to-HIGH transitions. The reset input can switch asynchronously to the clocks. A device reset initializes the internal read and write pointers of each FIFO and forces the full flags ($\overline{FFA}$, $\overline{FFC}$) LOW, the empty flags ($\overline{EFA}$, $\overline{EFB}$) LOW, the Almost-Empty flags ($\overline{AEA}$, $\overline{AEB}$) LOW and the Almost-Full flags ($\overline{AFA}$, $\overline{AFC}$) HIGH. After a reset, $\overline{FFA}$ is set HIGH after two LOW-to-HIGH transitions of CLKA and FFC is set HIGH after two LOW-to-HIGH transitions of CLKC. The device must be reset after power up before data is written to its memory.

A LOW-to-HIGH transition on the $\overline{RST}$ input loads the Almost-Full and Almost-Empty Offset register (X) with the values selected by the flag-select (FS0, FS1) inputs. The values that can be loaded into the registers are shown in Table 1.

TABLE 1 — FLAG PROGRAMMING

FS1	FS0	$\overline{RST}$	ALMOST-FULL AND ALMOST-EMPTY FLAG OFFSET REGISTER (X)
H	H	↑	16
H	L	↑	12
L	H	↑	8
L	L	↑	4

FIFO WRITE/READ OPERATION

The state of Port A data A0-A35 outputs is controlled by the Port A chip select ($\overline{CSA}$) and the Port A write/read select (W/$\overline{RA}$). The A0-A35 outputs are in the high-impedance state when either $\overline{CSA}$ or W/$\overline{RA}$ is HIGH. The A0-A35 outputs are active when both CSA and W/$\overline{RA}$ are LOW. Data is loaded into FIFO1 from the A0-A35 inputs on a LOW-to-HIGH transition of CLKA when $\overline{CSA}$ is LOW, W/$\overline{RA}$ is HIGH, ENA is HIGH, and $\overline{FFA}$ is HIGH. Data is read from FIFO2 to the A0-A35 outputs by a LOW-to-HIGH transition of CLKA when CSA is LOW, W/$\overline{RA}$ is LOW, ENA is HIGH, and EFA is HIGH (see Table 2).

The state of the Port B data (B0-B17) outputs is controlled by Port B read select (RENB). The B0-B17 outputs are in the high-impedance state when REN is LOW. The B0-B17 outputs are active when REN IS HIGH. Data is read from FIFO1 to the B0-B17 outputs by a LOW-to-HIGH transition of CLKB when RENB is HIGH, $\overline{EFB}$ is HIGH, and either SIZ0 or SIZ1 is LOW (see Table 3).

Data is loaded into FIFO2 from the C0-C17 inputs on a LOW-to-HIGH transition of CLKC when WENC is HIGH, $\overline{FFC}$ is HIGH, and either SIZ0 or SIZ1 is LOW (see Table 4).

The setup and hold time constraints to the Port Clocks for the Port A chip select (CSA) and write/read selects (W/$\overline{RA}$, RENB, WENC) are only for enabling write and read operations and are not related to high-impedance control of the data outputs. If a port enable is LOW during a clock cycle, the Port Chip select (for Port A) and write/read select (for all ports) can change states during the setup and hold time window of the cycle.

TABLE 2 — PORT-A ENABLE FUNCTION TABLE

$\overline{CSA}$	W/$\overline{RA}$	ENA	CLKA	A0-A35 Outputs	Port Functions
H	X	X	X	In High-Impedance State	None
L	H	L	X	In High-Impedance State	None
L	H	H	↑	In High-Impedance State	FIFO1 Write
L	L	L	X	Active, FIFO2 Output Register	None
L	L	H	↑	Active, FIFO2 Output Register	FIFO2 Read

TABLE 3 — PORT-B ENABLE FUNCTION TABLE

RENB	SIZ1, SIZ0	CLKB	B0-B17 Outputs	Port Functions
L	X	X	In High-Impedance State	None
H	One or the other LOW(1)	↑	Active, FIFO1 Output Register	FIFO1 read

NOTE:
1. At no time during the operation of the FIFO is it permissible to apply a LOW logic level simultaneously to both SIZ0 and SIZ1, nor is it permissible to apply a HIGH logic level simultaneously to both these inputs. These state combinations are reserved.

TABLE 4 — PORT-C ENABLE FUNCTION TABLE

WENC	SIZ1, SIZ0	CLKC	C0-C17 Inputs	Port Functions
L	X	X	In High-Impedance State	None
H	One or the other LOW(1)	↑	In High-Impedance State	FIFO2 write

NOTE:
1. At no time during the operation of the FIFO is it permissible to apply a LOW logic level simultaneously to both SIZ0 and SIZ1, nor is it permissible to apply a HIGH logic level simultaneously to both these inputs. These state combinations are reserved.

© 2019 Renesas Electronics Corporation

SYNCHRONIZED FIFO FLAGS

Each FIFO is synchronized to its Port Clock through two flip-flop stages. This is done to improve flag reliability by reducing the probability of metastable events on the output when CLKA operates asynchronously relative to CLKB or CLKC. $\overline{EFA}$, $\overline{AEA}$, $\overline{FFA}$, and $\overline{AFA}$ are synchronized to CLKA. $\overline{EFB}$ and $\overline{AEB}$ are synchronized to CLKB. $\overline{FFC}$ and $\overline{AFC}$ are synchronized to CLKC. Tables 5 and 6 show the relationship of each port flag to FIFO1 and FIFO2.

EMPTY FLAGS ($\overline{EFA}$, $\overline{EFB}$)

The empty flag of a FIFO is synchronized to the Port Clock that reads data from its array. When the empty flag is HIGH, new data can be read to the FIFO output register. When the empty flag is LOW, the FIFO is empty and attempted FIFO reads are ignored. When reading FIFO1 with a byte or word size on Port B, $\overline{EFB}$ is set LOW when the fourth byte or second word of the last long word is read.

The read pointer of a FIFO is incremented each time a new word is clocked to the output register. The state machine that controls an empty flag monitors a write-pointer and read-pointer comparator that indicates when the FIFO SRAM status is empty, empty+1, or empty+2. A word written to a FIFO can be read to the FIFO output register in a minimum of three cycles of the empty flag synchronizing clock. Therefore, an empty flag is LOW if a word in memory is the next data to be sent to the FIFO output register and two cycles of the Port Clock that reads data from the FIFO have not elapsed since the time the word was written. The empty flag of the FIFO is set HIGH by the second LOW-to-HIGH transition of the synchronizing clock, and the new data word can be read to the FIFO output register in the following cycle.

A LOW-to-HIGH transition on an empty flag synchronizing clock begins the first synchronization cycle of a write if the clock transition occurs at time t_{SKEW1} or greater after the write. Otherwise, the subsequent clock cycle can be the first synchronization cycle (see Figure 12 and 13).

FULL FLAG ($\overline{FFA}$, $\overline{FFC}$)

The full flag of a FIFO is synchronized to the Port Clock that writes data to its array. When the full flag is HIGH, a memory location is free in the SRAM to receive new data. No memory locations are free when the full flag is LOW and attempted writes to the FIFO are ignored.

Each time a word is written to a FIFO, the write pointer is incremented. The state machine that controls a full flag monitors a write-pointer and read-pointer comparator that indicates when the FIFO SRAM status is full, full-1, or full-2. From the time a word is read from a FIFO, the previous memory location is ready to be written in a minimum of three cycles of the full flag synchronizing clock. Therefore, a full flag is LOW if less than two cycles of the full flag synchronizing clock have elapsed since the next memory write location has been read. The second LOW-to-HIGH transition on the full flag synchronization clock after the read sets the full flag HIGH and the data can be written in the following clock cycle.

A LOW-to-HIGH transition on a full flag synchronizing clock begins the first synchronization cycle of a read if the clock transition occurs at time t_{SKEW1} or greater after the read. Otherwise, the subsequent clock cycle can be the first synchronization cycle (see Figure 14 and 15).

ALMOST-EMPTY FLAGS ($\overline{AEA}$, $\overline{AEB}$)

The Almost-Empty flag of a FIFO is synchronized to the Port Clock that reads data from its array. The state machine that controls an Almost-Empty flag monitors a write-pointer and a read-pointer comparator that indicates when the FIFO SRAM status is almost-empty, almost-empty+1, or almost-empty+2. The almost-empty state is defined by the value of the Almost-Full and Almost-Empty Offset register (X). This register is loaded with one of four preset values during a device reset (see Reset above). An Almost-Empty flag is LOW when the FIFO contains X or less long words in memory and is HIGH when the FIFO contains (X+1) or more long words.

Two LOW-to-HIGH transitions of the Almost-Empty flag synchronizing clock are required after a FIFO write for the Almost-Empty flag to reflect the new level of fill. Therefore, the Almost-Empty flag of a FIFO containing (X+1) or more long words remains LOW if two cycles of the synchronizing clock have not elapsed since the write that filled the memory to the (X+1) level. An Almost-Empty flag is set HIGH by the second LOW-to-HIGH transition of the synchronizing clock after the FIFO write that fills memory to the (X+1) level. A LOW-to-HIGH transition of an Almost-Empty flag synchronizing clock begins the first synchronization cycle if it occurs at time tSKEW2 or greater after the write that fills the FIFO to (X+1) long words. Otherwise, the subsequent synchronizing clock cycle can be the first synchronization cycle (see Figure 16 and 17).

ALMOST-FULL FLAGS ($\overline{AFA}$, $\overline{AFC}$)

The Almost-Full flag of a FIFO is synchronized to the Port Clock that writes data to its array. The state machine that controls an Almost-Full flag monitors a write-pointer and read-pointer comparator that indicates when the FIFO SRAM status is almost-full, almost-full-1, or almost-full-2. The almost-full state is defined by the value of the Almost-Full and Almost-Empty Offset register (X).

TABLE 5 — FIFO1 FLAG OPERATION

Number of 36-Bit Words in the FIFO1[1]	Synchronized to CLKB		Synchronized to CLKA	
	$\overline{EFB}$	$\overline{AEB}$	$\overline{AFA}$	$\overline{FFA}$
0	L	L	H	H
1 to X	H	L	H	H
(X+1) to [64–(X+1)]	H	H	H	H
(64–X) to 63	H	H	L	H
64	H	H	L	L

TABLE 6 — FIFO2 FLAG OPERATION

Number of 36-Bit Words in the FIFO2[1]	Synchronized to CLKA		Synchronized to CLKC	
	$\overline{EFA}$	$\overline{AEA}$	$\overline{AFC}$	$\overline{FFC}$
0	L	L	H	H
1 to X	H	L	H	H
(X+1) to [64–(X+1)]	H	H	H	H
(64–X) to 63	H	H	L	H
64	H	H	L	L

NOTE:
1. X is the value in the Almost-Empty flag and Almost-Full flag Offset register.

© 2019 Renesas Electronics Corporation

This register is loaded with one of four preset values during a device reset (see Reset above). An Almost-Full flag is LOW when the FIFO contains (64-X) or more long words in memory and is HIGH when the FIFO contains [64-(X+1)] or less long words.

Two LOW-to-HIGH transitions of the Almost-Full flag synchronizing clock are required after a FIFO read for the Almost-Full flag to reflect the new level of fill. Therefore, the Almost-Full flag of a FIFO containing [64-(X+1)] or less words remains LOW if two cycles of the synchronizing clock have not elapsed since the read that reduced the number of long words in memory to [64-(X+1)]. An Almost-Full flag is set HIGH by the second LOW-to-HIGH transition of the synchronizing clock after the FIFO read that reduces the number of long words in memory to [64-(X+1)]. A LOW-to-HIGH transition of an Almost-Full flag synchronizing clock begins the first synchronization cycle if it occurs at time t_{SKEW2} or greater after the read that reduces the number of long words in memory to [64-(X+1)]. Otherwise, the subsequent synchronizing clock cycle can be the first synchronization cycle (see Figure 18 and 19).

BUS SIZING

Both ports B and C, taken together, may be configured for either an 18-bit word or a 9-bit byte format, thus determining the word width of the data read from FIFO1 or written to FIFO2. Whichever bus size is selected applies to both ports B and C. It is not possible to configure the bus width of ports B and C independently.

The levels applied to the bus size select (SIZ0, SIZ1) inputs must be static through out FIFO operation. These levels can only be changed when the FIFO is idle (no read or write activity) just preceding Master Reset operation. The bus size as selected using SIZ0 and SIZ1 is implemented according to Figure 2. Note that neither a HIGH nor a LOW logic level should be applied to both SIZ0 and SIZ1 at the same time; these states are reserved.

Only 36-bit long-word data is written to or read from the two FIFO memories on the IDT723616. Bus-matching operations are done after data is read from the FIFO1 RAM and before data is written to the FIFO2 RAM.

BUS-MATCHING FIFO1 READS

Data is read from the FIFO1 RAM in 36-bit long word increments. Since Port B can only have a byte or word size, only the first one or two bytes appear on the selected portion of the FIFO1 output register, with the rest of the long word stored in auxiliary registers. In this case, subsequent FIFO1 reads with the same bus size implementation output the rest of the long word to the FIFO1 output register in the order shown by Figure 2.

When reading data from FIFO1 in byte format, the unused B0-B17 outputs remain inactive but static, with the unused FIFO1 output register bits holding the last data value to decrease power consumption.

BUS-MATCHING FIFO2 WRITES

Data is written to the FIFO2 RAM in 36-bit long word increments. Data can be written to FIFO2 with a byte or word bus size. This action stores the initial bytes or words in auxiliary registers. The CLKC rising edge that writes the fourth byte or the second word of long word to FIFO2 also stores the entire long word in FIFO2 RAM. The bytes are arranged in the manner shown in Figure 2.

BYTE SWAPPING

The byte-order arrangement of data read from FIFO1 or data written to FIFO2 can be changed synchronous to the rising edge of CLKB. Four modes of byte-order swapping (including no swap) can be done with any data port size selection. The order of the bytes are rearranged within the long word, but the bit order within the bytes remains constant.

The swap configuration can be selected independently for ports B and C. The Port B Swap Select inputs (SWB0 and SWB1) are used to choose the byte arrangement for Port B. The Port C Swap Select inputs (SWC0 and SWC1) are used to choose the byte arrangement for Port C. The levels applied to the swap select must be static throughout FIFO operation. These levels can only be changed when the FIFO is idle (no read or write activity) just preceding Master Reset operation. Figures 3 and 4 are examples of the byte-order swapping operations available for 18-bit words. Performing a byte swap and bus size simultaneously for a FIFO1 read first rearranges the bytes as shown in Figure 3, then outputs the bytes as shown in Figure 2. Simultaneous bus sizing and byte swapping operations for FIFO2 writes first loads the data according to Figure 2, then swaps the bytes as shown in Figure 4 when the long word is loaded to FIFO2 RAM.

PARITY CHECKING

The Port A inputs (A0-A35) have four parity trees to check the parity of incoming (or outgoing) data; the Port B inputs (B0-B17) have two parity trees to check the parity of outgoing data; Port C inputs (C0-C17) have two parity trees to check the parity of incoming data. A parity failure on one or more bytes of the Port A data bus is reported by a LOW level on the port parity error flag ($\overline{PEFA}$). A parity failure on one or more bytes of the Port C data bus that are valid for the bus size implementation is reported by a LOW level on the Port C parity error flag (PEFC). Odd or even parity checking can be selected, and the parity error flags can be ignored if this feature is not desired.

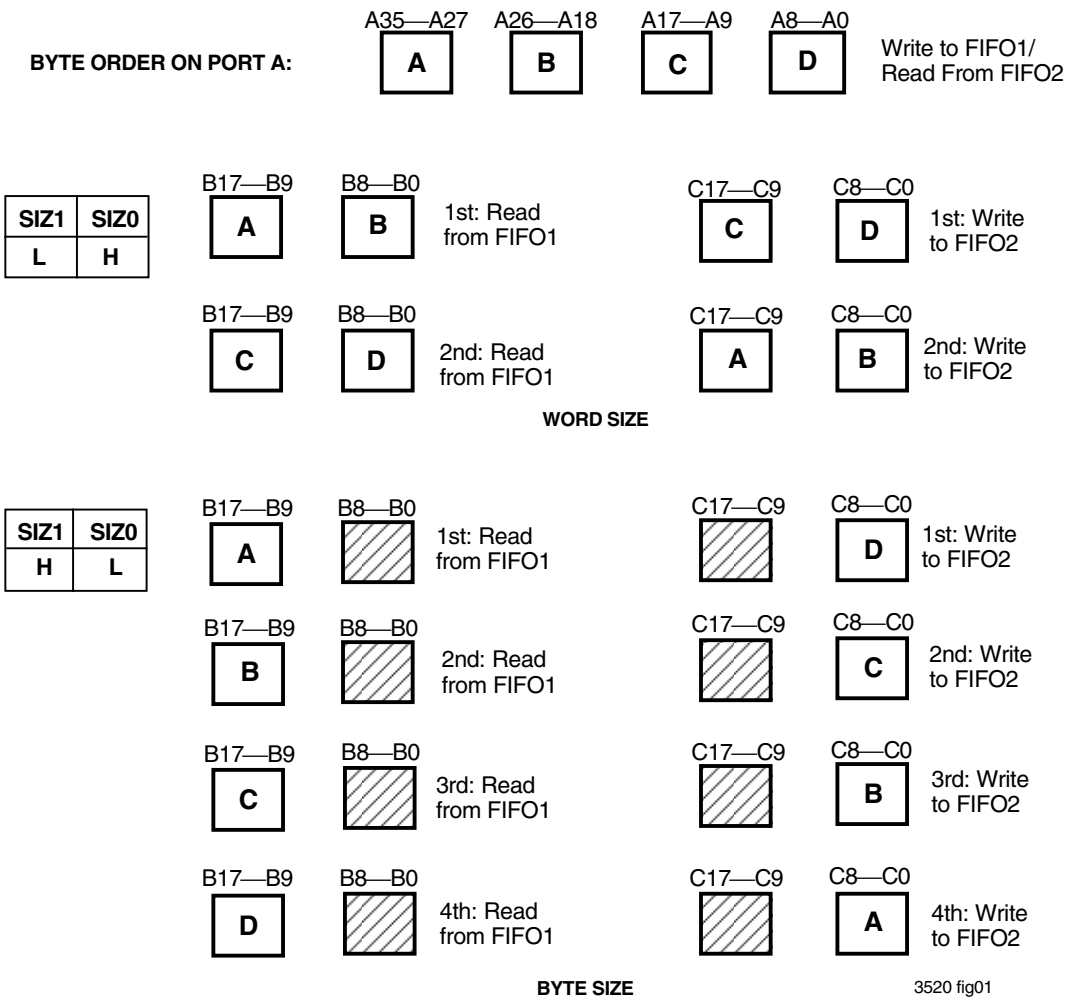
Parity status is checked on each input bus according to the level of the ODD/$\overline{EVEN}$ parity select input. A parity error on one or more valid bytes of a port is reported by a LOW level on the corresponding port parity error flag ($\overline{PEFA}$, $\overline{PEFC}$) output. Port A bytes are arranged as A0-A8, A9-A17, A18-A26, and A27-A35. Port C bytes are arranged as C0-C8 and C9-C17, and its valid bytes are those used in a Port C bus size implementation. When ODD/$\overline{EVEN}$ parity is selected, a port parity error flag ($\overline{PEFA}$, $\overline{PEFC}$) is LOW if any byte on the port has an ODD/EVEN number of LOW levels applied to the bits.

PARITY GENERATION

A HIGH level on the Port A parity generate select (PGA) or Port B parity generate select (PGB) enables the IDT723616 to generate parity bits for port reads from a FIFO. Port A bytes are arranged as A0-A8, A9-A17, A18-26, and A27-A35, with the most significant bit of each byte used as the parity bit. Port B bytes are arranged as B0-B8 and B9-B17, with the most significant bit of each byte used as the parity bit. A write to a FIFO stores the levels applied to all nine inputs of a byte regardless of the state of the parity generate select (PGA, PGB) inputs. When data is read from a port with parity generation selected, the lower eight bits of each byte are used to generate a parity bit according to the level on the ODD/$\overline{EVEN}$ select. The generated parity bits are substituted for the levels originally written to the most significant bits of each byte as the word is read to the data outputs.

Parity bits for FIFO data are generated after the data is read from SRAM and before the data is written to the output register. Therefore, the Port A parity generate select (PGA) and ODD/$\overline{EVEN}$ parity select (ODD/$\overline{EVEN}$) have setup and hold time constraints to the Port A clock (CLKA) and the Port B parity generate select (PGB) and ODD/$\overline{EVEN}$ have setup and hold-time constraints to the Port B clock (CLKB). These timing constraints only apply for a rising clock edge used to read a new long word to the FIFO output register.

© 2019 Renesas Electronics Corporation



NOTE:

1. At no time during the operation of the FIFO is it permissible to apply a LOW logic level simultaneously to both SIZ0 and SIZ1, nor is it permissible to apply a HIGH logic level simultaneously to both these inputs. These state combinations are reserved.

Figure 2. Bus Sizing

© 2019 Renesas Electronics Corporation

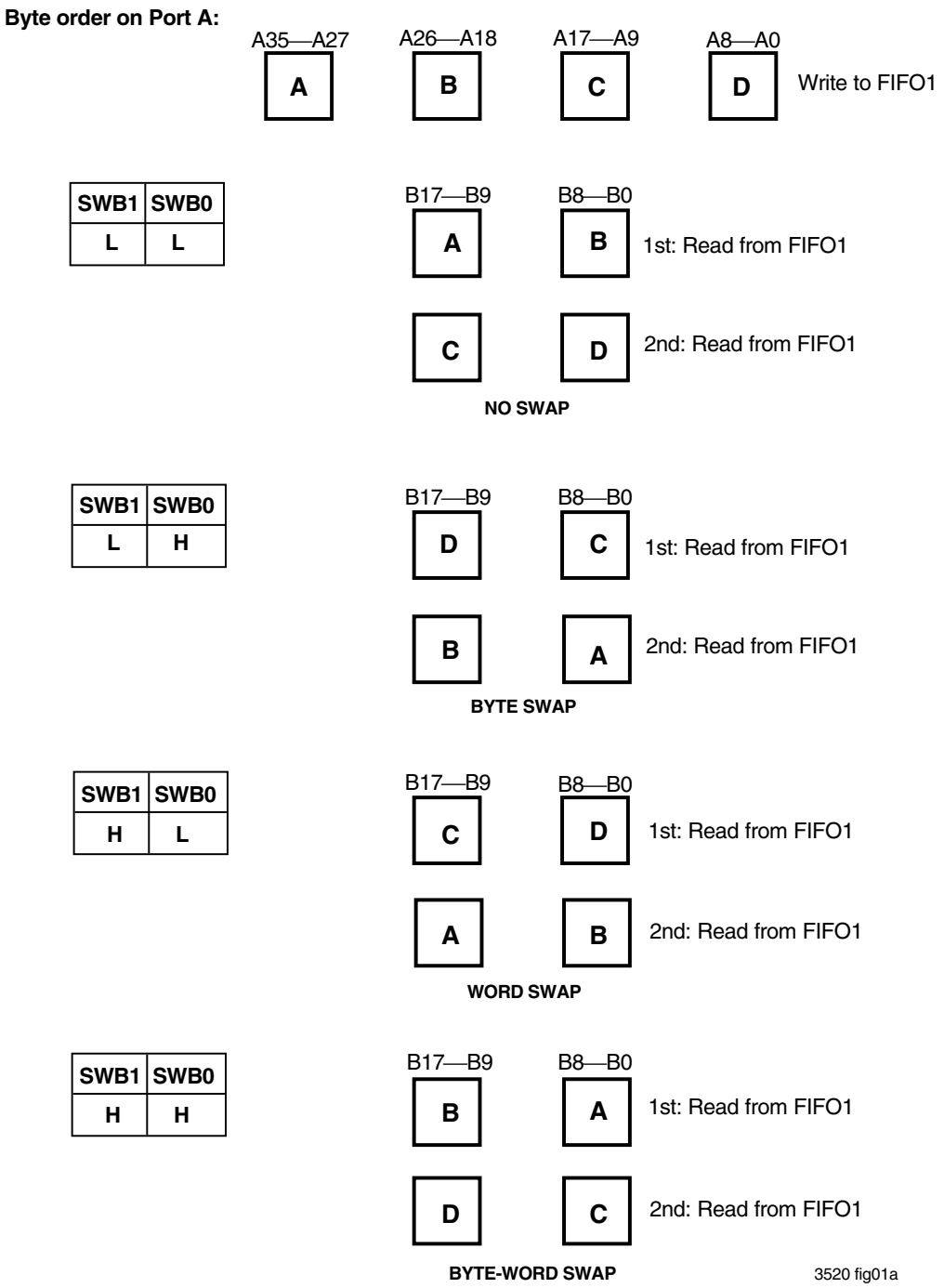


Figure 3. Port B Byte Swapping (Word Size Example)

© 2019 Renesas Electronics Corporation

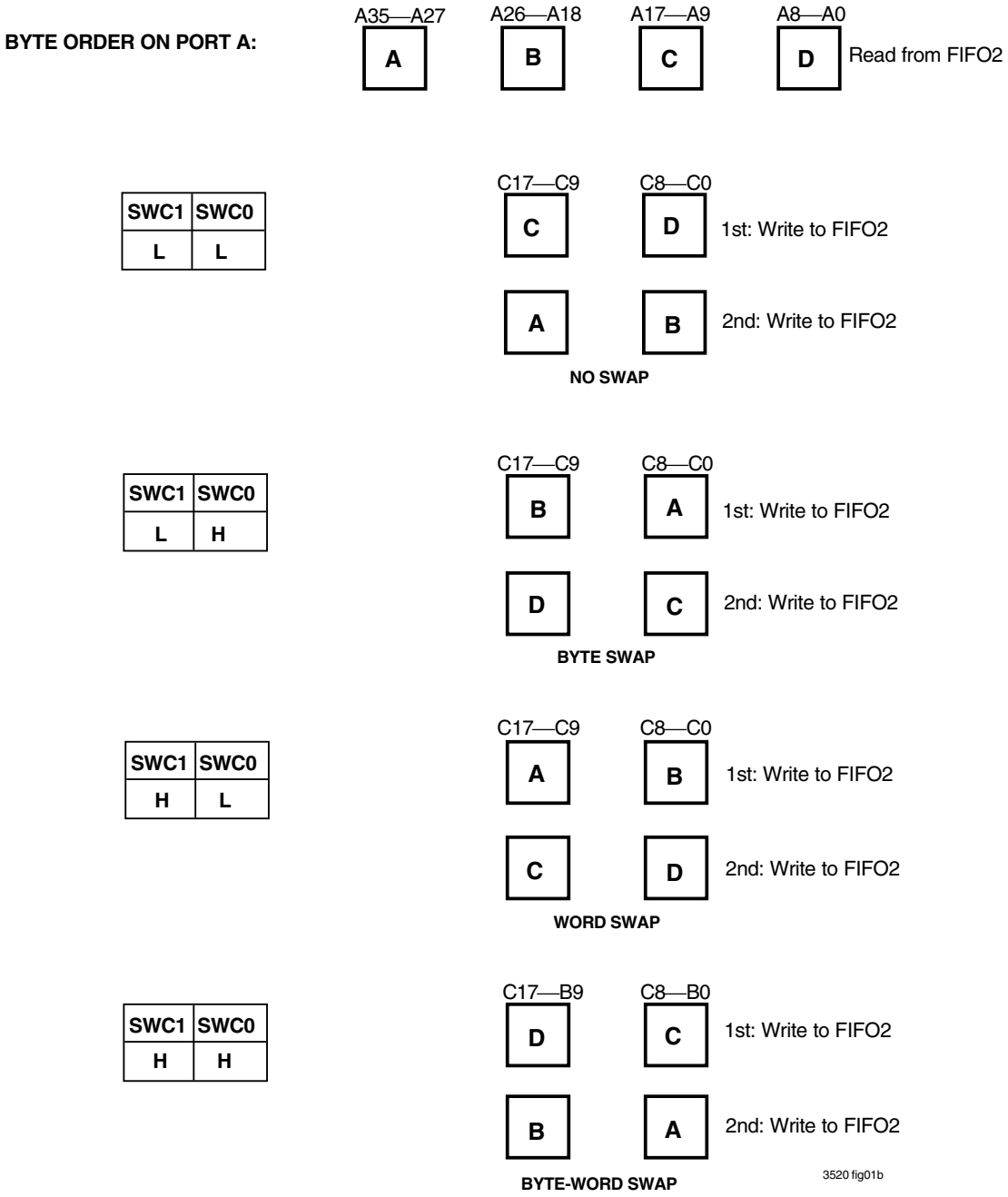


Figure 4. Port C Byte Swapping (Word Size Example)

© 2019 Renesas Electronics Corporation

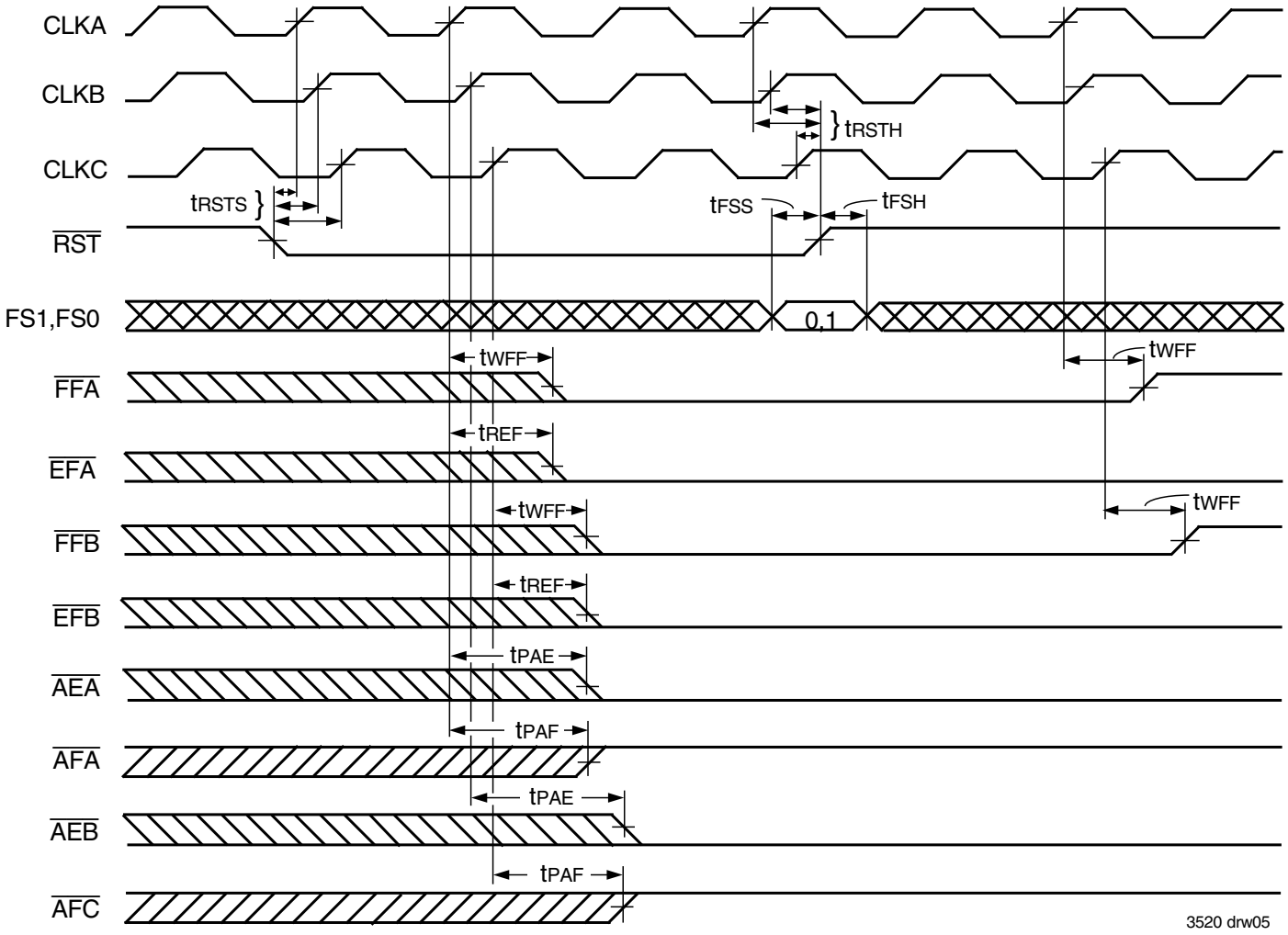
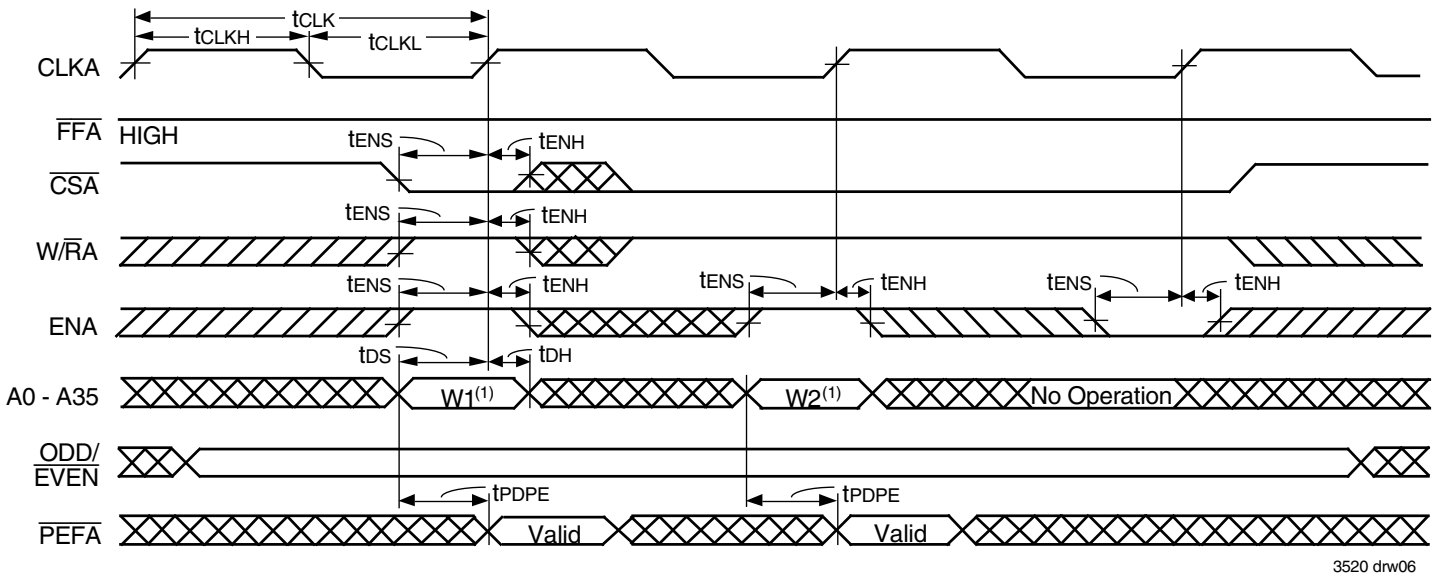


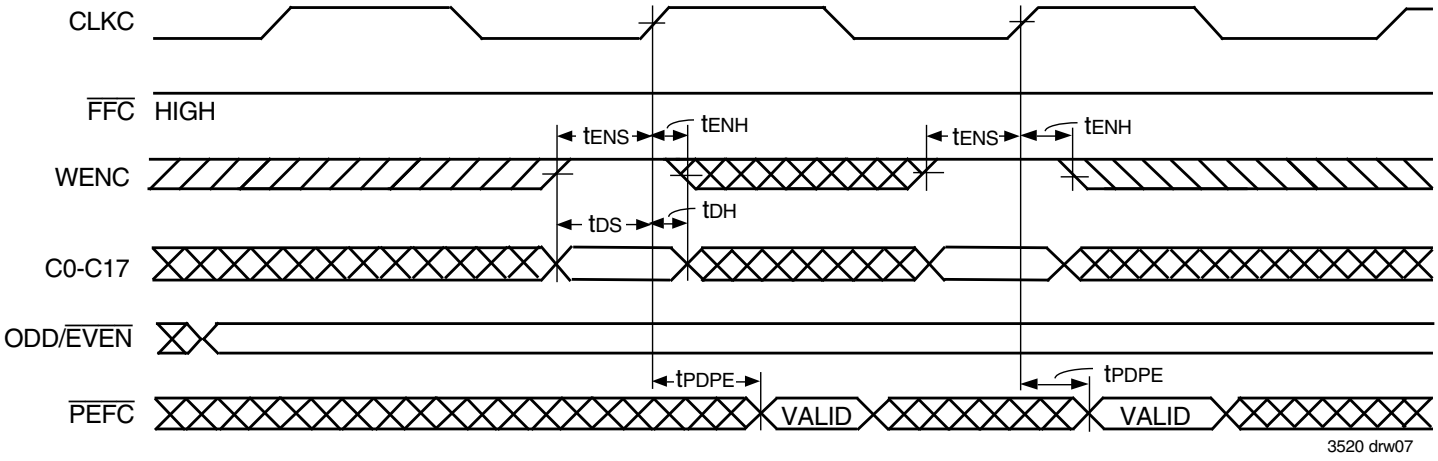
Figure 5. Device Reset Loading the X Register with the Value of Eight



NOTE:
1. Written to FIFO1.

Figure 6. Port-A Write Cycle Timing for FIFO1

© 2019 Renesas Electronics Corporation



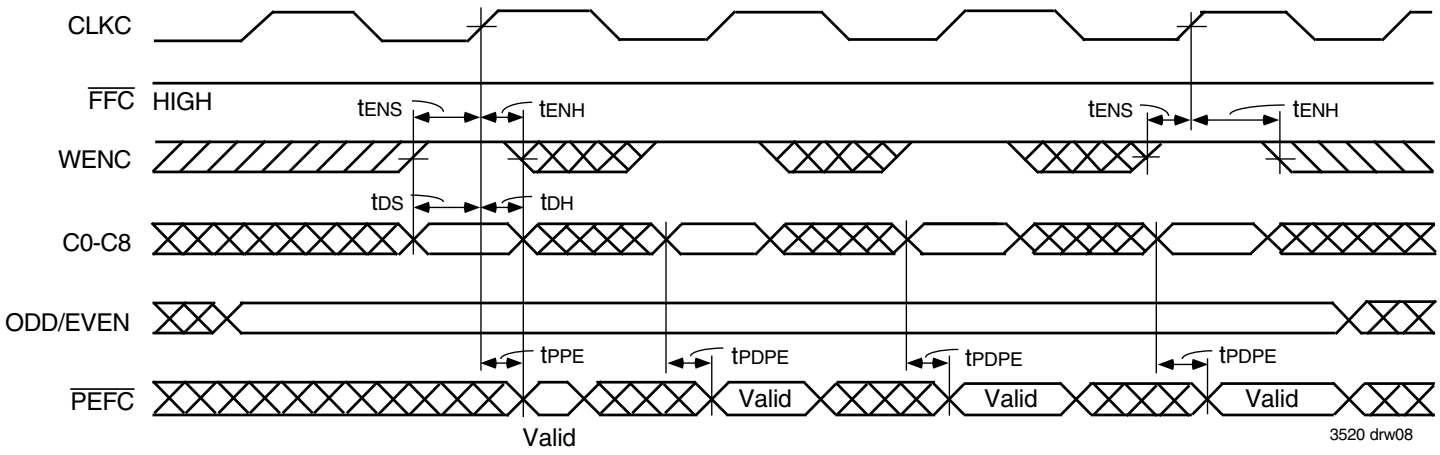
NOTE:
1. PEFC indicates parity error for the following bytes: C17-C9 and C8-C0.

DATA SWAP TABLE FOR WORD WRITES TO FIFO2

SWAP MODE		WRITE NO.	DATA WRITTEN TO FIFO2		DATA READ FROM FIFO2			
SWC1	SWC0		C17-C9	C8-C0	A35-27	A26-A18	A17-A9	A8-A0
L	L	1	C	D	A	B	C	D
		2	A	B				
L	H	1	B	A	A	B	C	D
		2	D	C				
H	L	1	A	B	A	B	C	D
		2	C	D				
H	H	1	D	C	A	B	C	D
		2	B	A				

Figure 7. Port-C Word Write Cycle Timing for FIFO2

© 2019 Renesas Electronics Corporation



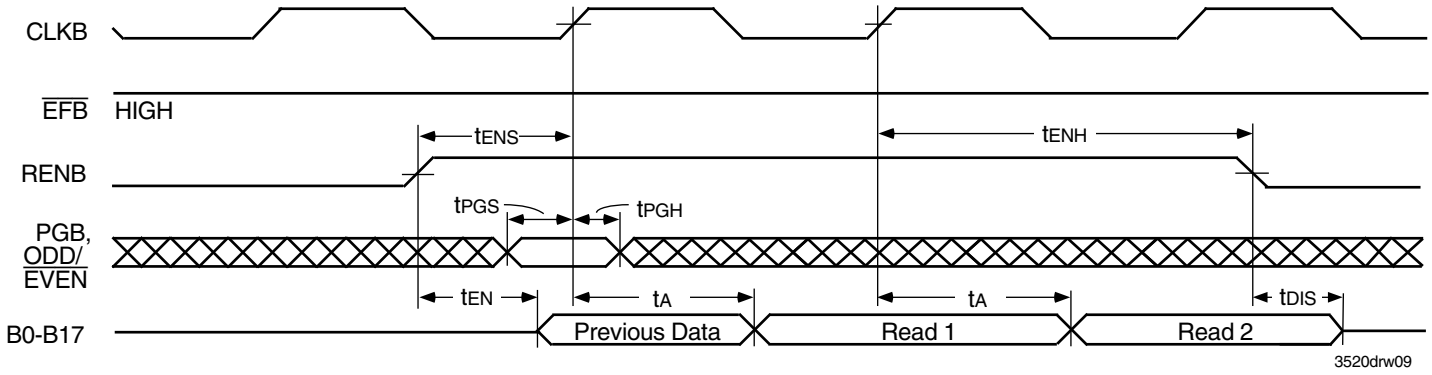
NOTE:
1. $\overline{PEFC}$ indicates parity error for the following byte: C8—C0.

DATA SWAP TABLE FOR BYTE WRITES TO FIFO2

SWAP MODE		WRITE NO.	DATA WRITTEN TO FIFO2		DATA READ FROM FIFO2		
SWC1	**SWC0**		**C8-C0**	**A35-27**	**A26-A18**	**A17-A9**	**A8-A0**
L	L	1	D	A	B	C	D
		2	C				
		3	B				
		4	A				
L	H	1	A	A	B	C	D
		2	B				
		3	C				
		4	D				
H	L	1	B	A	B	C	D
		2	A				
		3	D				
		4	C				
H	H	1	C	A	B	C	D
		2	D				
		3	A				
		4	B				

Figure 8. Port-C Byte Write Cycle Timing for FIFO2

© 2019 Renesas Electronics Corporation

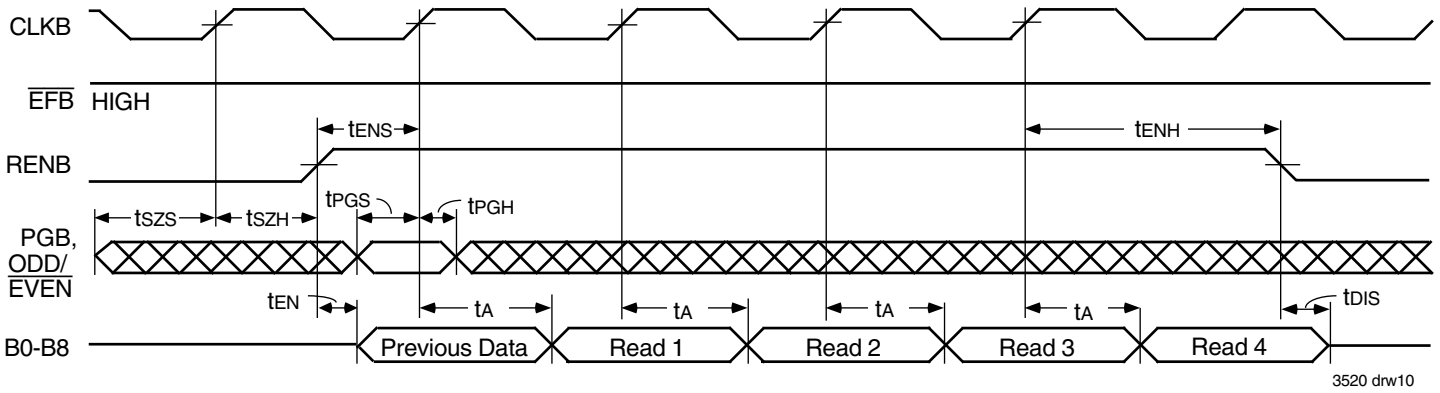


DATA SWAP TABLE FOR WORD READS FROM FIFO1

SWAP MODE		DATA WRITTEN TO FIFO1				READ NO.	DATA READ FROM FIFO1	
SWB1	SWB0	A35-A27	A26-A18	A17-A9	A8-A0		B17-B9	B8-B0
L	L	A	B	C	D	1 2	A C	B D
L	H	A	B	C	D	1 2	D B	C A
H	L	A	B	C	D	1 2	C A	D B
H	H	A	B	C	D	1 2	B D	A C

Figure 9. Port-B Word Read Cycle Timing for FIFO1

© 2019 Renesas Electronics Corporation



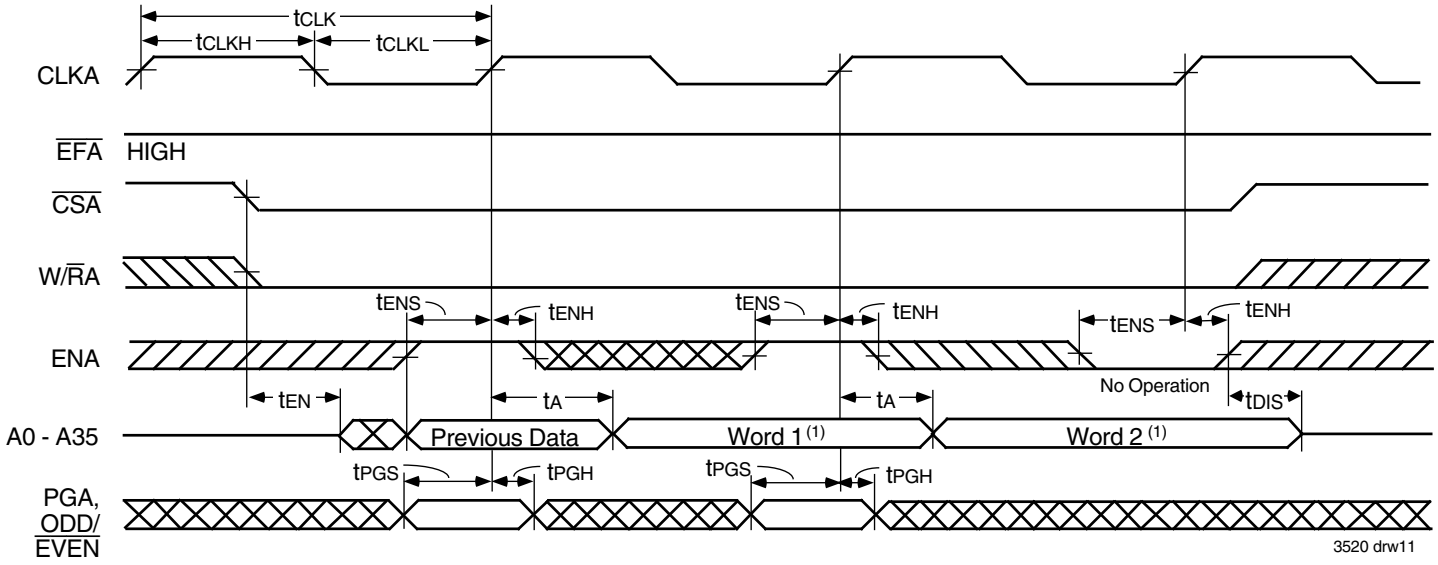
NOTE:
1. Unused bytes hold last FIFO1 output register data for byte-size reads.

DATA SWAP TABLE FOR BYTE READS FROM FIFO1

SWAP MODE		DATA WRITTEN TO FIFO 1				READ NO.	DATA READ FROM FIFO 1
SWB1	SWB0	A35-A27	A26-A18	A17-A9	A8-A0		B17-B9
L	L	A	B	C	D	1 2 3 4	A B C D
L	H	A	B	C	D	1 2 3 4	D C B A
H	L	A	B	C	D	1 2 3 4	C D A B
H	H	A	B	C	D	1 2 3 4	B A D C

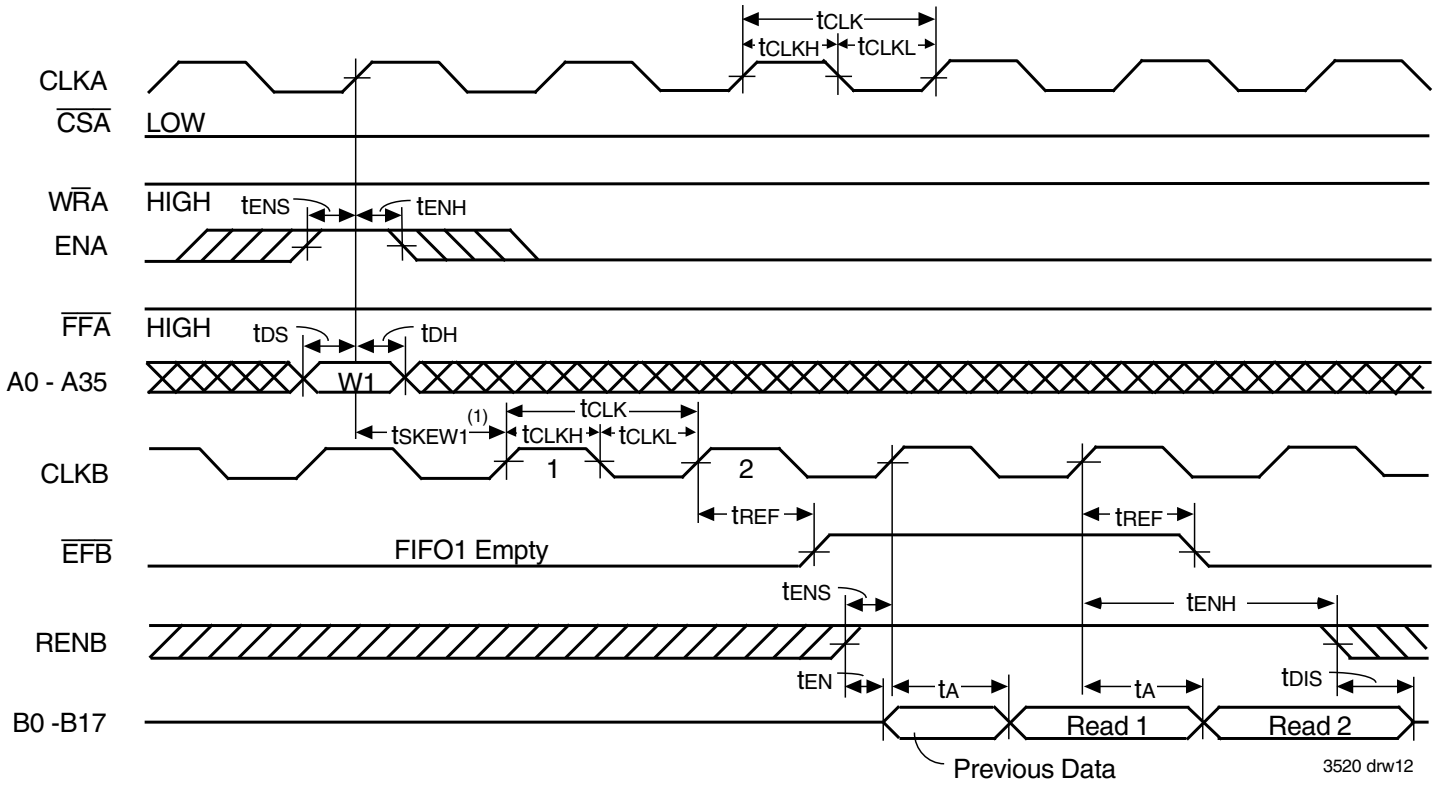
Figure 10. Port-B Byte Read Cycle Timing for FIFO1

© 2019 Renesas Electronics Corporation



NOTE:
1. Read from FIFO2.

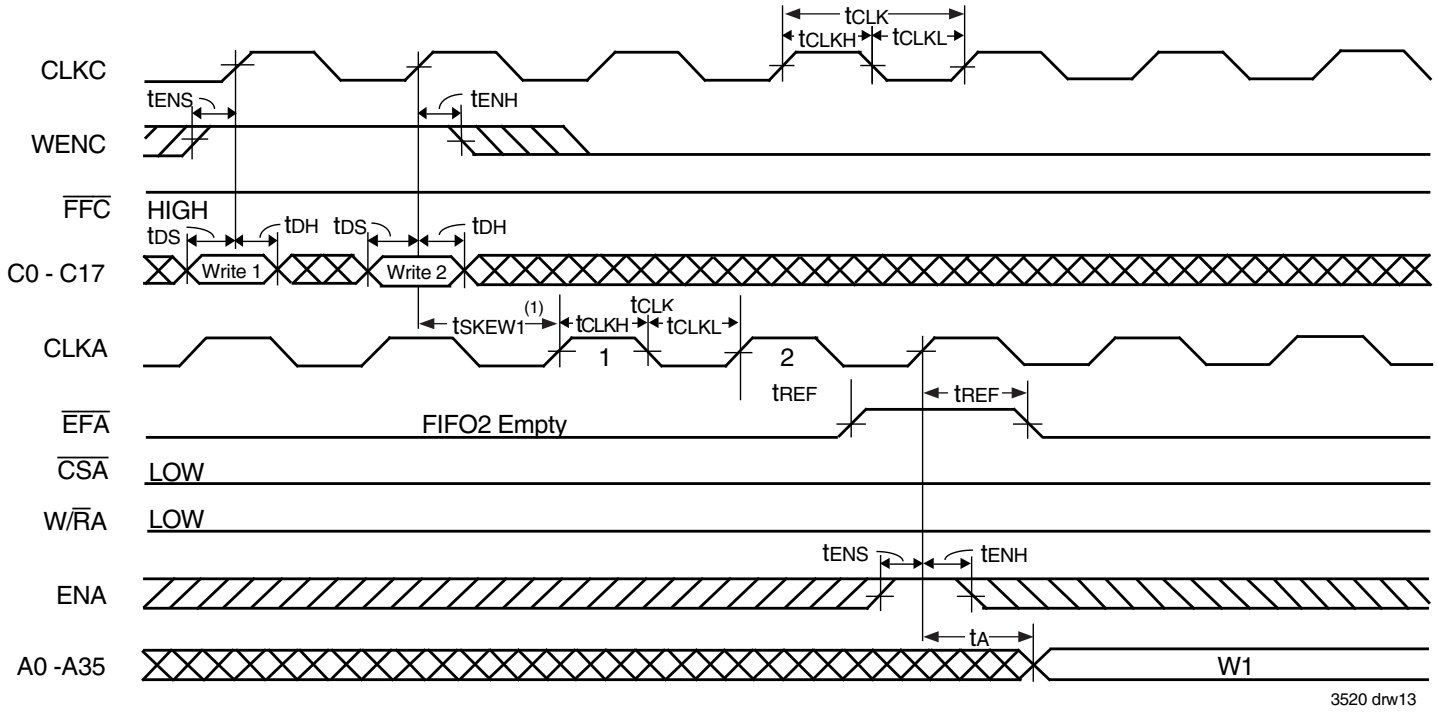
Figure 11. Port-A Read Cycle Timing for FIFO2



NOTES:
1. t_{SKEW1} is the minimum time between a rising CLKA edge and a rising CLKB edge for $\overline{EFB}$ to transition HIGH in the next CLKB cycle. If the time between the rising CLKA edge and rising CLKB edge is less than t_{SKEW1}, then the transition of $\overline{EFB}$ HIGH may occur one CLKB cycle later than shown.
2. Port-B size is word or byte; $\overline{EFB}$ is set LOW by the last word or byte read from FIFO1, respectively. (The word-size case is shown.)

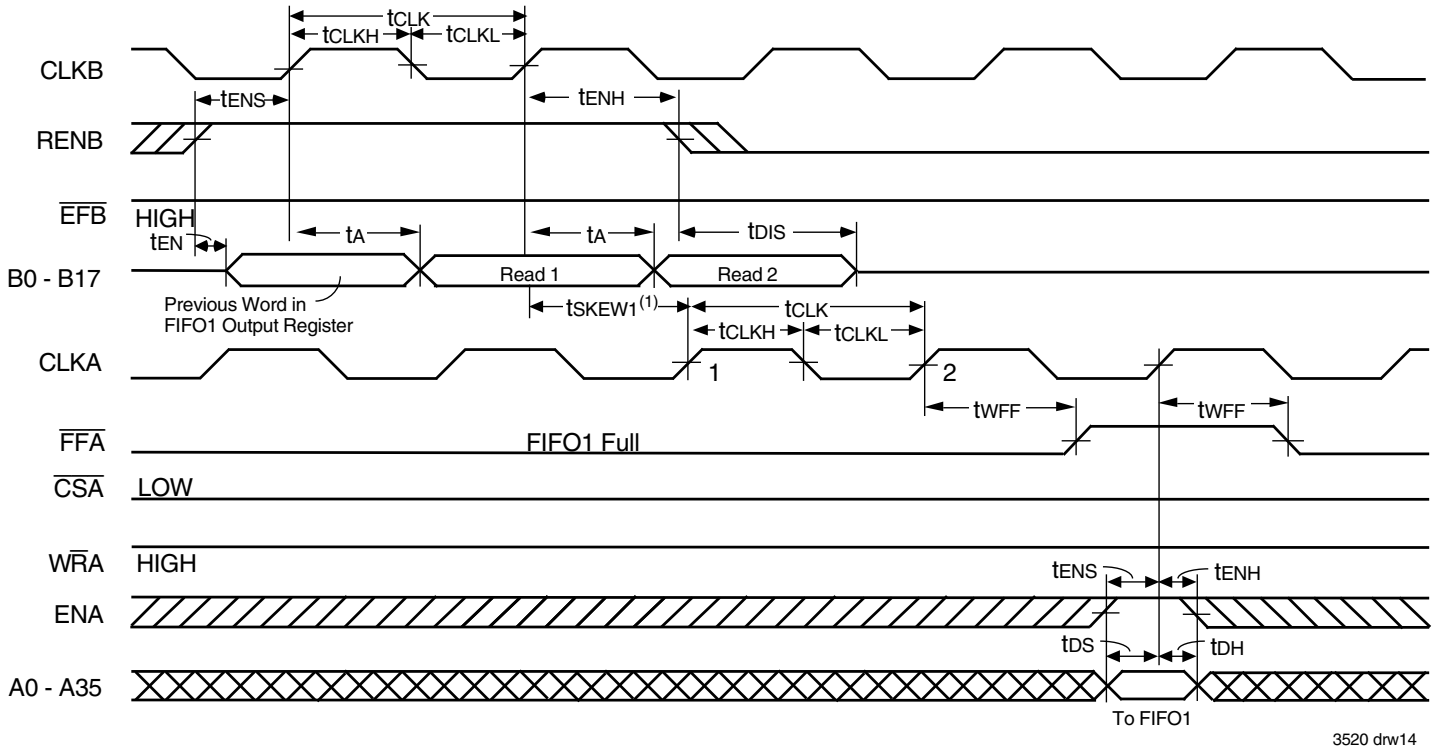
Figure 12. $\overline{EFB}$ Flag Timing and First Data Read when FIFO1 is Empty

© 2019 Renesas Electronics Corporation



NOTES:
1. t_{SKEW1} is the minimum time between a rising CLKC edge and a rising CLKA edge for $\overline{EFA}$ to transition HIGH in the next CLKA cycle. If the time between the rising CLKC edge and rising CLKA edge is less than t_{SKEW1}, then the transition of EFA HIGH may occur one CLKA cycle later than shown.
2. Port-C size is word or byte; t_{SKEW1} is referenced to the rising CLKC edge that writes the last word or byte of the long word, respectively. (The word-size case is shown.)

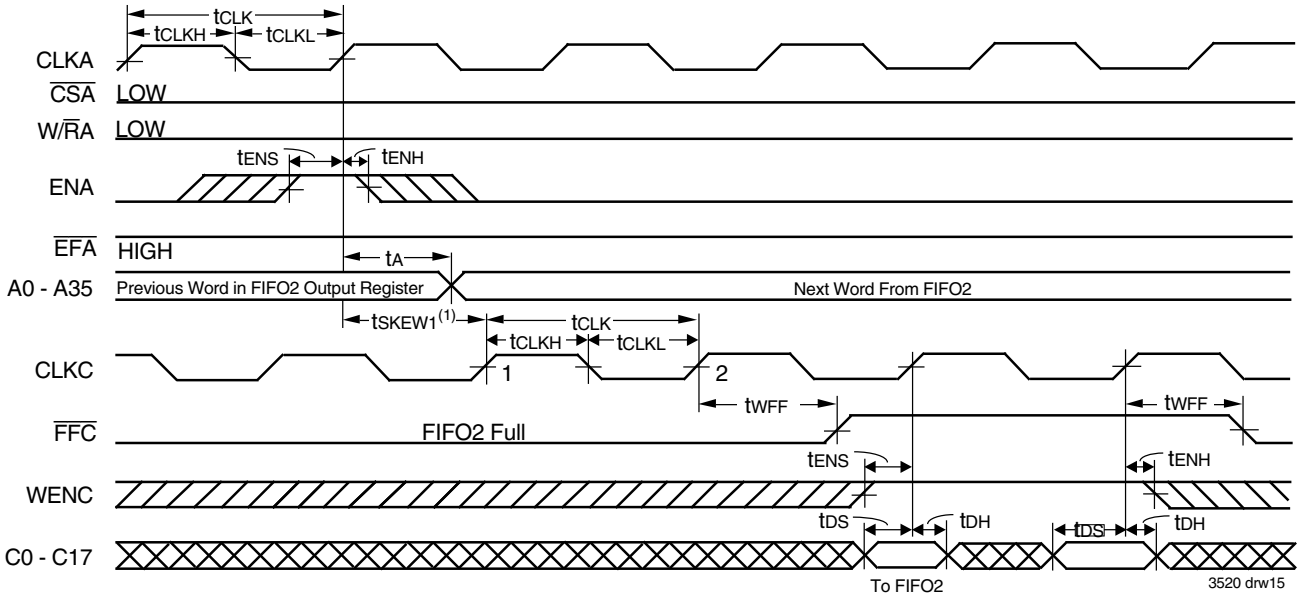
Figure 13. $\overline{EFA}$ Flag Timing and First Data Read when FIFO2 is Empty



NOTES:
1. t_{SKEW1} is the minimum time between a rising CLKB edge and a rising CLKA edge for $\overline{FFA}$ to transition HIGH in the next CLKA cycle. If the time between the rising CLKB edge and rising CLKA edge is less than t_{SKEW1}, then $\overline{FFA}$ may transition HIGH one CLKA cycle later than shown.
2. Port-B size is word or byte; t_{SKEW1} is referenced from the rising CLKB edge that reads the last word or byte of the long word, respectively. (The word-size case is shown.)

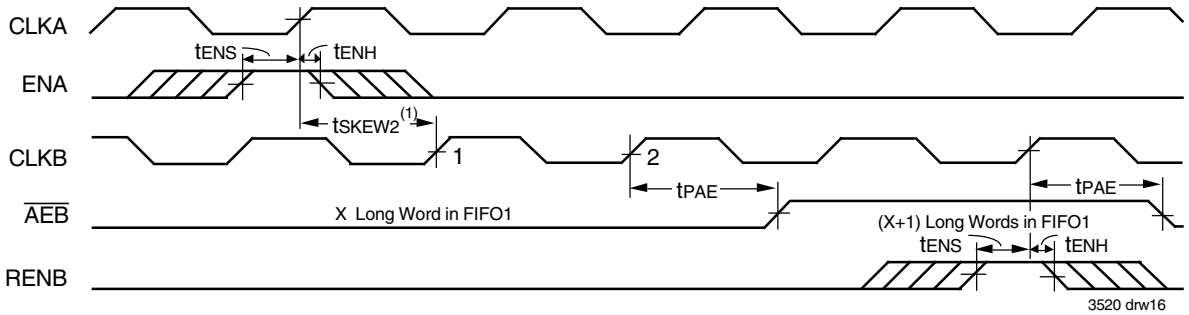
Figure 14. $\overline{FFA}$ Flag Timing and First Available Write when FIFO1 is Full

© 2019 Renesas Electronics Corporation



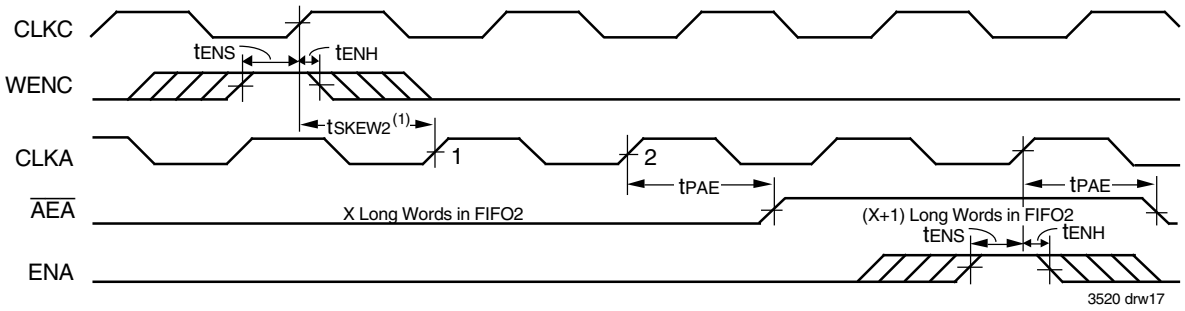
NOTES:
1. tSKEW1 is the minimum time between a rising CLKA edge and a rising CLKB edge for $\overline{FFB}$ to transition HIGH in the next CLKB cycle. If the time between the rising CLKA edge and rising CLKB edge is less than tSKEW1, then $\overline{FFB}$ may transition HIGH one CLKB cycle later than shown.
2. Port-C size is word or byte; $\overline{FFC}$ is set LOW by the last word or byte write of the long word, respectively. (The word-size case is shown.)

Figure 15. $\overline{FFC}$ Flag Timing and First Available Write when FIFO2 is Full



NOTES:
1. tSKEW2 is the minimum time between a rising CLKA edge and a rising CLKB edge for $\overline{AEB}$ to transition HIGH in the next CLKB cycle. If the time between the rising CLKA edge and rising CLKB edge is less than tSKEW2, then $\overline{AEB}$ may transition HIGH one CLKB cycle later than shown.
2. FIFO1 Write ($\overline{CSA}$ = LOW, W/$\overline{RA}$ = HIGH).
3. Port-B size is word or byte; $\overline{AEB}$ is set LOW by the last word or byte read of the long word, respectively.

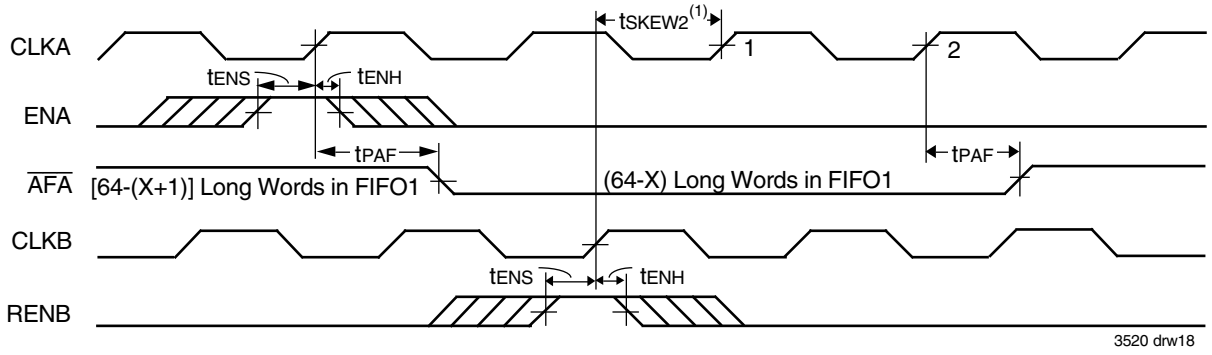
Figure 16. Timing for AEB when FIFO1 is Almost-Empty



NOTES:
1. tSKEW2 is the minimum time between a rising CLKC edge and a rising CLKA edge for $\overline{AEA}$ to transition HIGH in the next CLKA cycle. If the time between the rising CLKC edge and rising CLKA edge is less than tSKEW2, then $\overline{AEA}$ may transition HIGH one CLKA cycle later than shown.
2. FIFO2 read ($\overline{CSA}$ = LOW, W/$\overline{RA}$ = LOW).
3. Port-C size is word or byte; tSKEW2 is referenced from the rising CLKC edge that writes the last word or byte of the long word, respectively.

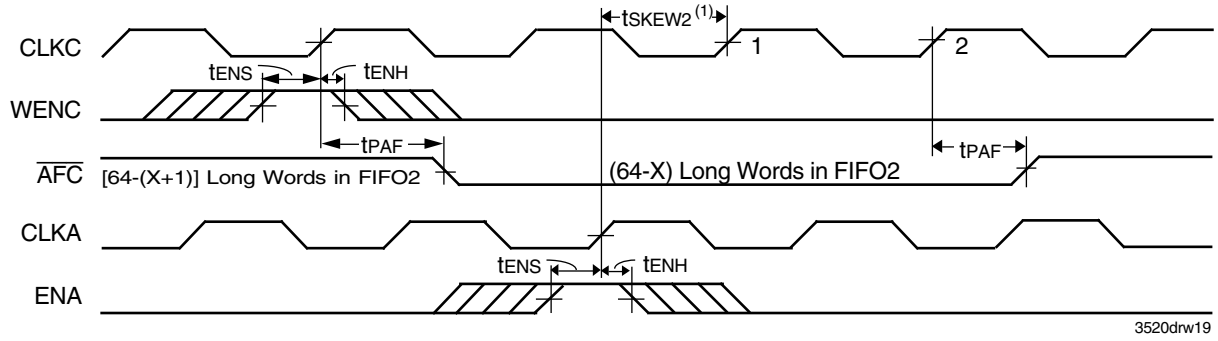
Figure 17. Timing for $\overline{AEA}$ when FIFO2 is Almost-Empty

© 2019 Renesas Electronics Corporation



NOTES:
1. tSKEW2 is the minimum time between a rising CLKA edge and a rising CLKB edge for AFA to transition HIGH in the next CLKA cycle. If the time between the rising CLKA edge and rising CLKB edge is less than tSKEW2, then AFA may transition HIGH one CLKB cycle later than shown.
2. FIFO1 Write (CSA = LOW, W/RA = HIGH).
3. Port-B size is word or byte; tSKEW2 is referenced from the last word or byte read of the long word, respectively.

Figure 18. Timing for AFA when FIFO1 is Almost-Full



NOTES:
1. tSKEW2 is the minimum time between a rising CLKC edge and a rising CLKA edge for AFC to transition HIGH in the next CLKC cycle. If the time between the rising CLKC edge and rising CLKA edge is less than tSKEW2, then AFC may transition HIGH one CLKA cycle later than shown.
2. Port-C size is word or byte; AFC is set LOW by the last word or byte read of the long word, respectively.

Figure 19. Timing for AFC when FIFO2 is Almost-Full

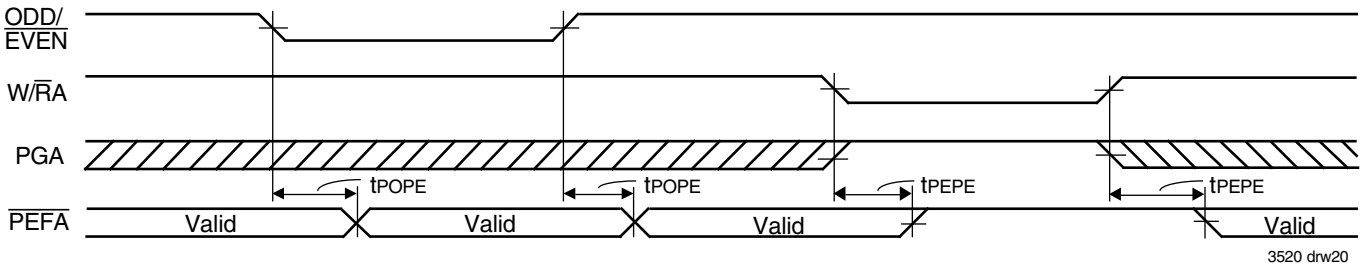


Figure 20. ODD/EVEN, W/RA and PGA to PEFA Timing

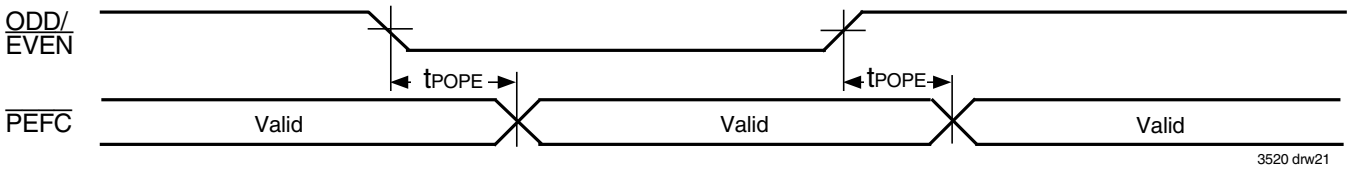
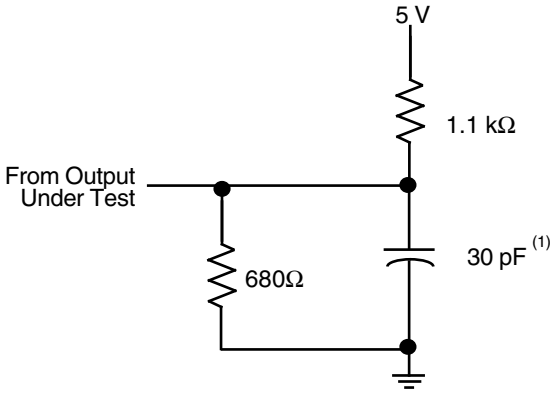


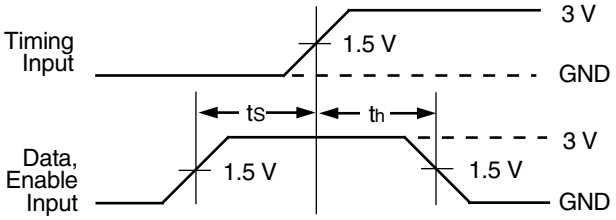
Figure 21. ODD/EVEN to PEFC Timing

© 2019 Renesas Electronics Corporation

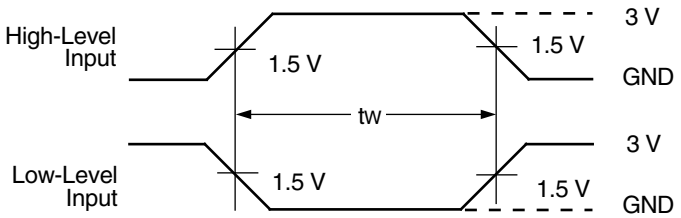
PARAMETER MEASUREMENT INFORMATION



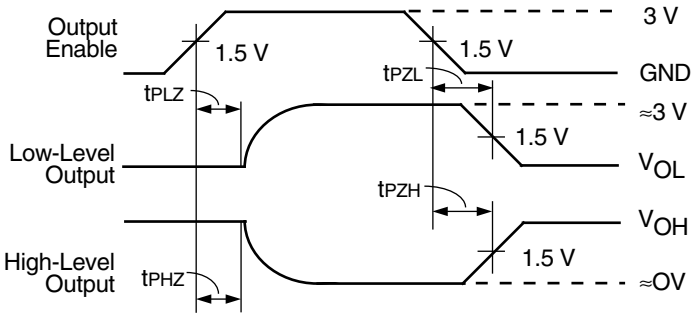
LOAD CIRCUIT



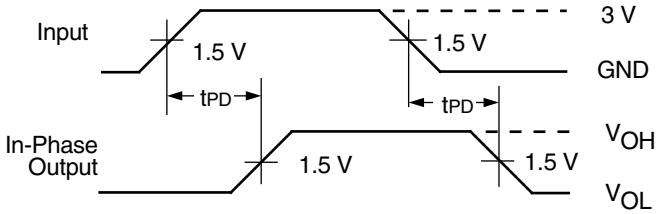
VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS PULSE DURATIONS



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES

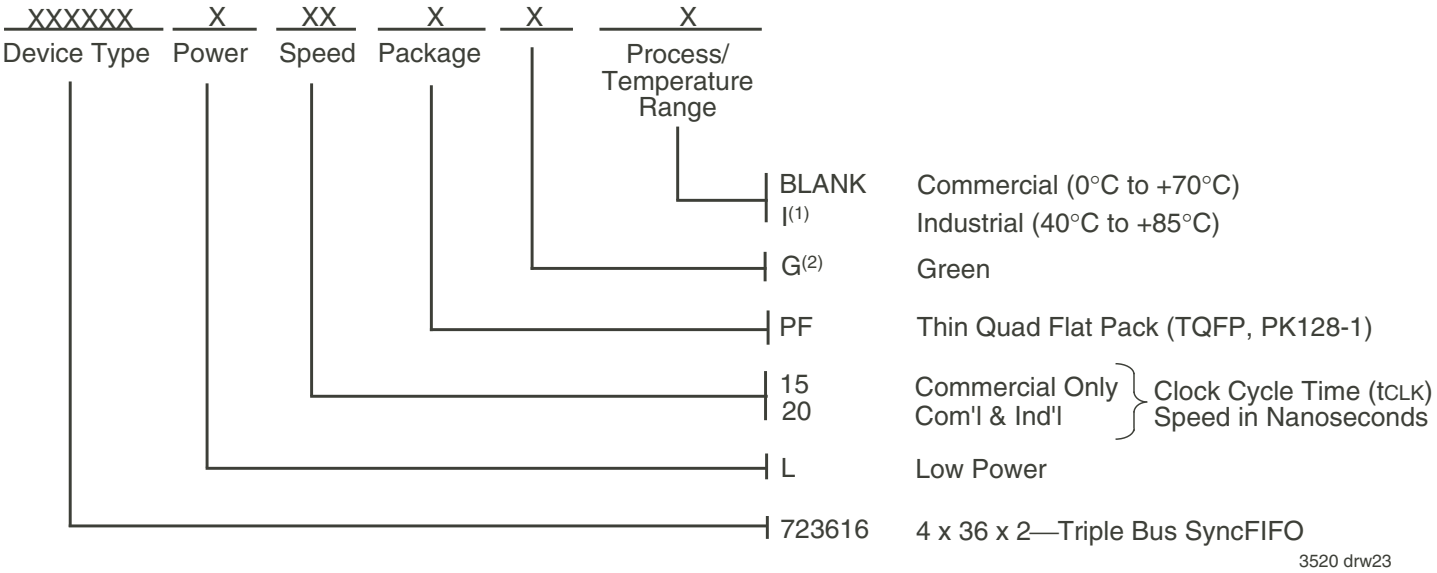
3520 drw22

NOTE:
1. Includes probe and jig capacitance.

Figure 22. Load Circuit and Voltage Waveforms

© 2019 Renesas Electronics Corporation

ORDERING INFORMATION



NOTES:
1. Industrial temperature range product for 20ns speed grade is available as a standard device. All other speed grades are available by special order.
2. Green parts available. For specific speeds and packages contact your sales office.

DATASHEET DOCUMENT HISTORY

03/05/2002	pgs. 1, 6, 8, 9 and 26.
02/04/2009	pgs. 1, and 26.
11/21/2014	PDN# CQ-14-08 issued. See IDT.com for PDN specifics.
08/08/2019	Datasheet changed to Obsolete Status.

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers skilled in the art designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only for development of an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising out of your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Rev.1.0 Mar 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
www.renesas.com/contact/

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

© 2020 Renesas Electronics Corporation. All rights reserved.