CMOS PARALLEL FIFO 64 x 4

IDT72401
IDT72403
OBSOLETE PARTS

FEATURES:

- **First-In/First-Out Dual-Port memory**
- **64 x 4 organization (IDT72401/72403)**
- **RAM-based FIFO with low fall-through time**
- **Low-power consumption**
  - *Active: 175mW (typ.)*
- **Maximum shift rate — 45MHz**
- **High data output drive capability**
- **Asynchronous and simultaneous read and write**
- **Fully expandable by bit width**
- **Fully expandable by word depth**
- **IDT72403 have Output Enable pin to enable output data**
- **High-speed data communications applications**
- **High-performance CMOS technology**
- **Available in CERDIP, plastic DIP and SOIC**
- **Military product compliant to MIL-STD-883, Class B**
- **Standard Military Drawing #5962-86846 and 5962-89523 is listed on this function.**
- **Green parts available, see ordering information**

DESCRIPTION:

The IDT72401 and IDT72403 are asynchronous high-performance First-In/First-Out memories organized 64 words by 4 bits. The IDT72403 also has an Output Enable ($\overline{OE}$) pin. The FIFOs accept 4-bit data at the data input (D_0-D_3). The stored data stack up on a first-in/first-out basis.

A Shift Out (SO) signal causes the data at the next to last word to be shifted to the output while all other data shifts down one location in the stack. The Input Ready (IR) signal acts like a flag to indicate when the input is ready for new data (IR = HIGH) or to signal when the FIFO is full (IR = LOW). The IR signal can also be used to cascade multiple devices together. The Output Ready (OR) signal is a flag to indicate that the output remains valid data (OR = HIGH) or to indicate that the FIFO is empty (OR = LOW). The OR can also be used to cascade multiple devices together.

Width expansion is accomplished by logically ANDing the IR and OR signals to form composite signals.

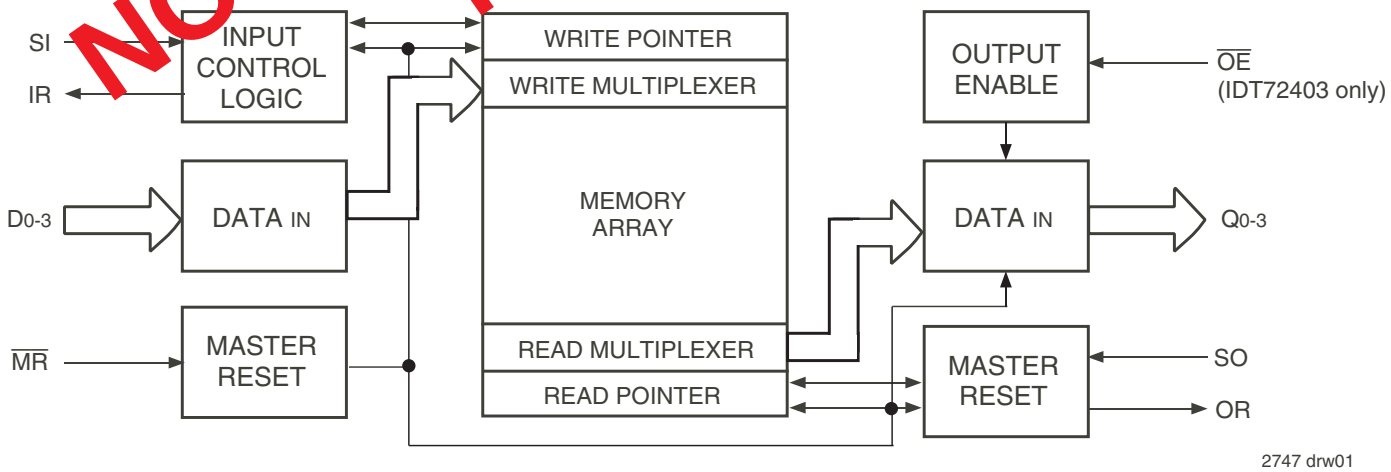
Depth expansion is accomplished by tying the data inputs of one device to the data outputs of the previous device. The IR pin of the receiving device is connected to the SO pin of the sending device and the OR pin of the sending device is connected to the Shift In (SI) pin of the receiving device.

Reading and writing operations are completely asynchronous allowing the FIFO to be used as a buffer between two digital machines of widely varying operating frequencies. The 45MHz speed makes these FIFOs ideal for high-speed communication and controller applications.

Military grade product is manufactured in compliance with the of MIL-STD-883, Class B.

OBSOLETE PARTS
NOT RECOMMENDED FOR
NEW DESIGNS

FUNCTIONAL BLOCK DIAGRAM

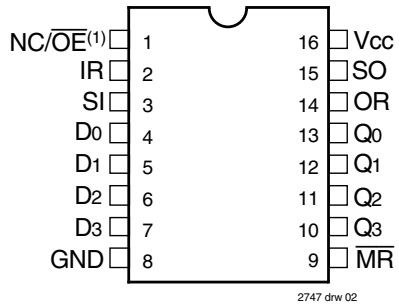


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PIN CONFIGURATIONS

IDT72401/IDT72403



PLASTIC DIP (P16-1, ORDER CODE: P)
CERDIP (D16-1, ORDER CODE: D)
SOIC (SO16-1, ORDER CODE: SO)
TOP VIEW

NOTE:
1. Pin 1: NC - No Connection IDT72401, $\overline{OE}$ - IDT72403

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
T_{STG}	Storage Temp.	–55 to +125	–65 to +150	°C
I_{OUT}	DC Output Current	–50 to +50	–50 to +50	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage Commercial/Military	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.0	—	—	V
V_{IL}(1)	Input High Voltage	—	—	0.8	V
T_A	Operating Temperature Commercial	0	—	70	°C
T_A	Operating Temperature Military	–55	—	125	°C

NOTE:
1. 1.5V undershoots are allowed for 10ns once per cycle.

DC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5.0V ± 10%, T_A = 0°C to +70°C; Military: V_{CC} = 5.0V ± 10%, T_A = –55°C to +125°C)

Symbol	Parameter	Test Conditions	IDT72401 IDT72403 Commercial f_{IN} = 45, 35, 25, 15, 10 MHz Min.	Max.	IDT72401 IDT72403(5) Military f_{IN} = 35, 25, 15, 10 MHz Min.	Max.	Unit
I_{IL}	Low-Level Input Current	V_{CC} = Max., GND ≤ V_I ≤ V_{CC}	–10	—	–10	—	µA
I_{IH}	High-Level Input Current	V_{CC}= Max., GND ≤ V_I ≤ V_{CC}	—	10	—	10	µA
V_{OL}	Low-Level Output Voltage	V_{CC}= Min., I_{OL} = 8mA	—	0.4	—	0.4	V
V_{OH}	High-Level Output Voltage	V_{CC}= Min., I_{OH} = –4mA	2.4	—	2.4	—	V
I_{OS}(1)	Output Short-Circuit Current	V_{CC}= Max., V_O = GND	–20	–110	–20	–110	mA
I_{HZ}(2)	HIGH Impedance Output Current	V_{CC}= Max., V_O = 2.4V	—	20	—	20	µA
I_{LZ}(2)	LOW Impedance Output Current	V_{CC}= Max., V_O = 0.4V	–20	—	–20	—	µA
I_{CC}(3,4)	Active Supply Current	V_{CC}= Max., f = 10MHz	—	35	—	45	mA

NOTES:
1. Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. Guaranteed but not tested.
2. IDT72403 only.
3. Tested with outputs open (I_{OUT} = 0). $\overline{OE}$ is HIGH for IDT72403.
4. For frequencies greater than 10MHz, I_{CC} = 35mA + (1.5mA x [f –10MHz]) commercial, and I_{CC} = 45mA + (1.5mA x [f –10MHz]) military.
5. Military availability for IDT72403 is 10MHz, 35MHz. IDT72401 is available for all MHz.

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OPERATING CONDITIONS

(Commercial: V_{CC} = 5.0V ± 10%, T_A = 0°C to +70°C; Military: V_{CC} = 5.0V ± 10%, T_A = –55°C to +125°C)

			Commercial		Commercial and Military[5]								
			IDT72401L45 IDT72403L45		IDT72401L35 IDT72403L35		IDT72401L25 IDT72403L25		IDT72401L15 IDT72403L15		IDT72401L10 IDT72403L10		
Symbol	Parameter	Figure	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
t_{SIH}[1]	Shift in HIGH Time	2	9	—	9	—	11	—	11	—	11	—	ns
t_{SIL}	Shift in LOW TIme	2	11	—	17	—	24	—	25	—	30	—	ns
t_{IDS}	Input Data Set-up	2	0	—	0	—	0	—	0	—	0	—	ns
t_{IDH}	Input Data Hold Time	2	13	—	15	—	20	—	30	—	40	—	ns
t_{SOH}[1]	Shift Out HIGH Time	5	9	—	9	—	11	—	11	—	11	—	ns
t_{SOL}	Shift Out LOW Time	5	11	—	17	—	24	—	25	—	25	—	ns
t_{MRW}	Master Reset Pulse	8	20	—	25	—	25	—	25	—	30	—	ns
t_{MRS}	Master Reset Pulse to SI	8	10	—	10	—	10	—	25	—	35	—	ns
t_{SIR}	Data Set-up to IR	4	3	—	3	—	5	—	5	—	5	—	ns
t_{HIR}	Data Hold from IR	4	13	—	15	—	20	—	30	—	30	—	ns
t_{SOR}[4]	Data Set-up to OR HIGH	7	0	—	0	—	0	—	0	—	0	—	ns

AC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5.0V ± 10%, T_A = 0°C to +70°C; Military: V_{CC} = 5.0V ± 10%, T_A = –55°C to +125°C)

			Commercial		Commercial and Military[5]								
			IDT72401L45 IDT72403L45		IDT72401L35 IDT72403L35		IDT72401L25 IDT72403L25		IDT72401L15 IDT72403L15		IDT72401L10 IDT72403L10		
Symbol	Parameter	Figure	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
f_{IN}	Shift In Rate	2	—	45	—	35	—	25	—	15	—	10	MHz
t_{IRL}[1]	Shift In to Input Ready LOW	2	—	18	—	18	—	21	—	35	—	40	ns
t_{IRH}[1]	Shift In to Input Ready HIGH	2	—	18	—	20	—	28	—	40	—	45	ns
f_{OUT}	Shift Out Rate	5	—	45	—	35	—	25	—	15	—	10	MHz
t_{ORL}[1]	Shift Out to Output Ready LOW	5	—	18	—	18	—	19	—	35	—	40	ns
t_{ORH}[1]	Shift Out to Output Ready HIGH	5	—	19	—	20	—	34	—	40	—	55	ns
t_{ODH}	Output Data Hold (Previous Word)	5	5	—	5	—	5	—	5	—	5	—	ns
t_{ODS}	Output Data Shift (Next Word)	5	—	19	—	20	—	34	—	40	—	55	ns
t_{PT}	Data Throughput or "Fall-Through"	4, 7	—	30	—	34	—	40	—	65	—	65	ns
t_{MRORL}	Master Reset to OR LOW	8	—	25	—	28	—	35	—	35	—	40	ns
t_{MRIRH}	Master Reset to IR HIGH	8	—	25	—	28	—	35	—	35	—	40	ns
t_{MRQ}	Master Reset to Data Output LOW	8	—	20	—	20	—	25	—	35	—	40	ns
t_{OOE}[3]	Output Valid from $\overline{OE}$ LOW	9	—	12	—	15	—	20	—	30	—	35	ns
t_{HZOE}[3,4]	Output High-Z from $\overline{OE}$ HIGH	9	—	12	—	12	—	15	—	25	—	30	ns
t_{IPH}[2,4]	Input Ready Pulse HIGH	4	9	—	9	—	11	—	11	—	11	—	ns
t_{OPH}[2,4]	Output Ready Pulse HIGH	7	9	—	9	—	11	—	11	—	11	—	ns

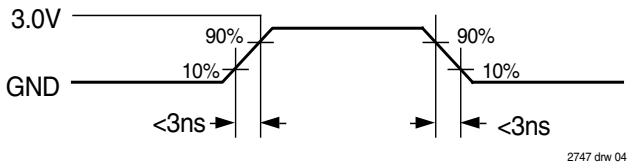
NOTES:

1. Since the FIFO is a very high-speed device, care must be excercised in the design of the hardware and timing utilized within the design. Device grounding and decoupling are crucial to correct operation as the FIFO will respond to very small glitches due to long reflective lines, high capacitances and/or poor supply decoupling and grounding. A monolithic ceramic capacitor of 0.1µF directly between V_{CC} and GND with very short lead length is recommended.
2. This parameter applies to FIFOs communicating with each other in a cascaded mode. IDT FIFOs are guaranteed to cascade with other IDT FIFOs of like speed grades.
3. IDT72403 only.
4. Guaranteed by design but not currently tested.
5. Military availability for IDT72403 is 10MHz, 35MHz. IDT72401 is available for all MHz.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1

ALL INPUT PULSES:

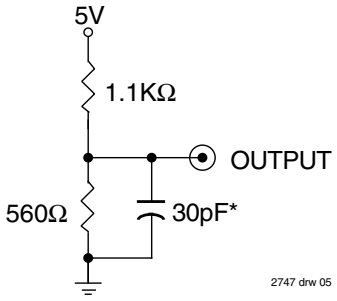


CAPACITANCE

(T_A = +25°C, f = 1.0MHz)

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	7	pF

NOTE:
1. Characterized values, not currently tested.



or equivalent circuit

Figure 1. AC Test Load

*Including scope and jig

SIGNAL DESCRIPTIONS

INPUTS:

DATA INPUT (D_{0-3})

Data input lines. The IDT72401 and IDT72403 have a 4-bit data input.

CONTROLS:

SHIFT IN (SI)

Shift In controls the input of the data into the FIFO. When SI is HIGH, data can be written to the FIFO via the D_{0-3} lines.

SHIFT OUT (SO)

Shift Out controls the output of data of the FIFO. When SO is HIGH, data can be read from the FIFO via the Data Output (Q_{0-3}) lines.

MASTER RESET ($\overline{MR}$)

Master Reset clears the FIFO of any data stored within. Upon power up, the FIFO should be cleared with a $\overline{MR}$. $\overline{MR}$ is active LOW.

INPUT READY (IR)

When Input Ready is HIGH, the FIFO is ready for new input data to be written to it. When IR is LOW the FIFO is unavailable for new input data. IR is also used to cascade many FIFOs together, as shown in Figures 10 and 11.

OUTPUT READY (OR)

When Output Ready is HIGH, the output (Q_{0-3}) contains valid data. When OR is LOW, the FIFO is unavailable for new output data. OR is also used to cascade many FIFOs together, as shown in Figures 10 and 11.

OUTPUT ENABLE ($\overline{OE}$) (IDT72403 ONLY)

Output enable is used to read FIFO data onto a bus. $\overline{OE}$ is active LOW.

OUTPUTS:

DATA OUTPUT (Q_{0-3})

Data Output lines. The IDT72401 and IDT72403 have a 4-bit data output.

FUNCTIONAL DESCRIPTION

The 64 x 4 FIFO is designed using a dual port RAM architecture as opposed to the traditional shift register approach. This FIFO architecture has a write pointer, a read pointer and control logic, which allow simultaneous read and write operations. The write pointer is incremented by the falling edge of the Shift In (SI) control; the read pointer is incremented by the falling edge of the Shift Out (SO). The Input Ready (IR) signals when the FIFO has an available memory location; Output Ready (OR) signals when there is valid data on the output. Output Enable ($\overline{OE}$) provides the capability of three-stating the FIFO outputs.

FIFO RESET

The FIFO must be reset upon power up using the Master Reset ($\overline{MR}$) signal. This causes the FIFO to enter an empty state, signified by Output Ready (OR) being LOW and Input Ready (IR) being HIGH. In this state, the data outputs (Q_{0-3}) will be LOW.

DATA INPUT

Data is shifted in on the LOW-to-HIGH transition of Shift In (SI). This loads input data into the first word location of the FIFO and causes Input Ready (IR) to go LOW. On the HIGH-to-LOW transition of SI, the write pointer is moved to the next word position and IR goes HIGH, indicating the readiness to accept new data. If the FIFO is full, IR will remain LOW until a word of data is shifted out.

DATA OUTPUT

Data is shifted out on the HIGH-to-LOW transition of Shift Out (SO). This causes the internal read pointer to be advanced to the next word location. If data is present, valid data will appear on the outputs and Output Ready (OR) will go HIGH. If data is not present, OR will stay LOW indicating the FIFO is empty. The last valid word read from the FIFO will remain at the FIFOs output when it is empty. When the FIFO is not empty, OR goes LOW on the LOW-to-HIGH transition of SO. Previous data remains on the output until the HIGH-to-LOW transition of SO).

FALL THROUGH MODE

The FIFO operates in a fall-through mode when data gets shifted into an empty FIFO. After a fall-through delay the data propagates to the output. When the data reaches the output, the Output Ready (OR) goes HIGH. Fall-through mode also occurs when the FIFO is completely full. When data is shifted out of the full FIFO, a location is available for new data. After a fall-through delay, the Input Ready (IR) goes HIGH. If Shift In (SI) is HIGH, the new data can be written to the FIFO.

Since these FIFOs are based on an internal dual-port RAM architecture with separate read and write pointers, the fall-through time (t_{PT}) is one cycle long. A word may be written into the FIFO on a clock cycle and can be accessed on the next clock cycle.

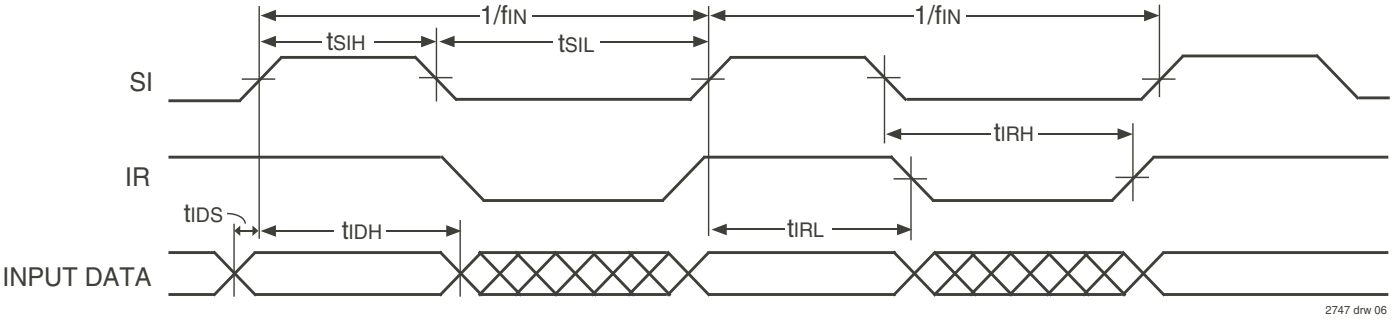
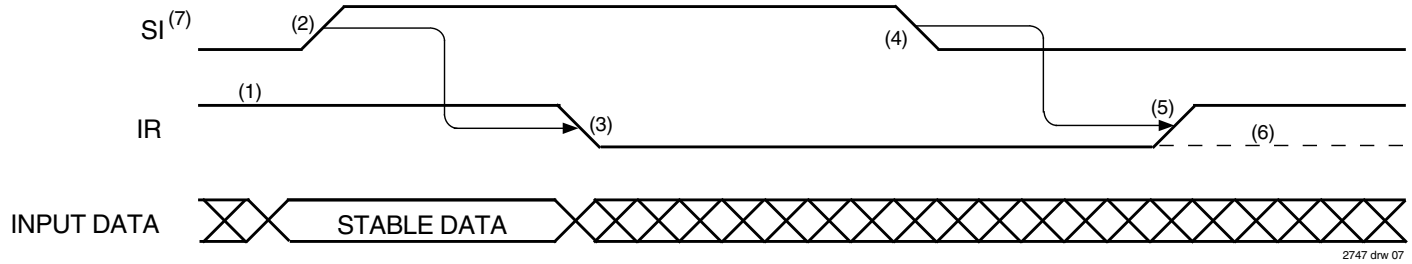
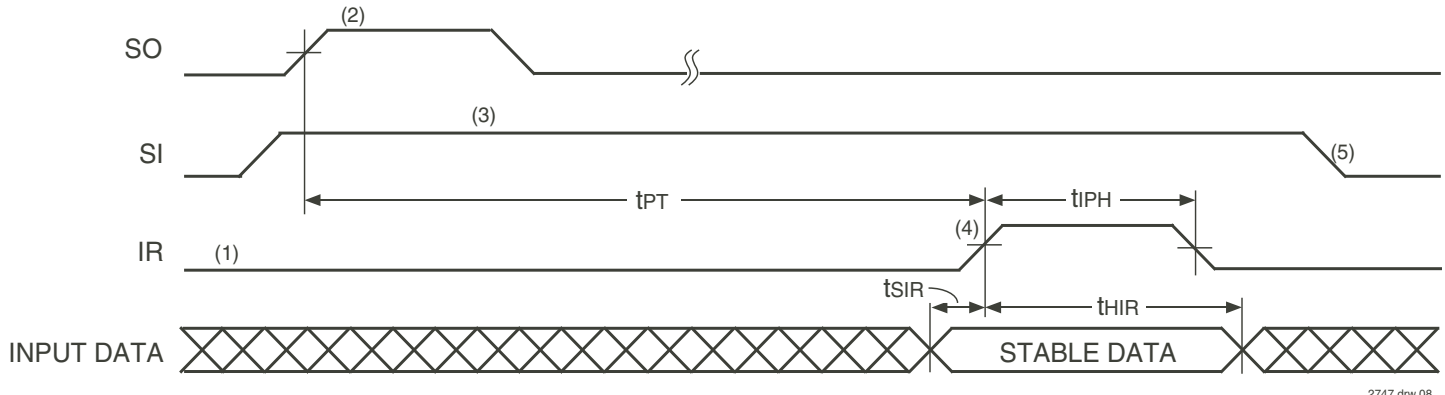


Figure 2. Input Timing



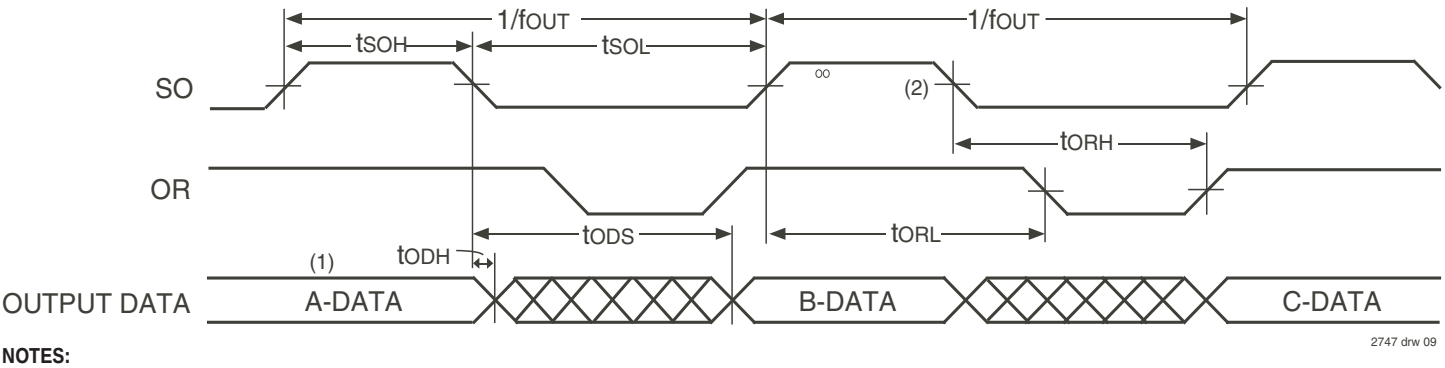
NOTES:
1. IR HIGH indicates space is available and a SI pulse may be applied.
2. Input Data is loaded into the first word.
3. IR goes LOW indicating the first word is full.
4. The write pointer is incremented.
5. The FIFO is ready for the next word.
6. If the FIFO is full then the IR remains LOW.
7. SI pulses applied while IR is LOW will be ignored (see Figure 4).

Figure 3. The Mechanism of Shifting Data Into the FIFO



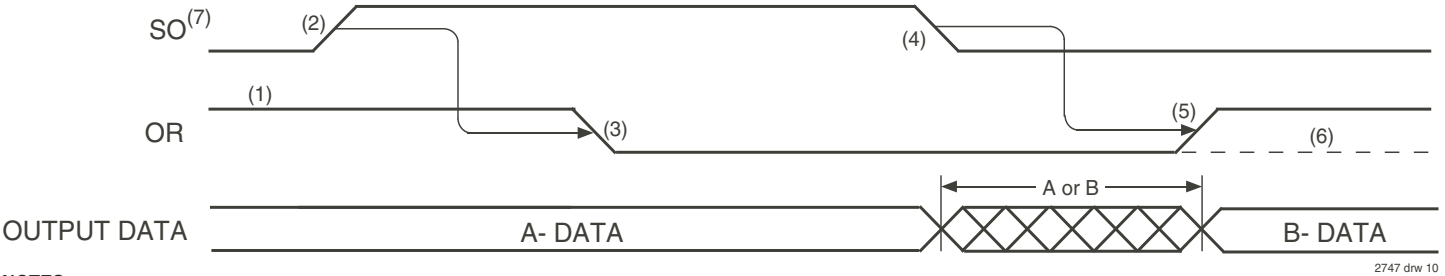
NOTES:
1. FIFO is initially full.
2. SO pulse is applied.
3. SI is held HIGH.
4. As soon as IR becomes HIGH the Input Data is loaded into the FIFO.
5. The write pointer is incremented. SI should not go LOW until (t_{PT} + t_{IPH}).

Figure 4. Data is Shifted In Whenever Shift In and Input Ready are Both HIGH



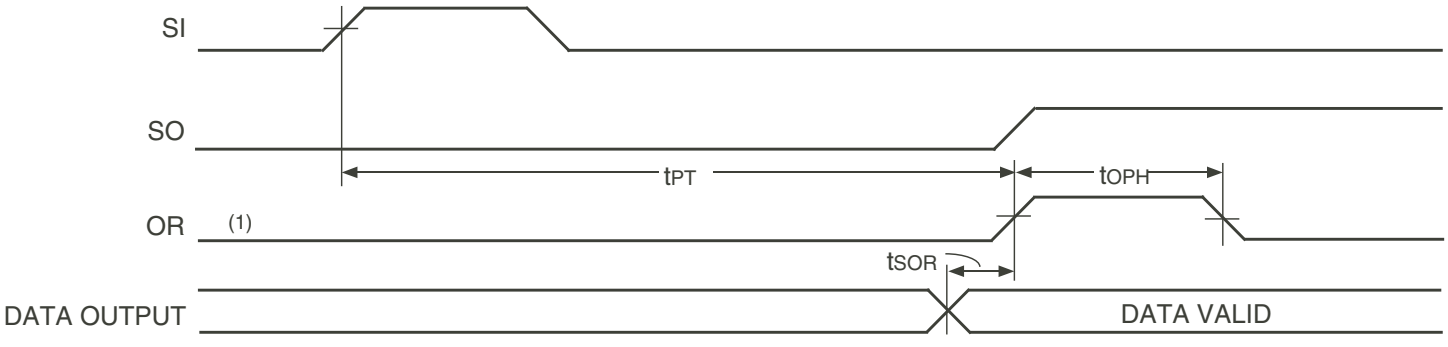
NOTES:
1. This data is loaded consecutively A, B, C.
2. Data is shifted out when SO makes a HIGH to LOW transition.

Figure 5. Output TIming



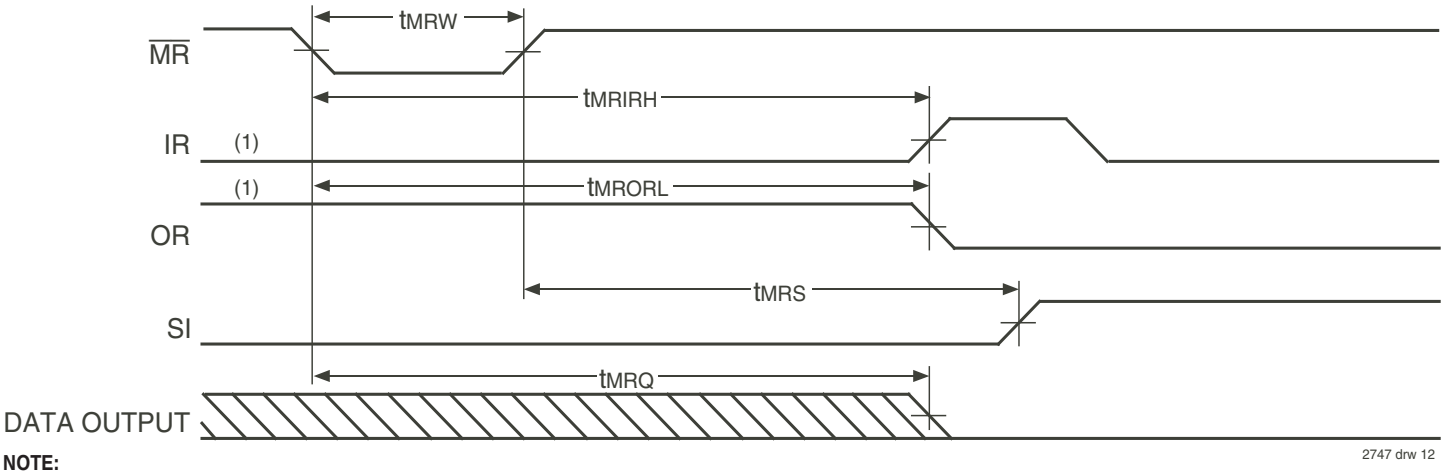
NOTES:
1. OR HIGH indicates that data is available and a SO pulse may be applied.
2. SO goes HIGH causing the next step.
3. OR goes LOW.
4. The read pointer is incremented.
5. OR goes HIGH indicating that new data (B) is now available at the FIFO outputs.
6. If the FIFO has only one word loaded (A DATA) then OR stays LOW and the A DATA remains unchanged at the outputs.
7. SO pulses applied when OR is LOW will be ignored.

Figure 6. The Mechanism of Shifting Data Out of the FIFO



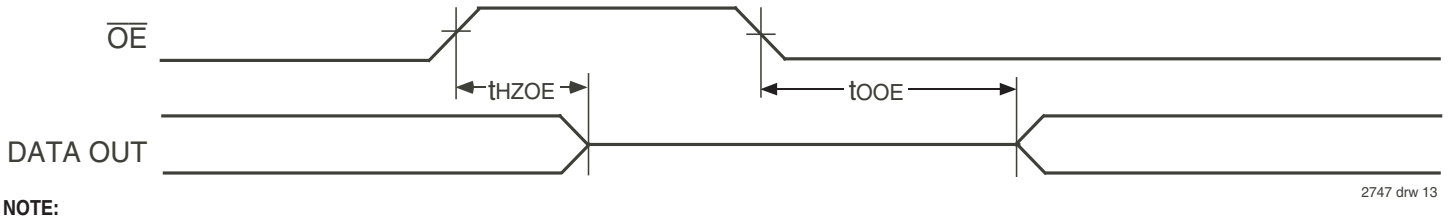
NOTE:
1. FIFO initially empty.

Figure 7. tPT and tOPH Specification



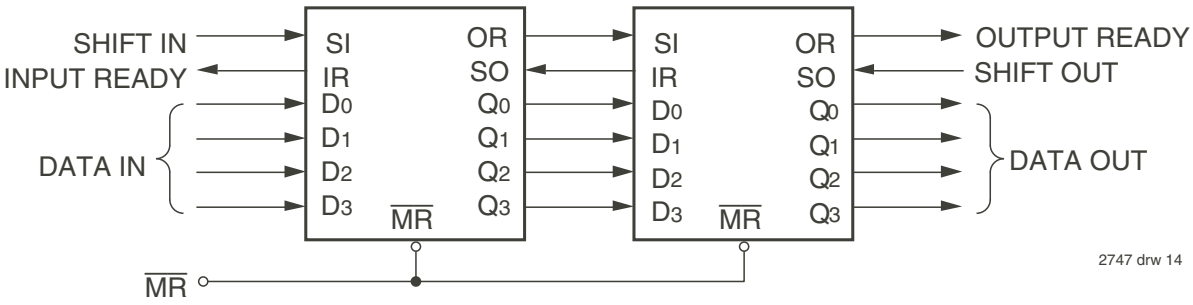
NOTE:
1. Worst case, FIFO initially full.

Figure 8. Master Reset Timing



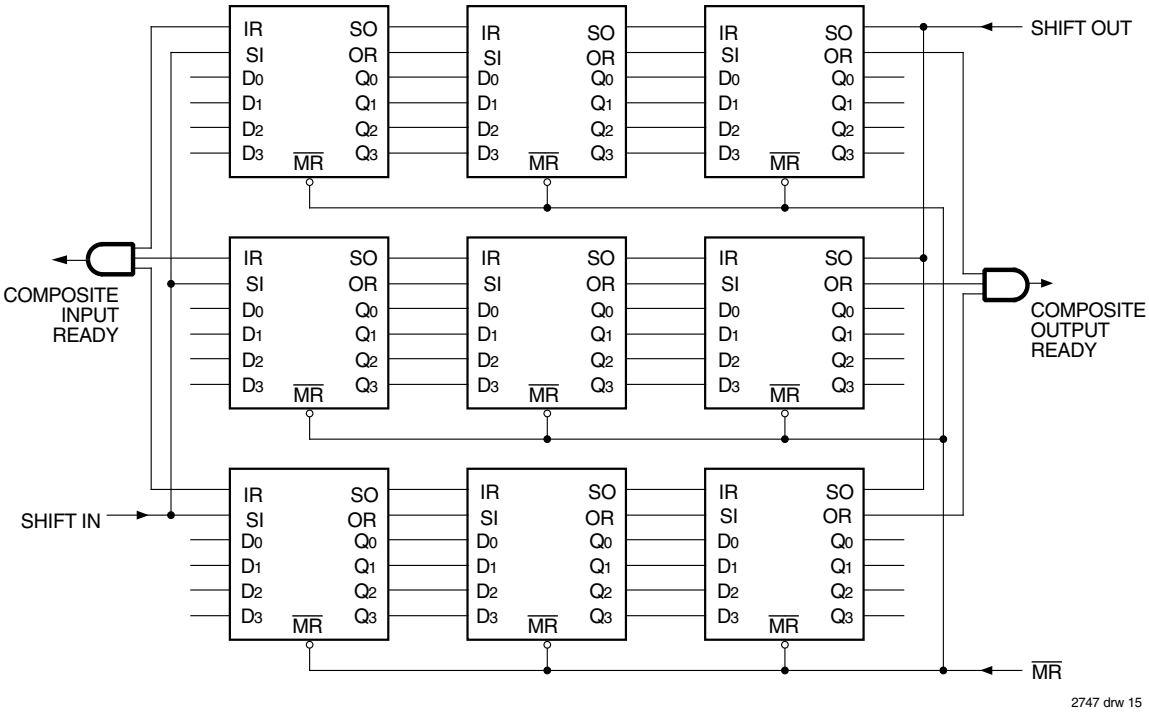
NOTE:
1. High-Z transitions are referenced to the steady-state VOH –500mV and VOL +500mV levels on the output. tHZOE is tested with 5pF load capacitance instead of 30pF as shown in Figure 1.

Figure 9. Output Enable Timing, IDT72403 Only



NOTE:
1. FIFOs can be easily cascaded to any desired path. The handshaking and associated timing between the FIFOs are handled by the inherent timing of the devices.

Figure 10. 128 x 4 Depth Expansion

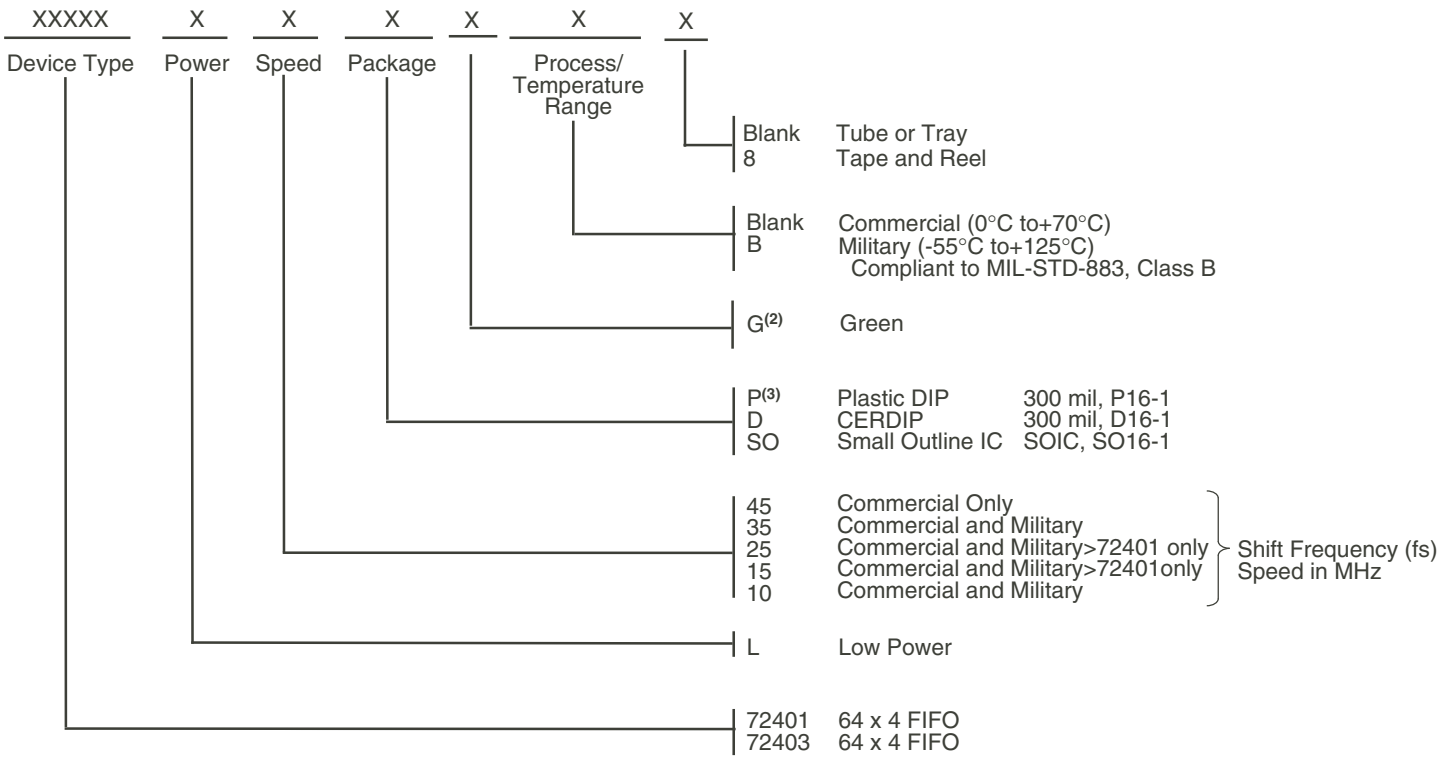


NOTES:

1. When the memory is empty, the last word will remain on the outputs until the $\overline{MR}$ is strobed or a new data word falls through to the output. However, OR will remain LOW, indicating data at the output is not valid.
2. When the output data changes as a result of a pulse on SO, the OR signal always goes LOW before there is any change in output data and stays LOW until the new data has appeared on the outputs. Anytime OR is HIGH, there is valid stable data on the outputs.
3. If SO is held HIGH while the memory is empty and a word is written into the input, that word will appear at the output after a fall-through time. OR will go HIGH for one internal cycle (at least t_{ORL}) and then go back LOW again. The stored word will remain on the outputs. If more words are written into the FIFO, they will line up behind the first word and will not appear on the outputs until SO has been brought LOW.
4. When the $\overline{MR}$ is brought LOW, the outputs are cleared to LOW, IR goes HIGH and OR goes LOW. If SI is HIGH when the $\overline{MR}$ goes HIGH, the data on the inputs will be written into the memory and IR will return to the LOW state until SI is brought LOW. If SI is LOW when the $\overline{MR}$ is ended, IR will go HIGH, but the data in the inputs will not enter the memory until SI goes HIGH.
5. FIFOs are expandable on depth and width. However, in forming wider words, two external gates are required to generate composite Input and OR flags. This is due to the variation of delays of the FIFOs.

Figure 11. 192 x 12 Depth and Width Expansion

ORDERING INFORMATION



2747 drw 16

NOTES:
1. Industrial temperature range is available by special order.
2. Green parts are available, for specific speeds and packages contact your sales office.
3. For "P", Plastic Dip, when ordering green package, the suffix is "PDG".

DATASHEET DOCUMENT HISTORY

07/10/2003 pgs. 2, 3, and 9.
10/27/2005 pgs. 1- 9.
04/25/2008 pgs. 1- 9.
02/11/2009 pg. 9.
06/29/2012 pgs. 1 and 9.
09/05/2014 PDN# CQ-14-06R1 issued. See IDT.com for PDN specifics.
08/22/2019 Datasheet changed to Obsolete Status.

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
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