3.3 VOLT CMOS SyncBiFIFO™ 64 x 36 x 2

72V3612

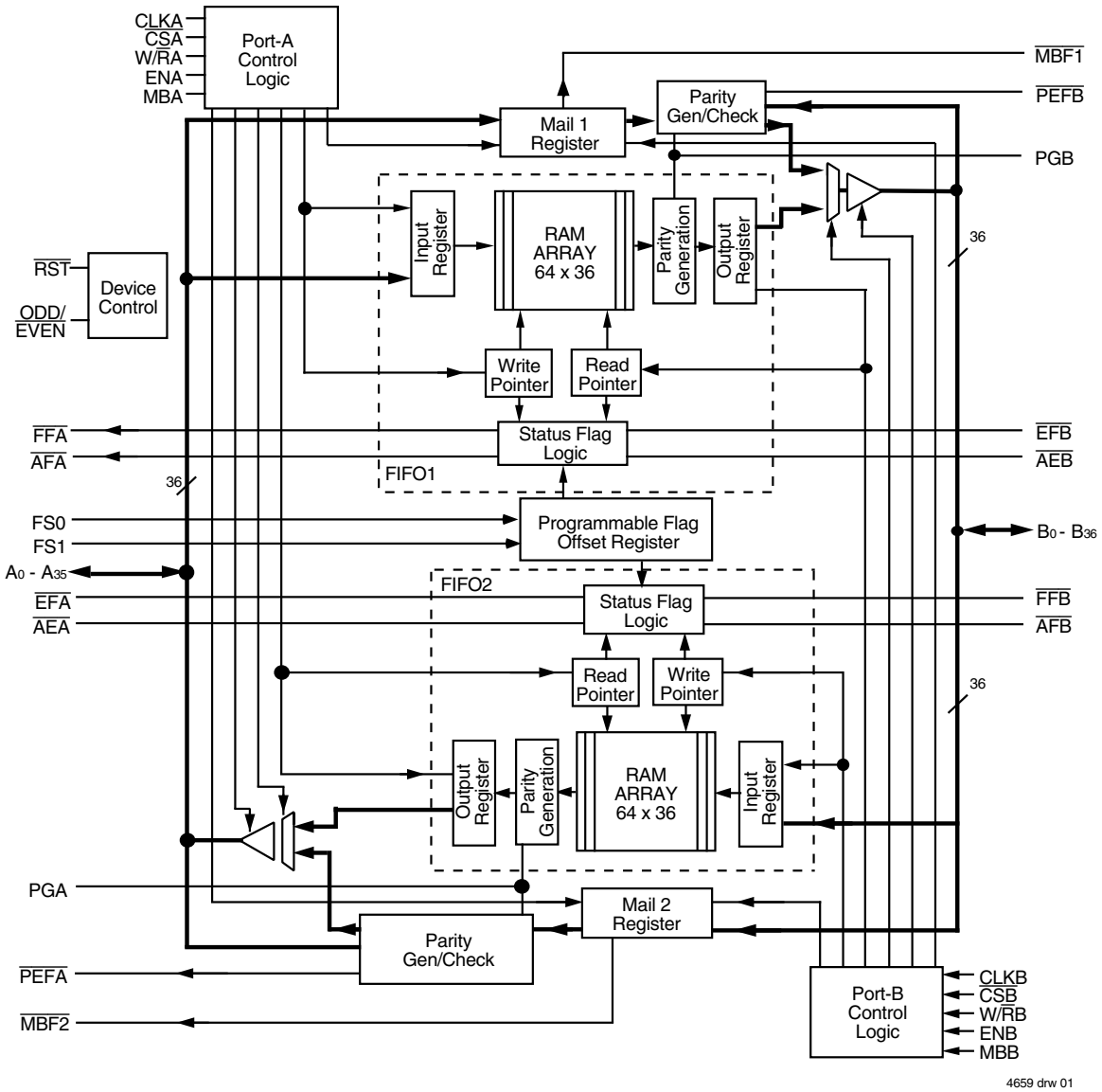
FEATURES:

- **Two independent clocked FIFOs (64 x 36 storage capacity each) buffering data in opposite directions**
- **Supports clock frequencies up to 83 MHz**
- **Fast access times of 8ns**
- **Free-running CLKA and CLKB can be asynchronous or coincident (simultaneous reading and writing of data on a single clock edge is permitted)**
- **Mailbox bypass Register for each FIFO**
- **Programmable Almost-Full and Almost-Empty Flags**
- **Microprocessor interface control logic**
- **$\overline{EFA}$, $\overline{FFA}$, $\overline{AEA}$, and $\overline{AFA}$ flags synchronized by CLKA**
- **$\overline{EFB}$, $\overline{FFB}$, $\overline{AEB}$, and $\overline{AFB}$ flags synchronized by CLKB**
- **Passive parity checking on each port**
- **Parity generation can be selected for each port**
- **Available in space saving 120-pin thin quad flat package (TQFP)**
- **Green parts available, see ordering information**

DESCRIPTION:

The IDT72V3612 is designed to run off a 3.3V supply for exceptionally low-power consumption. This device is a monolithic high-speed, low-power CMOS bi-directional clocked FIFO memory. It supports clock frequencies up to 83 MHz and has read access times as fast as 8ns. The FIFO operates in IDT Standard mode. Two independent 64 x 36 dual-port SRAM FIFOs on board the chip buffer data in opposite directions. Each FIFO has flags to indicate empty and full conditions and two programmable flags (Almost-Full and Almost-Empty) to

FUNCTIONAL BLOCK DIAGRAM



COMMERCIAL TEMPERATURE RANGE

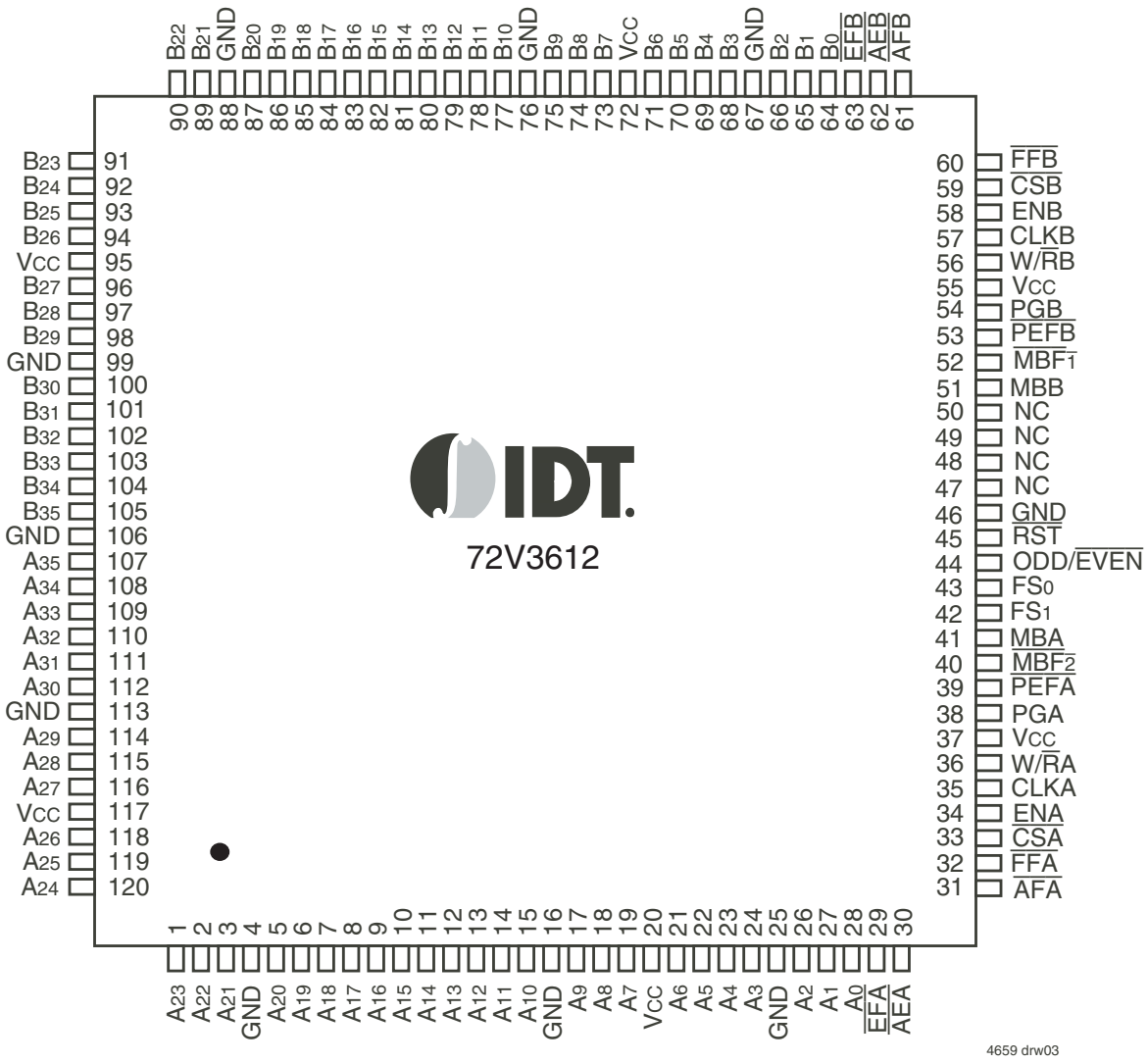
indicate when a selected number of words is stored in memory. Communication between each port can bypass the FIFOs via two 36-bit mailbox registers. Each mailbox register has a flag to signal when new mail has been stored. Parity is checked passively on each port and may be ignored if not desired. Parity generation can be selected for data read from each port. Two or more devices can be used in parallel to create wider data paths.

This device is a clocked FIFO, which means each port employs a synchronous interface. All data transfers through a port are gated to the LOW-to-HIGH transition of a port clock by enable signals. The clocks for each port are independent of one another and can be asynchronous or coincident. The enables for each port are arranged to provide a simple bi-directional interface between microprocessors and/or buses with synchronous control.

The Full Flag ($\overline{FFA}$, $\overline{FFB}$) and Almost-Full ($\overline{AFA}$, $\overline{AFB}$) flag of a FIFO are two-stage synchronized to the port clock that writes data to its array. The Empty Flag ($\overline{EFA}$, $\overline{EFB}$) and Almost-Empty ($\overline{AEA}$, $\overline{AEB}$) flag of a FIFO are two stage synchronized to the port clock that reads data from its array.

The IDT72V3612 is characterized for operation from 0°C to 70°C. This device is fabricated using high speed, submicron CMOS technology.

PIN CONFIGURATION



NOTES:
1. Pin 1 identifier in corner.
2. NC - No internal connection.

TQFP (PNG120, order code: PFG)
TOP VIEW

PIN DESCRIPTION

Symbol	Name	I/O	Description
A0-A35	Port A Data	I/O	36-bit bidirectional data port for side A.
$\overline{AEA}$	Port A Almost-Empty Flag	O (Port A)	Programmable Almost-Empty flag synchronized to CLKA. It is LOW when the number of words in the FIFO2 is less than or equal to the value in the offset register, X.
$\overline{AEB}$	Port B Almost-Empty Flag	O (PortB)	Programmable Almost-Empty flag synchronized to CLKB. It is LOW when the number of words in FIFO1 is less than or equal to the value in the offset register, X.
$\overline{AFA}$	Port A Almost-Full Flag	O (Port A)	Programmable Almost-Full flag synchronized to CLKA. It is LOW when the number of empty locations in FIFO1 is less than or equal to the value in the offset register, X.
$\overline{AFB}$	Port B Almost-Full Flag	O (Port B)	Programmable Almost-Full flag synchronized to CLKB. It is LOW when the number of empty locations in FIFO2 is less than or equal to the value in the offset register, X.
B0-B35	Port B Data.	I/O	36-bit bidirectional data port for side B.
CLKA	Port A Clock	I	CLKA is a continuous clock that synchronizes all data transfers through port A and can be asynchronous or coincident to CLKB. $\overline{EFA}$, $\overline{FFA}$, $\overline{AFA}$, and $\overline{AEA}$ are synchronized to the LOW-to-HIGH transition of CLKA.
CLKB	Port B Clock	I	CLKB is a continuous clock that synchronizes all data transfers through port B and can be asynchronous or coincident to CLKA. $\overline{EFB}$, $\overline{FFB}$, $\overline{AFB}$, and $\overline{AEB}$ are synchronized to the LOW-to-HIGH transition of CLKB.
$\overline{CSA}$	Port A Chip Select	I	$\overline{CSA}$ must be LOW to enable a LOW-to-HIGH transition of CLKA to read or write data on port A. The A0-A35 outputs are in the high-impedance state when $\overline{CSA}$ is HIGH.
$\overline{CSB}$	Port B Chip Select	I	$\overline{CSB}$ must be LOW to enable a LOW-to-HIGH transition of CLKB to read or write data on port B. The B0-B35 outputs are in the high-impedance state when $\overline{CSB}$ is HIGH.
$\overline{EFA}$	Port A Empty Flag	O (Port A)	$\overline{EFA}$ is synchronized to the LOW-to-HIGH transition of CLKA. When $\overline{EFA}$ is LOW, FIFO2 is empty, and reads from its memory are disabled. Data can be read from FIFO2 to the output register when $\overline{EFA}$ is HIGH. $\overline{EFA}$ is forced LOW when the device is reset and is set HIGH by the second LOW-to-HIGH transition of CLKA after data is loaded into empty FIFO2 memory.
$\overline{EFB}$	Port B Empty Flag	O (Port B)	$\overline{EFB}$ is synchronized to the LOW-to-HIGH transition of CLKB. When $\overline{EFB}$ is LOW, the FIFO1 is empty, and reads from its memory are disabled. Data can be read from FIFO1 to the output register when $\overline{EFB}$ is HIGH. $\overline{EFB}$ is forced LOW when the device is reset and is set HIGH by the second LOW-to-HIGH transition of CLKB after data is loaded into empty FIFO1 memory.
ENA	Port A Enable	I	ENA must be HIGH to enable a LOW-to-HIGH transition of CLKA to read or write data on port A.
ENB	Port B Enable	I	ENB must be HIGH to enable a LOW-to-HIGH transition of CLKB to read or write data on port B.
$\overline{FFA}$	Port A Full Flag	O (Port A)	$\overline{FFA}$ is synchronized to the LOW-to-HIGH transition of CLKA. When $\overline{FFA}$ is LOW, FIFO1 is full, and writes to its memory are disabled. $\overline{FFA}$ is forced LOW when the device is reset and is set HIGH by the second LOW-to-HIGH transition of CLKA after reset.
$\overline{FFB}$	Port B Full Flag	O (Port B)	$\overline{FFB}$ is synchronized to the LOW-to-HIGH transition of CLKB. When $\overline{FFB}$ is LOW, FIFO2 is full, and writes to its memory are disabled. $\overline{FFB}$ is forced LOW when the device is reset and is set HIGH by the second LOW-to-HIGH transition of CLKB after reset.
FS1, FS0	Flag Offset Selects	I	The LOW-to-HIGH transition of $\overline{RST}$ latches the values of FS0 and FS1, which selects one of four preset values for the Almost-Full flag and Almost-Empty flag.
MBA	Port A Mailbox Select	I	A HIGH level on MBA chooses a mailbox register for a port A read or write operation. When the A0-A35 outputs are active, a HIGH level on MBA selects data from the mail2 register for output, and a LOW level selects FIFO2 output register data for output.
MBB	Port B Mailbox Select	I	A HIGH level on MBB chooses a mailbox register for a port B read or write operation. When the B0-B35 outputs are active, a HIGH level on MBB selects data from the mail1 register for output, and a LOW level selects FIFO1 output register data for output.
$\overline{MBF1}$	Mail1 Register Flag	O	$\overline{MBF1}$ is set LOW by a LOW-to-HIGH transition of CLKA that writes data to the mail1 register. Writes to the mail1 register are inhibited while $\overline{MBF1}$ is set LOW. $\overline{MBF1}$ is set HIGH by a LOW-to-HIGH transition of CLKB when a port B read is selected and MBB is HIGH. $\overline{MBF1}$ is set HIGH when the device is reset.

PIN DESCRIPTION (CONTINUED)

Symbol	Name	I/O	Description
$\overline{MBF2}$	Mail2 Register Flag	O	$\overline{MBF2}$ is set LOW by a LOW-to-HIGH transition of CLKB that writes data to the mail2 register. Writes to the mail2 register are inhibited while $\overline{MBF2}$ is set LOW. $\overline{MBF2}$ is set HIGH by a LOW-to-HIGH transition of CLKA when a port A read is selected and MBA is HIGH. $\overline{MBF2}$ is set HIGH when the device is reset.
ODD/$\overline{EVEN}$	Odd/Even Parity Select	I	Odd parity is checked on each port when ODD/$\overline{EVEN}$ is HIGH, and even parity is checked when ODD/$\overline{EVEN}$ is LOW. ODD/$\overline{EVEN}$ also selects the type of parity generated for each port if parity generation is enabled for a read operation.
$\overline{PEFA}$	Port A Parity Error Flag	O (Port A)	When any byte applied to terminals A0-A35 fails parity, $\overline{PEFA}$ is LOW. Bytes are organized as A0-A8, A9-A17, A18-A26, and A27-A35, with the most significant bit of each byte serving as the parity bit. The type of parity checked is determined by the state of the ODD/$\overline{EVEN}$ input. The parity trees used to check the A0-A35 inputs are shared by the mail2 register to generate parity if parity generation is selected by PGA. Therefore, if a mail2 read with parity generation is setup by having W/$\overline{R}$A LOW, MBA HIGH, and PGA HIGH, the $\overline{PEFA}$ flag is forced HIGH regardless of the A0-A35 inputs.
$\overline{PEFB}$	Port B Parity Error Flag	O (Port B)	When any byte applied to terminals B0-B35 fails parity, $\overline{PEFB}$ is LOW. Bytes are organized as B0-B8, B9-B17, B18-B26, B27-B35 with the most significant bit of each byte serving as the parity bit. The type of parity checked is determined by the state of the ODD/$\overline{EVEN}$ input. The parity trees used to check the B0-B35 inputs are shared by the mail1 register to generate parity if parity generation is selected by PGB. Therefore, if a mail1 read with parity generation is setup by having W/$\overline{R}$B LOW, MBB HIGH, and PGB HIGH, the $\overline{PEFB}$ flag is forced HIGH regardless of the state of the B0-B35 inputs.
PGA	Port A Parity Generation	I	Parity is generated for data reads from port A when PGA is HIGH. The type of parity generated is selected by the state of the ODD/$\overline{EVEN}$ input. Bytes are organized as A0-A8, A9-A17, A18-A26, and A27-A35. The generated parity bits are output in the most significant bit of each byte.
PGB	Port B Parity Generation	I	Parity is generated for data reads from port B when PGB is HIGH. The type of parity generated is selected by the state of the ODD/$\overline{EVEN}$ input. Bytes are organized as B0-B8, B9-B17, B18-B26, and B27-B35. The generated parity bits are output in the most significant bit of each byte.
$\overline{RST}$	Reset	I	To reset the device, four LOW-to-HIGH transitions of CLKA and four LOW-to-HIGH transitions of CLKB must occur while $\overline{RST}$ is LOW. This sets the $\overline{AFA}$, $\overline{AFB}$, $\overline{MBF1}$, and $\overline{MBF2}$ flags HIGH and the $\overline{EFA}$, $\overline{EFB}$, $\overline{AEA}$, $\overline{AEB}$, $\overline{FFA}$, and $\overline{FFB}$ flags LOW. The LOW-to-HIGH transition of $\overline{RST}$ latches the status of the FS1 and FS0 inputs to select Almost-Full and Almost-Empty flag offset.
W/$\overline{R}$A	Port A Write/Read Select	I	A HIGH selects a write operation and a LOW selects a read operation on port A for a LOW-to-HIGH transition of CLKA. The A0-A35 outputs are in the high-impedance state when W/$\overline{R}$A is HIGH.
W/$\overline{R}$B	Port B Write/Read Select	I	A HIGH selects a write operation and a LOW selects a read operation on port B for a LOW-to-HIGH transition of CLKB. The B0-B35 outputs are in the high-impedance state when W/$\overline{R}$B is HIGH.

ABSOLUTE MAXIMUM RATINGS OVER OPERATING FREE-AIR TEMPERATURE RANGE (Unless otherwise noted)(2)

Symbol	Rating	Commercial	Unit
V_{CC}	Supply Voltage Range	–0.5 to +4.6	V
V_I(2)	Input Voltage Range	–0.5 to V_{CC}+0.5	V
V_O(2)	Output Voltage Range	–0.5 to V_{CC}+0.5	V
I_{IK}	Input Clamp Current, (V_I < 0 or V_I > V_{CC})	±20	mA
I_{OK}	Output Clamp Current, (V_O < 0 or V_O > V_{CC})	±50	mA
I_{OUT}	Continuous Output Current, (V_O = 0 to V_{CC})	±50	mA
I_{CC}	Continuous Current Through V_{CC} or GND	±500	mA
T_{STG}	Storage Temperature Range	–65 to 150	°C

NOTES:
1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "Recommended Operating Conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded provided the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}(1)	Supply Voltage	3.0	3.3	3.6	V
V_{IH}	HIGH Level Input Voltage	2	—	V_{CC}+0.5	V
V_{IL}	LOW-Level Input Voltage	—	—	0.8	V
I_{OH}	HIGH-Level Output Current	—	—	–4	mA
I_{OL}	LOW-Level Output Current	—	—	8	mA
T_A	Operating Free-air Temperature	0	—	70	°C

NOTE:
1. For 12ns (83MHz operation), Vcc=3.3V +/-0.15V, JEDEC JESD8-A compliant

ELECTRICAL CHARACTERISTICS OVER RECOMMENDED OPERATING FREE-AIR TEMPERATURE RANGE (Unless otherwise noted)

Symbol	Parameter	Test Conditions		IDT72V3612 Commercial t_{CLK} = 12, 15 ns			Unit
				Min.	Typ.(1)	Max.	
V_{OH}	Output Logic "1" Voltage	V_{CC} = 3.0V,	I_{OH} = –4 mA	2.4	—	—	V
V_{OL}	Output Logic "0" Voltage	V_{CC} = 3.0V,	I_{OL} = 8 mA	—	—	0.5	V
I_{LI}	Input Leakage Current (Any Input)	V_{CC} = 3.6V,	V_I = V_{CC} or 0	—	—	±5	µA
I_{LO}	Output Leakage Current	V_{CC} = 3.6V,	V_O = V_{CC} or 0	—	—	±5	µA
I_{CC}(2)	Standby Current	V_{CC} = 3.6V,	V_I = V_{CC} - 0.2V or 0	—	—	500	µA
C_{IN}	Input Capacitance	V_I = 0,	f = 1 MHz	—	4	—	pF
C_{OUT}	Output Capacitance	V_O = 0,	f = 1 MHZ	—	8	—	pF

NOTES:
1. All typical values are at V_{CC} = 3.3V, T_A = 25°C.
2. For additional I_{CC} information, see Figure 1, *Typical Characteristics: Supply Current (I_{CC}) vs. Clock Frequency (fs)*.

DETERMINING ACTIVE CURRENT CONSUMPTION AND POWER DISSIPATION

The $I_{CC(f)}$ current for the graph in Figure 1 was taken while simultaneously reading and writing the FIFO on the IDT72V3612 with CLKA and CLKB set to fs. All data inputs and data outputs change state during each clock cycle to consume the highest supply current. Data outputs were disconnected to normalize the graph to a zero-capacitance load. Once the capacitance load per data-output channel is known, the power dissipation can be calculated with the equation below.

CALCULATING POWER DISSIPATION

With $I_{CC(f)}$ taken from Figure 1, the maximum power dissipation (P_T) of the IDT72V3612 may be calculated by:

$$P_T = V_{CC} \times I_{CC(f)} + \sum_{N}(C_L \times (V_{OH} - V_{OL})^2 \times f_O)$$

where:

N	=	number of outputs = 36
C_L	=	output capacitance load
f_O	=	switching frequency of an output
V_{OH}	=	output HIGH level voltage
V_{OL}	=	output LOW level voltage

When no reads or writes are occurring on this device, the power dissipated by a single clock (CLKA or CLKB) input running at frequency fs is calculated by:

$$P_T = V_{CC} \times f_S \times 0.025 \text{ mA/MHz}$$

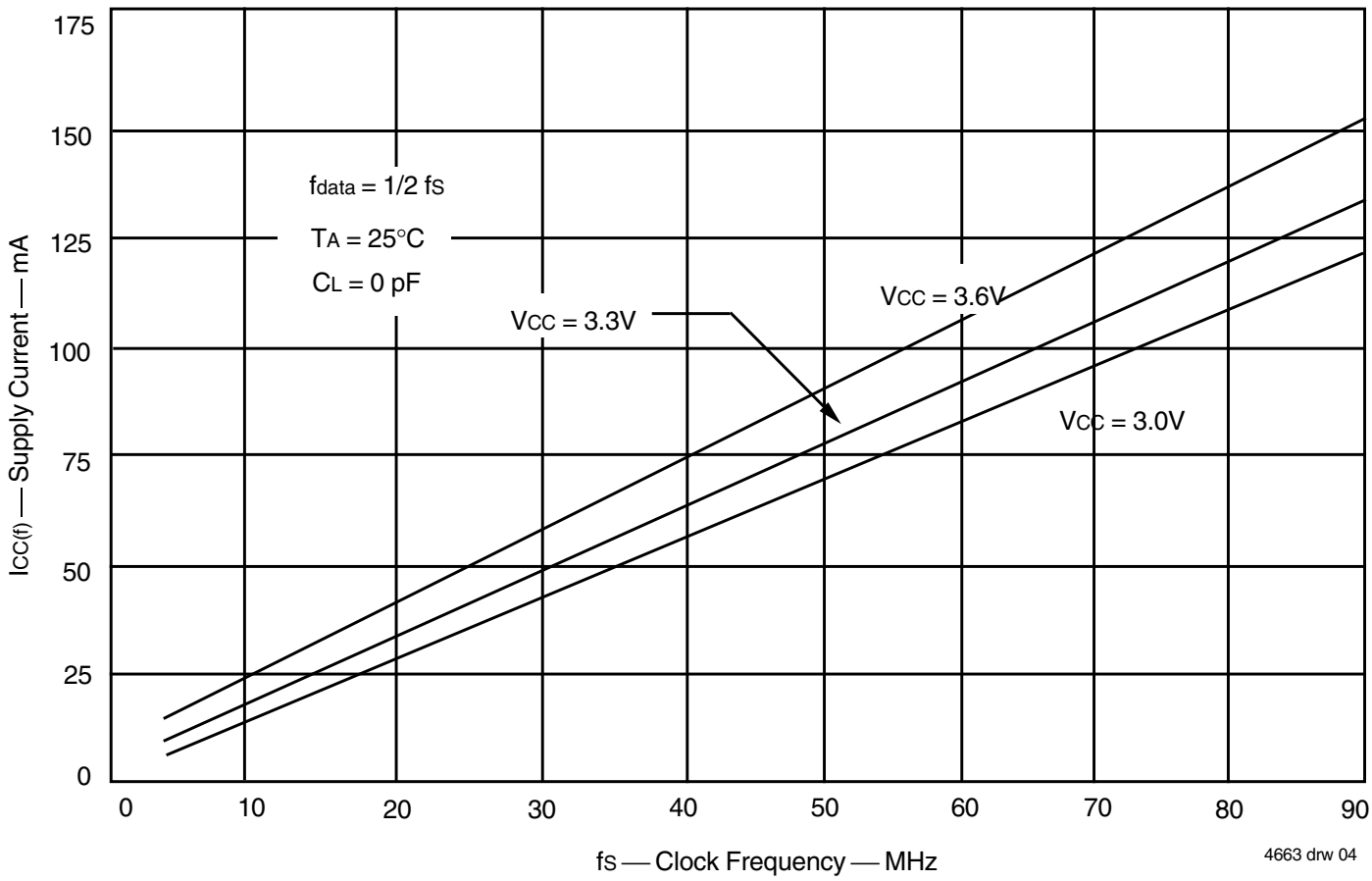


Figure 1. Typical Characteristics: Supply Current (I_{CC}) vs. Clock Frequency (fs)

DC ELECTRICAL CHARACTERISTICS OVER RECOMMENDED RANGES OF SUPPLY VOLTAGE AND OPERATING FREE-AIR TEMPERATURE

Commercial: Vcc=3.3V± 0.30V; for 12ns (83MHz) operation, Vcc=3.3V ±0.15V; T_A = 0° C to +70°C; JEDEC JESD8-A compliant

Symbol	Parameter	IDT72V3612L12		IDT72V3612L15		Unit
		Min.	Max.	Min.	Max.	
f_S	Clock Frequency, CLKA or CLKB	–	83	–	66.7	MHz
t_{CLK}	Clock Cycle Time, CLKA or CLKB	12	–	15	–	ns
t_{CLKH}	Pulse Duration, CLKA and CLKB HIGH	5	–	6	–	ns
t_{CLKL}	Pulse Duration, CLKA and CLKB LOW	5	–	6	–	ns
t_{DS}	Setup Time, A0-A35 before CLKA↑ and B0-B35 before CLKB↑	4	–	4	–	ns
t_{ENS1}	Setup Time, $\overline{CSA}$, W/$\overline{R}$A before CLKA↑; $\overline{CSB}$, W/$\overline{R}$B before CLKB↑	3.5	–	6	–	ns
t_{ENS2}	Setup Time, ENA, before CLKA↑; ENB before CLKB↑	3.5	–	4	–	ns
t_{ENS3}	Setup Time, MBA before CLKA↑: MBB before CLKB↑	3.5	–	4	–	ns
t_{PGS}	Setup Time, ODD/$\overline{EVEN}$ and PGA before CLKA↑; ODD/$\overline{EVEN}$ and PGB before CLKB↑(1)	3	–	4	–	ns
t_{RSTS}	Setup Time, $\overline{RST}$ LOW before CLKA↑ or CLKB↑(2)	4	–	5	–	ns
t_{FSS}	Setup Time, FS0/FS1 before $\overline{RST}$ HIGH	4	–	5	–	ns
t_{DH}	Hold Time, A0-A35 after CLKA↑ and B0-B35 after CLKB↑	0.5	–	1	–	ns
t_{ENH1}	Hold Time, $\overline{CSA}$ W/$\overline{R}$A after CLKA↑; $\overline{CSB}$, W/$\overline{R}$B after CLKB↑	0.5	–	1	–	ns
t_{ENH2}	Hold Time, ENA, after CLKA↑; ENB after CLKB↑	1	–	1	–	ns
t_{ENH3}	Hold Time, MBA after CLKA↑; MBB after CLKB↑	1	–	1	–	ns
t_{PGH}	Hold Time, ODD/$\overline{EVEN}$ and PGA after CLKA↑; ODD/$\overline{EVEN}$ and PGB after CLKB↑(1)	0	–	1	–	ns
t_{RSTH}	Hold Time, $\overline{RST}$ LOW after CLKA↑ or CLKB↑(2)	4	–	5	–	ns
t_{FSH}	Hold Time, FS0 and FS1 after $\overline{RST}$ HIGH	4	–	4	–	ns
t_{SKEW1}(3)	Skew Time, between CLKA↑ and CLKB↑ for $\overline{EFA}$, EFB, $\overline{FFA}$, and $\overline{FFB}$	5.5	–	8	–	ns
t_{SKEW2}(3,4)	Skew Time, between CLKA↑ and CLKB↑ for $\overline{AEA}$, $\overline{AEB}$, $\overline{AFA}$, and $\overline{AFB}$	14	–	14	–	ns

NOTES:
1. Only applies for a clock edge that does a FIFO read.
2. Requirement to count the clock edge as one of at least four needed to reset a FIFO.
3. Skew time is not a timing constraint for proper device operation and is only included to illustrate the timing relationship between CLKA cycle and CLKB cycle.
4. Design simulated, not tested.

SWITCHING CHARACTERISTICS OVER RECOMMENDED RANGES OF SUPPLY VOLTAGE AND OPERATING FREE-AIR TEMPERATURE, C_L = 30pF

Commercial: Vcc=3.3V± 0.30V; for 12ns (83MHz) operation, Vcc=3.3V ±0.15V; T_A = 0°C to +70°C; JEDEC JESD8-A compliant

Symbol	Parameter	IDT72V3612L12		IDT72V3612L15		Unit
		Min.	Max.	Min.	Max.	
t_A	Access Time, CLKA↑ to A0-A35 and CLKB↑ to B0-B35	1	8	2	10	ns
t_{WFF}	Propagation Delay Time, CLKA↑ to $\overline{FFA}$ and CLKB↑ to $\overline{FFB}$	1	8	2	10	ns
t_{REF}	Propagation Delay Time, CLKA↑ to $\overline{EFA}$ and CLKB↑ to $\overline{EFB}$	1	8	2	10	ns
t_{PAE}	Propagation Delay Time, CLKA↑ to $\overline{AEA}$ and CLKB↑ to $\overline{AEB}$	1	8	2	10	ns
t_{PAF}	Propagation Delay Time, CLKA↑ to $\overline{AFA}$ and CLKB↑ to $\overline{AFB}$	1	8	2	10	ns
t_{PMF}	Propagation Delay Time, CLKA↑ to $\overline{MBF1}$ LOW or $\overline{MBF2}$ HIGH and CLKB↑ to $\overline{MBF2}$ LOW or $\overline{MBF1}$ HIGH	1	8	1	9	ns
t_{PMR}	Propagation Delay Time, CLKA↑ to B0-B35[1] and CLKB↑ to A0-A35[2]	2	8	2	10	ns
t_{MDV}	Propagation Delay Time, MBA to A0-A35 valid and MBB to B0-B35 valid	1	8	1	10	ns
t_{PDPE}	Propagation Delay Time, A0-A35 valid to $\overline{PEFA}$ valid; B0-B35 valid to $\overline{PEFB}$ valid	2	8	2	10	ns
t_{POPE}	Propagation Delay Time, ODD/$\overline{EVEN}$ to $\overline{PEFA}$ and $\overline{PEFB}$	2	8	2	10	ns
t_{POPB}[3]	Propagation Delay Time, ODD/$\overline{EVEN}$ to parity bits (A8, A17, A26, A35) and (B8, B17, B26, B35)	2	8	2	10	ns
t_{PEPE}	Propagation Delay Time, W/$\overline{RA}$, $\overline{CSA}$, ENA, MBA or PGA to $\overline{PEFA}$; W/$\overline{RB}$, $\overline{CSB}$, ENB. MBB, PGB to $\overline{PEFB}$	1	8	1	10	ns
t_{PEPB}[3]	Propagation Delay Time, W/$\overline{RA}$, $\overline{CSA}$, ENA, MBA or PGA to parity bits (A8, A17, A26, A35); W/$\overline{RB}$, $\overline{CSB}$, ENB. MBB or PGB to parity bits (B8, B17, B26, B35)	2	8	2	10	ns
t_{RSF}	Propagation Delay Time, $\overline{RST}$ to ($\overline{AEA}$, $\overline{AEB}$) LOW and ($\overline{AFA}$, $\overline{AFB}$, $\overline{MBF1}$, $\overline{MBF2}$) HIGH	1	10	1	15	ns
t_{EN}	Enable Time, $\overline{CSA}$ and W/$\overline{RA}$ LOW to A0-A35 active and $\overline{CSB}$ $\overline{LOW}$ and W/$\overline{RB}$ HIGH to B0-B35 active	2	6	2	10	ns
t_{DIS}	Disable Time, $\overline{CSA}$ or W/$\overline{RA}$ HIGH to A0-A35 at high-impedance and $\overline{CSB}$ HIGH or W/$\overline{RB}$ LOW to B0-B35 at high impedance	1	6	1	8	ns

NOTES:
1. Writing data to the mail1 register when the B0-B35 outputs are active and MBB is HIGH.
2. Writing data to the mail2 register when the A0-A35 outputs are active and MBA is HIGH.
3. Only applies when reading data from a mail register.

SIGNAL DESCRIPTIONS

RESET

The IDT72V3612 is reset by taking the Reset ($\overline{RST}$) input LOW for at least four port A Clock (CLKA) and four port B Clock (CLKB) LOW-to-HIGH transitions. The Reset input can switch asynchronously to the clocks. A device reset initializes the internal read and write pointers of each FIFO and forces the Full Flags ($\overline{FFA}$, $\overline{FFB}$) LOW, the Empty Flags ($\overline{EFA}$, $\overline{EFB}$) LOW, the Almost-Empty flags ($\overline{AEA}$, $\overline{AEB}$) LOW and the Almost-Full flags ($\overline{AFA}$, $\overline{AFB}$) HIGH. A reset also forces the Mailbox Flags ($\overline{MBF1}$, $\overline{MBF2}$) HIGH. After a reset, $\overline{FFA}$ is set HIGH after two LOW-to-HIGH transitions of CLKA and $\overline{FFB}$ is set HIGH after two LOW-to-HIGH transitions of CLKB. The device must be reset after power up before data is written to its memory.

A LOW-to-HIGH transition on the $\overline{RST}$ input loads the Almost-Full and Almost-Empty registers (X) with the values selected by the Flag Select (FS0, FS1) inputs. The values that can be loaded into the registers are shown in Table 1. For the relevant Reset and preset value loading timing diagram, see Figure 2.

TABLE 1 – FLAG PROGRAMMING

FS1	FS0	$\overline{RST}$	ALMOST-FULL AND ALMOST-EMPTY FLAG OFFSET REGISTER (X)
H	H	↑	16
H	L	↑	12
L	H	↑	8
L	L	↑	4

FIFO WRITE/READ OPERATION

The state of port A data A0-A35 outputs is controlled by the port A Chip Select ($\overline{CSA}$) and the port A Write/Read select (W/$\overline{RA}$). The A0-A35 outputs are in the high-impedance state when either $\overline{CSA}$ or W/$\overline{RA}$ is HIGH. The A0-A35 outputs are active when both $\overline{CSA}$ and W/$\overline{RA}$ are LOW.

Data is loaded into FIFO1 from the A0-A35 inputs on a LOW-to-HIGH transition of CLKA when $\overline{CSA}$ is LOW, W/$\overline{RA}$ is HIGH, ENA is HIGH, MBA is LOW, and $\overline{FFA}$ is HIGH. Data is read from FIFO2 to the A0-A35 outputs by a LOW-to-HIGH transition of CLKA when $\overline{CSA}$ is LOW, W/$\overline{RA}$ is LOW, ENA is HIGH, MBA is LOW, and $\overline{EFA}$ is HIGH (see Table 2). Relevant Write and Read timing diagrams for Port A can be found in Figure 3 and Figure 6.

The port B control signals are identical to those of port A. The state of the port B data (B0-B35) outputs is controlled by the port B Chip Select ($\overline{CSB}$) and the port B Write/Read select (W/$\overline{RB}$). The B0-B35 outputs are in the high-impedance state when either $\overline{CSB}$ or W/$\overline{RB}$ is HIGH. The B0-B35 outputs are active when both $\overline{CSB}$ and W/$\overline{RB}$ are LOW.

Data is loaded into FIFO2 from the B0-B35 inputs on a LOW-to-HIGH transition of CLKB when $\overline{CSB}$ is LOW, W/$\overline{RB}$ is HIGH, ENB is HIGH, MBB is LOW, and $\overline{FFB}$ is HIGH. Data is read from FIFO1 to the B0-B35 outputs by a LOW-to-HIGH transition of CLKB when $\overline{CSB}$ is LOW, W/$\overline{RB}$ is LOW, ENB is HIGH, MBB is LOW, and $\overline{EFB}$ is HIGH (see Table 3). Relevant Write and Read timing diagrams for Port B can be found in Figure 4 and Figure 5.

The setup and hold time constraints to the port clocks for the port Chip Selects ($\overline{CSA}$, $\overline{CSB}$) and Write/Read selects (W/$\overline{RA}$, W/$\overline{RB}$) are only for enabling write

TABLE 2 – PORT-A ENABLE FUNCTION TABLE

$\overline{CSA}$	W/$\overline{RA}$	ENA	MBA	CLKA	Data A (A0-A35) I/O	Port Functions
H	X	X	X	X	Input	None
L	H	L	X	X	Input	None
L	H	H	L	↑	Input	FIFO1 Write
L	H	H	H	↑	Input	Mail1 Write
L	L	L	L	X	Output	None
L	L	H	L	↑	Output	FIFO2 Read
L	L	L	H	X	Output	None
L	L	H	H	↑	Output	Mail2 Read (Set $\overline{MBF2}$ HIGH)

TABLE 3 – PORT-B ENABLE FUNCTION TABLE

$\overline{CSB}$	W/$\overline{RB}$	ENB	MBB	CLKB	Data B (B0-B35) I/O	Port Functions
H	X	X	X	X	Input	None
L	H	L	X	X	Input	None
L	H	H	L	↑	Input	FIFO2 Write
L	H	H	H	↑	Input	Mail2 Write
L	L	L	L	X	Output	None
L	L	H	L	↑	Output	FIFO1 read
L	L	L	H	X	Output	None
L	L	H	H	↑	Output	Mail1 Read (Set $\overline{MBF1}$ HIGH)

and read operations and are not related to high-impedance control of the data outputs. If a port enable is LOW during a clock cycle, the port chip select and write/read select may change states during the setup and hold time window of the cycle.

SYNCHRONIZED FIFO FLAGS

Each FIFO is synchronized to its port clock through two flip-flop stages. This is done to improve flag reliability by reducing the probability of metastable events on the output when CLKA and CLKB operate asynchronously to one another. $\overline{EFA}$, $\overline{AEA}$, $\overline{FFA}$, and $\overline{AFA}$ are synchronized by CLKA. $\overline{EFB}$, $\overline{AEB}$, $\overline{FFB}$, and $\overline{AFB}$ are synchronized to CLKB. Tables 4 and 5 show the relationship of each port flag to the level of FIFO1 and FIFO2 fill.

EMPTY FLAGS ($\overline{EFA}$, $\overline{EFB}$)

The Empty Flag of a FIFO is synchronized to the port clock that reads data from its array. When the Empty Flag is HIGH, new data can be read to the FIFO output register. When the Empty Flag is LOW, the FIFO is empty and attempted FIFO reads are ignored.

The read pointer of a FIFO is incremented each time a new word is clocked to the output register. The state machine that controls an Empty Flag monitors a write-pointer and read-pointer comparator that indicates when the FIFO memory status is empty, empty+1, or empty+2. A word written to a FIFO can be read to the FIFO output register in a minimum of three cycles of the Empty Flag synchronizing clock. Therefore, an Empty Flag is LOW if a word in memory is the next data to be sent to the FIFO output register and two cycles of the port clock that reads data from the FIFO have not elapsed since the time the word was written. The Empty Flag of the FIFO is set HIGH by the second LOW-to-HIGH transition of the synchronizing clock, and the new data word can be read to the FIFO output register in the following cycle.

A LOW-to-HIGH transition on an Empty Flag synchronizing clock begins the first synchronization cycle of a write if the clock transition occurs at time t_{SKEW1} or greater after the write. Otherwise, the subsequent clock cycle can be the first synchronization cycle (see Figure 7 and Figure 8).

FULL FLAG ($\overline{FFA}$, $\overline{FFB}$)

The Full Flag of a FIFO is synchronized to the port clock that writes data to its array. When the Full Flag is HIGH, a memory location is free in the FIFO to receive new data. No memory locations are free when the Full Flag is LOW and attempted writes to the FIFO are ignored.

Each time a word is written to a FIFO, the write pointer is incremented. The state machine that controls a Full Flag monitors a write-pointer and read pointer comparator that indicates when the FIFO memory status is full, full-1, or full-2. From the time a word is read from a FIFO, the previous memory location is ready to be written in a minimum of three cycles of the Full Flag synchronizing clock. Therefore, a Full Flag is LOW if less than two cycles of the Full Flag synchronizing clock have elapsed since the next memory write location has been read. The second LOW-to-HIGH transition on the Full Flag synchronization clock after the read sets the Full Flag HIGH and the data can be written in the following clock cycle.

A LOW-to-HIGH transition on a Full Flag synchronizing clock begins the first synchronization cycle of a read if the clock transition occurs at time t_{SKEW1} or greater after the read. Otherwise, the subsequent clock cycle can be the first synchronization cycle (see Figure 9 and Figure 10).

ALMOST EMPTY FLAGS ($\overline{AEA}$, $\overline{AEB}$)

The Almost-Empty flag of a FIFO is synchronized to the port clock that reads data from its array. The state machine that controls an Almost-Empty flag monitors a write-pointer comparator that indicates when the FIFO memory status is almost-empty, almost-empty+1, or almost-empty+2. The almost-empty state is defined by the value of the Almost-Full and Almost-Empty Offset register (X). This register is loaded with one of four preset values during a device reset (see Reset section). An Almost-Empty flag is LOW when the FIFO contains X or less words in memory and is HIGH when the FIFO contains (X+1) or more words.

Two LOW-to-HIGH transitions of the Almost-Empty flag synchronizing clocks are required after a FIFO write for the Almost-Empty flag to reflect the new level of fill. Therefore, the Almost-Empty flag of a FIFO containing (X+1) or more words remains LOW if two cycles of the synchronizing clock have not elapsed since the write that filled the memory to the (X+1) level. An Almost-Empty flag is set HIGH by the second LOW-to-HIGH transition of the synchronizing clock after the FIFO write that fills memory to the (X+1) level. A LOW-to-HIGH transition of an Almost-Empty flag synchronizing clock begins the first synchronization cycle if it occurs at time t_{SKEW2} or greater after the write that fills the FIFO to (X+1) words. Otherwise, the subsequent synchronizing clock cycle can be the first synchronization cycle (see Figure 11 and 12).

ALMOST FULL FLAGS ($\overline{AFA}$, $\overline{AFB}$)

The Almost-Full flag of a FIFO is synchronized to the port clock that writes data to its array. The state machine that controls an Almost-Full flag monitors a write-pointer and read-pointer comparator that indicates when the FIFO memory status is almost-full, almost-full-1, or almost-full-2. The almost-full state is defined by the value of the Almost-Full and Almost-Empty Offset register (X). This register is loaded with one of four preset values during a device reset (see Reset section). An Almost-Full flag is LOW when the FIFO contains (64-

TABLE 4 – FIFO1 FLAG OPERATION

Number of Words in the FIFO1[1]	Synchronized to CLKB		Synchronized to CLKA	
	$\overline{EFB}$	$\overline{AEB}$	$\overline{AFA}$	$\overline{FFA}$
0	L	L	H	H
1 to X	H	L	H	H
(X+1) to [64-(X+1)]	H	H	H	H
(64-X) to 63	H	H	L	H
64	H	H	L	L

TABLE 5 – FIFO2 FLAG OPERATION

Number of Words in the FIFO2[1]	Synchronized to CLKB		Synchronized to CLKA	
	$\overline{EFA}$	$\overline{AEA}$	$\overline{AFB}$	$\overline{FFB}$
0	L	L	H	H
1 to X	H	L	H	H
(X+1) to [64-(X+1)]	H	H	H	H
(64-X) to 63	H	H	L	H
64	H	H	L	L

NOTE:
1. X is the value in the Almost-Empty flag and Almost-Full flag offset register.

X) or more words in memory and is HIGH when the FIFO contains [64-(X+1)] or less words.

Two LOW-to-HIGH transitions of the Almost-Full flag synchronizing clock are required after a FIFO read for the Almost-Full flag to reflect the new level of fill. Therefore, the Almost-Full flag of a FIFO containing [64-(X+1)] or less words remains LOW if two cycles of the synchronizing clock have not elapsed since the read that reduced the number of words in memory to [64-(X+1)]. An Almost-Full flag is set HIGH by the second LOW-to-HIGH transition of the synchronizing clock after the FIFO read that reduces the number of words in memory to [64-(X+1)]. A second LOW-to-HIGH transition of an Almost-Full flag synchronizing clock begins the first synchronization cycle if it occurs at time t_{SKEW2} or greater after the read that reduces the number of words in memory to [64-(X+1)]. Otherwise, the subsequent synchronizing clock cycle can be the first synchronization cycle (see Figure 13 and 14).

MAILBOX REGISTERS

Each FIFO has a 36-bit bypass register to pass command and control information between port A and port B without putting it in queue. The Mailbox select (MBA, MBB) inputs choose between a mail register and a FIFO for a port data transfer operation. A LOW-to-HIGH transition on CLKA writes A0-A35 data to the mail1 register when a port A write is selected by $\overline{CSA}$, W/$\overline{RA}$, and ENA and MBA HIGH. A LOW-to-HIGH transition on CLKB writes B0-B35 data to the mail2 register when a port B write is selected by $\overline{CSB}$, W/$\overline{RB}$, and ENB and MBB is HIGH. Writing data to a mail register sets the corresponding flag ($\overline{MBF1}$ or $\overline{MBF2}$) LOW. Attempted writes to a mail register are ignored while the mail flag is LOW.

When a port's data outputs are active, the data on the bus comes from the FIFO output register when the port Mailbox select input (MBA, MBB) is LOW and from the mail register when the port mailbox select input is HIGH. The Mail1 register Flag ($\overline{MBF1}$) is set HIGH by a LOW-to-HIGH transition on CLKB when a port B read is selected by $\overline{CSB}$, W/$\overline{RB}$, and ENB and MBB is HIGH. The Mail2 register Flag ($\overline{MBF2}$) is set HIGH by a LOW-to-HIGH transition on CLKA when port A read is selected by $\overline{CSA}$, W/$\overline{RA}$, and ENA and MBA is HIGH. The data in a mail register remains intact after it is read and changes only when new data is written to the register. Mail register and Mail Register Flag timing can be found in Figure 15 and Figure 16.

PARITY CHECKING

The port A inputs (A0-A35) and port B inputs (B0-B35) each have four parity trees to check the parity of incoming (or outgoing) data. A parity failure on one or more bytes of the input bus is reported by a LOW level on the port Parity Error Flag ($\overline{PEFA}$, $\overline{PEFB}$). Odd or even parity checking can be selected, and the Parity Error Flags can be ignored if this feature is not desired.

Parity status is checked on each input bus according to the level of the Odd/Even parity (ODD/$\overline{EVEN}$) select input. A parity error on one or more bytes of a port is reported by a LOW level on the corresponding port Parity Error Flag ($\overline{PEFA}$, $\overline{PEFB}$) output. Port A bytes are arranged as A0-A8, A9-A17, A18-A26, and A27-A35 with the most significant bit of each byte used as the parity bit. Port B bytes are arranged as B0-B8, B9-B17, B18-B26, and B27-B35, with the most significant bit of each byte used as the parity bit. When odd/even parity is selected, a port Parity Error Flag ($\overline{PEFA}$, $\overline{PEFB}$) is LOW if any byte on the port has an odd/even number of LOW levels applied to the bits.

The four parity trees used to check the A0-A35 inputs are shared by the mail2 register when parity generation is selected for port A reads (PGA = HIGH). When a port A read from the mail2 register with parity generation is selected with W/$\overline{RA}$ LOW, $\overline{CSA}$ LOW, ENA HIGH, MBA HIGH, and PGA HIGH, the port A Parity Error Flag ($\overline{PEFA}$) is held HIGH regardless of the levels applied to the A0-A35 inputs. Likewise, the parity trees used to check the B0-B35 inputs are shared by the mail1 register when parity generation is selected for port B reads (PGB = HIGH). When a port B read from the mail1 register with parity generation is selected with W/$\overline{RB}$ LOW, $\overline{CSB}$ LOW, ENB HIGH, MBB HIGH, and PGB HIGH, the port B Parity Error Flag ($\overline{PEFB}$) is held HIGH regardless of the levels applied to the B0-B35 inputs (see Figure 17 and Figure 18).

PARITY GENERATION

A HIGH level on the port A Parity Generate select (PGA) or port B Parity Generate select (PGB) enables the IDT72V3612 to generate parity bits for port reads from a FIFO or mailbox register. Port A bytes are arranged as A0-A8, A9-A17, A18-26, and A27-A35, with the most significant bit of each byte used as the parity bit. Port B bytes are arranged as B0-B8, B9-B17, B18-B26, and B27-B35, with the most significant bit of each byte used as the parity bit. A write to a FIFO or mail register stores the levels applied to all thirty-six inputs regardless of the state of the Parity Generate select (PGA, PGB) inputs. When data is read from a port with parity generation selected, the lower eight bits of each byte are used to generate a parity bit according to the level on the ODD/$\overline{EVEN}$ select. The generated parity bits are substituted for the levels originally written to the most significant bits of each byte as the word is read to the data outputs.

Parity bits for FIFO data are generated after the data is read from SRAM and before the data is written to the output register. Therefore, the port A Parity Generate select (PGA) and Odd/Even parity select (ODD/$\overline{EVEN}$) have setup and hold time constraints to the port A Clock (CLKA) and the port B Parity Generate select (PGB) and ODD/$\overline{EVEN}$ have setup and hold-time constraints to the port B Clock (CLKB). These timing constraints only apply for a rising clock edge used to read a new word to the FIFO output register.

The circuit used to generate parity for the mail1 data is shared by the port B bus (B0-B35) to check parity and the circuit used to generate parity for the mail2 data is shared by the port A bus (A0-A35) to check parity. The shared parity trees of a port are used to generate parity bits for the data in a mail register when the port Write/Read select (W/$\overline{RA}$, W/$\overline{RB}$) input is LOW, the port Mail select (MBA, MBB) input is HIGH, Chip Select ($\overline{CSA}$, $\overline{CSB}$) is LOW, Enable (ENA, ENB) is HIGH, and port Parity Generate select (PGA, PGB) is HIGH. Generating parity for mail register data does not change the contents of the register (see Figure 19 and Figure 20).

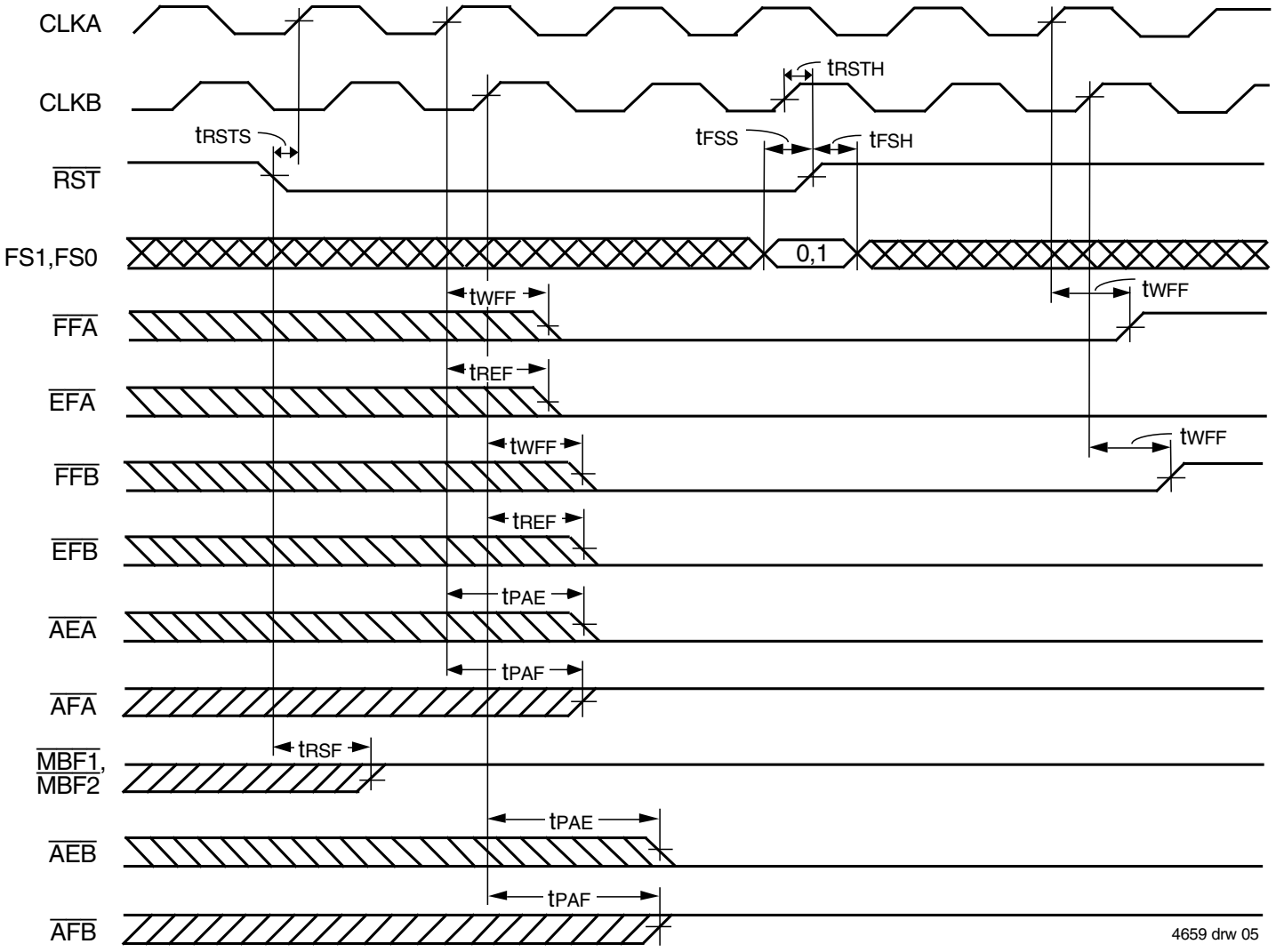
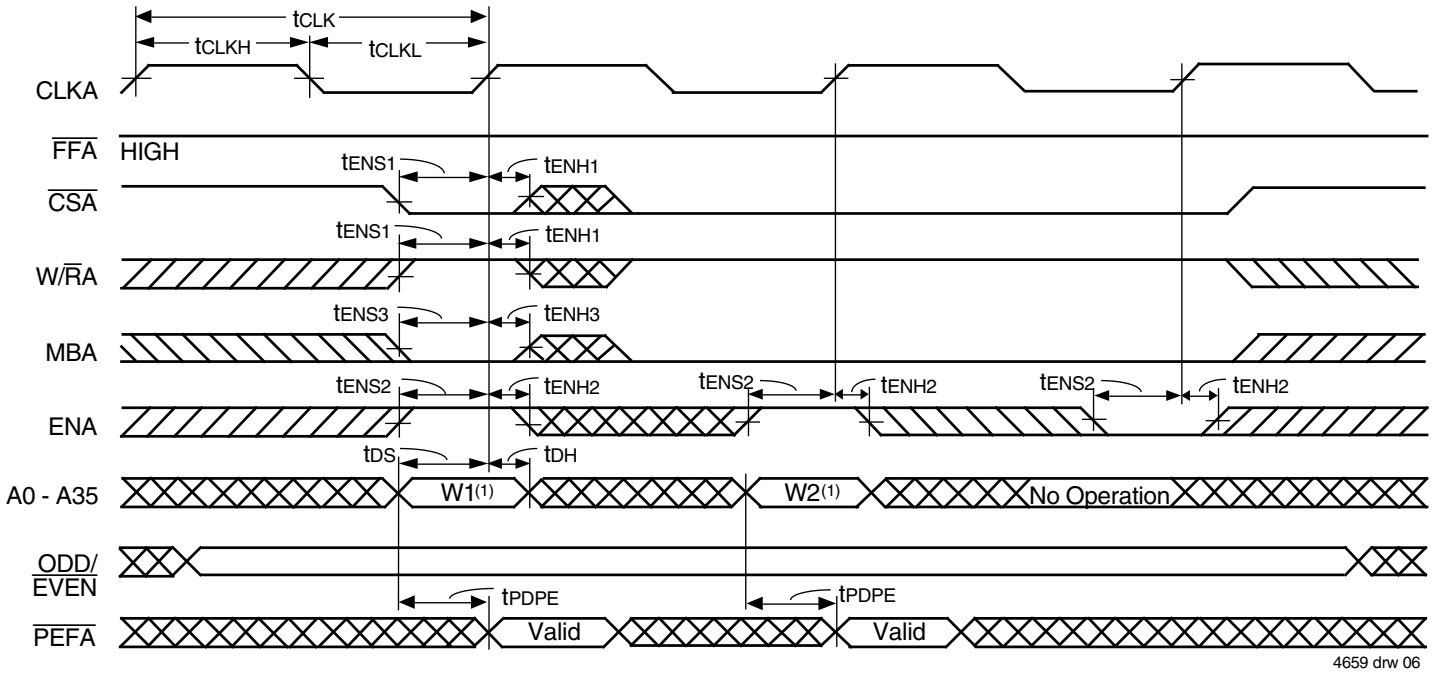
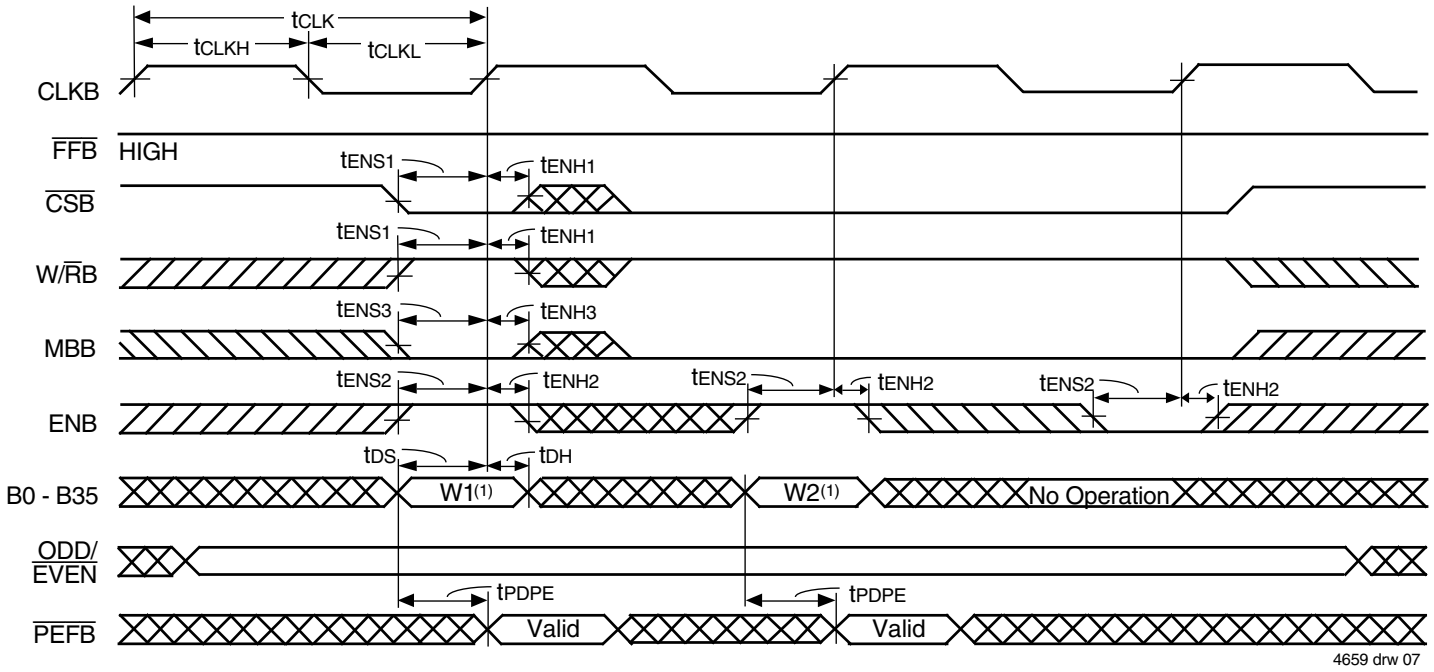


Figure 2. Device Reset and Loading the X Register with the Value of Eight



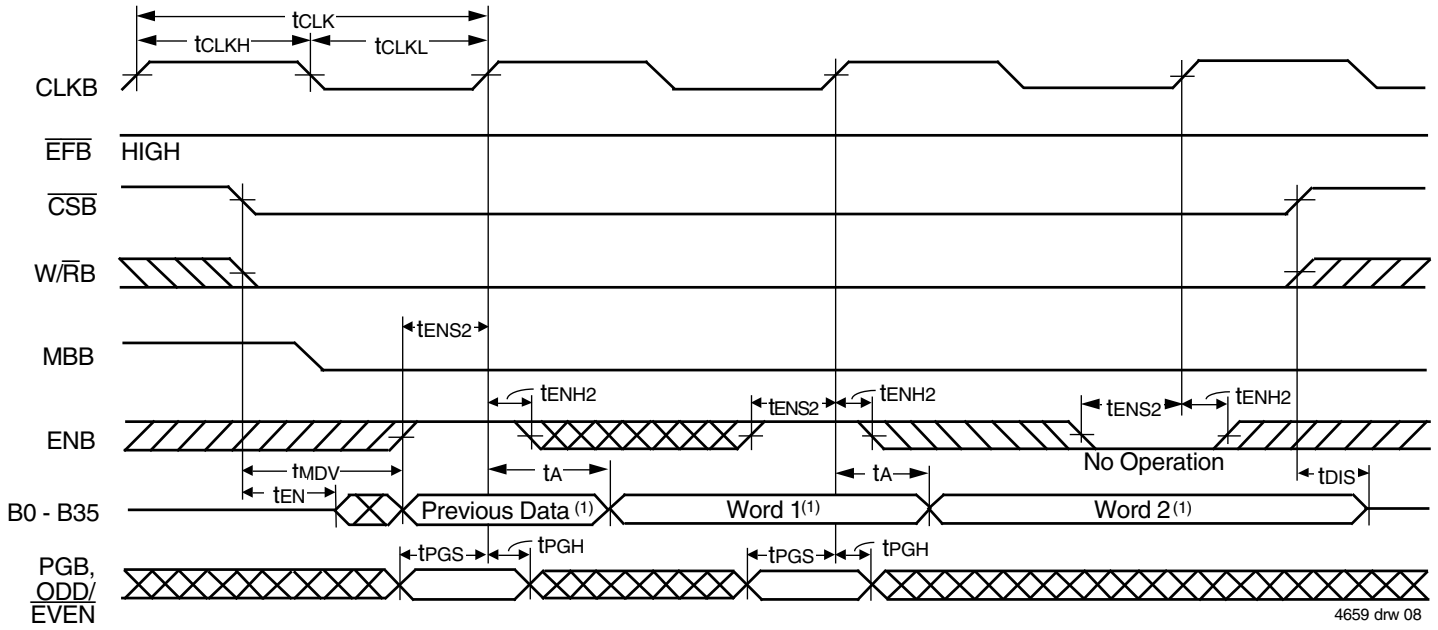
NOTE:
1. Written to FIFO1.

Figure 3. Port A Write Cycle Timing for FIFO1



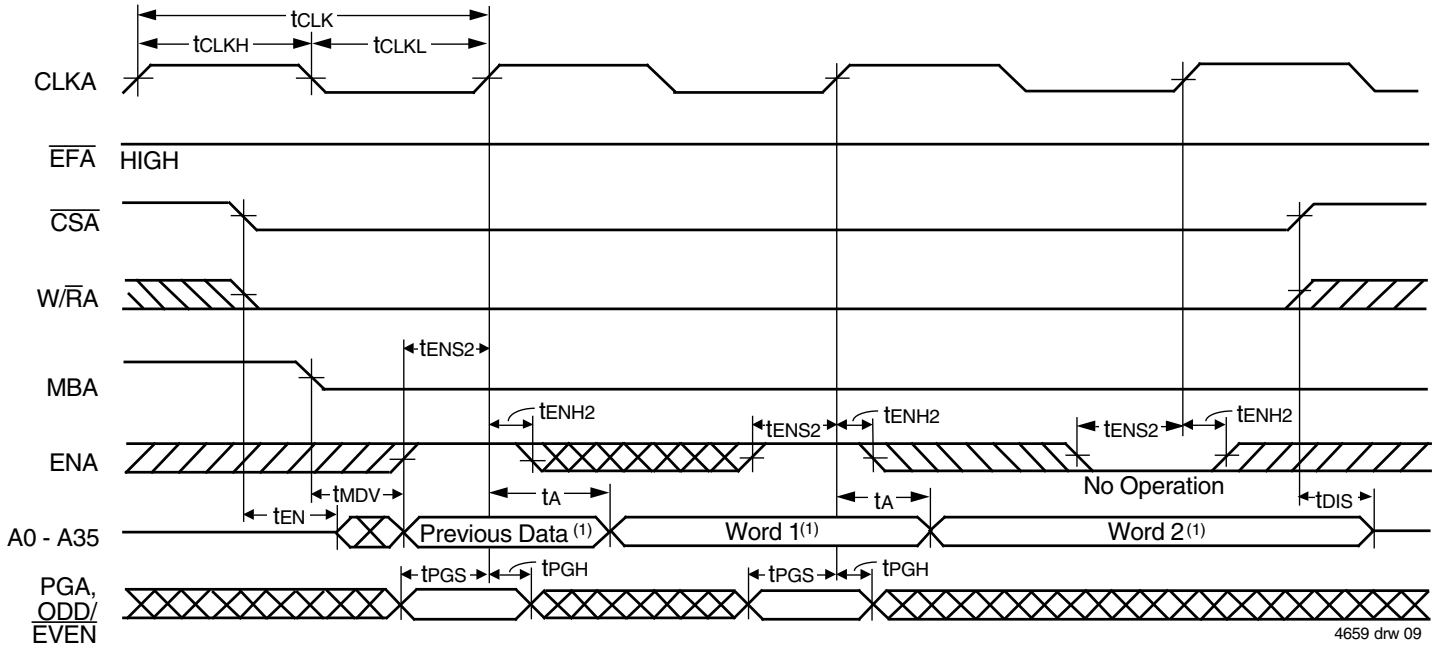
NOTE:
1. Written to FIFO2.

Figure 4. Port B Write Cycle Timing for FIFO2



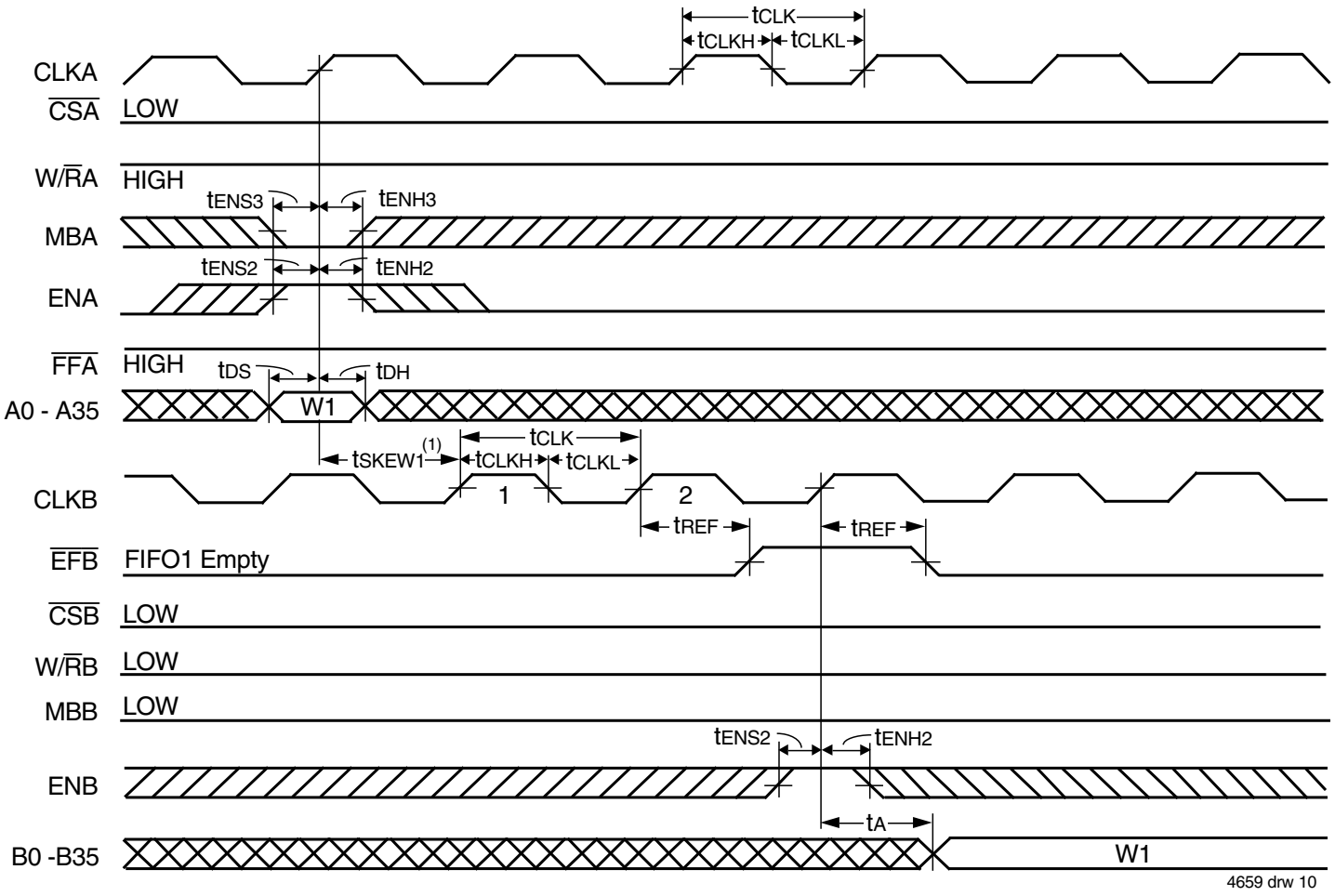
NOTE:
1. Read from FIFO1.

Figure 5. Port B Read Cycle Timing for FIFO1



NOTE:
1. Read from FIFO2.

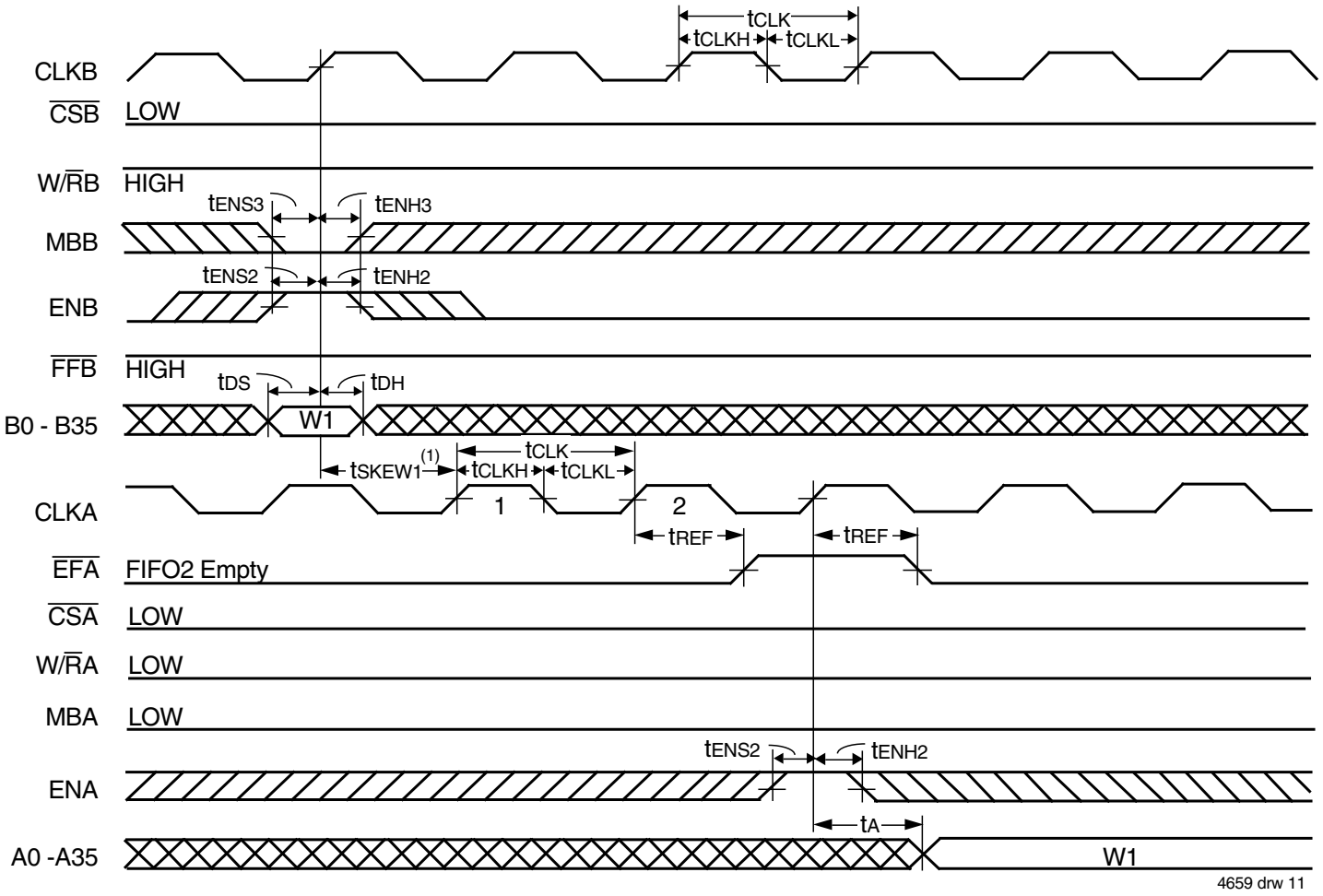
Figure 6. Port A Read Cycle Timing for FIFO2



NOTE:

1. t_{SKEW1} is the minimum time between a rising CLKA edge and a rising CLKB edge for $\overline{EFB}$ to transition HIGH in the next CLKB cycle. If the time between the rising CLKA edge and rising CLKB edge is less than t_{SKEW1}, then the transition of $\overline{EFB}$ HIGH may occur one CLKB cycle later than shown.

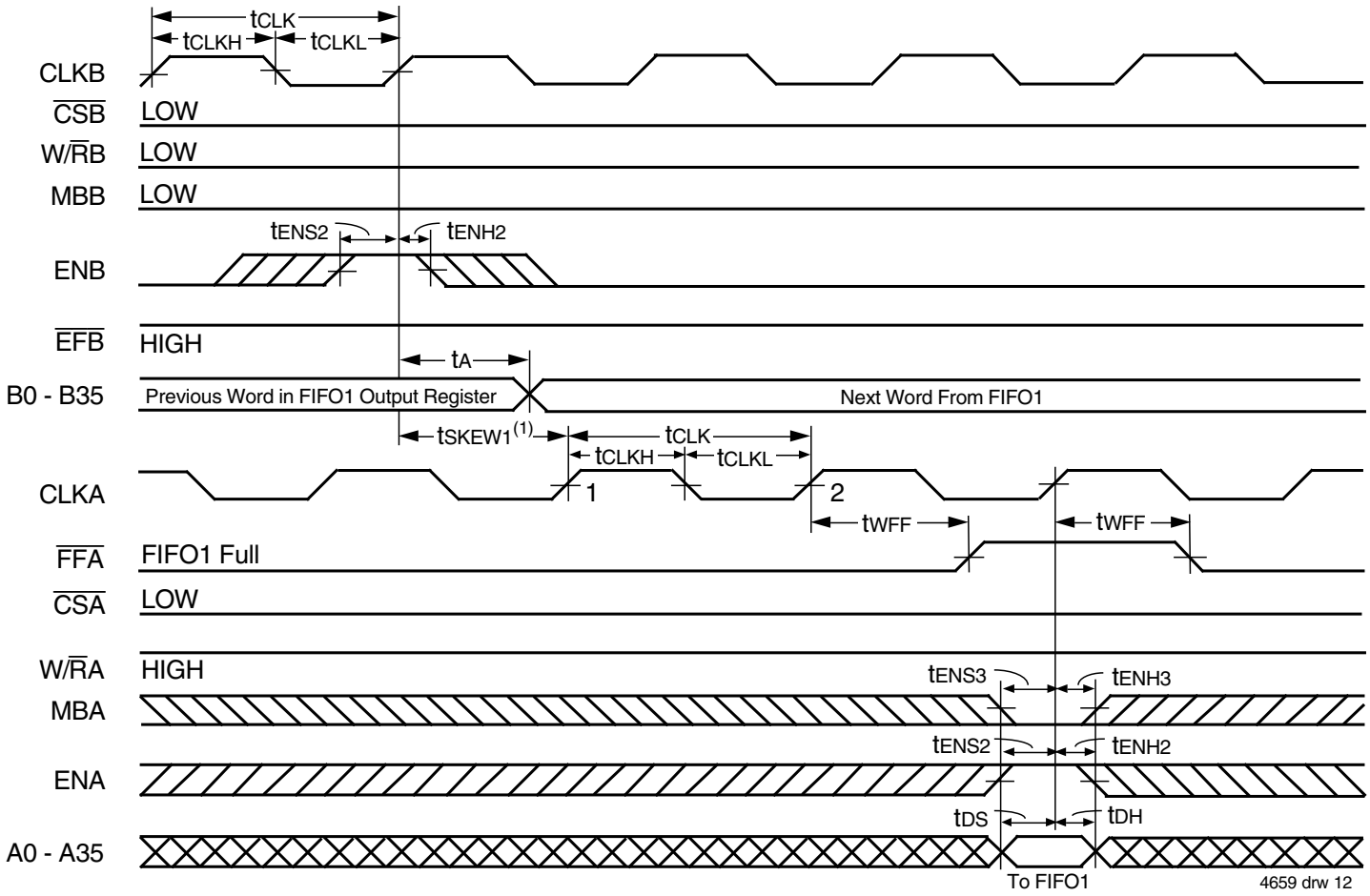
Figure 7. $\overline{EFB}$ Flag Timing and First Data Read when FIFO1 is Empty



NOTE:

1. t_{SKEW1} is the minimum time between a rising CLKB edge and a rising CLKA edge for $\overline{EFA}$ to transition HIGH in the next CLKA cycle. If the time between the rising CLKB edge and rising CLKA edge is less than t_{SKEW1}, then the transition of $\overline{EFA}$ HIGH may occur one CLKA cycle later than shown.

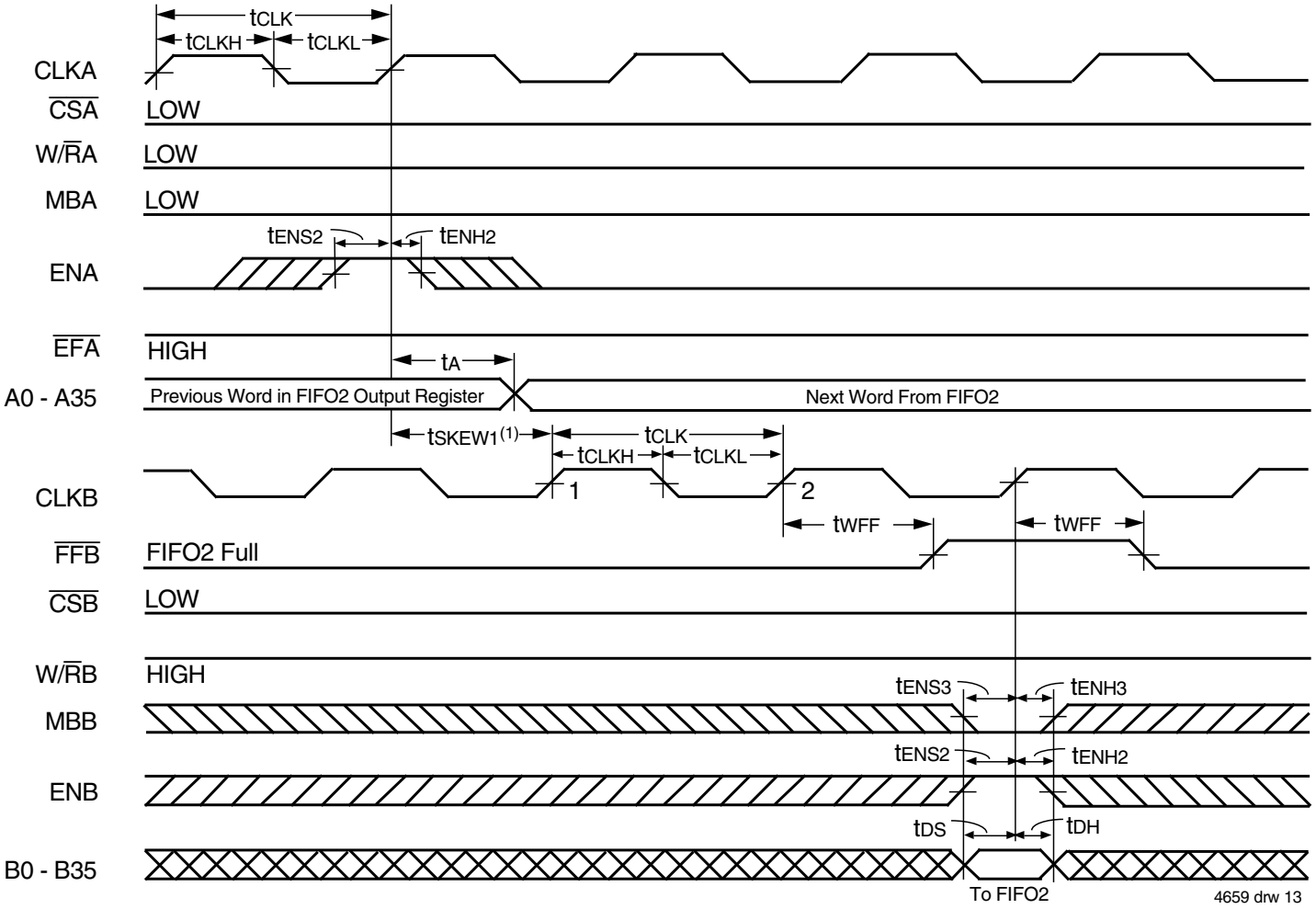
Figure 8. $\overline{EFA}$ Flag Timing and First Data Read when FIFO2 is Empty



NOTE:

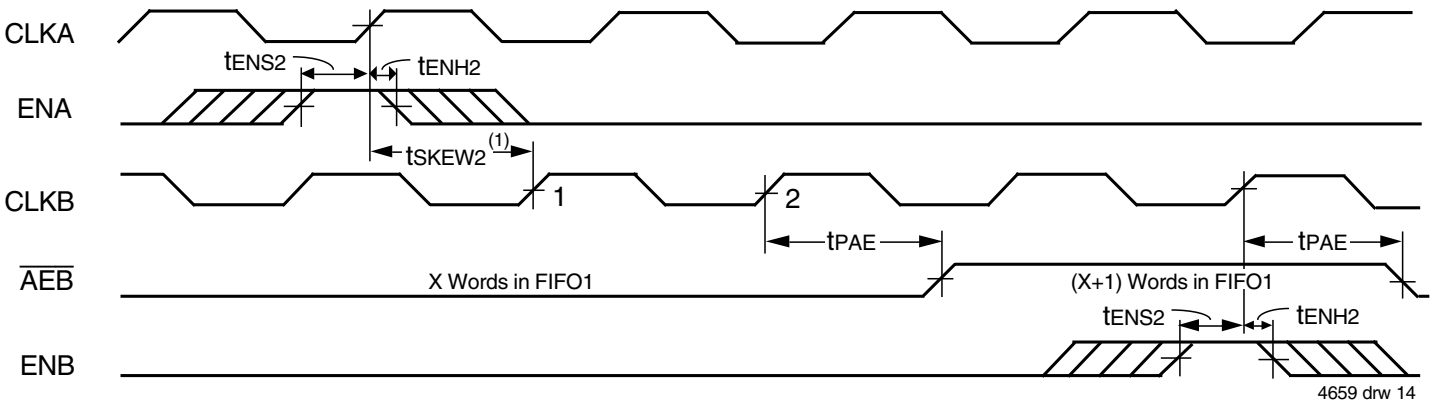
1. t_{SKEW1} is the minimum time between a rising CLKB edge and a rising CLKA edge for $\overline{FFA}$ to transition HIGH in the next CLKA cycle. If the time between the rising CLKB edge and rising CLKA edge is less than t_{SKEW1}, then $\overline{FFA}$ may transition HIGH one CLKA cycle later than shown.

Figure 9. $\overline{FFA}$ Flag Timing and First Available Write when FIFO1 is Full.



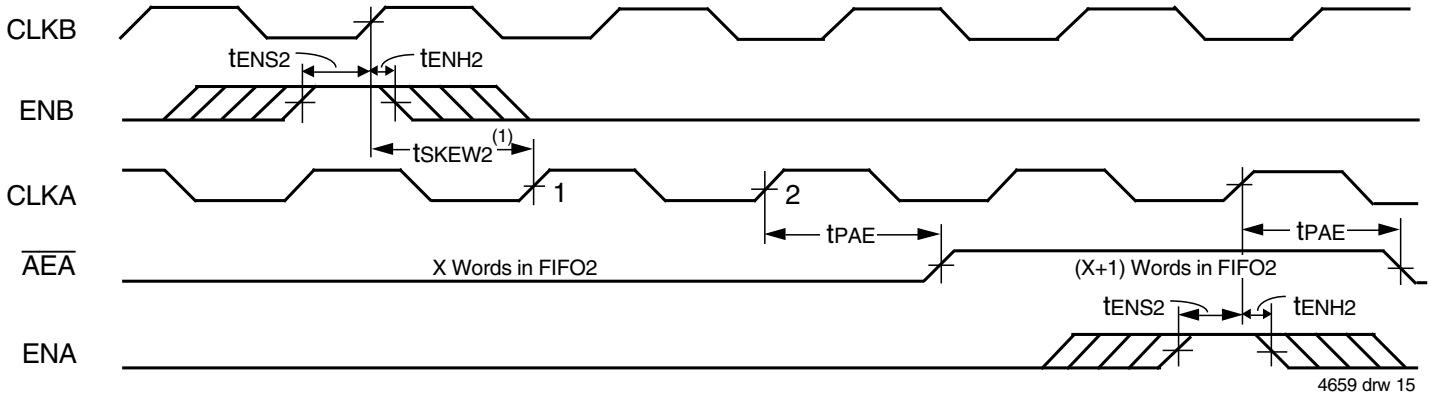
NOTE:
1. t_{SKEW1} is the minimum time between a rising CLKA edge and a rising CLKB edge for $\overline{FFB}$ to transition HIGH in the next CLKB cycle. If the time between the rising CLKA edge and rising CLKB edge is less than t_{SKEW1}, then $\overline{FFB}$ may transition HIGH one CLKB cycle later than shown.

Figure 10. $\overline{FFB}$ Flag Timing and First Available Write when FIFO2 is Full



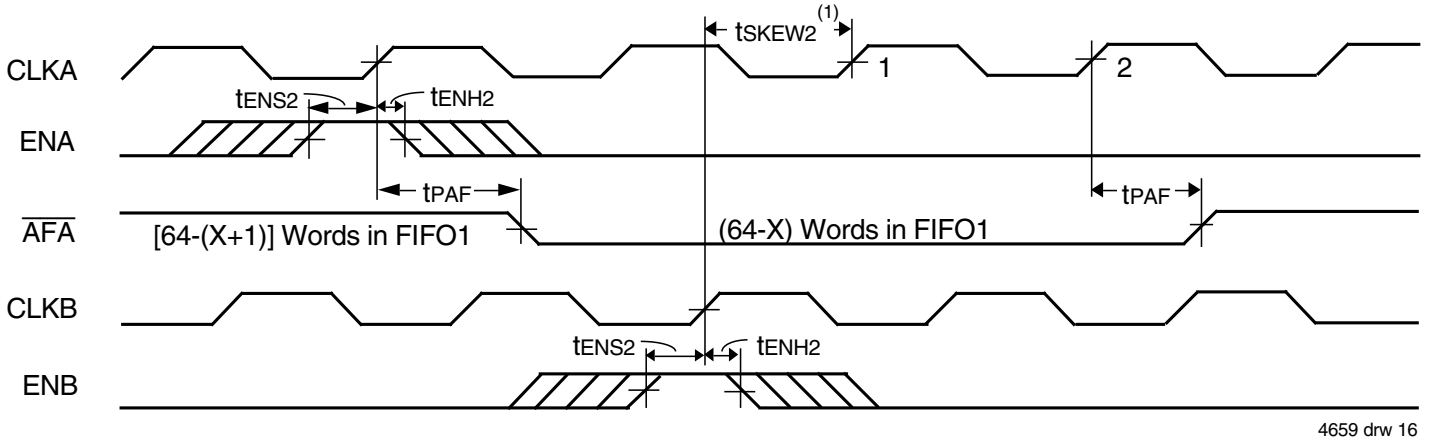
NOTES:
1. t_{SKEW2} is the minimum time between a rising CLKA edge and a rising CLKB edge for $\overline{AEB}$ to transition HIGH in the next CLKB cycle. If the time between the rising CLKA edge and rising CLKB edge is less than t_{SKEW2}, then $\overline{AEB}$ may transition HIGH one CLKB cycle later than shown.
2. FIFO1 Write ($\overline{CSA}$ = LOW, W/$\overline{RA}$ = HIGH, MBA = LOW), FIFO1 read ($\overline{CSB}$ = LOW, W/$\overline{RB}$ = LOW, MBB = LOW).

Figure 11. Timing for $\overline{AEB}$ when FIFO1 is Almost Empty



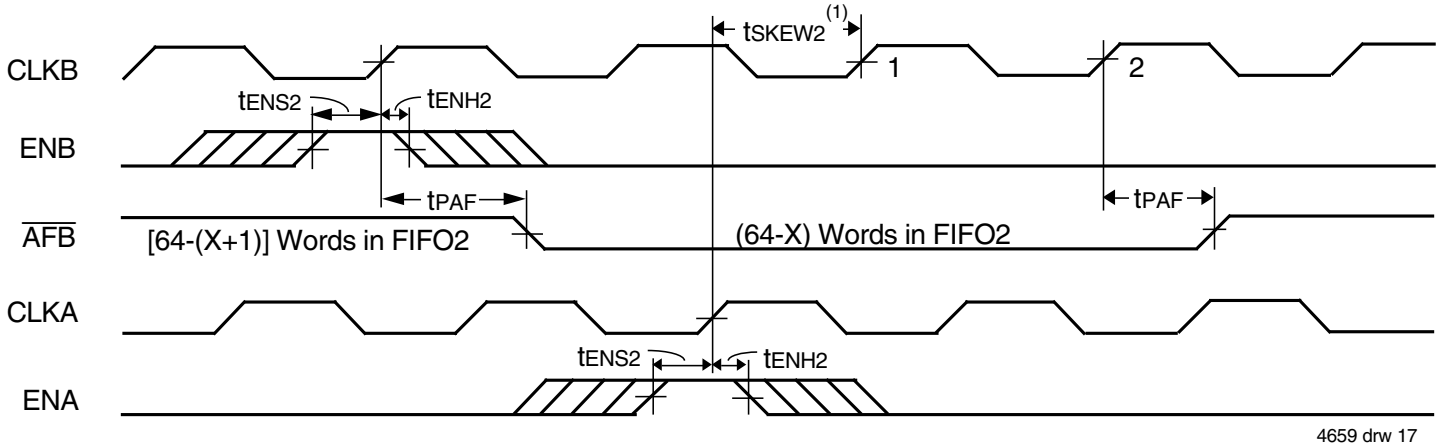
NOTES:
1. t_{SKEW2} is the minimum time between a rising CLKB edge and a rising CLKA edge for $\overline{AEA}$ to transition HIGH in the next CLKA cycle. If the time between the rising CLKB edge and rising CLKA edge is less than t_{SKEW2}, then $\overline{AEA}$ may transition HIGH one CLKA cycle later than shown.
2. FIFO2 Write ($\overline{CSB}$ = LOW, W/$\overline{RB}$ = HIGH, MBB = LOW), FIFO2 read ($\overline{CSA}$ = LOW, W/$\overline{RA}$ = LOW, MBA = LOW).

Figure 12. Timing for $\overline{AEA}$ when FIFO2 is Almost Empty



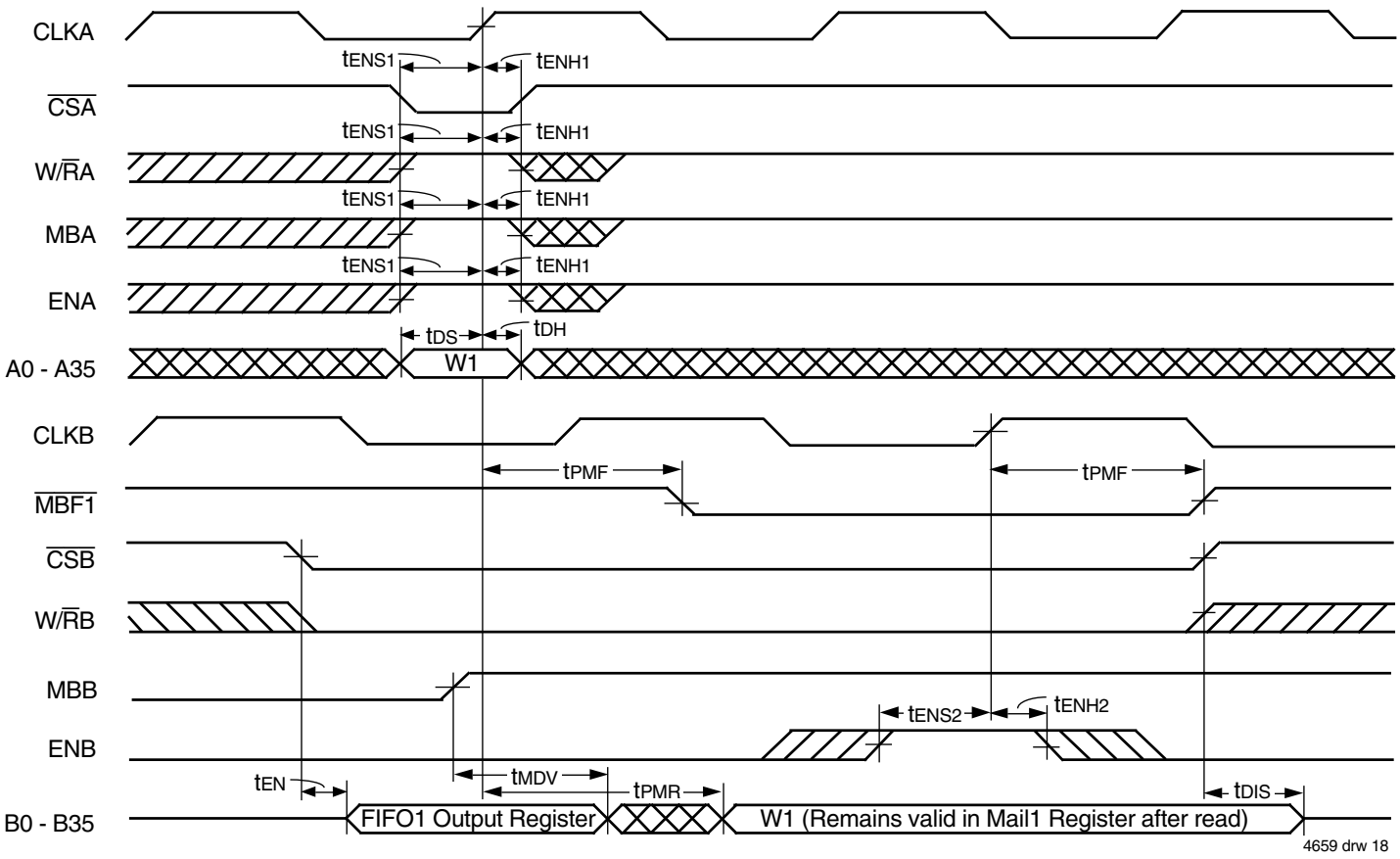
NOTES:
1. t_{SKEW2} is the minimum time between a rising CLKA edge and a rising CLKB edge for $\overline{AFA}$ to transition HIGH in the next CLKA cycle. If the time between the rising CLKA edge and rising CLKB edge is less than t_{SKEW2}, then $\overline{AFA}$ may transition HIGH one CLKA cycle later than shown.
2. FIFO1 Write ($\overline{CSA}$ = LOW, W/$\overline{RA}$ = HIGH, MBA = LOW), FIFO1 read ($\overline{CSB}$ = LOW, W/$\overline{RB}$ = LOW, MBB = LOW).

Figure 13. Timing for $\overline{AFA}$ when FIFO1 is Almost Full



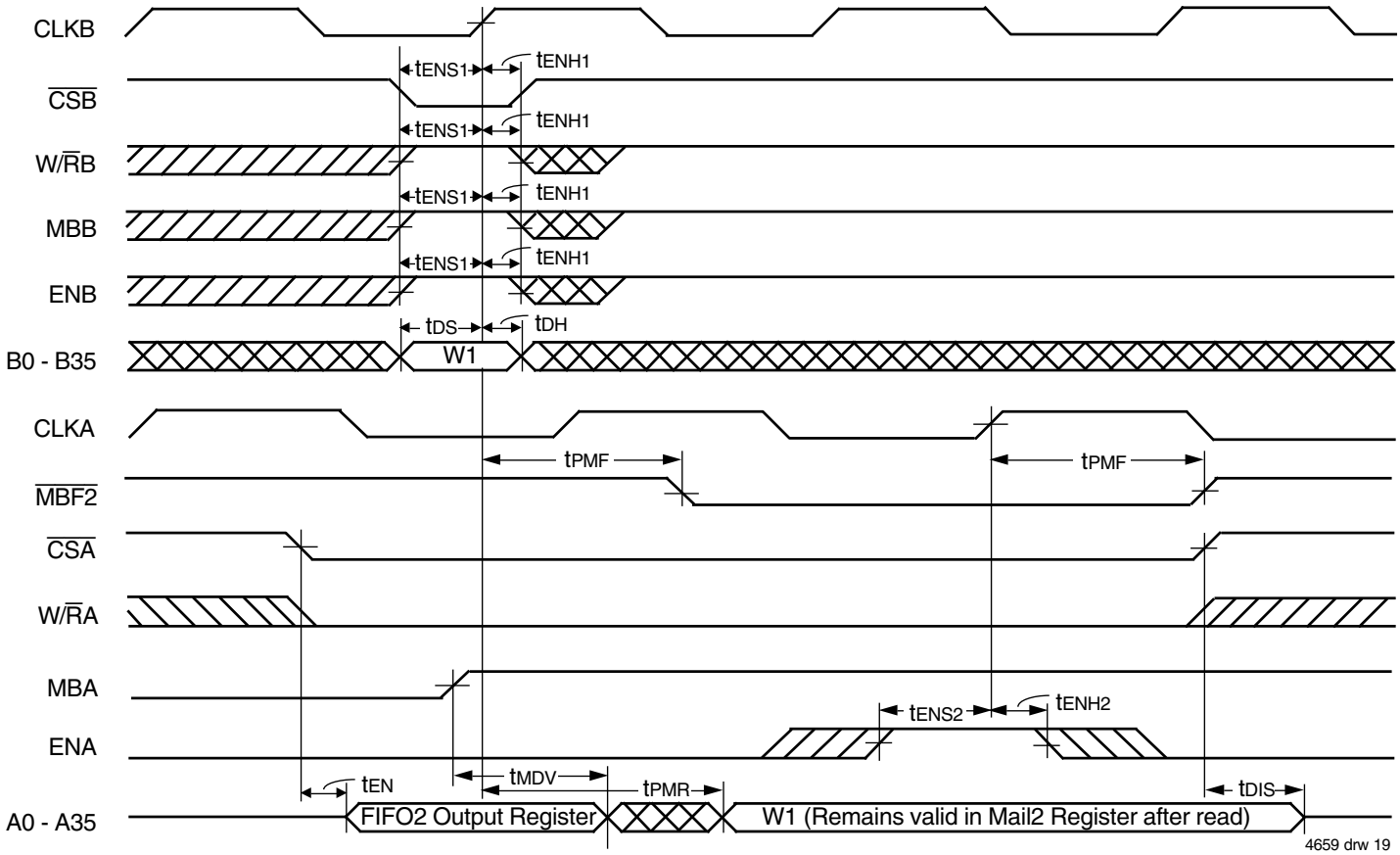
NOTES:
1. t_{SKEW2} is the minimum time between a rising CLKB edge and a rising CLKA edge for $\overline{AFB}$ to transition HIGH in the next CLKB cycle. If the time between the rising CLKB edge and rising CLKA edge is less than t_{SKEW2}, then $\overline{AFB}$ may transition HIGH one CLKB cycle later than shown.
2. FIFO2 Write ($\overline{CSB}$ = LOW, W/$\overline{RB}$ = HIGH, MBB = LOW), FIFO2 read ($\overline{CSA}$ = LOW, W/$\overline{RA}$ = LOW, MBA = LOW).

Figure 14. Timing for $\overline{AFB}$ when FIFO2 is Almost Full



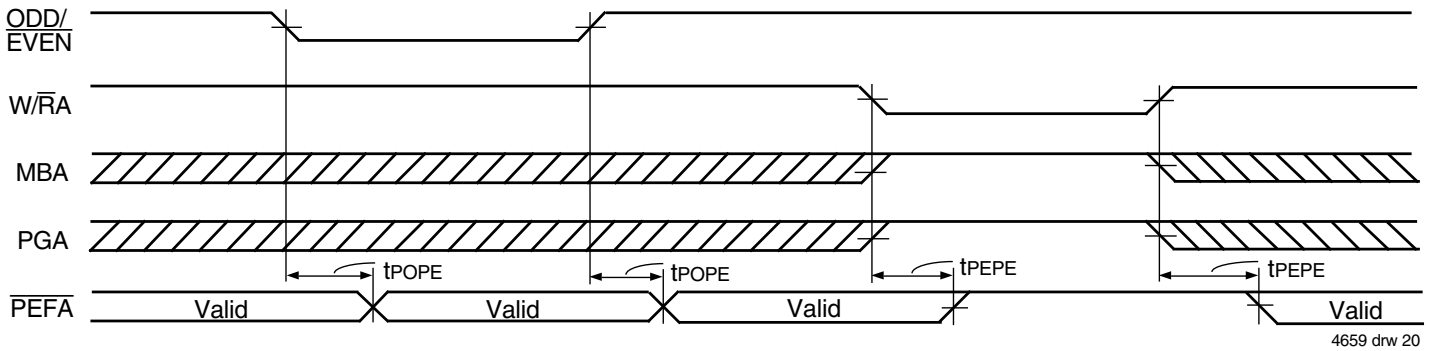
NOTE:
1. Port B parity generation off (PGB = LOW).

Figure 15. Timing for Mail1 Register and $\overline{\text{MBF1}}$ Flag



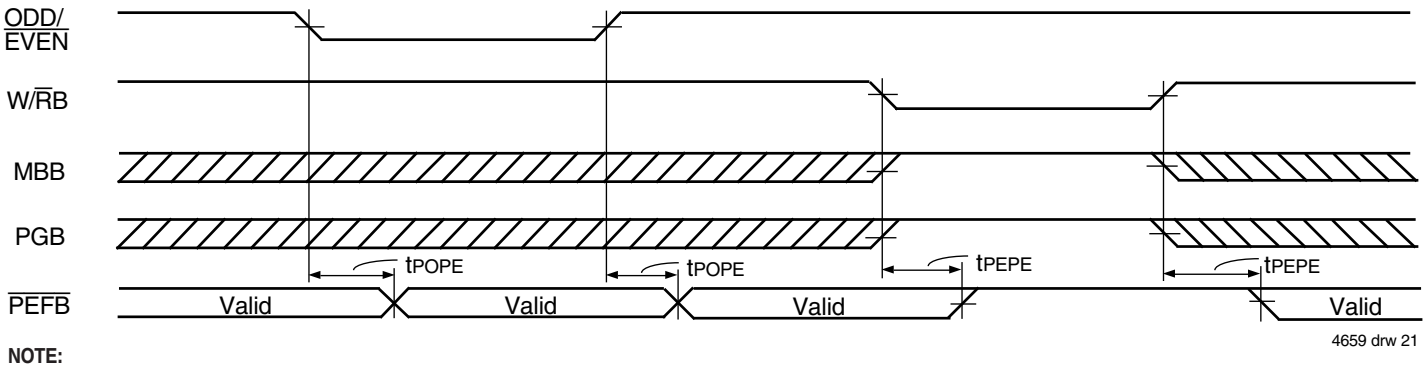
NOTE:
1. Port A parity generation off (PGA = LOW).

Figure 16. Timing for Mail2 Register and $\overline{MBF2}$ Flag



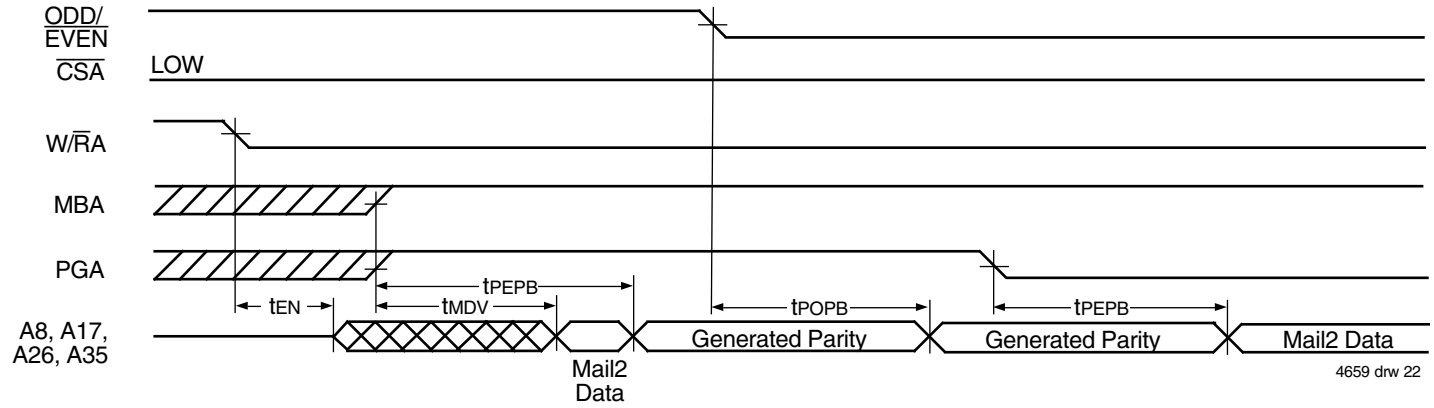
NOTE:
1. ENA is HIGH, and $\overline{CSA}$ is LOW.

Figure 17. ODD/$\overline{EVEN}$ W/RA, MBA, and PGA to $\overline{PEFA}$ Timing



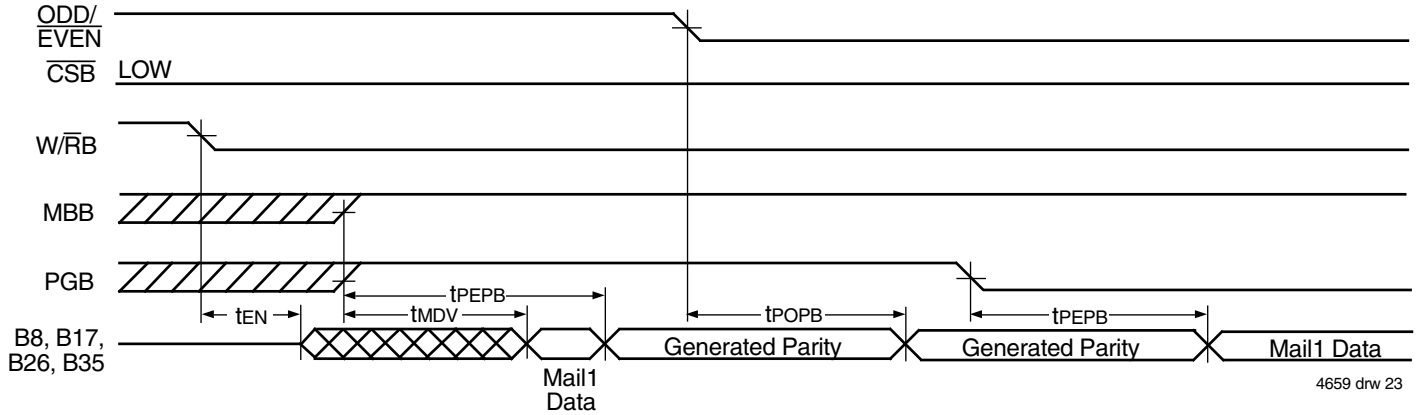
NOTE:
1. ENB is HIGH, and CSB is LOW.

Figure 18. ODD/EVEN W/RB, MBB, and PGB to PEFB Timing



NOTE:
1. ENA is HIGH.

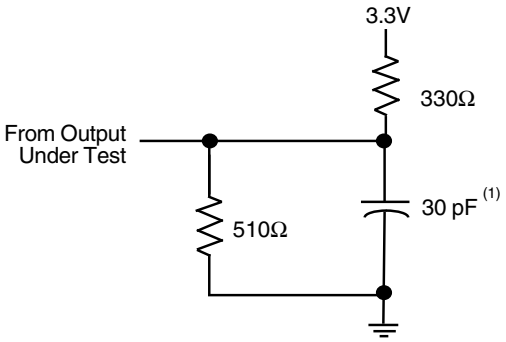
Figure 19. Parity Generation Timing when Reading from Mail2 Register



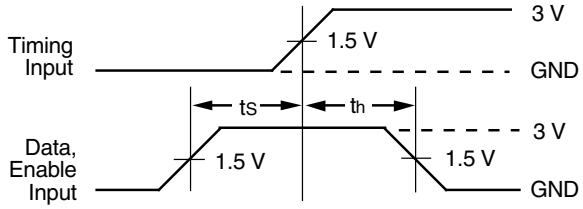
NOTE:
1. ENB is HIGH.

Figure 20. Parity Generation Timing when Reading from Mail1 Register

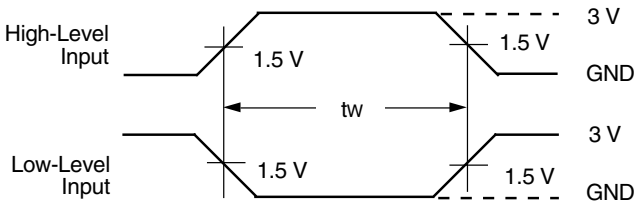
PARAMETER MEASUREMENT INFORMATION



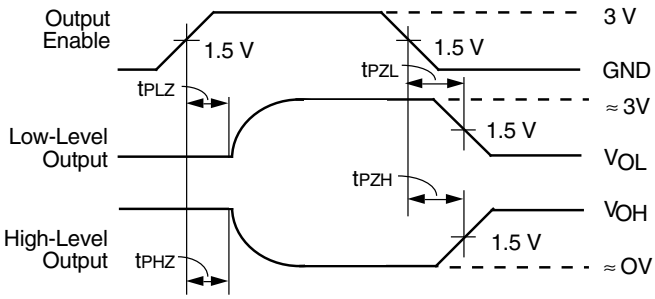
LOAD CIRCUIT



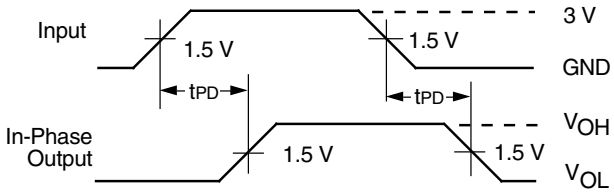
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES



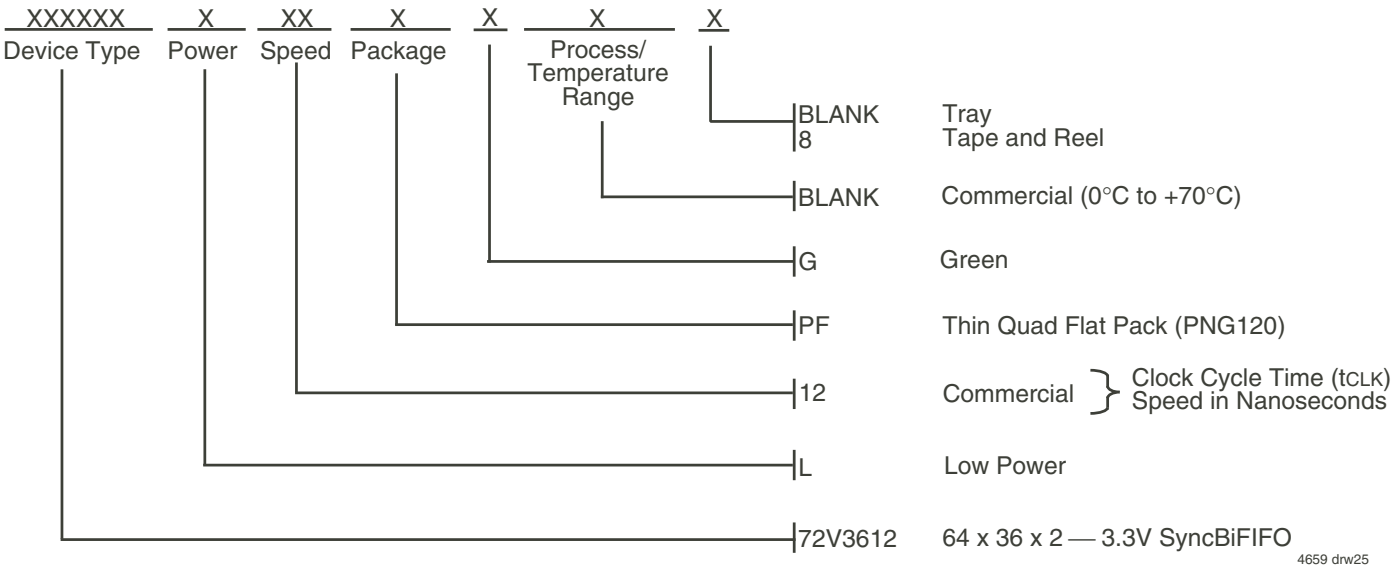
VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

4659 drw 24

NOTE:
1. Includes probe and jig capacitance

Figure 21. Load Circuit and Voltage Waveforms

ORDERING INFORMATION



ORDERABLE PART INFORMATION

Speed (ns)	Orderable Part ID	Pkg. Code	Pkg. Type	Temp. Grade
12	72V3612L12PFG	PNG120	TQFP	C

DATASHEET DOCUMENT HISTORY

07/10/2000 pg. 1.
05/27/2003 pg. 6.
06/08/2005 pgs. 1, 2, 3 and 25.
02/12/2009 pg. 25.
11/11/2013 pgs. 1, 2, 5, 7, 8, 10, 11 and 24.
01/09/2014 pg. 2.
08/22/2019 pgs. 2 and 24.
02/19/2020 pgs. 1-25.

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers skilled in the art designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only for development of an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising out of your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Rev.1.0 Mar 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
www.renesas.com/contact/

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

© 2020 Renesas Electronics Corporation. All rights reserved.