3.3 VOLT CMOS SyncFIFO™ WITH BUS-MATCHING

2,048 x 36 — ***IDT72V3653***

4,096 x 36 — ***IDT72V3663***

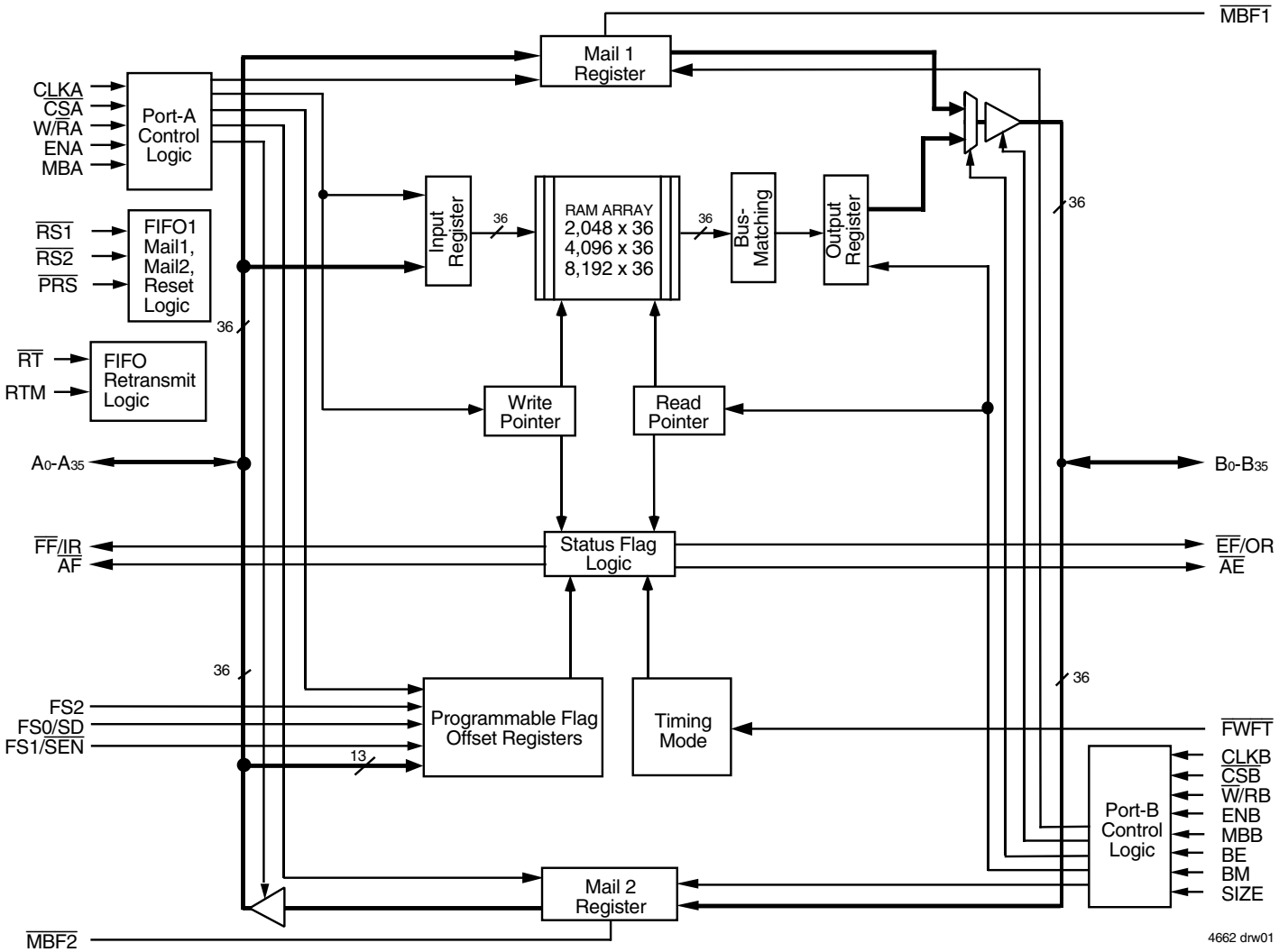
8,192 x 36 — ***IDT72V3673***

LEAD FINISH (SnPb) ARE IN EOL PROCESS - LAST TIME BUY EXPIRES JUNE 15, 2018

FEATURES

- **Memory storage capacity:**
  - **IDT72V3653 – 2,048 x 36**
  - **IDT72V3663 – 4,096 x 36**
  - **IDT72V3673 – 8,192 x 36**
- **Clock frequencies up to 100 MHz (6.5 ns access time)**
- **Clocked FIFO buffering data from Port A to Port B**
- **IDT Standard timing (using $\overline{EF}$ and $\overline{FF}$) or First Word Fall Through Timing (using OR and IR flag functions)**
- **Programmable Almost-Empty and Almost-Full flags; each has five default offsets (8, 16, 64, 256 and 1,024)**
- **Serial or parallel programming of partial flags**
- **Port B bus sizing of 36 bits (long word), 18 bits (word) and 9 bits (byte)**
- **Big- or Little-Endian format for word and byte bus sizes**
- **Retransmit Capability**
- **Reset clears data and configures FIFO, Partial Reset clears data but retains configuration settings**
- **Mailbox bypass registers for each FIFO**
- **Free-running CLKA and CLKB may be asynchronous or coincident (simultaneous reading and writing of data on a single clock edge is permitted)**
- **Easily expandable in width and depth**
- **Auto power down minimizes power dissipation**
- **Available in a space-saving 128-pin Thin Quad Flatpack (TQFP)**
- **Pin and functionally compatible versions of the 5V operating IDT723653/723663/723673**
- **Pin compatible with the lower density parts, IDT72V3623/72V3633/72V3643**
- **Industrial temperature range (–40°C to +85°C) is available**
- **Green parts available, see ordering information**

FUNCTIONAL BLOCK DIAGRAM



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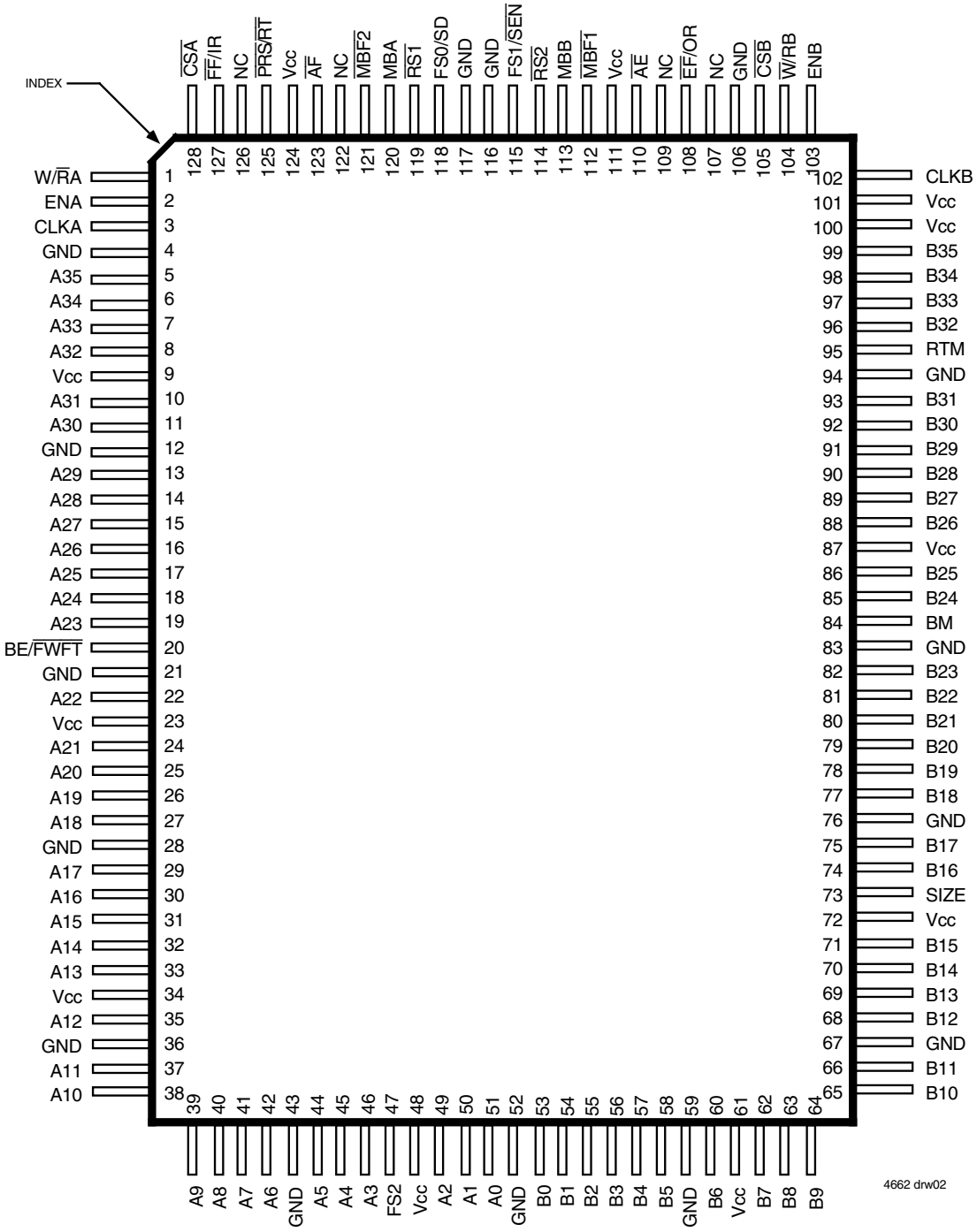
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DESCRIPTION

The IDT72V3653/72V3663/72V3673 are pin and functionally compatible versions of the IDT723653/723663/723673, designed to run off a 3.3V supply for exceptionally low power consumption. These devices are monolithic, high-speed, low-power, CMOS unidirectional Synchronous (clocked) FIFO memory which supports clock frequencies up to 100 MHz and has read access times as fast as 6.5 ns. The 2,048/4,096/8,192 x 36 dual-port SRAM FIFO buffers data from Port A to Port B. FIFO data on Port B can output in 36-bit, 18-bit, or 9-bit formats with a choice of Big- or Little-Endian configurations.

These devices are synchronous (clocked) FIFOs, meaning each port employs a synchronous interface. All data transfers through a port are gated to the LOW-to-HIGH transition of a port clock by enable signals. The clocks for

PIN CONFIGURATION



TQFP (PK128, order code: PF)
TOP VIEW

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each port are independent of one another and can be asynchronous or coincident. The enables for each port are arranged to provide a simple bidirectional interface between microprocessors and/or buses with synchronous control.

Communication between each port may bypass the FIFO via two mailbox registers. The mailbox registers' width matches the selected Port B bus width. Each mailbox register has a flag ($\overline{MBF1}$ and $\overline{MBF2}$) to signal when new mail has been stored.

Two kinds of reset are available on these FIFOs: Reset and Partial Reset. Reset initializes the read and write pointers to the first location of the memory array and selects serial flag programming, parallel flag programming, or one of five possible default flag offset settings, 8, 16, 64, 256 or 1,024.

Partial Reset also sets the read and write pointers to the first location of the memory. Unlike Reset, any settings existing prior to Partial Reset (i.e., programming method and partial flag default offsets) are retained. Partial Reset is useful since it permits flushing of the FIFO memory without changing any configuration settings.

The FIFO has Retransmit capability, a Retransmit is performed after four clock cycles of CLKA and CLKB, by taking the Retransmit pin, $\overline{RT}$ LOW while the Retransmit Mode pin, $\overline{RTM}$ is HIGH. When a Retransmit is performed the read pointer is reset to the first memory location.

These devices have two modes of operation: In the *IDT Standard mode*, the first word written to an empty FIFO is deposited into the memory array. A read operation is required to access that word (along with all other words residing in memory). In the *First Word Fall Through mode* (FWFT), the first word written to an empty FIFO appears automatically on the outputs, no read operation required (Nevertheless, accessing subsequent words does necessitate a formal read request). The state of the BE/$\overline{FWFT}$ pin during Reset determines the mode in use.

The FIFO has a combined Empty/Output Ready Flag ($\overline{EF}$/OR) and a combined Full/Input Ready Flag ($\overline{FF}$/IR). The $\overline{EF}$ and $\overline{FF}$ functions are selected in the IDT Standard mode. $\overline{EF}$ indicates whether or not the FIFO memory is empty. $\overline{FF}$ shows whether the memory is full or not. The IR and OR functions are selected in the First Word Fall Through mode. IR indicates whether or not the FIFO has available memory locations. OR shows whether the FIFO has data available for reading or not. It marks the presence of valid data on the outputs.

The FIFO has a programmable Almost-Empty flag ($\overline{AE}$) and a programmable Almost-Full flag ($\overline{AF}$). $\overline{AE}$ indicates when a selected number of words remain in the FIFO memory. $\overline{AF}$ indicates when the FIFO contains more than a selected number of words.

$\overline{FF}$/IR and $\overline{AF}$ are two-stage synchronized to the port clock that writes data into its array. $\overline{EF}$/OR and $\overline{AE}$ are two-stage synchronized to the port clock that reads data from its array. Programmable offsets for $\overline{AE}$ and $\overline{AF}$ are loaded in parallel using Port A or in serial via the SD input. Five default offset settings are also provided. The $\overline{AE}$ threshold can be set at 8, 16, 64, 256 or 1,024 locations from the empty boundary and the $\overline{AF}$ threshold can be set at 8, 16, 64, 256 or 1,024 locations from the full boundary. All these choices are made using the FS0, FS1 and FS2 inputs during Reset.

Interspersed Parity is available and can be selected during a Master Reset of the FIFO. If Interspersed Parity is selected then during parallel programming of the flag offset values, the device will ignore data line A8. If Non-Interspersed Parity is selected then data line A8 will become a valid bit.

Two or more devices may be used in parallel to create wider data paths. In First Word Fall Through mode, more than one device may be connected in series to create greater word depths. The addition of external components is unnecessary.

If, at any time, the FIFO is not actively performing a function, the chip will automatically power down. During the power down state, supply current consumption (I_{CC}) is at a minimum. Initiating any operation (by activating control inputs) will immediately take the device out of the Power Down state.

The IDT72V3653/72V3663/72V3673 are characterized for operation from 0°C to 70°C. Industrial temperature range (-40°C to +85°C) is available by special order. They are fabricated using high speed, submicron CMOS technology.

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PIN DESCRIPTIONS

Symbol	Name	I/O	Description
A0-A35	Port A Data	I/O	36-bit bidirectional data port for side A.
$\overline{AE}$	Almost-Empty Flag (Port B)	O	Programmable Almost-Empty flag synchronized to CLKB. It is LOW when the number of words in the FIFO is less than or equal to the value in the Almost-Empty B offset register, X.
$\overline{AF}$	Almost-Full Flag (Port A)	O	Programmable Almost-Full flag synchronized to CLKA. It is LOW when the number of empty locations in the FIFO is less than or equal to the value in the Almost-Full A offset register, Y.
B0-B35	Port B Data	I/O	36-bit bidirectional data port for side B.
BE/$\overline{FWFT}$	Big-Endian/ First Word Fall Through	I	This is a dual purpose pin. During Master Reset, a HIGH on BE will select Big-Endian operation. In this case, depending on the bus size, the most significant byte or word written to Port A is read from Port B first. A LOW on BE will select Little-Endian operation. In this case, the least significant byte or word written to Port A is read from Port B first. After Master Reset, this pin selects the timing mode. A HIGH on $\overline{FWFT}$ selects IDT Standard mode, a LOW selects First Word Fall Through mode. Once the timing mode has been selected, the level on $\overline{FWFT}$ must be static throughout device operation.
BM[1]	Bus-Match Select (Port B)	I	A HIGH on this pin enables either byte or word bus width on Port B, depending on the state of SIZE. A LOW selects long word operation. BM works with SIZE and BE to select the bus size and endian arrangement for Port B. The level of BM must be static throughout device operation.
CLKA	Port A Clock	I	CLKA is a continuous clock that synchronizes all data transfers through Port A and can be asynchronous or coincident to CLKB. $\overline{FF}$/IR and $\overline{AF}$ are synchronized to the LOW-to-HIGH transition of CLKA.
CLKB	Port B Clock	I	CLKB is a continuous clock that synchronizes all data transfers through Port B and can be asynchronous or coincident to CLKA. $\overline{EF}$/OR and $\overline{AE}$ are synchronized to the LOW-to-HIGH transition of CLKB.
$\overline{CSA}$	Port A Chip Select	I	$\overline{CSA}$ must be LOW to enable to LOW-to-HIGH transition of CLKA to read or write on Port A. The A0-A35 outputs are in the high-impedance state when $\overline{CSA}$ is HIGH.
$\overline{CSB}$	Port B Chip Select	I	$\overline{CSB}$ must be LOW to enable a LOW-to-HIGH transition of CLKB to read or write data on Port B. The B0-B35 outputs are in the high-impedance state when $\overline{CSB}$ is HIGH.
$\overline{EF}$/OR	Empty/Output Ready Flag (Port B)	O	This is a dual function pin. In the IDT Standard mode, the $\overline{EF}$ function is selected. $\overline{EF}$ indicates whether or not the FIFO memory is empty. In the FWFT mode, the OR function is selected. OR indicates the presence of valid data on the B0-B35 outputs, available for reading. $\overline{EF}$/OR is synchronized to the LOW-to-HIGH transition of CLKB.
ENA	Port A Enable	I	ENA must be HIGH to enable a LOW-to-HIGH transition of CLKA to read or write data on Port A.
ENB	Port B Enable	I	ENB must be HIGH to enable a LOW-to-HIGH transition of CLKB to read or write data on Port B.
$\overline{FF}$/IR	Full/Input Ready Flag (Port A)	O	This is a dual function pin. In the IDT Standard mode, the $\overline{FF}$ function is selected. $\overline{FF}$ indicates whether or not the FIFO memory is full. In the FWFT mode, the IR function is selected. IR indicates whether or not there is space available for writing to the FIFO memory. $\overline{FF}$/IR is synchronized to the LOW-to-HIGH transition of CLKA.
FS0/SD	Flag Offset Select 0/ Serial Data,	I	FS1/$\overline{SEN}$ and FS0/SD are dual-purpose inputs used for flag offset register programming. During Reset, FS1/$\overline{SEN}$ and FS0/SD, together with FS2 select the flag offset programming method. Three offset register programming methods are available: automatically load one of five preset values (8, 16, 64, 256 or 1,024), parallel load from Port A, and serial load.
FS1/$\overline{SEN}$	Flag Offset Select 1/ Serial Enable	I	When serial load is selected for flag offset register programming, FS1/$\overline{SEN}$ is used as an enable synchronous to the LOW-to-HIGH transition of CLKA. When FS1/$\overline{SEN}$ is LOW, a rising edge on CLKA load the bit present on FS0/SD into the X and Y registers. The number of bit writes required to program the offset registers is 22 for the IDT72V3653, 24 for the IDT72V3663, and 26 for the IDT72V3673. The first bit write stores the Y-register MSB and the last bit write stores the X-register LSB.
FS2[1]	Flag Offset Select 2	I	

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PIN DESCRIPTIONS (CONTINUED)

Symbol	Name	I/O	Description
MBA	Port A Mailbox Select	I	A HIGH level on MBA chooses a mailbox register for a Port A read or write operation.
MBB	Port B Mailbox Select	I	A HIGH level on MBB chooses a mailbox register for a Port B read or write operation. When the B0-B35 outputs are active, a HIGH level on MBB selects data from the mail1 register for output and a LOW level selects FIFO data for output.
$\overline{MBF1}$	Mail1 Register Flag	O	$\overline{MBF1}$ is set LOW by a LOW-to-HIGH transition of CLKA that writes data to the mail1 register. Writes to the mail1 register are inhibited while $\overline{MBF1}$ is LOW. $\overline{MBF1}$ is set HIGH by a LOW-to-HIGH transition of CLKB when a Port B read is selected and MBB is HIGH. $\overline{MBF1}$ is set HIGH following either a Reset ($\overline{RS1}$) or Partial Reset ($\overline{PRS}$).
$\overline{MBF2}$	Mail2 Register Flag	O	$\overline{MBF2}$ is set LOW by a LOW-to-HIGH transition of CLKB that writes data to the mail2 register. Writes to the mail2 register are inhibited while $\overline{MBF2}$ is LOW. $\overline{MBF2}$ is set HIGH by a LOW-to-HIGH transition of CLKA when a Port A read is selected and MBA is HIGH. $\overline{MBF2}$ is set HIGH following either a Reset ($\overline{RS2}$) or Partial Reset ($\overline{PRS}$).
$\overline{RS1}$, $\overline{RS2}$	Resets	I	A LOW on both pins initializes the FIFO read and write pointers to the first location of memory and sets the Port B output register to all zeroes. A LOW-to-HIGH transition on $\overline{RS1}$ selects the programming method (serial or parallel) and one of five programmable flag default offsets. It also configures Port B for bus size and endian arrangement. Four LOW-to-HIGH transitions of CLKA and four LOW-to-HIGH transitions of CLKB must occur while $\overline{RS1}$ is LOW.
$\overline{PRS}$/ $\overline{RT}$	Partial Reset/ Retransmit	I	This pin muxed for both Partial Reset and Retransmit operations, it is used in conjunction with the RTM pin. If RTM is LOW, then a LOW on this pin initializes the FIFO read and write pointers to the first location of memory and sets the Port B output register to all zeroes. During Partial Reset, the currently selected bus size, endian arrangement, programming method (serial or parallel), and programmable flag settings are all retained. If RTM is HIGH, then a LOW on this pin performs a Retransmit and initializes the read pointer only, to the first memory location.
RTM	Retransmit Mode	I	This pin is used in conjunction with the $\overline{RT}$ pin. When RTM is HIGH a Retransmit is performed when $\overline{RT}$ is taken HIGH.
SIZE[1]	Bus Size Select (Port B)	I	A HIGH on this pin when BM is HIGH selects byte bus (9-bit) size on Port B. A LOW on this pin when BM is HIGH selects word (18-bit) bus size. SIZE works with BM and BE to select the bus size and endian arrangement for Port B. The level of SIZE must be static throughout device operation.
W/$\overline{RA}$	Port A Write/ Read Select	I	A HIGH selects a write operation and a LOW selects a read operation on Port A for a LOW-to-HIGH transition of CLKA. The A0-A35 outputs are in the HIGH impedance state when W/$\overline{RA}$ is HIGH.
$\overline{W}$/RB	Port B Write/ Read Select	I	A LOW selects a write operation and a HIGH selects a read operation on Port B for a LOW-to-HIGH transition of CLKB. The B0-B35 outputs are in the HIGH impedance state when $\overline{W}$/RB is LOW.

NOTE:
1. FS2, BM and Size inputs are not TTL compatible. These inputs should be tied to GND or VCC.

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ABSOLUTE MAXIMUM RATINGS OVER OPERATING FREE-AIR TEMPERATURE RANGE (Unless otherwise noted)(1)

Symbol	Rating	Commercial	Unit
V_{CC}	Supply Voltage Range	–0.5 to +4.6	V
V_I(2)	Input Voltage Range	–0.5 to V_{CC}+0.5	V
V_O(2)	Output Voltage Range	–0.5 to V_{CC}+0.5	V
I_{IK}	Input Clamp Current (V_I < 0 or V_I > V_{CC})	±20	mA
I_{OK}	Output Clamp Current (V_O = < 0 or V_O > V_{CC})	±50	mA
I_{OUT}	Continuous Output Current (V_O = 0 to V_{CC})	±50	mA
I_{CC}	Continuous Current Through V_{CC} or GND	±400	mA
T_{STG}	Storage Temperature Range	–65 to 150	°C

NOTES:
1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded provided the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}(1)	Supply Voltage for 10ns	3.15	3.3	3.45	V
V_{CC}	Supply Voltage for 15ns	3.0	3.3	3.6	V
V_{IH}	High-Level Input Voltage	2	—	V_{CC}+0.5	V
V_{IL}	Low-Level Input Voltage	—	—	0.8	V
I_{OH}	High-Level Output Current	—	—	–4	mA
I_{OL}	Low-Level Output Current	—	—	8	mA
T_A	Operating Temperature	0	—	70	°C

NOTES:
1. For 10ns speed grade: V_{CC} = 3.3V ± 0.15V, JEDEC JESD8-A compliant

ELECTRICAL CHARACTERISTICS OVER RECOMMENDED OPERATING FREE-AIR TEMPERATURE RANGE (Unless otherwise noted)

				IDT72V3653 IDT72V3663 IDT72V3673 Commercial t_{CLK} = 10, 15ns(3)			
Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
V_{OH}	Output Logic "1" Voltage	V_{CC} = 3.0V,	I_{OH} = –4 mA	2.4	—	—	V
V_{OL}	Output Logic "0" Voltage	V_{CC} = 3.0V,	I_{OL} = 8 mA	—	—	0.5	V
I_{LI}	Input Leakage Current (Any Input)	V_{CC} = 3.6V,	V_I = V_{CC} or 0	—	—	10	µA
I_{LO}	Output Leakage Current	V_{CC} = 3.6V,	V_O = V_{CC} or 0	—	—	10	µA
I_{CC3}(2)	Standby Current (No Clocks running)	V_{CC} = 3.6V,	V_I = V_{CC} - 0.2V or 0	—	—	1	mA
I_{CC2}(2)	Standby Current (With CLKA & CLKB running)	V_{CC} = 3.6V,	V_I = V_{CC} - 0.2V or 0	—	—	5	mA
C_{IN}(4)	Input Capacitance	V_I = 0,	f = 1 MHz	—	4	—	pF
C_{OUT}(4)	Output Capacitance	V_O = 0,	f = 1 MHZ	—	8	—	pF

NOTES:
1. All typical values are at V_{CC} = 3.3V, T_A = 25°C.
2. For additional I_{CC} information, see Figure 1, *Typical Characteristics: Supply Current (I_{CC}) vs. Clock Frequency (fs)*.
3. Commercial-10ns speed grade only: V_{CC} = 3.3V ± 0.15V, T_A = 0° to +70°; JEDEC JESD8-A compliant
4. Characterized values, not currently tested.

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DETERMINING ACTIVE CURRENT CONSUMPTION AND POWER DISSIPATION

The $I_{CC(f)}$ current for the graph in Figure 1 was taken while simultaneously reading and writing a FIFO on the IDT72V3653/72V3663/72V3673 with CLKA and CLKB set to fs. All data inputs and data outputs change state during each clock cycle to consume the highest supply current. Data outputs were disconnected to normalize the graph to a zero capacitance load. Once the capacitance load per data-output channel and the number of IDT72V3653/72V3663/72V3673 inputs driven by TTL HIGH levels are known, the power dissipation can be calculated with the equation below.

CALCULATING POWER DISSIPATION

With $I_{CC(f)}$ taken from Figure 1, the maximum power dissipation (PT) of these FIFOs may be calculated by:

$$P_T = V_{CC} \times I_{CC(f)} + \sum_{N} (C_L \times V_{CC}^2 \times f_o)$$

where:

N	=	number of used outputs (36-bit (long word), 18-bit (word) or 9-bit (byte) bus size)
C_L	=	output capacitance load
f_o	=	switching frequency of an output

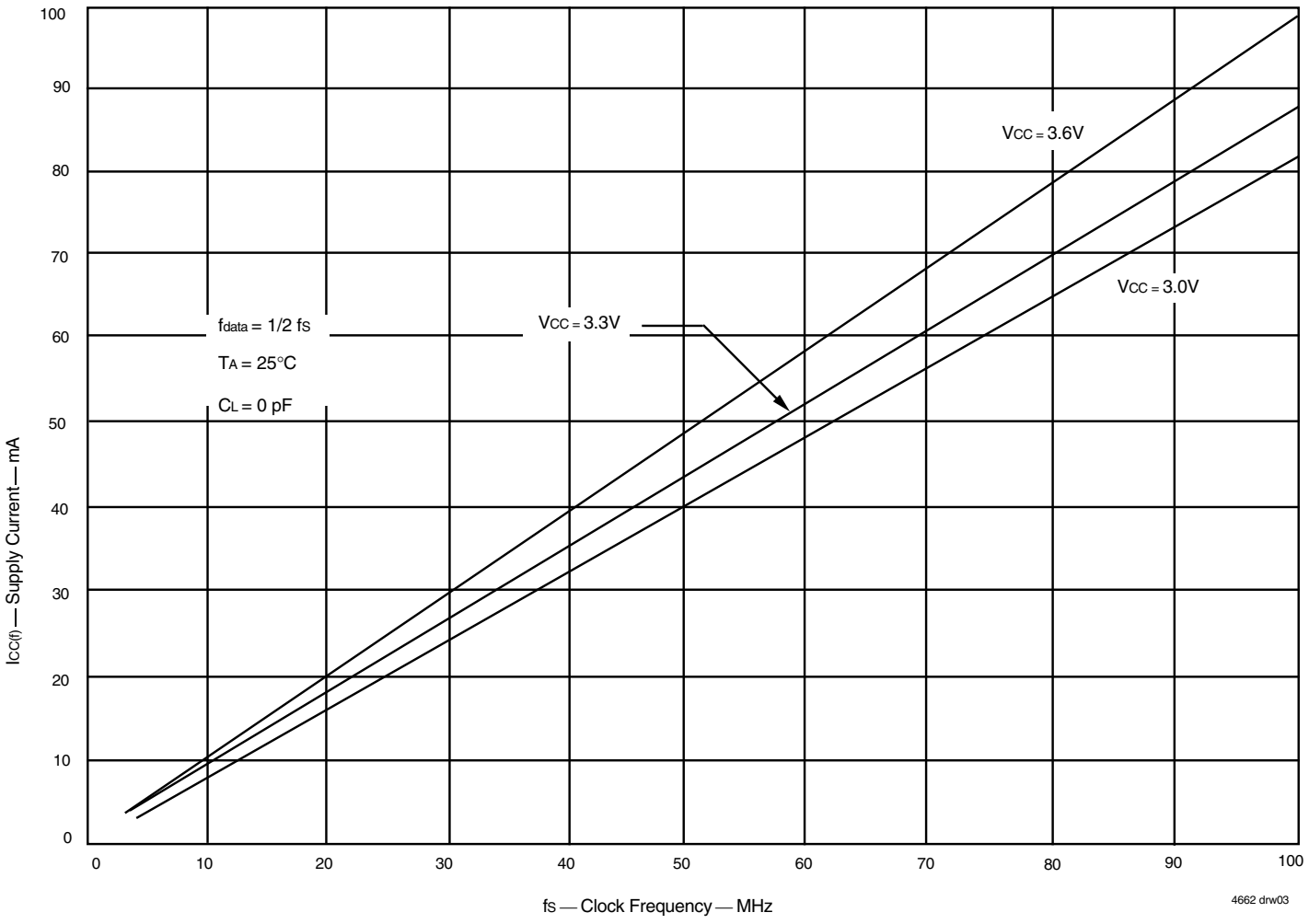


Figure 1. Typical Characteristics: Supply Current (I_{CC}) vs. Clock Frequency (fs)

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TIMING REQUIREMENTS OVER RECOMMENDED RANGES OF SUPPLY VOLTAGE AND OPERATING FREE-AIR TEMPERATURE

(For 10ns speed grade only: Vcc = 3.3V ± 0.15V; T_A = 0° C to +70° C; JEDEC JESD8-A compliant)

Symbol	Parameter	IDT72V3653L10[4] IDT72V3663L10[4] IDT72V3673L10[4]		IDT72V3653L15 IDT72V3663L15 IDT72V3673L15		Unit
		Min.	Max.	Min.	Max.	
f_S	Clock Frequency, CLKA or CLKB	—	100	—	66.7	MHz
t_{CLK}	Clock Cycle Time, CLKA or CLKB	10	—	15	—	ns
t_{CLKH}	Pulse Duration, CLKA or CLKB HIGH	4.5	—	6	—	ns
t_{CLKL}	Pulse Duration, CLKA and CLKB LOW	4.5	—	6	—	ns
t_{DS}	Setup Time, A0-A35 before CLKA↑ and B0-B35 before CLKB↑	3	—	4	—	ns
t_{ENS1}	Setup Time, $\overline{CSA}$ and W/$\overline{RA}$ before CLKA↑; $\overline{CSB}$ and $\overline{W}$/RB before CLKB↑	4	—	4.5	—	ns
t_{ENS2}	Setup Time, ENA, and MBA before CLKA↑; ENB and MBB before CLKB↑	3	—	4.5	—	ns
t_{RSTS}	Setup Time, $\overline{RS1}$ or $\overline{PRS}$ LOW before CLKA↑ or CLKB↑[1]	5	—	5	—	ns
t_{FSS}	Setup Time, FS0, FS1 and FS2 before $\overline{RS1}$ HIGH	7.5	—	7.5	—	ns
t_{BES}	Setup Time, BE/$\overline{FWFT}$ before $\overline{RS1}$ HIGH	7.5	—	7.5	—	ns
t_{SDS}	Setup Time, FS0/SD before CLKA↑	3	—	4	—	ns
t_{SENS}	Setup Time, FS1/$\overline{SEN}$ before CLKA↑	3	—	4	—	ns
t_{FWS}	Setup Time, FWFT before CLKA↑	0	—	0	—	ns
t_{DH}	Hold Time, A0-A35 after CLKA↑ and B0-B35 after CLKB↑	0.5	—	1	—	ns
t_{RTMS}	Setup Time, RTM before $\overline{RT1}$; RTM before $\overline{RT2}$	5	—	5	—	ns
t_{ENH}	Hold Time, $\overline{CSA}$, W/$\overline{RA}$, ENA, and MBA after CLKA↑; $\overline{CSB}$, $\overline{W}$/RB, ENB, and MBB after CLKB↑	0.5	—	1	—	ns
t_{RSTH}	Hold Time, $\overline{RS1}$ or $\overline{PRS}$ LOW after CLKA↑ or CLKB↑[1]	4	—	4	—	ns
t_{FSH}	Hold Time, FS0, FS1 and FS2 after $\overline{RS1}$ HIGH	2	—	2	—	ns
t_{BEH}	Hold Time, BE/$\overline{FWFT}$ after $\overline{RS1}$ HIGH	2	—	2	—	ns
t_{SDH}	Hold Time, FS0/SD after CLKA↑	0.5	—	1	—	ns
t_{SENH}	Hold Time, FS1/$\overline{SEN}$ HIGH after CLKA↑	0.5	—	1	—	ns
t_{SPH}	Hold Time, FS1/$\overline{SEN}$ HIGH after $\overline{RS1}$ HIGH	2	—	2	—	ns
t_{RTMH}	Hold Time, RTM after $\overline{RT1}$; RTM after $\overline{RT2}$	5	—	5	—	ns
t_{SKEW1}[2]	Skew Time between CLKA↑ and CLKB↑ for $\overline{EF}$/OR and $\overline{FF}$/IR	5	—	7.5	—	ns
t_{SKEW2}[2,3]	Skew Time between CLKA↑ and CLKB↑ for $\overline{AE}$ and $\overline{AF}$	12	—	12	—	ns

NOTES:

1. Requirement to count the clock edge as one of at least four needed to reset a FIFO.
2. Skew time is not a timing constraint for proper device operation and is only included to illustrate the timing relationship between CLKA cycle and CLKB cycle.
3. Design simulated, not tested.
4. For 10ns speed grade: Vcc = 3.3V ± 0.15V; T_A = 0° to +70°.

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SWITCHING CHARACTERISTICS OVER RECOMMENDED RANGES OF SUPPLY VOLTAGE AND OPERATING FREE-AIR TEMPERATURE, C_L = 30 pF

(For 10ns speed grade only: Vcc = 3.3V ± 0.15V; T_A = 0° C to +70° C; JEDEC JESD8-A compliant)

Symbol	Parameter	IDT72V3653L10[3] IDT72V3663L10[3] IDT72V3673L10[3] Min.	IDT72V3653L10[3] IDT72V3663L10[3] IDT72V3673L10[3] Max.	IDT72V3653L15 IDT72V3663L15 IDT72V3673L15 Min.	IDT72V3653L15 IDT72V3663L15 IDT72V3673L15 Max.	Unit
t_A	Access Time, CLKA↑ to A0-A35 and CLKB↑ to B0-B35	2	6.5	2	10	ns
t_{WFF}	Propagation Delay Time, CLKA↑ to $\overline{FF}$/IR	2	6.5	2	8	ns
t_{REF}	Propagation Delay Time, CLKB↑ to $\overline{EF}$/OR	1	6.5	1	8	ns
t_{PAE}	Propagation Delay Time, CLKB↑ to $\overline{AE}$	1	6.5	1	8	ns
t_{PAF}	Propagation Delay Time, CLKA↑ to $\overline{AF}$	1	6.5	1	8	ns
t_{PMF}	Propagation Delay Time, CLKA↑ to $\overline{MBF1}$ LOW or $\overline{MBF2}$ and CLKB↑ to $\overline{MBF2}$ LOW or $\overline{MBF1}$ HIGH	0	6.5	0	8	ns
t_{PMR}	Propagation Delay Time, CLKA↑ to B0-B35[1] and CLKB↑ to A0-A35[2]	3	8	2	10	ns
t_{MDV}	Propagation Delay Time, MBA to A0-A35 valid and MBB to B0-B35 Valid	3	6.5	2	10	ns
t_{RSF}	Propagation Delay Time, $\overline{RS1}$ or $\overline{PRS}$ LOW to $\overline{AE}$ LOW, $\overline{AF}$ HIGH, $\overline{MBF1}$ HIGH and $\overline{MBF2}$ HIGH	1	10	1	15	ns
t_{EN}	Enable Time, $\overline{CSA}$ and W/$\overline{R}$A LOW to A0-A35 Active and $\overline{CSB}$ LOW and $\overline{W}$/RB HIGH to B0-B35 Active	2	6	2	10	ns
t_{DIS}	Disable Time, $\overline{CSA}$ or W/$\overline{R}$A HIGH to A0-A35 at high impedance and $\overline{CSB}$ HIGH or $\overline{W}$/RB LOW to B0-B35 at high impedance	1	6	1	8	ns

NOTES:
1. Writing data to the mail1 register when the B0-B35 outputs are active and MBB is HIGH.
2. Writing data to the mail2 register when the A0-A35 outputs are active and MBA is HIGH.
3. For 10ns speed grade: Vcc = 3.3V ± 0.15V; T_A = 0° to +70°.

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SIGNAL DESCRIPTION

RESET ($\overline{RS1}$, $\overline{RS2}$)

After power up, a Reset operation must be performed by providing a LOW pulse to $\overline{RS1}$ and $\overline{RS2}$ simultaneously. Afterwards, the FIFO memory of the IDT72V3653/72V3663/72V3673 undergoes a complete reset by taking its Reset ($\overline{RS1}$ and $\overline{RS2}$) input LOW for at least four Port A clock (CLKA) and four Port B clock (CLKB) LOW-to-HIGH transitions. The Reset inputs can switch asynchronously to the clocks. A Reset initializes the internal read and write pointers and forces the Full/Input Ready flag ($\overline{FF}$/IR) LOW, the Empty/Output Ready flag ($\overline{EF}$/OR) LOW, the Almost-Empty flag ($\overline{AE}$) LOW, and the Almost-Full flag ($\overline{AF}$) HIGH. A Reset ($\overline{RS1}$) also forces the Mailbox flag ($\overline{MBF1}$) of the parallel mailbox register HIGH, and at the same time the $\overline{RS2}$ and $\overline{MBF2}$ operate likewise. After a Reset, the FIFO's Full/Input Ready flag is set HIGH after two write clock cycles to begin normal operation.

A LOW-to-HIGH transition on the FIFO Reset ($\overline{RS1}$) input latches the value of the Big-Endian (BE) input for determining the order by which bytes are transferred through Port B.

A LOW-to-HIGH transition on the FIFO Reset ($\overline{RS1}$) input also latches the values of the Flag Select (FS0, FS1 and FS2) inputs for choosing the Almost-Full and Almost-Empty offset programming method (for details see Table 1, *Flag Programming,* and Almost-Empty and Almost-Full flag offset programming section). The relevant Reset timing diagram can be found in Figure 3.

PARTIAL RESET ($\overline{PRS}$)

The FIFO memory of the IDT72V3653/72V3663/72V3673 undergoes a limited reset by taking its Partial Reset ($\overline{PRS}$) input LOW for at least four Port A clock (CLKA) and four Port B clock (CLKB) LOW-to-HIGH transitions. The RTM pin must be LOW during the time of Partial Reset. The Partial Reset input can switch asynchronously to the clocks. A Partial Reset initializes the internal read and write pointers and forces the Full/Input Ready flag ($\overline{FF}$/IR) LOW, the Empty/Output Ready flag ($\overline{EF}$/OR) LOW, the Almost-Empty flag ($\overline{AE}$) LOW, and the Almost-Full flag ($\overline{AF}$) HIGH. A Partial Reset also forces the Mailbox flag ($\overline{MBF1}$, $\overline{MBF2}$) of the parallel mailbox register HIGH. After a Partial Reset, the FIFO's Full/Input Ready flag is set HIGH after two Write Clock cycles to begin normal operation. See Figure 4, *Partial Reset (IDT Standard and FWFT Modes)* for the relevant timing diagram.

Whatever flag offsets, programming method (parallel or serial), and timing mode (FWFT or IDT Standard mode) are currently selected at the time a Partial Reset is initiated, those settings will be remain unchanged upon completion of the reset operation. A Partial Reset may be useful in the case where reprogramming a FIFO following a Reset would be inconvenient.

RETRANSMIT ($\overline{RT}$)

The FIFO memory of these devices undergoes a Retransmit by taking its associated Retransmit ($\overline{RT}$) input LOW for at least four Port A Clock (CLKA) and four Port B Clock (CLKB) LOW-to-HIGH transitions. The Retransmit initializes the read pointer of FIFO to the first memory location.

The RTM pin must be HIGH during the time of Retransmit. Note that the $\overline{RT}$ input is muxed with the $\overline{PRS}$ input, the state of the RTM pin determining whether this pin performs a Retransmit or a Partial Reset. See Figure 19 for Retransmit (Standard IDT mode) and figure 20 for Retransmit (FWFT mode) timing diagrams.

BIG-ENDIAN/FIRST WORD FALL THROUGH (BE/$\overline{FWFT}$)

— ENDIAN SELECTION

This is a dual purpose pin. At the time of Reset, the BE select function is active, permitting a choice of Big- or Little-Endian byte arrangement for data read from Port B. This selection determines the order by which bytes (or words) of data are transferred through this port. For the following illustrations, assume that a byte (or word) bus size has been selected for Port B. (Note that when Port B is configured for a long word size, the Big-Endian function has no application and the BE input is a "don't care"[1].)

A HIGH on the BE/$\overline{FWFT}$ input when the Reset ($\overline{RS1}$) input goes from LOW to HIGH will select a Big-Endian arrangement. In this case, the most significant byte (word) of the long word written to Port A will be read from Port B first; the least significant byte (word) of the long word written to Port A will be read from Port B last.

A LOW on the BE/$\overline{FWFT}$ input when the Reset ($\overline{RS1}$) input goes from LOW to HIGH will select a Little-Endian arrangement. In this case, the least significant byte (word) of the long word written to Port A will be read from Port B first; the most significant byte (word) of the long word written to Port A will be read from Port B last. Refer to Figure 2 for an illustration of the BE function. See Figure 3 (Reset) for an Endian select timing diagram.

— TIMING MODE SELECTION

After Reset, the FWFT select function is active, permitting a choice between two possible timing modes: IDT Standard mode or First Word Fall Through (FWFT) mode. Once the Reset ($\overline{RS1}$) input is HIGH, a HIGH on the BE/$\overline{FWFT}$ input during the next LOW-to-HIGH transition of CLKA and CLKB will select IDT Standard mode. This mode uses the Empty Flag function ($\overline{EF}$) to indicate whether or not there are any words present in the FIFO memory. It uses the Full Flag function ($\overline{FF}$) to indicate whether or not the FIFO memory has any free space for writing. In IDT Standard mode, every word read from the FIFO, including the first, must be requested using a formal read operation.

Once the Reset ($\overline{RS1}$) input is HIGH, a LOW on the BE/$\overline{FWFT}$ input during the next LOW-to-HIGH transition of CLKA and CLKB will select FWFT mode. This mode uses the Output Ready function (OR) to indicate whether or not there is valid data at the data outputs (B0-B35). It also uses the Input Ready function (IR) to indicate whether or not the FIFO memory has any free space for writing. In the FWFT mode, the first word written to an empty FIFO goes directly to data outputs, no read request necessary. Subsequent words must be accessed by performing a formal read operation.

Following Reset, the level applied to the BE/$\overline{FWFT}$ input to choose the desired timing mode must remain static throughout FIFO operation. Refer to Figure 3 (Reset) for a First Word Fall Through select timing diagram.

PROGRAMMING THE ALMOST-EMPTY AND ALMOST-FULL FLAGS

Two registers in the IDT72V3653/72V3663/72V3673 are used to hold the offset values for the Almost-Empty and Almost-Full flags. The Almost-Empty flag ($\overline{AE}$) Offset register is labeled X and Almost-Full flag ($\overline{AF}$) Offset register is labeled Y. The offset registers can be loaded with preset values during the reset of the FIFO, programmed in parallel using the FIFO's Port A data inputs, or programmed in serial using the Serial Data (SD) input (see Table 1). FS2 FS0/SD, and FS1/$\overline{SEN}$ function the same way in both IDT Standard and FWFT modes.

NOTE:

1. Either a HIGH or LOW can be applied to a "don't care" input with no change to the logical operation of the FIFO. Nevertheless, inputs that are temporarily "don't care" (along with unused inputs) must not be left open, rather they must be either HIGH or LOW.

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TABLE 1 — FLAG PROGRAMMING

FS2	FS1/$\overline{SEN}$	FS0/SD	$\overline{RS1}$	X AND Y REGISTERS[1]
H	H	H	↑	64
H	H	L	↑	16
H	L	H	↑	8
L	H	H	↑	256
L	L	H	↑	1,024
L	H	L	↑	Serial programming via SD
H	L	L	↑	Parallel programming via Port A[2,4]
L	L	L	↑	IP Mode[3,4]

NOTE:
1. X register holds the offset for $\overline{AE}$; Y register holds the offset for $\overline{AF}$.
2. When this method of parallel programming is selected, Port A will assume Non-Interspersed Parity.
3. When IP Mode is selected, only parallel programming of the offset values via Port A, can be performed and Port A will assume Interspersed Parity.
4. IF parallel programming is selected during a Master Reset, then FS0 & FS1 must remain LOW during FIFO operation.

— PRESET VALUES

To load a FIFO's Almost-Empty flag and Almost-Full flag Offset registers with one of the five preset values listed in Table 1, the flag select inputs must be HIGH or LOW during a reset. For example, to load the preset value of 64 into X and Y, FS0, FS1 and FS2 must be HIGH when $\overline{RS1}$ returns HIGH. For the relevant preset value loading timing diagram, see Figure 3.

— PARALLEL LOAD FROM PORT A

To program the X and Y registers from Port A, perform a Reset with FS2 HIGH or LOW and FS0 and FS1 LOW during the LOW-to-HIGH transition of $\overline{RS1}$. The state of FS2 at this point of reset will determine whether the parallel programming method has Interspersed Parity or Non-Interspersed Parity. Refer to Table 1 for Flag Programming Flag Offset setup. It is important to note that once parallel programming has been selected during a Master Reset by holding both FS0 & FS1 LOW, these inputs must remain LOW during all subsequent FIFO operation. They can only be toggled HIGH when future Master Resets are performed and other programming methods are desired.

After this reset is complete, the first two writes to the FIFO do not store data in RAM. The first two write cycles load the offset registers in the order Y, X. On the third write cycle the FIFO is ready to be loaded with a data word. See Figure 5, *Parallel Programming of the Almost-Full Flag and Almost-Empty Flag Offset Values after Reset (IDT Standard and FWFT modes),* for a detailed timing diagram. For Non-Interspersed Parity mode the Port A data inputs used by the Offset registers are (A10-A0), (A11-A0), or (A12-A0) for the IDT72V3653, IDT72V3663, or IDT72V3673, respectively. For Interspersed Parity mode the Port A data inputs used by the Offset registers are (A11-A9, A7-A0), (A12-A9, A7-A0), or (A13-A9, A7-A0) for the IDT72V3653, IDT72V3663, or IDT72V3673, respectively. The highest numbered input is used as the most significant bit of the binary number in each case. Valid programming values for the registers range from 1 to 2,044 for the IDT72V3653; 1 to 4,092 for the IDT72V3663; and 1 to 8,188 for the IDT72V3673. After all the offset registers are programmed from Port A, the FIFO begins normal operation.

INTERSPERSED PARITY

Interspersed Parity is selected during a Master Reset of the FIFO. Refer to Table 1 for the set-up configuration of Interspersed Parity. The Interspersed Parity function allows the user to select the location of the parity bits in the word loaded into the parallel port (A0-An) during programming of the flag offset values. If Interspersed Parity is selected then during parallel programming of the flag offset values, the device will ignore data line A8. If Non-Interspersed Parity is selected then data line A8 will become a valid bit. If Interspersed Parity is selected serial programming of the offset values is not permitted, only parallel programming can be done.

— SERIAL LOAD

To program the X and Y registers serially, initiate a Reset with FS2 LOW, FS0/SD LOW and FS1/$\overline{SEN}$ HIGH during the LOW-to-HIGH transition of $\overline{RS1}$. After this reset is complete, the X and Y register values are loaded bit-wise through the FS0/SD input on each LOW-to-HIGH transition of CLKA that the FS1/$\overline{SEN}$ input is LOW. There are 22-, 24- or 26-bit writes needed to complete the programming for the IDT72V3653, IDT72V3663 or the IDT72V3673, respectively. The two registers are written in the order Y, X. Each register value can be programmed from 1 to 2,044 (IDT72V3653), 1 to 4,092 (IDT72V3663) or 1 to 8,188 (IDT72V3673).

When the option to program the offset registers serially is chosen, the Full/Input Ready ($\overline{FF}$/IR) flag remains LOW until all register bits are written. $\overline{FF}$/IR is set HIGH by the LOW-to-HIGH transition of CLKA after the last bit is loaded to allow normal FIFO operation.

See Figure 6, *Serial Programming of the Almost-Full Flag and Almost-Empty Flag Offset Values after Reset (IDT Standard and FWFT Modes).*

FIFO WRITE/READ OPERATION

The state of the Port A data (A0-A35) lines is controlled by Port A Chip Select ($\overline{CSA}$) and Port A Write/Read select (W/$\overline{RA}$). The A0-A35 lines are in the High-impedance state when either $\overline{CSA}$ or W/$\overline{RA}$ is HIGH. The A0-A35 lines are active outputs when both $\overline{CSA}$ and W/$\overline{RA}$ are LOW.

Data is loaded into the FIFO from the A0-A35 inputs on a LOW-to-HIGH transition of CLKA when $\overline{CSA}$ is LOW, W/$\overline{RA}$ is HIGH, ENA is HIGH, MBA is LOW, and $\overline{FF}$/IR is HIGH (see Table 2). FIFO writes on Port A are independent of any concurrent reads on Port B.

The Port B control signals are identical to those of Port A with the exception that the Port B Write/Read select ($\overline{W}$/RB) is the inverse of the Port A Write/Read select (W/$\overline{RA}$). The state of the Port B data (B0-B35) lines is controlled by the Port B Chip Select ($\overline{CSB}$) and Port B Write/Read select ($\overline{W}$/RB). The B0-B35 lines are in the high-impedance state when either $\overline{CSB}$ is HIGH or $\overline{W}$/RB is LOW. The B0-B35 lines are active outputs when $\overline{CSB}$ is LOW and $\overline{W}$/RB is HIGH.

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TABLE 2 — PORT-A ENABLE FUNCTION TABLE

$\overline{CSA}$	W/$\overline{RA}$	ENA	MBA	CLKA	Data A (A0-A35) I/O	Port Functions
H	X	X	X	X	High-Impedance	None
L	H	L	X	X	Input	None
L	H	H	L	↑	Input	FIFO Write
L	H	H	H	↑	Input	Mail1 Write
L	L	L	L	X	Output	None
L	L	H	L	↑	Output	None
L	L	L	H	X	Output	None
L	L	H	H	↑	Output	Mail2 Read (Set $\overline{MBF2}$ HIGH)

TABLE 3 — PORT-B ENABLE FUNCTION TABLE

$\overline{CSB}$	$\overline{W}$/RB	ENB	MBB	CLKB	Data B (B0-B35) I/O	Port Functions
H	X	X	X	X	High-Impedance	None
L	L	L	X	X	Input	None
L	L	H	L	↑	Input	None
L	L	H	H	↑	Input	Mail2 Write
L	H	L	L	X	Output	None
L	H	H	L	↑	Output	FIFO read
L	H	L	H	X	Output	None
L	H	H	H	↑	Output	Mail1 Read (Set $\overline{MBF1}$ HIGH)

TABLE 4 — FIFO FLAG OPERATION (IDT STANDARD AND FWFT MODES)

Number of Words in FIFO[1,2]			Synchronized to CLKB		Synchronized to CLKA	
IDT72V3653[3]	IDT72V3663[3]	IDT72V3673[3]	$\overline{EF}$/OR	$\overline{AE}$	$\overline{AF}$	$\overline{FF}$/IR
0	0	0	L	L	H	H
1 to X	1 to X	1 to X	H	L	H	H
(X+1) to [2,048-(Y+1)]	(X+1) to [4,096-(Y+1)]	(X+1) to [8,192-(Y+1)]	H	H	H	H
(2,048-Y) to 2,047	(4,096-Y) to 4,095	(8,192-Y) to 8,191	H	H	L	H
2,048	4,096	8,192	H	H	L	L

NOTES:
1. When a word loaded to an empty FIFO is shifted to the output register, its previous FIFO memory location is free.
2. Data in the output register does not count as a "word in FIFO memory". Since in FWFT mode, the first word written to an empty FIFO goes unrequested to the output register (no read operation necessary), it is not included in the memory count.
3. X is the Almost-Empty offset used by $\overline{AE}$. Y is the Almost-Full offset used by $\overline{AF}$. Both X and Y are selected during a FIFO reset or Port A programming.

Data is read from the FIFO to the B0-B35 outputs by a LOW-to-HIGH transition of CLKB when $\overline{CSB}$ is LOW, $\overline{W}$/RB is HIGH, ENB is HIGH, MBB is LOW, and $\overline{EF}$/OR is HIGH (see Table 3). FIFO reads on Port B are independent of any concurrent writes on Port A.

The setup and hold time constraints to the port clocks for the port Chip Selects and Write/Read selects are only for enabling write and read operations and are not related to high-impedance control of the data outputs. If a port enable is LOW during a clock cycle, the port's Chip Select and Write/Read select may change states during the setup and hold time window of the cycle.

When operating the FIFO in FWFT mode and the Output Ready flag is LOW, the next word written is automatically sent to the FIFO's output register by the LOW-to-HIGH transition of the port clock that sets the Output Ready flag HIGH. When the Output Ready flag is HIGH, data residing in the FIFO's memory array is clocked to the output register only when a read is selected using the port's Chip Select, Write/Read select, Enable, and Mailbox select.

When operating the FIFO in IDT Standard mode, regardless of whether the Empty Flag is LOW or HIGH, data residing in the FIFO's memory array is clocked to the output register only when a read is selected using the port's Chip Select, Write/Read select, Enable, and Mailbox select. Port A Write timing diagram can be found in Figure 7. Relevant Port B Read timing diagrams together with Bus-Matching and Endian select can be found in Figure 8, 9 and 10.

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SYNCHRONIZED FIFO FLAGS

Each FIFO is synchronized to its port clock through at least two flip-flop stages. This is done to improve flag-signal reliability by reducing the probability of metastable events when CLKA and CLKB operate asynchronously to one another. $\overline{FF}$/IR, and $\overline{AF}$ are synchronized to CLKA. $\overline{EF}$/OR and $\overline{AE}$ are synchronized to CLKB. Table 4 shows the relationship of each port flag to the number of words stored in memory.

EMPTY/OUTPUT READY FLAGS ($\overline{EF}$/OR)

These are dual purpose flags. In the FWFT mode, the Output Ready (OR) function is selected. When the Output-Ready flag is HIGH, new data is present in the FIFO output register. When the Output Ready flag is LOW, the previous data word is present in the FIFO output register and attempted FIFO reads are ignored.

In the IDT Standard mode, the Empty Flag ($\overline{EF}$) function is selected. When the Empty Flag is HIGH, data is available in the FIFO's memory for reading to the output register. When the Empty Flag is LOW, the previous data word is present in the FIFO output register and attempted FIFO reads are ignored.

The Empty/Output Ready flag of a FIFO is synchronized to the port clock that reads data from its array (CLKB). For both the FWFT and IDT Standard modes, the FIFO read pointer is incremented each time a new word is clocked to its output register. The state machine that controls an Output Ready flag monitors a write pointer and read pointer comparator that indicates when the FIFO memory status is empty, empty+1, or empty+2.

In FWFT mode, from the time a word is written to a FIFO, it can be shifted to the FIFO output register in a minimum of three cycles of the Output Ready flag synchronizing clock. Therefore, an Output Ready flag is LOW if a word in memory is the next data to be sent to the FIFO output register and three cycles of the port Clock that reads data from the FIFO have not elapsed since the time the word was written. The Output Ready flag of the FIFO remains LOW until the third LOW-to-HIGH transition of the synchronizing clock occurs, simultaneously forcing the Output Ready flag HIGH and shifting the word to the FIFO output register.

In IDT Standard mode, from the time a word is written to a FIFO, the Empty Flag will indicate the presence of data available for reading in a minimum of two cycles of the Empty Flag synchronizing clock. Therefore, an Empty Flag is LOW if a word in memory is the next data to be sent to the FIFO output register and two cycles of the port Clock that reads data from the FIFO have not elapsed since the time the word was written. The Empty Flag of the FIFO remains LOW until the second LOW-to-HIGH transition of the synchronizing clock occurs, forcing the Empty Flag HIGH; only then can data be read.

A LOW-to-HIGH transition on an Empty/Output Ready flag synchronizing clock begins the first synchronization cycle of a write if the clock transition occurs at time t_{SKEW1} or greater after the write. Otherwise, the subsequent clock cycle can be the first synchronization cycle (see Figures 11 and 12).

FULL/INPUT READY FLAGS ($\overline{FF}$/IR)

This is a dual purpose flag. In FWFT mode, the Input Ready (IR) function is selected. In IDT Standard mode, the Full Flag ($\overline{FF}$) function is selected. For both timing modes, when the Full/Input Ready flag is HIGH, a memory location is free in the FIFO to receive new data. No memory locations are free when the Full/Input Ready flag is LOW and attempted writes to the FIFO are ignored.

The Full/Input Ready flag of a FIFO is synchronized to the port clock that writes data to its array (CLKA). For both FWFT and IDT Standard modes, each time a word is written to a FIFO, its write pointer is incremented. The state machine that controls a Full/Input Ready flag monitors a write pointer and read pointer comparator that indicates when the FIFO memory status is full, full-1, or full-2. From the time a word is read from a FIFO, its previous memory location is ready to be written to in a minimum of two cycles of the Full/Input Ready flag synchronizing clock. Therefore, an Full/Input Ready flag is LOW if less than two cycles of the Full/Input Ready flag synchronizing clock have elapsed since the next memory write location has been read. The second LOW-to-HIGH transition on the Full/Input Ready flag synchronizing clock after the read sets the Full/Input Ready flag HIGH.

A LOW-to-HIGH transition on a Full/Input Ready flag synchronizing clock begins the first synchronization cycle of a read if the clock transition occurs at time t_{SKEW1} or greater after the read. Otherwise, the subsequent clock cycle can be the first synchronization cycle (see Figures 13 and 14).

ALMOST-EMPTY FLAG ($\overline{AE}$)

The Almost-Empty flag of a FIFO is synchronized to the port clock that reads data from its array (CLKB). The state machine that controls an Almost-Empty flag monitors a write pointer and read pointer comparator that indicates when the FIFO memory status is almost-empty, almost-empty+1, or almost-empty+2. The Almost-Empty state is defined by the contents of register X. These registers are loaded with preset values during a FIFO reset, programmed from Port A, or programmed serially (see Almost-Empty flag and Almost-Full flag offset programming section). An Almost-Empty flag is LOW when its FIFO contains X or less words and is HIGH when its FIFO contains (X+1) or more words. Note that a data word present in the FIFO output register has been read from memory.

Two LOW-to-HIGH transitions of the Almost-Empty flag synchronizing clock are required after a FIFO write for its Almost-Empty flag to reflect the new level of fill. Therefore, the Almost-Empty flag of a FIFO containing (X+1) or more words remains LOW if two cycles of its synchronizing clock have not elapsed since the write that filled the memory to the (X+1) level. An Almost-Empty flag is set HIGH by the second LOW-to-HIGH transition of its synchronizing clock after the FIFO write that fills memory to the (X+1) level. A LOW-to-HIGH transition of an Almost-Empty flag synchronizing clock begins the first synchronization cycle if it occurs at time t_{SKEW2} or greater after the write that fills the FIFO to (X+1) words. Otherwise, the subsequent synchronizing clock cycle may be the first synchronization cycle. (See Figure 15).

ALMOST-FULL FLAG ($\overline{AF}$)

The Almost-Full flag of a FIFO is synchronized to the port clock that writes data to its array. The state machine that controls an Almost-Full flag monitors a write pointer and read pointer comparator that indicates when the FIFO memory status is almost-full, almost-full-1, or almost-full-2. The Almost-Full state is defined by the contents of register Y. These registers are loaded with preset values during a FIFO reset or, programmed from Port A, or programmed serially (see Almost-Empty flag and Almost-Full flag offset programming section). An Almost-Full flag is LOW when the number of words in its FIFO is greater than or equal to (2,048-Y), (4,096-Y), or (8,192-Y) for the IDT72V3653, IDT72V3663, or IDT72V3673 respectively. An Almost-Full flag is HIGH when the number of words in its FIFO is less than or equal to [2,048-(Y+1)], [4,096-(Y+1)], or [8,192-(Y+1)] for the IDT72V3653, IDT72V3663, or IDT72V3673 respectively. Note that a data word present in the FIFO output register has been read from memory.

Two LOW-to-HIGH transitions of the Almost-Full flag synchronizing clock are required after a FIFO read for its Almost-Full flag to reflect the new level of fill. Therefore, the Almost-Full flag of a FIFO containing [2,048/4,096/8,192-(Y+1)] or less words remains LOW if two cycles of its synchronizing clock have not elapsed since the read that reduced the number of words in memory to [2,048/4,096/8,192-(Y+1)]. An Almost-Full flag is set HIGH by the second LOW-to-HIGH transition of its synchronizing clock after the FIFO read that reduces the number of words in memory to [2,048/4,096/8,192-(Y+1)]. A LOW-to-HIGH transition of an Almost-Full flag synchronizing clock begins the

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first synchronization cycle if it occurs at time t_{SKEW2} or greater after the read that reduces the number of words in memory to [2,048/4,096/8,192-(Y+1)]. Otherwise, the subsequent synchronizing clock cycle may be the first synchronization cycle (see Figure 16).

MAILBOX REGISTERS

Two 36-bit bypass registers are on the IDT72V3653/72V3663/72V3673 to pass command and control information between Port A and Port B without putting it in queue. The Mailbox select (MBA, MBB) inputs choose between a mail register and a FIFO for a port data transfer operation. The usable width of both the Mail1 and Mail2 Registers matches the selected bus size for Port B.

A LOW-to-HIGH transition on CLKA writes data to the Mail1 Register when a Port A write is selected by $\overline{CSA}$, W/$\overline{R}$A, and ENA with MBA HIGH. If the selected Port B bus size is 36 bits, the usable width of the Mail1 Register employs data lines A0-A35. If the selected Port B bus size is 18 bits, then the usable width of the Mail1 Register employs data lines A0-A17. (In this case, A18-A35 are don't care inputs.) If the selected Port B bus size is 9 bits, then the usable width of the Mail1 Register employs data lines A0-A8. (In this case, A9-A35 are don't care inputs.)

A LOW-to-HIGH transition on CLKB writes B0-B35 data to the Mail2 Register when a Port B write is selected by $\overline{CSB}$, $\overline{W}$/RB, and ENB with MBB HIGH. If the selected Port B bus size is 36 bits, the usable width of the Mail2 employs data lines B0-B35. If the selected Port B bus size is 18 bits, then the usable width of the Mail2 Register employs data lines B0-B17. (In this case, B18-B35 are don't care inputs.) If the selected Port B bus size is 9 bits, then the usable width of the Mail2 Register employs data lines B0-B8. (In this case, B9-B35 are don't care inputs.)

Writing data to a mail register sets its corresponding flag ($\overline{MBF1}$ or $\overline{MBF2}$) LOW. Attempted writes to a mail register are ignored while the mail flag is LOW.

When data outputs of a port are active, the data on the bus comes from the FIFO output register when the port Mailbox select input is LOW and from the mail register when the port Mailbox select input is HIGH.

The Mail1 Register Flag ($\overline{MBF1}$) is set HIGH by a LOW-to-HIGH transition on CLKB when a Port B read is selected by $\overline{CSB}$, $\overline{W}$/RB, and ENB with MBB HIGH. For a 36-bit bus size, 36 bits of mailbox data are placed on B0-B35. For an 18-bit bus size, 18 bits of mailbox data are placed on B0-B17. (In this case, B18-B35 are indeterminate.) For a 9-bit bus size, 9 bits of mailbox data are placed on B0-B8. (In this case, B9-B35 are indeterminate.)

The Mail2 Register Flag ($\overline{MBF2}$) is set HIGH by a LOW-to-HIGH transition on CLKA when a Port A read is selected by $\overline{CSA}$, W/$\overline{R}$A, and ENA with MBA HIGH.

For a 36-bit bus size, 36 bits of mailbox data are placed on A0-A35. For an 18-bit bus size, 18 bits of mailbox data are placed on A0-A17. (In this case, A18-A35 are indeterminate.) For a 9-bit bus size, 9 bits of mailbox data are placed on A0-A8. (In this case, A9-A35 are indeterminate.)

The data in a mail register remains intact after it is read and changes only when new data is written to the register. The Endian select feature has no effect on mailbox data. For mail register and mail register flag timing diagrams, see Figure 17 and 18.

BUS SIZING

The Port B bus can be configured in a 36-bit long word, 18-bit word, or 9-bit byte format for data read from the FIFO. The levels applied to the Port B Bus Size select (SIZE) and the Bus-Match select (BM) determine the Port B bus size. These levels should be static throughout FIFO operation. Both bus size selections are implemented at the completion of Reset, by the time the Full/Input Ready flag is set HIGH, as shown in Figure 2.

Two different methods for sequencing data transfer are available for Port B when the bus size selection is either byte-or word-size. They are referred to as Big-Endian (most significant byte first) and Little-Endian (least significant byte first). The level applied to the Big-Endian select (BE) input during the LOW-to-HIGH transition of $\overline{RS1}$ selects the endian method that will be active during FIFO operation. BE is a don't care input when the bus size selected for Port B is long word. The endian method is implemented at the completion of Reset, by the time the Full/Input Ready flag is set HIGH, as shown in Figure 2.

Only 36-bit long word data is written to or read from the FIFO memory on the IDT72V3653/72V3663/72V3673. Bus-matching operations are done after data is read from the FIFO RAM. These bus-matching operations are not available when transferring data via mailbox registers. Furthermore, both the word- and byte-size bus selections limit the width of the data bus that can be used for mail register operations. In this case, only those byte lanes belonging to the selected word- or byte-size bus can carry mailbox data. The remaining data outputs will be indeterminate. The remaining data inputs will be don't care inputs. For example, when a word-size bus is selected, then mailbox data can be transmitted only between A0-A17 and B0-B17. When a byte-size bus is selected, then mailbox data can be transmitted only between A0-A8 and B0-B8. (See Figures 17 and 18).

BUS-MATCHING FIFO READS

Data is read from the FIFO RAM in 36-bit long word increments. If a long word bus size is implemented, the entire long word immediately shifts to the FIFO output register. If byte or word size is implemented on Port B, only the first one or two bytes appear on the selected portion of the FIFO output register, with the rest of the long word stored in auxiliary registers. In this case, subsequent FIFO reads output the rest of the long word to the FIFO output register in the order shown by Figure 2.

When reading data from FIFO in byte or word format, the unused B0-B35 outputs are indeterminate.

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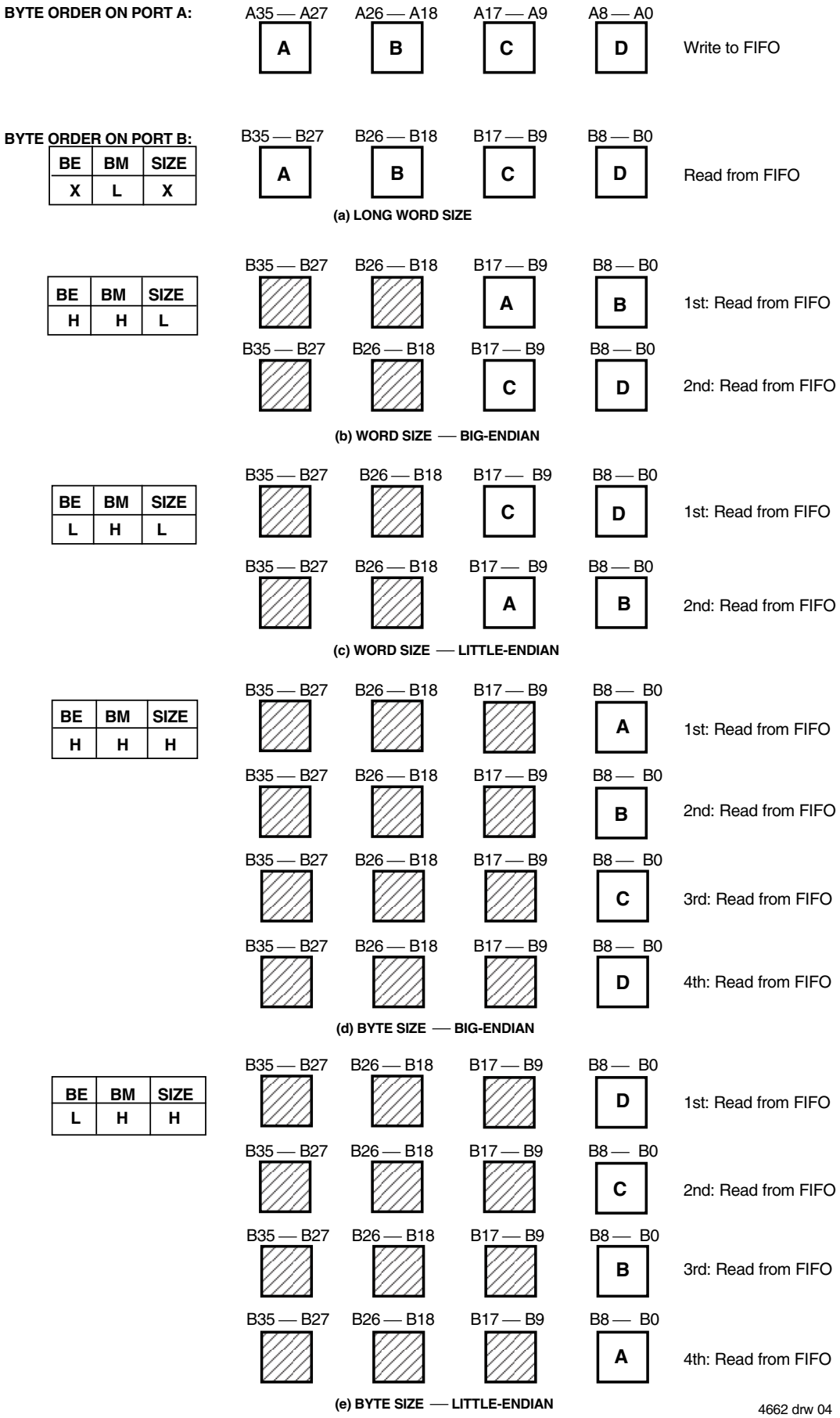
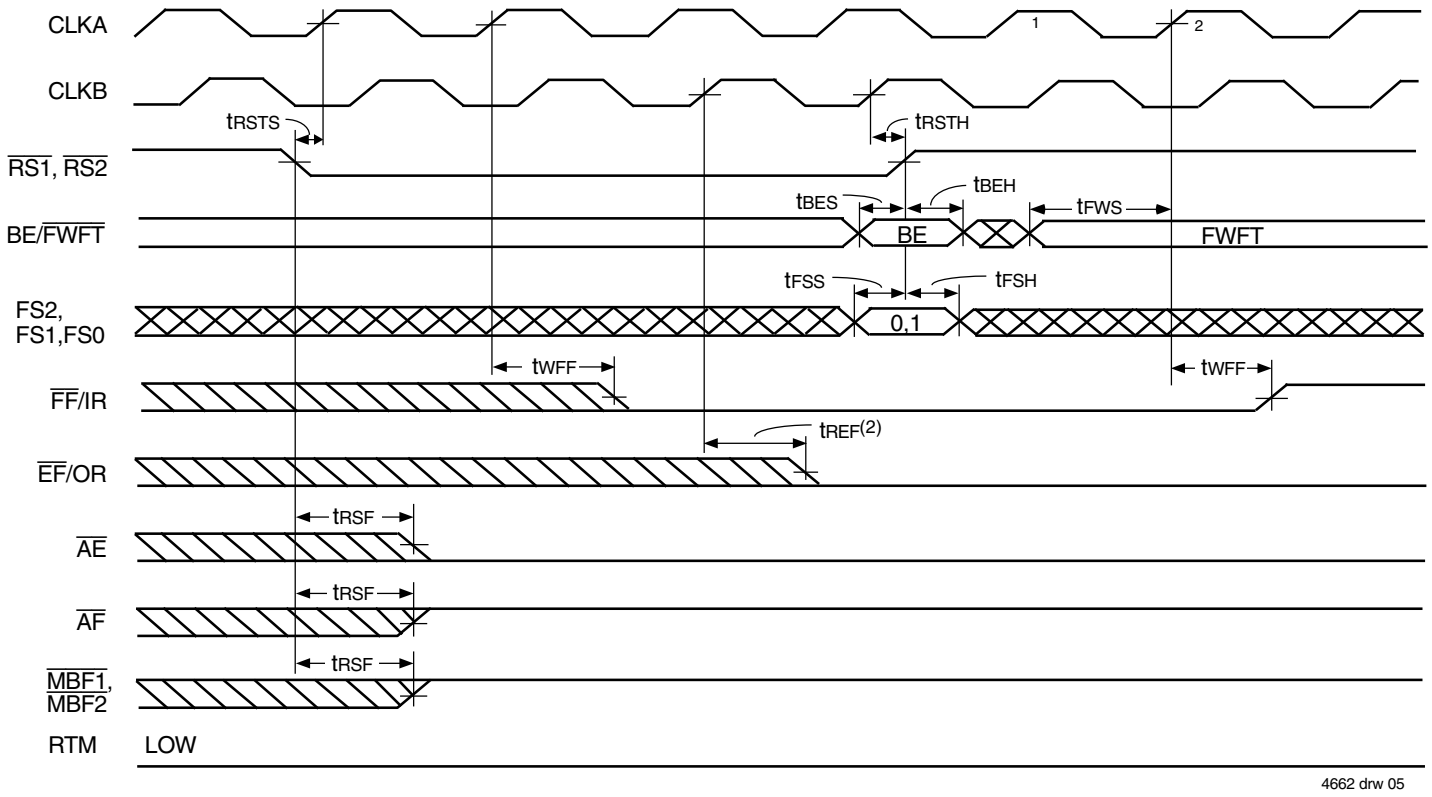


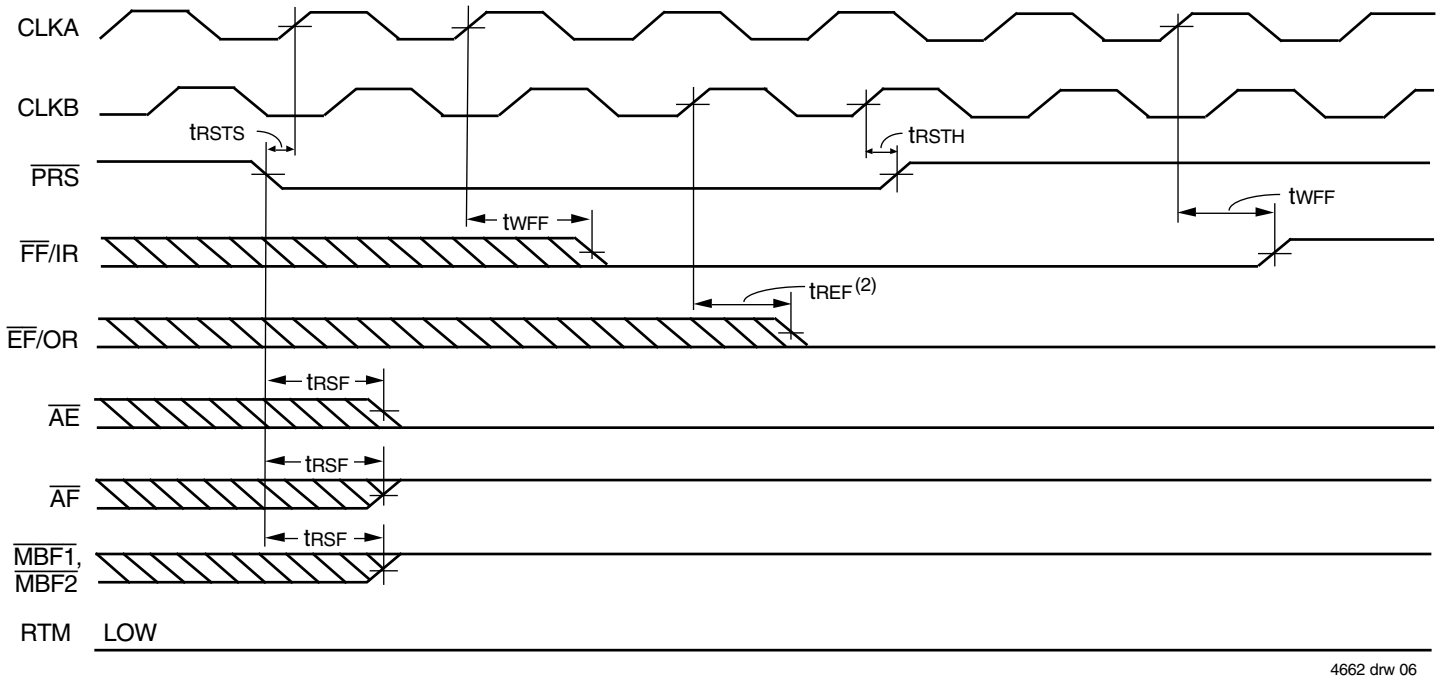
Figure 2. Bus sizing

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NOTES:
1. $\overline{PRS}$ must be HIGH during Reset.
2. If BE/$\overline{FWFT}$ is HIGH, then $\overline{EF}$/OR will go LOW one CLKB cycle earlier than in this case where BE/$\overline{FWFT}$ is LOW.

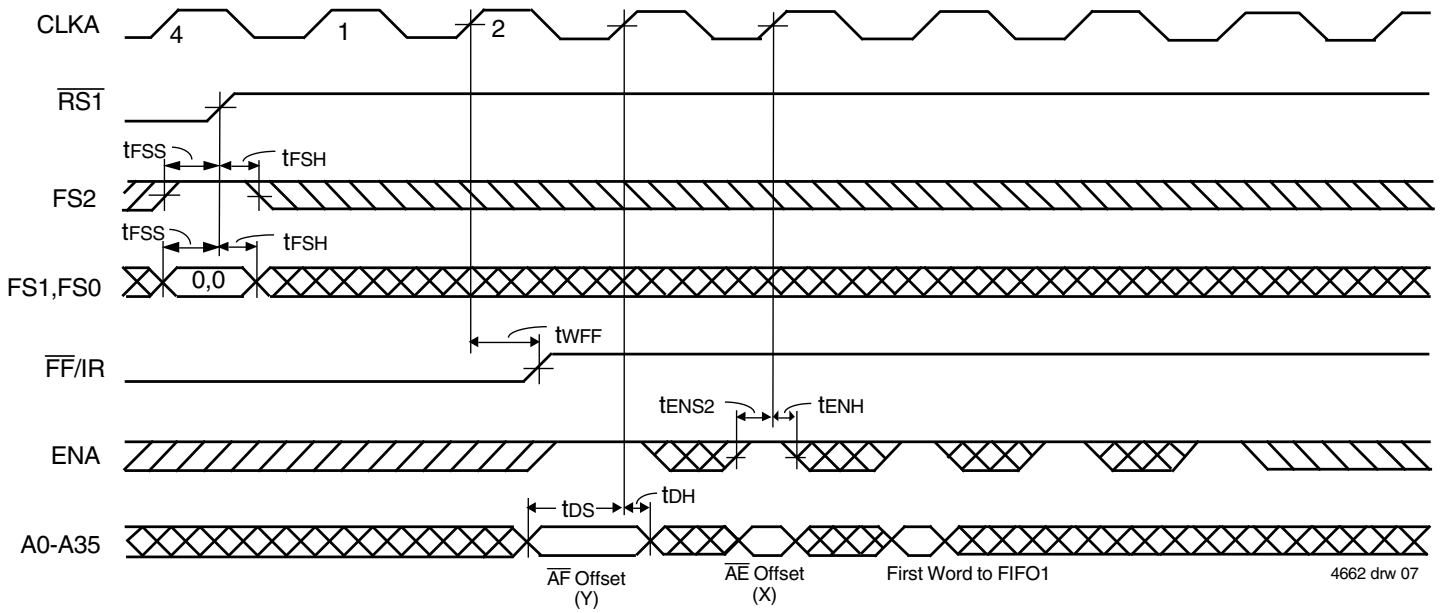
Figure 3. Reset and Loading X and Y with a Preset Value of Eight (IDT Standard and FWFT Modes)



NOTES:
1. $\overline{RS1}$ must be HIGH during Partial Reset.
2. If BE/$\overline{FWFT}$ is HIGH, then $\overline{EF}$/OR will go LOW one CLKB cycle earlier than in this case where BE/$\overline{FWFT}$ is LOW.

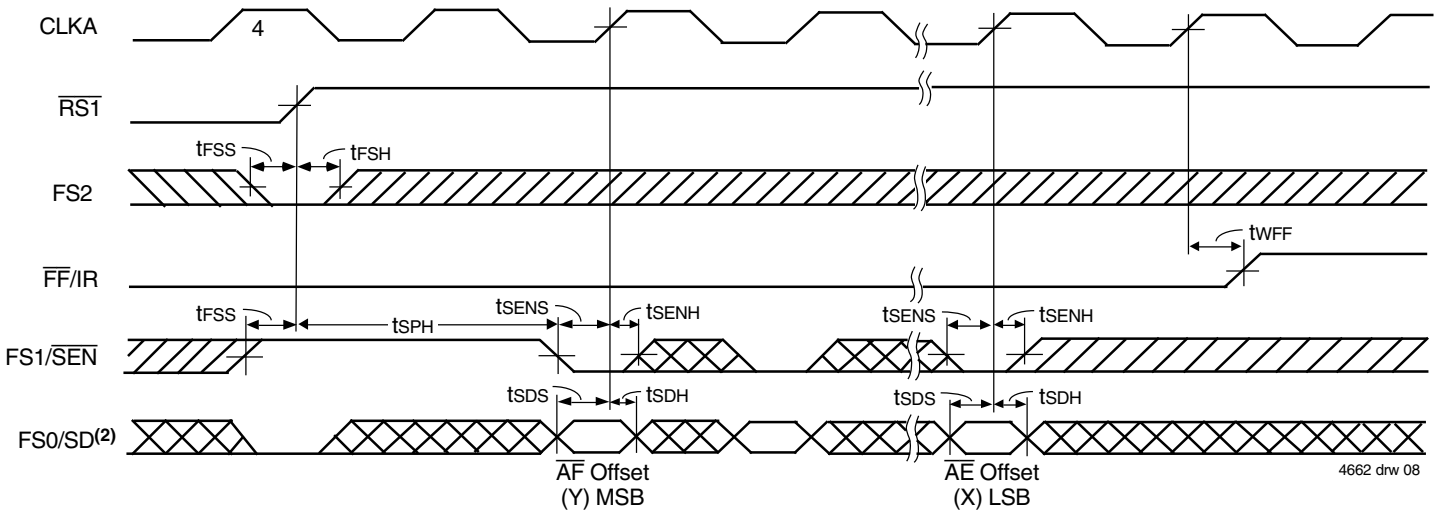
Figure 4. Partial Reset (IDT Standard and FWFT Modes)

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NOTE:
1. $\overline{CSA}$ = LOW, W/$\overline{RA}$ = HIGH, MBA = LOW.

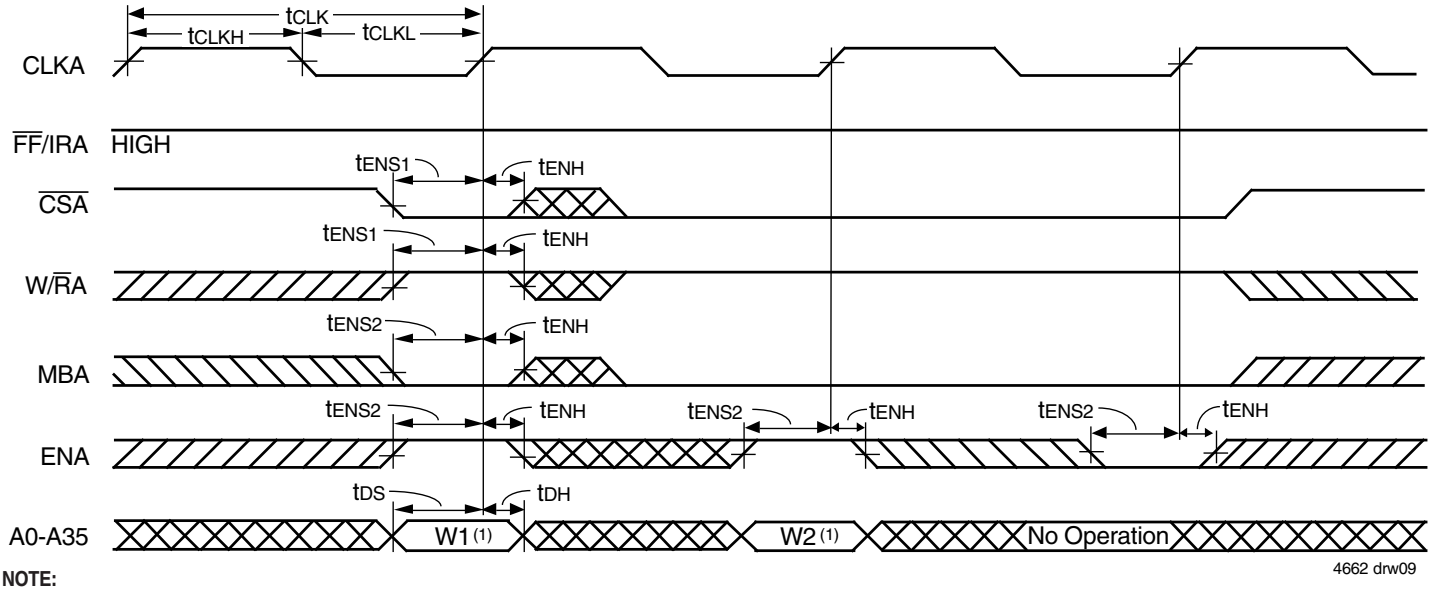
Figure 5. Parallel Programming of the Almost-Full Flag and Almost-Empty Flag Offset Values after Reset (IDT Standard and FWFT Modes)



NOTES:
1. It is not necessary to program offset register bits on consecutive clock cycles. FIFO write attempts are ignored until $\overline{FF}$/IR is set HIGH.
2. Programmable offsets are written serially to the SD input in the order $\overline{AF}$ offset (Y) and $\overline{AE}$ offset (X).

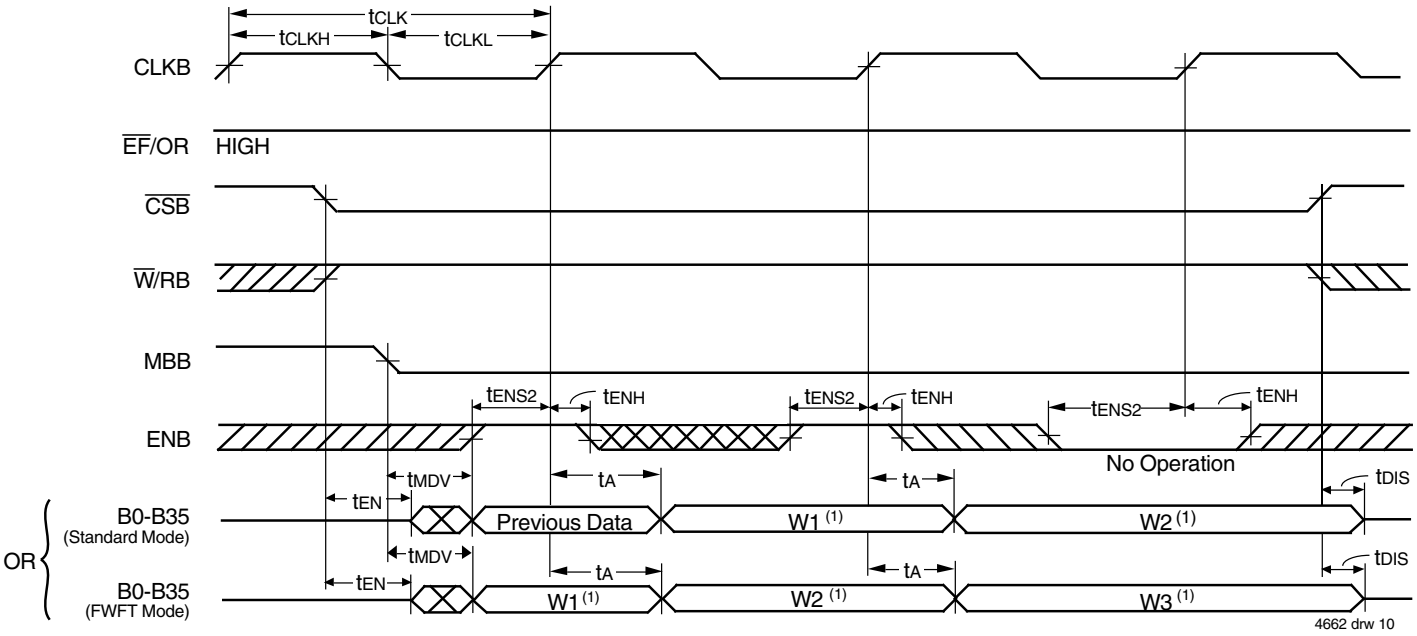
Figure 6. Serial Programming of the Almost-Full Flag and Almost-Empty Flag Offset Values after Reset (IDT Standard and FWFT Modes)

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NOTE:
1. Written to FIFO.

Figure 7. Port A Write Cycle Timing for FIFO (IDT Standard and FWFT Modes)



NOTE:
1. Data read from the FIFO

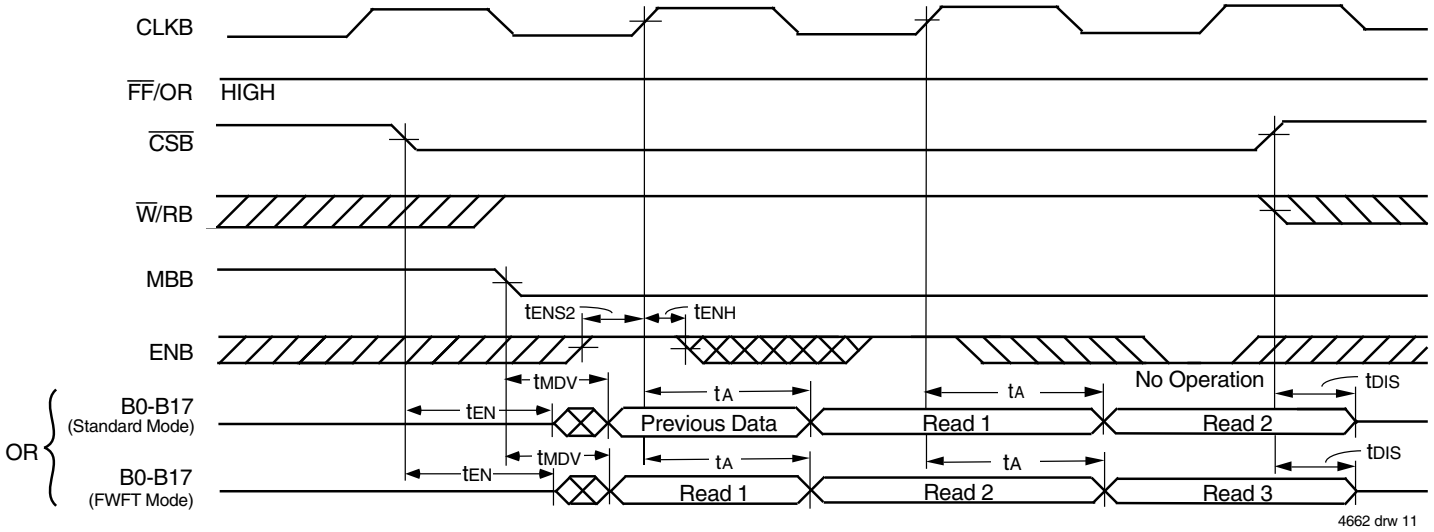
DATA SIZE TABLE FOR FIFO LONG-WORD READS

SIZE MODE(1) (SELECT AT RESET)			DATA WRITTEN TO FIFO				DATA READ FROM FIFO			
BM	**SIZE**	**BE**	**A35-A27**	**A26-A18**	**A17-A9**	**A8-A0**	**B35-B27**	**B26-B18**	**B17-B9**	**B8-B0**
L	X	X	A	B	C	D	A	B	C	D

NOTE:
1. BE is selected at Reset: BM and SIZE must be static throughout device operation.

Figure 8. Port B Long-Word Read Cycle (IDT Standard and FWFT Modes)

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NOTE:
1. Unused word B18-B35 are indeterminate.

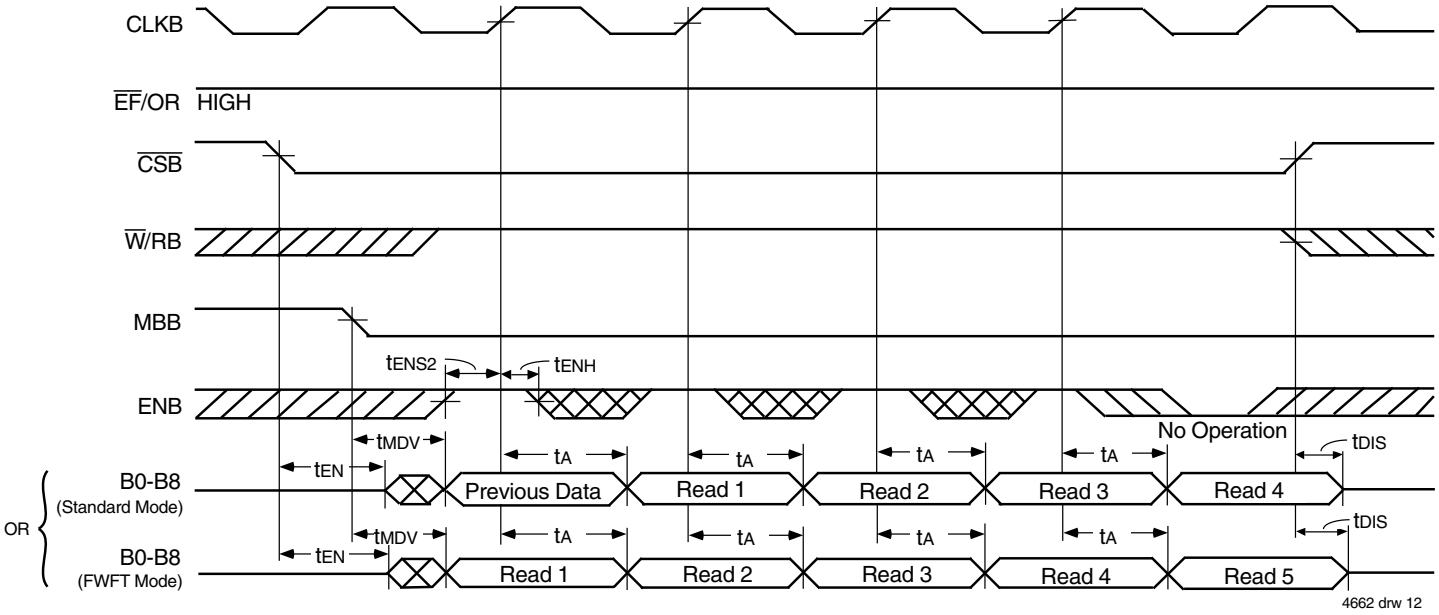
DATA SIZE TABLE FOR WORD READS

SIZE MODE (1)			DATA WRITTEN TO FIFO 1				READ NO.	DATA READ FROM FIFO	
BM	SIZE	BE	A35-A27	A26-A18	A17-A9	A8-A0		B17-B9	B8-B0
H	L	H	A	B	C	D	1 2	A C	B D
H	L	L	A	B	C	D	1 2	C A	D B

NOTE:
1. BE is selected at Reset: BM and SIZE must be static throughout device operation.

Figure 9. Port B Word Read Cycle Timing (IDT Standard and FWFT Modes)

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NOTE:
1. Unused bytes B9-B17, B18-B26, and B27-B35 are indeterminate.

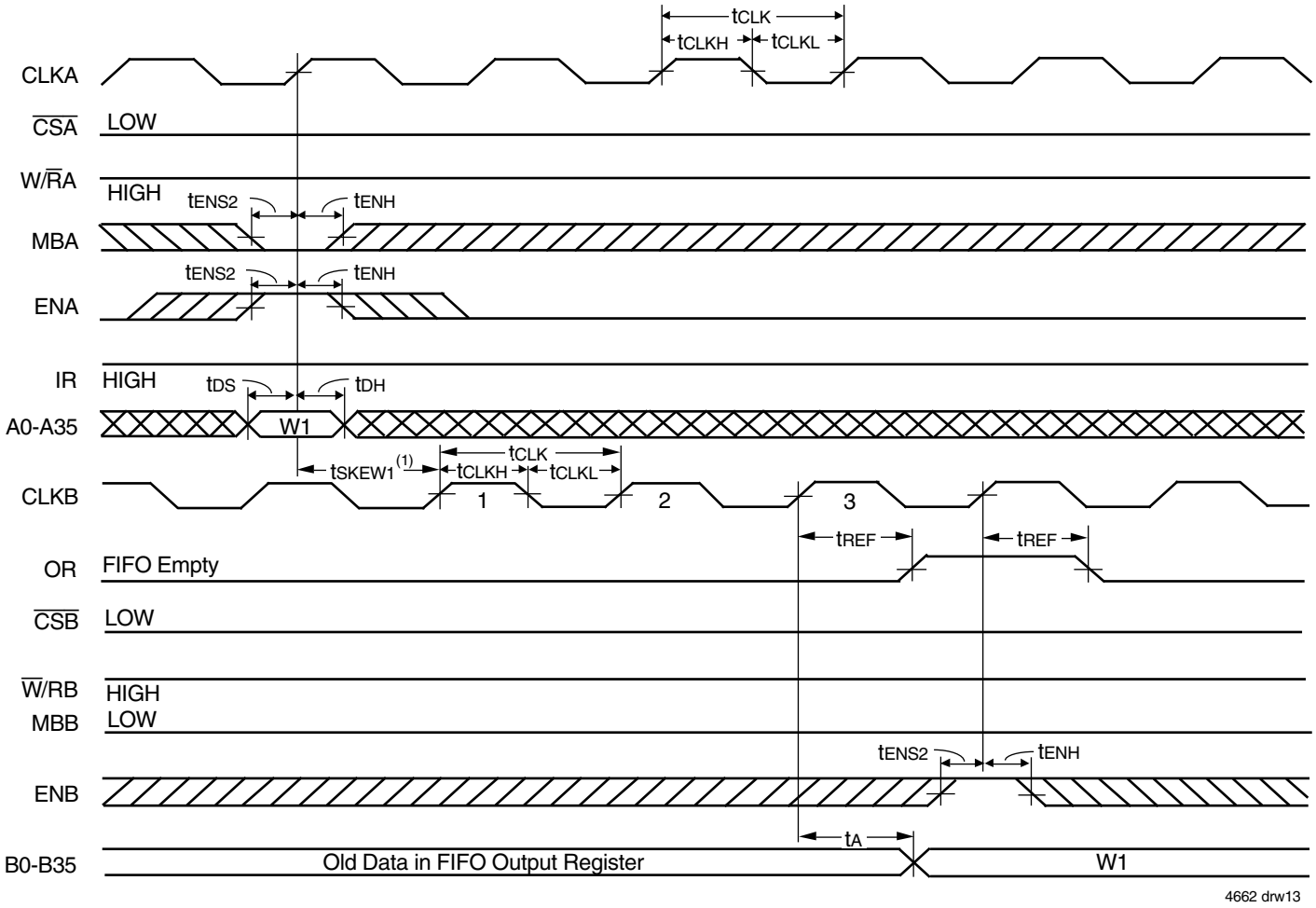
DATA SIZE TABLE FOR BYTE READS

SIZE MODE[1]			DATA WRITTEN TO FIFO				READ NO.	DATA READ FROM FIFO
BM	SIZE	BE	A35-A27	A26-A18	A17-A9	A8-A0		B8-B0
H	H	H	A	B	C	D	1	A
							2	B
							3	C
							4	D
H	H	L	A	B	C	D	1	D
							2	C
							3	B
							4	A

NOTE:
1. BE is selected at Reset: BM and SIZE must be static throughout device operation.

Figure 10. Port B Byte Read Cycle Timing (IDT Standard and FWFT Modes)

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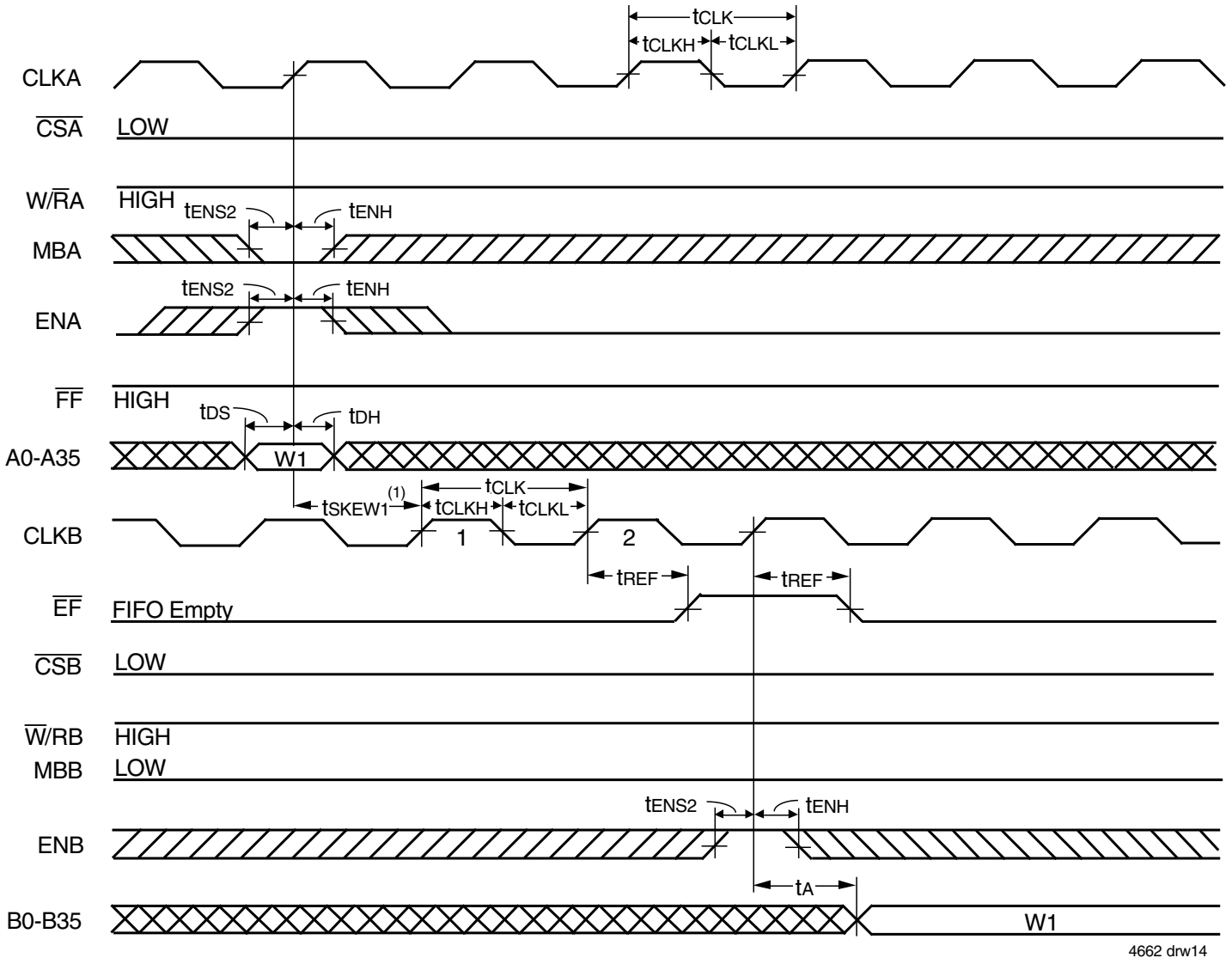


NOTES:

1. t_{SKEW1} is the minimum time between a rising CLKA edge and a rising CLKB edge for OR to transition HIGH and to clock the next word to the FIFO output register in three CLKB cycles. If the time between the rising CLKA edge and rising CLKB edge is less than t_{SKEW1}, then the transition of OR HIGH and load of the first word to the output register may occur one CLKB cycle later than shown.
2. If Port B size is word or byte, OR is set LOW by the last word or byte read from the FIFO, respectively.

Figure 11. OR Flag Timing and First Data Word Fall Through when FIFO is Empty (FWFT Mode)

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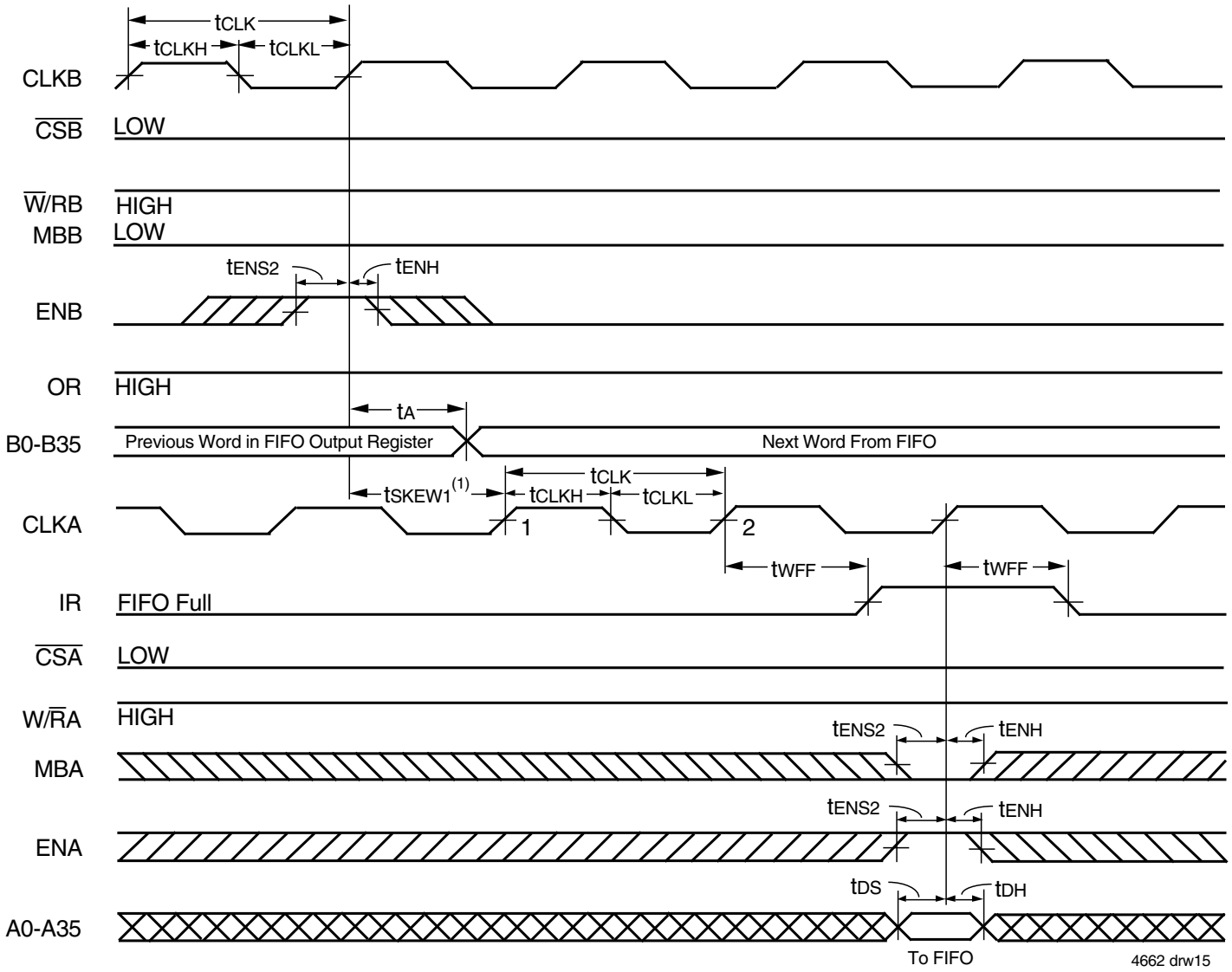


NOTES:

1. t_{SKEW1} is the minimum time between a rising CLKA edge and a rising CLKB edge for $\overline{EF}$ to transition HIGH in the next CLKB cycle. If the time between the rising CLKA edge and rising CLKB edge is less than t_{SKEW1}, then the transition of $\overline{EF}$ HIGH may occur one CLKB cycle later than shown.
2. If Port B size is word or byte, $\overline{EF}$ is set LOW by the last word or byte read from the FIFO, respectively.

Figure 12. $\overline{EF}$ Flag Timing and First Data Read when FIFO is Empty (IDT Standard Mode)

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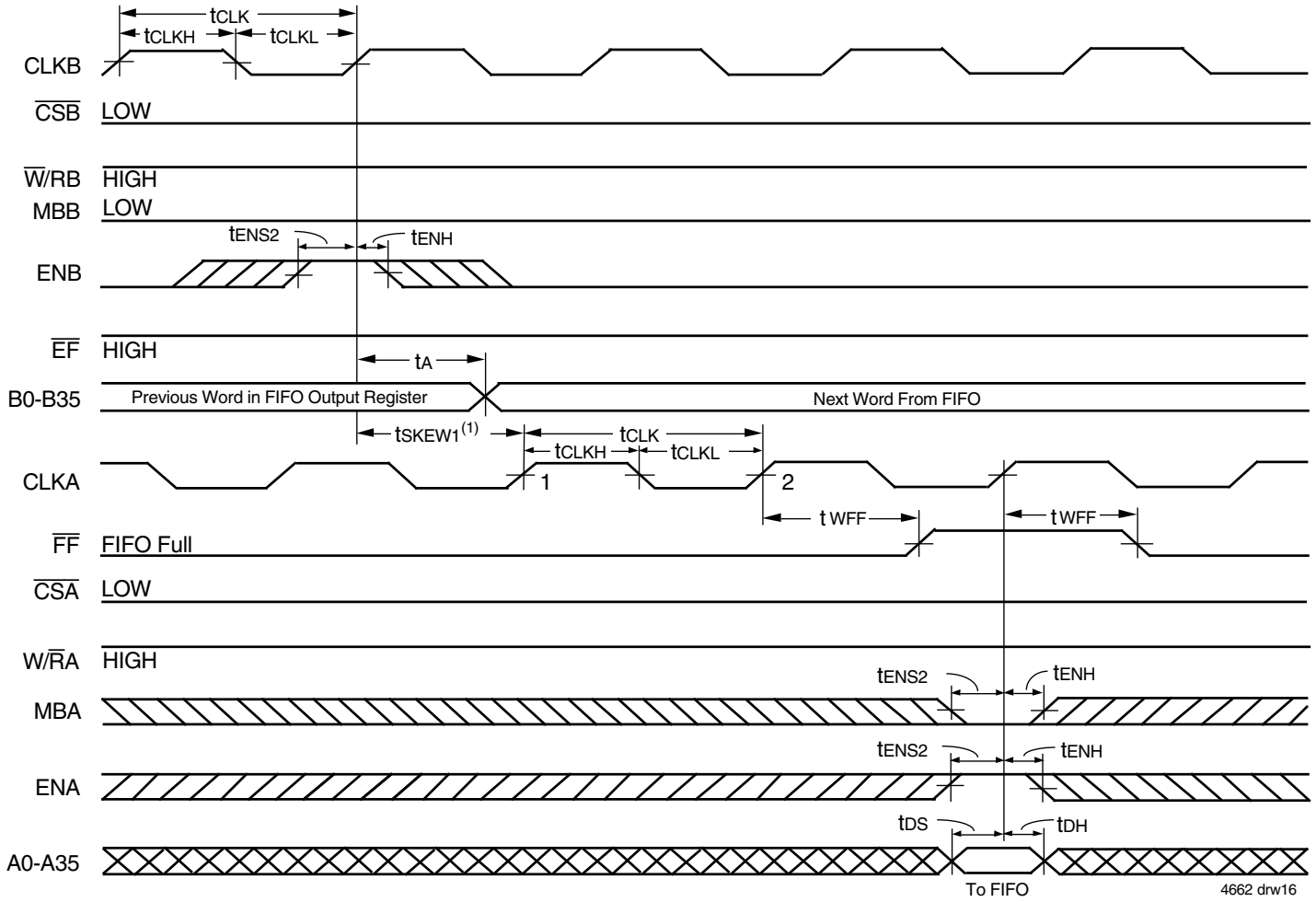


NOTES:

1. t_{SKEW1} is the minimum time between a rising CLKB edge and a rising CLKA edge for IR to transition HIGH in the next CLKA cycle. If the time between the rising CLKB edge and rising CLKA edge is less than t_{SKEW1}, then IR may transition HIGH one CLKA cycle later than shown.
2. If Port B size is word or byte, t_{SKEW1} is referenced to the rising CLKB edge that reads the last word or byte write of the long word, respectively.

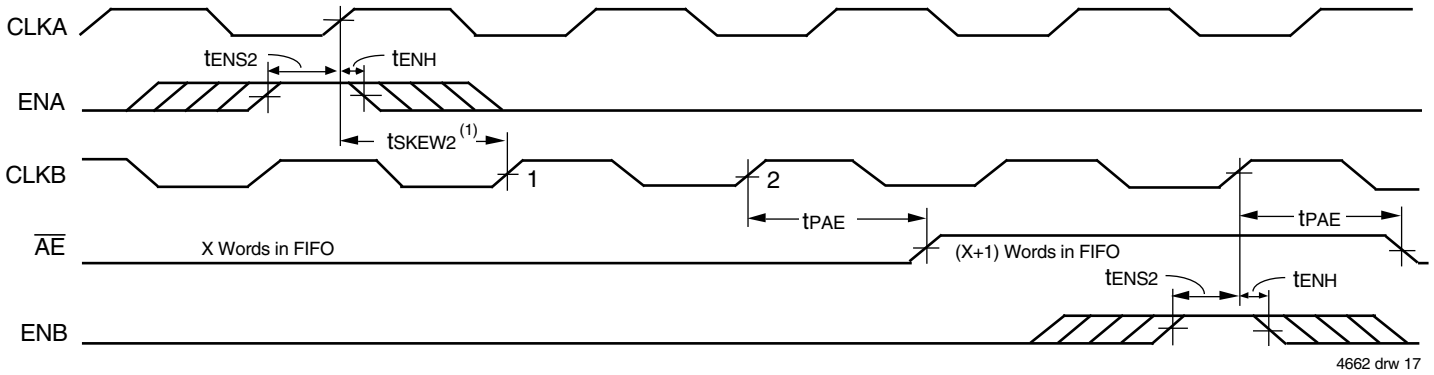
Figure 13. IR Flag Timing and First Available Write when FIFO is Full (FWFT Mode)

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NOTES:
1. tSKEW1 is the minimum time between a rising CLKB edge and a rising CLKA edge for FF to transition HIGH in the next CLKA cycle. If the time between the rising CLKB edge and rising CLKA edge is less than tSKEW1, then FF may transition HIGH one CLKA cycle later than shown.
2. If Port B size is word or byte, tSKEW1 is referenced from the rising CLKB edge that reads the last word or byte of the long word, respectively.

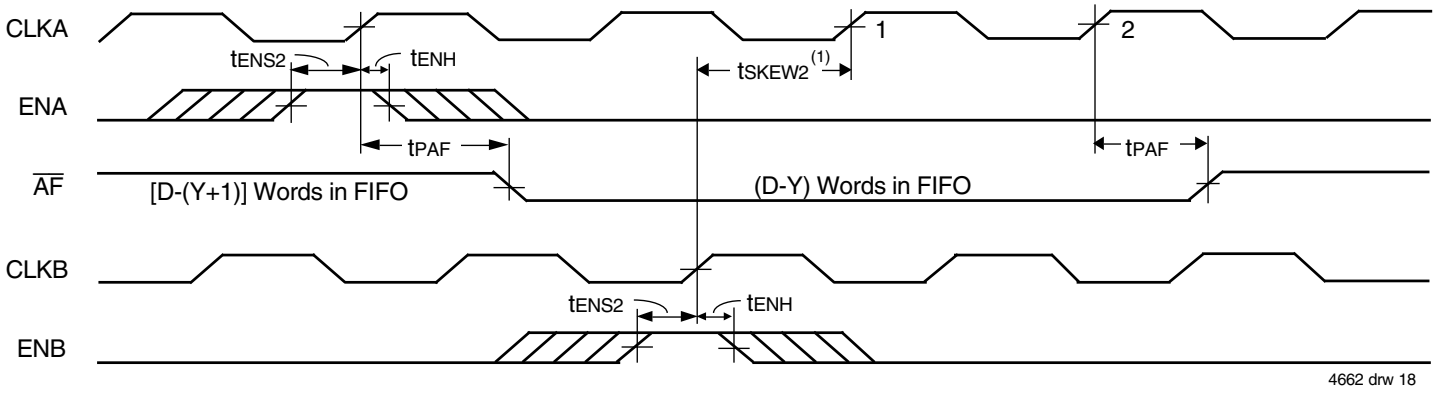
Figure 14. FF Flag Timing and First Available Write when FIFO is Full (IDT Standard Mode)



NOTES:
1. tSKEW2 is the minimum time between a rising CLKA edge and a rising CLKB edge for AE to transition HIGH in the next CLKB cycle. If the time between the rising CLKA edge and rising CLKB edge is less than tSKEW2, then AE may transition HIGH one CLKB cycle later than shown.
2. FIFO Write (CSA = LOW, W/RA = LOW, MBA = LOW), FIFO read (CSB = LOW, W/RB = HIGH, MBB = LOW). Data in the FIFO output register has been read from the FIFO.
3. If Port B size is word or byte, AE is set LOW by the last word or byte read from the FIFO, respectively.

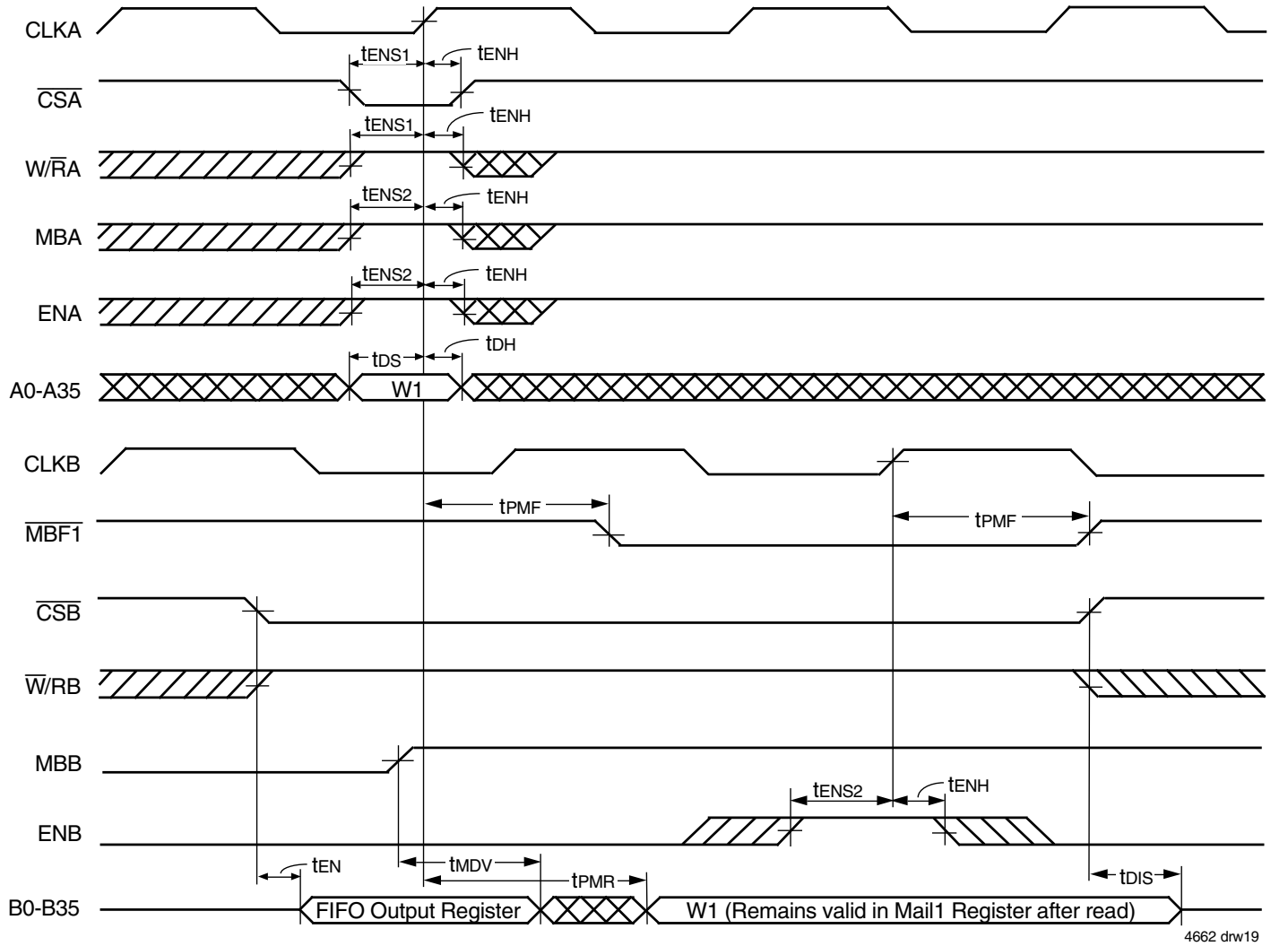
Figure 15. Timing for AE when the FIFO is Almost-Empty (IDT Standard and FWFT Modes).

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NOTES:
1. t_{SKEW2} is the minimum time between a rising CLKA edge and a rising CLKB edge for $\overline{AF}$ to transition HIGH in the next CLKA cycle. If the time between the rising CLKA edge and rising CLKB edge is less than t_{SKEW2}, then $\overline{AF}$ may transition HIGH one CLKA cycle later than shown.
2. FIFO Write ($\overline{CSA}$ = LOW, W/$\overline{RA}$ = HIGH, MBA = LOW), FIFO read ($\overline{CSB}$ = LOW, $\overline{W}$/RB = HIGH, MBB = LOW). Data in the FIFO output register has been read from the FIFO.
3. D = Maximum FIFO Depth = 2,048 for the IDT72V3653, 4,096 for the IDT72V3663, 8,192 for the IDT72V3673.
4. If Port B size is word or byte, t_{SKEW2} is referenced from the rising CLKB edge that reads the last word or byte of the long word, respectively.

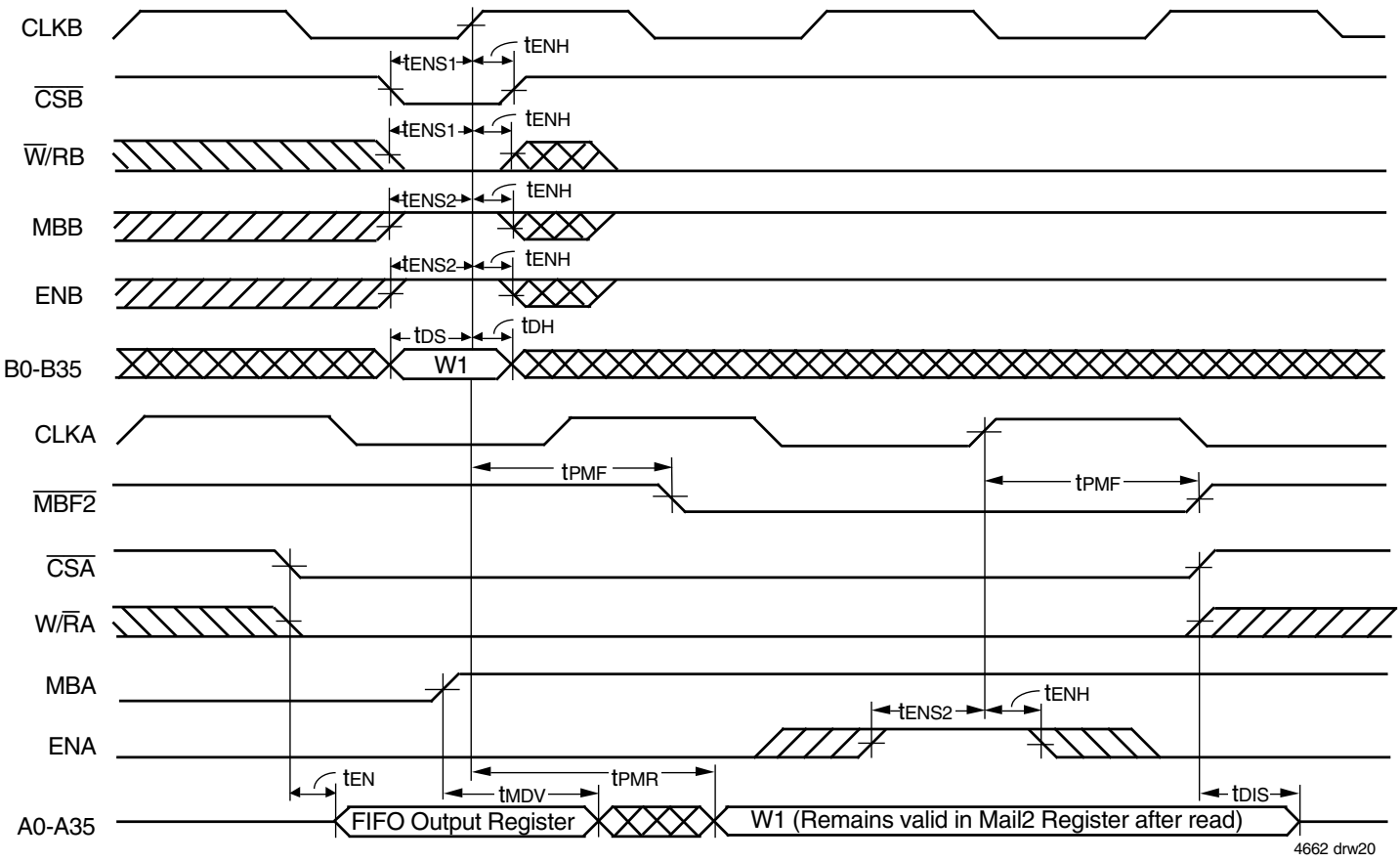
Figure 16. Timing for $\overline{AF}$ when the FIFO is Almost-Full (IDT Standard and FWFT Modes).



NOTE:
1. If Port B is configured for word size, data can be written to the Mail1 Register using A0-A17 (A18-A35 are don't care inputs). In this first case B0-B17 will have valid data (B18-B35 will be indeterminate). If Port B is configured for byte size, data can be written to the Mail1 Register using A0-A8 (A9-A35 are don't care inputs). In this second case, B0-B8 will have valid data (B9-B35 will be indeterminate).

Figure 17. Timing for Mail1 Register and $\overline{MBF1}$ Flag (IDT Standard and FWFT Modes)

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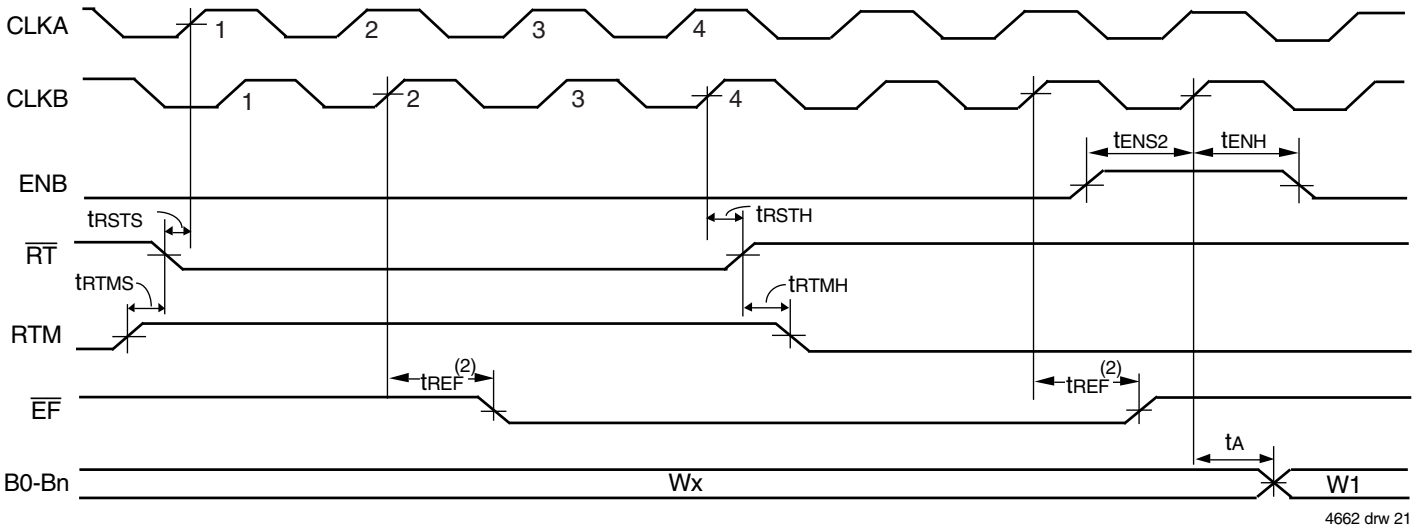


NOTE:

1. If Port B is configured for word size, data can be written to the Mail2 Register using B0-B17 (B18-B35 are don't care inputs). In this first case A0-A17 will have valid data (A18-A35 will be indeterminate). If Port B is configured for byte size, data can be written to the Mail2 Register using B0-B8 (B9-B35 are don't care inputs). In this second case, A0-A8 will have valid data (A9-A35 will be indeterminate).

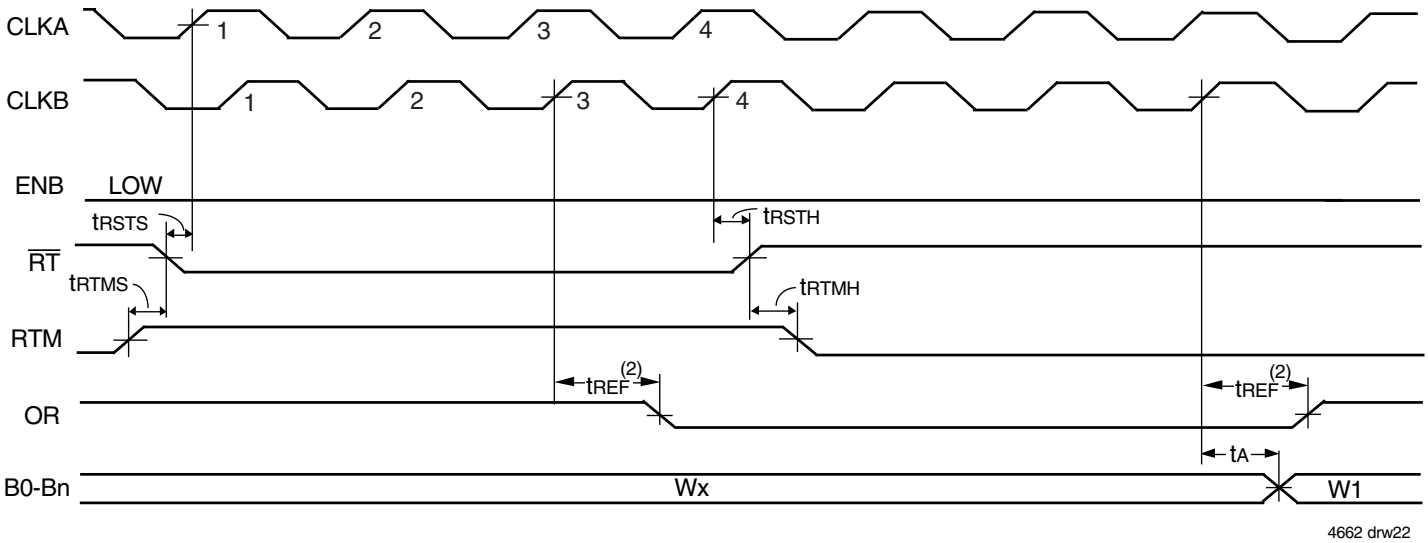
Figure 18. Timing for Mail2 Register and $\overline{\text{MBF2}}$ Flag (IDT Standard and FWFT Modes)

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NOTE:
1. $\overline{CSB}$ = LOW; $\overline{W}$/RB is HIGH
2. Retransmit setup is complete after $\overline{EF}$ returns HIGH, only then can a read operation begin.
3. W1 = first word written to the FIFO after Master Reset.
4. No more than D-2 may be written to the FIFO between Reset (Master or Partial) and Retransmit setup. Therefore, $\overline{FF}$ will be LOW throughout the Retransmit setup procedure. D = 2,048, 4,096 and 8,192 for the IDT72V3653, IDT72V3663 and IDT72V3673 respectively.

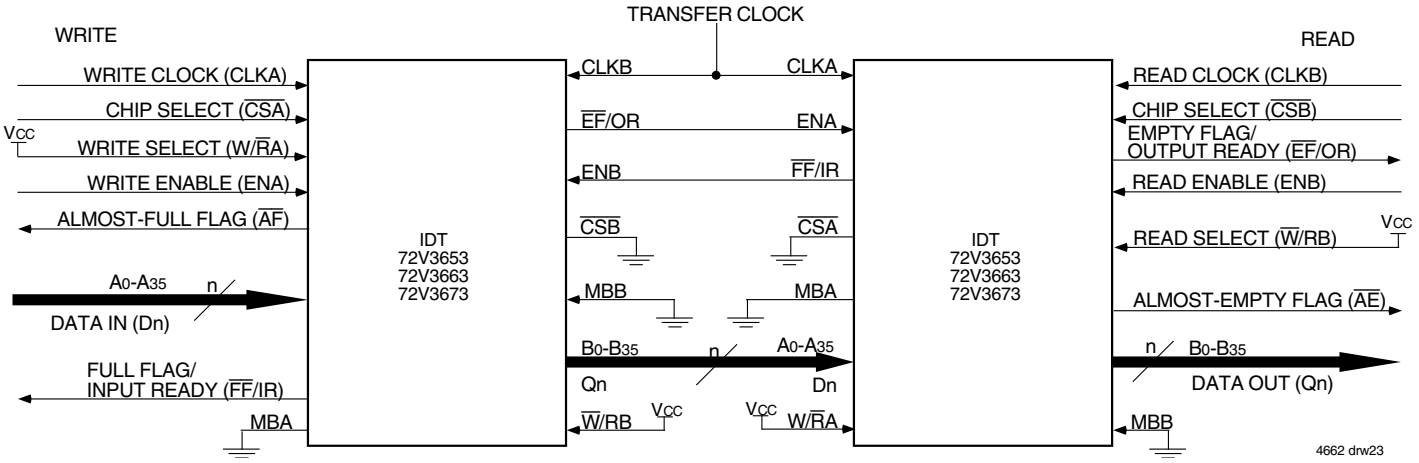
Figure 19. Retransmit Timing (IDT Standard Mode)



NOTE:
1. $\overline{CSB}$ = LOW; $\overline{W}$/RB is HIGH
2. Retransmit setup is complete after OR returns HIGH, only then can a read operation begin.
3. W1 = first word written to the FIFO after Master Reset.
4. No more than D-2 may be written to the FIFO between Reset (Master or Partial) and Retransmit setup. Therefore, $\overline{IR}$ will be LOW throughout the Retransmit setup procedure. D = 2,048, 4,096 and 8,192 for the IDT72V3653, IDT72V3663 and IDT72V3673 respectively.

Figure 20. Retransmit Timing (FWFT Mode)

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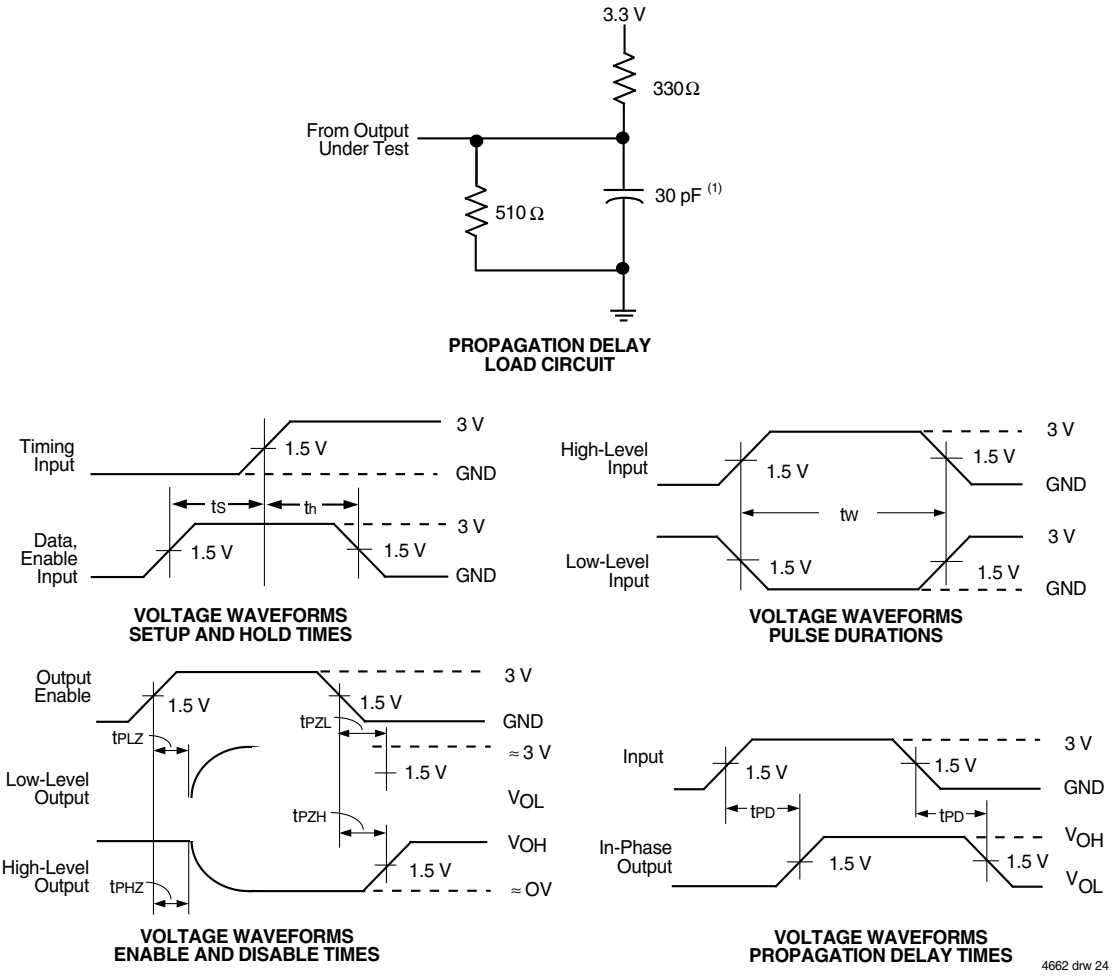


NOTES:
1. Mailbox feature is not supported in depth expansion applications. (MBA + MBB tie to GND)
2. Transfer clock should be set either to the Write Port Clock (CLKA) or the Read Port Clock (CLKB), whichever is faster.
3. The amount of time it takes for EF/OR of the last FIFO in the chain to go HIGH (i.e. valid data to appear on the last FIFO's outputs) after a word has been written to the first FIFO is the sum of the delays for each individual FIFO: (N - 1)*(4*transfer clock) + 3*TRCLK, where N is the number of FIFOs in the expansion and TRCLK is the CLKB period.
4. The amount of time it takes for FF/IR of the first FIFO in the chain to go HIGH after a word has been read from the last FIFO is the sum of the delays for each individual FIFO: (N - 1)*(3*transfer clock) + 2*TWCLK, where N is the number of FIFOs in the expansion and TWCLK is the CLKA period.

Figure 21. Block Diagram of 256 x 36, 512 x 36, 1,024 x 36 Synchronous FIFO Memory with Programmable Flags used in Depth Expansion Configuration

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PARAMETER MEASUREMENT INFORMATION

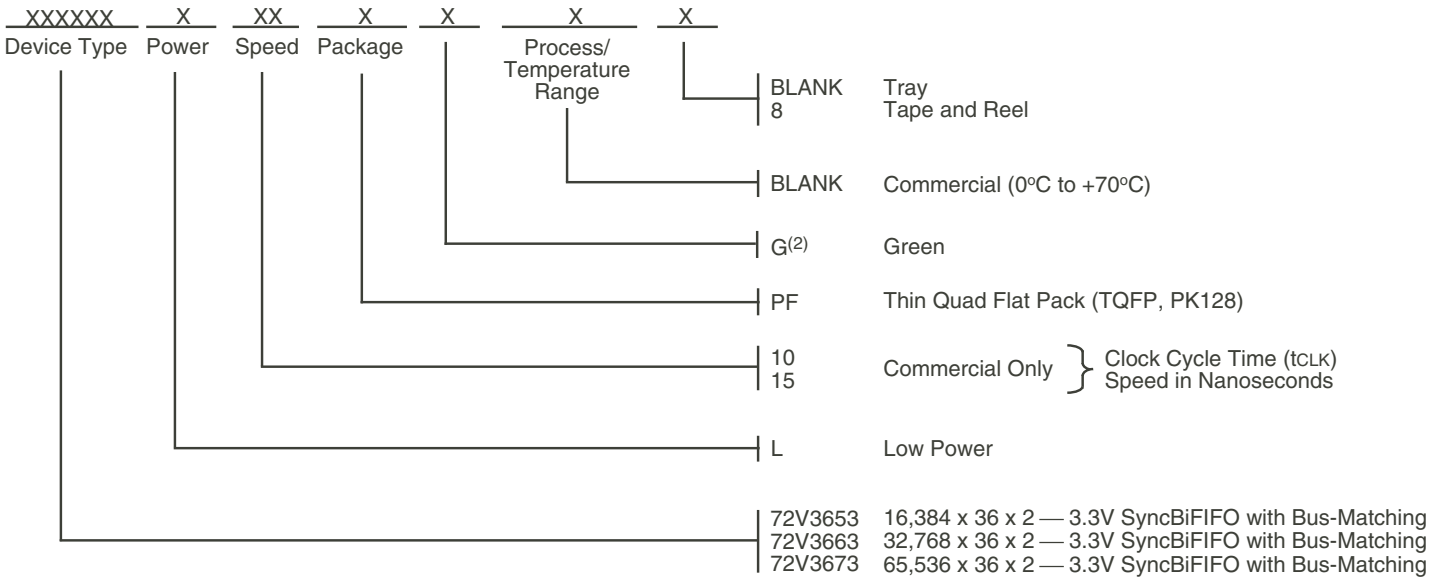


NOTE:
1. Includes probe and jig capacitance.

Figure 22. Load Circuit and Voltage Waveforms.

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ORDERING INFORMATION



4662 drw 25

NOTES:
1. Industrial temperature range is available by special order.
2. Green parts available. For specific speeds and packages contact your sales office.
   LEAD FINISH (SnPb) parts are in EOL process. Product Discontinuation Notice - PDN# SP-17-02

DATASHEET DOCUMENT HISTORY

06/23/2000	pgs. 1-5, 7-9, 11, 12, 14, 17, 18, 21-26, 28 and 29.
09/27/2001	pgs. 5, 6, 7, 8, 9, 12 and 30.
11/03/2003	pg. 1.
02/05/2009	pgs. 1 and 30.
05/13/2016	pgs. 1-3 and 30.
03/22/2018	Product Discontinuation Notice - PDN# SP-17-02 Last time buy expires June 15, 2018.

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