# 1.8V CONFIGURABLE BUFFER WITH ADDRESS-PARITY TEST

**IDT74SSTU32866B**

## FEATURES:

- 1.8V Operation
- SSTL_18 style clock and data inputs
- Differential CLK input
- Configurable as 25-bit 1:1 or 14-bit 1:2 registered buffer
- Control inputs compatible with LVCMOS levels
- Flow-through architecture for optimum PCB design
- Latch-up performance exceeds 100mA
- ESD >2000V per MIL-STD-883, Method 3015; >200V using machine model (C = 200pF, R = 0)
- Checks parity on data inputs
- Available in 96-pin LFBGA package

## APPLICATIONS:

- Along with CSPU877/A/D DDR2-400 PLL, provides complete solution for DDR2-400/533 DIMMs
- Optimized for DDR2-400/533 (PC2-3200/4300) JEDEC Raw Cards E, F, and G

## DESCRIPTION:

This 25-bit 1:1 / 14-bit 1:2 configurable registered buffer is designed for 1.7V to 1.9V $V_{DD}$ operation. In the 1:1 pinout configuration, only one device per DIMM is requred to drive nine SDRAM loads. In the 1:2 pinout configuration, two devices per DIMM are required to drive eighteen SDRAM loads. All inputs are SSTL_18, except reset ($\overline{RESET}$) and control (Cn) inputs, which are LVCMOS. All outputs are edge-controlled circuits optimized for unterminated DIMM loads, and meet SSTL_18 specifications, except the open-drain error ($\overline{QERR}$) output.

The SSTU32866B operates from a differential clock (CLK and $\overline{CLK}$). Data are registered at the crossing of CLK going high and $\overline{CLK}$ going low. Parity is checked on the parity bit (PAR_IN) input which arrives one cycle after the input data to which it applies. The $\overline{QERR}$ output is open drain.

When used as a single device, the C0 and C1 inputs are tied low. In this configuration, the partial-parity-out (PPO) and $\overline{QERR}$ signals are produced two clock cycles after the corresponding data output.

When used in pairs, the C0 input of the first register is tied low and the C0 input of the second register is tied high. The C1 input of both registers are tied high. The $\overline{QERR}$ output of the first SSTU32866B is left floating and the valid error information is latched on the $\overline{QERR}$ output of the second SSTU32866B.

If an error occurs and the $\overline{QERR}$ output is driven low, it stays latched low for two clock cycles or until $\overline{RESET}$ is driven low. The DIMM-dependent signals (DODT, DCKE, $\overline{DCS}$, and $\overline{CSR}$) are not included in the parity check.

The CO input controls the pinout configuration of the 1:2 pinout from register A configuration (when low) to register B configuration (when high). The C1 input controls the pinout configurationfrom 25-bit 1:1 (when low) to 14-bit 1:2 (when high). C0 and C1 should not be switched during normal operation. They should be hard-wired to a valid low or high level to configure the register in the desired mode. In the 25-bit 1:1 pinout configuration, the A6, D6, and H6 terminals are driven low and should not be used.

The device supports low-power standby operation. When $\overline{RESET}$ is low, the differential input recievers are disabled, and undriven (floating) data, clock, and reference voltage ($V_{REF}$) inputs are allowed. In addition, when $\overline{RESET}$ is low, all registers are reset and all outputs except $\overline{QERR}$ are forced low. The LVCMOS $\overline{RESET}$ and Cn inputs always must be held at a valid logic high or low level.

There are two $V_{REF}$ pins (A3 and T3). However, it is necessary to only connect one of the two $V_{REF}$ pins to the external $V_{REF}$ power supply. An unused $V_{REF}$ pin should be terminated with a $V_{REF}$ coupling capacitor.

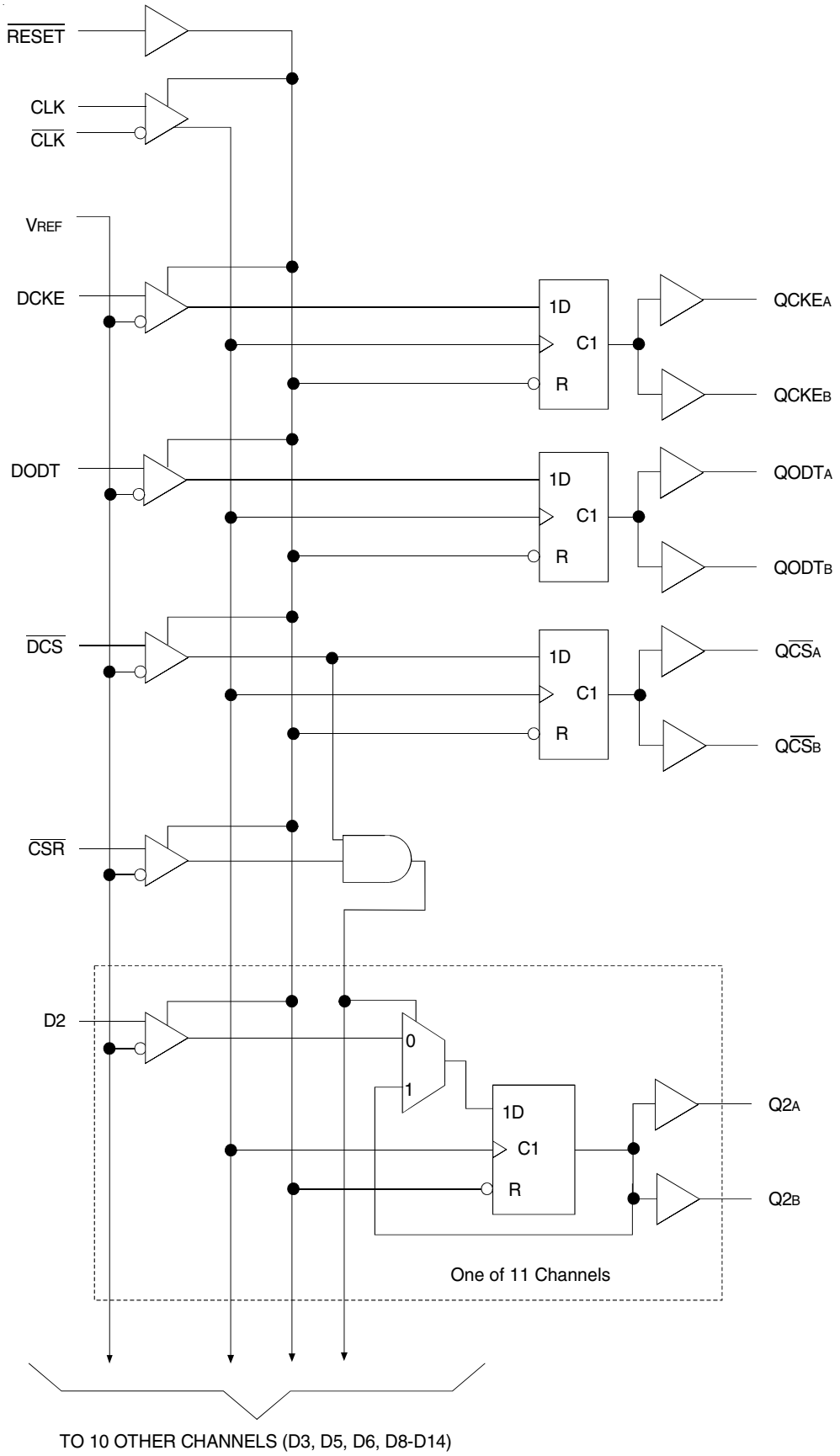
The device also supports low-power active operation by monitoring both system chip select ($\overline{DCS}$ and $\overline{CSR}$) inputs and will gate the Qn and PPO outputs from changing states when both $\overline{DCS}$ and $\overline{CSR}$ inputs are high. If either $\overline{DCS}$ or $\overline{CSR}$ input is low, the Qn and PPO outputs will function normally. Also, if the internal low power signal ($\overline{LPS1}$) is high, the device will gate the $\overline{QERR}$ output from changing states. If $\overline{LPS1}$ is low, the $\overline{QERR}$ output will function normally. The $\overline{RESET}$ input has priority over the $\overline{DCS}$ and $\overline{CSR}$ control and when driven low will force the Qn and PPO outputs low, and the $\overline{QERR}$ output high. If the $\overline{DCS}$ control functionality is not desired, then the $\overline{CSR}$ input can be hard-wired to ground, in which case the setup-time requirement for $\overline{DCS}$ would be the same as for the other D data inputs. To control the low-power mode with $\overline{DCS}$ only, then the $\overline{CSR}$ input should be pulled up to $V_{DD}$ through a pullup resistor.

To ensure defined outputs from the register before a stable clock has been supplied, $\overline{RESET}$ must be held in the low state during power up.



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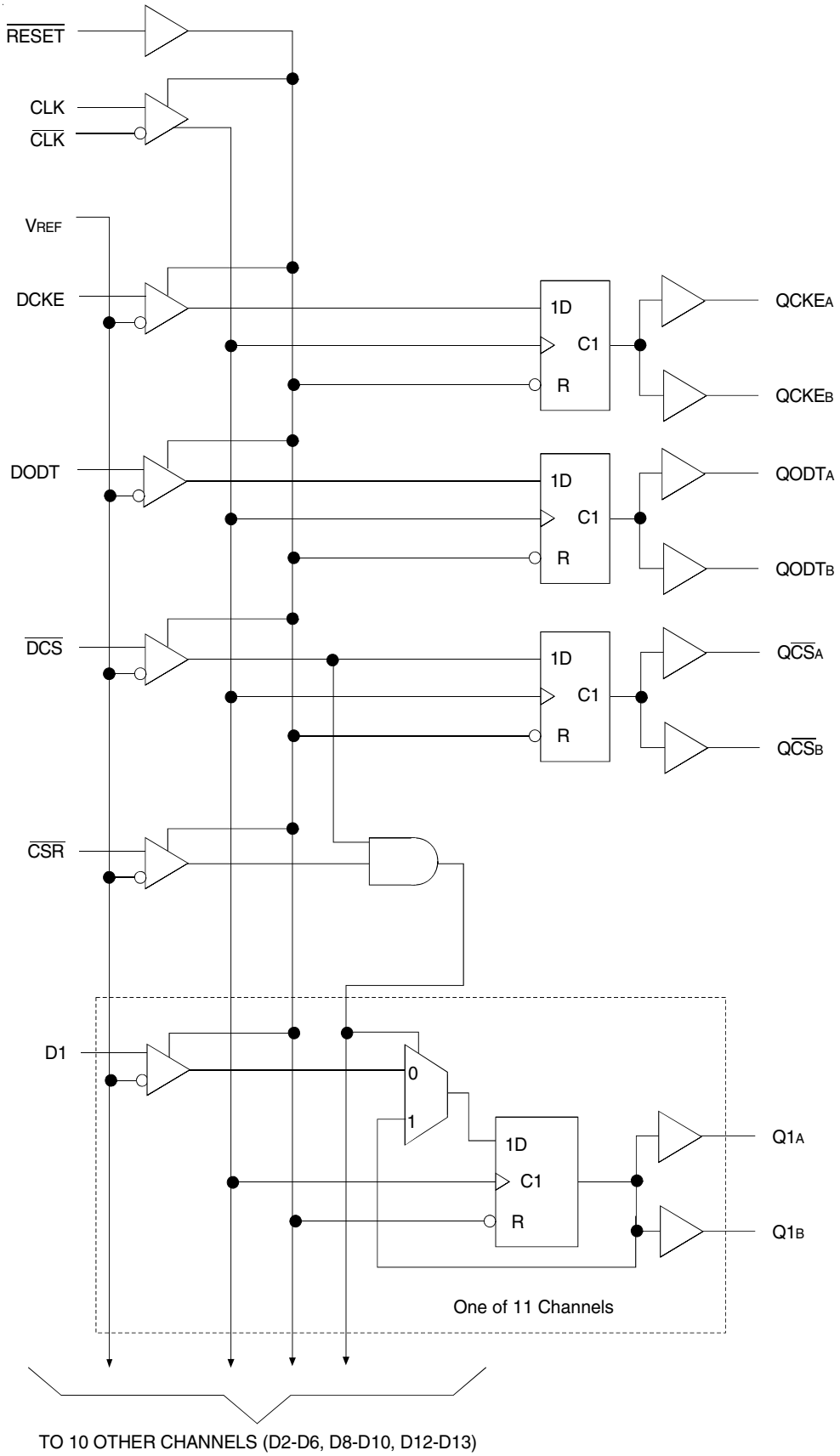
# FUNCTIONAL BLOCK DIAGRAM (1:2) - A CONFIGURATION (POSITIVE LOGIC)





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# FUNCTIONAL BLOCK DIAGRAM (1:2) - B CONFIGURATION (POSITIVE LOGIC)





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## PIN CONFIGURATION (TYPE A)

| | A | B | C | D | E | F | G | H | J | K | L | M | N | P | R | T |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 6 | QCKEB | Q2B | Q3B | QODTB | Q5B | Q6B | C0 | $\overline{QCS}$B | NC | Q8B | Q9B | Q10B | Q11B | Q12B | Q13B | Q14B |
| 5 | QCKEA | Q2A | Q3A | QODTA | Q5A | Q6A | C1 | $\overline{QCS}$A | NC | Q8A | Q9A | Q10A | Q11A | Q12A | Q13A | Q14A |
| 4 | VDD | GND | VDD | GND | VDD | GND | VDD | GND | VDD | GND | VDD | GND | VDD | GND | VDD | VDD |
| 3 | VREF | GND | VDD | GND | VDD | GND | VDD | GND | VDD | GND | VDD | GND | VDD | GND | VDD | VREF |
| 2 | PPO | DNU | DNU | $\overline{QERR}$ | DNU | DNU | $\overline{RESET}$ | $\overline{DCS}$ | $\overline{CSR}$ | DNU | DNU | DNU | DNU | DNU | DNU | DNU |
| 1 | DCKE | D2 | D3 | DODT | D5 | D6 | PAR_IN | CLK | $\overline{CLK}$ | D8 | D9 | D10 | D11 | D12 | D13 | D14 |

96-PIN LFBGA
1:2 REGISTER (TYPE A, FRONTSIDE)
TOP VIEW

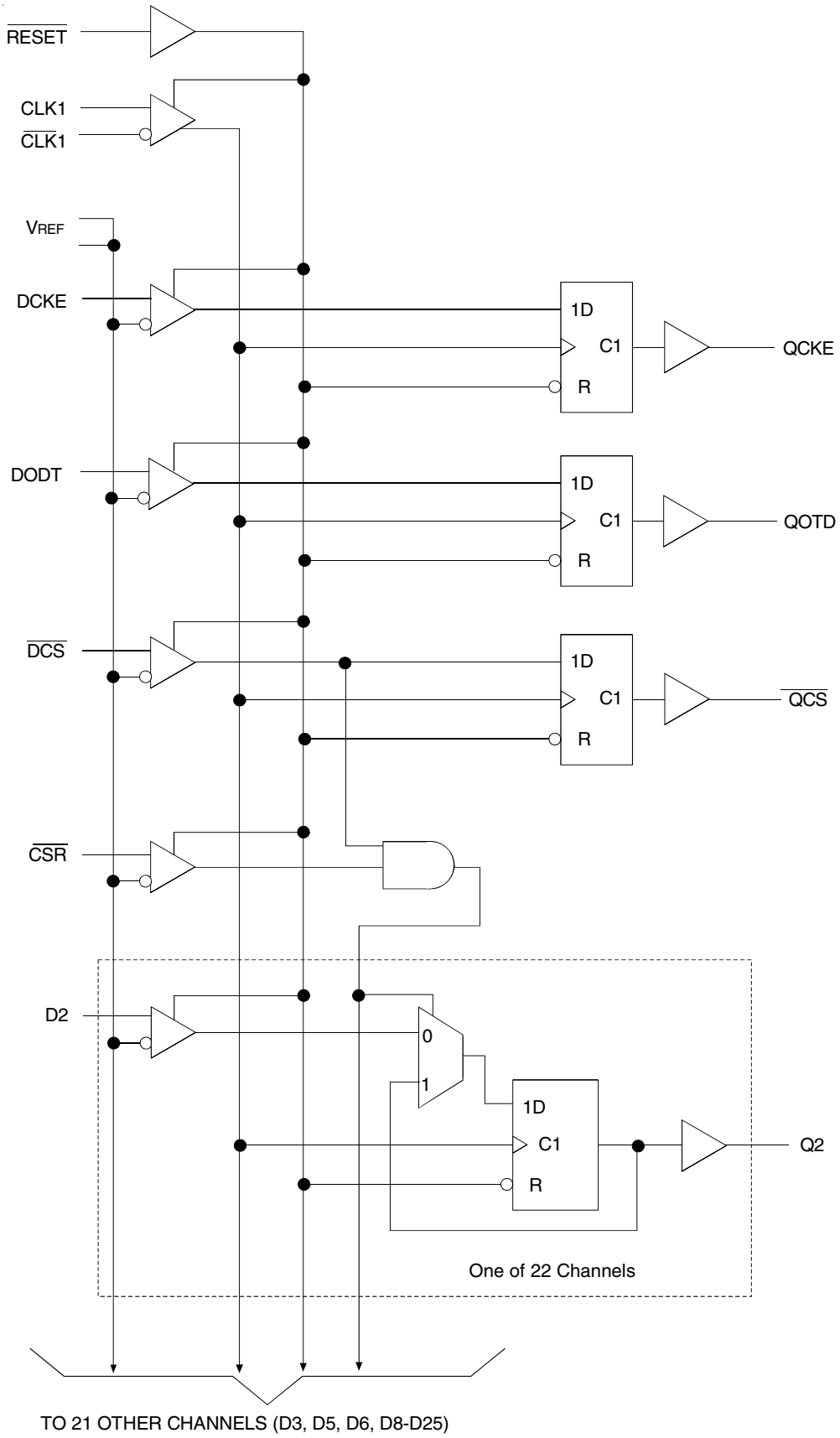
## PIN CONFIGURATION (TYPE B)

| | A | B | C | D | E | F | G | H | J | K | L | M | N | P | R | T |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 6 | Q1B | Q2B | Q3B | Q4B | Q5B | Q6B | C0 | $\overline{QCS}$B | NC | Q8B | Q9B | Q10B | QODTB | Q12B | Q13B | QCKEB |
| 5 | Q1A | Q2A | Q3A | Q4A | Q5A | Q6A | C1 | $\overline{QCS}$A | NC | Q8A | Q9A | Q10A | QODTA | Q12A | Q13A | QCKEA |
| 4 | VDD | GND | VDD | GND | VDD | GND | VDD | GND | VDD | GND | VDD | GND | VDD | GND | VDD | VDD |
| 3 | VREF | GND | VDD | GND | VDD | GND | VDD | GND | VDD | GND | VDD | GND | VDD | GND | VDD | VREF |
| 2 | PPO | DNU | DNU | $\overline{QERR}$ | DNU | DNU | $\overline{RESET}$ | $\overline{DCS}$ | $\overline{CSR}$ | DNU | DNU | DNU | DNU | DNU | DNU | DNU |
| 1 | D1 | D2 | D3 | D4 | D5 | D6 | PAR_IN | CLK | $\overline{CLK}$ | D8 | D9 | D10 | DODT | D12 | D13 | DCKE |

96-PIN LFBGA
1:2 REGISTER (TYPE B, BACKSIDE)
TOP VIEW


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# FUNCTIONAL BLOCK DIAGRAM (1:1)





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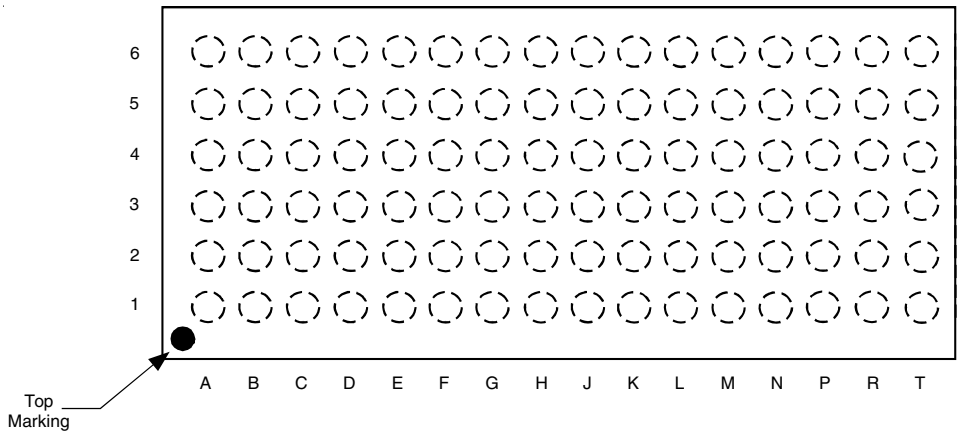
## PIN CONFIGURATION

| | A | B | C | D | E | F | G | H | J | K | L | M | N | P | R | T |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 6 | DNU | Q15 | Q16 | DNU | Q17 | Q18 | C0 | DNU | NC | Q19 | Q20 | Q21 | Q22 | Q23 | Q24 | Q25 |
| 5 | QCKE | Q2 | Q3 | QODT | Q5 | Q6 | C1 | $\overline{QCS}$ | NC | Q8 | Q9 | Q10 | Q11 | Q12 | Q13 | Q14 |
| 4 | VDD | GND | VDD | GND | VDD | GND | VDD | GND | VDD | GND | VDD | GND | VDD | GND | VDD | VDD |
| 3 | VREF | GND | VDD | GND | VDD | GND | VDD | GND | VDD | GND | VDD | GND | VDD | GND | VDD | VREF |
| 2 | PPO | D15 | D16 | $\overline{QERR}$ | D17 | D18 | $\overline{RESET}$ | $\overline{DCS}$ | $\overline{CSR}$ | D19 | D20 | D21 | D22 | D23 | D24 | D25 |
| 1 | DCKE | D2 | D3 | DODT | D5 | D6 | PAR_IN | CLK | $\overline{CLK}$ | D8 | D9 | D10 | D11 | D12 | D13 | D14 |

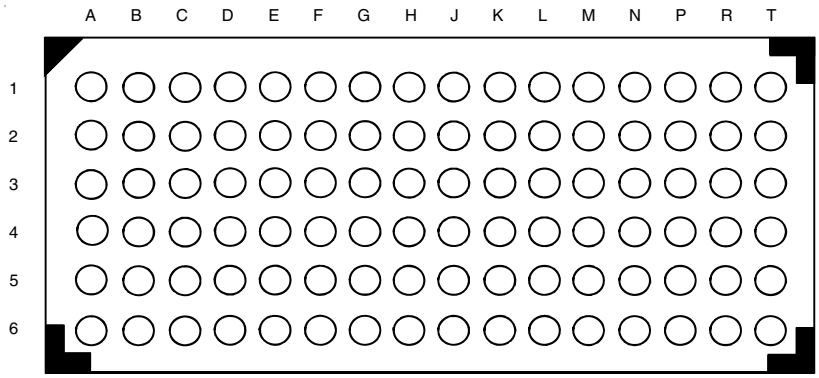
*Rows 3 and 4 are reserved for VDD and GND.

96-PIN LFBGA
1:1 REGISTER
TOP VIEW

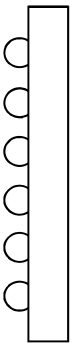
## 96 BALL LFBGA PACKAGE ATTRIBUTES




TOP VIEW




BOTTOM VIEW



SIDE VIEW


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## FUNCTION TABLE (EACH FLIP-FLOP) (1)

| Inputs | | | | | | Qx | Q$\overline{CS}$x | QODTx, QCKEx |
|---|---|---|---|---|---|---|---|---|
| $\overline{RESET}$ | $\overline{DCS}$ | $\overline{CSR}$ | CLK | $\overline{CLK}$ | Dx, DODT, DCKE | Outputs | Output | Outputs |
| H | L | L | ↑ | ↓ | L | L | L | L |
| H | L | L | ↑ | ↓ | H | H | L | H |
| H | L | L | L or H | L or H | X | $Q_0$(2) | $Q_0$(2) | $Q_0$(2) |
| H | L | H | ↑ | ↓ | L | L | L | L |
| H | L | H | ↑ | ↓ | H | H | L | H |
| H | L | H | L or H | L or H | X | $Q_0$(2) | $Q_0$(2) | $Q_0$(2) |
| H | H | L | ↑ | ↓ | L | L | H | L |
| H | H | L | ↑ | ↓ | H | H | H | H |
| H | H | L | L or H | L or H | X | $Q_0$(2) | $Q_0$(2) | $Q_0$(2) |
| H | H | H | ↑ | ↓ | L | $Q_0$(2) | H | L |
| H | H | H | ↑ | ↓ | H | $Q_0$(2) | H | H |
| H | H | H | L or H | L or H | X | $Q_0$(2) | $Q_0$(2) | $Q_0$(2) |
| L | X or Floating | X or Floating | X or Floating | X or Floating | X or Floating | L | L | L |

NOTES:
1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   ↑ = LOW to HIGH
   ↓ = HIGH to LOW
2. Output level before the indicated steady-state conditions were established.

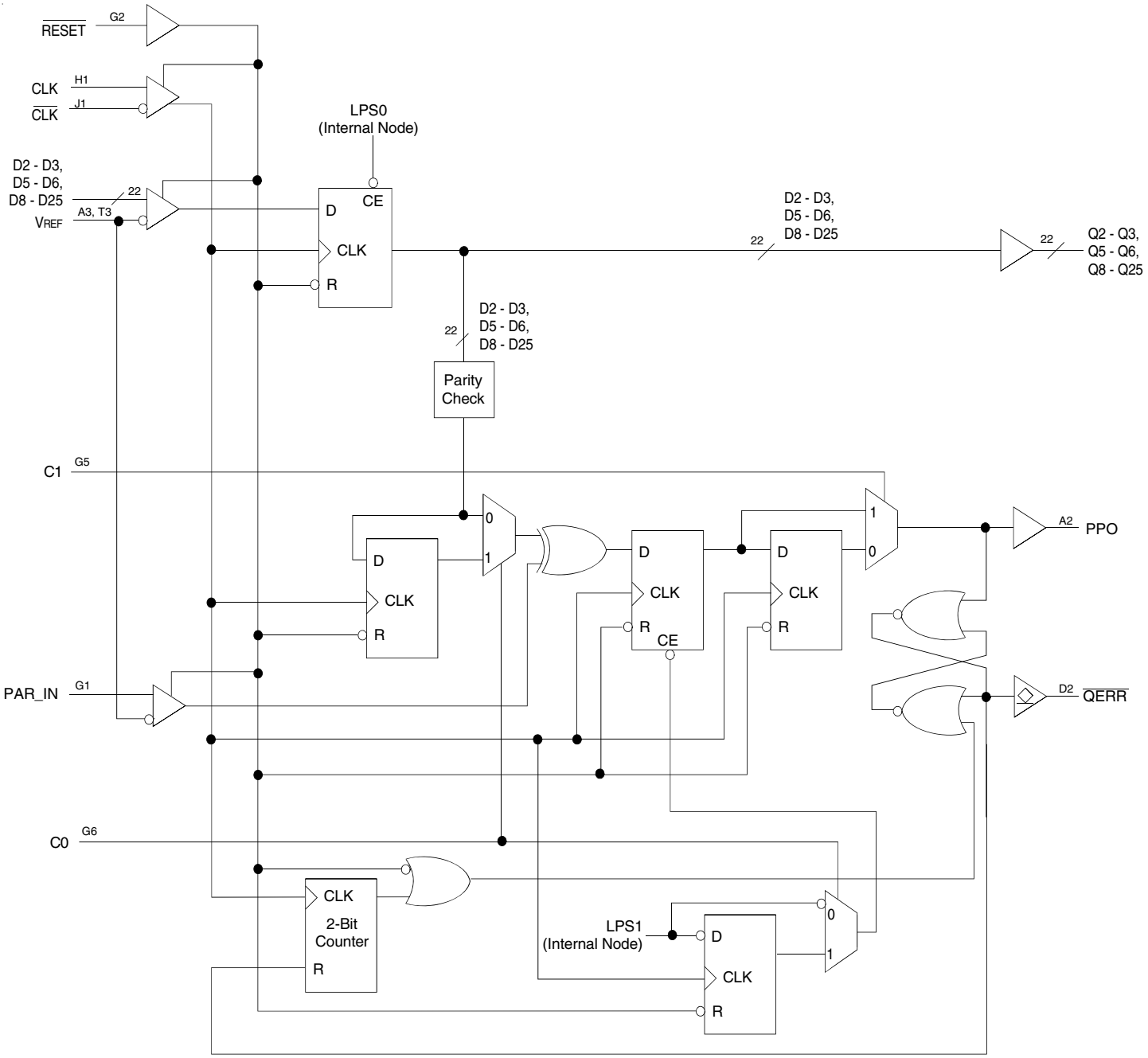
## PARITY AND STANDBY FUNCTION TABLE(1)

| Inputs | | | | | | | Outputs | |
|---|---|---|---|---|---|---|---|---|
| $\overline{RESET}$ | $\overline{DCS}$ | $\overline{CSR}$ | CLK | $\overline{CLK}$ | Σ of Inputs = H (D1 - D25) | PAR_IN(2) | PPO(3) | $\overline{QERR}$(4) |
| H | L | X | ↑ | ↓ | Even | L | L | H |
| H | L | X | ↑ | ↓ | Odd | L | H | L |
| H | L | X | ↑ | ↓ | Even | H | H | L |
| H | L | X | ↑ | ↓ | Odd | H | L | H |
| H | H | L | ↑ | ↓ | Even | L | L | H |
| H | H | L | ↑ | ↓ | Odd | L | H | L |
| H | H | L | ↑ | ↓ | Even | H | H | L |
| H | H | L | ↑ | ↓ | Odd | H | L | H |
| H | H | H | ↑ | ↓ | X | X | $PPO_0$ | $\overline{QERR}_0$ |
| H | X | X | L or H | L or H | X | X | $PPO_0$ | $\overline{QERR}_0$ |
| L | X or Floating | X or Floating | X or Floating | X or Floating | X or Floating | X or Floating | L | H |

NOTES:
1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   ↑ = LOW to HIGH
   ↓ = HIGH to LOW
2. Data Inputs = D2, D3, D5, D6, D8 - D25 when C0 = 0 and C1 = 0.
   Data Inputs = D2, D3, D5, D6, D8 - D14 when C0 = 0 and C1 = 1.
   Data Inputs = D1 - D6, D8 - D10, D12, D13 when C0 = 1 and C1 = 1.
3. PAR_IN arrives one clock cycle (C0 = 0), or two clock cycles (C0 = 1), after the data to which it applies.
4. This transition assumes $\overline{QERR}$ is HIGH at the crossing of CLK going HIGH and $\overline{CLK}$ going LOW. If $\overline{QERR}$ is LOW, it stays latched LOW for two clock cycles or until $\overline{RESET}$ is driven LOW.


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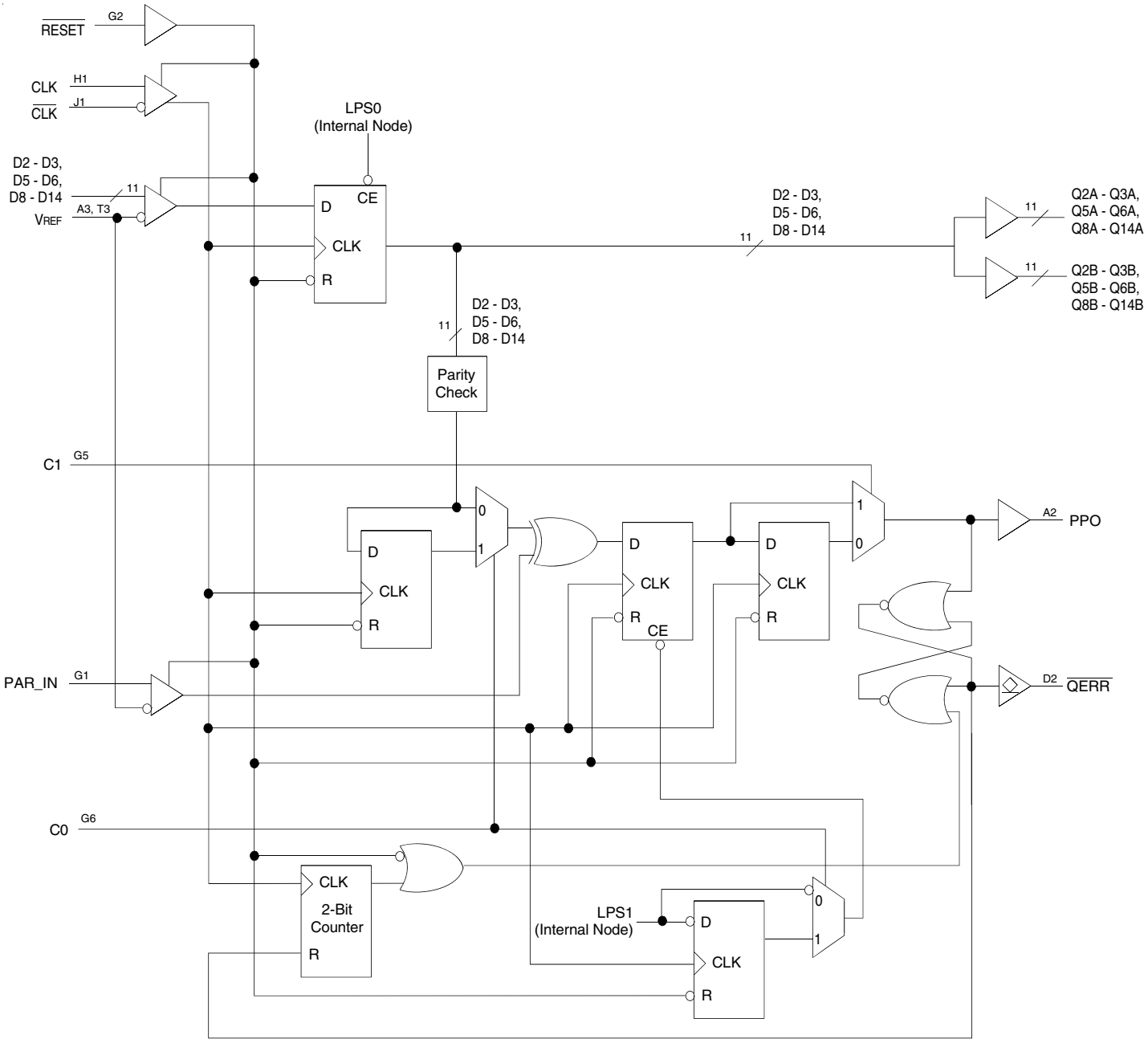
# LOGIC DIAGRAM (1:1)




*Parity Logic Diagram for 1:1 Register - A Configuration (Positive Logic); C0 = 0, C1 = 0*


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# LOGIC DIAGRAM (1:2)




*Parity Logic Diagram for 1:2 Register - A Configuration (Positive Logic); C0 = 0, C1 = 1*


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## ABSOLUTE MAXIMUM RATINGS (1)

| Symbol | Description | | Max. | Unit |
|---|---|---|---|---|
| $V_{DD}$ | Supply Voltage Range | | –0.5 to 2.5 | V |
| $V_I$(2,3) | Input Voltage Range | | –0.5 to 2.5 | V |
| $V_O$(2,3) | Output Voltage Range | | –0.5 to $V_{DD}$ +0.5 | V |
| $I_{IK}$ | Input Clamp Current | $V_I$ < 0 | ±50 | mA |
| | | $V_I$ > $V_{DD}$ | | |
| $I_{OK}$ | Output Clamp Current | $V_O$ < 0 | ±50 | mA |
| | | $V_O$ > $V_{DD}$ | | |
| $I_O$ | Continuous Output Current, $V_O$ = 0 to $V_{DD}$ | | ±50 | mA |
| $V_{DD}$ | Continuous Current through each $V_{DD}$ or GND | | ±100 | mA |
| $T_{STG}$ | Storage Temperature Range | | –65 to +150 | °C |

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. The input and output negative voltage ratings may be exceeded if the ratings of the I/P and O/P clamp current are observed.
3. This value is limited to 2.5V maximum.

## MODE SELECT

| $C_0$ | $C_1$ | Device Mode |
|---|---|---|
| 0 | 0 | 1:1 25-bit to 25-bit |
| 0 | 1 | 1:2 14-bit to 28-bit, Front (Type A) |
| 1 | 0 | Reserved |
| 1 | 1 | 1:2 14-bit to 28-bit, Back (Type B) |

## TERMINAL FUNCTIONS (ALL PINS)

| Terminal Name | Electrical Characteristics | Description |
|---|---|---|
| GND | Ground Input | Ground |
| $V_{DD}$ | 1.8V nominal | Power Supply Voltage |
| $V_{REF}$ | 0.9V nominal | Input Reference Voltage |
| CLK | Differential Input | Positive Master Clock Input |
| $\overline{CLK}$ | Differential Input | Negative Master Clock Input |
| Cx | LVCMOS Input | Configuration Control Inputs |
| $\overline{RESET}$ | LVCMOS Input | Asynchronous Reset Input. Resets registers and disables $V_{REF}$ data and clock differential-input receivers. |
| $\overline{CSR}$, $\overline{DCS}$ | SSTL_18 Input | Chip Select Inputs. Disables outputs Dx switching when both inputs are HIGH. |
| Dx | SSTL_18 Input | Data Input. Clocked in on the crossing of the rising edge of CLK and the falling edge of $\overline{CLK}$. |
| DODT | SSTL_18 Input | The outputs of this register bit will not be suspended by the $\overline{DCS}$ and $\overline{CSR}$ controls |
| DCKE | SSTL_18 Input | The outputs of this register bit will not be suspended by the $\overline{DCS}$ and $\overline{CSR}$ controls |
| Qx | 1.8V CMOS | Data Outputs that are suspended by the $\overline{DCS}$ and $\overline{CSR}$ controls |
| $\overline{QCS}$x | 1.8V CMOS | Data Output that will not be suspended by the $\overline{DCS}$ and $\overline{CSR}$ controls |
| QODTx | 1.8V CMOS | Data Output that will not be suspended by the $\overline{DCS}$ and $\overline{CSR}$ controls |
| QCKEx | 1.8V CMOS | Data Output that will not be suspended by the $\overline{DCS}$ and $\overline{CSR}$ controls |
| PAR_IN | SSTL_18 Input | Parity Input. Clocked on the rising edge of CLK one cycle after corresponding data input. |
| $\overline{QERR}$ | Open Drain Output | Output Error bit, generated one cycle after the corresponding data output |
| PPO | 1.8V CMOS | Partial Parity Output. Indicates ODD parity of Data Inputs and Parity In. |


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## OPERATING CHARACTERISTICS, $T_A$ = 25ºC (1,2)

| Symbol | Parameter | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Supply Voltage | | 1.7 | — | 1.9 | V |
| $V_{REF}$ | Reference Voltage | | 0.49 * $V_{DD}$ | 0.5 * $V_{DD}$ | 0.51 * $V_{DD}$ | V |
| $V_{TT}$ | Termination Voltage | | $V_{REF}$– 40mV | $V_{REF}$ | $V_{REF}$+ 40mV | V |
| $V_I$ | Input Voltage | | 0 | — | $V_{DD}$ | V |
| $V_{IH}$ | AC High-Level Input Voltage | Data Inputs, $\overline{CSR}$, $\overline{DCS}$, PAR_IN | $V_{REF}$+ 250mV | — | — | V |
| $V_{IL}$ | AC Low-Level Input Voltage | | — | — | $V_{REF}$– 250mV | |
| $V_{IH}$ | DC High-Level Input Voltage | | $V_{REF}$+ 125mV | — | — | |
| $V_{IL}$ | DC Low-Level Input Voltage | | — | — | $V_{REF}$– 125mV | |
| $V_{IH}$ | High-Level Input Voltage | $\overline{RESET}$, Cx | 0.65 * $V_{DD}$ | — | — | V |
| $V_{IL}$ | Low-Level Input Voltage | $\overline{RESET}$, Cx | — | — | 0.35 * $V_{DD}$ | V |
| $V_{ICR}$ | Common Mode Input Voltage | CLK, $\overline{CLK}$ | 0.675 | — | 1.125 | V |
| $V_{ID}$ | Differential Input Voltage | CLK, $\overline{CLK}$ | 600 | — | — | mV |
| $I_{OH}$ | High-Level Output Current | Data Outputs, PPO | — | — | –8 | mA |
| $I_{OL}$ | Low-Level Output Current | Data Outputs, PPO, $\overline{QERR}$ | — | — | 8 | |
| $T_A$ | Operating Free-Air Temperature | | 0 | — | 70 | °C |

NOTES:
1. The $\overline{RESET}$ and Cx inputs of the device must be held at valid levels (not floating) to ensure proper device operation.
2. The differential inputs must not be floating unless $\overline{RESET}$ is LOW.

## DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Operating Condition: $T_A$ = 0°C to +70°C, $V_{DD}$ = 1.8V ±0.1V

| Symbol | Parameter | Test Conditions | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $I_{OH}$ = –6 mA | | 1.2 | — | — | V |
| $V_{OL}$ | Output LOW Voltage | $I_{OL}$ = 6 mA | | — | — | 0.5 | V |
| $I_I$ | All Inputs(1) | $V_I$ = $V_{DD}$ or GND | | — | — | ±5 | µA |
| $I_{DD}$ | Static Standby | $I_O$ = 0, $V_{DD}$ = 1.9V, $\overline{RESET}$ = GND | | — | — | 100 | µA |
| | Static Operating | $I_O$ = 0, $V_{DD}$ = 1.9V, $\overline{RESET}$ = $V_{DD}$, $V_I$ = $V_{IH\ (AC)}$ or $V_{IL\ (AC)}$ | | — | — | 40 | mA |
| $I_{DDD}$ | Dynamic Operating (Clock Only) | $I_O$ = 0, $V_{DD}$ = 1.8V, $\overline{RESET}$ = $V_{DD}$, $V_I$ = $V_{IH\ (AC)}$ or $V_{IL\ (AC)}$, CLK and $\overline{CLK}$ Switching 50% Duty Cycle. | | — | — | — | µA/Clock MHz |
| | Dynamic Operating (Per Each Data Input) | $I_O$ = 0, $V_{DD}$ = 1.8V, $\overline{RESET}$ = $V_{DD}$, $V_I$ = $V_{IH\ (AC)}$ or $V_{IL\ (AC)}$, CLK and $\overline{CLK}$ Switching at 50% Duty Cycle. One Data Input Switching at Half Clock Frequency, 50% Duty Cycle. | 1:1 Mode | — | — | — | µA/Clock MHz/Data Input |
| | | | 1:2 Mode | — | — | — | |
| $C_I$ | Data Inputs, $\overline{CSR}$, PAR_IN | | | 2.5 | — | 3.5 | pF |
| | CLK and $\overline{CLK}$ | $V_{ICR}$ = 0.9V, $V_{ID}$ = 600mV | | 2 | — | 3 | |
| | $\overline{RESET}$ | $V_I$ = $V_{DD}$ or GND | | — | — | — | |

NOTE:
1. Each $V_{REF}$ pin (A3, T3) should be tested independently, with the other pin open circuit.


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## TIMING REQUIREMENTS OVER RECOMMENDED OPERATING FREE-AIR TEMPERATURE RANGE

| Symbol | Parameter | | $V_{DD}$ = 1.8V ± 0.1V Min. | $V_{DD}$ = 1.8V ± 0.1V Max. | Unit |
|---|---|---|---|---|---|
| $f_{CLOCK}$ | Clock Frequency | | — | 270 | MHz |
| $t_W$ | Pulse Duration, CLK, $\overline{CLK}$ HIGH or LOW | | 1 | — | ns |
| $t_{ACT}$(1,2) | Differential Inputs Active Time | | — | 10 | ns |
| $t_{INACT}$(1,3) | Differential Inputs Inactive Time | | — | 15 | ns |
| $t_{SU}$ | Setup Time | $\overline{DCS}$ before CLK↑, $\overline{CLK}$↓, $\overline{CSR}$ HIGH; $\overline{CSR}$ before CLK↑, $\overline{CLK}$↓, $\overline{DCS}$ HIGH | 0.7 | — | ns |
| | | $\overline{DCS}$ before CLK↑, $\overline{CLK}$↓, $\overline{CSR}$ LOW | 0.5 | — | |
| | | DODT, DCKE, and data before CLK↑, $\overline{CLK}$↓ | 0.5 | — | |
| | | PAR_IN before CLK↑, $\overline{CLK}$↓ | 0.5 | — | |
| $t_H$ | Hold Time | $\overline{DCS}$ , DODT, DCKE, and data after CLK↑, $\overline{CLK}$↓ | 0.5 | — | ns |
| | | PAR_IN after CLK↑, $\overline{CLK}$↓ | 0.5 | — | |

NOTES:
1. This parameter is not production tested.
2. Data and $V_{REF}$ inputs must be low a minimum time of $t_{ACT}$ max, after $\overline{RESET}$ is taken HIGH.
3. Data, $V_{REF}$, and clock inputs must be held at valid levels (not floating) a minimum time of $t_{INACT}$ max, after $\overline{RESET}$ is taken LOW.

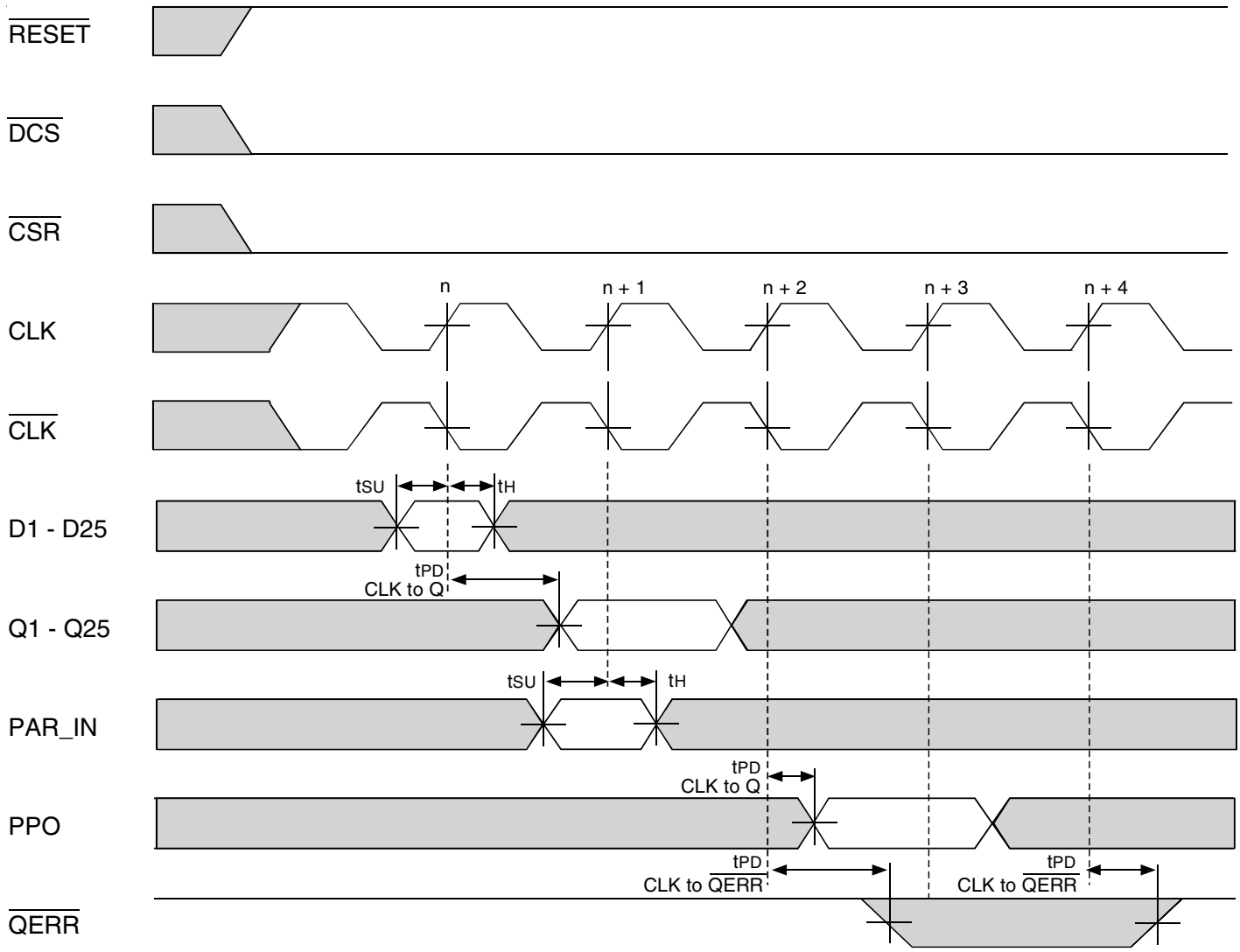
## SWITCHING CHARACTERISTICS OVER RECOMMENDED FREE-AIR OPERATING RANGE (UNLESS OTHERWISE NOTED) (1)

| Symbol | Parameter | $V_{DD}$ = 1.8V ± 0.1V Min | $V_{DD}$ = 1.8V ± 0.1V Max. | Unit |
|---|---|---|---|---|
| $f_{MAX}$ | | 270 | — | MHz |
| $t_{PDM}$(2) | CLK and $\overline{CLK}$ to Q | 1.41 | 2.15 | ns |
| $t_{PDMSS}$(2,3) | CLK and $\overline{CLK}$ to Q (simultaneous switching) | — | 2.35 | ns |
| $t_{RPHL}$ | $\overline{RESET}$ to Q | — | 3 | ns |
| dV/dt_r | Output slew rate from 20% to 80% | 1 | 4 | V/ns |
| dV/dt_f | Output slew rate from 20% to 80% | 1 | 4 | V/ns |
| dV/dt_Δ(4) | Output slew rate from 20% to 80% | — | 1 | V/ns |
| $t_{PD}$ | CLK and $\overline{CLK}$ to PPO | 0.5(5) | 1.8(5) | ns |
| $t_{PLH}$ | CLK and $\overline{CLK}$ to QERR | 1.2(5) | 3(5) | ns |
| $t_{PHL}$ | CLK and $\overline{CLK}$ to QERR | 1(5) | 2.4(5) | ns |
| $t_{RPHL}$ | $\overline{RESET}$ to PPO | — | 3 | ns |
| $t_{RPLH}$ | $\overline{RESET}$ to QERR | — | 3 | ns |

NOTES:
1. See TEST CIRCUITS AND WAVEFORMS.
2. Includes 350ps of test load transmission line delay.
3. This parameter is not production tested.
4. Difference between dV/dt_r (rising edge rate) and dV/dt_f (falling edge rate).
5. For reference only. Final values to be determined.


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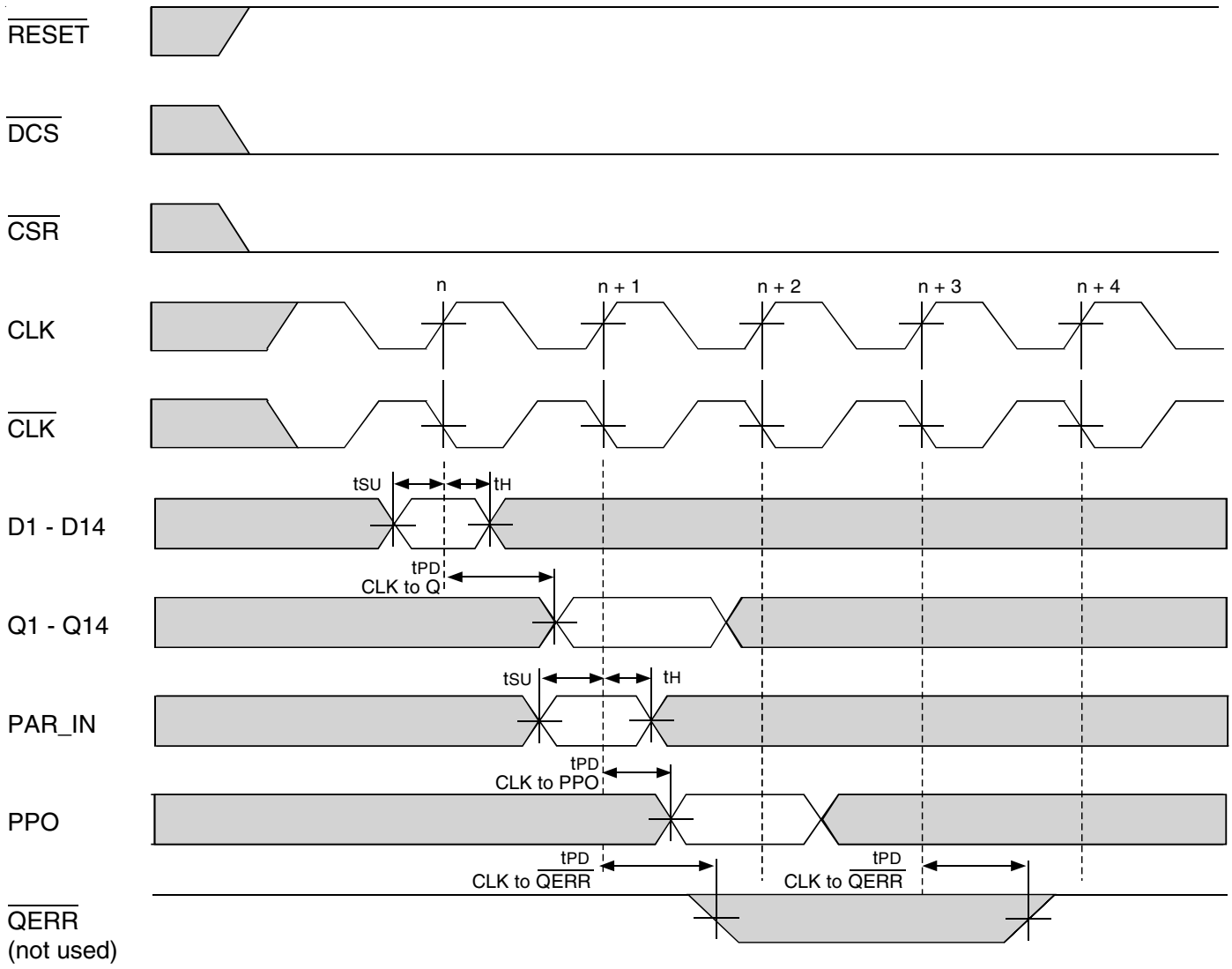
## REGISTER TIMING




*Timing Diagram for SSTU32866B Used as a Single Device; C0 = 0, C1 = 0*


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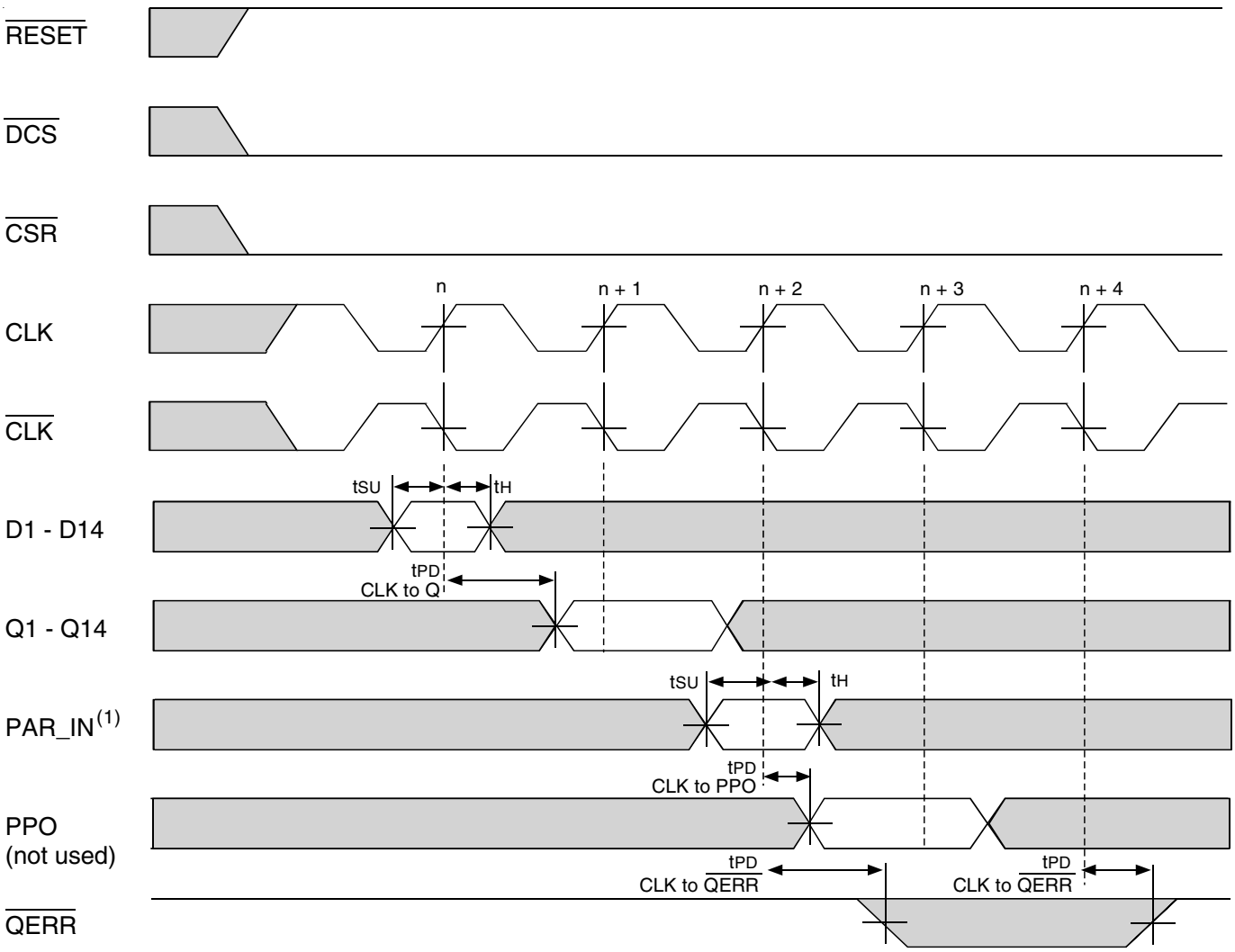
## REGISTER TIMING




*Timing Diagram for the First SSTU32866B (1:2 Register-A Configuration) Device Used in a Pair; C0 = 0, C1 = 1*


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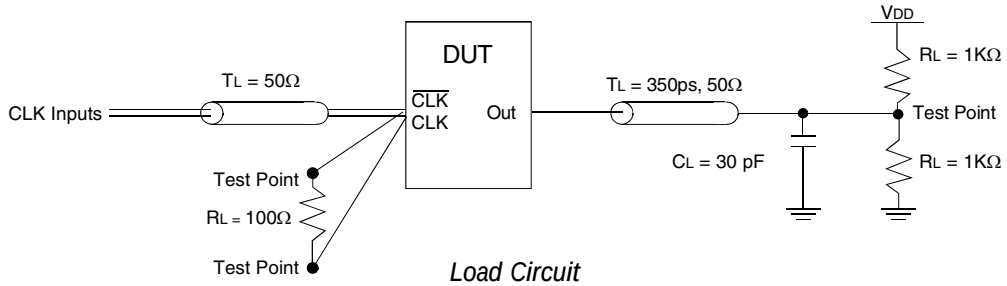
## REGISTER TIMING



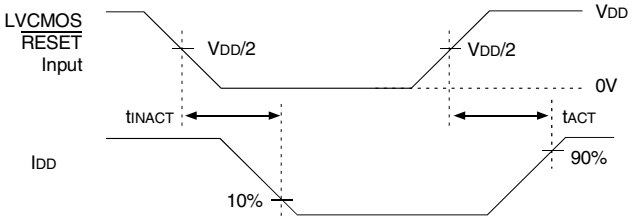

*Timing Diagram for the First SSTU32866B (1:2 Register-B Configuration) Device Used in a Pair; C0 = 1, C1 = 1*


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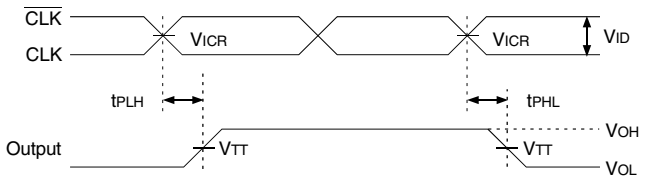
# TEST CIRCUITS AND WAVEFORMS ($V_{DD}$ = 1.8V ± 0.1V)



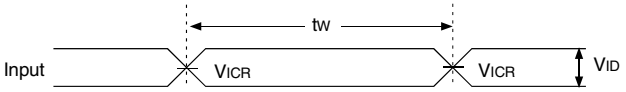

*Load Circuit*



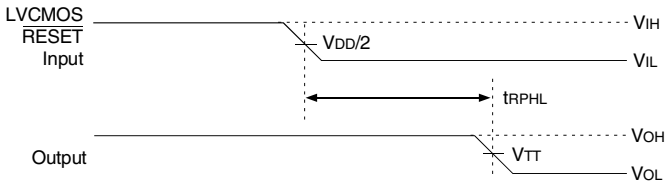

*Voltage and Current Waveforms*
*Inputs Active and Inactive Times*



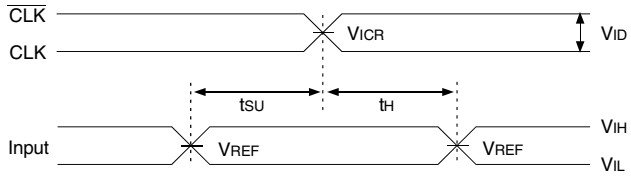

*Voltage Waveforms - Propagation Delay Times*




*Voltage Waveforms - Pulse Duration*




*Voltage Waveforms - Propagation Delay Times*

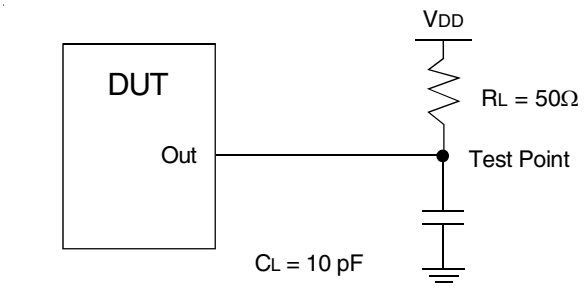



*Voltage Waveforms - Setup and Hold Times*

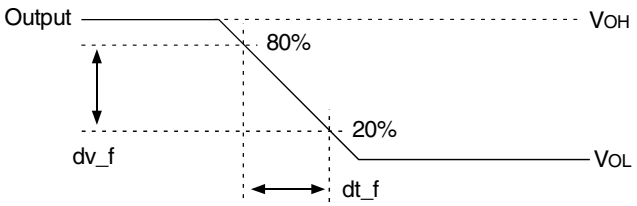
NOTES:
1. $C_L$ includes probe and jig capacitance.
2. $I_{DD}$ tested with clock and data inputs held at $V_{DD}$ or GND, and $I_O$ = 0mA
3. All input pulses are supplied by generators having the following characteristics: PRR ≤10MHz, $Z_O$ = 50Ω, input slew rate = 1 V/ns ±20% (unless otherwise specified).
4. The outputs are measured one at a time with one transition per measurement.
5. $V_{TT} = V_{REF} = V_{DD}/2$
6. $V_{IH} = V_{REF}$ + 250mV (AC voltage levels) for differential inputs. $V_{IH} = V_{DD}$ for LVCMOS input.
7. $V_{IL} = V_{REF}$ - 250mV (AC voltage levels) for differential inputs. $V_{IL}$ = GND for LVCMOS input.
8. $V_{ID}$ = 600mV.
9. $t_{PLH}$ and $t_{PHL}$ are the same as $t_{PDM}$.


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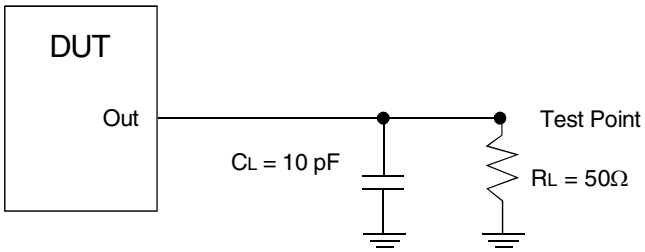
# TEST CIRCUITS AND WAVEFORMS ($V_{DD}$ = 1.8V ± 0.1V)



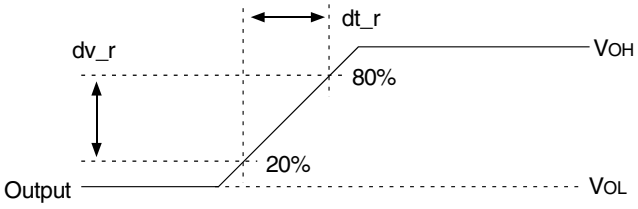

*Load Circuit - High-to-Low Slew-Rate Adjustment*



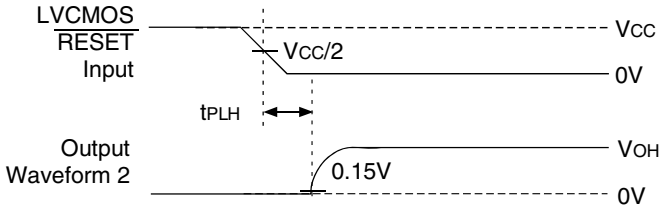

*Voltage Waveforms - High-to-Low Slew-Rate Adjustment*



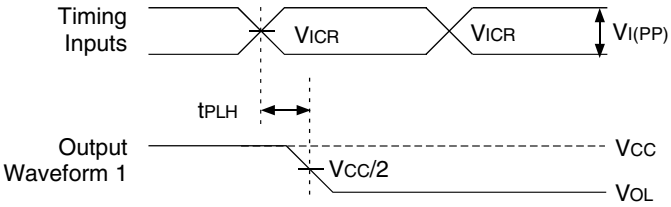

*Load Circuit - Low-to-High Slew-Rate Adjustment*



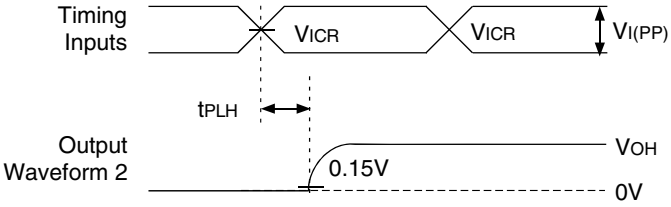

*Voltage Waveforms - Low-to-High Slew-Rate Adjustment*




*Voltage Waveforms - Open Drain Low-to-High Transition Time, Reset*




*Voltage Waveforms - Open Drain Hight-to-Low Transition Time, Clock*

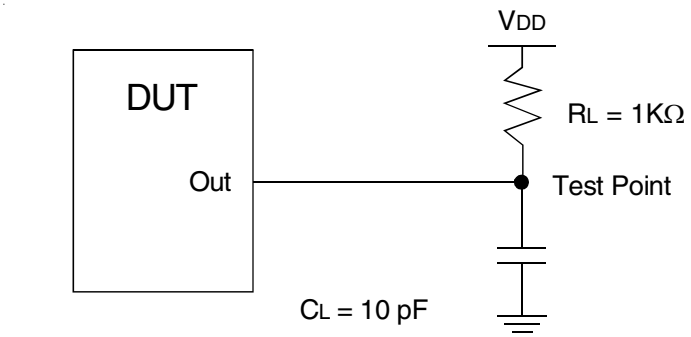



*Voltage Waveforms - Open Drain Low-to-High Transition Time, Clock*

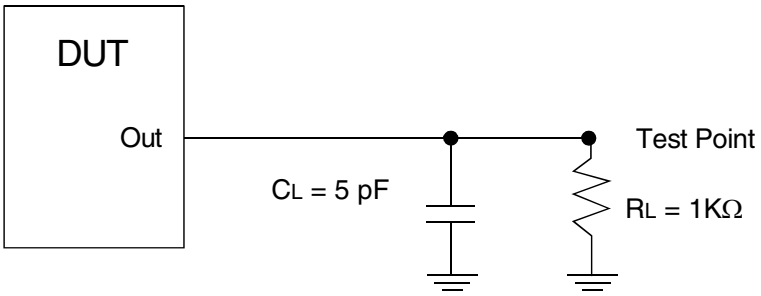
NOTES:
1. $C_L$ includes probe and jig capacitance.
2. All input pulses are supplied by generators having the following characteristics: PRR ≤10MHz, $Z_O$ = 50Ω, input slew rate = 1 V/ns ±20% (unless otherwise specified).


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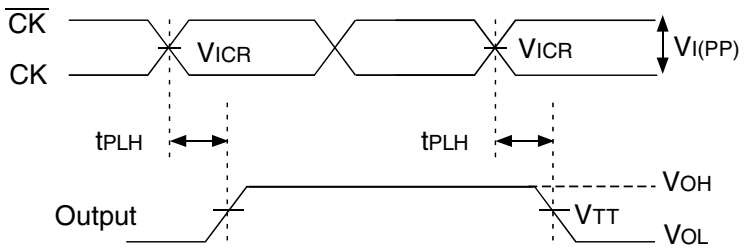
# TEST CIRCUITS AND WAVEFORMS ($V_{DD}$ = 1.8V ± 0.1V)



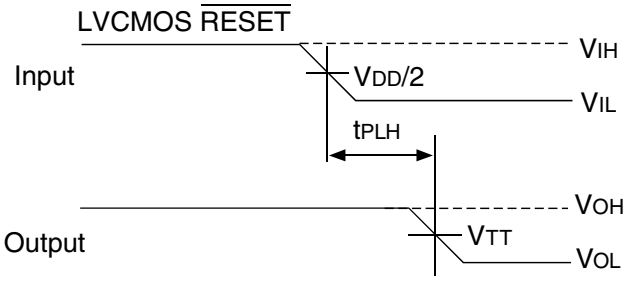

*Load Circuit - $\overline{QERR}$ Output*




*Load Circuit - Partial-Parity-Out Load Circuit*



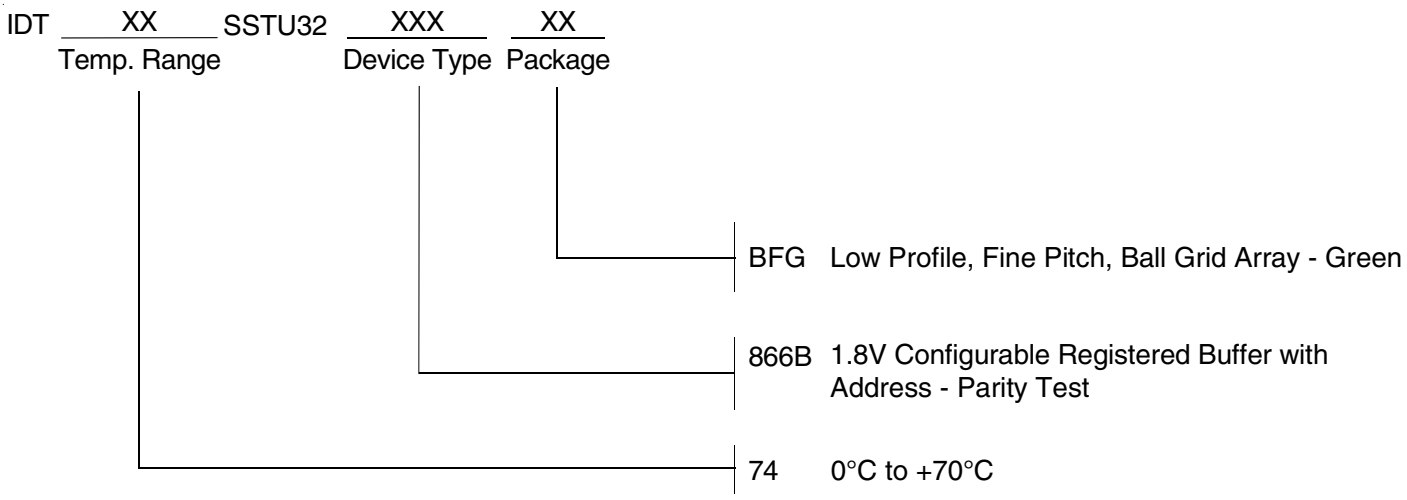

*Voltage Waveforms - Propagation Delay Times with Respect to Clock Inputs*




*Voltage Waveforms - Propagation Delay Times with Respect to Reset Inputs*


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