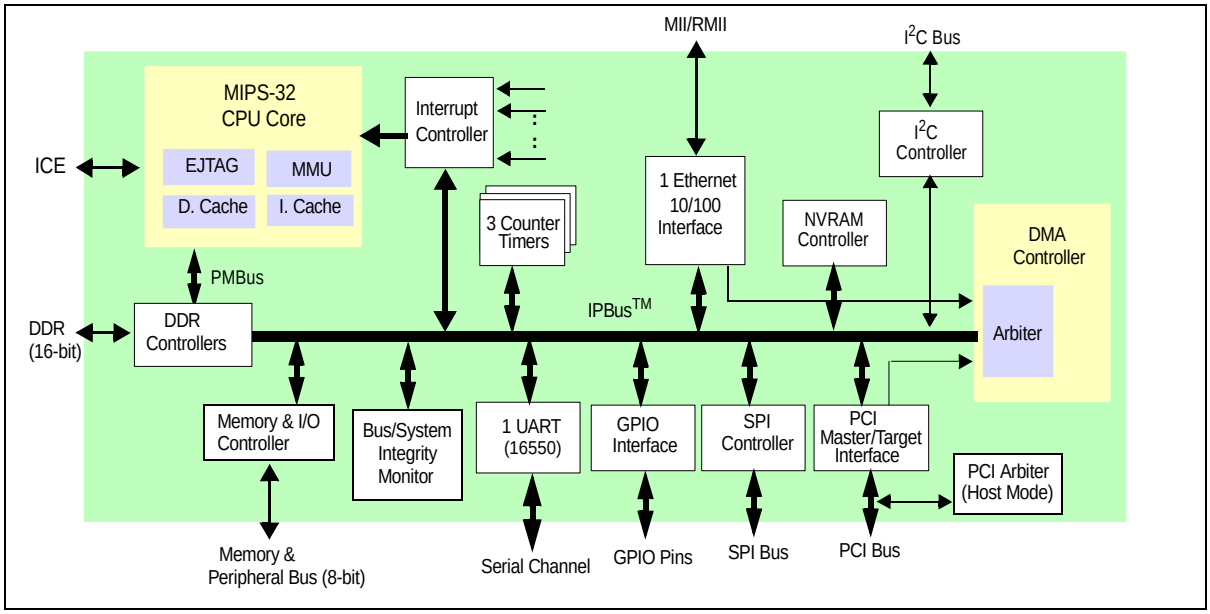
Device Overview

The 79RC32435 is a member of the IDT™ Interprise™ family of PCI integrated communications processors. It incorporates a high performance CPU core and a number of on-chip peripherals. The integrated processor is designed to transfer information from I/O modules to main memory with minimal CPU intervention, using a highly sophisticated direct memory access (DMA) engine. All data transfers through the RC32435 are achieved by writing data from an on-chip I/O peripheral to main memory and then out to another I/O module.

Features

- **32-bit CPU Core**
  - *MIPS32 instruction set*
  - *Cache Sizes: 8KB instruction and data caches, 4-Way set associative, cache line locking, non-blocking prefetches*
  - *16 dual-entry JTLB with variable page sizes*
  - *3-entry instruction TLB*
  - *3-entry data TLB*
  - *Max issue rate of one 32x16 multiply per clock*
  - *Max issue rate of one 32x32 multiply every other clock*
  - *CPU control with start, stop, and single stepping*
  - *Software breakpoints support*
  - *Hardware breakpoints on virtual addresses*
  - *ICE Interface that is compatible with v2.5 of the EJTAG Specification*
- **PCI Interface**
  - *32-bit PCI revision 2.2 compliant*
  - *Supports host or satellite operation in both master and target modes*
  - *Support for synchronous and asynchronous operation*
  - *PCI clock supports frequencies from 16 MHz to 66 MHz*
  - *PCI arbiter in Host mode: supports 6 external masters, fixed priority or round robin arbitration*
  - *I_2O "like" PCI Messaging Unit*
- **Ethernet Interface**
  - *10 and 100 Mb/s ISO/IEC 8802-3:1996 compliant*
  - *Supports MII or RMII PHY interface*
  - *Supports 64 entry hash table based multicast address filtering*
  - *512 byte transmit and receive FIFOs*
  - *Supports flow control functions outlined in IEEE Std. 802.3x-1997*
- **DDR Memory Controller**
  - *Supports up to 256MB of DDR SDRAM*
  - *1 chip select supporting 4 internal DDR banks*
  - *Supports a 16-bit wide data port using x8 or x16 bit wide DDR SDRAM devices*
  - *Supports 64 Mb, 128 Mb, 256 Mb, 512 Mb, and 1Gb DDR SDRAM devices*
  - *Data bus multiplexing support allows interfacing to standard DDR DIMMs and SODIMMs*
  - *Automatic refresh generation*

Block Diagram



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- **Non-Volatile RAM**
  - *Provides 512-bits of non-volatile storage*
  - *Eliminates need for external boot configuration vector*
  - *Stores initial PCI configuration register values when PCI configured to operate in satellite mode with suspended CPU execution*
  - *Authorization unit ensures only authorized software will operate on the system*
- **Memory and Peripheral Device Controller**
  - *Provides "glueless" interface to standard SRAM, Flash, ROM, dual-port memory, and peripheral devices*
  - *Demultiplexed address and data buses: 8-bit data bus, 26-bit address bus, 4 chip selects, control for external data bus buffers*

    Automatic byte gathering and scattering
  - *Flexible protocol configuration parameters: programmable number of wait states (0 to 63), programmable postread/post-write delay (0 to 31), supports external wait state generation, supports Intel and Motorola style peripherals*
  - *Write protect capability per chip select*
  - *Programmable bus transaction timer generates warm reset when counter expires*
  - *Supports up to 64 MB of memory per chip select*
- **DMA Controller**
  - *6 DMA channels: two channels for PCI (PCI to Memory and Memory to PCI), two channels for the Ethernet interface, and two channels for memory to memory DMA operations*
  - *Provides flexible descriptor based operation*
  - *Supports unaligned transfers (i.e., source or destination address may be on any byte boundary) with arbitrary byte length*
- **Universal Asynchronous Receiver Transmitter (UART)**
  - *Compatible with the 16550 and 16450 UARTs*
  - *16-byte transmit and receive buffers*
  - *Programmable baud rate generator derived from the system clock*
  - *Fully programmable serial characteristics:*
    - *5, 6, 7, or 8 bit characters*
    - *Even, odd or no parity bit generation and detection*
    - *1, 1-1/2 or 2 stop bit generation*
  - *Line break generation and detection*
  - *False start bit detection*
  - *Internal loopback mode*
- **I^2C-Bus**
  - *Supports standard 100 Kbps mode as well as 400 Kbps fast mode*
  - *Supports 7-bit and 10-bit addressing*
  - *Supports four modes: master transmitter, master receiver, slave transmitter, slave receiver*
- **Additional General Purpose Peripherals**
  - *Interrupt controller*
  - *System integrity functions*
  - *General purpose I/O controller*
  - *Serial peripheral interface (SPI)*
- **Counter/Timers**
  - *Three general purpose 32-bit counter timers*
  - *Timers may be cascaded*
  - *Selectable counter/timer clock source*
- **JTAG Interface**
  - *Compatible with IEEE Std. 1149.1 - 1990*

CPU Execution Core

The 32-bit CPU core is 100% compatible with the MIPS32 instruction set architecture (ISA). Specifically, this device features the 4Kc CPU core developed by MIPS Technologies Inc. (www.mips.com). This core issues a single instruction per cycle, includes a five stage pipeline and is optimized for applications that require integer arithmetic.

The CPU core includes 8 KB instruction and 8 KB data caches. Both caches are 4-way set associative and can be locked on a per line basis, which allows the programmer control over this precious on-chip memory resource. The core also features a memory management unit (MMU). The CPU core also incorporates an enhanced joint test access group (EJTAG) interface that is used to interface to in-circuit emulator tools, providing access to internal registers and enabling the part to be controlled externally, simplifying the system debug process.

The use of this core allows IDT's customers to leverage the broad range of software and development tools available for the MIPS architecture, including operating systems, compilers, and in-circuit emulators.

PCI Interface

The PCI interface on the RC32435 is compatible with version 2.2 of the PCI specification. An on-chip arbiter supports up to six external bus masters, supporting both fixed priority and rotating priority arbitration schemes. The part can support both satellite and host PCI configurations, enabling the RC32435 to act as a slave controller for a PCI add-in card application or as the primary PCI controller in the system. The PCI interface can be operated synchronously or asynchronously to the other I/O interfaces on the RC32435 device.

Ethernet Interface

The RC32435 has one Ethernet Channel supporting 10Mbps and 100Mbps speeds to provide a standard media independent interface (MII or RMII), allowing a wide range of external devices to be connected efficiently.

Double Data Rate Memory Controller

The RC32435 incorporates a high performance double data rate (DDR) memory controller which supports x16 memory configurations up to 256MB. This module provides all of the signals required to interface to discrete memory devices, including a chip select, differential clocking outputs and data strobes.

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Memory and I/O Controller

The RC32435 uses a dedicated local memory/IO controller including a de-multiplexed 8-bit data and 26-bit address bus. It includes all of the signals required to interface directly to a maximum of four Intel or Motorola-style external peripherals.

DMA Controller

The DMA controller consists of 6 independent DMA channels, all of which operate in exactly the same manner. The DMA controller off-loads the CPU core from moving data among the on-chip interfaces, external peripherals, and memory. The controller supports scatter/gather DMA with no alignment restrictions, making it appropriate for communications and graphics systems.

UART Interface

The RC32435 contains a serial channel (UART) that is compatible with the industry standard 16550 UART.

I^2C Interface

The standard I2C interface allows the RC32435 to connect to a number of standard external peripherals for a more complete system solution. The RC32435 supports both master and slave operations.

General Purpose I/O Controller

The RC32435 has 14 general purpose input/output pins. Each pin may be used as an active high or active low level interrupt or non-maskable interrupt input, and each signal may be used as a bit input or output port.

System Integrity Functions

The RC32435 contains a programmable watchdog timer that generates a non-maskable interrupt (NMI) when the counter expires and also contains an address space monitor that reports errors in response to accesses to undecoded address regions.

Thermal Considerations

The RC32435 is guaranteed in an ambient temperature range of 0° to +70° C for commercial temperature devices and - 40° to +85° for industrial temperature devices.

Revision History

January 19, 2006: Initial publication.

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Pin Description Table

The following table lists the functions of the pins provided on the RC32435. Some of the functions listed may be multiplexed onto the same pin.

The active polarity of a signal is defined using a suffix. Signals ending with an “N” are defined as being active, or asserted, when at a logic zero (low) level. All other signals (including clocks, buses, and select lines) will be interpreted as being active, or asserted, when at a logic one (high) level.

Signal	Type	Name/Description
Memory and Peripheral Bus		
BDIRN	O	**External Buffer Direction.** Controls the direction of the external data bus buffer for the memory and peripheral bus. If the RC32435 memory and peripheral bus is connected to the A side of a transceiver, such as an IDT74FCT245, then this pin may be directly connected to the direction control (e.g., BDIR) pin of the transceiver.
BOEN	O	**External Buffer Enable.** This signal provides an output enable control for an external buffer on the memory and peripheral data bus.
WEN	O	**Write Enables.** This signal is the memory and peripheral bus write enable signal.
CSN[3:0]	O	**Chip Selects.** These signals are used to select an external device on the memory and peripheral bus.
MADDR[21:0]	O	**Address Bus.** 22-bit memory and peripheral bus address bus. MADDR[25:22] are available as GPIO alternate functions.
MDATA[7:0]	I/O	**Data Bus.** 8-bit memory and peripheral data bus. During a cold reset, these pins function as inputs that are used to load the boot configuration vector.
OEN	O	**Output Enable.** This signal is asserted when data should be driven by an external device on the memory and peripheral bus.
RWN	O	**Read Write.** This signal indicates whether the transaction on the memory and peripheral bus is a read transaction or a write transaction. A high level indicates a read from an external device. A low level indicates a write to an external device.
WAITACKN	I	**Wait or Transfer Acknowledge.** When configured as wait, this signal is asserted during a memory and peripheral bus transaction to extend the bus cycle. When configured as a transfer acknowledge, this signal is asserted during a transaction to signal the completion of the transaction.
DDR Bus		
DDRADDR[13:0]	O	**DDR Address Bus.** 14-bit multiplexed DDR address bus. This bus is used to transfer the addresses to the DDR devices.
DDRBA[1:0]	O	**DDR Bank Address.** These signals are used to transfer the bank address to the DDRs.
DDRCASN	O	**DDR Column Address Strobe.** This signal is asserted during DDR transactions.
DDRCKE	O	**DDR Clock Enable.** The DDR clock enable signal is asserted during normal DDR operation. This signal is negated following a cold reset or during a power down operation.
DDRCKN	O	**DDR Negative DDR clock.** This signal is the negative clock of the differential DDR clock pair.

Table 1 Pin Description (Part 1 of 6)

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Signal	Type	Name/Description
DDRCKP	O	**DDR Positive DDR clock.** This signal is the positive clock of the differential DDR clock pair.
DDRCSN	O	**DDR Chip Selects.** This active low signal is used to select DDR device(s) on the DDR bus.
DDRDATA[15:0]	I/O	**DDR Data Bus.** 16-bit DDR data bus is used to transfer data between the RC32435 and the DDR devices. Data is transferred on both edges of the clock.
DDRDM[1:0]	O	**DDR Data Write Enables.** Byte data write enables are used to enable specific byte lanes during DDR writes. DDRDM[0] corresponds to DDRDATA[7:0] DDRDM[1] corresponds to DDRDATA[15:8]
DDRDQS[1:0]	I/O	**DDR Data Strobes.** DDR byte data strobes are used to clock data between DDR devices and the RC32435. These strobes are inputs during DDR reads and outputs during DDR writes. DDRDQS[0] corresponds to DDRDATA[7:0] DDRDQS[1] corresponds to DDRDATA[15:8]
DDRRASN	O	**DDR Row Address Strobe.** The DDR row address strobe is asserted during DDR transactions.
DDRVREF	I	**DDR Voltage Reference.** SSTL_2 DDR voltage reference is generated by an external source.
DDRWEN	O	**DDR Write Enable.** DDR write enable is asserted during DDR write transactions.
PCI Bus		
PCIAD[31:0]	I/O	**PCI Multiplexed Address/Data Bus**. Address is driven by a bus master during initial PCIFRAMEN assertion. Data is then driven by the bus master during writes or by the bus target during reads.
PCICBEN[3:0]	I/O	**PCI Multiplexed Command/Byte Enable Bus**. PCI commands are driven by the bus master during the initial PCIFRAMEN assertion. Byte enable signals are driven by the bus master during subsequent data phase(s).
PCICLK	I	**PCI Clock**. Clock used for all PCI bus transactions.
PCIDEVSELN	I/O	**PCI Device Select**. This signal is driven by a bus target to indicate that the target has decoded the address as one of its own address spaces.
PCIFRAMEN	I/O	**PCI Frame**. Driven by a bus master. Assertion indicates the beginning of a bus transaction. Negation indicates the last data.
PCIGNTN[3:0]	I/O	**PCI Bus Grant**. **In PCI host mode with internal arbiter:** The assertion of these signals indicates to the agent that the internal RC32435 arbiter has granted the agent access to the PCI bus. **In PCI host mode with external arbiter:** PCIGNTN[0]: asserted by an external arbiter to indicate to the RC32435 that access to the PCI bus has been granted. PCIGNTN[3:1]: unused and driven high. **In PCI satellite mode:** PCIGNTN[0]: This signal is asserted by an external arbiter to indicate to the RC32435 that access to the PCI bus has been granted. PCIGNTN[3:1]: unused and driven high.
PCIIRDYN	I/O	**PCI Initiator Ready**. Driven by the bus master to indicate that the current datum can complete.

Table 1 Pin Description (Part 2 of 6)

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Signal	Type	Name/Description
PCILOCKN	I/O	**PCI Lock**. This signal is asserted by an external bus master to indicate that an exclusive operation is occurring.
PCIPAR	I/O	**PCI Parity**. Even parity of the PCIAD[31:0] bus. Driven by the bus master during address and write Data phases. Driven by the bus target during the read data phase.
PCIPERRN	I/O	**PCI Parity Error**. If a parity error is detected, this signal is asserted by the receiving bus agent 2 clocks after the data is received.
PCIREQN[3:0]	I/O	**PCI Bus Request.** **In PCI host mode with internal arbiter:** These signals are inputs whose assertion indicates to the internal RC32435 arbiter that an agent desires ownership of the PCI bus. **In PCI host mode with external arbiter:** PCIREQN[0]: asserted by the RC32435 to request ownership of the PCI bus. PCIREQN[3:1]: unused and driven high. **In PCI satellite mode:** PCIREQN[0]: this signal is asserted by the RC32435 to request use of the PCI bus. PCIREQN[1]: function changes to PCIIDSEL and is used as a chip select during configuration read and write transactions. PCIREQN[3:2]: unused and driven high.
PCIRSTN	I/O	**PCI Reset**. In host mode, this signal is asserted by the RC32435 to generate a PCI reset. In satellite mode, assertion of this signal initiates a warm reset.
PCISERRN	I/O	**PCI System Error**. This signal is driven by an agent to indicate an address parity error, data parity error during a special cycle command, or any other system error. Requires an external pull-up.
PCISTOPN	I/O	**PCI Stop**. Driven by the bus target to terminate the current bus transaction. For example, to indicate a retry.
PCITRDYN	I/O	**PCI Target Ready**. Driven by the bus target to indicate that the current data can complete.
General Purpose Input/Output		
GPIO[0]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: U0SOUT Alternate function: UART channel 0 serial output.
GPIO[1]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: U0SINP Alternate function: UART channel 0 serial input.
GPIO[2]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: U0RTSN Alternate function: UART channel 0 request to send.
GPIO[3]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: U0CTSN Alternate function: UART channel 0 clear to send.

Table 1 Pin Description (Part 3 of 6)

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Signal	Type	Name/Description
GPIO[4]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: MADDR[22] Alternate function: Memory and peripheral bus address.
GPIO[5]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: MADDR[23] Alternate function: Memory and peripheral bus address.
GPIO[6]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: MADDR[24] Alternate function: Memory and peripheral bus address. The value of this pin may be used as a counter timer clock input (see Counter Timer Clock Select Register in Chapter 14, Counter/Timers, of the RC32435 User Manual).
GPIO[7]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: MADDR[25] Alternate function: Memory and peripheral bus address. The value of this pin may be used as a counter timer clock input (see Counter Timer Clock Select Register in Chapter 14, Counter/Timers, of the RC32435 User Manual).
GPIO[8]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: CPU Alternate function: CPU or DMA debug output pin.
GPIO[9]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: PCIREQN[4] Alternate function: PCI Request 4.
GPIO[10]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: PCIGNTN[4] Alternate function: PCI Grant 4.
GPIO[11]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: PCIREQN[5] Alternate function: PCI Request 5.
GPIO[12]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: PCIGNTN[5] Alternate function: PCI Grant 5.
GPIO[13]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: PCIMUINTN Alternate function: PCI Messaging unit interrupt output.
SPI Interface		
SCK	I/O	**Serial Clock**. This signal is used as the serial clock output. This pin may be used as a bit input/output port.

Table 1 Pin Description (Part 4 of 6)

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Signal	Type	Name/Description
SDI	I/O	**Serial Data Input**. This signal is used to shift in serial data. This pin may be used as a bit input/output port.
SDO	I/O	**Serial Data Output**. This signal is used shift out serial data.
I^2C Bus Interface		
SCL	I/O	**I^2C Clock.** I^2C-bus clock.
SDA	I/O	**I^2C Data Bus.** I^2C-bus data bus.
Ethernet Interfaces		
MIICL	I	**Ethernet MII Collision Detected.** This signal is asserted by the ethernet PHY when a collision is detected.
MIICRS	I	**Ethernet MII Carrier Sense.** This signal is asserted by the ethernet PHY when either the transmit or receive medium is not idle.
MIIRXCLK	I	**Ethernet MII Receive Clock.** This clock is a continuous clock that provides a timing reference for the reception of data. This pin also functions as the RMII REF_CLK input.
MIIRXD[3:0]	I	**Ethernet MII Receive Data.** This nibble wide data bus contains the data received by the ethernet PHY. This pin also functions as the RMII RXD[1:0] input.
MIIRXDV	I	**Ethernet MII Receive Data Valid.** The assertion of this signal indicates that valid receive data is in the MII receive data bus. This pin also functions as the RMII CRS_DV input.
MIIRXER	I	**Ethernet MII Receive Error.** The assertion of this signal indicates that an error was detected somewhere in the ethernet frame currently being sent in the MII receive data bus. This pin also functions as the RMII RX_ER input.
MIITXCLK	I	**Ethernet MII Transmit Clock.** This clock is a continuous clock that provides a timing reference for the transfer of transmit data.
MIITXD[3:0]	O	**Ethernet MII Transmit Data.** This nibble wide data bus contains the data to be transmitted. This pin also functions as the RMII TXD[1:0] output.
MIITXENP	O	**Ethernet MII Transmit Enable.** The assertion of this signal indicates that data is present on the MII for transmission. This pin also functions as the RMII TX_EN output.
MIITXER	O	**Ethernet MII Transmit Coding Error.** When this signal is asserted together with MIITXENP, the ethernet PHY will transmit symbols which are not valid data or delimiters.
MIIMDC	O	**MII Management Data Clock.** This signal is used as a timing reference for transmission of data on the management interface.
MIIMDIO	I/O	**MII Management Data.** This bidirectional signal is used to transfer data between the station management entity and the ethernet PHY.
EJTAG / JTAG		
JTAG_TMS	I	**JTAG Mode**. The value on this signal controls the test mode select of the boundary scan logic or JTAG Controller. When using the EJTAG debug interface, this pin should be left disconnected (since there is an internal pull-up) or driven high.

Table 1 Pin Description (Part 5 of 6)

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Signal	Type	Name/Description
EJTAG_TMS	I	**EJTAG Mode**. The value on this signal controls the test mode select of the EJTAG Controller. When using the JTAG boundary scan, this pin should be left disconnected (since there is an internal pull-up) or driven high.
JTAG_TRST_N	I	**JTAG Reset**. This active low signal asynchronously resets the boundary scan logic, JTAG TAP Controller, and the EJTAG Debug TAP Controller. An external pull-up on the board is recommended to meet the JTAG specification in cases where the tester can access this signal. However, for systems running in functional mode, one of the following should occur: 1) actively drive this signal low with control logic 2) statically drive this signal low with an external pull-down on the board 3) clock JTAG_TCK while holding EJTAG_TMS and/or JTAG_TMS high.
JTAG_TCK	I	**JTAG Clock**. This is an input test clock used to clock the shifting of data into or out of the boundary scan logic, JTAG Controller, or the EJTAG Controller. JTAG_TCK is independent of the system and the processor clock with a nominal 50% duty cycle.
JTAG_TDO	O	**JTAG Data Output**. This is the serial data shifted out from the boundary scan logic, JTAG Controller, or the EJTAG Controller. When no data is being shifted out, this signal is tri-stated.
JTAG_TDI	I	**JTAG Data Input**. This is the serial data input to the boundary scan logic, JTAG Controller, or the EJTAG Controller.
System		
CLK	I	**Master Clock.** This is the master clock input. The processor frequency is a multiple of this clock frequency. This clock is used as the system clock for all memory and peripheral bus operations.
EXTBCV	I	**Load External Boot Configuration Vector.** When this pin is asserted (i.e., high) the boot configuration vector is loaded from an externally supplied value during a cold reset. When this pin is negated, the boot configuration vector is taken from the NVRAM located on-chip.
EXTCLK	O	**External Clock.** This clock is used for all memory and peripheral bus operations.
COLDRSTN	I	**Cold Reset.** The assertion of this signal initiates a cold reset. This causes the processor state to be initialized, boot configuration to be loaded, and the internal PLL to lock onto the master clock (CLK).
RSTN	I/O	**Reset.** The assertion of this bidirectional signal initiates a warm reset. This signal is asserted by the RC32435 during a warm reset.

Table 1 Pin Description (Part 6 of 6)

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Pin Characteristics

Note: Some input pads of the RC32435 do not contain internal pull-ups or pull-downs. Unused inputs should be tied off to appropriate levels. This is especially critical for unused control signal inputs (such as WAITACKN) which, if left floating, could adversely affect the RC32435's operation. Also, any input pin left floating can cause a slight increase in power consumption.

Function	Pin Name	Type	Buffer	I/O Type	Internal Resistor	Notes[1]
Memory and Peripheral Bus	BDIRN	O	LVTTL	High Drive		
	BOEN	O	LVTTL	High Drive		
	WEN	O	LVTTL	High Drive		
	CSN[3:0]	O	LVTTL	High Drive		
	MADDR[21:0]	I/O	LVTTL	High Drive		
	MDATA[7:0]	I/O	LVTTL	High Drive		
	OEN	O	LVTTL	High Drive		
	RWN	O	LVTTL	High Drive		
	WAITACKN	I	LVTTL	STI	pull-up	
DDR Bus	DDRADDR[13:0]	O	SSTL_2			
	DDRBA[1:0]	O	SSTL_2			
	DDRCASN	O	SSTL_2			
	DDRCKE	O	SSTL_2 / LVC-MOS			
	DDRCKN	O	SSTL_2			
	DDRCKP	O	SSTL_2			
	DDRCSN	O	SSTL_2			
	DDRDATA[15:0]	I/O	SSTL_2			
	DDRDM[1:0]	O	SSTL_2			
	DDRDQS[1:0]	I/O	SSTL_2			
	DDRRASN	O	SSTL_2			
	DDRVREF	I	Analog			
	DDRWEN	O	SSTL_2			
PCI Bus Interface	PCIAD[31:0]	I/O	PCI			
	PCICBEN[3:0]	I/O	PCI			
	PCICLK	I	PCI			
	PCIDEVSELN	I/O	PCI			pull-up on board
	PCIFRAMEN	I/O	PCI			pull-up on board
	PCIGNTN[3:0]	I/O	PCI			pull-up on board
	PCIIRDYN	I/O	PCI			pull-up on board
	PCILOCKN	I/O	PCI			
	PCIPAR	I/O	PCI			
	PCIPERRN	I/O	PCI			
	PCIREQN[3:0]	I/O	PCI			pull-up on board
	PCIRSTN	I/O	PCI			pull-down on board
	PCISERRN	I/O	PCI	Open Collector		pull-up on board
	PCISTOPN	I/O	PCI			pull-up on board
	PCITRDYN	I/O	PCI			pull-up on board
General Purpose I/O	GPIO[8:0]	I/O	LVTTL	High Drive	pull-up	
	GPIO[13:9]	I/O	PCI			pull-up on board

Table 2 Pin Characteristics (Part 1 of 2)

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Function	Pin Name	Type	Buffer	I/O Type	Internal Resistor	Notes[1]
Serial Peripheral Interface	SCK	I/O	LVTTL	High Drive	pull-up	pull-up on board
	SDI	I/O	LVTTL	High Drive	pull-up	pull-up on board
	SDO	I/O	LVTTL	High Drive	pull-up	pull-up on board
I^2C-Bus Interface	SCL	I/O	LVTTL	Low Drive/STI		pull-up on board[2]
	SDA	I/O	LVTTL	Low Drive/STI		pull-up on board[2]
Ethernet Interfaces	MIICL	I	LVTTL	STI	pull-down	
	MIICRS	I	LVTTL	STI	pull-down	
	MIIRXCLK	I	LVTTL	STI	pull-up	
	MIIRXD[3:0]	I	LVTTL	STI	pull-up	
	MIIRXDV	I	LVTTL	STI	pull-down	
	MIIRXER	I	LVTTL	STI	pull-down	
	MIITXCLK	I	LVTTL	STI	pull-up	
	MIITXD[3:0]	O	LVTTL	Low Drive		
	MIITXENP	O	LVTTL	Low Drive		
	MIITXER	O	LVTTL	Low Drive		
	MIIMDC	O	LVTTL	Low Drive		
	MIIMDIO	I/O	LVTTL	Low Drive	pull-up	
EJTAG / JTAG	JTAG_TMS	I	LVTTL	STI	pull-up	
	EJTAG_TMS	I	LVTTL	STI	pull-up	
	JTAG_TRST_N	I	LVTTL	STI	pull-up	
	JTAG_TCK	I	LVTTL	STI	pull-up	
	JTAG_TDO	O	LVTTL	Low Drive		
	JTAG_TDI	I	LVTTL	STI	pull-up	
System	CLK	I	LVTTL	STI		
	EXTBCV	I	LVTTL	STI	pull-down	
	EXTCLK	O	LVTTL	High Drive		
	COLDRSTN	I	LVTTL	STI		
	RSTN	I/O	LVTTL	Low Drive / STI	pull-up	pull-up on board

Table 2 Pin Characteristics (Part 2 of 2)

1. External pull-up required in most system applications. Some applications may require additional pull-ups not identified in this table.

2. Use a 2.2K pull-up resistor for I2C pins.

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Boot Configuration Vector

The encoding of the boot configuration vector is described in Table 3, and the vector input is illustrated in Figure 4. The value of the boot configuration vector read in by the RC32435 during a cold reset may be determined by reading the Boot Configuration Vector (BCV) Register.

Signal	Name/Description
MADDR[3:0]	**CPU Pipeline Clock Multiplier**. This field specifies the value by which the PLL multiplies the master clock input (CLK) to obtain the processor clock frequency (PCLK). For master clock input frequency constraints, refer to Table 3.2 in the RC32435 User Manual. 0x0 - PLL Bypass 0x1 - Multiply by 3 0x2 - Multiply by 4 0x3 - Multiply by 5 - Reserved 0x4 - Multiply by 5 0x5 - Multiply by 6 - Reserved 0x6 - Multiply by 6 0x7 - Multiply by 8 0x8 - Multiply by 10 0x9 through 0xF - Reserved
MADDR[5:4]	**External Clock Divider**. This field specifies the value by which the IPBus clock (ICLK), which is always 1/2 PCLK, is divided in order to generate the external clock output on the EXTCLK pin. 0x0 - Divide by 1 0x1 - Divide by 2 0x2 - Divide by 4 0x3 - reserved
MADDR[6]	**Endian.** This bit specifies the endianness. 0x0 - little endian 0x1 - big endian
MADDR[7]	**Reset Mode**. This bit specifies the length of time the RSTN signal is driven. 0x0 - Normal reset: RSTN driven for minimum of 4000 clock cycles. If the internal boot configuration vector is selected, the expiration of an 18-bit counter operating at the master clock input (CLK) frequency is used as the PLL stabilization delay. 0x1 - Reserved
MADDR[10:8]	**PCI Mode**. This bit controls the operating mode of the PCI bus interface. The initial value of the EN bit in the PCIC register is determined by the PCI mode. 0x0 - Disabled (EN initial value is zero) 0x1 - PCI satellite mode with PCI target not ready (EN initial value is one) 0x2 - PCI satellite mode with suspended CPU execution (EN initial value is one) 0x3 - PCI host mode with external arbiter (EN initial value is zero) 0x4 - PCI host mode with internal arbiter using fixed priority arbitration algorithm (EN initial value is zero) 0x5 - PCI host mode with internal arbiter using round robin arbitration algorithm (EN initial value is zero) 0x6 - *reserved* 0x7 - *reserved*

Table 3 Boot Configuration Encoding (Part 1 of 2)

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Signal	Name/Description
MADDR[11]	**Disable Watchdog Timer**. When this bit is set, the watchdog timer is disabled following a cold reset. 0x0 - Watchdog timer enabled 0x1 - Watchdog timer disabled
MADDR[13:12]	**Reserved**. These pins must be driven low during boot configuration.
MADDR[15:14]	**Reserved**. Must be set to zero.

Table 3 Boot Configuration Encoding (Part 2 of 2)

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Logic Diagram — RC32435

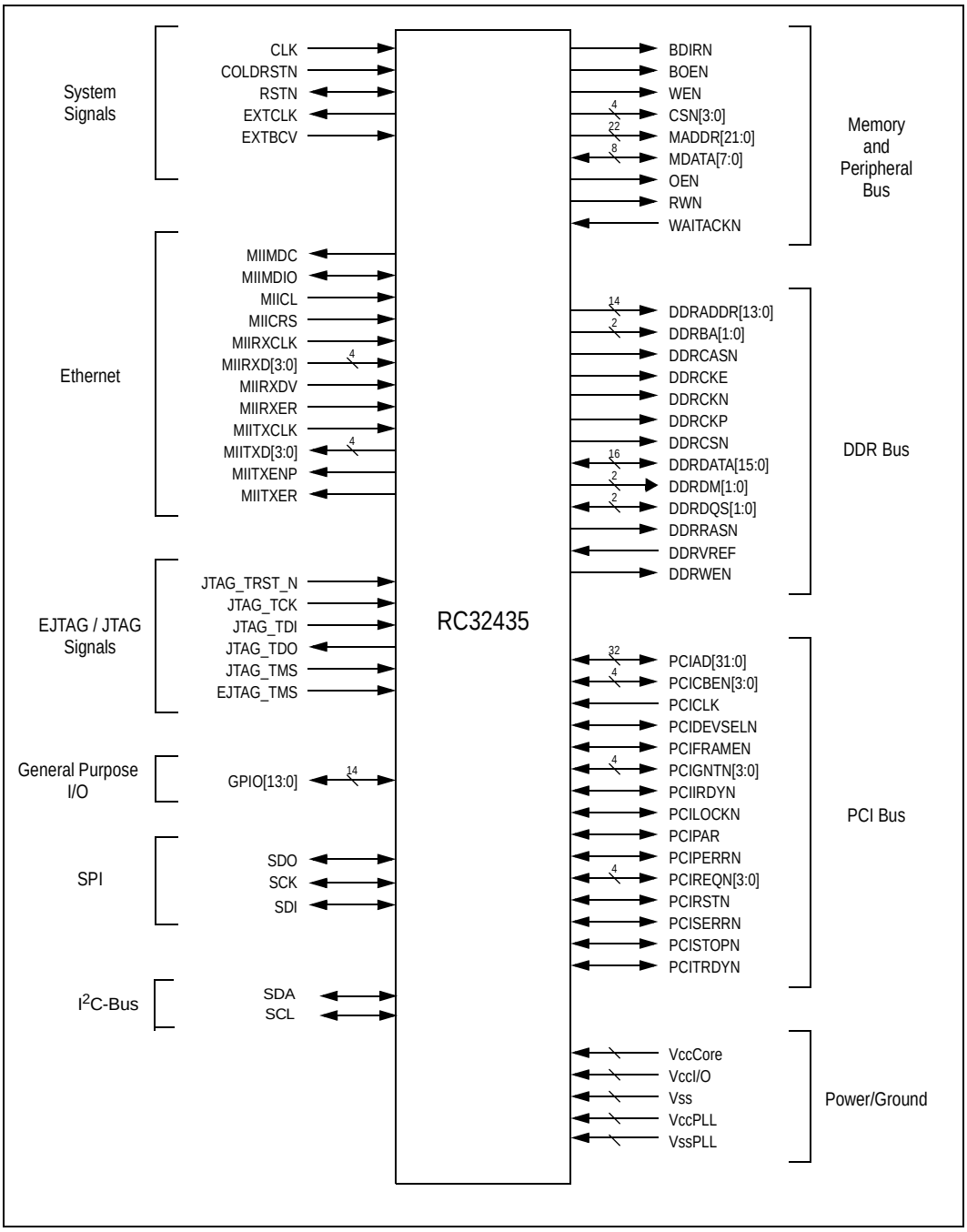


Figure 1 Logic Diagram

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AC Timing Definitions

Below are examples of the AC timing characteristics used throughout this document.

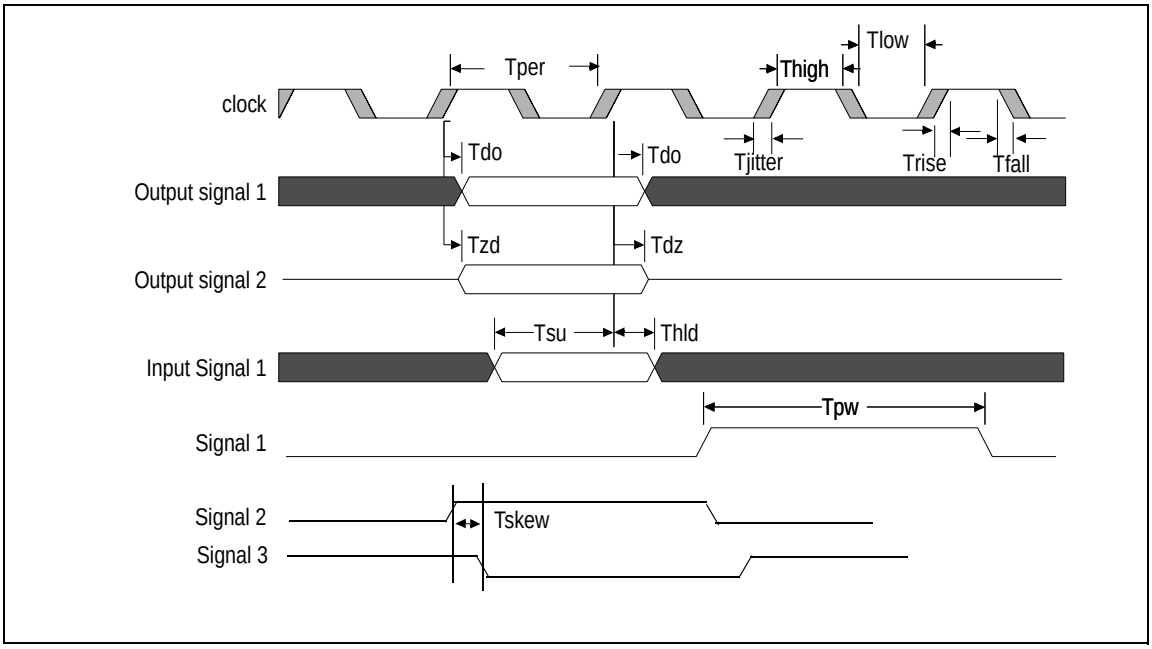


Figure 2 AC Timing Definitions Waveform

Symbol	Definition
Tper	Clock period.
Tlow	Clock low. Amount of time the clock is low in one clock period.
Thigh	Clock high. Amount of time the clock is high in one clock period.
Trise	Rise time. Low to high transition time.
Tfall	Fall time. High to low transition time.
Tjitter	Jitter. Amount of time the reference clock (or signal) edge can vary on either the rising or falling edges.
Tdo	Data out. Amount of time after the reference clock edge that the output will become valid. The minimum time represents the data output hold. The maximum time represents the earliest time the designer can use the data.
Tzd	Z state to data valid. Amount of time after the reference clock edge that the tri-stated output takes to become valid.
Tdz	Data valid to Z state. Amount of time after the reference clock edge that the valid output takes to become tri-stated.
Tsu	Input set-up. Amount of time before the reference clock edge that the input must be valid.
Thld	Input hold. Amount of time after the reference clock edge that the input must remain valid.
Tpw	Pulse width. Amount of time the input or output is active for asynchronous signals.
Tslew	Slew rate. The rise or fall rate for a signal to go from a high to low, or low to high.
X(clock)	Timing value. This notation represents a value of 'X' multiplied by the clock time period of the specified clock. Using 5(CLK) as an example: X = 5 and the oscillator clock (CLK) = 25MHz, then the timing value is 200.
Tskew	Skew. The amount of time two signal edges deviate from one another.

Table 4 AC Timing Definitions

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System Clock Parameters

(Values based on systems running at recommended supply voltages and operating temperatures, as shown in Tables 15 and 16.)

Parameter	Symbol	Reference Edge	266MHz		300MHz		350MHz		400MHz		Units	Timing Diagram Reference
			Min	Max	Min	Max	Min	Max	Min	Max		
PCLK[1]	Frequency	none	200	266	200	300	200	350	200	400	MHz	See Figure 3.
	Tper		3.8	5.0	3.3	5.0	2.85	5.0	2.5	5.0	ns	
ICLK[2,3,4]	Frequency	none	100	133	100	150	100	175	100	200	MHz	
	Tper		7.5	10.0	6.7	10.0	5.7	10.0	5.0	10.0	ns	
CLK[5]	Frequency	none	25	125	25	125	25	125	25	125	MHz	
	Tper_5a		8.0	40.0	8.0	40.0	8.0	40.0	8.0	40.0	ns	
	Thigh_5a, Tlow_5a		40	60	40	60	40	60	40	60	% of Tper_5a	
	Trise_5a, Tfall_5a		—	3.0	—	3.0	—	3.0	—	3.0	ns	
	Tjitter_5a		—	0.1	—	0.1	—	0.1	—	0.1	ns	

Table 5 Clock Parameters

1. The CPU pipeline clock (PCLK) speed is selected during cold reset by the boot configuration vector (see Table 3). Refer to Chapter 3, Clocking and Initialization, in the RC32435 User Reference Manual for the allowable frequency ranges of CLK and PCLK.
2. ICLK is the internal IPBus clock. It is always equal to PCLK divided by 2. This clock cannot be sampled externally.
3. The ethernet clock (MIIxRXCLK and MIIxTXCLK) frequency must be equal to or less than 1/2 ICLK (MIIxRXCLK and MIIxTXCLK <= 1/2(ICLK)).
4. PCICLK must be equal to or less than two times ICLK (PCICLK <= 2(ICLK)) with a maximum PCICLK of 66 MHz.
5. The input clock (CLK) is input from the external oscillator to the internal PLL.

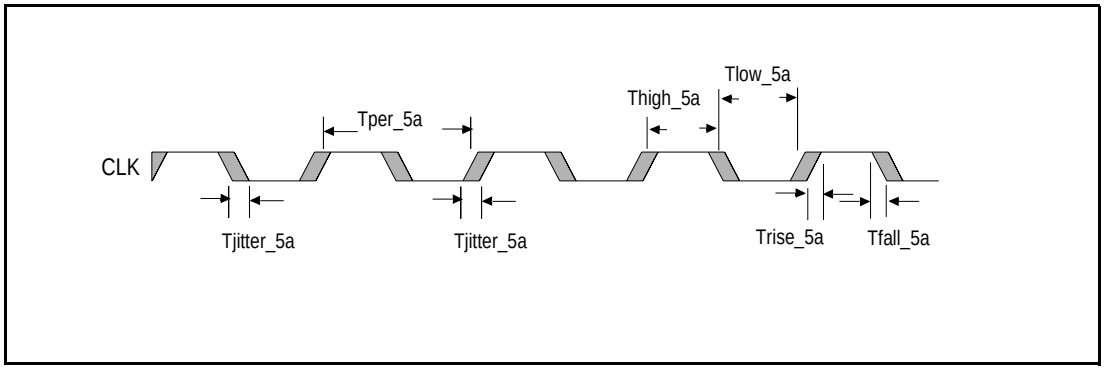


Figure 3 Clock Parameters Waveform

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AC Timing Characteristics

(Values given below are based on systems running at recommended operating temperatures and supply voltages, shown in Tables 15 and 16.)

Signal	Symbol	Reference Edge	266MHz		300MHz		350MHz		400MHz		Unit	Conditions	Timing Diagram Reference
			Min	Max	Min	Max	Min	Max	Min	Max			
Reset													
COLDRSTN[1]	Tpw_6a[2]	none	OSC	—	OSC	—	OSC	—	OSC	—	ms	Cold reset	See Figures 4 and 5.
	Trise_6a	none	—	5.0	—	5.0	—	5.0	—	5.0	ns	Cold reset	
RSTN[3] (input)	Tpw_6b[2]	none	2(CLK)	—	2(CLK)	—	2(CLK)	—	2(CLK)	—	ns	Warm reset	
RSTN[3] (output)	Tdo_6c	COLDRSTN falling	—	15.0	—	15.0	—	15.0	—	15.0	ns	Cold reset	
MADDR[15:0] (boot vector)	Tdz_6d[2]	COLDRSTN falling	—	30.0	—	30.0	—	30.0	—	30.0	ns	Cold reset	
	Tdz_6d[2]	RSTN falling	—	5(CLK)	—	5(CLK)	—	5(CLK)	—	5(CLK)	ns	Warm reset	
	Tzd_6d[2]	RSTN rising	2(CLK)	—	2(CLK)	—	2(CLK)	—	2(CLK)	—	ns	Warm reset	

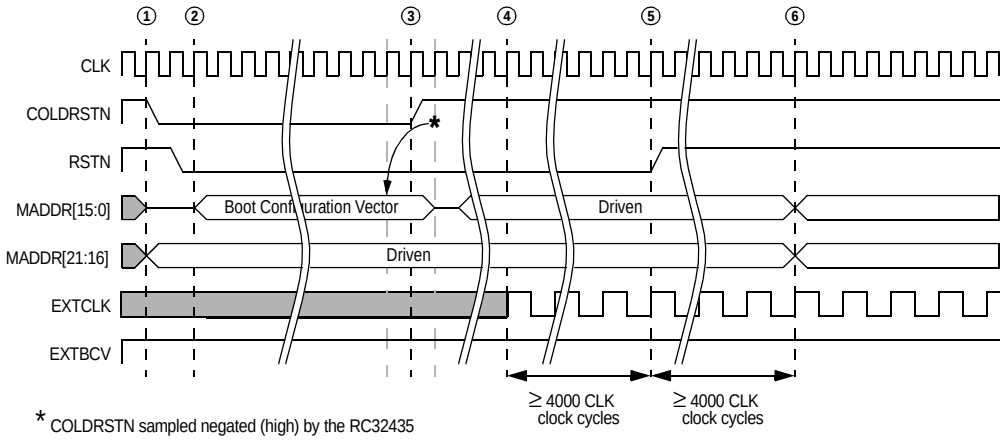
Table 6 Reset and System AC Timing Characteristics

1. The COLDRSTN minimum pulse width is the oscillator stabilization time (OSC) with V_{cc} stable.

2. The values for this symbol were determined by calculation, not by testing.

3. RSTN is a bidirectional signal. It is treated as an asynchronous input.

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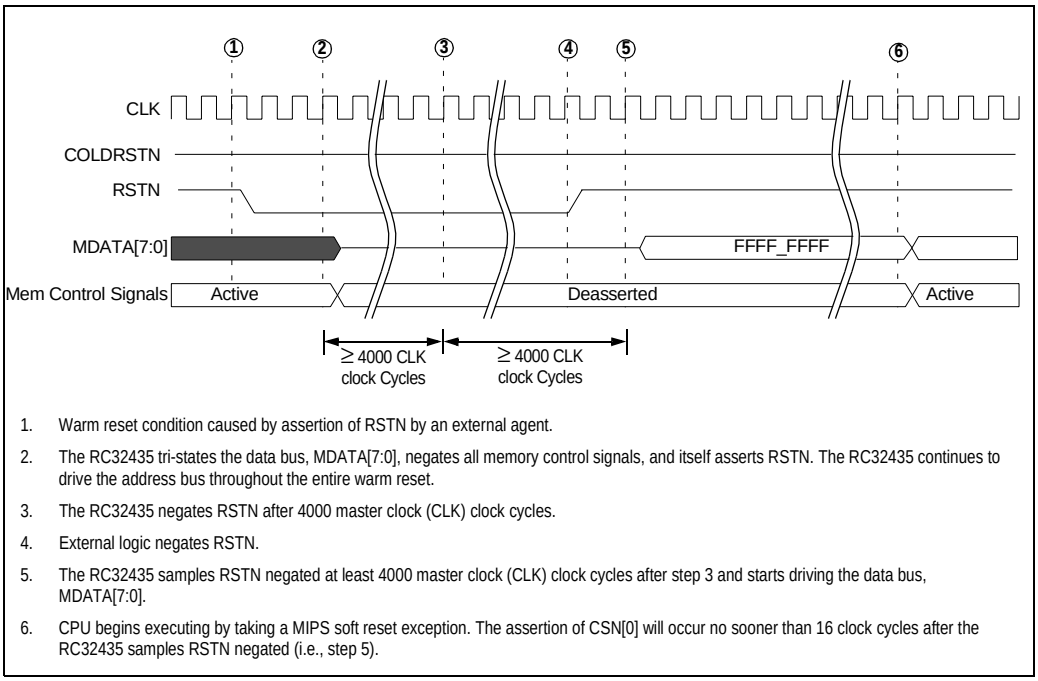


1. EXTBCV is asserted (i.e., pulled-up). COLDRSTN is asserted by external logic. The RC32435 responds by immediately tri-stating the bottom 16-bits of the memory and peripheral address bus (MADDR[15:0]), driving the remaining address bus signals (i.e., MADDR[21:16]), and asserting RSTN. EXTCLK is undefined at this point.
2. External logic drives the boot configuration vector on MADDR[15:0].
3. External logic negates COLDRSTN and tri-states the boot configuration vector on MADDR[15:0]. In response, the RC32435 stops sampling the boot configuration vector and retains the boot configuration vector value seen two clock cycles earlier (i.e., the value on the MADDR[15:0] lines two rising edges of CLK earlier). Within 16 CLK clock cycles after COLDRSTN is sampled negated, the RC32435 begins driving MADDR[15:0].
4. The RC32435 waits for the NVRAM to initialize (if the Disable NVRAM Initialization mode is not selected in the boot configuration vector) and for the PLL to stabilize.
5. The RC32435 then begins generating EXTCLK.
6. After at least 4000 CLK clock cycles, the RC32435 tri-states RSTN.
7. At least 4000 CLK clock cycles after negating RSTN, the RC32435 samples RSTN. If RSTN is negated, cold reset has completed and the RC32435 CPU begins executing by taking MIPS reset exception.

Figure 4 COLD Reset Operation with External Boot Configuration Vector AC Timing Waveform

Note: For a diagram showing the COLD Reset Operation with Internal Boot Configuration Vector, see Figure 3.6 in the RC32435 User Reference Manual.

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1. Warm reset condition caused by assertion of RSTN by an external agent.
2. The RC32435 tri-states the data bus, MDATA[7:0], negates all memory control signals, and itself asserts RSTN. The RC32435 continues to drive the address bus throughout the entire warm reset.
3. The RC32435 negates RSTN after 4000 master clock (CLK) clock cycles.
4. External logic negates RSTN.
5. The RC32435 samples RSTN negated at least 4000 master clock (CLK) clock cycles after step 3 and starts driving the data bus, MDATA[7:0].
6. CPU begins executing by taking a MIPS soft reset exception. The assertion of CSN[0] will occur no sooner than 16 clock cycles after the RC32435 samples RSTN negated (i.e., step 5).

Figure 5 Externally Initiated Warm Reset AC Timing Waveform

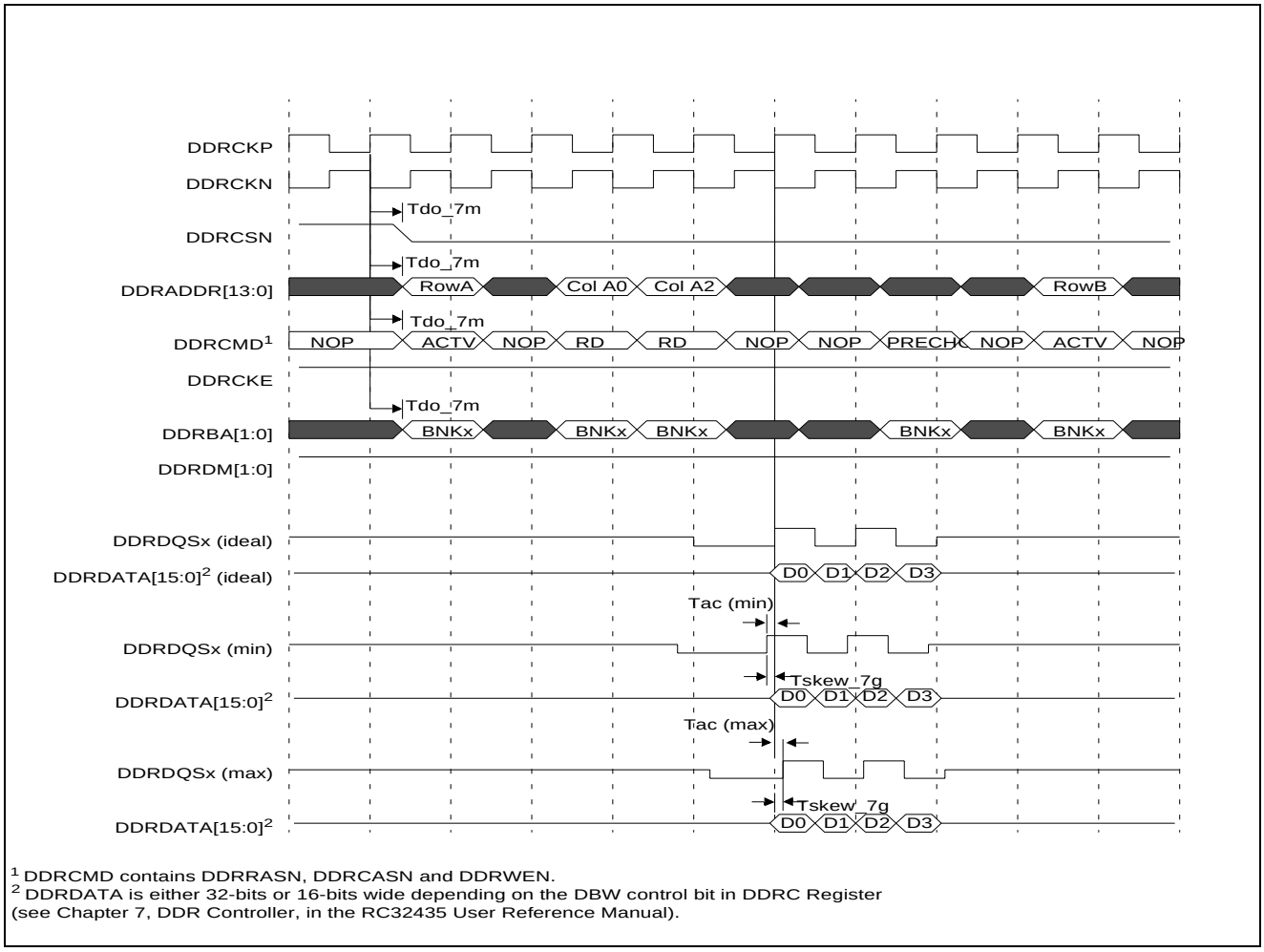
Signal	Symbol	Reference Edge	266MHz		300MHz		350MHz		400MHz		Unit	Timing Diagram Reference
			Min	Max	Min	Max	Min	Max	Min	Max		
Memory Bus - DDR Access												
DDRDATA[15:0]	Tskew_7g	DDRDQSx	0	0.9	0	0.8[1]	0	0.7	0.0	0.6	ns	See Figures 6 and 7.
	Tdo_7k[2]		1.2	1.9	1.0	1.7	0.7	1.5	0.5	1.4	ns	
DDRDM[1:0]	Tdo_7l	DDRDQSx	1.2	1.9	1.0	1.7	0.7	1.5	0.5	1.4	ns	
DDRDQS[1:0]	Tdo_7i	DDRCKP	-0.75	0.75	-0.75	0.75	-0.7	0.7	-0.7	0.7	ns	
DDRADDR[13:0], DDRBA[1:0], DDRCASN, DDRCKE, DDRCSN, DDRRASN, DDRWEN	Tdo_7m	DDRCKP	1.0	4.0	1.0	4.3	1.0	4.0	1.0	4.0	ns	

Table 7 DDR SDRAM Timing Characteristics

1. Meets DDR timing requirements for 150MHz clock rate DDR SDRAMs with 300 ps remaining margin to compensate for PCB propagation mismatches, which is adequate to guarantee functional timing, provided the RC32435 DDR layout guidelines are adhered to.

2. Setup times are calculated as applicable clock period - Tdo max. For example, if the DDR is running at 266MHz, it uses a 133MHz input clock. The period for a 133MHz clock is 7.5ns. If the Tdo max value is 4.6ns, the T_{IS} parameter is 7.5ns minus 4.6ns = 2.9ns. The DDR spec for this parameter is 1ns, so there is 1.9ns of slack left over for board propagation. Calculations for T_{DS} are similar, but since this parameter is taken relative to the DDRDQS signals, which are referenced on both edges, the effective period with a 133MHz input clock is only 3.75ns. So, if the max Tdo is 1.9ns, we have 3.75ns minus 1.9ns = 1.85ns for T_{DS}. The DDR data sheet specs a value of 0.5ns for 266MHz, so this leaves 1.35ns slack for board propagation delays.

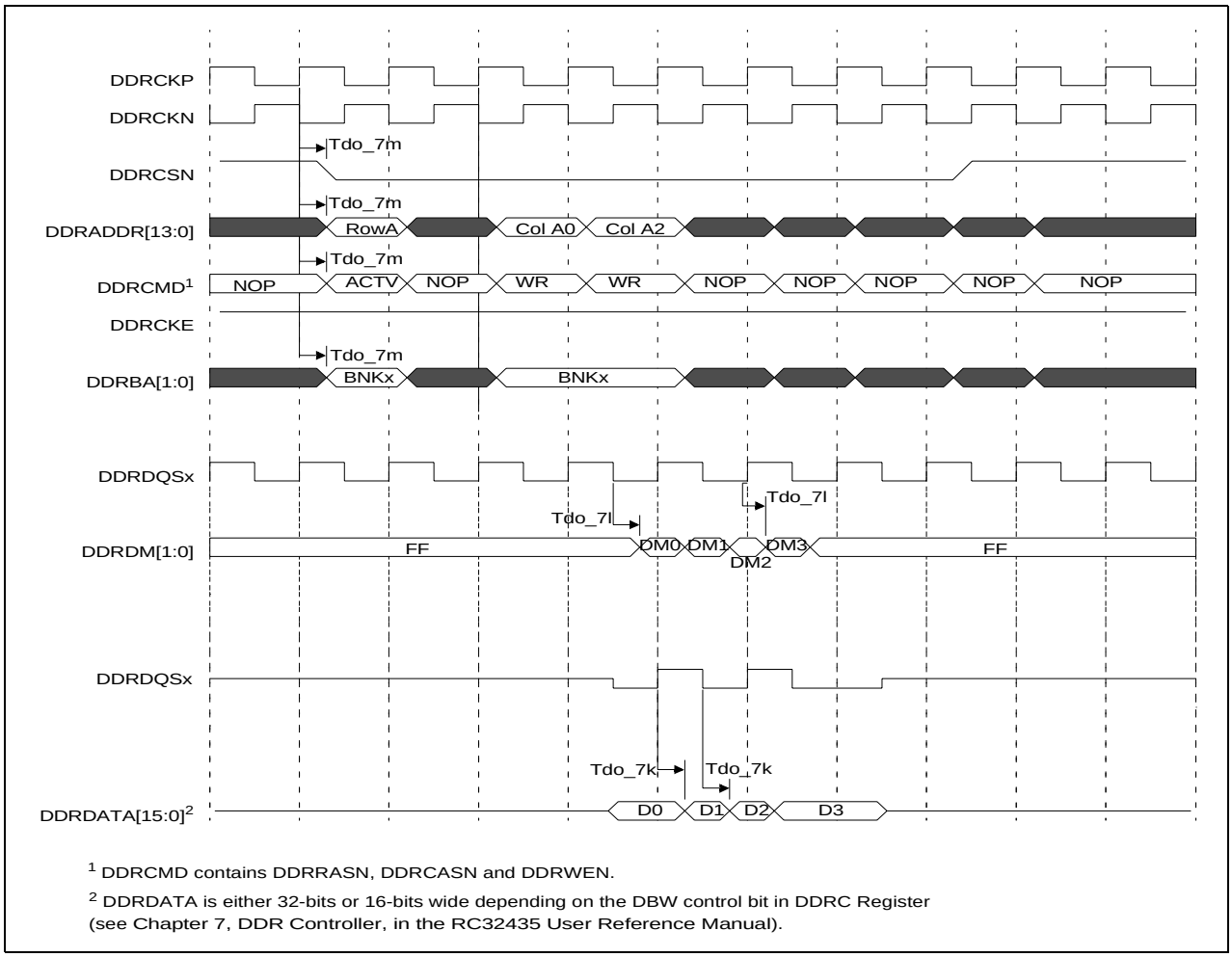
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[1] DDRCMD contains DDRRASN, DDRCASN and DDRWEN.
[2] DDRDATA is either 32-bits or 16-bits wide depending on the DBW control bit in DDRC Register (see Chapter 7, DDR Controller, in the RC32435 User Reference Manual).

Figure 6 DDR SDRAM AC Timing Waveform - SDRAM Read Access

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[1] DDRCMD contains DDRRASN, DDRCASN and DDRWEN.

[2] DDRDATA is either 32-bits or 16-bits wide depending on the DBW control bit in DDRC Register (see Chapter 7, DDR Controller, in the RC32435 User Reference Manual).

Figure 7 DDR SDRAM Timing Waveform — Write Access

Signal	Symbol	Reference Edge	266MHz		300MHz		350MHz		400MHz		Unit	Condi-tions	Timing Diagram Reference
			Min	Max	Min	Max	Min	Max	Min	Max			
Memory and Peripheral Bus[1]													See Figures 8 and 9.
MADDR[21:0]	Tdo_8a	EXTCLK rising	0.4	4.5	0.4	4.5	0.4	4.5	0.4	4.5	ns		
	Tdz_8a[2]		—	—	—	—	—	—	—	—	ns		
	Tzd_8a[2]		—	—	—	—	—	—	—	—	ns		
MADDR[25:22]	Tdo_8b	EXTCLK rising	0.4	4.5	0.4	4.5	0.4	4.5	0.4	4.5	ns		
	Tdz_8b[2]		—	—	—	—	—	—	—	—	ns		
	Tzd_8b[2]		—	—	—	—	—	—	—	—	ns		

Table 8 Memory and Peripheral Bus AC Timing Characteristics (Part 1 of 2)

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Signal	Symbol	Reference Edge	266MHz		300MHz		350MHz		400MHz		Unit	Condi-tions	Timing Diagram Reference
			Min	Max	Min	Max	Min	Max	Min	Max			
MDATA[7:0]	Tsu_8c	EXTCLK rising	6.0	—	6.0	—	6.0	—	6.0	—	ns		See Figures 8 and 9 (cont.).
	Thld_8c		0	—	0	—	0	—	0	—	ns		
	Tdo_8c		0.4	4.5	0.4	4.5	0.4	4.5	0.4	4.5	ns		
	Tdz_8c[2]		0	0.5	0	0.5	0	0.5	0	0.5	ns		
	Tzd_8c[2]		0.4	3.3	0.4	3.3	0.4	3.3	0.4	3.3	ns		
EXTCLK[3]	Tper_8d	none	7.5	—	6.66	—	6.66	—	6.66	—	ns		
BDIRN	Tdo_8e	EXTCLK rising	0.4	3.8	0.4	3.8	0.4	3.8	0.4	3.8	ns		
	Tdz_8e[2]		—	—	—	—	—	—	—	—	ns		
	Tzd_8e[2]		—	—	—	—	—	—	—	—	ns		
BOEN	Tdo_8f	EXTCLK rising	0.4	3.8	0.4	3.8	0.4	3.8	0.4	3.8	ns		
	Tdz_8f[2]		—	—	—	—	—	—	—	—	ns		
	Tzd_8f[2]		—	—	—	—	—	—	—	—	ns		
WAITACKN[4]	Tsu_8h	EXTCLK rising	6.5	—	6.5	—	6.5	—	6.5	—	ns		
	Thld_8h		0	—	0	—	0	—	0	—	ns		
	Tpw_8h[2]	none	2(EXTCLK)	—	2(EXTCLK)	—	2(EXTCLK)	—	2(EXTCLK)	—	ns		
CSN[3:0]	Tdo_8i	EXTCLK rising	0.4	4.0	0.4	4.0	0.4	4.0	0.4	4.0	ns		
	Tdz_8i[2]		—	—	—	—	—	—	—	—	ns		
	Tzd_8i[2]		—	—	—	—	—	—	—	—	ns		
RWN	Tdo_8j	EXTCLK rising	0.4	3.8	0.4	3.8	0.4	3.8	0.4	3.8	ns		
	Tdz_8j[2]		—	—	—	—	—	—	—	—	ns		
	Tzd_8j[2]		—	—	—	—	—	—	—	—	ns		
OEN	Tdo_8k	EXTCLK rising	0.4	4.0	0.4	4.0	0.4	4.0	0.4	4.0	ns		
	Tdz_8k[2]		—	—	—	—	—	—	—	—	ns		
	Tzd_8k[2]		—	—	—	—	—	—	—	—	ns		
WEN	Tdo_8l	EXTCLK rising	0.4	3.7	0.4	3.7	0.4	3.7	0.4	3.7	ns		
	Tdz_8l[2]		—	—	—	—	—	—	—	—	ns		
	Tzd_8l[2]		—	—	—	—	—	—	—	—	ns		

Table 8 Memory and Peripheral Bus AC Timing Characteristics (Part 2 of 2)

1. The RC32435 provides bus turnaround cycles to prevent bus contention when going from read to write, write to read, and during external bus ownership. For example, there are no cycles where an external device and the RC32435 are both driving. See Chapter 6, Device Controller, in the RC32435 User Reference Manual.

2. The values for this symbol were determined by calculation, not by testing.

3. The frequency of EXTCLK is programmable. See the External Clock Divider (MDATA[5:4]) description in Table 3 of this data sheet.

4. WAITACKN must meet the setup and hold times if it is synchronous or the minimum pulse width if it is asynchronous.

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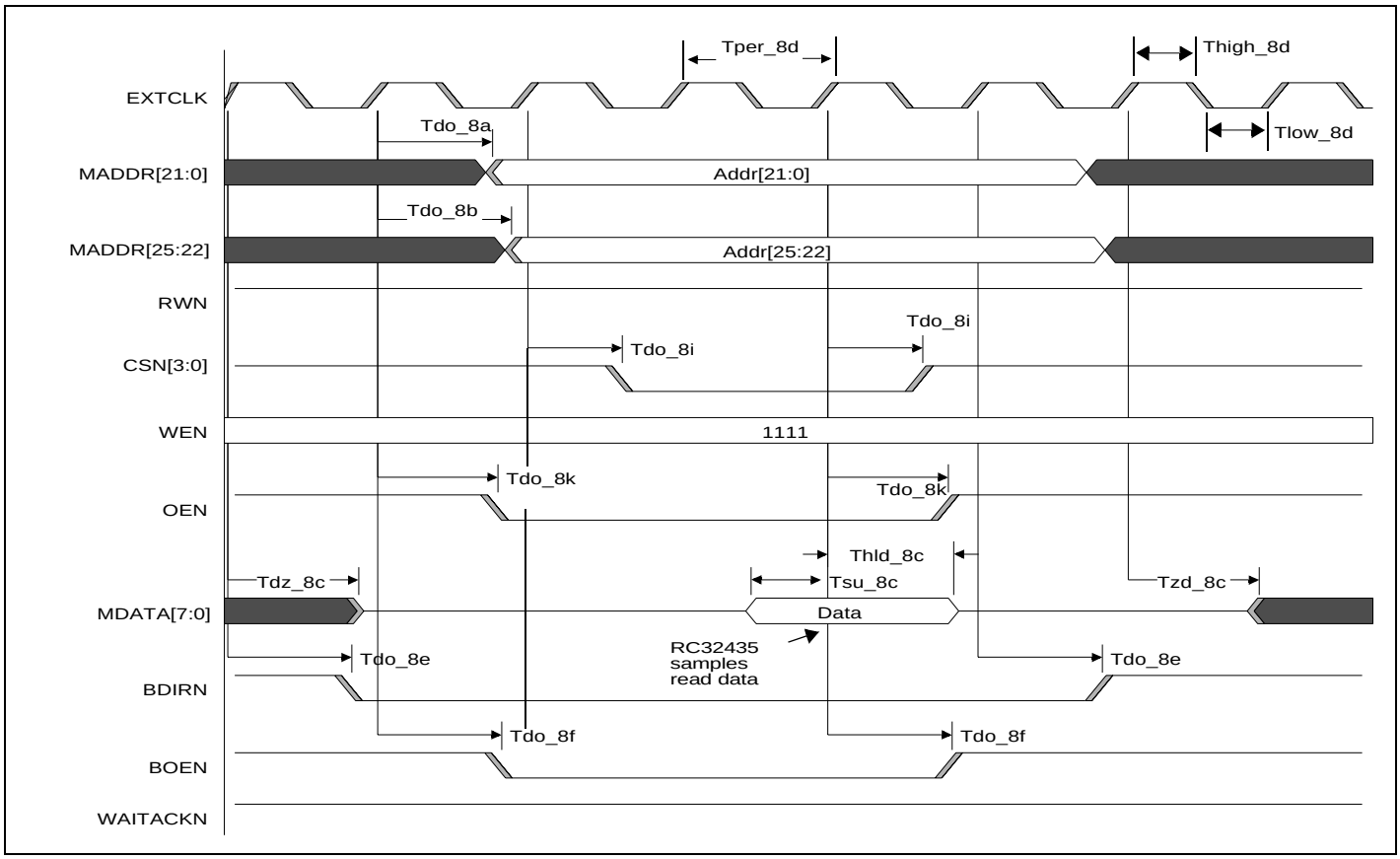


Figure 8 Memory and Peripheral Bus AC Timing Waveform — Read Access

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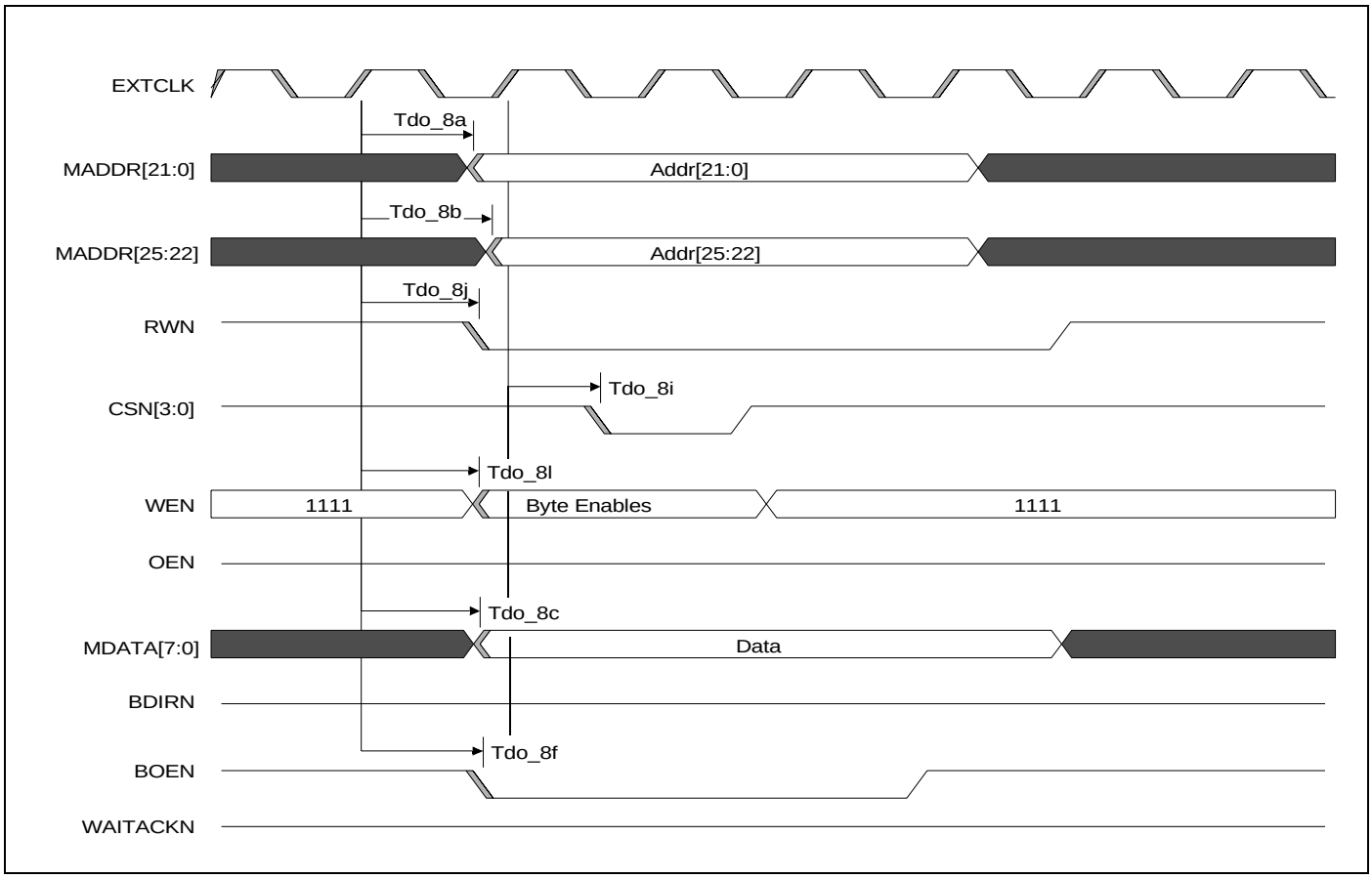


Figure 9 Memory and Peripheral Bus AC Timing Waveform — Write Access

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Signal	Symbol	Reference Edge	266MHz		300MHz		350MHz		400MHz		Unit	Condi-tions	Timing Diagram Reference
			Min	Max	Min	Max	Min	Max	Min	Max			
Ethernet													
MIIMDC	Tper_9a	None	30.0	—	30.0	—	30.0	—	30.0	—	ns		See Figure 10.
	Thigh_9a, Tlow_9a		12.0	—	12.0	—	12.0	—	12.0	—	ns		
MIIMDIO	Tsu_9b	MIIMDC rising	10.0	—	10.0	—	10.0	—	10.0	—	ns		
	Thld_9b		0.0	—	0.0	—	0.0	—	0.0	—	ns		
	Tdo_9b[1]		10	300	10	300	10	300	10	300	ns		
Ethernet — MII Mode													
MIIRXCLK, MIITXCLK[2]	Tper_9c	None	399.96	400.4	399.96	400.4	399.96	400.4	399.96	400.4	ns	10 Mbps	See Figure 10.
	Thigh_9c, Tlow_9c		140	260	140	260	140	260	140	260	ns		
	Trise_9c, Tfall_9c		—	3.0	—	3.0	—	3.0	—	3.0	ns		
MIIRXCLK, MIITXCLK[2]	Tper_9d	None	39.9	40.0	39.9	40.0	39.9	40.0	39.9	40.0	ns	100 Mbps	
	Thigh_9d, Tlow_9d		14.0	26.0	14.0	26.0	14.0	26.0	14.0	26.0	ns		
	Trise_9d, Tfall_9d		—	2.0	—	2.0	—	2.0	—	2.0	ns		
MIIRXD[3:0], MIIRXDV, MIIRXER	Tsu_9e	MIIxRXCLK rising	10.0	—	10.0	—	10.0	—	10.0	—	ns		
	Thld_9e		10.0	—	10.0	—	10.0	—	10.0	—	ns		
MIITXD[3:0], MIITXENP, MIITXER	Tdo_9f	MIIxTXCLK rising	0.0	25.0	0.0	25.0	0.0	25.0	0.0	25.0	ns		
Ethernet — RMII Mode													
RMIIREFCLK	Tper_9i	None	19.9	20.1	19.9	20.1	19.9	20.1	19.9	20.1	ns		See Figure 10.
	Thigh_9i, Tlow_9i		7.0	13.0	7.0	13.0	7.0	13.0	7.0	13.0	ns		
RMIITXEN, RMIITXD[1:0]	Tdo_9j	MIIRXCLK rising	2.0	—	2.0	—	2.0	—	2.0	—	ns		
RMIICRSDV, RMIIRXER, RMIIRXD[1:0]	Tsu_9k		5.5	14.5	5.5	14.5	5.5	14.5	5.5	14.5	ns		

Table 9 Ethernet AC Timing Characteristics

1. The values for this symbol were determined by calculation, not by testing.

2. The ethernet clock (MIIRXCLK and MIITXCLK) frequency must be equal to or less than 1/2 ICLK (MIIRXCLK and MIITXCLK <= 1/2(ICLK)).

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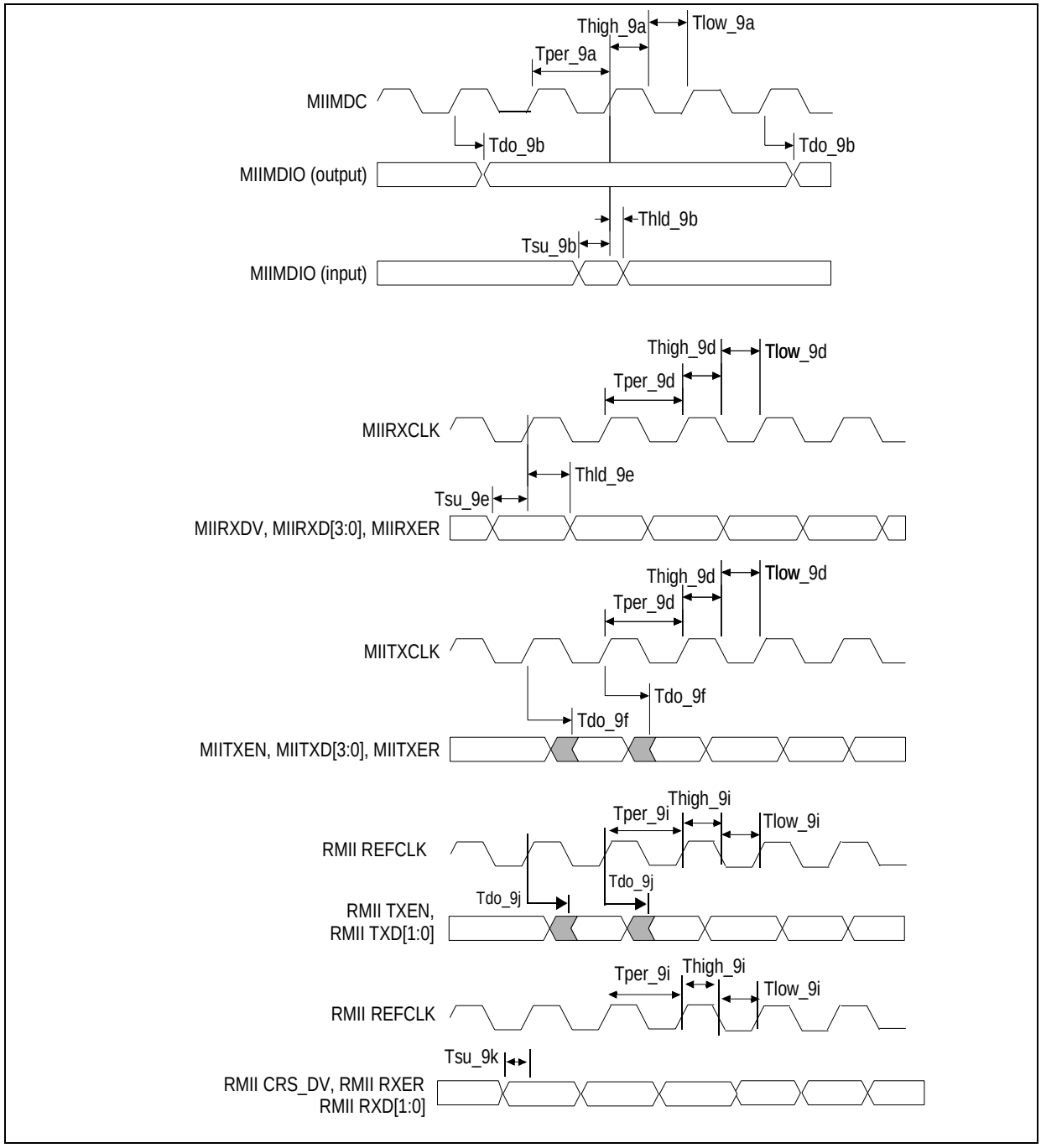


Figure 10 Ethernet AC Timing Waveform

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Signal	Symbol	Reference Edge	266MHz		300MHz		350MHz		400MHz		Unit	Condi-tions	Timing Diagram Reference
			Min	Max	Min	Max	Min	Max	Min	Max			
PCI[1]													
PCICLK[2]	Tper_10a	none	15.0	30.0	15.0	30.0	15.0	30.0	15.0	30.0	ns	66 MHz PCI	See Figure 11.
	Thigh_10a, Tlow_10a		6.0	—	6.0	—	6.0	—	6.0	—	ns		
	Tslew_10a		1.5	4.0	1.5	4.0	1.5	4.0	1.5	4.0	V/ns		
PCIAD[31:0], PCIBEN[3:0], PCIDEVSELN, PCIFRA-MEN,PCIIR-DYN, PCILOCKN, PCIPAR, PCI-PERRN, PCIS-TOPN, PCITRDY	Tsu_10b	PCICLK rising	3.0	—	3.0	—	3.0	—	3.0	—	ns		
	Thld_10b		0	—	0	—	0	—	0	—	ns		
	Tdo_10b		2.0	6.0	2.0	6.0	2.0	6.0	2.0	6.0	ns		
	Tdz_10b[3]		—	14.0	—	14.0	—	14.0	—	14.0	ns		
	Tzd_10b[3]		2.0	—	2.0	—	2.0	—	2.0	—	ns		
PCIGNTN[3:0], PCIREQN[3:0]	Tsu_10c	PCICLK rising	5.0	—	5.0	—	5.0	—	5.0	—	ns		
	Thld_10c		0	—	0	—	0	—	0	—	ns		
	Tdo_10c		2.0	6.0	2.0	6.0	2.0	6.0	2.0	6.0	ns		
PCIRSTN (out-put)[4]	Tpw_10d[3]	None	4000 (CLK)	—	4000 (CLK)	—	4000 (CLK)	—	4000 (CLK)	—	ns		See Figures 15 and 16
PCIRSTN (input)[4,5]	Tpw_10e[3]	None	2(CLK)	—	2(CLK)	—	2(CLK)	—	2(CLK)	—	ns		
	Tdz_10e[3]	PCIRSTN falling	6(CLK)	—	6(CLK)	—	6(CLK)	—	6(CLK)	—	ns		
PCISERRN[6]	Tsu_10f	PCICLK rising	3.0	—	3.0	—	3.0	—	3.0	—	ns		See Figure 11
	Thld_10f		0	—	0	—	0	—	0	—	ns		
	Tdo_10f		2.0	6.0	2.0	6.0	2.0	6.0	2.0	6.0	ns		
PCIMUINTN[6]	Tdo_10g	PCICLK rising	4.7	11.1	4.7	11.1	4.7	11.1	4.7	11.1	ns		

Table 10 PCI AC Timing Characteristics

1. This PCI interface conforms to the PCI Local Bus Specification, Rev 2.2.

2. PCICLK must be equal to or less than two times ICLK (PCICLK <= 2(ICLK)) with a maximum PCICLK of 66 MHz.

3. The values for this symbol were determined by calculation, not by testing.

4. PCIRSTN is an output in host mode and an input in satellite mode.

5. To meet the PCI delay specification from reset asserted to outputs floating, the PCI reset should be logically combined with the COLDRSTN input, instead of input on PCIRSTN.

6. PCISERRN and PCIMUINTN use open collector I/O types.

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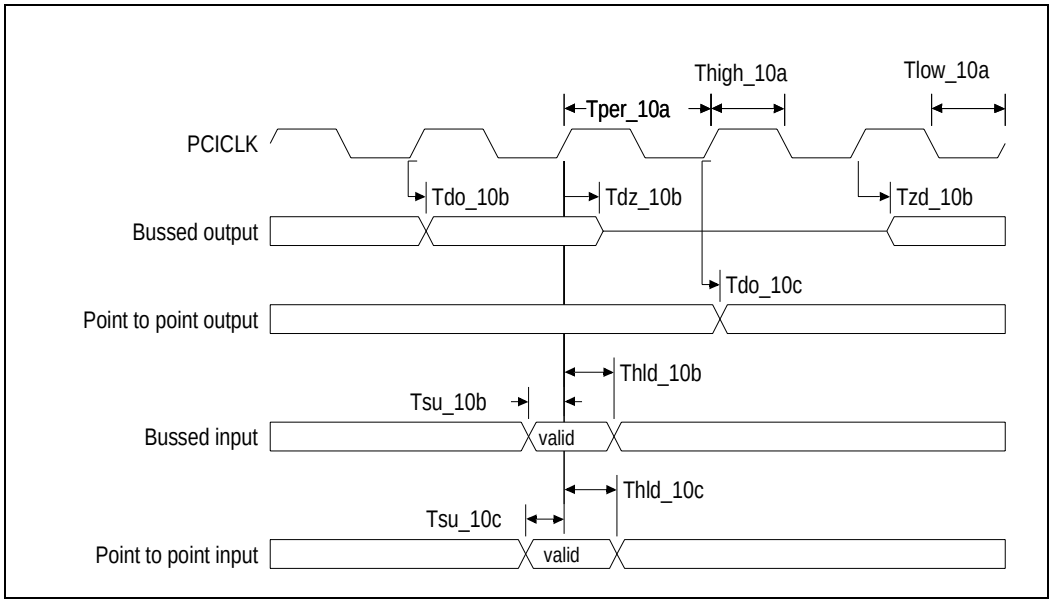
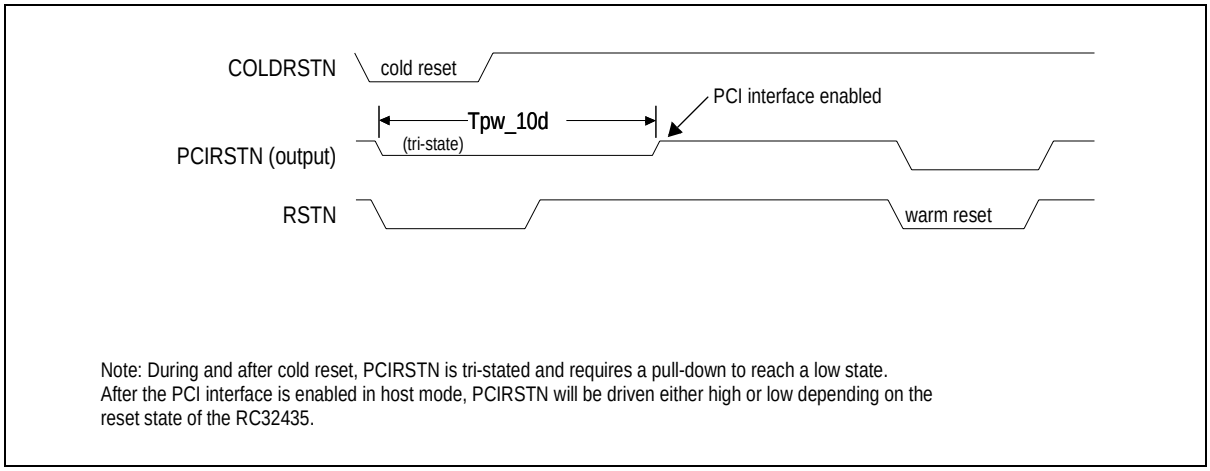


Figure 11 PCI AC Timing Waveform



Note: During and after cold reset, PCIRSTN is tri-stated and requires a pull-down to reach a low state. After the PCI interface is enabled in host mode, PCIRSTN will be driven either high or low depending on the reset state of the RC32435.

Figure 12 PCI AC Timing Waveform — PCI Reset in Host Mode

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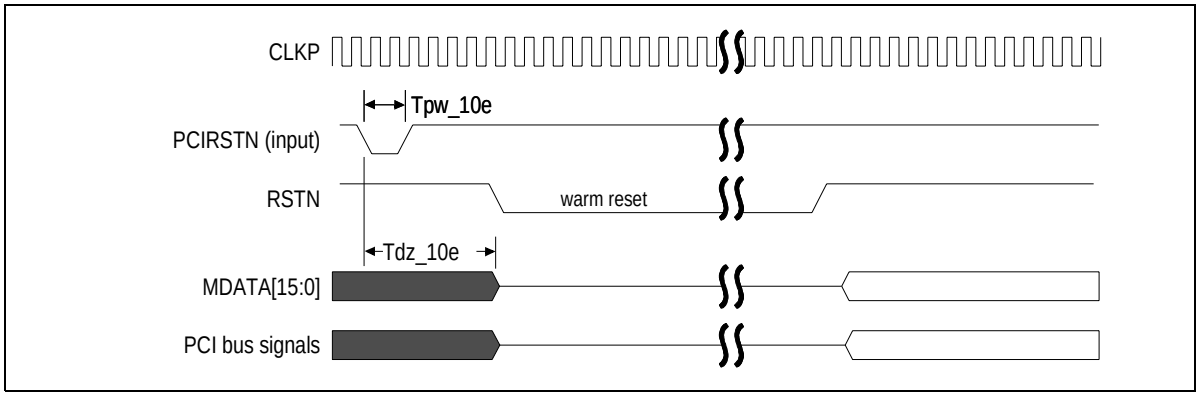


Figure 13 PCI AC Timing Waveform — PCI Reset in Satellite Mode

Signal	Symbol	Reference Edge	266MHz		300MHz		350MHz		400MHz		Unit	Conditions	Timing Diagram Reference
			Min	Max	Min	Max	Min	Max	Min	Max			
I²C[1]													
SCL	Frequency	none	0	100	0	100	0	100	0	100	kHz	100 KHz	See Figure 14.
	Thigh_12a, Tlow_12a		4.0	—	4.0	—	4.0	—	4.0	—	µs		
	Trise_12a		—	1000	—	1000	—	1000	—	1000	ns		
	Tfall_12a		—	300	—	300	—	300	—	300	ns		
SDA	Tsu_12b	SCL rising	250	—	250	—	250	—	250	—	ns		
	Thld_12b		0	3.45	0	3.45	0	3.45	0	3.45	µs		
	Trise_12b		—	1000	—	1000	—	1000	—	1000	ns		
	Tfall_12b		—	300	—	300	—	300	—	300	ns		
Start or repeated start condition	Tsu_12c	SDA falling	4.7	—	4.7	—	4.7	—	4.7	—	µs		
	Thld_12c		4.0	—	4.0	—	4.0	—	4.0	—	µs		
Stop condition	Tsu_12d	SDA rising	4.0	—	4.0	—	4.0	—	4.0	—	µs		
Bus free time between a stop and start condition	Tdelay_12e		4.7	—	4.7	—	4.7	—	4.7	—	µs		
SCL	Frequency	none	0	400	0	400	0	400	0	400	kHz	400 KHz	
	Thigh_12a, Tlow_12a		0.6	—	0.6	—	0.6	—	0.6	—	µs		
	Trise_12a		—	300	—	300	—	300	—	300	ns		
	Tfall_12a		—	300	—	300	—	300	—	300	ns		
SDA	Tsu_12b	SCL rising	100	—	100	—	100	—	100	—	ns		
	Thld_12b		0	0.9	0	0.9	0	0.9	0	0.9	µs		
	Trise_12b		—	300	—	300	—	300	—	300	ns		
	Tfall_12ba		—	300	—	300	—	300	—	300	ns		

Table 11 I²C AC Timing Characteristics (Part 1 of 2)

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Signal	Symbol	Reference Edge	266MHz		300MHz		350MHz		400MHz		Unit	Conditions	Timing Diagram Reference
			Min	Max	Min	Max	Min	Max	Min	Max			
Start or repeated start condition	Tsu_12c	SDA falling	0.6	—	0.6	—	0.6	—	0.6	—	µs	400 KHz	See Figure 14.
	Thld_12c		0.6	—	0.6	—	0.6	—	0.6	—	µs		
Stop condition	Tsu_12d	SDA rising	0.6	—	0.6	—	0.6	—	0.6	—	µs		
Bus free time between a stop and start condition	Tdelay_12e		1.3	—	1.3	—	1.3	—	1.3	—	µs		

Table 11 I²C AC Timing Characteristics (Part 2 of 2)

1. For more information, see the I²C-Bus specification by Philips Semiconductor.

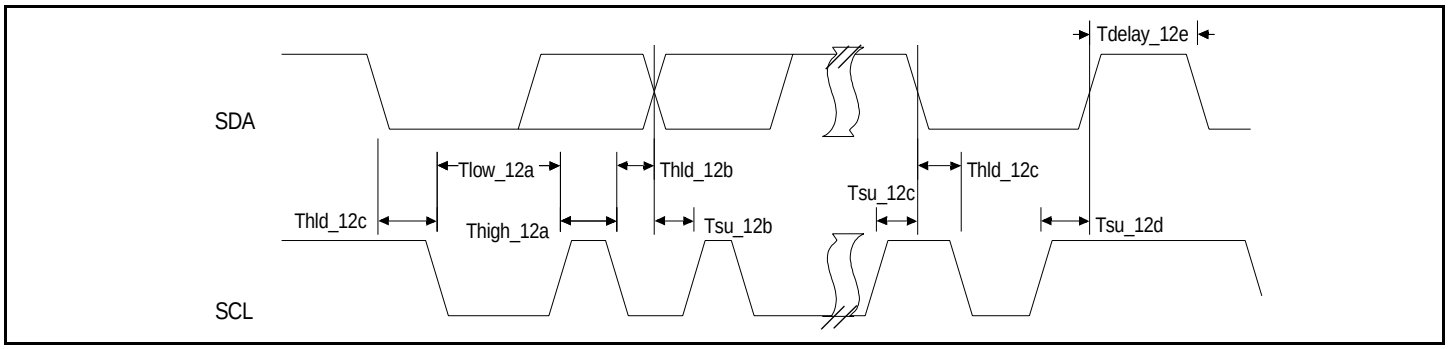


Figure 14 I2C AC Timing Waveform

Signal	Symbol	Reference Edge	266MHz		300MHz		350MHz		400MHz		Unit	Conditions	Timing Diagram Reference
			Min	Max	Min	Max	Min	Max	Min	Max			
GPIO													
GPIO[13:0]	Tpw_13b[1]	None	2(ICLK)	—	2(ICLK)	—	2(ICLK)	—	2(ICLK)	—	ns		See Figure 15.

Table 12 GPIO AC Timing Characteristics

1. The values for this symbol were determined by calculation, not by testing.

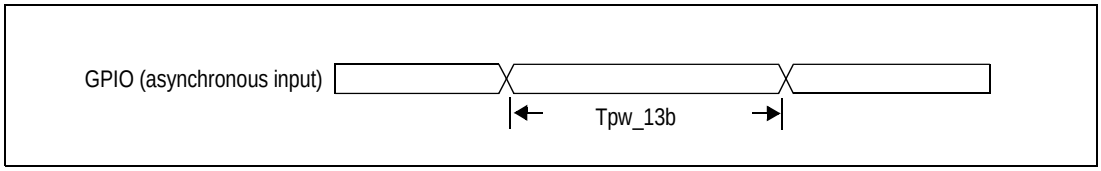


Figure 15 GPIO AC Timing Waveform

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Signal	Symbol	Reference Edge	266MHz		300MHz		350MHz		400MHz		Unit	Condi-tions	Timing Diagram Reference
			Min	Max	Min	Max	Min	Max	Min	Max			
SPI[1]													
SCK	Tper_15a	None	100	166667	100	166667	100	166667	100	166667	ns	SPI	See Figures 16, 17, and 18.
	Thigh_15a, Tlow_15a		40	83353	40	83353	40	83353	40	83353	ns	SPI	
SDI	Tsu_15b	SCK rising or falling	60	—	60	—	60	—	60	—	ns	SPI	See Figures 16, 17, and 18.
	Thld_15b		60	—	60	—	60	—	60	—	ns	SPI	
SDO	Tdo_15c	SCK rising or falling	0	60	0	60	0	60	0	60	ns	SPI	
SCK, SDI, SDO	Tpw_15e	None	2(ICLK)	—	2(ICLK)	—	2(ICLK)	—	2(ICLK)	—	ns	Bit I/O	

Table 13 SPI AC Timing Characteristics

1. In SPI mode, the SCK period and sampling edge are programmable. In PCI mode, the SCK period is fixed and the sampling edge is rising.

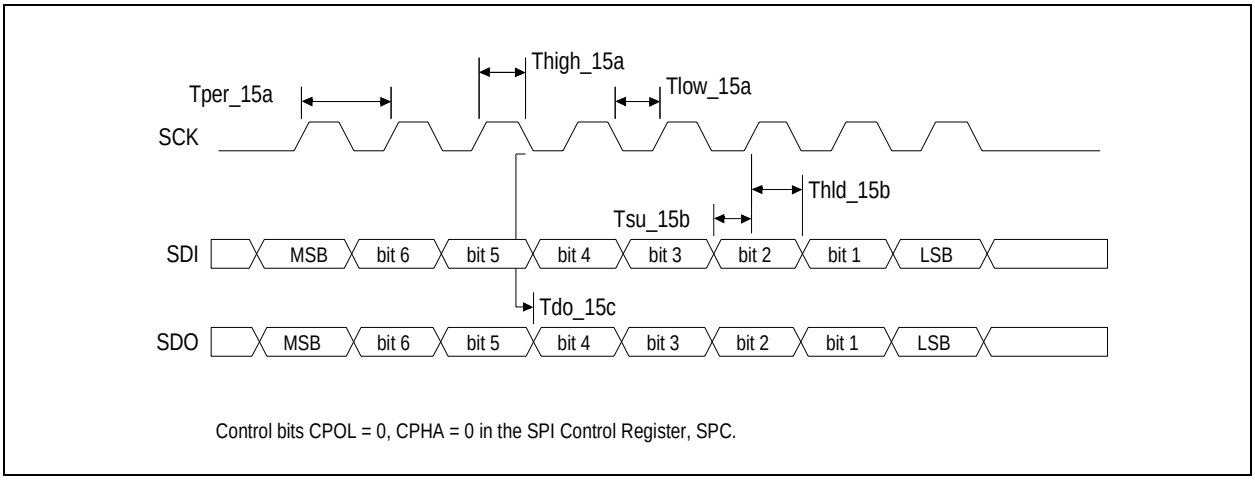


Figure 16 SPI AC Timing Waveform — Clock Polarity 0, Clock Phase 0

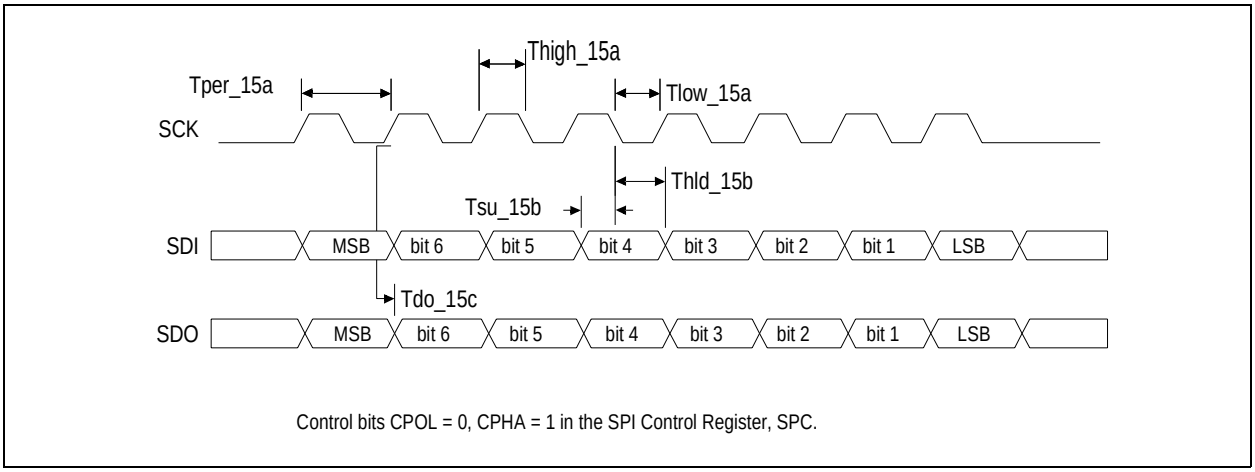


Figure 17 SPI AC Timing Waveform — Clock Polarity 0, Clock Phase 1

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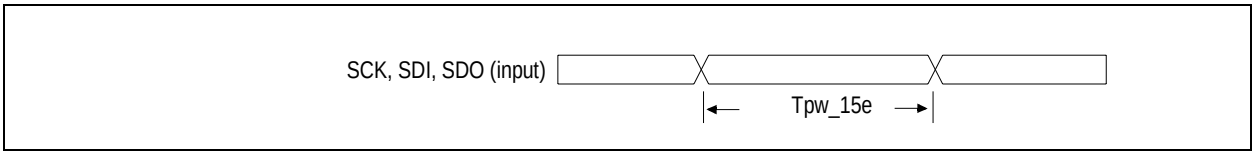


Figure 18 SPI AC Timing Waveform — Bit I/O Mode

Signal	Symbol	Reference Edge	266MHz		300MHz		350MHz		400MHz		Unit	Condi-tions	Timing Diagram Reference
			Min	Max	Min	Max	Min	Max	Min	Max			
EJTAG and JTAG													
JTAG_TCK	Tper_16a	none	25.0	50.0	25.0	50.0	25.0	50.0	25.0	50.0	ns		See Figure 19.
	Thigh_16a, Tlow_16a		10.0	25.0	10.0	25.0	10.0	25.0	10.0	25.0	ns		
JTAG_TMS[1], JTAG_TDI	Tsu_16b	JTAG_TCK rising	2.4	—	2.4	—	2.4	—	2.4	—	ns		
	Thld_16b		1.0	—	1.0	—	1.0	—	1.0	—	ns		
JTAG_TDO	Tdo_16c	JTAG_TCK fall-ing	—	11.3	—	11.3	—	11.3	—	11.3	ns		
	Tdz_16c[2]		—	11.3	—	11.3	—	11.3	—	11.3	ns		
JTAG_TRST_N	Tpw_16d[2]	none	25.0	—	25.0	—	25.0	—	25.0	—	ns		
EJTAG_TMS[1]	Tsu_16e	JTAG_TCK rising	2.0	—	2.0	—	2.0	—	2.0	—	ns		
	Thld_6e		1.0	—	1.0	—	1.0	—	1.0	—	ns		

Table 14 JTAG AC Timing Characteristics

1. The JTAG specification, IEEE 1149.1, recommends that both JTAG_TMS and EJTAG_TMS should be held at 1 while the signal applied at JTAG_TRST_N changes from 0 to 1. Otherwise, a race may occur if JTAG_TRST_N is deasserted (going from low to high) on a rising edge of JTAG_TCK when either JTAG_TMS or EJTAG_TMS is low, because the TAP controller might go to either the Run-Test/Idle state or stay in the Test-Logic-Reset state.

2. The values for this symbol were determined by calculation, not by testing.

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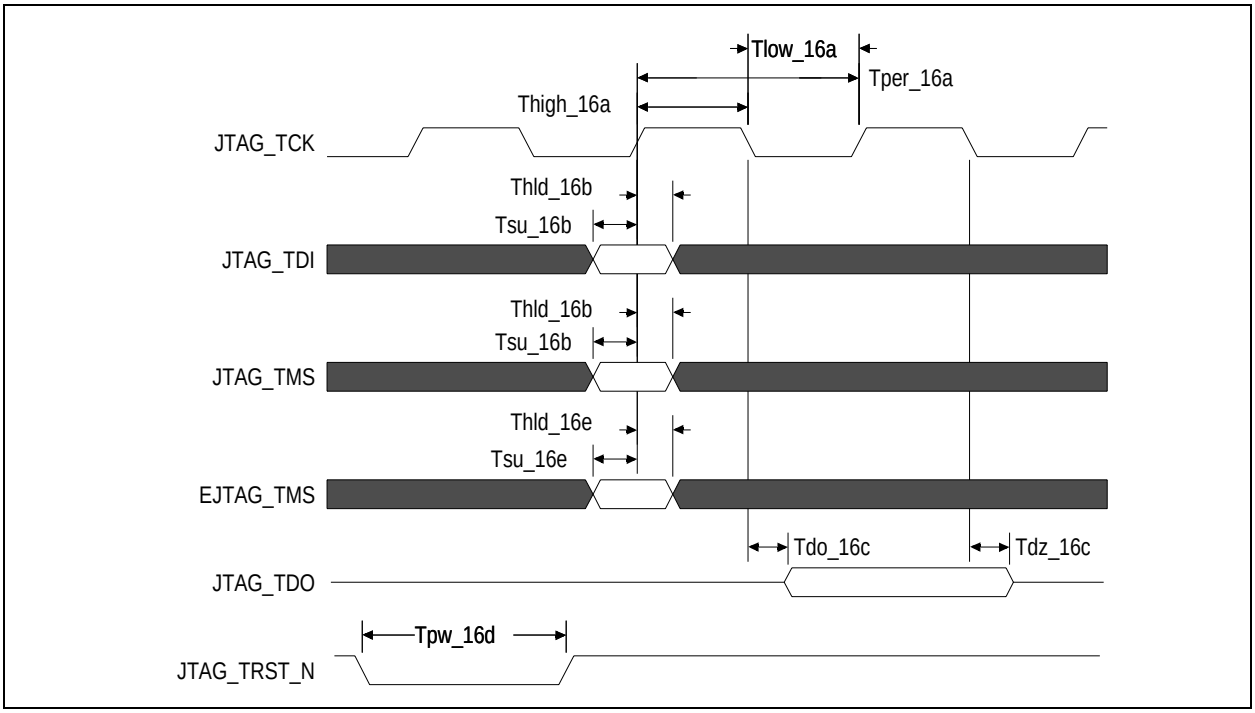


Figure 19 JTAG AC Timing Waveform

The IEEE 1149.1 specification requires that the JTAG and EJTAG TAP controllers be reset at power-up whether or not the interfaces are used for a boundary scan or a probe. Reset can occur through a pull-down resistor on JTAG_TRST_N if the probe is not connected. However, on-chip pull-up resistors are implemented on the RC32435 due to an IEEE 1149.1 requirement. Having on-chip pull-up and external pull-down resistors for the JTAG_TRST_N signal requires special care in the design to ensure that a valid logical level is provided to JTAG_TRST_N, such as using a small external pull-down resistor to ensure this level overrides the on-chip pull-up. An alternative is to use an active power-up reset circuit for JTAG_TRST_N, which drives JTAG_TRST_N low only at power-up and then holds JTAG_TRST_N high afterwards with a pull-up resistor.

Figure 20 shows the electrical connection of the EJTAG probe target system connector.

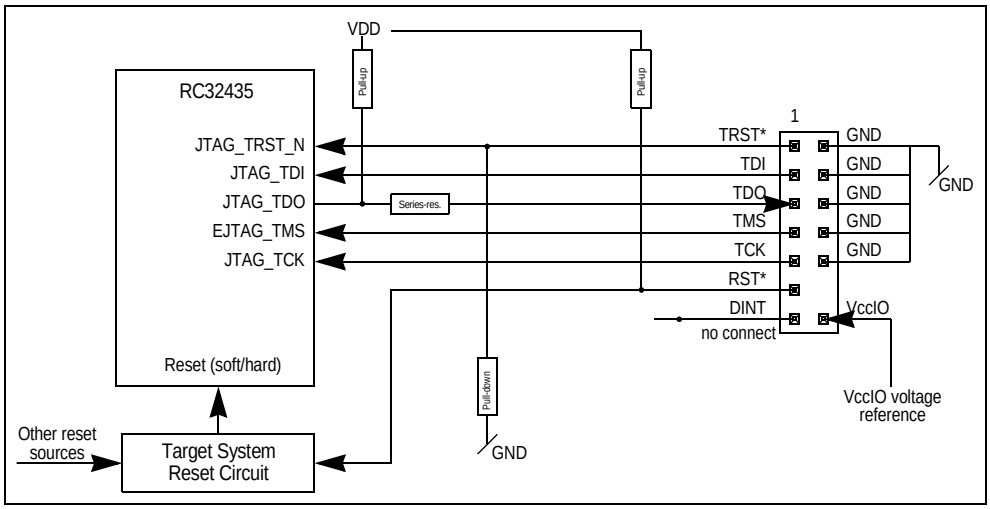


Figure 20 Target System Electrical EJTAG Connection

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Using the EJTAG Probe

In Figure 20, the pull-up resistors for JTAG_TDO and RST*, the pull-down resistor for JTAG_TRST_N, and the series resistor for JTAG_TDO must be adjusted to the specific design. However, the recommended pull-up/down resistor is 1.0 kΩ because a low value reduces crosstalk on the cable to the connector, allowing higher JTAG_TCK frequencies. A typical value for the series resistor is 33 Ω. Recommended resistor values have ± 5% tolerance.

If a probe is used, the pull-up resistor on JTAG_TDO must ensure that the JTAG_TDO level is high when no probe is connected and the JTAG_TDO output is tri-stated. This requirement allows reliable connection of the probe if it is hooked-up when the power is already on (hot plug). The pull-up resistor value of around 47 kΩ should be sufficient. Optional diodes to protect against overshoot and undershoot voltage can be added on the signals of the chip with EJTAG.

If a probe is used, the RST* signal must have a pull-up resistor because it is controlled by an open-collector (OC) driver in the probe, and thus is actively pulled low only. The pull-up resistor is responsible for the high value when not driven by the probe of 25pF. The input on the target system reset circuit must be able to accept the rise time when the pull-up resistor charges the capacitance to a high logical level. Vcc I/O must connect to a voltage reference that drops rapidly to below 0.5V when the target system loses power, even with a capacitive load of 25pF. The probe can thus detect the lost power condition.

For additional information on EJTAG, refer to Chapter 17 of the RC32435 User Reference Manual.

Phase-Locked Loop (PLL)

The phase-locked loop (PLL) multiplies the external oscillator input (pin CLK) according to the parameter provided by the boot configuration vector to create the processor clock (PCLK). Inherently, PLL circuits are only capable of generating clock frequencies within a limited range.

PLL Filters

It is recommended that the system designer provide a filter network of passive components for the PLL analog and digital power supplies. The PLL circuit power and PLL circuit ground should be isolated from power and ground with a filter circuit such as the one shown in Figure 21. Because the optimum values for the filter components depend upon the application and the system noise environment, these values should be considered as starting points for further experimentation within your specific application.

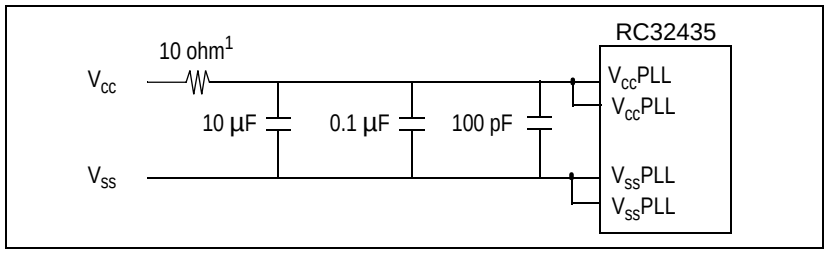


Figure 21 PLL Filter Circuit for Noisy Environments

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Recommended Operating Supply Voltages

Symbol	Parameter	Minimum	Typical	Maximum	Unit
V_{SS}	Common ground	0	0	0	V
V_{SS}PLL	PLL ground				
V_{CC}I/O	I/O supply except for SSTL_2[1]	3.135	3.3	3.465	V
V_{CC}SI/O (DDR)	I/O supply for SSTL_2[1]	2.375	2.5	2.625	V
V_{CC}PLL	PLL supply (digital)	1.1	1.2	1.3	V
V_{CC}APLL	PLL supply (analog)	3.135	3.3	3.465	V
V_{CC}Core	Internal logic supply	1.1	1.2	1.3	V
DDRVREF[2]	SSTL_2 input reference voltage	0.5(VccSI/O)	0.5(VccSI/O)	0.5(VccSI/O)	V
V_{TT}[3]	SSTL_2 termination voltage	DDRVREF - 0.04	DDRVREF	DDRVREF + 0.04	V

Table 15 RC32435 Operating Voltages

1. SSTL_2 I/Os are used to connect to DDR SDRAM.
2. Peak-to-peak AC noise on DDRVREF may not exceed ± 2% DDRVREF (DC).
3. V_{TT} of the SSTL_2 transmitting device must track DDRVREF of the receiving device.

Recommended Operating Temperatures

Grade	Temperature
Commercial	0°C to +70°C Ambient
Industrial	-40°C to +85°C Ambient

Table 16 RC32435 Operating Temperatures

Capacitive Load Deration

Refer to the 79RC32435 IBIS Model on the IDT web site (www.idt.com).

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Power-on Sequence

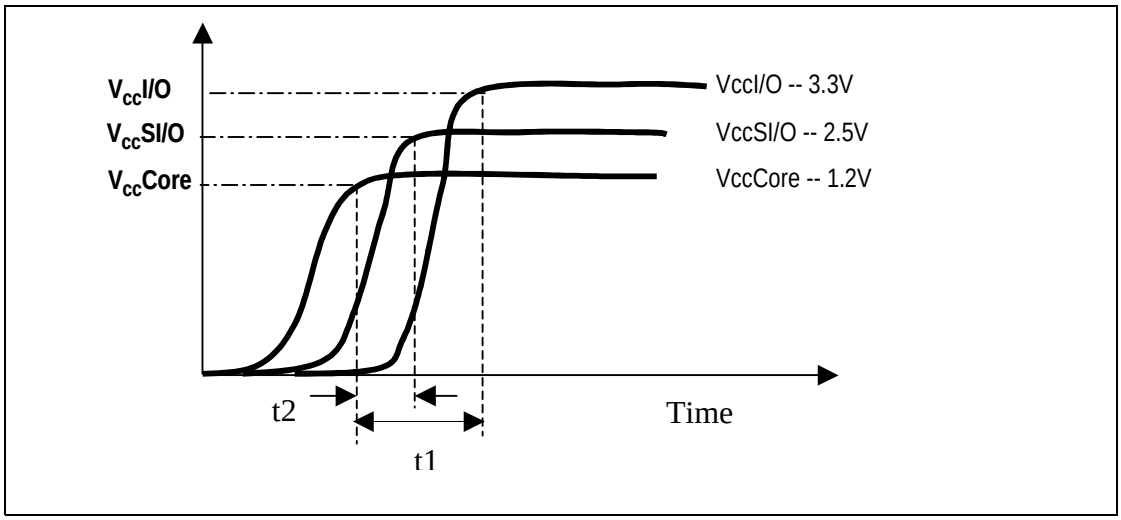
Three power-on sequences are given below. Sequence #1 is recommended because it will prevent I/O conflicts and will also allow the input signals to propagate when the I/O powers are brought up.

Note: The ESD diodes may be damaged if one of the voltages is applied and one of the other voltages is at a ground level.

A. Recommended Sequence

t2 > 0 whenever possible (V_{cc}Core)

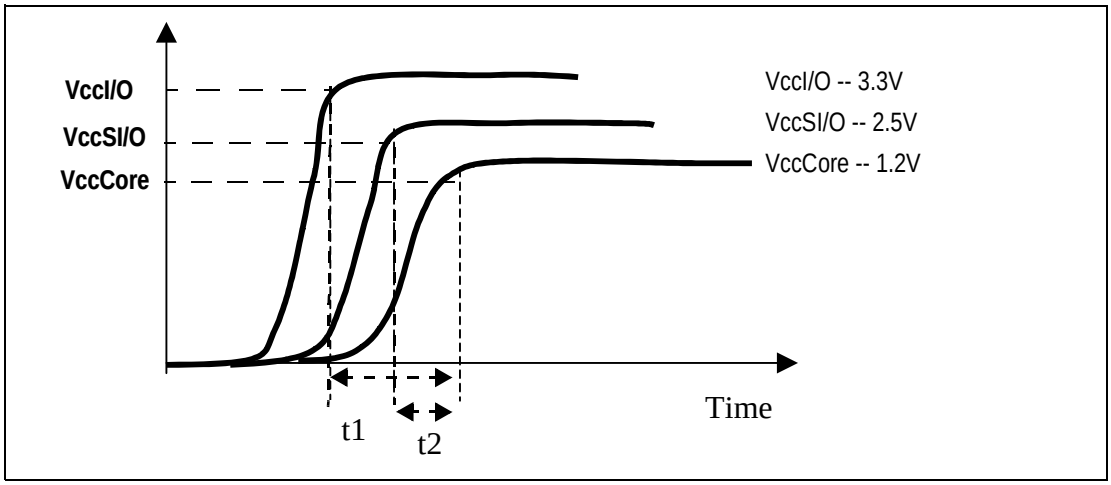
t1 - t2 can be 0 (V_{cc}SI/O followed by V_{cc}I/O)



B. Reverse Voltage Sequence

If sequence A is not feasible, then Sequence B can be used:

t1 <50ms and t2 <50ms to prevent damage.



C. Simultaneous Power-up

VccI/O, VccSI/O, and VccCore can be powered up simultaneously.

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Power Consumption

Parameter		266MHz		300MHz		350MHz		400MHz		Unit	Conditions
		Typ.	**Max.**	**Typ.**	**Max.**	**Typ.**	**Max.**	**Typ.**	**Max.**		
I_{cc} I/O		215	270	220	275	225	280	230	285	mA	C_L = 35 pF $T_{ambient}$ = 25°C Max. values use the maximum voltages listed in Table 15. Typical values use the typical voltages listed in that table. Note: For additional information, see Power Considerations for IDT Processors on the IDT web site www.idt.com.
I_{cc} SI/O (DDR)		70	85	75	90	85	100	95	110	mA	
I_{cc} Core, I_{cc} PLL	Normal mode	325	510	350	550	400	610	450	670	mA	
	Standby mode[1]	220	—	240	—	260	—	280	—	mA	
Power Dissipation	Normal mode	1.27	1.82	1.36	1.90	1.45	2.02	1.54	2.15	W	
	Standby mode[1]	0.73	—	0.78	—	0.84	—	0.90	—	W	

Table 17 RC32435 Power Consumption

1. The RC32435 enter Standby mode by executing WAIT instructions. Minimal I/O switching is assumed. On-chip logic outside the CPU core continues to function.

Power Curve

The following graph contains a power curve that shows power consumption at various core frequencies.

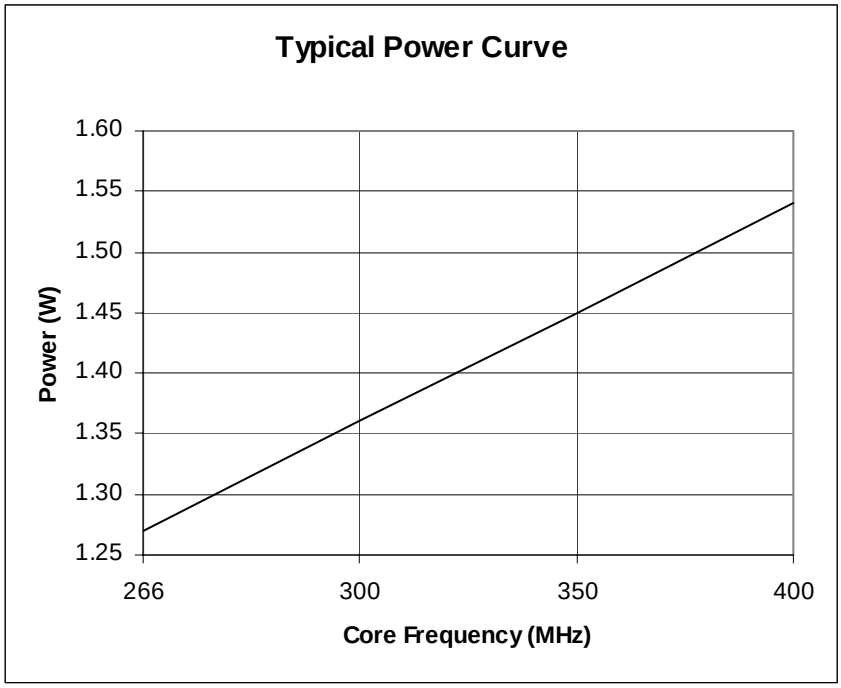


Figure 22 RC32435 Typical Power Usage

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DC Electrical Characteristics

Values based on systems running at recommended supply voltages, as shown in Table 15.

Note: See Table 2, Pin Characteristics, for a complete I/O listing.

I/O Type	Para-meter	Min.	Typical	Max.	Unit	Conditions
LOW Drive Output	I_{OL}	—	14.0	—	mA	V_{OL} = 0.4V
	I_{OH}	—	-12.0	—	mA	V_{OH} = 1.5V
HIGH Drive Output	I_{OL}	—	41.0	—	mA	V_{OL} = 0.4V
	I_{OH}	—	-42.0	—	mA	V_{OH} = 1.5V
Schmitt Trigger Input (STI)	V_{IL}	-0.3	—	0.8	V	—
	V_{IH}	2.0	—	V_{cc}I/O + 0.5	V	—
SSTL_2 (for DDR SDRAM)	I_{OL}	7.6	—	—	mA	V_{OL} = 0.5V
	I_{OH}	-7.6	—	—	mA	V_{OH} = 1.76V
	V_{IL}	-0.3	—	0.5(V_{cc}SI/O) - 0.18	V	
	V_{IH}	0.5(V_{cc}SI/O) + 0.18	—	V_{cc}SI/O + 0.3	V	
PCI	I_{OH}(AC) Switching	-12(V_{cc}I/O)	—	—	mA	0 < V_{OUT} < 0.3(V_{cc}I/O)
		-17.1(V_{cc}I/O - V_{OUT})	—	—	mA	0.3(V_{cc}I/O) < V_{OUT} < 0.9(V_{cc}I/O)
		—	—	-32(V_{cc}I/O)	—	0.7(V_{cc}I/O)
		16(V_{cc}I/O)	—	See Note 1	mA	0.7(V_{cc}I/O) < V_{OUT} < V_{cc}I/O
	I_{OL}(AC) Switching	+16(V_{cc}I/O)	—	—	mA	V_{cc}I/O > V_{OUT} > 0.6(V_{cc}I/O)
		+26.7(V_{OUT})	—	—	mA	0.6(V_{cc}I/O) > V_{OUT} > 0.1(V_{cc}I/O)
		—	—	+38(V_{cc}I/O)	mA	V_{OUT} = 0.18(V_{cc}I/O)
		—	—	See Note 2	mA	0.18(V_{cc}I/O) > V_{OUT} > 0
	V_{IL}	-0.3	—	0.3(V_{cc}I/O)	V	
	V_{IH}	0.5(V_{cc}I/O)	—	5.5	V	
Capacitance	C_{IN}	—	—	10.5	pF	—
Leakage	Inputs	—	—	± 10	µA	Vcc (max)
	$I/O_{LEAK\ W/O}$ Pull-ups/ downs	—	—	± 10	µA	Vcc (max)
	$I/O_{LEAK\ WITH}$ Pull-ups/ downs	—	—	± 80	µA	Vcc (max)

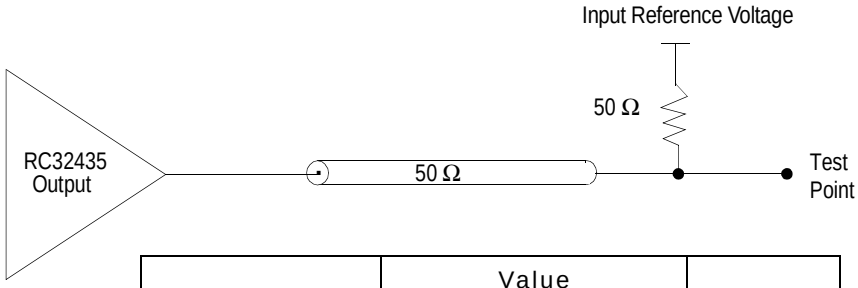
Table 18 DC Electrical Characteristics

Note 1: $I_{OH}(AC)\ max = (98/V_{CC}I/O) * (V_{OUT} - V_{CC}I/O) * (V_{OUT} + 0.4V_{CC}I/O)$

Note 2: $I_{OL}(AC)\ max = (256/V_{CC}I/O) * V_{OUT} * (V_{CC}I/O - V_{OUT})$

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AC Test Conditions



Parameter	Value		Units
	SSTL I/O	Other I/O	
Input pulse levels	0 to 2.5	0 to 3.3	V
Input rise/fall	0.8	1.0	ns
Input reference level	0.5(VccSI/O)	0.5(VccI/O)	V
Output reference levels	1.25	1.5	V
AC test load	35	35	pF

Figure 23 AC Test Conditions

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Absolute Maximum Ratings

Symbol	Parameter	Min[1]	Max[1]	Unit
V_{CC}I/O	I/O supply except for SSTL_2[2]	-0.6	4.0	V
V_{CC}SI/O (DDR)	I/O supply for SSTL_2[2]	-0.6	4.0	V
V_{CC}Core	Core Supply Voltage	-0.6	2.0	V
V_{CC}PLL	PLL supply (digital)	-0.6	2.0	V
V_{CC}APLL	PLL supply (analog)	-0.6	4.0	V
VinI/O	I/O Input Voltage except for SSTL_2	-0.6	V_{cc}I/O+ 0.5	V
VinSI/O	I/O Input Voltage for SSTL_2	-0.6	V_{cc}SI/O+ 0.5	V
T_a Industrial	Ambient Operating Temperature	-40	+85	°C
T_a Commercial	Ambient Operating Temperature	0	+70	°C
T_s	Storage Temperature	-40	+125	°C

Table 19 Absolute Maximum Ratings

1. Functional and tested operating conditions are given in Table 15. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.

2. SSTL_2 I/Os are used to connect to DDR SDRAM.

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Package Pin-out — 256-BGA Signal Pinout for the RC32435

The following table lists the pin numbers, signal names, and number of alternate functions for the RC32435 device. Signal names ending with an "_n" or "n" are active when low.

Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt
A1	RWN		E1	MIIRXD[3]		J1	GPIO[3]	1	N1	PCIAD[29]	
A2	OEN		E2	MIIRXD[2]		J2	JTAG_TCK		N2	PCIAD[28]	
A3	CSN[2]		E3	MIITXD[0]		J3	GPIO[2]	1	N3	PCIAD[30]	
A4	CSN[0]		E4	MIITXD[1]		J4	EJTAG_TMS		N4	PCIAD[18]	
A5	MADDR[10]		E5	V_{cc} I/0		J5	V_{cc} CORE		N5	PCIREQN[1]	
A6	MDATA[6]		E6	V_{cc} I/0		J6	V_{ss}		N6	PCIREQN[2]	
A7	GPIO[7]	1	E7	V_{cc} I/0		J7	V_{ss}		N7	PCIIRDYN	
A8	GPIO[4]	1	E8	V_{cc} CORE		J8	V_{ss}		N8	PCILOCKN	
A9	MADDR[16]		E9	V_{cc} CORE		J9	V_{ss}		N9	PCIPERRN	
A10	MADDR[13]		E10	V_{cc} I/0		J10	V_{ss}		N10	PCIAD[15]	
A11	V_{ss} PLL		E11	V_{cc} DDR		J11	V_{cc} CORE		N11	PCIAD[11]	
A12	JTAG_TDI		E12	V_{cc} DDR		J12	V_{cc} CORE		N12	PCICBEN[0]	
A13	MADDR[9]		E13	DDRDATA[6]		J13	DDRCKN		N13	DDRADDR[5]	
A14	MADDR[7]		E14	DDRDATA[5]		J14	DDRVREF		N14	DDRADDR[4]	
A15	MADDR[5]		E15	DDRADDR[13]		J15	DDRCKP		N15	DDRADDR[3]	
A16	MADDR[2]		E16	DDRDATA[4]		J16	DDRDQS[0]		N16	DDRBA[0]	
B1	BOEN		F1	MIITXD[2]		K1	JTG_TDO		P1	PCIAD[27]	
B2	RSTN		F2	MIIRXCLK		K2	SCK		P2	PCIAD[26]	
B3	CSN[3]		F3	MIITXD[3]		K3	Reserved		P3	GPIO[10]	1
B4	CSN[1]		F4	MIITXENP		K4	SDO		P4	PCIAD[20]	
B5	MADDR[11]		F5	V_{cc} I/0		K5	V_{cc} I/0		P5	PCIREQN[3]	
B6	MDATA[1]		F6	V_{ss}		K6	V_{cc} I/0		P6	PCIREQN[0]	
B7	MDATA[4]		F7	V_{ss}		K7	V_{ss}		P7	PCIFRAMEN	
B8	GPIO[5]	1	F8	V_{ss}		K8	V_{ss}		P8	PCISTOPN	
B9	MADDR[17]		F9	V_{cc} CORE		K9	V_{ss}		P9	PCISERRN	
B10	MADDR[12]		F10	V_{ss}		K10	V_{ss}		P10	PCIAD[14]	
B11	V_{cc} PLL		F11	V_{ss}		K11	V_{ss}		P11	PCIAD[10]	
B12	V_{ss} APLL		F12	V_{cc} DDR		K12	V_{cc} DDR		P12	PCIAD[7]	
B13	MADDR[8]		F13	DDRDATA[9]		K13	DDRCKE		P13	PCIAD[4]	
B14	MADDR[6]		F14	DDRDATA[8]		K14	DDRADDR[11]		P14	DDRADDR[0]	
B15	MADDR[3]		F15	DDRDM[0]		K15	DDRADDR[10]		P15	DDRADDR[2]	
B16	MADDR[1]		F16	DDRDATA[7]		K16	DDRADDR[12]		P16	DDRCSN	
C1	EXTCLK		G1	MIIRXDV		L1	SDA		R1	PCIAD[25]	

Table 20 RC32435 Pinout (Part 1 of 2)

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Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt
C2	BDIRN		G2	MIITXER		L2	SCL		R2	PCICBEN[3]	
C3	COLDRSTN		G3	MIIRXER		L3	GPIO[8]	1	R3	PCIAD[23]	
C4	WEN		G4	MIITXCLK		L4	SDI		R4	PCIAD[21]	
C5	MDATA[3]		G5	V_{CC} I/0		L5	V_{CC} I/0		R5	PCIAD[17]	
C6	MDATA[5]		G6	V_{SS}		L6	V_{SS}		R6	PCIRSTN	
C7	GPIO[6]	1	G7	V_{SS}		L7	V_{SS}		R7	PCICBEN[2]	
C8	MADDR[21]		G8	V_{SS}		L8	V_{CC} CORE		R8	PCITRDYN	
C9	MADDR[18]		G9	V_{SS}		L9	V_{SS}		R9	PCICBEN[1]	
C10	MADDR[14]		G10	V_{SS}		L10	V_{SS}		R10	PCIAD[12]	
C11	JTAG_TMS		G11	V_{SS}		L11	V_{SS}		R11	PCIAD[8]	
C12	V_{CC} APLL		G12	V_{CC} DDR		L12	V_{CC} DDR		R12	PCIAD[5]	
C13	CLK		G13	DDRDM[1]		L13	DDRADDR[9]		R13	PCIAD[3]	
C14	MADDR[4]		G14	DDRDQS[1]		L14	DDRWEN		R14	PCIAD[0]	
C15	MADDR[0]		G15	DDRDATA[10]		L15	DDRCASN		R15	PCIGNTN[2]	
C16	DDRDATA[0]		G16	DDRDATA[11]		L16	DDRADDR[8]		R16	DDRADDR[1]	
D1	MIIRXD[0]		H1	MIIMDIO		M1	GPIO[12]	1	T1	PCIAD[24]	
D2	MIICL		H2	MIIMDC		M2	PCIAD[31]		T2	GPIO[13]	1
D3	MIICRS		H3	GPIO[0]	1	M3	GPIO[11]	1	T3	PCIAD[22]	
D4	MIIRXD[1]		H4	GPIO[1]	1	M4	GPIO[9]	1	T4	PCIAD[19]	
D5	MDATA[7]		H5	V_{CC} CORE		M5	V_{CC} I/0		T5	PCIAD[16]	
D6	MDATA[2]		H6	V_{CC} CORE		M6	V_{CC} I/0		T6	PCICLK	
D7	MDATA[0]		H7	V_{SS}		M7	V_{CC} I/0		T7	PCIGNTN[0]	
D8	MADDR[20]		H8	V_{SS}		M8	V_{CC} CORE		T8	PCIDEVSELN	
D9	MADDR[19]		H9	V_{SS}		M9	V_{CC} CORE		T9	PCIPAR	
D10	MADDR[15]		H10	V_{SS}		M10	V_{CC} I/0		T10	PCIAD[13]	
D11	EXTBCV		H11	V_{SS}		M11	V_{CC} DDR		T11	PCIAD[9]	
D12	JTAG_TRSTN		H12	V_{CC} CORE		M12	V_{CC} DDR		T12	PCIAD[6]	
D13	WAITACKN		H13	DDRDATA[15]		M13	DDRRASN		T13	PCIAD[2]	
D14	DDRDATA[2]		H14	DDRDATA[14]		M14	DDRBA[1]		T14	PCIAD[1]	
D15	DDRDATA[3]		H15	DDRDATA[12]		M15	DDRADDR[6]		T15	PCIGNTN[1]	
D16	DDRDATA[1]		H16	DDRDATA[13]		M16	DDRADDR[7]		T16	PCIGNTN[3]	

Table 20 RC32435 Pinout (Part 2 of 2)

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RC32435 Alternate Signal Functions

Pin	GPIO	Alternate	Pin	GPIO	Alternate
A7	GPIO[7]	MADDR[25]	J3	GPIO[2]	U0RTSN
A8	GPIO[4]	MADDR[22]	L3	GPIO[8]	CPU
B8	GPIO[5]	MADDR[23]	M1	GPIO[12]	PCIGNTN[5]
C7	GPIO[6]	MADDR[24]	M3	GPIO[11]	PCIREQN[5]
H3	GPIO[0]	U0SOUT	M4	GPIO[9]	PCIREQN[4]
H4	GPIO[1]	U0SINP	P3	GPIO[10]	PCIGNTN[4]
J1	GPIO[3]	U0CTSN	T2	GPIO[13]	PCIMUINTN

Table 21 RC32435 Alternate Signal Functions

RC32435 Power Pins

V_{cc} I/O	V_{cc} DDR	V_{cc} Core	V_{cc} PLL	V_{cc} APLL
E5	E11	E8	B11	C12
E6	E12	E9		
E7	F12	F9		
E10	G12	H5		
F5	K12	H6		
G5	L12	H12		
K5	M11	J5		
K6	M12	J11		
L5		J12		
M5		L8		
M6		M8		
M7		M9		
M10				

Table 22 RC32435 Power Pins

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RC32435 Ground Pins

V_{ss}	V_{ss}	V_{ss} PLL
F6	J6	A11, B12
F7	J7	
F8	J8	
F10	J9	
F11	J10	
G6	K7	
G7	K8	
G8	K9	
G9	K10	
G10	K11	
G11	L6	
H7	L7	
H8	L9	
H9	L10	
H10	L11	
H11		

Table 23 RC32435 Ground Pins

RC32435 Signals Listed Alphabetically

The following table lists the RC32435 pins in alphabetical order.

Signal Name	I/O Type	Location	Signal Category
BDIRN	O	C2	Memory and Peripheral Bus
BOEN	O	B1	
CLK	I	C13	System
COLDRSTN	I	C3	
CSN[0]	O	A4	Memory and Peripheral Bus
CSN[1]	O	B4	
CSN[2]	O	A3	
CSN[3]	O	B3	

Table 24 RC32435 Alphabetical Signal List (Part 1 of 7)

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Signal Name	I/O Type	Location	Signal Category
DDRADDR[0]	O	P14	DDR Bus
DDRADDR[1]	O	R16	
DDRADDR[2]	O	P15	
DDRADDR[3]	O	N15	
DDRADDR[4]	O	N14	
DDRADDR[5]	O	N13	
DDRADDR[6]	O	M15	
DDRADDR[7]	O	M16	
DDRADDR[8]	O	L16	
DDRADDR[9]	O	L13	
DDRADDR[10]	O	K15	
DDRADDR[11]	O	K14	
DDRADDR[12]	O	K16	
DDRADDR[13]	O	E15	
DDRBA[0]	O	N16	
DDRBA[1]	O	M14	
DDRCASN	O	L15	
DDRCKE	O	K13	
DDRCKN	O	J13	
DDRCKP	O	J15	
DDRCSN	O	P16	
DDRDATA[0]	I/O	C16	
DDRDATA[1]	I/O	D16	
DDRDATA[2]	I/O	D14	
DDRDATA[3]	I/O	D15	
DDRDATA[4]	I/O	E16	
DDRDATA[5]	I/O	E14	
DDRDATA[6]	I/O	E13	
DDRDATA[7]	I/O	F16	
DDRDATA[8]	I/O	F14	
DDRDATA[9]	I/O	F13	
DDRDATA[10]	I/O	G15	
DDRDATA[11]	I/O	G16	
DDRDATA[12]	I/O	H15	
DDRDATA[13]	I/O	H16	
DDRDATA[14]	I/O	H14	

Table 24 RC32435 Alphabetical Signal List (Part 2 of 7)

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Signal Name	I/O Type	Location	Signal Category
DDRDATA[15]	I/O	H13	DDR Bus
DDRDM[0]	O	F15	
DDRDM[1]	O	G13	
DDRDQS[0]	I/O	J16	
DDRDQS[1]	I/O	G14	
DDRRASN	O	M13	
DDRVREF	I	J14	
DDRWEN	O	L14	
EJTAG_TMS	I	J4	JTAG / EJTAG
EXTBCV	I	D11	System
EXTCLK	O	C1	
GPIO[0]	I/O	H3	General Purpose Input/Output
GPIO[1]	I/O	H4	
GPIO[2]	I/O	J3	
GPIO[3]	I/O	J1	
GPIO[4]	I/O	A8	
GPIO[5]	I/O	B8	
GPIO[6]	I/O	C7	
GPIO[7]	I/O	A7	
GPIO[8]	I/O	L3	
GPIO[9]	I/O	M4	
GPIO[10]	I/O	P3	
GPIO[11]	I/O	M3	
GPIO[12]	I/O	M1	
GPIO[13]	I/O	T2	
JTAG_TCK	I	J2	JTAG / EJTAG
JTAG_TDI	I	A12	
JTAG_TDO	O	K1	
JTAG_TMS	I	C11	
JTAG_TRSTN	I	D12	

Table 24 RC32435 Alphabetical Signal List (Part 3 of 7)

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Signal Name	I/O Type	Location	Signal Category
MADDR[0]	O	C15	Memory and Peripheral Bus
MADDR[1]	O	B16	
MADDR[2]	O	A16	
MADDR[3]	O	B15	
MADDR[4]	O	C14	
MADDR[5]	O	A15	
MADDR[6]	O	B14	
MADDR[7]	O	A14	
MADDR[8]	O	B13	
MADDR[9]	O	A13	
MADDR[10]	O	A5	
MADDR[11]	O	B5	
MADDR[12]	O	B10	
MADDR[13]	O	A10	
MADDR[14]	O	C10	
MADDR[15]	O	D10	
MADDR[16]	O	A9	
MADDR[17]	O	B9	
MADDR[18]	O	C9	
MADDR[19]	O	D9	
MADDR[20]	O	D8	
MADDR[21]	O	C8	
MDATA[0]	I/O	D7	
MDATA[1]	I/O	B6	
MDATA[2]	I/O	D6	
MDATA[3]	I/O	C5	
MDATA[4]	I/O	B7	
MDATA[5]	I/O	C6	
MDATA[6]	I/O	A6	
MDATA[7]	I/O	D5	

Table 24 RC32435 Alphabetical Signal List (Part 4 of 7)

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Signal Name	I/O Type	Location	Signal Category
MIICL	I	D2	Ethernet Interface
MIICRS	I	D3	
MIIMDC	O	H2	
MIIMDIO	I/O	H1	
MIIRXCLK	I	F2	
MIIRXD[0]	I	D1	
MIIRXD[1]	I	D4	
MIIRXD[2]	I	E2	
MIIRXD[3]	I	E1	
MIIRXDV	I	G1	
MIIRXER	I	G3	
MIITXCLK	I	G4	
MIITXD[0]	O	E3	
MIITXD[1]	O	E4	
MIITXD[2]	O	F1	
MIITXD[3]	O	F3	
MIITXENP	O	F4	
MIITXER	O	G2	
OEN	O	A2	Memory and Peripheral Bus
PCIAD[0]	I/O	R14	PCI Bus Interface
PCIAD[1]	I/O	T14	
PCIAD[2]	I/O	T13	
PCIAD[3]	I/O	R13	
PCIAD[4]	I/O	P13	
PCIAD[5]	I/O	R12	
PCIAD[6]	I/O	T12	
PCIAD[7]	I/O	P12	
PCIAD[8]	I/O	R11	
PCIAD[9]	I/O	T11	
PCIAD[10]	I/O	P11	
PCIAD[11]	I/O	N11	
PCIAD[12]	I/O	R10	
PCIAD[13]	I/O	T10	
PCIAD[14]	I/O	P10	
PCIAD[15]	I/O	N10	
PCIAD[16]	I/O	T5	

Table 24 RC32435 Alphabetical Signal List (Part 5 of 7)

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Signal Name	I/O Type	Location	Signal Category
PCIAD[17]	I/O	R5	PCI Bus Interface
PCIAD[18]	I/O	N4	
PCIAD[19]	I/O	T4	
PCIAD[20]	I/O	P4	
PCIAD[21]	I/O	R4	
PCIAD[22]	I/O	T3	
PCIAD[23]	I/O	R3	
PCIAD[24]	I/O	T1	
PCIAD[25]	I/O	R1	
PCIAD[26]	I/O	P2	
PCIAD[27]	I/O	P1	
PCIAD[28]	I/O	N2	
PCIAD[29]	I/O	N1	
PCIAD[30]	I/O	N3	
PCIAD[31]	I/O	M2	
PCIBEN[0]	I/O	N12	
PCIBEN[1]	I/O	R9	
PCIBEN[2]	I/O	R7	
PCIBEN[3]	I/O	R2	
PCICLK	I	T6	
PCIDEVSELN	I/O	T8	
PCIFRAMEN	I/O	P7	
PCIGNTN[0]	I/O	T7	
PCIGNTN[1]	I/O	T15	
PCIGNTN[2]	I/O	R15	
PCIGNTN[3]	I/O	T16	
PCIIRDYN	I/O	N7	
PCILOCKN	I/O	N8	
PCIPAR	I/O	T9	
PCIPERRN	I/O	N9	
PCIREQN[0]	I/O	P6	
PCIREQN[1]	I/O	N5	
PCIREQN[2]	I/O	N6	
PCIREQN[3]	I/O	P5	
PCIRSTN	I/O	R6	
PCISERRN	I/O	P9	

Table 24 RC32435 Alphabetical Signal List (Part 6 of 7)

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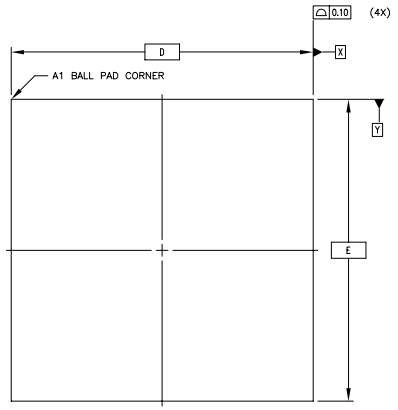
Signal Name	I/O Type	Location	Signal Category
PCISTOPN	I/O	P8	PCI Bus Interface
PCITRDYN	I/O	R8	
RSTN	I/O	B2	System
RWN	O	A1	Memory and Peripheral Bus
SCK	I/O	K2	Serial Peripheral Interface
SCL	I/O	L2	I^2C
SDA	I/O	L1	
SDI	I/O	L4	Serial Peripheral Interface
SDO	I/O	K4	
Vcc APLL		C12	Power
Vcc Core		E8, E9, F9, H5, H6, H12, J5, J11, J12, L8, M8, M9	
Vcc DDR		E11, E12, F12, G12, K12, L12, M11, M12	
Vcc I/O		E5, E6, E7, E10, F5, G5, K5, K6, L5, M5, M6, M7, M10	
Vcc PLL		B11	
Vss		F6, F7, F8, F10, F11, G6, G7, G8, G9, G10, G11, H7, H8, H9, H10, H11, J6, J7, J8, J9, J10, K7, K8, K9, K10, K11, L6, L7, L9, L10, L11	Ground
Vss APLL		B12	
Vss PLL		A11	
WAITACKN	I	D13	Memory and Peripheral Bus
WEN	O	C4	
Reserved		K3, L1, L2	

Table 24 RC32435 Alphabetical Signal List (Part 7 of 7)

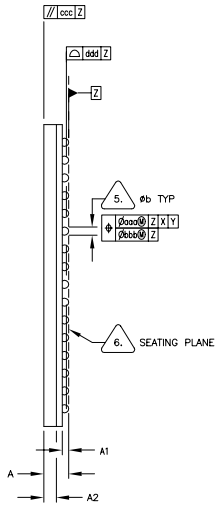
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RC32435 Package Drawing — 256-pin CABGA

REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
	00	INITIAL RELEASE	06/09/00	D.G
	01	JEDEC VARIATION MODIFICATION	07/11/00	D.G
	02	UPDATE MAX. THICKNESS A	10/02/02	



TOP VIEW



SIDE VIEW

SYMBOL	JEDEC VARIATION AAF-1 MIN	NOM	MAX	NOTE
A	1.30	1.40	1.70	
A1	.31	.36	.41	
A2	.65	.70	.75	
D		17.00 BSC		
D1		15.00 BSC		
E		17.00 BSC		
E1		15.00 BSC		
MD		16		3
ME		16		3
N		256		4
e		1.00 BSC		
b	.41	.46	.51	5
aaa	–	–	.15	
bbb	–	–	.08	
ccc	–	–	.10	
ddd	–	–	.12	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN MILLIMETERS
DECIMAL: XX ±0.10, XXX ±0.05, XXXX ±0.08
ANGULAR: ±1°

APPROVALS	DATE
DRAWN .GX	06/09/00
CHECKED	

Integrated Device Technology, Inc.
2975 Stender Way, Santa Clara, CA 95054
(408) 727-6116 FAX (408) 492-8074

BC256 PACKAGE OUTLINE
17.0 X 17.0 mm BODY CABGA

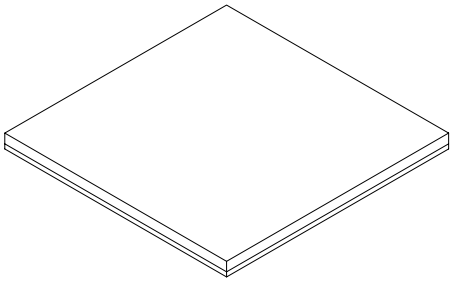
DRAWING No.	SIZE	SCALE	REV
PSC-4093	C	N/A	02

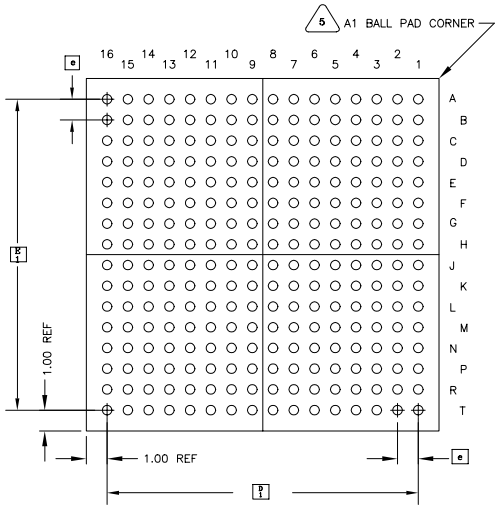
DO NOT SCALE DRAWING — SHEET 1 OF 2

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RC32435 Package Drawing — Page Two

REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
	00	INITIAL RELEASE	06/09/00	D.G
	01	JEDEC VARIATION MODIFICATION	07/11/00	D.G
	02	UPDATE MAX. THICKNESS A	10/02/02	





BOTTOM VIEW
256 SOLDER BALLS

NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M–1994.
2. "e" REPRESENTS THE BASIC SOLDER BALL GRID PITCH.
3. "MD" IS THE MAXIMUM SOLDER BALL MATRIX SIZE IN THE "D" DIRECTION.
   "ME" IS THE MAXIMUM SOLDER BALL MATRIX SIZE IN THE "E" DIRECTION.
4. "N" IS THE MAXIMUM ALLOWABLE NUMBER OF SOLDER BALLS.
5. DIMENSION "b" IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM Z.
6. PRIMARY DATUM Z AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
7. "A1" ID CORNER MUST BE IDENTIFIED. IDENTIFICATION MAY BE BY MEANS OF CHAMFER, METALLIZED OR INK MARK, INDENTATION OR OTHER FEATURE OF THE PACKAGE BODY.
8. ALL DIMENSIONS ARE IN MILLIMETERS.
9. THIS DRAWING CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MO–192 VARIATION AAF–1
   EXCEPTIONS:
   b MIN=0.41 NOM=0.46 MAX=0.51

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN MILLIMETERS
DECIMAL ANGULAR
X.X ±0.10 ±1°
X.XX ±0.05
X.XXX ±0.00

APPROVALS	DATE
DRAWN BX	06/09/00
CHECKED	

Integrated Device Technology, Inc.
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(408) 727–6116 FAX (408) 492–8074

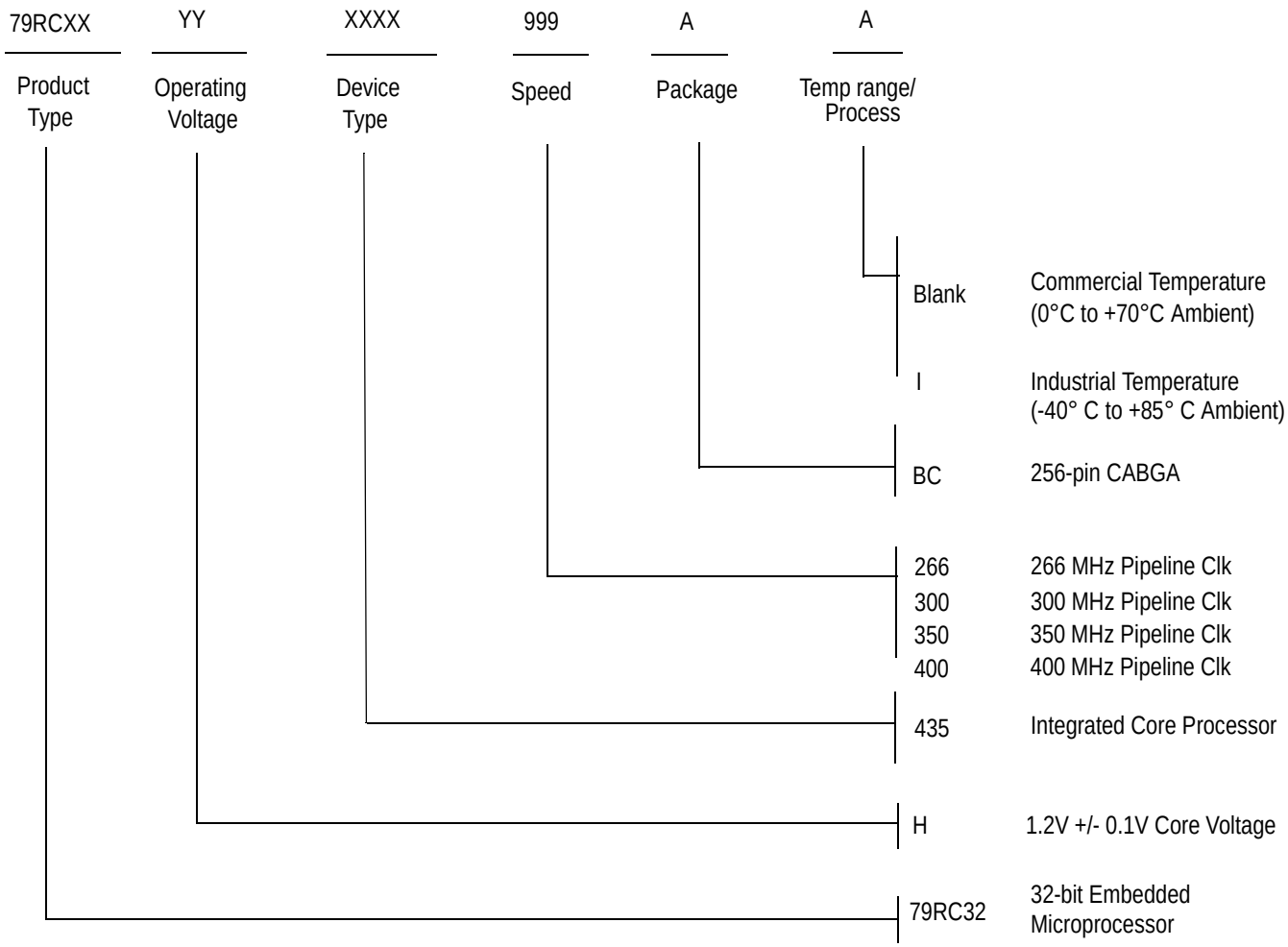
BC256 PACKAGE OUTLINE
17.0 X 17.0 mm BODY CABGA

DRAWING No.	SIZE	SCALE	REV
PSC–4093	C	N/A	02

DO NOT SCALE DRAWING — SHEET 2 OF 2

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Ordering Information



Valid Combinations

79RC32H435 - 266BC, 300BC, 350BC, 400BC	256-pin CABGA package, Commercial Temperature
79RC32H435 - 266BCI, 300BCI, 350BCI	256-pin CABGA package, Industrial Temperature

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(Rev.1.0 Mar 2020)

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