Frequency Generator/Jitter Attenuation Device For Wireless Infrastructure Applications

813076

OBSOLETE

DATASHEET

General Description

The ICS813076I is a member of the HiperClocks family of high performance clock solutions from IDT. The ICS813076I a PLL based synchronous clock solution that is optimized for wireless infrastructure equipment where frequency translation and jitter attenuation is needed.

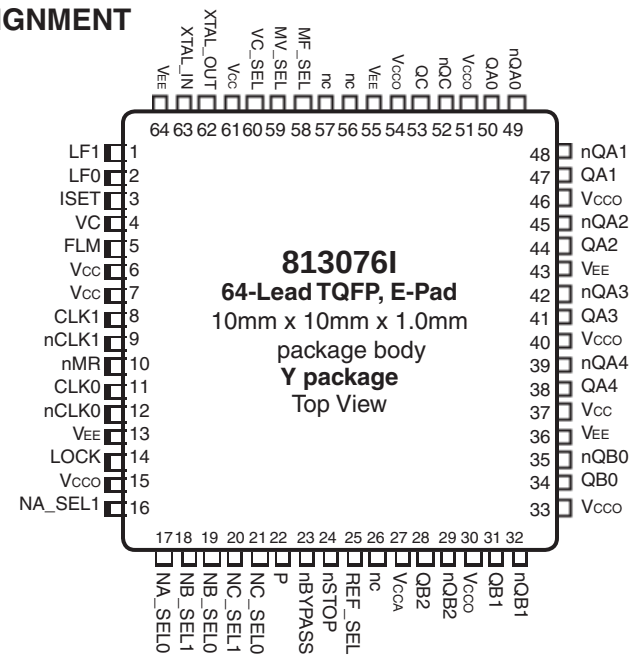
The device contains two internal PLL stages that are cascaded in series. The first PLL stage attenuates the reference clock jitter by using an internal or external VCXO circuit. The internal VCXO requires the connection of an external inexpensive pullable crystal (XTAL) to the ICS813076I. This first PLL stage (VCXO PLL) uses external passive loop filter components which are used to optimize the PLL loop bandwidth and damping characteristics for the given application. The output of the first stage VCXO PLL is a stable and jitter-tolerant reference input for the second PLL stage of 30.72MHz. The second PLL stage provides frequency translation by multiplying the output of the first stage up to 614.4MHz. The low phase noise characteristics of the clock signal is maintained by the internal FemtoClock™ PLL, which requires no external components or configuration. Two independently configurable frequency dividers translate the 491.52MHz or 614.4MHz internal VCO signal to the desired output frequencies. All frequency translation ratios are set by device configuration pins. Alternative to the clock frequency multiplication functionality, the ICS813076I can work as a VCXO. Enabling the VCXO mode allows the output frequency of 614.4MHz/N or 491.52MHz/N to be pulled by the input voltage of the VC pin.

- Supported input reference clock frequencies:
  15.36MHz,
  30.72MHz
  61.44MHz
- Supported output clock frequencies:
  30.72MHz
  122.88MHz
  153.6MHz
  491.52MHz
  614.4MHz

Features

- Two operation modes: input frequency multiplier and VCXO
- Nine differential LVPECL outputs, organized in three independent output banks
- Two selectable differential input clocks can accept the following differential input levels: LVDS, LVPECL, LVHSTL, SSTL, HCSL
- Maximum output frequency: 614.4MHz
- FemtoClock VCO frequency: 491.52MHz or 614.4MHz (typical)
- Frequency generation optimized for wireless infrastructure equipment
- Attenuates the phase jitter of the input clock signal by using a low-cost pullable fundamental mode crystal (XTAL)
- Multiplies the input clock frequency by 1, 4, 5, 16 or 20
- LVCMOS/LVTTL levels for all input/output controls
- PLL fast-lock control
- VCXO PLL bandwidth can be optimized for jitter attenuation and reference frequency tracking using external loop filter components
- Absolute pull range: ±50ppm
- RMS phase jitter (12kHz – 20MHz): 0.97ps (typical)
- Full 3.3V supply
- -40°C to 85°C ambient operating temperature
- Available in lead-free (RoHS 6) package
- For functional replacement device use 8T49N286-dddNLGI

Pin Assignment



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Block Diagram

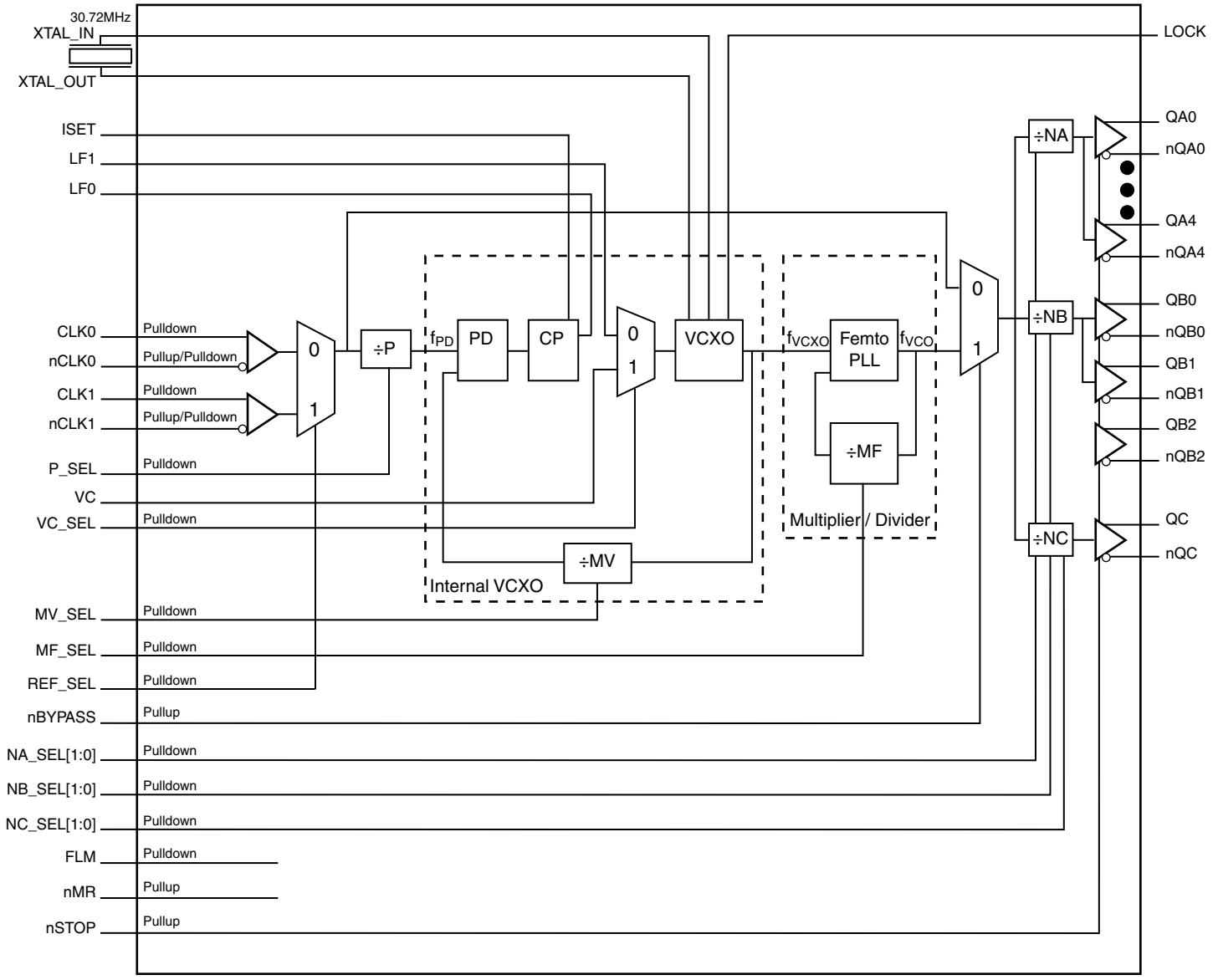


TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1	LF1	Analog Input		Input from external loop filter. VCXO control voltage input.
2	LF0	Analog Output		Output to external loop filter. Charge pump output.
3	ISET	Analog		Charge pump current setting pin.
4	VC	Analog		Control voltage to the VCXO.
5	FLM	Input	Pulldown	VCXO-PLL fast lock mode. LVCMOS/LVTTL interface levels. See Table 3H.
6, 7, 37, 61	V_{CC}	Power		Core power supply pins.
8	CLK1	Input	Pulldown	Non-inverting differential reference clock input.
9	nCLK1	Input	Pullup/ Pulldown	Inverting differential clock input. $V_{CC}/2$ bias voltage when left floating.
10	nMR	Input	Pullup	Master reset pin. LVCMOS/LVTTL interface levels. See Table 3I.
11	CLK0	Input	Pulldown	Non-inverting differential reference clock input.
12	nCLK0	Input	Pullup/ Pulldown	Inverting differential clock input. $V_{CC}/2$ bias voltage when left floating.
13, 36, 43, 55, 64	V_{EE}	Power		Negative supply pins.
14	LOCK	Output		VCXO-PLL lock state. In VCXO-PLL mode (VC_SEL = 0), logic HIGH at the LOCK output indicates frequency lock of the VCXO-PLL. In VCXO-PLL mode (VC_SEL = 1), the state of LOCK is always 0. LVCMOS/LVTTL interface levels.
15, 30, 33, 40, 46, 51, 54	V_{CCO}	Power		Output supply pins.
16, 17	NA_SEL1, NA_SEL0	Input	Pulldown	FemtoPLL output-divider for QA outputs. LVCMOS/LVTTL interface levels. See Table 3F.
18, 19	NB_SEL1, NB_SEL0	Input	Pulldown	FemtoPLL output-divider for QB outputs. LVCMOS/LVTTL interface levels. See Table 3F.
20, 21	NC_SEL1, NC_SEL0	Input	Pulldown	FemtoPLL output-divider for QC outputs. LVCMOS/LVTTL interface levels. See Table 3F.
22	P_SEL	Input	Pulldown	VCXO pre-divider selection. LVCMOS/LVTTL interface levels. See Table 3B.
23	nBYPASS	Input	Pullup	PLL mode selection. LVCMOS/LVTTL interface levels. See Table 3G.
24	nSTOP	Input	Pullup	Ouput clock stop pin. LVCMOS/LVTTL interface levels. See Table 3J.
25	REF_SEL	Input	Pulldown	Selects the input reference clock. LVCMOS/LVTTL interface levels. See Table 3E.
26, 56, 57	nc	Unused		No connect.
27	V_{CCA}	Power		Analog supply pin.
28, 29 31, 32 34, 35	QB2, nQB2 QB1, nQB1 QB0, nQB0	Output		Differential Bank B clock outputs. LVPECL interface levels.
38, 39 41, 42 44, 45 47, 48 49, 50	QA4, nQA4 QA3, nQA3 QA2, nQA2 QA1, nQA1 nQA0, QA0	Output		Differential Bank A clock outputs. LVPECL interface levels.
52, 53	nQC, QC	Output		Differential Bank C clock outputs. LVPECL interface levels.
58	MF_SEL	Input	Pulldown	Femto-PLL feedback divider selection. LVCMOS/LVTTL interface levels. See Table 3D.
59	MV_SEL	Input	Pulldown	VCXO M-divider selection. LVCMOS/LVTTL interface levels. See Table 3C.
60	VC_SEL	Input	Pulldown	Controls the mode of operation. LVCMOS/LVTTL interface levels. See Table 3K.
62, 63	XTAL_OUT, XTAL_IN	Input		VCXO crystal oscillator interface. XTAL_IN is the input. XTAL_OUT is the output.

NOTE: *Pulldown and Pullup* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ

DEVICE CONFIGURATION

The ICS813076I is a two stage device, a VCXO PLL stage followed by a low phase noise FemtoClock PLL multiplier stage. The VCXO PLL stage uses a pullable crystal to lock to the reference clock. The low phase noise FemtoClock multiplies the VCXO PLL output clock up to 614.4MHz and three independent output dividers scale the frequency down to the desired output frequencies. With a given input and VCXO frequency, the output frequency is a function of the P, MV, MF and NA, NB, NC dividers, and can be set by pulling configuration pins high or low. See "ICS813076I Examples Frequency Configuration (f_{VCXO} = 30.72MHz)" for typical device configurations. Note that for correct operation, the input frequency times the MV-divider must be 30.72MHz ± 50ppm. The ICS813076I supports up to three output frequencies f_{OUT} independently.

TABLE 3A. FREQUENCY CONFIGURATION EXAMPLES TABLE (f_{VCXO} = 30.72MHz)

f_{IN} (MHz)	f_{OUT} (MHz)	Ratio	Configuration			
			P	MV	MF	NA, NB, NC
30.72	30.72	1	1	1	20	20
30.72	122.8	4	1	1	20	5
30.72	153.6	5	1	1	20	4
30.72	614.4	20	1	1	20	1
30.72	24.576	4/5	1	1	16	20
30.72	98.304	16/5	1	1	16	5
30.72	122.8	4	1	1	16	4
30.72	491.52	16	1	1	16	1

NOTE: The example frequency configuration table is intended to show the most common frequency translations. The following example will illustrate the configuration process.

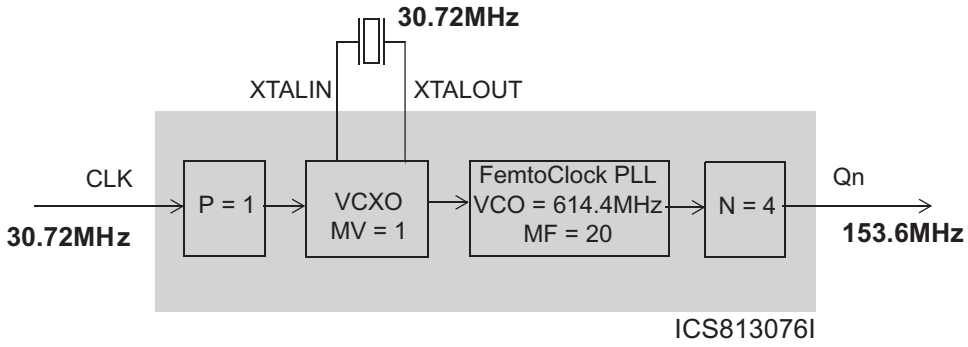


FIGURE 1. APPLICATION EXAMPLE (153.6MHz CLOCK GENERATION AND JITTER ATTENUATION)

The VCXO pre-divider (P) down-scales the input reference frequency f_{REF} and enables the use of the ICS813076I at a variety of input frequencies. P_SEL and MV_SEL must be set to match the VCXO frequency: $f_{REF} \div P = f_{VCXO} \div MV$. For instance, at the nominal VCXO frequency of 30.72MHz and if MV equals two, the input frequency must be an integer multiple of 15.36MHz.

TABLE 3B. VCXO PRE-DIVIDER (P) CONFIGURATION TABLE

Input P_SEL	Pre-Divider Function	Operation
0	÷1	$f_{PD} = f_{REF} \div 1$
1	÷2	$f_{PD} = f_{REF} \div 2$

TABLE 3C. VCXO MULTIPLIER (MV-DIVIDER) CONFIGURATION TABLE

Input MV_SEL	Multiplier MV Function	Operation
0	1	$f_{VCXO} = f_{PD}$
1	2	$f_{VCXO} = f_{PD} * 2$

TABLE 3D. FEMTOCLOCK FEEDBACK DIVIDER (MF) CONFIGURATION TABLE

Input MF_SEL	Multiplier MF Function	Operation
0	20	$f_{VCO} = f_{VCXO} * 20$
1	16	$f_{VCO} = f_{VCXO} * 16$

TABLE 3E. INPUT REFERENCE CLOCK MULTIPLEXER CONFIGURATION TABLE

Input REF_SEL	Operation
0 (default)	Selects CLK0, nCLK0 as PLL reference signal
1	Selects CLK1, nCLK1 as PLL reference signal

TABLE 3F. PLL OUTPUT-DIVIDER (NA, NB, NC) CONFIGURATION TABLE

Inputs		Output Dividers NA, NB, NC	Operation
Nx_SEL1	Nx_SEL0		
0	0	÷1	$f_{OUT} = f_{VCO}$
0	1	÷4	$f_{OUT} = f_{VCO} \div 4$
1	0	÷5	$f_{OUT} = f_{VCO} \div 5$
1	1	÷20	$f_{OUT} = f_{VCO} \div 20$

The FemtoClock PLL stage multiplies the VCXO frequency (30.72MHz) to 491.52MHz or 614.4MHz. The output frequency equals: $[(f_{REF} \div P) * MV * MF] \div N$. The NA, NB and NC dividers operate independently.

TABLE 3G. PLL BYPASS CONFIGURATION TABLE

Input nBYPASS	Operation
0	$f_{OUT} = f_{REF} \div N$ VCXO and PLL bypassed, no jitter attenuation and frequency multiplication. AC specifications do not apply.
1 (default)	$((f_{REF} \div P) * MV * MF) \div N$ VCXO and PLL operation, jitter attenuation and frequency multiplication enabled.

The nBYPASS control should be set to logic HIGH for normal operation. nBYPASS = 0 enables the PLL bypass mode for factory test.

Table 3H. Fast Lock Mode Configuration Table

Input	
FLM	Operation
0 (default)	Normal operation.
1	Fast PLL lock operation. Use this mode only during start-up to decrease PLL lock time.

Table 3I. Reset and Output Configuration Table

Input	
nMR	Operation
0	The Femto-PLL is reset.
1 (default)	Normal operation and outputs are enabled.

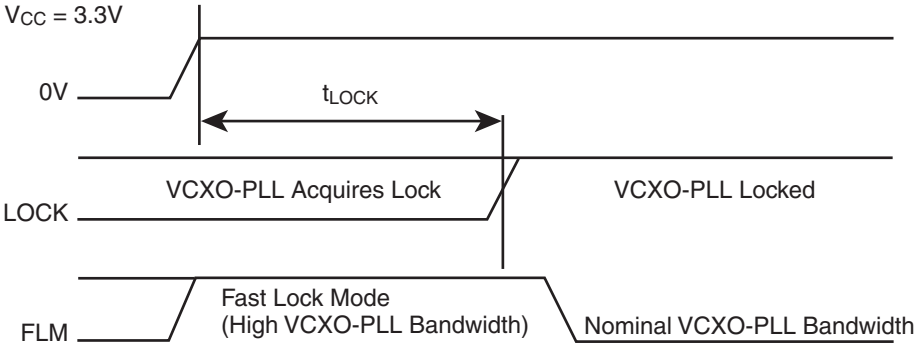


Figure 2. Recommended Start-up Timing Diagram

Table 3J. Reset and Output Configuration Table

Input	
nSTOP	Operation
0	QA[4:0], QB[2:0] and QC outputs are stopped in logic LOW state. nQA[4:0], nQB[2:0] and nQC outputs are stopped in logic HIGH state (QX = LOW, nQX = HIGH). The assertion of nSTOP is asynchronous to the internal clock signal and may cause an output runt pulse.
1 (default)	Normal operation and outputs enabled.

Table 3K. VC_SEL Configuration Table

Input VC_SEL	Mode of Operation	VC Function	CLKx Input Function	LF0, LF1, ISET Function	Output Frequency
0 (default)	Frequency multiplier: the reference clock signal is jitter attenuated and frequency-multiplied	VC input has no function	Enabled, the device locks to CLK0 or CLK1	Enabled	$f_{OUT} = ((f_{REF} / P)*MV*MF)/N$ f_{XTAL} = 30.72MHz The PLL locks to the selected CLKx input
1	VCXO: the output frequency is a function of an input voltage. The device can be used as a integrated oscillator in an external PLL	VC controls the VCXO frequency directly f_{VCXO} = 30.72MHz±50ppm	Disabled	Disabled	f_{OUT} = (30.72MHz ± 50ppm)*MF/N f_{OUT} is pulled by the control voltage on the VC pin

Absolute Maximum Ratings

Supply Voltage, V_{CC}	4.6V
Inputs, V_I	-0.5V to V_{CC} + 0.5V
Outputs, I_O (LVPECL)	
Continuous Current	50mA
Surge Current	100mA
Package Thermal Impedance, θ_{JA}	31.8°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Table 4A. Power Supply DC Characteristics, $V_{CC} = V_{CCO} = 3.3V \pm 5\%$, $V_{EE} = 0V$, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Core Supply Voltage		3.135	3.3	3.465	V
V_{CCA}	Analog Supply Voltage		V_{CC} – 0.09	3.3	V_{CC}	V
V_{CO}	Output Supply Voltage		3.135	3.3	3.465	V
I_{EE}	Power Supply Current				250	mA
I_{CCA}	Analog Supply Current				17	mA

Table 4B. LVCMOS/LVTTL DC Characteristics, $V_{CC} = V_{CCO} = 3.3V \pm 5\%$, $V_{EE} = 0V$, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			2		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage			-0.3		0.8	V
I_{IH}	Input High Current	NA_SEL[0:1], NB_SEL[0:1], NC_SEL[0:1], MF_SEL, FLM, P_SEL, MV_SEL, REF_SEL, VC_SEL	$V_{CC} = V_{IN} = 3.465V$			150	µA
		nMR, nSTOP, nBYPASS	$V_{CC} = V_{IN} = 3.465V$			5	µA
I_{IL}	Input Low Current	NA_SEL[0:1], NB_SEL[0:1], NC_SEL[0:1], MF_SEL, FLM, P_SEL, MV_SEL, REF_SEL, VC_SEL	$V_{CC} = 3.465V$, $V_{IN} = 0V$	-5			µA
		nMR, nSTOP, nBYPASS	$V_{CC} = 3.465V$, $V_{IN} = 0V$	-150			µA

TABLE 4C. DIFFERENTIAL DC CHARACTERISTICS, V_{CC} = V_{CCO} = 3.3V±5%, V_{EE} = 0V, T_A = -40°C TO 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	CLK0, CLK1 nCLK0, nCLK1	V_{IN} = V_{CC} = 3.465V			150	µA
I_{IL}	Input Low Current	CLK0, CLK1	V_{IN} = 0V, V_{CC} = 3.465V	-5			µA
		nCLK0, nCLK1	V_{IN} = 0V, V_{CC} = 3.465V	-150			µA
V_C	VCXO Control Voltage			0		V_{CC}	V
V_{PP}	Peak-to-Peak Input Voltage; NOTE 1			0.15		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			V_{EE} + 0.5		V_{EE} - 0.85	V

NOTE 1: V_{IL} should not be less than -0.3V.
NOTE 2: Common mode voltage is defined as V_{IH}.

TABLE 4D. LVPECL DC CHARACTERISTICS, V_{CC} = V_{CCO} = 3.3V±5%, V_{EE} = 0V, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		V_{CCO} - 1.4		V_{CCO} - 0.9	V
V_{OL}	Output Low Voltage; NOTE 1		V_{CCO} - 2.0		V_{CCO} - 1.7	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.6		1.0	V

NOTE 1: Outputs terminated with 50Ω to V_{CCO} - 2V.

TABLE 5A. AC CHARACTERISTICS, $V_{CC} = V_{CCO} = 3.3V \pm 5\%$, $V_{EE} = 0V$, $T_A = -40°C$ TO $85°C$ (VC = 0, FREQUENCY MULTIPLIER)

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{REF}	Input Frequency; NOTE 1	CLK0/nCLK0 or CLK1/nCLK1	nBYPASS = 1	15.36MHz - 50ppm		61.44MHz + 50ppm	
fosc	XTAL Frequency				30.72		MHz
f_{OUT}	Output Frequency; NOTE 2	QAx, QBx, QC	nBYPASS = 1, MF = 20, N = 1		614.4		MHz
			nBYPASS = 1, MF = 20, N = 4		153.6		MHz
			nBYPASS = 1, MF = 20, N = 5		122.88		MHz
			nBYPASS = 1, MF = 20, N = 20		30.72		MHz
			nBYPASS = 1, MF = 16, N = 1		491.52		MHz
			nBYPASS = 1, MF = 16, N = 4		122.88		MHz
			nBYPASS = 1, MF = 16, N = 5		98.304		MHz
			nBYPASS = 1, MF = 16, N = 20		24.576		MHz
*t*jit(Ø)	RMS Phase Jitter; Integration Range: 12kHz - 20MHz		f_{OUT} = 61.44MHz, XTAL = 30.72MHz		0.97		ps
Φ_n	Single-Side Band Phase Noise at f_{OUT} = 614MHz	10Hz offset	XTAL = 30.72MHz		-59.4		dBc/Hz
		100Hz offset			-60.4		dBc/Hz
		1kHz offset			-79.4		dBc/Hz
		10kHz offset			-106.7		dBc/Hz
		100kHz offset			-112.9		dBc/Hz
		spurious	Does not include harmonic spurs	-42			dB
		sub harmonics		-19			dB
*t*sk(o)	Output Skew; NOTE 3	$f_{QA} = f_{QB} = f_{QC}$				240	ps
t_R / t_F	Output Rise/Fall Time		20% to 80%	160		700	ps
odc	Output Duty Cycle		N ≠ 1	45		55	%
			N = 1	40		60	%
t_{LOCK}	PLL Lock Time	FLM = 1			360	600	ms
		FLM = 0			2.5	5.0	s

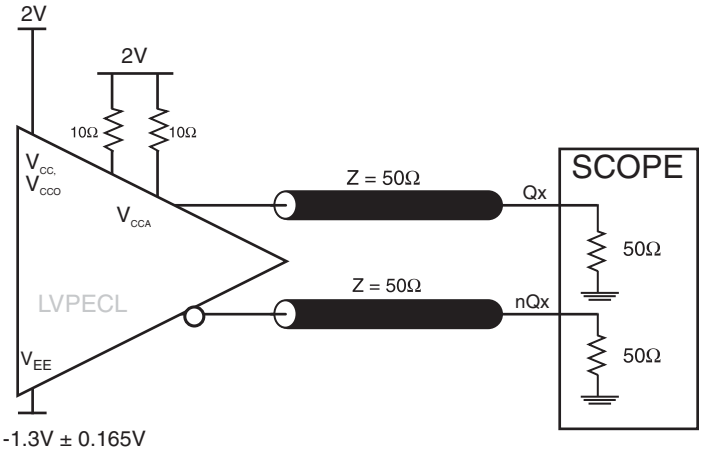
NOTE 1: f_{REF} depends on P and M. In all applications, $f_{REF} = (30.72MHz \div MV * P) \pm 50ppm$.
NOTE 2: $f_{OUT} = ((f_{REF} \div P) * MV * MF) \div N$.
NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions.

TABLE 5B. AC CHARACTERISTICS, $V_{CC} = V_{CCO} = 3.3V \pm 5\%$, $V_{EE} = 0V$, $T_A = -40°C$ TO $85°C$ (VC = 1, VCXO MODE)

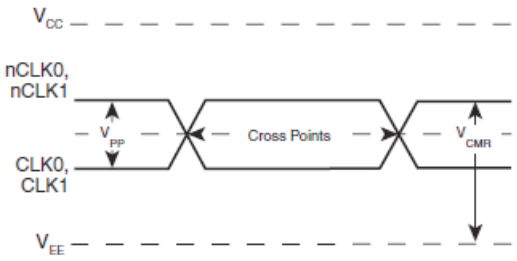
Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
fosc	XTAL Frequency				30.72		MHz
f_{OUT}	Output Frequency; NOTE 1	QAx, QBx, QC	nBYPASS = 1, MF = 20, N = 1		614.4		MHz
			nBYPASS = 1, MF = 20, N = 4		153.6		MHz
			nBYPASS = 1, MF = 20, N = 5		122.88		MHz
			nBYPASS = 1, MF = 20, N = 20		30.72		MHz
			nBYPASS = 1, MF = 16, N = 1		491.52		MHz
			nBYPASS = 1, MF = 16, N = 4		122.88		MHz
			nBYPASS = 1, MF = 16, N = 5		98.304		MHz
			nBYPASS = 1, MF = 16, N = 20		24.576		MHz
APR	Absolute Pull Range			-50		50	ppm
BW	Modulation Bandwidth of VCXO				200		kHz
L_{VC}	Tuning Linearity		VC = 0.6V to 1.4V		±6.5		%
tjit(Ø)	RMS Phase Jitter; Integration Range: 12kHz - 20MHz		f_{OUT} = 122.88MHz, XTAL = 30.72MHz		0.88		ps/rms
F_n	Single-Side Band Phase Noise at f_{OUT} = 122.88MHz	10Hz offset	XTAL = 30.72MHz		-41.18		dBc/Hz
		100Hz offset			-72.82		dBc/Hz
		1kHz offset			-104.19		dBc/Hz
		10kHz offset			-126.63		dBc/Hz
		100kHz offset			-128.57		dBc/Hz
		spurious	Does not include harmonic spurs		-51		dB
		sub harmonics			-11		dB
tsk(o)	Output Skew; NOTE 2	$f_{QA} = f_{QB} = f_{QC}$				240	ps
t_R / t_F	Output Rise/Fall Time		20% to 80%	160		700	ps
odc	Output Duty Cycle		N ≠ 1	45		55	%
			N = 1	40		60	%

NOTE 1: $f_{OUT} = ((30.72MHz) * MF) \div N \pm 50ppm$.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions.

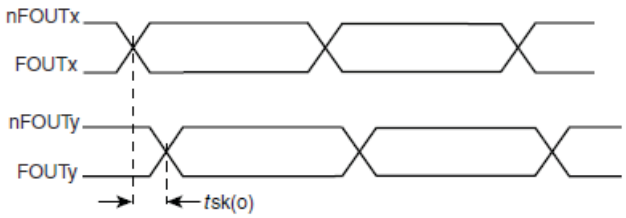
PARAMETER MEASUREMENT INFORMATION



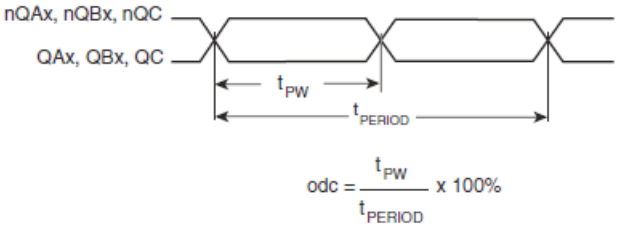
3.3V OUTPUT LOAD AC TEST CIRCUIT



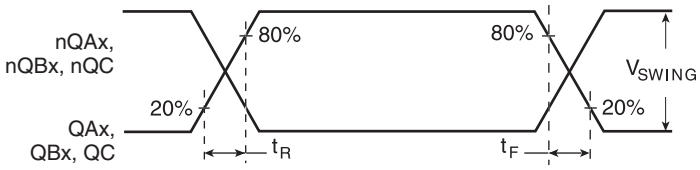
DIFFERENTIAL INPUT LEVEL



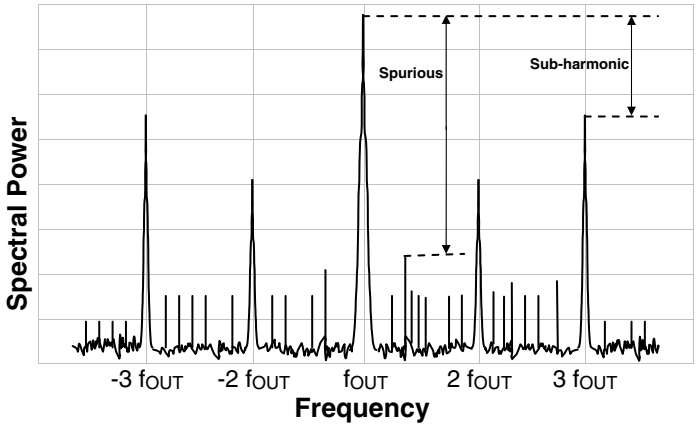
OUTPUT SKEW



OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD



OUTPUT RISE/FALL TIME



SPURIOUS/SUB-HARMONICS

APPLICATION INFORMATION

POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The ICS813076I provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{CC}, V_{CCA}, and V_{CCO} should be individually connected to the power supply plane through vias, and 0.01µF bypass capacitors should be used for each pin. *Figure 3* illustrates this for a generic V_{CC} pin and also shows that V_{CCA} requires that an additional10Ω resistor along with a 10µF bypass capacitor be connected to the V_{CCA} pin.

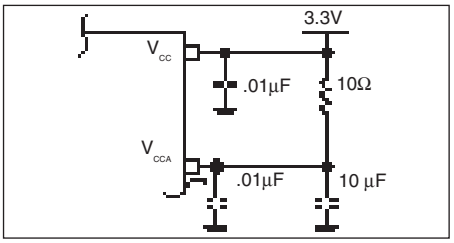


FIGURE 3. POWER SUPPLY FILTERING

WIRING THE DIFFERENTIAL INPUT TO ACCEPT SINGLE ENDED LEVELS

Figure 4 shows how the differential input can be wired to accept single ended levels. The reference voltage V_REF ≃ V_{CC}/2 is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and V_{CC} = 3.3V, V_REF should be 1.25V and R2/R1 = 0.609.

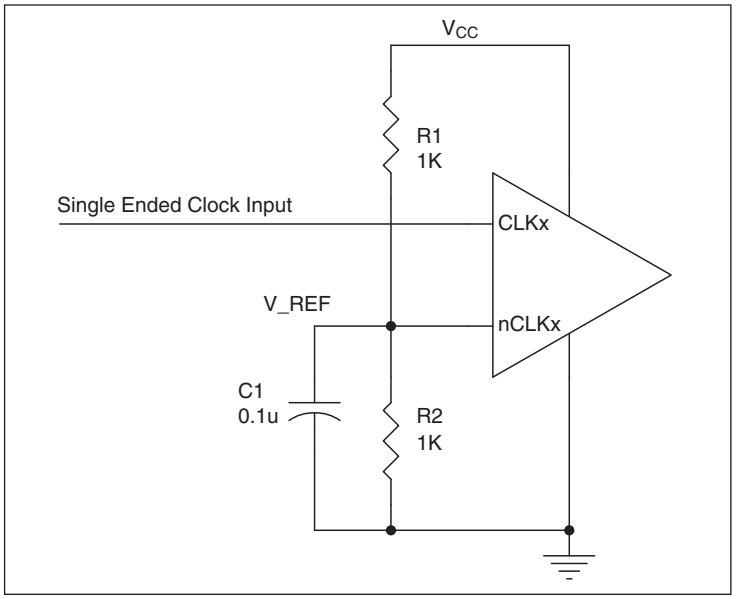


FIGURE 4. SINGLE-ENDED SIGNAL DRIVING DIFFERENTIAL INPUT

Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, SSTL, HCSL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. *Figures 5A to 5F* show interface examples for the HiPerClockS CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only.

Please consult with the vendor of the driver component to confirm the driver termination requirements. For example in Figure 5A, the input termination applies for IDT HiPerClockS open emitter LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

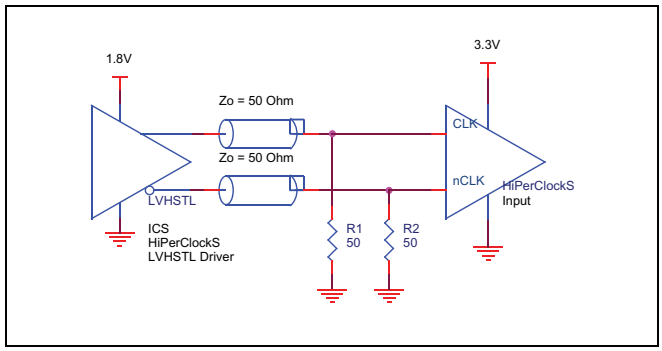


Figure 5A. HiPerClockS CLK/nCLK Input Driven by an IDT Open Emitter HiPerClockS LVHSTL Driver

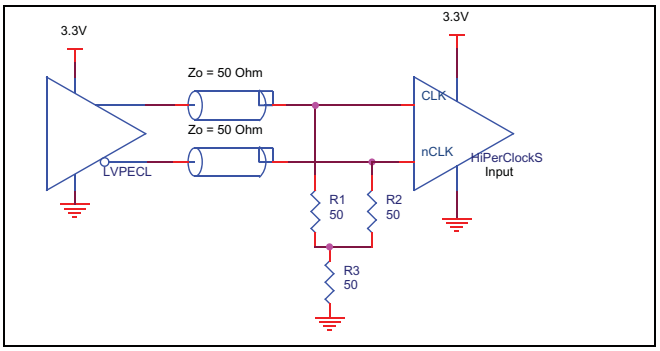


Figure 5B. HiPerClockS CLK/nCLK Input Driven by a 3.3V LVPECL Driver

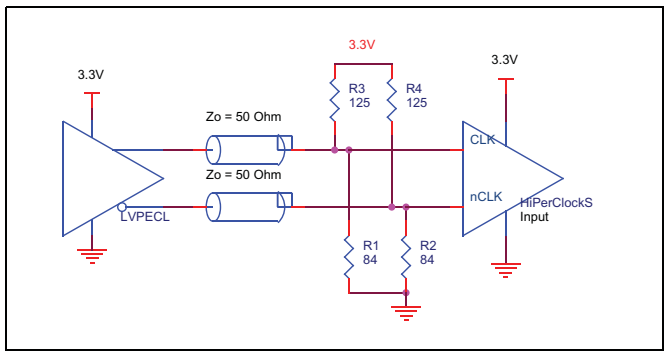


Figure 5C. HiPerClockS CLK/nCLK Input Driven by a 3.3V LVPECL Driver

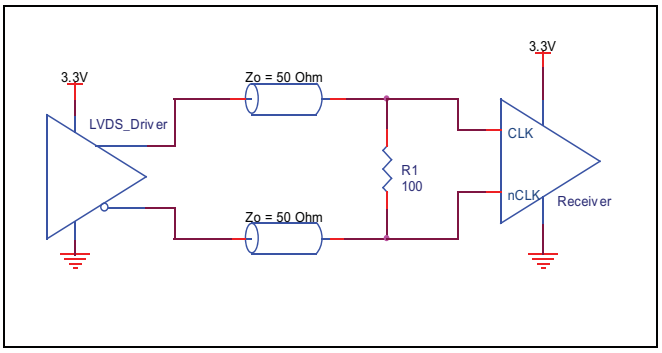


Figure 5D. HiPerClockS CLK/nCLK Input Driven by a 3.3V LVDS Driver

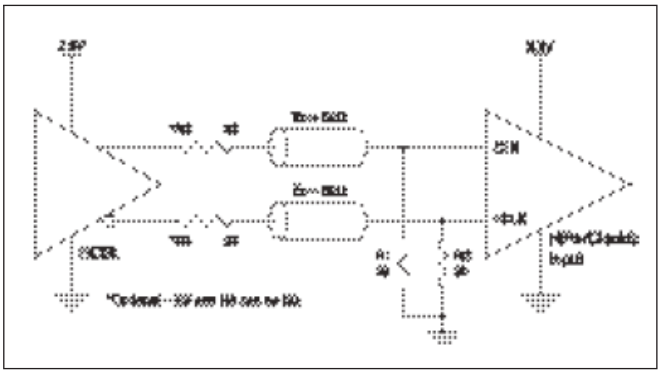


Figure 5E. HiPerClockS CLK/nCLK Input Driven by a 3.3V HCSL Driver

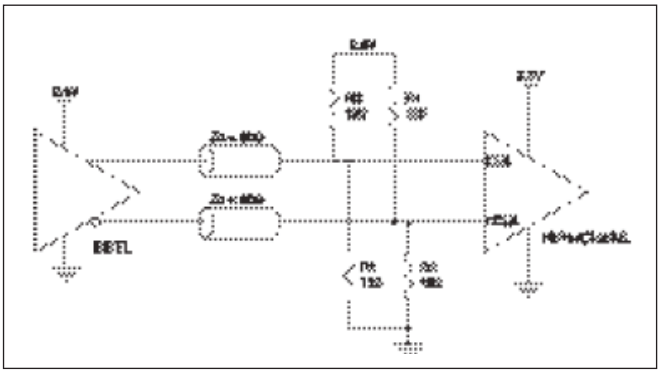


Figure 5F. HiPerClockS CLK/nCLK Input Driven by a 2.5V SSTL Driver

Recommendations for Unused Input and Output Pins

Inputs:

CLK/nCLK Inputs

For applications not requiring the use of the differential input, both CLK and nCLK can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from CLK to ground.

LVCMOS Control Pins

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs:

LVPECL Outputs

All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 6A and 6B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

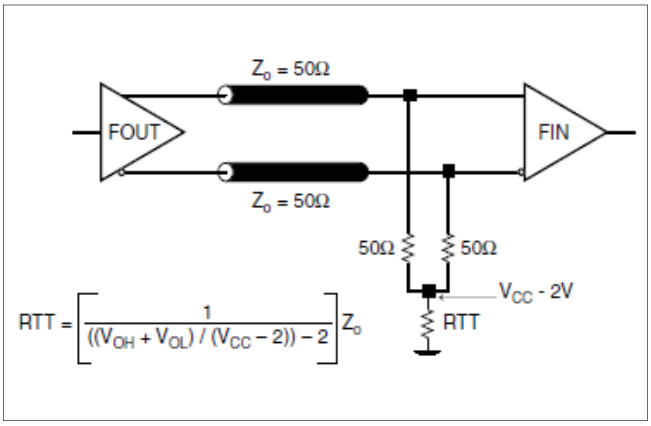


Figure 6A. LVPECL Output Termination

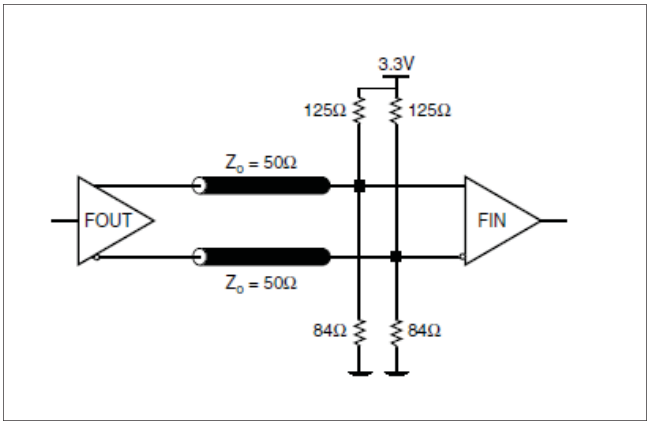


Figure 6B. LVPECL Output Termination

EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 7.* The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as "heat pipes". The number of vias (i.e. "heat pipes") are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, refer to the Application Note on the *Surface Mount Assembly* of Amkor's Thermally/Electrically Enhance Leadfame Base Package, Amkor Technology.

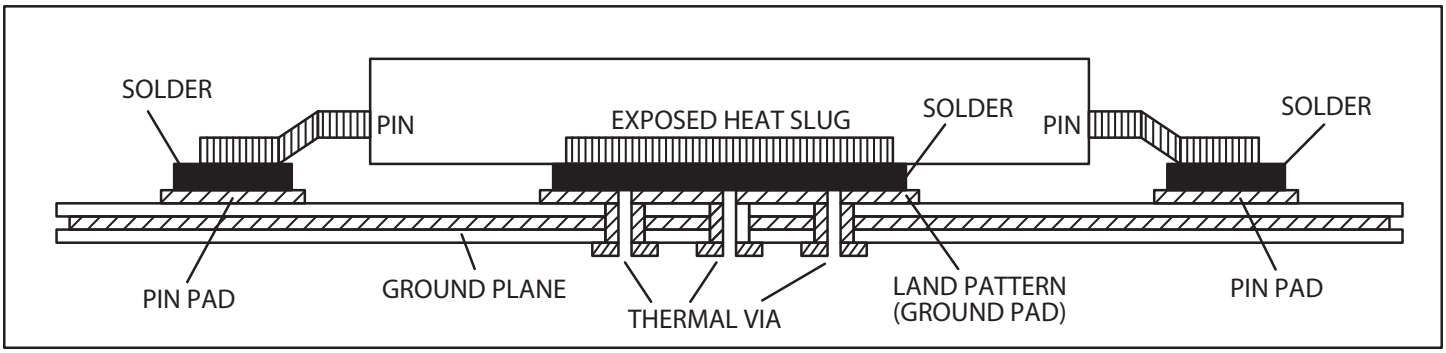


Figure 7. Assembly for Exposed Pad Thermal Release Path –Side View (Drawing not to Scale)

SCHEMATIC LAYOUT

Figure 8 shows an example of the ICS813076I application schematic. In this example, the device is operated at $V_{CC} = V_{CCO} = 3.3V$. The decoupling capacitors should be located as close as possible to the power pin. The input is driven by a 3.3V LVPECL driver. An optional 3-pole filter can also be used for additional spur reduction. It is recommended that the loop filter components be laid out for the 3-pole option. This will also allow the 2-pole filter to be used.

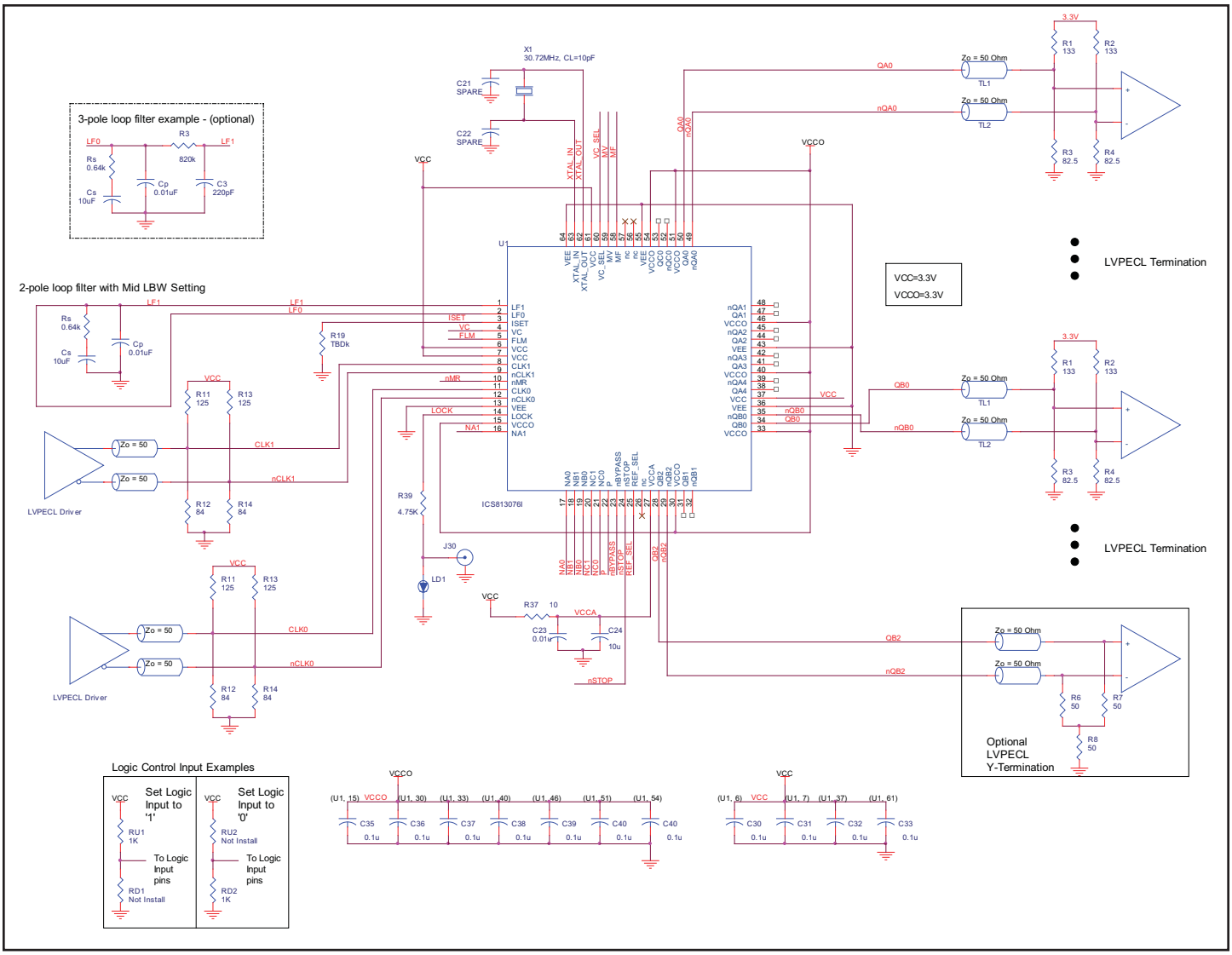


FIGURE 8. ICS813076I APPLICATION SCHEMATIC

POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the ICS813076I.
Equations and example calculations are also provided.

1. Power Dissipation.
The total power dissipation for the ICS813076I is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{CC} = 3.3V + 5% = 3.465V, which gives worst case results.
NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)$_{MAX}$ = V_{CC_MAX} * I_{EE} = 3.465V * 250mA = **866.25mW**
- Power (outputs)$_{MAX}$ = **30mW/Loaded Output pair**
  If all outputs are loaded, the total power is 9 * 30mW = **270mW**

Total Power$_{_MAX}$ (3.465V, with all outputs switching) = 866.25mW + 270mW = **1136.25mW**

2. Junction Temperature.
Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 31.8°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:
85°C + 1.136W * 31.8°C/W = 121.1°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

TABLE 6. THERMAL RESISTANCE θ_{JA} FOR 64 LEAD TQFP, E-PAD FORCED CONVECTION

θ_{JA} by Velocity (Meters per Second)			
	0	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	31.8°C/W	25.8°C/W	24.2°C/W

3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

LVPECL output driver circuit and termination are shown in *Figure 9.*

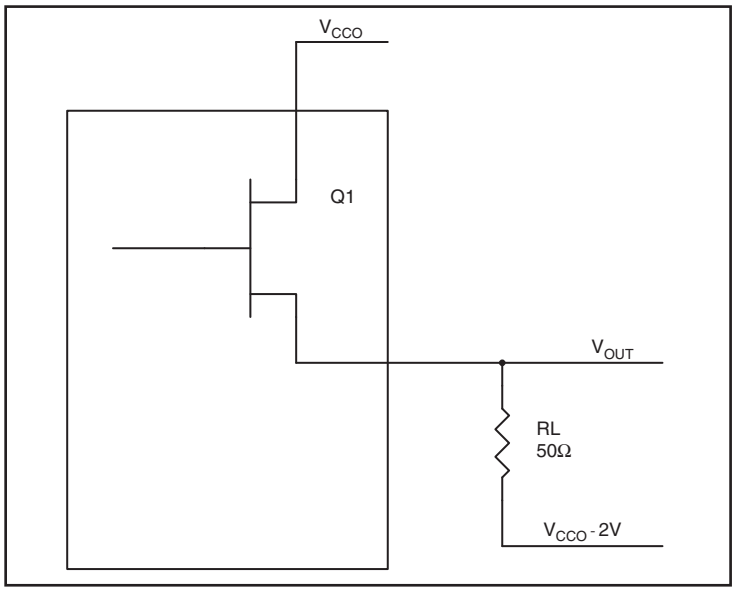


FIGURE 9. LVPECL DRIVER CIRCUIT AND TERMINATION

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of V_{CCO} – 2V.

- For logic high, $V_{OUT} = V_{OH_MAX} = \mathbf{V_{CC_MAX} - 0.9V}$

  $(V_{CCO_MAX} - V_{OH_MAX}) = \mathbf{0.9V}$

- For logic low, $V_{OUT} = V_{OL_MAX} = \mathbf{V_{CC_MAX} - 1.7V}$

  $(V_{CCO_MAX} - V_{OL_MAX}) = \mathbf{1.7V}$

Pd_H is power dissipation when the output drives high.
Pd_L is the power dissipation when the output drives low.

$Pd_H = [(V_{OH_MAX} - (V_{CCO_MAX} - 2V))/R_L] * (V_{CCO_MAX} - V_{OH_MAX}) = [(2V - (V_{CCO_MAX} - V_{OH_MAX}))/R_L] * (V_{CCO_MAX} - V_{OH_MAX}) =$
$[(2V - 0.9V)/50\Omega] * 0.9V =$ **19.8mW**

$Pd_L = [(V_{OL_MAX} - (V_{CCO_MAX} - 2V))/R_L] * (V_{CCO_MAX} - V_{OL_MAX}) = [(2V - (V_{CCO_MAX} - V_{OL_MAX}))/R_L] * (V_{CCO_MAX} - V_{OL_MAX}) =$
$[(2V - 1.7V)/50\Omega] * 1.7V =$ **10.2mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **30mW**

VCXO-PLL External Components

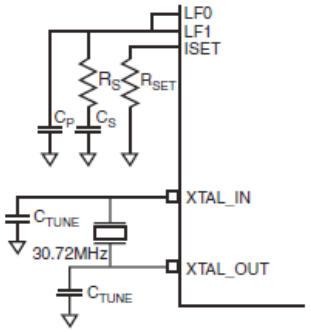
Choosing the correct external components and having a proper printed circuit board (PCB) layout is a key task for quality operation of the VCXO-PLL. In choosing a crystal, special precaution must be taken with the package and load capacitance (C_L). In addition, frequency, accuracy and temperature range must also be considered. Since the pulling range of a crystal also varies with the package, it is recommended that a metal-canned package like HC49 be used. Generally, a metal-canned package has a larger pulling range than a surface mounted device (SMD). For crystal selection information, refer to the *VCXO Crystal Selection Application Note.*

The crystal's load capacitance C_L characteristic determines its resonating frequency and is closely related to the VCXO tuning range. The total external capacitance seen by the crystal when installed on a board is the sum of the stray board capacitance, IC package lead capacitance, internal varactor capacitance and any installed tuning capacitors (C_{TUNE}).

If the crystal C_L is greater than the total external capacitance, the VCXO will oscillate at a higher frequency than the crystal specification. If the crystal C_L is lower than the total external capacitance, the VCXO will oscillate at a lower frequency than the crystal specification. In either case, the absolute tuning range is reduced. The correct value of C_L is dependant on the characteristics of the VCXO. The recommended C_L in the Crystal Parameter Table balances the tuning range by centering the tuning curve.

The *VCXO-PLL Loop Bandwidth Selection Table* shows R_S, C_S and C_P values for recommended high, mid and low loop bandwidth configurations. The device has been characterized using these parameters. For other configurations, refer to the *Loop Filter Component Selection for VCXO Based PLLs Application Note.*

The crystal and external loop filter components should be kept as close as possible to the device. Loop filter and crystal traces should be kept short and separated from each other. Other signal traces should be kept separate and not run underneath the device, loop filter or crystal components.



VCXO Characteristics Table

Symbol	Parameter	Typical	Unit
k_{VCXO}	VCXO Gain	11	kHz/V
C_{V_LOW}	Low Varactor Capacitance	10	pF
C_{V_HIGH}	High Varactor Capacitance	25	pF

VCXO-PLL Loop Bandwidth Selection Table

Bandwidth	Crystal Frequency (MHz)	MV	R_S (kΩ)	C_S (µF)	C_P (µF)	R_{SET} (kΩ)
72Hz (Low)	30.72MHz	2	1.5	10	0.1	20
259Hz (Mid)	30.72MHz	1	0.64	10	0.01	4.75
871Hz (High)	30.72MHz	1	1	4.7	0.001	2.21

Crystal Characteristics

Symbol	Parameter	Minimum	Typical	Maximum	Units
	Mode of Operation	Fundamental			
f_N	Frequency		30.72		MHz
f_T	Frequency Tolerance			±20	ppm
f_S	Frequency Stability			±20	ppm
	Operating Temperature Range	-40		85	°C
C_L	Load Capacitance		10		pF
C_O	Shunt Capacitance		4		pF
C_O/C_1	Pullability Ratio		220	240	
ESR	Equivalent Series Resistance			20	
	Drive Level			1	mW
	Aging @ 25°C			±3 per year	ppm

Reliability Information

Table 7. θ_{JA} vs. Air Flow Table for 64 Lead TQFP, E-Pad

θ_{JA} by Velocity (Meters per Second)			
	0	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	31.8°C/W	25.8°C/W	24.2°C/W

Transistor Count

The transistor count for ICS813076I is: 4709

Package Outline - Y Suffix for 64 Lead TQFP, E-Pad

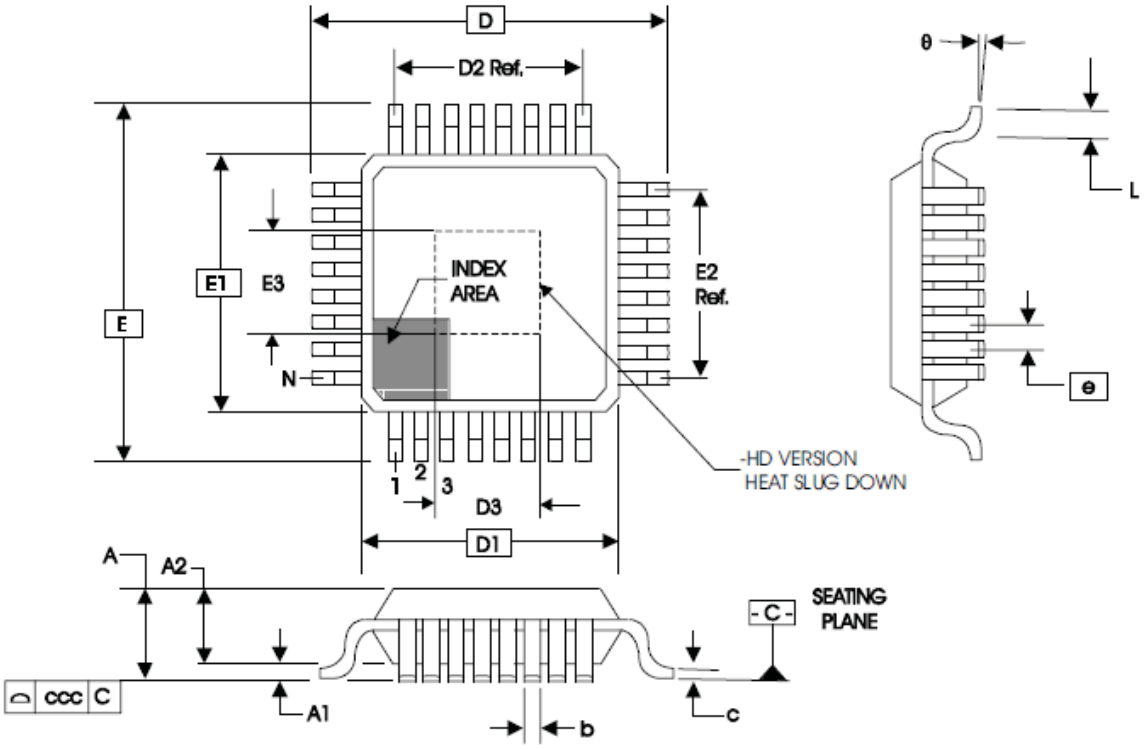


Table 7. Package Dimensions

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS			
SYMBOL	ACD-HD		
	MINIMUM	NOMINAL	MAXIMUM
N		64	
A	--	--	1.20
A1	0.05	0.10	0.15
A2	0.95	1.0	1.05
b	0.17	0.22	0.27
c	0.09	--	0.20
D		12.00 BASIC	
D1		10.00 BASIC	
D2		7.50 Ref.	
E		12.00 BASIC	
E1		10.00 BASIC	
E2		7.50 Ref.	
e		0.50 BASIC	
L	0.45	0.60	0.75
θ	0°	--	7°
ccc	--	--	0.08
D3 & E3	4.5	5.0	5.5

Reference Document: JEDEC Publication 95, MS-026

TABLE 9. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
813076CYILF	ICS813076CYILF	64 Lead “Lead-Free” TQFP, E-Pad	Tray	-40°C to 85°C
813076CYILFT	ICS813076CYILF	64 Lead “Lead-Free” TQFP, E-Pad	500 Tape & Reel	-40°C to 85°C

NOTE: Parts that are ordered with an “LF” suffix to the part number are the Pb-Free configuration and are RoHS compliant.

Revision History

7/29/16 Added OBSOLETE to the front page.

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