Universal Octal T1/E1/J1 LIU with Integrated Clock Adapter

IDT82P5088

FEATURES

- Eight channel T1/E1/J1 long haul/short haul line interfaces
- Supports HPS (Hitless Protection Switching) for 1+1 protection without external relays
- Receiver sensitivity exceeds -36 dB@772KHz and -43 dB@1024 KHz
- Programmable T1/E1/J1 switchability allowing one bill of material for any line condition
- 3.3 V and 1.8 V power supply with 5 V tolerant inputs
- Meets or exceeds specifications in
  - ANSI T1.102, T1.403 and T1.408
  - ITU I.431, G.703,G.736, G.775 and G.823
  - ETSI 300-166, 300-233 and TBR 12/13
  - AT&T Pub 62411
- Per channel software selectable on:
  - Wave-shaping templates for short haul and long haul LBO (Line Build Out)
  - Line terminating impedance (T1:100 Ω, J1:110 Ω, E1:75 Ω/120 Ω)
  - Adjustment of arbitrary pulse shape
  - JA (jitter attenuator) position (receive path and transmit path)
  - Single rail/dual rail system interfaces
  - B8ZS/HDB3/AMI line encoding/decoding
  - Active edge of transmit clock (TCLK) and receive clock (RCLK)
  - Active level of transmit data (TDATA) and receive data (RDATA)
  - Receiver or transmitter power down
  - High impedance setting for line drivers
  - PRBS (Pseudo Random Bit Sequence) generation and detection with 2^{15}-1 PRBS polynomials for E1
  - QRSS (Quasi Random Sequence Signals) generation and detection with 2^{20}-1 QRSS polynomials for T1/J1
  - 16-bit BPV (Bipolar Pulse Violation)/Excess Zero/PRBS or QRSS error counter
  - Analog loopback, Digital loopback, Remote loopback and Inband loopback
- Per channel cable attenuation indication
- Adaptive receive sensitivity
- Non-intrusive monitoring per ITU G.772 specification
- Short circuit protection for line drivers
- LOS (Loss Of Signal) & AIS (alarm indication signal) detection
- JTAG interface
- Supports serial control interface, Motorola and Intel Non-Multiplexed interfaces
- Package:
  Available in 256-pin BGA
  Green package options available

DESCRIPTION

The IDT82P5088 is an eight port line intereface that can be configured per port to any combination of T1, E1 or J1 ports. In receive path, an adaptive equalizer is integrated to remove the distortion introduced by the cable attenuation. The IDT82P5088 also performs clock/data recovery, AMI/B8ZS/HDB3 line decoding and detects and reports the LOS conditions. In the transmit path, there is an AMI/B8ZS/HDB3 encoder, waveform shaper, LBOs and jitter attenuator for each channel. The jitter attenuators in both the transmit path and receive path can be disabled. The IDT82P5088 supports both single rail and dual rail system interfaces. To facilitate network maintenance, a PRBS/QRSS generation/detection circuit is integrated in each channel, and different types of loopbacks can be set on a per channel basis. Four different kinds of line terminating impedance, 75Ω, 100 Ω, 110 Ω and 120 Ω are selectable on a per channel basis. The chip also provides driver short-circuit protection and supports JTAG boundary scanning.

The IDT82P5088 can be used in SDH/SONET, WAN, routers, wireless base stations, IADs, IMA, IMAPs, gateways, frame relay access devices, CSU/DSU equipment, etc.

IDT and the IDT logo are trademarks of Integrated Device Technology, Inc.

© 2019 Renesas Electronics Corporation

FUNCTIONAL BLOCK DIAGRAM

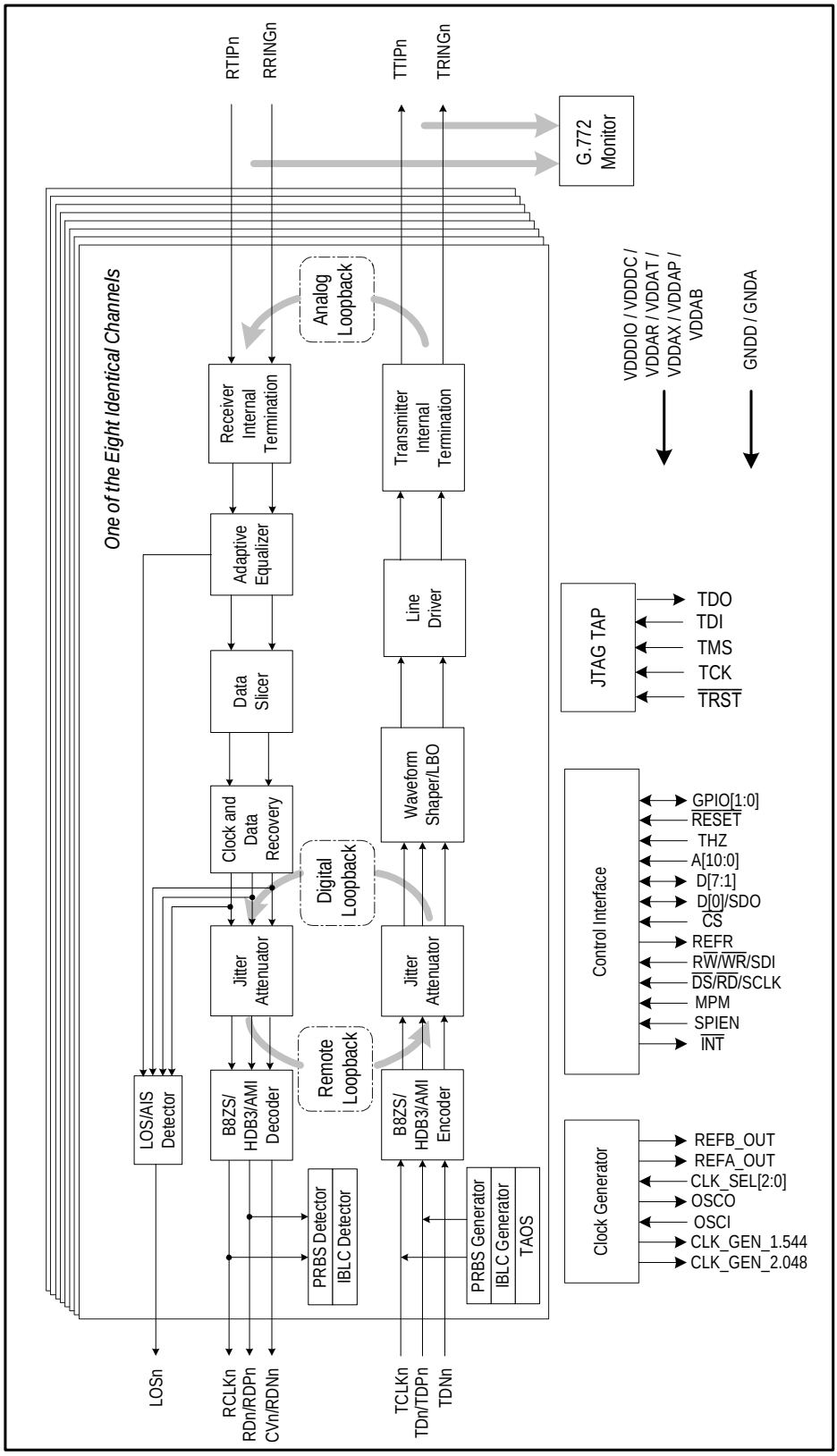


Figure-1 Block Diagram

© 2019 Renesas Electronics Corporation

Tables of Contents

1 IDT82P5088 PIN CONFIGURATIONS 9

2 PIN DESCRIPTION 10

3 FUNCTIONAL DESCRIPTION 17

3.1 T1/E1/J1 MODE SELECTION 17

3.2 TRANSMIT PATH 17

3.2.1 TRANSMIT PATH SYSTEM INTERFACE 17

3.2.2 ENCODER 17

3.2.3 PULSE SHAPER 17

3.2.3.1 Preset Pulse Templates 17

3.2.3.2 LBO (Line Build Out) 18

3.2.3.3 User-Programmable Arbitrary Waveform 18

3.2.4 TRANSMIT PATH LINE INTERFACE 22

3.2.5 TRANSMIT PATH POWER DOWN 22

3.2.6 TRANSMIT JITTER ATTENUATOR 22

3.3 RECEIVE PATH 24

3.3.1 RECEIVE INTERNAL TERMINATION 24

3.3.2 LINE MONITOR 25

3.3.3 ADAPTIVE EQUALIZER 25

3.3.4 RECEIVE SENSITIVITY 25

3.3.5 DATA SLICER 25

3.3.6 CDR (Clock & Data Recovery) 25

3.3.7 DECODER 25

3.3.8 RECEIVE PATH SYSTEM INTERFACE 25

3.3.9 RECEIVE PATH POWER DOWN 25

3.3.10 G.772 NON-INTRUSIVE MONITORING 26

3.3.11 RECEIVE JITTER ATTENUATOR 26

3.3.12 LOS AND AIS DETECTION 27

3.3.12.1 LOS DETECTION 27

3.3.12.2 AIS DETECTION 29

3.4 TRANSMIT AND DETECT INTERNAL PATTERNS 30

3.4.1 TRANSMIT ALL ONES 30

3.4.2 TRANSMIT ALL ZEROS 30

3.4.3 PRBS/QRSS GENERATION AND DETECTION 30

3.5 LOOPBACK 31

3.5.1 ANALOG LOOPBACK 31

3.5.2 DIGITAL LOOPBACK 31

3.5.3 REMOTE LOOPBACK 31

© 2019 Renesas Electronics Corporation

3.5.4 INBAND LOOPBACK 33
3.5.4.1 Transmit Activate/Deactivate Loopback Code 33
3.5.4.2 Receive Activate/Deactivate Loopback Code 33
3.5.4.3 Automatic Remote Loopback 33
3.6 ERROR DETECTION/COUNTING AND INSERTION 34
3.6.1 DEFINITION OF LINE CODING ERROR 34
3.6.2 ERROR DETECTION AND COUNTING 34
3.6.3 BIPOLAR VIOLATION AND PRBS ERROR INSERTION 35
3.7 LINE DRIVER FAILURE MONITORING 35
3.8 CLOCK GENERATOR AND TCLK 36
3.8.1 CLOCK GENERATOR 36
3.8.2 TRANSMIT CLOCK (TCLK) 36
3.9 MICROPROCESSOR INTERFACE 37
3.9.1 SPI Mode 37
3.9.2 Parallel Microprocessor Interface 37
3.10 INTERRUPT HANDLING 38
3.11 GENERAL PURPOSE I/O 39
3.12 RESET OPERATION 39
3.13 POWER SUPPLY 39
4 PROGRAMMING INFORMATION 40
4.1 REGISTER LIST AND MAP 40
4.2 RESERVED REGISTERS 40
4.3 REGISTER DESCRIPTION 42
4.3.1 GLOBAL REGISTERS 42
4.3.2 PER CHANNEL CONTROL REGISTERS 44
4.3.3 TRANSMIT PATH CONTROL REGISTERS 44
4.3.4 RECEIVE PATH CONTROL REGISTERS 47
4.3.5 NETWORK DIAGNOSTICS CONTROL REGISTERS 49
4.3.6 TRANSMIT AND RECEIVE TERMINATION REGISTER 52
4.3.7 INTERRUPT CONTROL REGISTERS 52
4.3.8 LINE STATUS REGISTERS 55
4.3.9 INTERRUPT STATUS REGISTERS 58
4.3.10 COUNTER REGISTERS 59
5 IEEE STD 1149.1 JTAG TEST ACCESS PORT 60
5.1 JTAG INSTRUCTIONS AND INSTRUCTION REGISTER 61
5.2 JTAG DATA REGISTER 61
5.2.1 DEVICE IDENTIFICATION REGISTER (IDR) 61
5.2.2 BYPASS REGISTER (BR) 61
5.2.3 BOUNDARY SCAN REGISTER (BSR) 61
5.2.4 TEST ACCESS PORT CONTROLLER 62
6 TEST SPECIFICATIONS 64

© 2019 Renesas Electronics Corporation

6.1 Absolute maximum Ratings 64
6.2 Recommended Operating Conditions 64
6.3 D.C. Characteristics 65
6.4 T1/J1 Line Receiver Electrical Characteristics 66
6.5 E1 Line Receiver Electrical Characteristics 67
6.6 T1/J1 Line Transmitter Electrical Characteristics 67
6.7 E1 Line Transmitter Electrical Characteristics 68
6.8 Transmitter and Receiver Timing Characteristics 69
6.9 Jitter Tolerance 70
6.9.1 T1/J1 Mode 70
6.9.2 E1 Mode 71
6.10 Jitter Transfer 73
6.10.1 T1/J1 Mode 73
6.10.2 E1 Mode 74

7 MICROCONTROLLER INTERFACE TIMING 77
7.1 Motorola Non-Multiplexed Mode 77
7.1.1 Read Cycle Specification 77
7.1.2 Write Cycle Specification 77
7.2 Intel Non-Multiplexed Mode 78
7.2.1 Read Cycle Specification 78
7.2.2 Write Cycle Specification 79
7.3 SPI Mode 80

8 THERMAL CHARACTERISTICS 81

8 ORDERING INFORMATION 81

© 2019 Renesas Electronics Corporation

List Of Tables

Table-1 Pin Description 10
Table-2 Transmit Waveform Value For E1 75 W 19
Table-3 Transmit Waveform Value For E1 120 W 19
Table-4 Transmit Waveform Value For T1 0~133 ft 19
Table-5 Transmit Waveform Value For T1 133~266 ft 19
Table-6 Transmit Waveform Value For T1 266~399 ft 20
Table-7 Transmit Waveform Value For T1 399~533 ft 20
Table-8 Transmit Waveform Value For T1 533~655 ft 20
Table-9 Transmit Waveform Value For J1 0~655 ft 20
Table-10 Transmit Waveform Value For DS1 0 dB LBO 21
Table-11 Transmit Waveform Value For DS1 -7.5 dB LBO 21
Table-12 Transmit Waveform Value For DS1 -15.0 dB LBO 21
Table-13 Transmit Waveform Value For DS1 -22.5 dB LBO 21
Table-14 Impedance Matching for Transmitter 22
Table-15 Related Bit / Register In Chapter 3.2.6 23
Table-16 Impedance Matching for Receiver 24
Table-17 Criteria Of Speed Adjustment Start 27
Table-18 Related Bit / Register In Chapter 3.3.11 27
Table-19 LOS Declare and Clear Criteria for Short Haul Mode 28
Table-20 LOS Declare and Clear Criteria for Long Haul Mode 29
Table-21 AIS Condition 30
Table-22 Criteria for Setting/Clearing the PRBS_S Bit 30
Table-23 EXZ Definition 34
Table-24 Reference Clock Selection 36
Table-25 Parallel Microprocessor Interface 37
Table-26 Interrupt Event 38
Table-27 Global Register List and Map 40
Table-28 Per Channel Register List and Map 41
Table-29 ID: Chip Revision Register 42
Table-30 RST: Reset Register 42
Table-31 MON: G.772 Monitor control Register 42
Table-32 GPIO: General Purpose IO Pin Definition Register 42
Table-33 REFOUT: Reference clock output select Register 43
Table-34 INTCH: Interrupt Channel Indication Register 43
Table-35 TIMER INTE: Timer Interrupt Enable Register 43
Table-36 TIMER INTS: Timer Interrupt Status Register 44

© 2019 Renesas Electronics Corporation

Table-37 TIE1 MODE: T1 or E1 Mode Select Register 44
Table-38 TJACF: Jitter Attenuator Configuration Register for Transmit Path 44
Table-39 TCF0: Transmitter Configuration Register 0 for Transmit Path 44
Table-40 TCF1: Transmitter Configuration Register 1 for Transmit Path 45
Table-41 TCF2: Transmitter Configuration Register 2 for Transmit Path 46
Table-42 TCF3: Transmitter Configuration Register 3 for Transmit Path 46
Table-43 TCF4: Transmitter Configuration Register 4 for Transmit Path 46
Table-44 RJACF: Jitter Attenuator Configuration Register for Receive Path 47
Table-45 RCF0: Receiver Configuration Register 0 for Receive Path 47
Table-46 RCF1: Receiver Configuration Register 1 for Receive Path 48
Table-47 RCF2: Receiver Configuration Register 2 for Receive Path 49
Table-48 MAINT0: Maintenance Function Control Register 0 49
Table-49 MAINT1: Maintenance Function Control Register 1 49
Table-50 MAINT2: Maintenance Function Control Register 2 50
Table-51 MAINT3: Maintenance Function Control Register 3 50
Table-52 MAINT4: Maintenance Function Control Register 4 51
Table-53 MAINT5: Maintenance Function Control Register 5 51
Table-54 MAINT6: Maintenance Function Control Register 6 51
Table-55 TERM: Transmit and Receive Termination Configuration Register 52
Table-56 INTENC0: Interrupt Mask Register 0 52
Table-57 INTENC1: Interrupt Mask Register 1 53
Table-58 INTES: Interrupt Trigger Edges Select Register 54
Table-59 STAT0: Line Status Register 0 (real time status monitor) 55
Table-61 TJITT: Jitter Measure Value Indicate Register (Transmit Path) 57
Table-62 TJITT: Jitter Measure Value Indicate Register (Receive Path) 57
Table-60 STAT1: Line Status Register 1 (real time status monitor) 57
Table-63 INTS0: Interrupt Status Register 0 58
Table-64 INTS1: Interrupt Status Register 1 59
Table-65 CNTL: Error Counter L-byte Register 0 59
Table-66 CNTH: Error Counter H-byte Register 1 59
Table-67 REFC: E1 Reference Clock Output Control 59
Table-68 Instruction Register Description 61
Table-69 Device Identification Register Description 61
Table-70 TAP Controller State Description 62
Table-71 JTAG Timing Characteristics 75

© 2019 Renesas Electronics Corporation

List Of Figures

Figure-1 Block Diagram 2
Figure-2 IDT82P5088 CABGA256 Package Pin Assignment (top view) 9
Figure-3 E1 Waveform Template Diagram 17
Figure-4 E1 Pulse Template Test Circuit 17
Figure-5 DSX-1 Waveform Template 18
Figure-6 T1 Pulse Template Test Circuit 18
Figure-7 Jitter Attenuator 22
Figure-8 Receive Path Function Block Diagram 24
Figure-9 Transmit/Receive Line Circuit 24
Figure-10 Monitoring Receive Line in Another Chip 25
Figure-11 Monitor Transmit Line in Another Chip 25
Figure-12 G.772 Monitoring Diagram 26
Figure-13 LOS Declare and Clear 27
Figure-14 Analog Loopback 31
Figure-15 Digital Loopback 31
Figure-16 Remote Loopback 32
Figure-17 Auto Report Mode 34
Figure-18 Manual Report Mode 35
Figure-19 Clock Generator 36
Figure-20 TCLK Operation Flowchart 36
Figure-21 Read Operation In SPI Mode 37
Figure-22 Write Operation In SPI Mode 37
Figure-23 JTAG Architecture 60
Figure-24 JTAG State Diagram 63
Figure-25 Transmit System Interface Timing 70
Figure-26 Receive System Interface Timing 70
Figure-27 T1/J1 Jitter Tolerance Performance Requirement 71
Figure-28 E1 Jitter Tolerance Performance Requirement 72
Figure-29 T1/J1 Jitter Transfer Performance Requirement (AT&T62411 / GR-253-CORE / TR-TSY-000009) 74
Figure-30 E1 Jitter Transfer Performance Requirement (G.736) 75
Figure-31 JTAG Interface Timing 76
Figure-32 Motorola Non-Multiplexed Mode Read Cycle 77
Figure-33 Motorola Non-Multiplexed Mode Write Cycle 78
Figure-34 Intel Non-Multiplexed Mode Read Cycle 79
Figure-35 Intel Non-Multiplexed Mode Write Cycle 79
Figure-36 SPI Timing Diagram 80

© 2019 Renesas Electronics Corporation

1 IDT82P5088 PIN CONFIGURATIONS

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
A	TTIP4	TRING4	VDDAT4	VDDAR4	VDDAR3	TRING3	TTIP3	TTIP2	TRING2	VDDAR1	TRING1	TTIP1	VDDAP	$\overline{\text{RESET}}$	REFA_OUT	CLK_GEN_1.544
B	TDN8	VDDAX4	GNDA	RTIP4	VDDAT3	GNDA	VDDAX3	VDDAX2	VDDAT2	GNDA	GNDA	VDDAT1	OSCI	REFB_OUT	CLK_SEL2	THZ
C	TDN7	TD8/TDP8	GNDA	RRING4	GNDA	GNDA	GNDA	GNDA	VDDAR2	GNDA	RTIP1	VDDAX1	OSCO	CLK_SEL1	GNDD	REFR
D	TDN6	TD7/TDP7	GNDA	GNDA	RRING3	RTIP3	GNDA	RTIP2	RRING2	GNDA	RRING1	VDDAB	GPIO1	CLK_GEN_2.048	CLK_SEL0	GNDD
E	TDN4	TD5/TDP5	TDN5	TD6/TDP6	GNDD	GNDD	GNDD	GNDD	GNDD	GNDD	GNDD	GNDD	GPIO0	VDDAX5	VDDAT5	TTIP5
F	TDN2	TD3/TDP3	TDN3	TD4/TDP4	VDDDIO	GNDD	GNDD	GNDD	GNDD	GNDD	GNDD	GNDD	GNDA	RTIP5	GNDA	TRING5
G	NC	TD1/TDP1	TDN1	TD2/TDP2	VDDDIO	GNDD	GNDD	GNDD	GNDD	GNDD	GNDD	GNDD	GNDA	RRING5	GNDA	VDDAR5
H	NC	TCLK7	NC	TCLK8	VDDDIO	VDDDC	VDDDC	VDDDC	GNDD	GNDD	GNDD	GNDD	RRING6	VDDAT6	VDDAR6	TRING6
J	TCLK6	NC	TCLK5	NC	VDDDIO	VDDDC	VDDDC	VDDDC	VDDDC	VDDDC	VDDDC	VDDDIO	RTIP6	GNDA	VDDAX6	TTIP6
K	TCLK4	NC	TCLK3	NC	VDDDIO	VDDDC	VDDDC	VDDDC	VDDDC	VDDDC	VDDDC	VDDDIO	GNDA	GNDA	VDDAX7	TTIP7
L	TCLK2	NC	TCLK1	CV8/RDN8	RD8/RDP8	VDDDC	VDDDC	VDDDC	VDDDC	VDDDC	VDDDC	VDDDIO	RTIP7	GNDA	GNDA	TRING7
M	CV7/RDN7	RD7/RDP7	CV6/RDN6	RD6/RDP6	LOS5	RCLK3	A0	A5	D4	D0/SDO	MPM	VDDDIO	RRING7	GNDA	VDDAR7	VDDAT7
N	CV5/RDN5	RD5/RDP5	CV4/RDN4	LOS7	RCLK5	LOS2	A1	A6	D5	$\overline{\text{DS}}$/$\overline{\text{RD}}$/SCLK	SPIEN	GNDD	GNDA	RTIP8	RRING8	VDDAR8
P	RD4/RDP4	CV3/RDN3	RD1/RDP1	RCLK7	LOS4	RCLK2	A2	A7	A10	D3	R$\overline{\text{W}}$/$\overline{\text{WR}}$/SDI	GNDD	GNDA	GNDA	GNDA	VDDAT8
R	RD3/RDP3	RD2/RDP2	LOS8	LOS6	RCLK4	LOS1	A3	A8	D7	D2	$\overline{\text{CS}}$	VDDDIO	$\overline{\text{TRST}}$	TDO	VDDAX8	TRING8
T	CV2/RDN2	CV1/RDN1	RCLK8	RCLK6	LOS3	RCLK1	A4	A9	D6	D1	$\overline{\text{INT}}$	GNDD	TDI	TMS	TCK	TTIP8

Figure-2 IDT82P5088 CABGA256 Package Pin Assignment (top view)

© 2019 Renesas Electronics Corporation

2 PIN DESCRIPTION

Table-1 Pin Description

Name	Type	Pin No. PBGA256	Description
Transmit and Receive Line Interface			
TTIP1 TTIP2 TTIP3 TTIP4 TTIP5 TTIP6 TTIP7 TTIP8 TRING1 TRING2 TRING3 TRING4 TRING5 TRING6 TRING7 TRING8	Output Analog	A12 A8 A7 A1 E16 J16 K16 T16 A11 A9 A6 A2 F16 H16 L16 R16	TTIPn[1]/TRINGn: Transmit Bipolar Tip/Ring for Channel 1~8 These pins are the differential line driver outputs and can be set to high impedance state globally or individually. A logic high on THZ pin turns all these pins into high impedance state. When THZ bit (TCF1, 23H...)[2] is set to '1', the TTIPn/TRINGn in the corresponding channel is set to high impedance state. In summary, these pins will become high impedance in the following conditions: • THZ pin is high: all TTIPn/TRINGn enter high impedance; • THZn bit is set to 1: the corresponding TTIPn/TRINGn become high impedance; • Loss of MCLK: all TTIPn/TRINGn pins become high impedance;· • Loss of TCLKn: the corresponding TTIPn/TRINGn become HZ (exceptions: Remote Loopback; Transmit internal pattern by MCLK); • Transmitter path power down: the corresponding TTIPn/TRINGn become high impedance; • After software reset; pin reset and power on: all TTIPn/TRINGn enter high impedance.
RTIP1 RTIP2 RTIP3 RTIP4 RTIP5 RTIP6 RTIP7 RTIP8 RRING1 RRING2 RRING3 RRING4 RRING5 RRING6 RRING7 RRING8	Input Analog	C11 D8 D6 B4 F14 J13 L13 N14 D11 D9 D5 C4 G14 H13 M13 N15	RTIPn/RRINGn: Receive Bipolar Tip/Ring for Channel 1~8 These pins are the differential line receiver inputs.

Notes:

1. The footprint 'n' (n = 1~8) represents one of the eight channels.
2. The name and address of the registers that contain the preceding bit. Only the address of channel 1 register is listed, the rest addresses are represented by '...'. Users can find these omitted addresses in the *Register Description* section.

© 2019 Renesas Electronics Corporation

Table-1 Pin Description (Continued)

<table>
<tr><th>Name</th><th>Type</th><th>Pin No.
PBGA256</th><th>Description</th></tr>
<tr><td colspan="4">Transmit and Receive Digital Data Interface</td></tr>
<tr><td>TD1/TDP1
TD2/TDP2
TD3/TDP3
TD4/TDP4
TD5/TDP5
TD6/TDP6
TD7/TDP7
TD8/TDP8

TDN1
TDN2
TDN3
TDN4
TDN5
TDN6
TDN7
TDN8</td><td>Input</td><td>G2
G4
F2
F4
E2
E4
D2
C2

G3
F1
F3
E1
E3
D1
C1
B1</td><td>TDn: Transmit Data for Channel 1~8
In Single Rail Mode, the NRZ data to be transmitted is input on these pins. Data on TDn is sampled into the device on the active edge of TCLKn. The active edge of TCLKn is selected by the TCLK_SEL bit (TCF0, 22H...). Data is encoded by AMI, HDB3 or B8ZS line code rules before being transmitted to the line. In this mode, TDNn should be connected to ground.

TDPn/TDNn: Positive/Negative Transmit Data for Channel 1~8
In Dual Rail Mode, the NRZ data to be transmitted is input on these pins. Data on TDPn/TDNn is sampled into the device on the active edge of TCLKn. The active edge of the TCLKn is selected by the TCLK_SEL bit (TCF0, 22H...)
The line code in Dual Rail Mode is as follows:
<table>
<tr><th>TDPn</th><th>TDNn</th><th>Output Pulse</th></tr>
<tr><td>0</td><td>0</td><td>Space</td></tr>
<tr><td>0</td><td>1</td><td>Positive Pulse</td></tr>
<tr><td>1</td><td>0</td><td>Negative Pulse</td></tr>
<tr><td>1</td><td>1</td><td>Space</td></tr>
</table>
</td></tr>
<tr><td>TCLK1
TCLK2
TCLK3
TCLK4
TCLK5
TCLK6
TCLK7
TCLK8</td><td>Input</td><td>L3
L1
K3
K1
J3
J1
H2
H4</td><td>TCLKn: Transmit Clock for Channel 1~8
These pins input 1.544 MHz for T1/J1 mode or 2.048 MHz for E1 mode transmit clock. The transmit data on TDn orTDPn/TDNn is sampled into the device on the active edge of TCLKn. If TCLKn is missing[1] and the TCLKn missing interrupt is not masked, an interrupt will be generated.</td></tr>
<tr><td>RD1/RDP1
RD2/RDP2
RD3/RDP3
RD4/RDP4
RD5/RDP5
RD6/RDP6
RD7/RDP7
RD8/RDP8

CV1/RDN1
CV2/RDN2
CV3/RDN3
CV4/RDN4
CV5/RDN5
CV6/RDN6
CV7/RDN7
CV8/RDN8</td><td>Output</td><td>P3
R2
R1
P1
N2
M4
M2
L5

T2
T1
P2
N3
N1
M3
M1
L4</td><td>RDn: Receive Data for Channel 1~8
In Single Rail Mode, the NRZ receive data is output on these pins. Data is decoded according to AMI, HDB3 or B8ZS line code rules. The active level on RDn pin is selected by the RD_INV bit (RCF0, 28H...).

CVn: Code Violation for Channel 1~8
In Single Rail Mode, the BPV/CV errors in received data streams will be reported by driving pin CVn to high level for a full clock cycle. The B8ZS/HDB3 line code violation can be indicated when the B8ZS/HDB3 decoder is enabled. When AMI decoder is selected, the bipolar violation can be indicated.

RDPn/RDNn: Positive/Negative Receive Data for Channel 1~8
In Dual Rail Mode with Clock & Data Recovery (CDR), these pins output the NRZ data with the recovered clock. An active level on RDPn indicates the receipt of a positive pulse on RTIPn/RRINGn while an active level on RDNn indicates the receipt of a negative pulse on RTIPn/RRINGn. The active level on RDPn/RDNn is selected by the RD_INV bit (RCF0, 28H...). When CDR is disabled, these pins directly output the raw RZ sliced data. The output data on RDn and RDPn/RDNn is updated on the active edge of RCLKn.</td></tr>
<tr><td>RCLK1
RCLK2
RCLK3
RCLK4
RCLK5
RCLK6
RCLK7
RCLK8</td><td>Output</td><td>T6
P6
M6
R5
N5
T4
P4
T3</td><td>RCLKn: Receive Clock for Channel 1~8
These pins output 1.544 MHz for T1/J1 mode or 2.048 MHz for E1 mode receive clock. Under LOS conditions, if RAISE bit (MAINT1, 2CH...) is ‘1’, RCLKn is derived from MCLK.
In clock recovery mode, these pins provide the clock recovered from the signal received on RTIPn/RRINGn. The receive data (RDn in Single Rail Mode or RDPn/RDNn in Dual Rail Mode) is updated on the active edge of RCLKn. The active edge is selected by the RCLK_SEL bit (RCF0, 28H...).
If clock recovery is bypassed, RCLKn is the exclusive OR(XOR) output of the Dual Rail sliced data RDPn and RDNn. This signal can be used in the applications with external clock recovery circuitry.</td></tr>
</table>

Notes:

1. TCLKn missing: the state of TCLKn continues to be high level or low level over 70 clock cycles.

© 2019 Renesas Electronics Corporation

Table-1 Pin Description (Continued)

Name	Type	Pin No. PBGA256	Description
LOS1 LOS2 LOS3 LOS4 LOS5 LOS6 LOS7 LOS8	Output	R6 N6 T5 P5 M5 R4 N4 R3	LOSn: Loss of Signal Output for Channel 1~8 These pins are used to indicate the loss of received signals. When LOSn pin becomes high, it indicates the loss of received signals in channel n. The LOSn pin will become low automatically when valid received signal is detected again. The criteria of loss of signal are described in 3.3.12 LOS AND AIS DETECTION.
Clock Generator			
OSCI	Input	B13	OSCI: Crystal Oscillator Input This pin is connected to an external clock source. The clock frequency of OSCI is defined by CLK_SEL[2:0]. The clock accuracy should be ±32 ppm and duty cycle should be from 40% to 60%.
OSCO	Output	C13	OSCO: Crystal Oscillator Output This pin outputs the inverted, buffered clock input from OSCI.
CLK_SEL[0] CLK_SEL[1] CLK_SEL[2]	Input	D15 C14 B15	CLK_SEL[2:0]: Clock Selection These three pins select the input clock signal: When the CLK_SEL[2] pin is low, the input clock signal is N X 1.544 MHz; When the CLK_SEL[2] pin is high, the input clock signal is N X 2.048 MHz. When the CLK_SEL[1:0] pins are '00', the N is 1; When the CLK_SEL[1:0] pins are '01', the N is 2; When the CLK_SEL[1:0] pins are '10', the N is 3; When the CLK_SEL[1:0] pins are '11', the N is 4. CLK_SEL[2:0] are Schmitt-trigger inputs.
CLK_- GEN_1.544	Output	A16	CLK_GEN_1.544: Clock Generator 1.544 MHz Output This pin outputs the 1.544 MHz clock signal generated by the Clock Generator.
CLK_- GEN_2.048	Output	D14	CLK_GEN_2.048: Clock Generator 2.048 MHz Output This pin outputs the 2.048 MHz clock signal generated by the Clock Generator.
REFA_OUT	Output	A15	REFA_OUT: Reference Clock Output A The frequecy is 2.048 MHz (E1) or 1.544 MHz (T1/J1) When no LOS is detected, this pin outputs a recovered clock from the Clock and Data Recovery function block of one of the eight links. The link is selected by the RO1[2:0] bits (REFOUT, 07H). When LOS is detected, this pin outputs MCLK or high level, as selected by the REFH_LOS bit (REFC, 3EH...). Note: MCLK is a clock derived from OSCI using an internal PLL, and the frequency is 2.048 MHz (E1) or 1.544 MHz (T1/J1).
REFB_OUT	Output	B14	REFB_OUT: Reference Clock Output B The frequecy is 2.048 MHz (E1) or 1.544 MHz (T1/J1) When no LOS is detected, this pin outputs a recovered clock from the Clock and Data Recovery function block of one of the eight links. The link is selected by the RO2[2:0] bits (REFOUT, 07H). When LOS is detected, this pin outputs MCLK or high level, as selected by the REFH_LOS bit (REFC, 3EH...).
Control Interface			
$\overline{\text{RESET}}$	Input	A14	**$\overline{\text{RESET}}$**: Reset (Active Low) A low pulse for more than 100 ns on this pin resets the device. All the registers are accessible 2 ms after the reset. The $\overline{\text{RESET}}$ pin is a Schmitt-trigger input with a weak pull-up resistor. The OSCI clock must exist when the device is reset.
GPIO0 GPIO1	Output / Input	E13 D13	General Purpose I/O [1:0] These two pins can be defined as input pins or output pins by the DIR[1:0] bits (GPIO, 06H) respectively. When the pins are input, their polarities are indicated by the LEVEL[1:0] bits (GPIO, 06H) respectively. When the pins are output, their polarities are controlled by the LEVEL[1:0] bits (GPIO, 06H) respectively. GPIO[1:0] are Schmitt-trigger input/output with a pull-up resistor.

© 2019 Renesas Electronics Corporation

Table-1 Pin Description (Continued)

Name	Type	Pin No. PBGA256	Description
THZ	Input	B16	THZ: Transmit High-Z A high level on this pin puts all the TTIPn/TRINGn pins into high impedance state. THZ is a Schmitt-trigger input.
$\overline{\text{INT}}$	Output	T11	**$\overline{\text{INT}}$**: Interrupt (Active Low) This is the open drain, active low interrupt output. This pin will stay low until all the active unmasked interrupt indication bits are cleared.
REFR	Output	C16	REFR: This pin should be connected to ground via an external 10K resistor.
$\overline{\text{CS}}$	Input	R11	**$\overline{\text{CS}}$**: Chip Select (Active Low) This pin must be asserted low to enable the microprocessor interface. The signal must be asserted high at least once after power up to clear the internal test modes. A transition from high to low must occur on this pin for each Read/Write operation and can not return to high until the operation is completed. $\overline{\text{CS}}$ is a Schmitt-trigger input.
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10	Input	M7 N7 P7 R7 T7 M8 N8 P8 R8 T8 P9	A[10:0]: Address Bus In parallel mode, the signals on these pins select the register for the microprocessor to access. In SPI mode, these pins should be connected to ground. A[10:0] are Schmitt-trigger inputs.
D0 / SDO D1 D2 D3 D4 D5 D6 D7	Output / Input	M10 T10 R10 P10 M9 N9 T9 R9	D[7:0]: Bi-directional Data Bus In parallel mode, the signals on these pins are the data for Read / Write operation. In SPI mode, the D[7:1] pins should be connected to the ground through a 10 K resistor. D[7:0] are Schmitt-trigger inputs/outputs. SDO: Serial Data Output In SPI mode, the data is serially output on this pin.
MPM	Input	M11	MPM: Micro Controller Mode In parallel mode, set this pin low for Motorola mode or high for Intel mode. In SPI mode, set this pin to a fixed level (high or low). This pin is useless in SPI mode. MPM is a Schmitt-trigger input.
R**$\overline{\text{W}}$** / **$\overline{\text{WR}}$** / SDI	Input	P11	R**$\overline{\text{W}}$**: Read / Write Select In parallel Motorola mode, this pin is active high for read operation and active low for write operation. **$\overline{\text{WR}}$**: Write Strobe (Active Low) In parallel Intel mode, this pin is active low for write operation. SDI: Serial Data Input In SPI mode, the address/control and/or data are serially input on this pin. R$\overline{\text{W}}$ / $\overline{\text{WR}}$ / SDI is a Schmitt-trigger input.

© 2019 Renesas Electronics Corporation

Table-1 Pin Description (Continued)

Name	Type	Pin No. PBGA256	Description
$\overline{DS}$ / **$\overline{RD}$** / SCLK	Input	N10	**$\overline{DS}$**: Data Strobe (Active Low) In parallel Motorola mode, this pin is active low. **$\overline{RD}$**: Read Strobe (Active Low) In parallel Intel mode, this pin is active low for read operation. SCLK: Serial Clock In SPI mode, this pin inputs the timing for the SDO and SDI pins. The signal on the SDO pin is updated on the falling edge of SCLK, while the signal on the SDI pin is sampled on the rising edge of SCLK. $\overline{DS}$ / $\overline{RD}$ / SCLK is a Schmitt-trigger input.
SPIEN	Input	N11	SPIEN: Serial Microprocessor Interface Enable When this pin is low, the microprocessor interface is in parallel mode. When this pin is high, the microprocessor interface is in SPI mode. SPIEN is a Schmitt-trigger input.
JTAG Signals			
$\overline{TRST}$	Input	R13	**$\overline{TRST}$**: Test Reset (Active Low) A low signal on this pin resets the JTAG test port. This pin is a Schmitt-triggered input with an internal pull-up resistor. It must be connected to the $\overline{RESET}$ pin or ground when JTAG is not used.
TMS	Input	T14	TMS: Test Mode Select The signal on this pin controls the JTAG test performance and is sampled on the rising edge of TCK. This pin is a Schmitt-triggered input with an internal pull-up resistor.
TCK	Input	T15	TCK: Test Clock The clock for the JTAG test is input on this pin. TDI and TMS are sampled on the rising edge of TCK and TDO is clocked out of the device on the falling edge of TCK. This pin is a Schmitt-triggered input with an internal pull-up resistor.
TDI	Input	T13	TDI: Test Input The test data is sampled at this pin on the rising edge of TCK. This pin is a Schmitt-triggered input with an internal pull-up resistor.
TDO	High-Z	R14	TDO: Test Output The test data are output on this pin. It is updated on the falling edge of TCK. This pin is High-Z except during the process of data scanning.
Power Supplies and Grounds			
VDDDIO	Power	F5, G5, H5, J5, J12, K5, K12, L12, M12, R12	VDDDIO: 3.3 V I/O Power Supply
VDDDC	Power	H6, H7, H8, J6, J7, J8, J9, J10, J11, K6, K7, K8, K9, K10, K11, L6, L7, L8, L9, L10, L11	VDDDC: 1.8 V Digital Core Power Supply

© 2019 Renesas Electronics Corporation

Table-1 Pin Description (Continued)

Name	Type	Pin No.	Description
		PBGA256	
VDDAR[1] VDDAR[2] VDDAR[3] VDDAR[4] VDDAR[5] VDDAR[6] VDDAR[7] VDDAR[8]	Power	A10 C9 A5 A4 G16 H15 M15 N16	VDDAR[8:1]: 3.3 V Power Supply for Receiver
VDDAT[1] VDDAT[2] VDDAT[3] VDDAT[4] VDDAT[5] VDDAT[6] VDDAT[7] VDDAT[8]	Power	B12 B9 B5 A3 E15 H14 M16 P16	VDDAT[8:1]: 3.3 V Power Supply for Transmitter
VDDAX[1] VDDAX[2] VDDAX[3] VDDAX[4] VDDAX[5] VDDAX[6] VDDAX[7] VDDAX[8]	Power	C12 B8 B7 B2 E14 J15 K15 R15	VDDAX[8:1]: 3.3 V Power Supply for Transmit Driver
VDDAP	Power	A13	VDDAP: 3.3 V Power Analog PLL
VDDAB	Power	D12	VDDAB: 3.3 V Power Analog Bias
GNDD	Ground	C15, D16, E5, E6, E7, E8, E9, E10, E11, E12, F6, F7, F8, F9, F10, F11, F12, G6, G7, G8, G9, G10, G11, G12, H9, H10, H11, H12, N12, P12, T12	GNDD: Digital Ground

© 2019 Renesas Electronics Corporation

Table-1 Pin Description (Continued)

Name	Type	Pin No. PBGA256	Description
GNDA	Ground	B3, B6, B10, B11, C3, C5, C6, C7, C8, C10, D3, D4, D7, D10, F13, F15, G13, G15, J14, K13, K14, L14, L15, M14, N13, P13, P14, P15	GNDA: Analog Ground
Others			
NC	-	G1, H1, H3, J2, J4, K2, K4, L2	NC: No Connection No Connection. These pins are not internally connected.

© 2019 Renesas Electronics Corporation

3 FUNCTIONAL DESCRIPTION

3.1 T1/E1/J1 MODE SELECTION

The IDT82P5088 can be used as an eight-channel E1 LIU or an eight-channel T1/J1 LIU. In E1 application, the TEMODE bit (T1E1 mode, 20H...) should be set to '0'. In T1/J1 application, the T1E1 bit should be set to '1'.

3.2 TRANSMIT PATH

The transmit path of each channel of the IDT82P5088 consists of an Encoder, an Jitter Attenuator, a Waveform Shaper, a set of LBOs, a Line Driver and a Programmable Transmit Termination.

3.2.1 TRANSMIT PATH SYSTEM INTERFACE

The transmit path system interface consists of TCLKn pin, TDn/TDPn pin and TDNn pin. In E1 mode, the TCLKn is a 2.048 MHz clock. In T1/J1 mode, the TCLKn is a 1.544 MHz clock. If the TCLKn is missing for more than 70 MCLK cycles, an interrupt will be generated if it is not masked.

Transmit data is sampled on the TDn/TDPn and TDNn pins by the active edge of TCLKn. The active edge of TCLKn can be selected by the TCLK_SEL bit (TCF0, 22H...). And the active level of the data on TDn/TDPn and TDNn can be selected by the TD_INV bit (TCF0, 22H...).

The transmit data from the system side can be provided in two different ways: Single Rail and Dual Rail. In Single Rail mode, only TDn pin is used for transmitting data and the T_MD[1] bit (TCF0, 22H...) should be set to '0'. In Dual Rail Mode, both TDPn and TDNn pins are used for transmitting data, the T_MD[1] bit (TCF0, 22H...) should be set to '1'.

3.2.2 ENCODER

When T1/J1 mode is selected, in Single Rail mode, the Encoder can be selected to be a B8ZS encoder or an AMI encoder by setting T_MD[0] bit (TCF0, 22H...).

When E1 mode is selected, in Single Rail mode, the Encoder can be configured to be a HDB3 encoder or an AMI encoder by setting T_MD[0] bit (TCF0, 22H...).

In both T1/J1 mode and E1 mode, when Dual Rail mode is selected (bit T_MD[1] is '1'), the Encoder is by-passed. In the Dual Rail mode, a logic '1' on the TDPn pin and a logic '0' on the TDNn pin results in a negative pulse on the TTIPn/TRINGn; a logic '0' on TDPn pin and a logic '1' on TDNn pin results in a positive pulse on the TTIPn/TRINGn. If both TDPn and TDNn are logic '1' or logic '0', the TTIPn/TRINGn outputs a space (Refer to TDn, TDPn/TDNn Pin Description).

3.2.3 PULSE SHAPER

The IDT82P5088 provides three ways of manipulating the pulse shape before sending it. The first is to use preset pulse templates for short haul application, the second is to use LBO (Line Build Out) for long haul application and the other way is to use user-programmable arbitrary waveform template.

3.2.3.1 Preset Pulse Templates

For E1 applications, the pulse shape is shown in Figure-3 according to the G.703 and the measuring diagram is shown in Figure-4. In internal impedance matching mode, if the cable impedance is 75 Ω, the PULS[3:0] bits (TCF1, 23H...) should be set to '0000'; if the cable impedance is 120 Ω, the PULS[3:0] bits (TCF1, 23H...) should be set to '0001'. In external impedance matching mode, for both E1/75 Ω and E1/120 Ω cable impedance, PULS[3:0] should be set to '0001'.

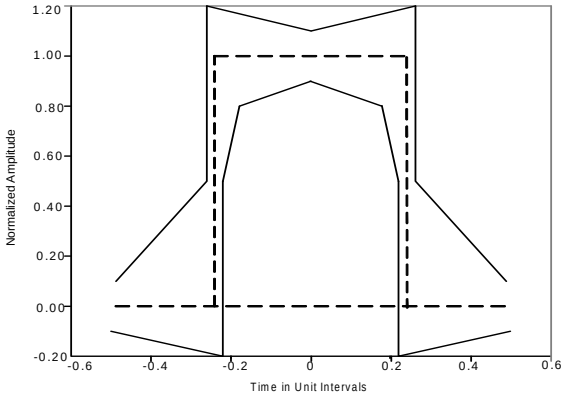


Figure-3 E1 Waveform Template Diagram

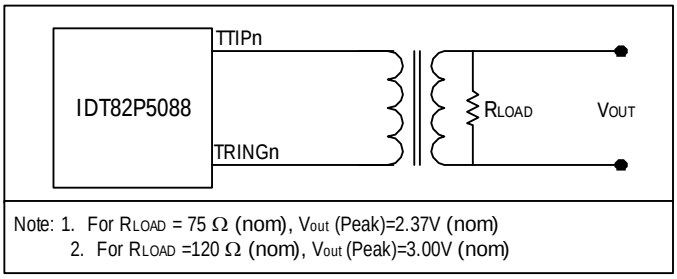


Figure-4 E1 Pulse Template Test Circuit

For T1 applications, the pulse shape is shown in Figure-5 according to the T1.102 and the measuring diagram is shown in Figure-6. This also meets the requirement of G.703, 2001. The cable length is divided into five grades, and there are five pulse templates used for each of the cable length. The pulse template is selected by PULS[3:0] bits (TCF1, 23H...).

© 2019 Renesas Electronics Corporation

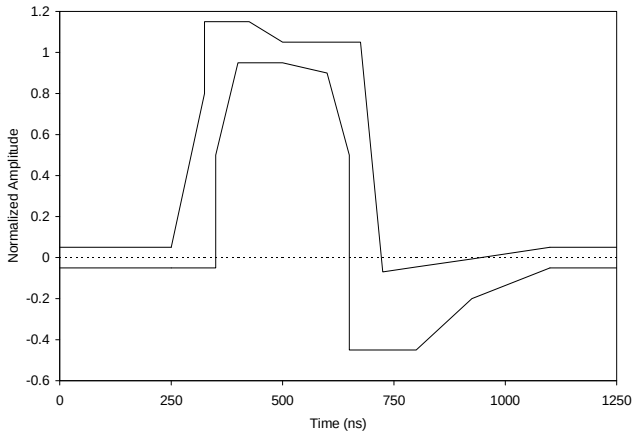


Figure-5 DSX-1 Waveform Template

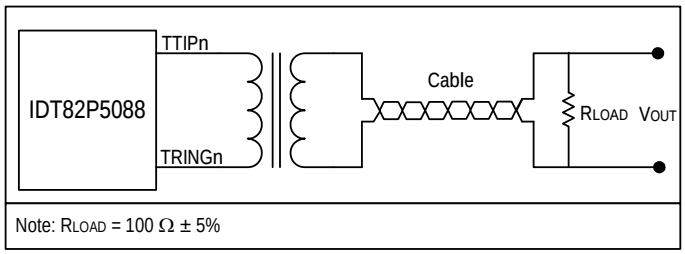


Figure-6 T1 Pulse Template Test Circuit

For J1 applications, the PULS[3:0] (TCF1, 23H...) should be set to '0111'. Table-14 lists these values.

3.2.3.2 LBO (Line Build Out)

To prevent the cross-talk at the far end, the output of TTIP/TRING could be attenuated before transmission for long haul applications. The FCC Part 68 Regulations specifies four grades of attenuation with a step of 7.5 dB. Three LBOs are used to implement the pulse attenuation. The PULS[3:0] bits (TCF1, 23H...) are used to select the attenuation grade. Both Table-14 and Table-16 list these values.

3.2.3.3 User-Programmable Arbitrary Waveform

When the PULS[3:0] bits are set to '11xx', user-programmable arbitrary waveform generator mode can be used in the corresponding channel. This allows the transmitter performance to be tuned for a wide variety of line condition or special application.

Each pulse shape can extend up to 4 UIs (Unit Interval), addressed by UI[1:0] bits (TCF3, 25H...) and each UI is divided into 16 sub-phases, addressed by the SAMP[3:0] bits (TCF3, 25H...). The pulse amplitude of each phase is represented by a binary byte, within the range from +63 to -63, stored in WDAT[6:0] bits (TCF4, 26H...) in signed magnitude form. The most positive number +63 (D) represents the maximum positive amplitude of the transmit pulse while the most negative number -63 (D) represents the maximum negative amplitude of the transmit pulse. Therefore, up to 64 bytes are used. For each channel, a 64 bytes RAM is available.

There are twelve standard templates which are stored in a local ROM. User can select one of them as reference and make some changes to get the desired waveform.

User can change the wave shape and the amplitude to get the desired pulse shape. In order to do this, firstly, users can choose a set of waveform value from the following twelve tables, which is the most similar to the desired pulse shape. Table-2, Table-3, Table-4, Table-5, Table-6, Table-7, Table-8, Table-9, Table-10, Table-11, Table-12 and Table-13 list the sample data and scaling data of each of the twelve templates. Then modify the corresponding sample data to get the desired transmit pulse shape.

Secondly, through the value of SCAL[5:0] bits increased or decreased by 1, the pulse amplitude can be scaled up or down at the percentage ratio against the standard pulse amplitude if needed. For different pulse shapes, the value of SCAL[5:0] bits and the scaling percentage ratio are different. The following twelve tables list these values.

Do the followings step by step, the desired waveform can be programmed, based on the selected waveform template:

(1).Select the UI by UI[1:0] bits (TCF3, 25H...)

(2).Specify the sample address in the selected UI by SAMP [3:0] bits (TCF3, 25H...)

(3).Write sample data to WDAT[6:0] bits (TCF4, 26H...). It contains the data to be stored in the RAM, addressed by the selected UI and the corresponding sample address.

(4).Set the RW bit (TCF3, 25H...) to '0' to implement writing data to RAM, or to '1' to implement read data from RAM

(5).Implement the Read from RAM/Write to RAM by setting the DONE bit (TCF3, 25H...)

Repeat the above steps until all the sample data are written to or read from the internal RAM.

(6).Write the scaling data to SCAL[5:0] bits (TCF2, 24H...) to scale the amplitude of the waveform based on the selected standard pulse amplitude

When more than one UI is used to compose the pulse template, the overlap of two consecutive pulses could make the pulse amplitude overflow (exceed the maximum limitation) if the pulse amplitude is not set properly. This overflow is captured by DAC_IS bit (INTS1, 3BH...), and, if enabled by the DAC_IE bit (INTENC1, 34H...), an interrupt will be generated.

The following tables give all the sample data based on the preset pulse templates and LBOs in detail for reference. For preset pulse templates and LBOs, scaling up/down against the pulse amplitude is not supported.

1.Table-2 Transmit Waveform Value For E1 75 Ω
2.Table-3 Transmit Waveform Value For E1 120 Ω
3.Table-4 Transmit Waveform Value For T1 0~133 ft
4.Table-5 Transmit Waveform Value For T1 133~266 ft
5.Table-6 Transmit Waveform Value For T1 266~399 ft
6.Table-7 Transmit Waveform Value For T1 399~533 ft
7.Table-8 Transmit Waveform Value For T1 533~655 ft
8.Table-9 Transmit Waveform Value For J1 0~655 ft
9.Table-10 Transmit Waveform Value For DS1 0 dB LBO
10.Table-11 Transmit Waveform Value For DS1 -7.5 dB LBO
11.Table-12 Transmit Waveform Value For DS1 -15.0 dB LBO

© 2019 Renesas Electronics Corporation

12.Table-13 Transmit Waveform Value For DS1 -22.5 dB LBO

Table-2 Transmit Waveform Value For E1 75 Ω

Sample	UI 1	UI 2	UI 3	UI 4
1	0000000	0000000	0000000	0000000
2	0000000	0000000	0000000	0000000
3	0000000	0000000	0000000	0000000
4	0001100	0000000	0000000	0000000
5	0110000	0000000	0000000	0000000
6	0110000	0000000	0000000	0000000
7	0110000	0000000	0000000	0000000
8	0110000	0000000	0000000	0000000
9	0110000	0000000	0000000	0000000
10	0110000	0000000	0000000	0000000
11	0110000	0000000	0000000	0000000
12	0110000	0000000	0000000	0000000
13	0000000	0000000	0000000	0000000
14	0000000	0000000	0000000	0000000
15	0000000	0000000	0000000	0000000
16	0000000	0000000	0000000	0000000

SCAL[5:0] = 100001 (default), One step change of this value of SCAL[5:0] results in 3% scaling up/down against the pulse amplitude.

Table-3 Transmit Waveform Value For E1 120 Ω

Sample	UI 1	UI 2	UI 3	UI 4
1	0000000	0000000	0000000	0000000
2	0000000	0000000	0000000	0000000
3	0000000	0000000	0000000	0000000
4	0001111	0000000	0000000	0000000
5	0111100	0000000	0000000	0000000
6	0111100	0000000	0000000	0000000
7	0111100	0000000	0000000	0000000
8	0111100	0000000	0000000	0000000
9	0111100	0000000	0000000	0000000
10	0111100	0000000	0000000	0000000
11	0111100	0000000	0000000	0000000
12	0111100	0000000	0000000	0000000
13	0000000	0000000	0000000	0000000
14	0000000	0000000	0000000	0000000
15	0000000	0000000	0000000	0000000
16	0000000	0000000	0000000	0000000

SCAL[5:0] = 100001 (default), One step change of this value of SCAL[5:0] results in 3% scaling up/down against the pulse amplitude.

Table-4 Transmit Waveform Value For T1 0~133 ft

Sample	UI 1	UI 2	UI 3	UI 4
1	0010111	1000010	0000000	0000000
2	0100111	1000001	0000000	0000000
3	0100111	0000000	0000000	0000000
4	0100110	0000000	0000000	0000000
5	0100101	0000000	0000000	0000000
6	0100101	0000000	0000000	0000000
7	0100101	0000000	0000000	0000000
8	0100100	0000000	0000000	0000000
9	0100011	0000000	0000000	0000000
10	1001010	0000000	0000000	0000000
11	1001010	0000000	0000000	0000000
12	1001001	0000000	0000000	0000000
13	1000111	0000000	0000000	0000000
14	1000101	0000000	0000000	0000000
15	1000100	0000000	0000000	0000000
16	1000011	0000000	0000000	0000000

SCAL[5:0] = 110110[1] (default), One step change of this value of SCAL[5:0] results in 2% scaling up/down against the pulse amplitude.
1. In T1 mode, when arbitrary pulse for short haul application is configured, users should write '110110' to SCAL[5:0] bits if no scaling is required.

Table-5 Transmit Waveform Value For T1 133~266 ft

Sample	UI 1	UI 2	UI 3	UI 4
1	0011011	1000011	0000000	0000000
2	0101110	1000010	0000000	0000000
3	0101100	1000001	0000000	0000000
4	0101010	0000000	0000000	0000000
5	0101001	0000000	0000000	0000000
6	0101000	0000000	0000000	0000000
7	0100111	0000000	0000000	0000000
8	0100110	0000000	0000000	0000000
9	0100101	0000000	0000000	0000000
10	1010000	0000000	0000000	0000000
11	1001111	0000000	0000000	0000000
12	1001101	0000000	0000000	0000000
13	1001010	0000000	0000000	0000000
14	1001000	0000000	0000000	0000000
15	1000110	0000000	0000000	0000000
16	1000100	0000000	0000000	0000000

See Table-4

© 2019 Renesas Electronics Corporation

Table-6 Transmit Waveform Value For T1 266~399 ft

Sample	UI 1	UI 2	UI 3	UI 4
1	0011111	1000011	0000000	0000000
2	0110100	1000010	0000000	0000000
3	0101111	1000001	0000000	0000000
4	0101100	0000000	0000000	0000000
5	0101011	0000000	0000000	0000000
6	0101010	0000000	0000000	0000000
7	0101001	0000000	0000000	0000000
8	0101000	0000000	0000000	0000000
9	0100101	0000000	0000000	0000000
10	1010111	0000000	0000000	0000000
11	1010011	0000000	0000000	0000000
12	1010000	0000000	0000000	0000000
13	1001011	0000000	0000000	0000000
14	1001000	0000000	0000000	0000000
15	1000110	0000000	0000000	0000000
16	1000100	0000000	0000000	0000000
See Table-4				

Table-7 Transmit Waveform Value For T1 399~533 ft

Sample	UI 1	UI 2	UI 3	UI 4
1	0100000	1000011	0000000	0000000
2	0111011	1000010	0000000	0000000
3	0110101	1000001	0000000	0000000
4	0101111	0000000	0000000	0000000
5	0101110	0000000	0000000	0000000
6	0101101	0000000	0000000	0000000
7	0101100	0000000	0000000	0000000
8	0101010	0000000	0000000	0000000
9	0101000	0000000	0000000	0000000
10	1011000	0000000	0000000	0000000
11	1011000	0000000	0000000	0000000
12	1010011	0000000	0000000	0000000
13	1001100	0000000	0000000	0000000
14	1001000	0000000	0000000	0000000
15	1000110	0000000	0000000	0000000
16	1000100	0000000	0000000	0000000
See Table-4				

Table-8 Transmit Waveform Value For T1 533~655 ft

Sample	UI 1	UI 2	UI 3	UI 4
1	0100000	1000011	0000000	0000000
2	0111111	1000010	0000000	0000000
3	0111000	1000001	0000000	0000000
4	0110011	0000000	0000000	0000000
5	0101111	0000000	0000000	0000000
6	0101110	0000000	0000000	0000000
7	0101101	0000000	0000000	0000000
8	0101100	0000000	0000000	0000000
9	0101001	0000000	0000000	0000000
10	1011111	0000000	0000000	0000000
11	1011110	0000000	0000000	0000000
12	1010111	0000000	0000000	0000000
13	1001111	0000000	0000000	0000000
14	1001001	0000000	0000000	0000000
15	1000111	0000000	0000000	0000000
16	1000100	0000000	0000000	0000000
See Table-4				

Table-9 Transmit Waveform Value For J1 0~655 ft

Sample	UI 1	UI 2	UI 3	UI 4
1	0010111	1000010	0000000	0000000
2	0100111	1000001	0000000	0000000
3	0100111	0000000	0000000	0000000
4	0100110	0000000	0000000	0000000
5	0100101	0000000	0000000	0000000
6	0100101	0000000	0000000	0000000
7	0100101	0000000	0000000	0000000
8	0100100	0000000	0000000	0000000
9	0100011	0000000	0000000	0000000
10	1001010	0000000	0000000	0000000
11	1001010	0000000	0000000	0000000
12	1001001	0000000	0000000	0000000
13	1000111	0000000	0000000	0000000
14	1000101	0000000	0000000	0000000
15	1000100	0000000	0000000	0000000
16	1000011	0000000	0000000	0000000
SCAL[5:0] = 110110 (default), One step change of this value of SCAL[5:0] results in 2% scaling up/down against the pulse amplitude.				

© 2019 Renesas Electronics Corporation

Table-10 Transmit Waveform Value For DS1 0 dB LBO

Sample	UI 1	UI 2	UI 3	UI 4
1	0010111	1000010	0000000	0000000
2	0100111	1000001	0000000	0000000
3	0100111	0000000	0000000	0000000
4	0100110	0000000	0000000	0000000
5	0100101	0000000	0000000	0000000
6	0100101	0000000	0000000	0000000
7	0100101	0000000	0000000	0000000
8	0100100	0000000	0000000	0000000
9	0100011	0000000	0000000	0000000
10	1001010	0000000	0000000	0000000
11	1001010	0000000	0000000	0000000
12	1001001	0000000	0000000	0000000
13	1000111	0000000	0000000	0000000
14	1000101	0000000	0000000	0000000
15	1000100	0000000	0000000	0000000
16	1000011	0000000	0000000	0000000

SCAL[5:0] = 110110 (default), One step change of this Value results in 2% scaling up/down against the pulse amplitude.

Table-11 Transmit Waveform Value For DS1 -7.5 dB LBO

Sample	UI 1	UI 2	UI 3	UI 4
1	0000000	0010100	0000010	0000000
2	0000010	0010010	0000010	0000000
3	0001001	0010000	0000010	0000000
4	0010011	0001110	0000010	0000000
5	0011101	0001100	0000010	0000000
6	0100101	0001011	0000001	0000000
7	0101011	0001010	0000001	0000000
8	0110001	0001001	0000001	0000000
9	0110110	0001000	0000001	0000000
10	0111010	0000111	0000001	0000000
11	0111001	0000110	0000001	0000000
12	0110000	0000101	0000001	0000000
13	0101000	0000100	0000000	0000000
14	0100000	0000100	0000000	0000000
15	0011010	0000011	0000000	0000000
16	0010111	0000011	0000000	0000000

SCAL[5:0] = 010001 (default), One step change of this value of SCAL[5:0] results in 6.25% scaling up/down against the pulse amplitude.

Table-12 Transmit Waveform Value For DS1 -15.0 dB LBO

Sample	UI 1	UI 2	UI 3	UI 4
1	0000000	0110101	0001111	0000011
2	0000000	0110011	0001101	0000010
3	0000000	0110000	0001100	0000010
4	0000001	0101101	0001011	0000010
5	0000100	0101010	0001010	0000010
6	0001000	0100111	0001001	0000001
7	0001110	0100100	0001000	0000001
8	0010100	0100001	0000111	0000001
9	0011011	0011110	0000110	0000001
10	0100010	0011100	0000110	0000001
11	0101010	0011010	0000101	0000001
12	0110000	0010111	0000101	0000001
13	0110101	0010101	0000100	0000001
14	0110111	0010100	0000100	0000000
15	0111000	0010010	0000011	0000000
16	0110111	0010000	0000011	0000000

SCAL[5:0] = 001000 (default), One step change of the value of SCAL[5:0] results in 12.5% scaling up/down against the pulse amplitude.

Table-13 Transmit Waveform Value For DS1 -22.5 dB LBO

Sample	UI 1	UI 2	UI 3	UI 4
1	0000001	0110101	0011011	0000111
2	0000011	0110101	0011001	0000110
3	0000101	0110100	0010111	0000110
4	0001000	0110011	0010101	0000101
5	0001100	0110010	0010100	0000101
6	0010001	0110000	0010010	0000101
7	0010110	0101110	0010001	0000100
8	0011011	0101101	0010000	0000100
9	0100001	0101011	0001110	0000100
10	0100110	0101001	0001101	0000100
11	0101010	0100111	0001100	0000011
12	0101110	0100100	0001011	0000011
13	0110001	0100010	0001010	0000011
14	0110011	0100000	0001001	0000011
15	0110100	0011110	0001000	0000011
16	0110100	0011100	0001000	0000010

SCAL[5:0] = 000100 (default), One step change of this value of SCAL[5:0] results in 25% scaling up/down against the pulse amplitude.

© 2019 Renesas Electronics Corporation

3.2.4 TRANSMIT PATH LINE INTERFACE

The transmit line interface consists of TTIPn pin and TRINGn pin. The impedance matching can be realized by the internal impedance matching circuit or the external impedance matching circuit. If T_TERM[2] is set to '0', the internal impedance matching circuit will be selected. In this case, the T_TERM[1:0] bits (TERM, 32H...) can be set to choose 75 Ω, 100 Ω, 110 Ω or 120 Ω internal impedance of TTIPn/TRINGn. If T_TERM[2] is set to '1', the internal impedance matching circuit will be disabled. In this case, the external impedance matching circuit will be used to realize the impedance matching. For T1/J1 mode, the external impedance matching circuit for the transmitter is not supported. Figure-9 shows the appropriate external components to connect with the cable for one channel. Table-14 is the list of the recommended impedance matching for transmitter.

The TTIPn/TRINGn can be turned into high impedance globally by pulling THZ pin to high or individually by setting the T_HZ bit (TCF1, 23H...) to '1'. In this state, the internal transmit circuits are still active.

Besides, in the following cases, TTIPn/TRINGn will also become high impedance:

- Loss of MCLK: all TTIPn/TRINGn pins become high impedance;·
- Loss of TCLKn: corresponding TTIPn/TRINGn become HZ (exceptions: Remote Loopback; Transmit internal pattern by MCLK);
- Transmit path power down;
- After software reset; pin reset and power on.

Table-14 Impedance Matching for Transmitter

Cable Configuration	Internal Termination			External Termination		
	T_TERM[2:0]	PULS[3:0]	R_T	T_TERM[2:0]	PULS[3:0]	R_T
E1/75 Ω	000	0000	0 Ω	1XX	0001	9.4 Ω
E1/120 Ω	001	0001			0001	
T1/0~133 ft	010	0010		-	-	-
T1/133~266 ft		0011				
T1/266~399 ft		0100				
T1/399~533 ft		0101				
T1/533~655 ft		0110				
J1/0~655 ft	011	0111				
0 dB LBO	010	1000				
-7.5 dB LBO		1001				
-15.0 dB LBO		1010				
-22.5 dB LBO		1011				

Note: The precision of the resistors should be better than ± 1%

3.2.5 TRANSMIT PATH POWER DOWN

The transmit path can be powered down individually by setting the T_OFF bit (TCF0, 22H...) to '1'. In this case, the TTIPn/TRINGn pins are turned into high impedance.

3.2.6 TRANSMIT JITTER ATTENUATOR

The Transmit Jitter Attenuator of each link can be chosen to be used or not. This selection is made by the TJA_E bit (TJACF, 21H...).

The Jitter Attenuator consists of a FIFO and a DPLL, as shown in Figure 7.

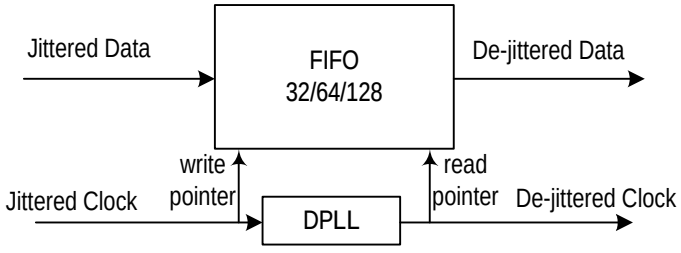


Figure-7 Jitter Attenuator

The FIFO is used as a pool to buffer the jittered input data, then the data is clocked out of the FIFO by a de-jittered clock. The depth of the FIFO can be 32 bits, 64 bits or 128 bits, as selected by the TJA_DP[1:0] bits (TJACF, 21H...). Accordingly, the constant delay produced by the Jitter Attenuator is 16 bits, 32 bits or 64 bits. The 128-bit FIFO is used when large jitter tolerance is expected, and the 32-bit FIFO is used in delay sensitive applications.

The DPLL is used to generate a de-jittered clock to clock out the data stored in the FIFO. The DPLL can only attenuate the incoming jitter whose frequency is above Corner Frequency (CF). The jitter which frequency is lower than the CF passes through the DPLL without any attenuation. In T1/J1 applications, the CF of the DPLL can be 5 Hz or 1.26 Hz, as selected by the TJA_BW bit (TJACF, 21H...). In E1 applications, the CF of the DPLL can be 6.77 Hz or 0.87 Hz, as selected by the TJA_BW bit (TJACF, 21H...). The lower the CF is, the longer time is needed to achieve synchronization.

If the incoming data moves faster than the outgoing data, the FIFO will overflow. If the incoming data moves slower than the outgoing data, the FIFO will underflow. The overflow or underflow is captured by the

© 2019 Renesas Electronics Corporation

TJA_IS bit. When the TJA_IS bit (INTS1, 3BH...) is '1', an interrupt will be reported on the $\overline{INT}$ pin if enabled by the TJA_IE bit (INTENC1, 34H...).

To avoid overflowing or underflowing, the JA-Limit function can be enabled by setting the TJA_LIMT bit (TJACF, 21H...). When the JA-Limit function is enabled, the speed of the outgoing data will be adjusted automatically if the FIFO is close to its full or emptiness. Though the LA-Limit function can reduce the possibility of FIFO overflow and underflow, the quality of jitter attenuation is deteriorated.

Selected by the TJITT_TEST bit (TJACF, 21H...), the real time interval between the read and write pointer of the FIFO or the peak-peak interval between the read and write pointer of the FIFO can be indicated in the TJITT[6:0] bits. When the TJITT_TEST bit is '0', the current interval between the read and write pointer of the FIFO will be written into the TJITT[6:0] bits. When the TJITT_TEST bit is '1', the current interval is compared with the old one in the TJITT[6:0] bits and the larger one will be indicated by the TJITT[6:0] bits.

The performance of Receive Jitter Attenuator meets the ITUT I.431, G.703, G.736 - 739, G.823, G.824, ETSI 300011, ETSI TBR 12/13, AT&T TR62411, TR43802, TR-TSY 009, TR-TSY 253, TR-TRY 499 standards. Refer to Chapter 6.9 Jitter Tolerance and Chapter 6.9 Jitter Tolerance for details.

Table-15 Related Bit / Register In Chapter 3.2.6

Bit	Register	Address (Hex)
TJA_E	Transmit Jitter Attenuation Configuration	X21H
TJA_DP[1:0]		
TJA_BW		
TJA_LIMT		
TJITT_TEST		
TJA_IS	Interrupt Status 1	X3BH
TJA_IE	Interrupt Enable Control 1	X34H
TJITT[6:0]	Transmit Jitter Measure Value Indication	X38H

© 2019 Renesas Electronics Corporation

3.3 RECEIVE PATH

The receive path consists of Receive Internal Termination, Monitor Gain, Amplitude/Wave Shape Detector, Digital Tuning Controller, Adaptive Equalizer, Data Slicer, CDR (Clock and Data Recovery), Jitter Attenuator, Decoder and LOS/AIS Detector. Refer to Figure-8.

3.3.1 RECEIVE INTERNAL TERMINATION

The impedance matching can be realized by the internal impedance matching circuit or the external impedance matching circuit. If R_TERM[2] is set to '0', the internal impedance matching circuit will be selected. In this case, the R_TERM[1:0] bits (TERM, 32H...) can be set to choose 75 Ω, 100 Ω, 110 Ω or 120 Ω internal impedance of RTIPn/RRINGn. If R_TERM[2] is set to '1', the internal impedance matching circuit will be disabled. In this case, the external impedance matching circuit will be used to realize the impedance matching.

Figure-9 shows the appropriate external components to connect with the cable for one channel. Table-16 is the list of the recommended impedance matching for receiver.

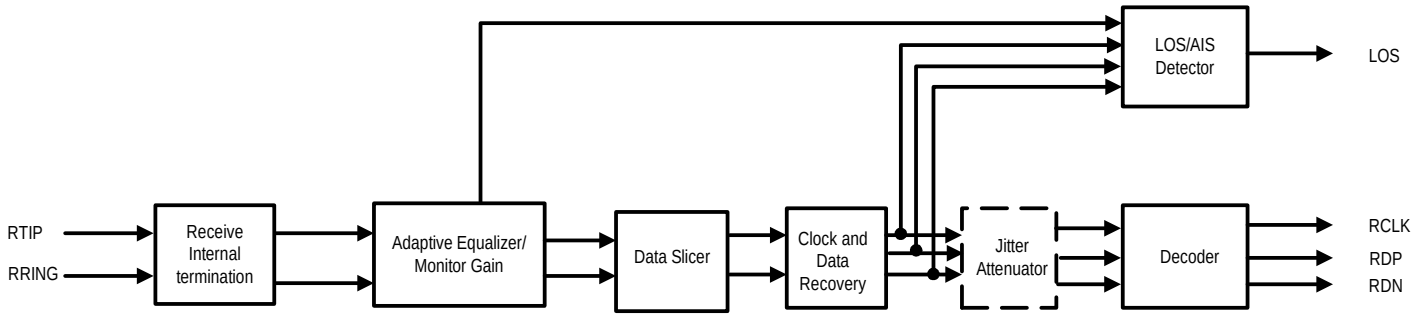
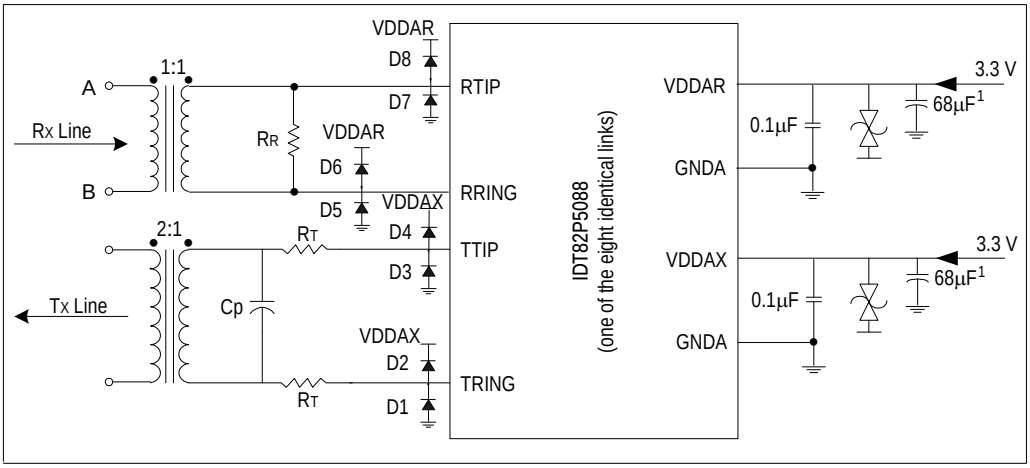


Figure-8 Receive Path Function Block Diagram

Table-16 Impedance Matching for Receiver

Cable Configuration	Internal Termination		External Termination	
	R_TERM[2:0]	R_R	R_TERM[2:0]	R_R
E1/75 Ω	000	120 Ω	1XX	75 Ω
E1/120 Ω	001			120 Ω
T1	010			100 Ω
J1	011			110 Ω



Note: 1. Common decoupling capacitor
2. Cp 0-560 (pF)
3. D1 - D8, Motorola - MBR0540T1; International Rectifier - 11DQ04 or 10BQ060

Figure-9 Transmit/Receive Line Circuit

© 2019 Renesas Electronics Corporation

3.3.2 LINE MONITOR

In both T1/J1 and E1 short haul applications, the non-intrusive monitoring on channels located in other chips can be performed by tapping the monitored channel through a high impedance bridging circuit. Refer to Figure-10 and Figure-11.

After a high resistance bridging circuit, the signal arriving at the RTIPn/RRINGn is dramatically attenuated. To compensate this attenuation, the Monitor Gain can be used to boost the signal by 22 dB, 26 dB and 32 dB, selected by MG[1:0] bits (RCF2, 2AH...). For normal operation, the Monitor Gain should be set to 0 dB.

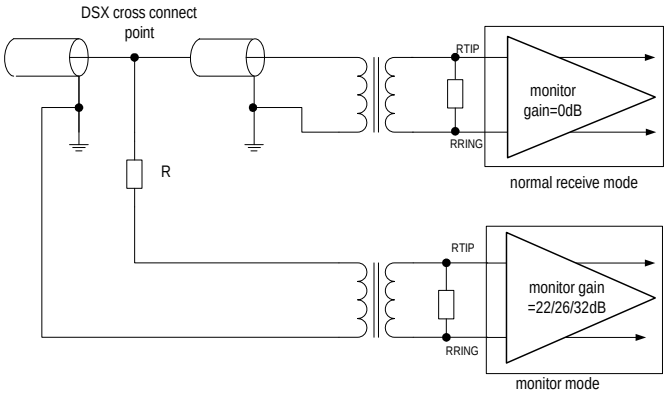


Figure-10 Monitoring Receive Line in Another Chip

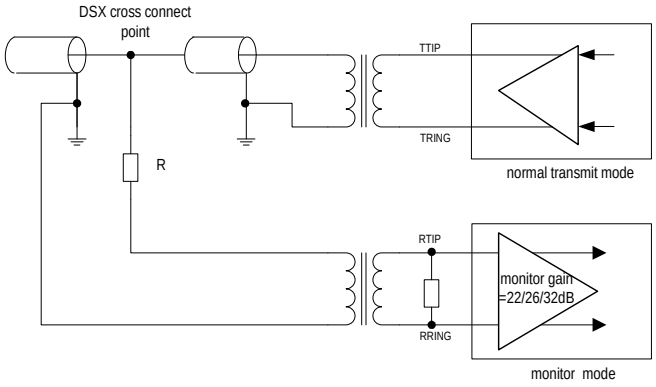


Figure-11 Monitor Transmit Line in Another Chip

3.3.3 ADAPTIVE EQUALIZER

The adaptive equalizer can remove most of the signal distortion due to intersymbol interference caused by cable attenuation. It can be enabled or disabled by setting EQ_ON bit to '1' or '0' (RCF1, 29H...).

The Amplitude/wave shape detector keeps on measuring the amplitude/wave shape of the incoming signals during an observation period. This observation period can be 32, 64, 128 or 256 symbol periods, as selected by UPDW[1:0] bits (RCF2, 2AH...). A shorter observation period allows quicker response to pulse amplitude variation while a longer observation period can minimize the possible overshoots. The default observation period is 128 symbol periods.

Based on the observed peak value for a period, the equalizer will be adjusted to achieve a normalized signal. LATT[4:0] bits (STAT1, 37H...) indicate the signal attenuation introduced by the cable in approximately 2 dB per step.

3.3.4 RECEIVE SENSITIVITY

For short haul application, the Receive Sensitivity for both E1 and T1/J1 is -10 dB. For long haul application, the receive sensitivity is -43 dB for E1 and -36 dB for T1/J1.

3.3.5 DATA SLICER

The Data Slicer is used to generate a standard amplitude mark or a space according to the amplitude of the input signals. The threshold can be 40%, 50%, 60% or 70%, as selected by the SLICE[1:0] bits (RCF2, 2AH...). The output of the Data Slicer is forwarded to the CDR (Clock & Data Recovery) unit or to the RDPn/RDNn pins directly if the CDR is disabled.

3.3.6 CDR (Clock & Data Recovery)

The CDR is used to recover the clock from the received signals. The recovered clock tracks the jitter in the data output from the Data Slicer and keeps the phase relationship between data and clock during the absence of the incoming pulse. The CDR can also be by-passed in the Dual Rail mode. When CDR is by-passed, the data from the Data Slicer is output to the RDPn/RDNn pins directly.

3.3.7 DECODER

In T1/J1 applications, the R_MD[1:0] bits (RCF0, 28H...) is used to select the AMI decoder or B8ZS decoder. In E1 applications, the R_MD[1:0] bits (RCF0, 28H...) are used to select the AMI decoder or HDB3 decoder.

3.3.8 RECEIVE PATH SYSTEM INTERFACE

The receive path system interface consists of RCLKn pin, RDn/RDPn pin and RDNn pin. In E1 mode, the RCLKn outputs a recovered 2.048 MHz clock. In T1/J1 mode, the RCLKn outputs a recovered 1.544 MHz clock. The received data is updated on the RDn/RDPn and RDNn pins on the active edge of RCLKn. The active edge of RCLKn can be selected by the RCLK_SEL bit (RCF0, 28H...). And the active level of the data on RDn/RDPn and RDNn can also be selected by the RD_INV bit (RCF0, 28H...).

The received data can be output to the system side in two different ways: Single Rail or Dual Rail, as selected by R_MD bit [1] (RCF0,28H...). In Single Rail mode, only RDn pin is used to output data and the RDNn/CVn pin is used to report the received errors. In Dual Rail Mode, both RDPn pin and RDNn pin are used for outputting data.

In the receive Dual Rail mode, the CDR unit can be by-passed by setting R_MD[1:0] to '11' (binary). In this situation, the output data from the Data Slicer will be output to the RDPn/RDNn pins directly, and the RCLKn outputs the exclusive OR (XOR) of the RDPn and RDNn.

3.3.9 RECEIVE PATH POWER DOWN

The receive path can be powered down individually by setting R_OFF bit (RCF0, 28H...) to '1'. In this case, the RCLKn, RDn/RDPn, RDPn and LOSn will be logic low.

© 2019 Renesas Electronics Corporation

3.3.10 G.772 NON-INTRUSIVE MONITORING

In applications using only seven channels, channel 1 can be configured to monitor the data received or transmitted in any one of the remaining channels. The MON[3:0] bits (MON, 05H) determine which channel and which direction (transmit/receive) will be monitored. The monitoring is non-intrusive per ITU-T G.772. Figure-12 illustrates the concept.

The monitored line signal (transmit or receive) goes through Channel 1's Clock and Data Recovery. The signal can be observed digitally at the RCLK1, RD1/RDP1 and RDN1. If Channel 1 is configured to Remote Loopback while in the Monitoring mode, the monitored data will be output on TTIP1/TRING1.

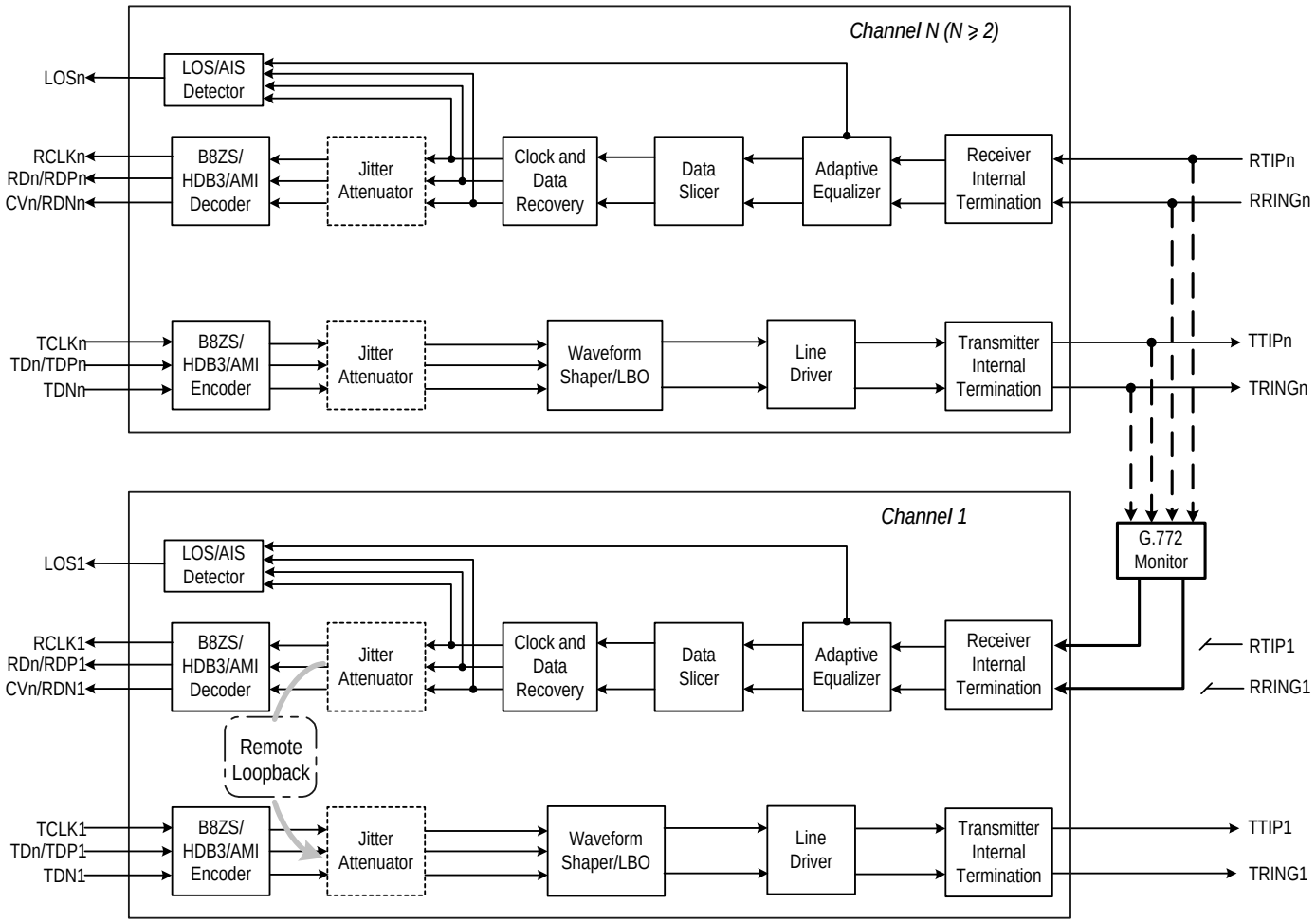


Figure-12 G.772 Monitoring Diagram

3.3.11 RECEIVE JITTER ATTENUATOR

The Receive Jitter Attenuator of each link can be chosen to be used or not. This selection is made by the RJA_E bit (RJACF, 27H...).

The Jitter Attenuator consists of a FIFO and a DPLL, as shown in Figure 7.

The FIFO is used as a pool to buffer the jittered input data, then the data is clocked out of the FIFO by a de-jittered clock. The depth of the FIFO can be 32 bits, 64 bits or 128 bits, as selected by the RJA_DP[1:0] bits (RJACF, 27H...). Accordingly, the constant delay produced by the Jitter Attenuator is 16 bits, 32 bits or 64 bits. The 128-bit FIFO is used when large jitter tolerance is expected, while the 32-bit FIFO is used in delay sensitive applications.

The DPLL is used to generate a de-jittered clock to clock out the data stored in the FIFO. The DPLL can only attenuate the incoming jitter whose frequency is above Corner Frequency (CF). The jitter whose frequency is lower than the CF passes through the DPLL without any attenuation. In T1/J1 applications, the CF of the DPLL can be 5 Hz or 1.26 Hz, as selected by the RJA_BW bit. In E1 applications, the CF of the DPLL can be 6.77 Hz or 0.87 Hz, as selected by the RJA_BW bit (RJACF, 27H...). The lower the CF is, the longer time is needed to achieve synchronization.

If the incoming data moves faster than the outgoing data, the FIFO will overflow. If the incoming data moves slower than the outgoing data, the FIFO will underflow. The overflow or underflow is captured by the

© 2019 Renesas Electronics Corporation

RJA_IS bit (INTS1, 3BH...). When the RJA_IS bit is '1', an interrupt will be reported on the $\overline{INT}$ pin if enabled by the RJA_IE bit (INTENC1, 34H...).

To avoid overflow or underflow, the JA-Limit function can be enabled by setting the RJA_LIMT bit (RJACF, 27H...). When the JA-Limit function is enabled, the speed of the outgoing data will be adjusted automatically if the FIFO is close to its full or emptiness. The criteria of speed adjustment start are listed in Table 17. Though the JA-Limit function can reduce the possibility of FIFO overflow and underflow, the quality of jitter attenuation is deteriorated.

Table-17 Criteria Of Speed Adjustment Start

FIFO Depth	Criteria Of Speed Adjustment Start
32 bits	2-bit close to full or empty
64 bits	3-bit close to full or empty
128 bits	4-bit close to full or empty

Selected by the RJITT_TEST bit (RJACF, 27H...), the real time interval between the read and write pointer of the FIFO or the peak-peak interval between the read and write pointer of the FIFO can be indicated in the RJITT[6:0] bits (RJITT, 39H...). When the RJITT_TEST bit is '0', the current interval between the read and write pointer of the FIFO will be written into the RJITT[6:0] bits. When the RJITT_TEST bit is '1', the current interval will be compared with the old one in the RJITT[6:0] bits and the larger one will be indicated by the RJITT[6:0] bits.

The performance of Receive Jitter Attenuator meets the ITU-T I.431, G.703, G.736 - 739, G.823, G.824, ETSI 300011, ETSI TBR 12/13, AT&T TR62411, TR43802, TR-TSY 009, TR-TSY 253, TR-TRY 499 standards. Refer to Chapter 6.9 Jitter Tolerance and Chapter 6.10 Jitter Transfer for details.

Table-18 Related Bit / Register In Chapter 3.3.11

Bit	Register	Address (Hex)
RJA_E	Receive Jitter Attenuation Configuration	X27H
RJA_DP[1:0]		
RJA_BW		
RJA_LIMT		
RJITT_TEST		
RJA_IS	Interrupt Status 1	X3BH
RJA_IE	Interrupt Enable Control 1	X34H
RJITT[6:0]	Receive Jitter Measure Value Indication	X39H

3.3.12 LOS AND AIS DETECTION

3.3.12.1LOS DETECTION

The Loss of Signal Detector monitors the amplitude of the incoming signal level and pulse density of the received signal on RTIPn and RRINGn.

- LOS declare (LOS=1)

A LOS is detected when the incoming signal has "no transitions", i.e., when the signal level is less than Q dB below nominal for N consecutive pulse intervals. Here N is defined by LAC bit (MAINT1, 2CH...). LOS will be declared by pulling LOSn pin to high (LOS=1) and LOS interrupt will be generated if it is not masked.

- LOS clear (LOS=0)

The LOS is cleared when the incoming signal has "transitions", i.e., when the signal level is greater than P dB below nominal and has an average pulse density of at least 12.5% for M consecutive pulse intervals, starting with the receipt of a pulse. Here M is defined by LAC bit (MAINT1, 2CH...). LOS status is cleared by pulling LOSn pin to low.

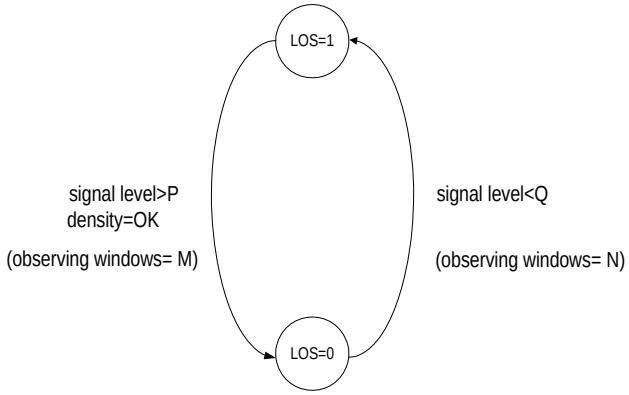


Figure-13 LOS Declare and Clear

- LOS detect level threshold

In short haul mode, the amplitude threshold Q is fixed on 800 mVpp, while P=Q+200 mVpp (200 mVpp is the LOS level detect hysteresis). In line monitor mode, the amplitude threshold Q is fixed on 1600 mVpp, while P=Q+400 mVpp (400 mVpp is the LOS level detect hysteresis).

In long haul mode, the value of Q can be selected by LOS[4:0] bit (RCF1, 29H...), while P=Q+4 dB (4 dB is the LOS level detect hysteresis). The LOS[4:0] default value is 10101 (-46 dB).

- Criteria for declare and clear of a LOS detect

The detection supports the ANSI T1.231 and I.431 for T1/J1 mode and G.775 and ETSI 300233/I.431 for E1 mode. The criteria can be selected by LAC bit (MAINT1, 2CH...) and TE_MODE bit (T1E1 mode, 20H...).

Table-19 and Table-20 summarize LOS declare and clear criteria for both short haul and long haul application.

- All Ones output during LOS

On the system side, the RDPn/RDNn will reflect the input pulse "transition" at the RTIPn/RRINGn side and output recovery clock (but the quality of the output clock can not be guaranteed when the input level is lower than

© 2019 Renesas Electronics Corporation

the maximum receive sensitivity) when RAISE bit (MAINT1, 2CH...) is 0; or output All Ones as AIS when RAISE bit (MAINT1, 2CH...) is 1. In this case RCLKn output is replaced by MCLK.

On the line side, the TTIPn/TRINGn will output All Ones as AIS when ATAO bit (MAINT1, 2CH...) is 1. The All Ones pattern uses MCLK as the reference clock.

LOS indicator is always active for all kinds of loopback modes.

Table-19 LOS Declare and Clear Criteria for Short Haul Mode

Control bit		LOS declare threshold	LOS clear threshold
TEMODE	LAC		
1=T1/J1	0=T1.231	Level < 800 mVpp N=175 bits	Level > 1 Vpp M=128 bits 12.5% mark density <100 consecutive zeroes
	1=I.431	Level < 800 mVpp N=1544 bits	Level > 1 Vpp M=128 bits 12.5% mark density <100 consecutive zeroes
0=E1	0=G.775	Level < 800 mVpp N=32 bits	Level > 1 Vpp M=32 bits 12.5% mark density <16 consecutive zeroes
	1=I.431/ETSI	Level < 800 mVpp N=2048 bits	Level > 1 Vpp M=32 bits 12.5% mark density <16 consecutive zeroes

© 2019 Renesas Electronics Corporation

Table-20 LOS Declare and Clear Criteria for Long Haul Mode

Control bit					LOS declare threshold	LOS clear threshold	Note
TEMODE	LAC		LOS[4:0]	Q (dB)			
1=T1/J1	0	T1.231	00000 00001 … 10001 … 10101 10110-11111	-4 -6 … -38 … -46 -48	Level < Q N=175 bits	Level > Q+ 4dB M=128 bits 12.5% mark density <100 consecutive zeroes	
	1	-	00000 … 00110	-4 -16	Level < Q N=1544 bits	Level > Q+ 4dB M=128 bits 12.5% mark density <100 consecutive zeroes	I.431 Level detect range is -18 to -30 dB.
		I.431	00111 … 01101	-18 … -30			
		-	01110 … 10001 … 10101 10110-11111	-32 … -38 … -46 -48			
0=E1	0	-	00000 … 00010	-4 … -8	Level < Q N=32 bits	Level > Q+ 4dB M=32 bits 12.5% mark density <16 consecutive zeroes	G.775 Level detect range is -9 to -35 dB.
		G.775	00011 … 10000	-10 … -36			
		-	10001 … 10101(default) 10110-11111	-38 … -46 -48			
	1	-	00000	-4	Level < Q N=2048 bits	Level > Q+ 4dB M=32 bits 12.5% mark density <16 consecutive zeroes	I.431 Level detect range is -6 to -20 dB.
		I.431/ ETSI	00001 … 01000	-6 … -20			
		-	01001 … 10101(default) 10110-11111	-22 … -46 -48			

3.3.12.2AIS DETECTION

The Alarm Indication Signal can be detected by the IDT82P5088 when the Clock&Data Recovery unit is enabled. The status of AIS detection is reflected in the AIS_S bit (STAT0, 36H...). In T1/J1 applications, the criteria for declaring/clearing AIS detection are in compliance with the ANSI T1.231. In E1 applications, the criteria for declaring/clearing AIS detection comply with the ITU G.775 or the ETSI 300233, as selected by the LAC bit (MAINT1,2CH...). Table-21 summarizes different criteria for AIS detection Declaring/Clearing.

© 2019 Renesas Electronics Corporation

Table-21 AIS Condition

	ITU G.775 for E1 (LAC bit is set to '0' by default)	ETSI 300233 for E1 (LAC bit is set to '1')	ANSI T1.231 for T1/J1
AIS detected	Less than 3 zeros contained in each of two consecutive 512-bit streams are received	Less than 3 zeros contained in a 512-bit stream are received	Less than 9 zeros contained in an 8192-bit stream (a ones density of 99.9% over a period of 5.3ms)
AIS cleared	3 or more zeros contained in each of two consecutive 512-bit streams are received	3 or more zeros contained in a 512-bit stream are received	9 or more zeros contained in an 8192-bit stream are received

3.4 TRANSMIT AND DETECT INTERNAL PATTERNS

The internal patterns (All Ones, All Zeros, PRBS/QRSS pattern and Activate/Deactivate Loopback Code) will be generated and detected by the IDT82P5088. TCLKn is used as the reference clock by default. MCLK can also be used as the reference clock by setting the PATT_CLK bit (MAINT1, 2CH...) to '1'.

If the PATT_CLK bit (MAINT1, 2CH...) is set to '0' and the PATT[1:0] bits (MAINT1, 2CH...) are set to '00', the transmit path will operate in normal mode.

3.4.1 TRANSMIT ALL ONES

In transmit direction, the All Ones data can be inserted into the data stream when the PATT[1:0] bits (MAINT1, 2CH...) are set to '01'. The transmit data stream is output from TTIPn/TRINGn. In this case, either TCLKn or MCLK can be used as the transmit clock, as selected by the PATT_CLK bit (MAINT1, 2CH...).

3.4.2 TRANSMIT ALL ZEROS

If the PATT_CLK bit (MAINT1, 2CH...) is set to '1', the All Zeros will be inserted into the transmit data stream when the PATT[1:0] bits (MAINT1, 2CH...) are set to '00'.

3.4.3 PRBS/QRSS GENERATION AND DETECTION

A PRBS/QRSS will be generated in the transmit direction and detected in the receive direction by IDT82P5088. The QRSS is 2^{20}-1 for T1/J1 applications and the PRBS is 2^{15}-1 for E1 applications, with maximum zero restrictions according to the AT&T TR62411 and ITU-T O.151.

When the PATT[1:0] bits (MAINT1, 2CH...) are set to '10', the PRBS/QRSS pattern will be inserted into the transmit data stream with the MSB first. The PRBS/QRSS pattern will be transmitted directly or invertedly.

The PRBS/QRSS in the received data stream will be monitored. If the PRBS/QRSS has reached synchronization status, the PRBS_S bit (STAT0, 36H...) will be set to '1', even in the presence of a logic error rate less than or equal to 10^{-1}. The criteria for setting/clearing the PRBS_S bit are shown in Table-22.

Table-22 Criteria for Setting/Clearing the PRBS_S Bit

PRBS/QRSS Detection	6 or less than 6 bit errors detected in a 64 bits hopping window.
PRBS/QRSS Missing	More than 6 bit errors detected in a 64 bits hopping window.

PRBS data can be inverted through setting the PRBS_INV bit (MAINT1, 2CH...).

Any change of PRBS_S bit will be captured by PRBS_IS bit (INTS0, 3AH...). The PRBS_IES bit (INTES, 35H...) can be used to determine whether the '0' to '1' change of PRBS_S bit will be captured by the PRBS_IS bit or any changes of PRBS_S bit will be captured by the PRBS_IS bit. When the PRBS_IS bit is '1', an interrupt will be generated if the PRBS_IE bit (INTENC0, 33H...) is set to '1'.

The received PRBS/QRSS logic errors can be counted in a 16-bit counter if the ERR_SEL [1:0] bits (MAINT6, 31H...) are set to '00'. Refer to Refer to 3.6 ERROR DETECTION/COUNTING AND INSERTION for the operation of the error counter.

© 2019 Renesas Electronics Corporation

3.5 LOOPBACK

To facilitate testing and diagnosis, the IDT82P5088 provides four different loopback configurations: Analog Loopback, Digital Loopback, Remote Loopback and Inband Loopback.

3.5.1 ANALOG LOOPBACK

When the ALP bit (MAINT0, 2BH...) is set to '1', the corresponding channel is configured in Analog Loopback mode. In this mode, the transmit signals are looped back to the Receiver Internal Termination in the receive path then output from RCLKn, RDn, RDPn/RDNn. The all-ones pattern can be generated during analog loopback. At the same time, the transmit signals are still output to TTIPn/TRINGn in transmit direction. Figure-14 shows the process. The THZ bit (TCF1, 23H...) shall be set to '0' in Analog Loopback mode.

3.5.2 DIGITAL LOOPBACK

When the DLP bit (MAINT0, 2BH...) is set to '1', the corresponding channel is configured in Digital Loopback mode. In this mode, the transmit signals are looped back to the jitter attenuator (if enabled) and decoder in receive path, then output from RCLKn, RDn, RDPn/RDNn. At the same time, the transmit signals are still output to TTIPn/TRINGn in transmit direction. Figure-15 shows the process.

Both Analog Loopback mode and Digital Loopback mode allow the sending of the internal patterns (All Ones, All Zeros, PRBS, etc.) which will overwrite the transmit signals. In this case, either TCLKn or MCLK can be used as the reference clock for internal patterns transmission.

3.5.3 REMOTE LOOPBACK

When the RLP bit (MAINT0, 2BH...) is set to '1', the corresponding channel is configured in Remote Loopback mode. In this mode, the recovered clock and data output from Clock and Data Recovery on the receive path is looped back to the jitter attenuator (if enabled) and Waveform Shaper in transmit path. Figure-16 shows the process.

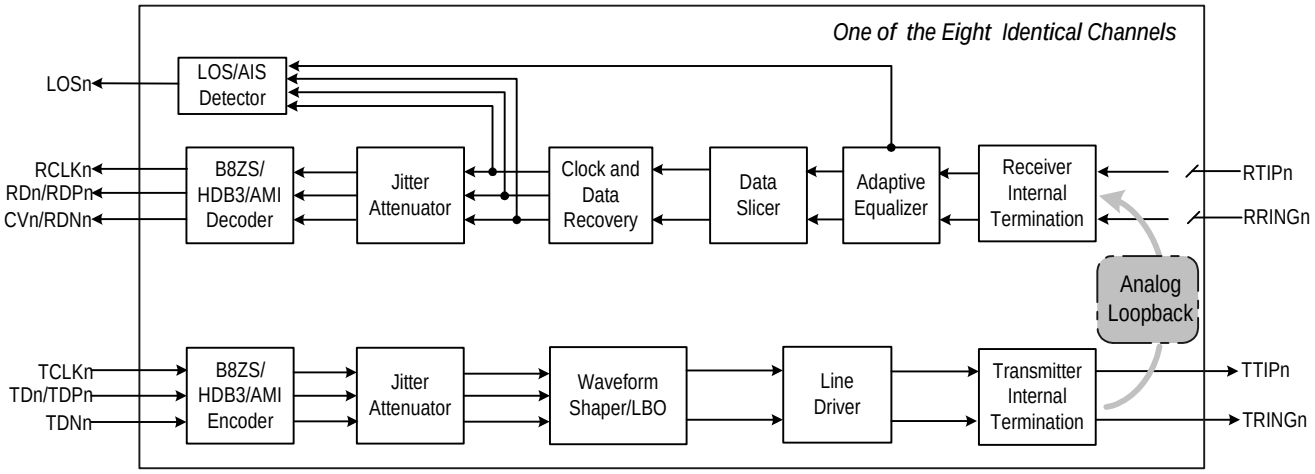


Figure-14 Analog Loopback

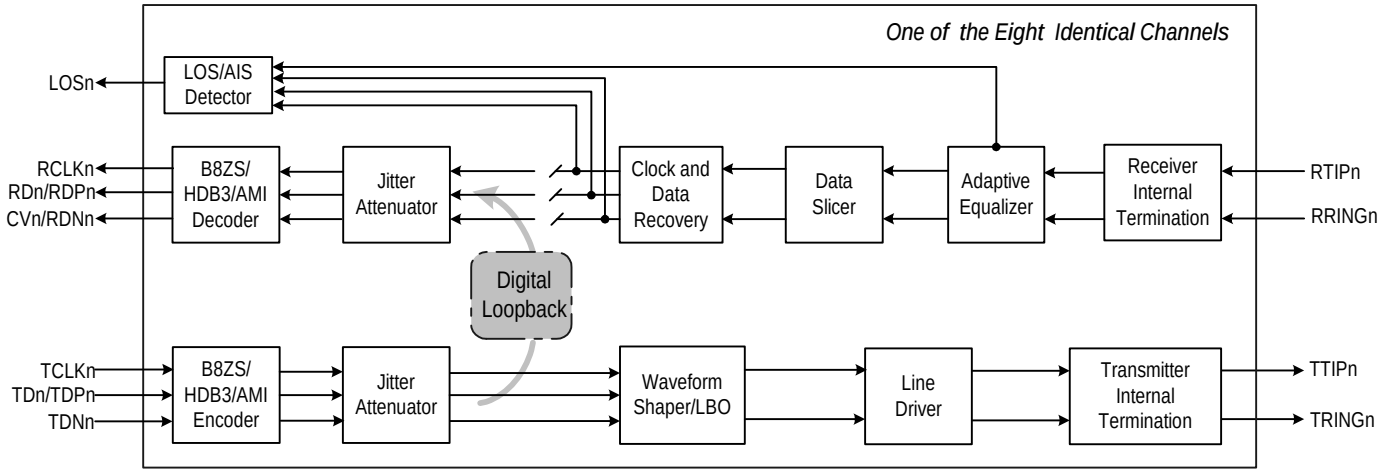


Figure-15 Digital Loopback

© 2019 Renesas Electronics Corporation

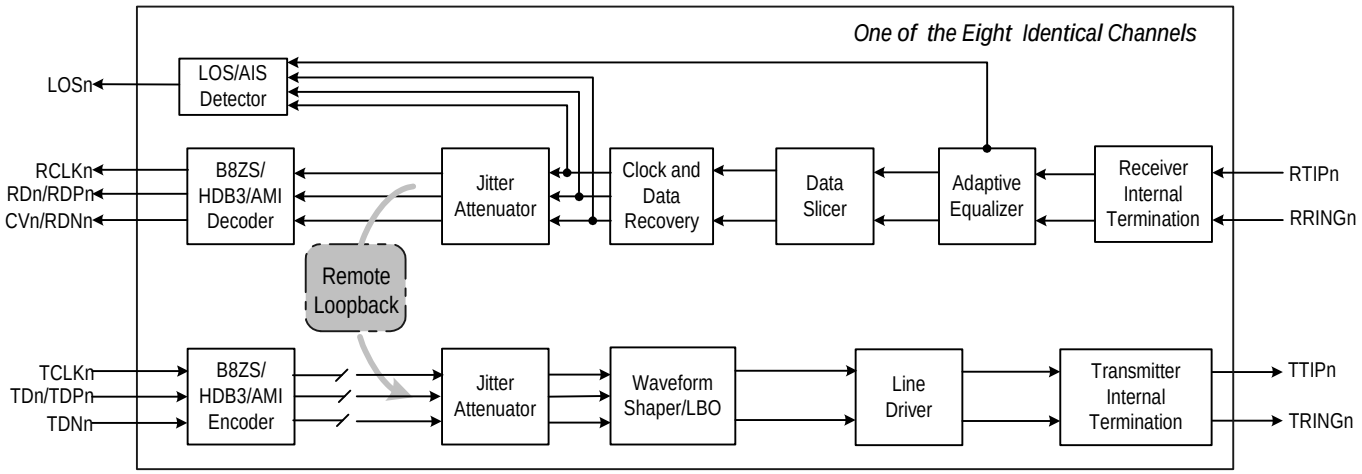


Figure-16 Remote Loopback

© 2019 Renesas Electronics Corporation

3.5.4 INBAND LOOPBACK

When PATT[1:0] bits (MAINT1, 2CH...) are set to '11', the corresponding channel is configured in Inband Loopback mode. In this mode, an activate/Deactivate Loopback Code is generated repeatedly in transmit direction per ANSI T1. 403 which overwrite the transmit signals. In receive direction, the code is detected per ANSI T1. 403, even in the presence of 10^{-2} bit error rate.

If the Automatic Remote Loopback is enabled by setting ARLP bit (MAINT0, 2BH...) to '1', the chip will establish/demolish the Remote Loopback based on the reception of the Activate Loopback Code/Deactivate Loopback Code for 5.1 s. If the ARLP bit (MAINT0, 2BH...) is set to '0', the Remote Loopback can also be demolished forcedly.

3.5.4.1 Transmit Activate/Deactivate Loopback Code

The pattern of the transmit Activate/Deactivate Loopback Code is defined by the TNLP[7:0] bits (MAINT3, 2EH...). Whether the code represents an Activate Loopback Code or a Deactivate Loopback Code is judged by the far end receiver. The length of the pattern ranges from 5 bits to 8 bits, as selected by the TNLP_L[1:0] bits (MAINT2, 2DH...). The pattern can be programmed to 6-bit-long or 8-bit-long respectively by repeating itself if it is 3-bit-long or 4-bit-long. When the PATT[1:0] bits (MAINT1, 2CH...) are set to '11', the transmission of the Activate/Deactivate Loopback Code is initiated. If the PATT_CLK bit (MAINT1, 2CH...) is set to '0' and the PATT[1:0] bits (MAINT1, 2CH...) are set to '00', the transmission of the Activate/Deactivate Loopback Code will stop.

The local transmit activate/deactivate code setting should be the same as the receive code setting in the remote end. It is the same thing for the other way round.

3.5.4.2 Receive Activate/Deactivate Loopback Code

The pattern of the receive Activate Loopback Code is defined by the RNLPA[7:0] bits (MAINT4, 2FH...). The length of this pattern ranges from 5 bits to 8 bits, as selected by the RNLPA_L [1:0] bits (MAINT2, 2DH...). The pattern can be programmed to 6-bit-long or 8-bit-long respectively by repeating itself if it is 3-bit-long or 4-bit-long.

The pattern of the receive Deactivate Loopback Code is defined by the RNLPD[7:0] bits (MAINT5, 30H...). The length of the receive Deactivate Loopback Code ranges from 5 bits to 8 bits, as selected by the RNLPD_L[1:0] bits (MAINT2, 2DH...). The pattern can be programmed to 6-bit-long or 8-bit-long respectively by repeating itself if it is 3-bit-long or 4-bit-long.

After the Activate Loopback Code has been detected in the receive data for more than 30 ms (in E1 mode) / 40 ms (in T1/J1 mode), the NLPA_S bit (STAT0, 36H...) will be set to '1' to declare the reception of the Activate Loopback Code.

After the Deactivate Loopback Code has been detected in the receive data for more than 30 ms (In E1 mode) / 40 ms (In T1/J1 mode), the NLPD_S bit (STAT0, 36H...) will be set to '1' to declare the reception of the Deactivate Loopback Code.

When the NLPA_IES bit (INTES, 35H...) is set to '0', only the '0' to '1' transition of the NLPA_S bit will generate an interrupt and set the NLPA_IS bit (INTS0, 3AH...) to '1'. When the NLPA_IES bit is set to '1', any changes of the NLPA_S bit will generate an interrupt and set the NLPA_IS bit (INTS0, 3AH...) to '1'. The NLPA_IS bit will be reset to '0' after being read.

When the NLPD_IES bit (INTES, 35H...) is set to '0', only the '0' to '1' transition of the NLPD_S bit will generate an interrupt and set the NLPD_IS bit (INTS0, 3AH...) to '1'. When the NLPD_IES bit is set to '1', any changes of the NLPD_S bit will generate an interrupt and set the NLPD_IS bit (INTS0, 3AH...) to '1'. The NLPD_IS bit will be reset to '0' after being read.

3.5.4.3 Automatic Remote Loopback

When ARLP bit (MAINT0, 2BH...) is set to '1', the corresponding channel is configured into the Automatic Remote Loopback mode. In this mode, if the Activate Loopback Code has been detected in the receive data for more than 5.1 s, the Remote Loopback (shown as Figure-16) will be established automatically, and the ARLP_S bit (STAT0, 36H...) will be set to '1' to indicate the establishment of the Remote Loopback. The NLPA_S bit (STAT0, 36H...) is set to '1' to generate an interrupt. In this case, the Remote Loopback mode will still be kept even if the receiver stop receiving the Activate Loopback Code.

If the Deactivate Loopback Code has been detected in the receive data for more than 5.1 s, the Remote Loopback will be demolished automatically, and the ARLP_S bit (STAT0, 36H...) will set to '0' to indicate the demolishment of the Remote Loopback. The NLPD_S bit (STAT0, 36H...) is set to '1' to generate an interrupt.

The Remote Loopback can also be demolished forcedly by setting ARLP bit (MAINT0, 2BH...) to '0'.

© 2019 Renesas Electronics Corporation

3.6 ERROR DETECTION/COUNTING AND INSERTION

3.6.1 DEFINITION OF LINE CODING ERROR

The following line encoding errors can be detected and counted by the IDT82P5088:

- Received Bipolar Violation (BPV) Error: In AMI coding, when two consecutive pulses of the same polarity are received, a BPV error is declared.
- HDB3/B8ZS Code Violation (CV) Error: In HDB3/B8ZS coding, a CV error is declared when two consecutive BPV errors are detected, and the pulses that have the same polarity as the previous pulse are not the HDB3/B8ZS zero substitution pulses.
- Excess Zero (EXZ) Error: there are two standards defining the EXZ errors: ANSI and FCC. The EXZ_DEF bit (MAINT6, 31H...) chooses which standard will be adopted by the corresponding channel to judge the EXZ error. Table-23 shows definition of EXZ.

Table-23 EXZ Definition

	EXZ Definition	
	ANSI	FCC
AMI	More than 15 consecutive 0s are detected	More than 80 consecutive 0s are detected
HDB3	More than 3 consecutive 0s are detected	More than 3 consecutive 0s are detected
B8ZS	More than 7 consecutive 0s are detected	More than 7 consecutive 0s are detected

3.6.2 ERROR DETECTION AND COUNTING

Which type of the receiving errors (Received CV/BPV errors, excess zero errors and PRBS logic errors) will be counted is determined by ERR_SEL[1:0] bits (MAINT6, 31H...). Only one type of receiving error can be counted at a time except that when the ERR_SEL[1:0] bits are set to '11', both CV/BPV and EXZ errors will be detected and counted.

The receiving errors are counted in an internal 16-bit Error Counter. Once an error is detected, an error interrupt which is indicated by corresponding bit in (INTS1, 3BH...) will be generated if it is not masked. This Error Counter can be operated in two modes: Auto Report Mode and Manual Report Mode, as selected by the CNT_MD bit (MAINT6, 31H...). In Single Rail mode, once BPV or CV errors are detected, the CVn pin will be driven to high for one RCLK period.

- Auto Report Mode

In Auto Report Mode, the internal counter starts to count the received errors when the CNT_MD bit (MAINT6, 31H...) is set to '1'. A one-second timer is used to set the counting period. The received errors are counted within one second. If the one-second timer expires, the value in the internal counter will be transferred to (CNTL, 3CH...) and (CNTH, 3DH...), then the internal counter will be reset and start to count received errors for the next second. The errors occurred during the transfer will be accumulated to the next round. The expiration of the one-second timer will set TMOV_IS bit (INTS1, 3BH...) to '1', and will generate an interrupt if the TIMER_IE bit (INTENC1, 34H...) is set to '0'. The CV_IS bit (INTS1, 3BH...) will be cleared after the interrupt register is read. The content in the (CNTL, 3CH...) and (CNTH, 3DH...) should be read within the next second. If the counter overflows, a counter overflow interrupt which is indicated by CNT_OV_IS bit (INTS1, 3BH...) will be generated if it is not masked by CNT_IE bit (INTENC1, 34H...).

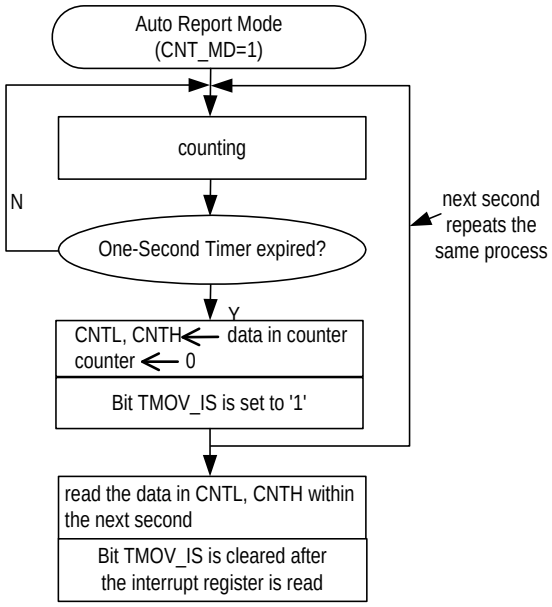


Figure-17 Auto Report Mode

© 2019 Renesas Electronics Corporation

• Manual Report Mode

In Manual Report Mode, the internal Error Counter starts to count the received errors when the CNT_MD bit (MAINT6, 31H...) is set to '0'. When there is a '0' to '1' transition on the CNT_STOP bit (MAINT6, 31H...), the data in the counter will be transferred to (CNTL, 3CH...) and (CNTH, 3DH...), then the counter will be reset. The errors occurred during the transfer will be accumulated to the next round. If the counter overflows, a counter overflow interrupt indicated by CNTOV_IS bit (INTS1, 3BH...) will be generated if it is not masked by CNT_IE bit (INTENC1, 34H...).

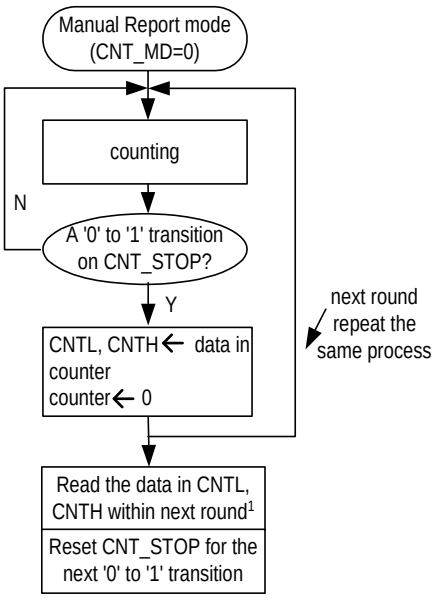


Figure-18 Manual Report Mode

Note: 1. It is recommended that users should do the followings within next round of error counting: Read the data in CNTL and CNTH; Reset CNT_TRF bit for the next '0' to '1' transition on this bit.

3.6.3 BIPOLAR VIOLATION AND PRBS ERROR INSERTION

Only when three consecutive '1's are detected in the transmit data stream, will a '0' to '1' transition on the BPV_INS bit (MAINT6, 31H...) generate a bipolar violation pulse, and the polarity of the second '1' in the series will be inverted.

A '0' to '1' transition on the EER_INS bit (MAINT6, 31H...) will generate a logic error during the PRBS/QRSS transmission.

3.7 LINE DRIVER FAILURE MONITORING

The transmit driver failure monitor can be enabled or disabled by setting DFM_OFF bit (TCF1, 23H...). If the transmit driver failure monitor is enabled, the transmit driver failure will be captured by DF_S bit (STAT0, 36H...). The transition of the DF_S bit is reflected by DF_IS bit (INTS0, 3AH...), and, if enabled by DF_IE bit (INTENC0, 33H...), will generate an interrupt. When there is a short circuit on the TTIPn/TRINGn port, the output current will be limited to 100 mA (typical) and an interrupt will be generated.

© 2019 Renesas Electronics Corporation

3.8 CLOCK GENERATOR AND TCLK

3.8.1 CLOCK GENERATOR

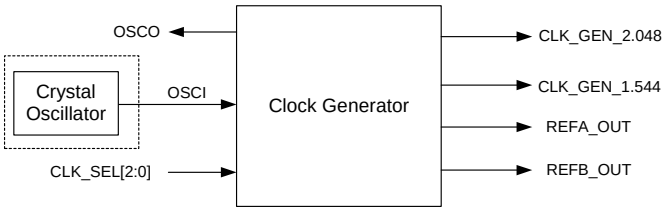


Figure-19 Clock Generator

The OSCI pin is connected to an external Crystal Oscillator. In T1 mode E1 Rate of Transmit System interface, this clock must keep the Crystal Oscillator same with system transmit clock (TSCKn/MTSCK).

The OSCO pin outputs the inverted, buffered clock input from OSCI.

The clock frequency of OSCI is defined by CLK_SEL[2:0]. Refer to Table-24.

Table-24 Reference Clock Selection

CLK_SEL[2:0]	Input Clock Signal (MHz)
000	1 X 1.544
001	2 X 1.544
010	3 X 1.544
011	4 X 1.544
100	1 X 2.048
101	2 X 2.048
110	3 X 2.048
111	4 X 2.048

The CLK_GEN_1.544 pin outputs the 1.544 MHz clock signal and the CLK_GEN_2.048 outputs the 2.048 MHz clock signal.

The frequecy of the REFA_OUT/REFB_OUT pins is 2.048 MHz (E1) or 1.544 MHz (T1/J1). When no LOS is detected, the REFA_OUT/REFB_OUT pins output a recovered clock from the Clock and Data Recovery function block of one of the eight links. The REFA_OUT link is selected by the RO1[2:0] bits (b2~0, T1/J1-007H / b2~0, E1-007H); The REFB_OUT link is selected by the RO2[2:0] bits (b5~3, T1/J1-007H / b5~3, E1-007H). When LOS is detected, the REFA_OUT/REFB_OUT pins output MCLK or high level, as selected by the REFH_LOS bit (b0, T1/J1-03EH,... / b0, E1-03EH,...). *

Note: MCLK is a clock derived from OSCI using an internal PLL, and the frequency is 2.048 MHz (E1) or 1.544 MHz (T1/J1).

3.8.2 TRANSMIT CLOCK (TCLK)

The TCLKn is used to sample the transmit data on TDn/TDPn, TDNn. The active edge of TCLKn can be selected by the TCLK_SEL bit (TCF0, 22H...). During Transmit All Ones, PRBS/QRSS patterns or Inband Loopback Code, either TCLKn or MCLK can be used as the reference clock. This is selected by the PATT_CLK bit (MAINT1, 2CH...).

But for Automatic Transmit All Ones and AIS, only MCLK is used as the reference clock and the PATT_CLK bit is ignored. In Automatic Transmit All Ones condition, the ATAO bit (MAINT1, 2CH) is set to '1'. In AIS condition, the RAISE bit (MAINT1, 2CH) is set to '1'.

If TCLKn has been missing for more than 70 MCLK cycles, TCLK_LOS bit (STAT0, 36H...) will be set, and the corresponding TTIPn/TRINGn will become high impedance if this channel is not used for remote loopback or is not using MCLK to transmit internal patterns (TAOS, All Zeros, PRBS and in-band loopback code). When TCLKn is detected again, TCLK_LOS bit (STAT0, 36H...) will be cleared. The reference frequency to detect a TCLKn loss is derived from MCLK.

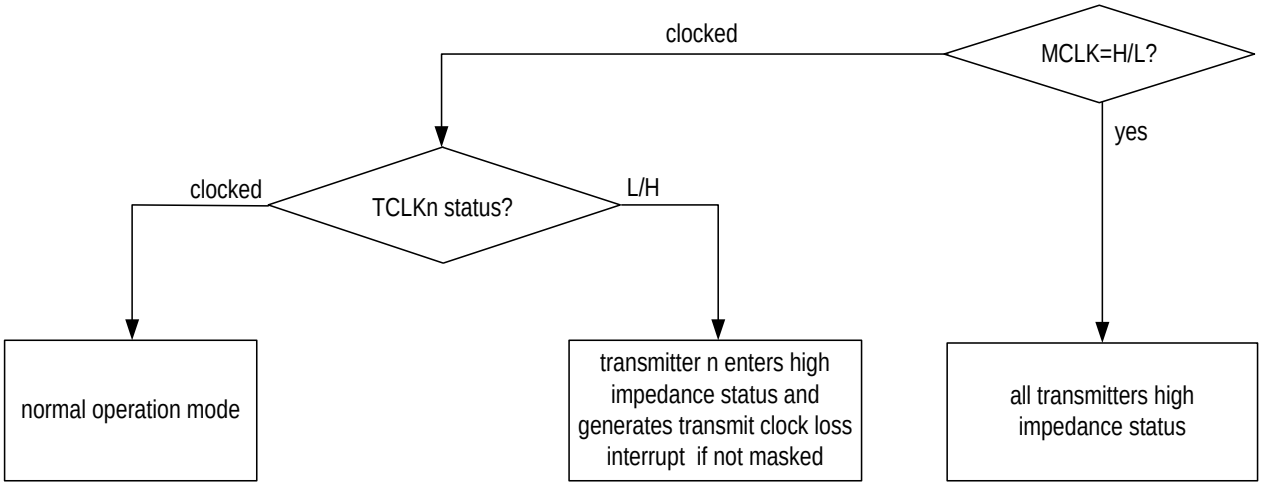


Figure-20 TCLK Operation Flowchart

© 2019 Renesas Electronics Corporation

3.9 MICROPROCESSOR INTERFACE

The microprocessor interface provides access to read and write the registers in the device. The interface consists of Serial Peripheral Interface (SPI) and parallel microprocessor interface.

3.9.1 SPI Mode

Pull the SPIEN pin to high, and the microprocessor interface will be set in SPI mode.

In this mode, only the $\overline{CS}$, SCLK, SDI and SDO pins are interfaced with the microprocessor. A falling transition on $\overline{CS}$ pin indicates the start of a read/write operation, and a rising transition indicates the end of the operation. After the $\overline{CS}$ pin is set to low, two bytes include instruction and address bytes on the SDI pin are input to the device on the rising edge of the SCLK pin. First byte consists of one instruction bit at MSB and three address bits at LSB, and the second byte is low 8 address bits. If the MSB is '1', it is read operation. If the MSB is '0', it is write operation. If the device is in read operation, the data read from the specified register is output on the SDO pin on the falling edge of the SCLK (refer to Figure 21). If the device is in write operation, the data written to the specified register is input on the SDI pin following the address byte (refer to Figure 22).

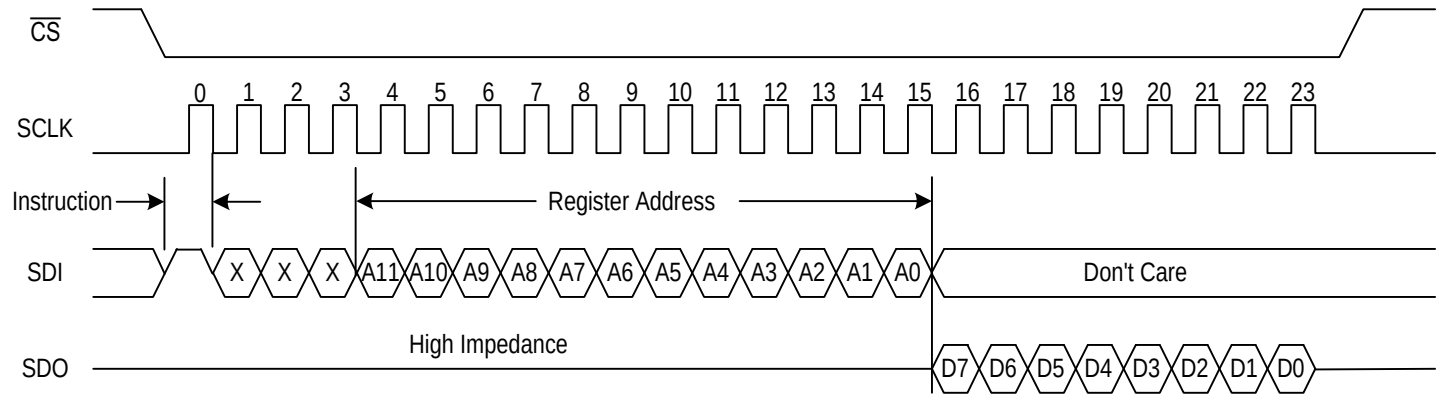


Figure-21 Read Operation In SPI Mode

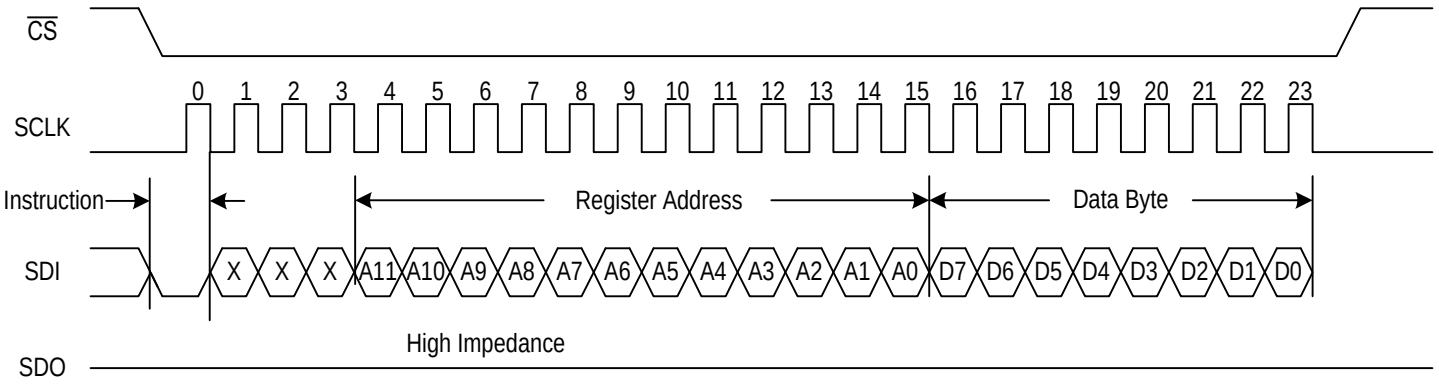


Figure-22 Write Operation In SPI Mode

3.9.2 Parallel Microprocessor Interface

Pull the SPIEN pin to low, the microprocessor interface will be set in parallel mode. In this mode, the interface is compatible with the Motorola and the Intel microprocessor, which is selected by the MPM pin. The IDT82P5088 uses separate address bus and data bus. The mode selection and the interfaced pin are tabularized in Table 25.

Table-25 Parallel Microprocessor Interface

Pin MPM	Microprocessor Interface	Interfaced Pin
Low	Motorola	$\overline{CS}$, $\overline{DS}$, $\overline{RW}$, A[10:0], D[7:0]
High	Intel	$\overline{CS}$, $\overline{RD}$, $\overline{WR}$, A[10:0], D[7:0]

© 2019 Renesas Electronics Corporation

3.10 INTERRUPT HANDLING

An active level on the $\overline{INT}$ pin represents an interrupt of the IDT82P5088. The INT_CH[7:0] bits (INTCH, 09H) should be read to identify which channel(s) generate the interrupt.

The interrupt event is captured by the corresponding bit in the Interrupt Status Register (INTS0, 3AH...) or (INTS1, 3BH...). Every kind of interrupt can be enabled/disabled individually by the corresponding bit in the register (INTENC0, 33H...) or (INTENC1, 34H...). Some event is reflected by the corresponding bit in the Status Register (STAT0, 36H...) or (STAT1, 37H...), and the Interrupt Trigger Edge Selection Register can be used to determine how the Status Register sets the Interrupt Status Register.

After the Interrupt Status Register (INTS0, 3AH...) or (INTS1, 3BH...) is read, the corresponding bit indicating which channel generates the interrupt in the INTCH register (09H) will be reset. Only when all the pending interrupt is acknowledged through reading the Interrupt Status Registers of all the channels (INTS0, 3AH...) or (INTS1, 3BH...) will all the bits in the INTCH register (09H) be reset and the $\overline{INT}$ pin become inactive.

There are totally fourteen kinds of events that could be the interrupt source for one channel:

(1).LOS Detected
(2).AIS Detected
(3).Driver Failure Detected
(4).TCLK Loss
(5).Synchronization Status of PRBS
(6).PRBS Error Detected
(7).Code Violation Received
(8).Excessive Zeros Received
(9).JA FIFO Overflow/Underflow
(10).Inband Loopback Code Status
(11).Equalizer Out of Range
(12).One-Second Timer Expired
(13).Error Counter Overflow
(14).Arbitrary Waveform Generator Overflow

Table-26 is a summary of all kinds of interrupt and their associated Status bit, Interrupt Status bit, Interrupt Trigger Edge Selection bit and Interrupt Mask bit.

Table-26 Interrupt Event

Interrupt Event	Status bit (STAT0, STAT1)	Interrupt Status bit (INTS0, INTS1)	Interrupt Edge Selection bit (INTES)	Interrupt Mask bit (INTENC0, INTENC1)
LOS Detected	LOS_S	LOS_IS	LOS_IES	LOS_IE
AIS Detected	AIS_S	AIS_IS	AIS_IES	AIS_IE
Driver Failure Detected	DF_S	DF_IS	DF_IES	DF_IE
TCLKn Loss	TCLK_LOS	TCLK_LOS_IS	TCLK_IES	TCLK_IE
Synchronization Status of PRBS/QRSS	PRBS_S	PRBS_IS	PRBS_IES	PRBS_IE
PRBS/QRSS Error		ERR_IS		ERR_IE
Code Violation Received		CV_IS		CV_IE
Excessive Zeros Received		EXZ_IS		EXZ_IE
JA FIFO Overflow		JAOV_IS		JAOV_IE
JA FIFO Underflow		JAUD_IS		JAUD_IE
Equalizer Out of Range	EQ_S	EQ_IS	EQ_IES	EQ_IE
Inband Loopback Activate Code Status	NLPA_S	NLPA_IS	NLPA_IES	NLPA_IE
Inband Loopback Deactivate Code Status	NLPD_S	NLPD_IS	NLPD_IES	NLPD_IE
One-Second Timer Expired		TMOV_IS		TIMER_IE
Error Counter Overflow		CNT_OV_IS		CNT_IE
Arbitrary Waveform Generator Overflow		DAC_OV_IS		DAC_OV_IE

© 2019 Renesas Electronics Corporation

3.11 GENERAL PURPOSE I/O

The IDT82P5088 provides two general purpose digital I/O pins: GPIO1, GPIO0. These two pins can be considered as digital Input or Output port by the DIR1 bit (GPIO, 06H) and DIR0 bit (GPIO, 06H) respectively. If the GPIO1 and GPIO0 are configured as Input port, the LEVEL1 bit (GPIO, 06H) and the LEVEL0 bit (GPIO, 06H) are used to reflect the level of the GPIO1 pin and the GPIO0 pin respectively. If the GPIO1 and GPIO0 are configured as Output port, the content in the LEVEL1 bit and LEVEL0 bit determines the logic value of GPIO1 pin and GPIO0 pin respectively.

3.12 RESET OPERATION

The chip can be reset in two ways:

- Software Reset: Writing to the RST register (04H) will reset the chip in 1 us.
- Hardware Reset: Asserting the $\overline{\text{RESET}}$ pin low for a minimum of 100 ns will reset the chip.
  During Hardware Reset, the device requires an active clock on MCLK. For T1/J1 operation, bit TE_MODE(T1E1 mode, 20H...) is set after reset. Before accessing any other registers a delay of 50 us is required to allow the internal clocking to be settled.

After reset, all drivers output are in high impedance state, all the internal flip-flops are reset, and all the registers are initialized to default values. When performing a software reset, the TE_MODE bit (T1E1 mode, 20H...) will not be reset and stay with the set value.

3.13 POWER SUPPLY

This chip uses 3.3 V and 1.8 V power supply.

© 2019 Renesas Electronics Corporation

4 PROGRAMMING INFORMATION

4.1 REGISTER LIST AND MAP

The IDT82P5088 registers can be divided into Global Registers and Local Registers. The operation on the Global Registers affects all the eight channels while the operation on Local Registers only affects that specific channel. For different channel, the address of Local Register is different. Table-27 is the map of Global Registers and Table-28 is the map of Local Registers.

4.2 RESERVED REGISTERS

When writing to registers with reserved bit locations, the default state must be written to the reserved bits to ensure proper device operation.

Table-27 Global Register List and Map

Address (Hex)	Register	R/W	Map							
			b7	b6	b5	b4	b3	b2	b1	b0
000 ~ 001	Reserved									
002	ID	R	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
003	Reserved									
004	RST	W	-	-	-	-	-	-	-	-
005	MON	R/W	-	-	-	-	MON3	MON2	MON1	MON1
006	GPIO	R/W	-	-	-	-	LEVEL1	LEVEL0	DIR1	DIR0
007	REFOUT	R/W	-	-	RO22	RO21	RO20	RO12	RO11	RO10
008	Reserved									
009	INTCH	R	INT_CH7	INT_CH6	INT_CH5	INT_CH4	INT_CH3	INT_CH2	INT_CH1	INT_CH0
00A ~00B	Reserved									
00C	TIMER INTE	R/W								TMOVIE
00D	TIMER INTS	R/W								TMOVIS
00E ~ 016	Reserved									

© 2019 Renesas Electronics Corporation

Table-28 Per Channel Register List and Map

Address (Hex)	Register	R/W	Map							
CH1-CH8			b7	b6	b5	b4	b3	b2	b1	b0
X20*	T1E1 mode		-	-	-	-	-	-	-	TEMODE
Transmit Path Control Registers										
X21	TJACF	R/W	-	-	TJITT_TEST	TJA_LIMIT	TJA_E	TJA_DP1	TJA_DP0	TJA_BW
X22	TCF0	R/W	-	-	-	T_OFF	TD_INV	TCLK_SEL	T_MD1	T_MD0
X23	TCF1	R/W	-	-	DFM_OFF	THZ	PULS3	PULS2	PULS1	PULS0
X24	TCF2	R/W	-	-	SCAL5	SCAL4	SCAL3	SCAL2	SCAL1	SCAL0
X25	TCF3	R/W	DONE	RW	UI1	UI0	SAMP3	SAMP2	SAMP1	SAMP0
X26	TCF4	R/W	-	WDAT6	WDAT5	WDAT4	WDAT3	WDAT2	WDAT1	WDAT0
Receive Path Control Registers										
X27	RJACF	R/W	-	-	RJITT_TEST	RJA_LIMIT	RJA_E	RJA_DP1	RJA_DP0	RJA_BW
X28	RCF0	R/W	-	-	-	R_OFF	RD_INV	RCLK_SEL	R_MD1	R_MD0
X29	RCF1	R/W	-	EQ_ON	FIXG	LOS4	LOS3	LOS2	LOS1	LOS0
X2A	RCF2	R/W	-	-	SLICE1	SLICE0	UPDW1	UPDW0	MG1	MG0
Network Diagnostics Control Registers										
X2B	MAINT0	R/W	-	-	-	-	ARLP	RLP	ALP	DLP
X2C	MAINT1	R/W	-	PATT1	PATT0	PATT_CLK	PRBS_INV	LAC	RAISE	ATAO
X2D	MAINT2	R/W	-	-	TNLP_L1	TNLP_L0	RNLPA_L1	RNLPA_L0	RNLPD_L1	RNLPD_L0
X2E	MAINT3	R/W	TNLP7	TNLP6	TNLP5	TNLP4	TNLP3	TNLP2	TNLP1	TNLP0
X2F	MAINT4	R/W	RNLPA7	RNLPA6	RNLPA5	RNLPA4	RNLPA3	RNLPA2	RNLPA1	RNLPA0
X30	MAINT5	R/W	RNLPD7	RNLPD6	RNLPD5	RNLPD4	RNLPD3	RNLPD2	RNLPD1	RNLPD0
X31	MAINT6	R/W	-	BPV_INS	ERR_INS	EXZ_DEF	ERR_SEL1	ERR_SEL0	CNT_MD	CNT_STOP
Transmit and Receive Termination Registers										
X32	TERM	R/W	-	-	T_TERM2	T_TERM1	T_TERM0	R_TERM2	R_TERM1	R_TERM0
Interrupt Control Registers										
X33	INTENC0	R/W	-	NLPA_IE	NLPD_IE	PRBS_IE	TCLK_IE	DF_IE	AIS_IE	LOS_IE
X34	INTENC1	R/W	-	DAC_IE	TJA_IE	RJA_IE	ERR_IE	EXZ_IE	CV_IE	CNT_IE
X35	INTES	R/W	-	NLPA_IES	NLPD_IES	PRBS_IES	TCLK_IES	DF_IES	AIS_IES	LOS_IES
Line Status Registers										
X36	STAT0	R	ARLP_S	NLPA_S	NLPD_S	PRBS_S	TCLK_LOS	DF_S	AIS_S	LOS_S
X37	STAT1	R	-	-	-	LATT4	LATT3	LATT2	LATT1	LATT0
X38	TJITT	R	-	TJITT6	TJITT5	TJITT4	TJITT3	TJITT2	TJITT1	TJITT0
X39	RJITT	R	-	RJITT6	RJITT5	RJITT4	RJITT3	RJITT2	RJITT1	RJITT0
Interrupt Status Registers										
X3A	INTS0	R/W	-	NLPA_IS	NLPD_IS	PRBS_IS	TCLK_LOS_IS	DF_IS	AIS_IS	LOS_IS
X3B	INTS1	R/W	-	DAC_IS	TJA_IS	RJA_IS	ERR_IS	EXZ_IS	CV_IS	CNTOV_IS
Counter Registers										
X3C	CNTL	R	CNT_L7	CNT_L6	CNT_L5	CNT_L4	CNT_L3	CNT_L2	CNT_L1	CNT_L0
X3D	CNTH	R	CNL_H15	CNL_H14	CNL_H13	CNL_H12	CNL_H11	CNL_H10	CNL_H9	CNL_H8
X3E	REFC	R/W	-	-	-	-	-	-	-	REFH_LOS

* note: In the 'Address' column, the 'X' represents 0 ~ 7 corresponding to the eight links.

© 2019 Renesas Electronics Corporation

4.3 REGISTER DESCRIPTION

4.3.1 GLOBAL REGISTERS

Table-29 ID: Chip Revision Register

(R, Address = 02H)

Symbol	Bit	Default	Description
ID[7:0]	7-0	01H	Current Silicon Chip ID.

Table-30 RST: Reset Register

(W, Address = 04H)

Symbol	Bit	Default	Description
RST[7:0]	7-0	01H	Software reset. A write operation on this register will reset all internal registers to their default values, and the status of all ports are set to the default status. The content in this register can not be changed. After reset, all drivers output are in high impedance state. Note: Bit T1E1 (GCF0, 20H) will keep set value and will not be reset.

Table-31 MON: G.772 Monitor control Register

(R/W, Address = 05H)

Symbol	Bit	Default	Description
-	7-4	0	Reserved
MON[3:0]	3-0	0000	MON selects the transmitter or receiver channel to be monitored. = 0000: receiver 1 is in normal operation without monitoring = 0001: monitor receiver 2 = 0010: monitor receiver 3 = 0011: monitor receiver 4 = 0100: monitor receiver 5 = 0101: monitor receiver 6 = 0110: monitor receiver 7 = 0111: monitor receiver 8 = 1000: transmitter 1 is in normal operation without monitoring = 1001: monitor transmitter 2 = 1010: monitor transmitter 3 = 1011: monitor transmitter 4 = 1100: monitor transmitter 5 = 1101: monitor transmitter 6 = 1110: monitor transmitter 7 = 1111: monitor transmitter 8

Table-32 GPIO: General Purpose IO Pin Definition Register

(R/W, Address = 06H)

Symbol	Bit	Default	Description
-	7-4	0000	Reserved.
LEVEL1	3	-	When GPIO1 is defined as an output port, this bit determines the output level on GPIO1 pin. = 0: low level output on port GPIO1 = 1: high level output on port GPIO1 When GPIO1 is defined as an input port, this bit reflects the input level of GPIO1 pin. = 0: low level input on port GPIO1 = 1: high level input on port GPIO1

© 2019 Renesas Electronics Corporation

Table-32 GPIO: General Purpose IO Pin Definition Register (Continued)

(R/W, Address = 06H)

Symbol	Bit	Default	Description
LEVEL0	2	-	When GPIO0 is defined as an output port, this bit determines the output level on GPIO0 pin. = 0: low level output on port GPIO0 = 1: high level output on port GPIO0 When GPIO0 is defined as an input port, this bit reflects the input level on GPIO0 pin = 0: low level input on port GPIO0 = 1: high level input on port GPIO0
DIR1	1	1	= 0: port GPIO1 is configured as output port = 1: port GPIO1 is configured as input port
DIR0	0	1	= 0: port GPIO0 is configured as output port = 1: port GPIO0 is configured as input port

Table-33 REFOUT: Reference clock output select Register

(R/W, Address = 07H)

Symbol	Bit	Default	Description
-	7-6	00	Reserved
RO2[2:0]	5-3	000	= 000: RCLK1 internally loop to REFB output pin = 001: RCLK2 internally loop to REFB output pin = 010: RCLK3 internally loop to REFB output pin = 011: RCLK4 internally loop to REFB output pin = 000: RCLK5 internally loop to REFB output pin = 101: RCLK6 internally loop to REFB output pin = 110: RCLK7 internally loop to REFB output pin = 111: RCLK8 internally loop to REFB output pin
RO1[2:0]	2-0	000	= 000: RCLK1 internally loop to REFA output pin = 001: RCLK2 internally loop to REFA output pin = 010: RCLK3 internally loop to REFA output pin = 011: RCLK4 internally loop to REFA output pin = 100: RCLK5 internally loop to REFA output pin = 101: RCLK6 internally loop to REFA output pin = 110: RCLK7 internally loop to REFA output pin = 111: RCLK8 internally loop to REFA output pin

Table-34 INTCH: Interrupt Channel Indication Register

(R, Address = 09H)

Symbol	Bit	Default	Description
INT_CH[7:0]	7-0	00H	INT_CH[n]=1 indicates that an interrupt was generated by channel [n+1] respectively.

Table-35 TIMER INTE: Timer Interrupt Enable Register

(R, Address = 0CH)

Symbol	Bit	Default	Description
-	7-1	000000	Reserved.
TMOVIE	0	0	= 0: mask interrupt = 1: enable timer over interrupt

© 2019 Renesas Electronics Corporation

Table-36 TIMER INTS: Timer Interrupt Status Register

(bit TMOV_IS is reset after writing a 1 into this bit position)(R, Address = 0DH)

Symbol	Bit	Default	Description
-	7-1	000000	Reserved.
TMOVIS	0	0	Indicate One second timer whether is over or not. = 0: One second timer is not over since last reset TMOVIS. = 1: One second timer is over and generate an interrupt request if no masked.

4.3.2 PER CHANNEL CONTROL REGISTERS

Table-37 TIE1 MODE: T1 or E1 Mode Select Register

(R/W, Address = X20H)

Symbol	Bit	Default	Description
-	7-1	000000	Reserved
TEMODE	0	0	This bit selects the operating mode for the current link. = 0: E1 mode is selected. = 1: T1/J1 mode is selected.

4.3.3 TRANSMIT PATH CONTROL REGISTERS

Table-38 TJACF: Jitter Attenuator Configuration Register for Transmit Path

(R/W, Address = X21H)

<table>
<tr><th>Symbol</th><th>Bit</th><th>Default</th><th colspan="3">Description</th></tr>
<tr><td>-</td><td>7-6</td><td>00</td><td colspan="3">Reserved</td></tr>
<tr><td>TJITT_TEST</td><td>5</td><td>0</td><td colspan="3">This bit selects jitter measure mode
= 0: real time mode (update jitter measuring value each received clock cycle)
= 1: accumulation mode (measuring p-p value of jitter since last read)</td></tr>
<tr><td>TJA_LIMIT</td><td>4</td><td>1</td><td colspan="3">Wide Jitter Attenuation bandwidth
= 0: normal mode
= 1: JA limit mode</td></tr>
<tr><td>TJA_E</td><td>3</td><td>00</td><td colspan="3">Jitter Attenuator configuration
= 0: JA not used
= 1: JA enabled</td></tr>
<tr><td>TJA_DP[1:0]</td><td>2-1</td><td>00</td><td colspan="3">Jitter Attenuator depth selection
= 00: 128 bits
= 01: 64 bits
= 10/11: 32 bits</td></tr>
<tr><td rowspan="4">TJA_BW</td><td rowspan="4">0</td><td rowspan="4">0</td><td colspan="3">Jitter transfer function bandwidth selection</td></tr>
<tr><td>JABW</td><td>T1/J1</td><td>E1</td></tr>
<tr><td>0</td><td>5 Hz</td><td>6.77 Hz</td></tr>
<tr><td>1</td><td>1.26 Hz</td><td>0.87 Hz</td></tr>
</table>

Table-39 TCF0: Transmitter Configuration Register 0 for Transmit Path

(R/W, Address = X22H)

Symbol	Bit	Default	Description
-	7-5	000	Reserved

© 2019 Renesas Electronics Corporation

Table-39 TCF0: Transmitter Configuration Register 0 for Transmit Path (Continued)

(R/W, Address = X22H)

Symbol	Bit	Default	Description
T_OFF	4	0	Transmitter power down enable = 0: Transmitter power up = 1: Transmitter power down and line driver high impedance
TD_INV	3	0	Transmit data invert = 0: data on TDn or TDPn/TDNn is active high = 1: data on TDn or TDPn/TDNn is active low
TCLK_SEL	2	0	Transmit clock edge select = 0: data on TDn or TDPn/TDNn is sampled on the falling edges of TCLKn = 1: data on TDn or TDPn/TDNn is sampled on the rising edges of TCLKn
T_MD[1:0]	1-0	00	Transmitter operation mode control bits which select different stages of transmit data path = 00: enable HDB3/B8ZS encoder and waveform shaper blocks, input on TDn is single rail NRZ data = 01: enable AMI encoder and waveform shaper blocks, input on pin TDn is single rail NRZ data = 1x: encoder is bypassed, dual rail NRZ transmit data input on pin TDPn/TDNn

Table-40 TCF1: Transmitter Configuration Register 1 for Transmit Path

(R/W, Address = X23H)

<table>
<tr><th>Symbol</th><th>Bit</th><th>Default</th><th colspan="6">Description</th></tr>
<tr><td>-</td><td>7-6</td><td>00</td><td colspan="6">Reserved. This bit should be ‘0’ for normal operation.</td></tr>
<tr><td>DFM_OFF</td><td>5</td><td>0</td><td colspan="6">Transmit driver failure monitor disable
= 0: DFM is enabled
= 1: DFM is disabled</td></tr>
<tr><td>THZ</td><td>4</td><td>1</td><td colspan="6">Transmit line driver high impedance enable
= 0: normal state
= 1: transmit line driver high impedance enable (other transmit path still in normal state)</td></tr>
<tr><td rowspan="15">PULS[3:0]</td><td rowspan="15">3-0</td><td rowspan="15">0000</td><td colspan="6">These bits select the transmit template/LBO for short-haul/long-haul applications.</td></tr>
<tr><td></td><td>T1/E1/J1</td><td>TCLK</td><td>Cable Impedance</td><td>Cable Range or LBO</td><td>Cable Loss</td></tr>
<tr><td>0000[1]</td><td>E1</td><td>2.048 MHz</td><td>75 Ω</td><td>-</td><td>0~43 dB (default)</td></tr>
<tr><td>0001</td><td>E1</td><td>2.048 MHz</td><td>120 Ω</td><td>-</td><td>0~43 dB</td></tr>
<tr><td>0010</td><td>DSX1</td><td>1.544 MHz</td><td>100 Ω</td><td>0~133 ft</td><td>0~0.6 dB</td></tr>
<tr><td>0011</td><td>DSX1</td><td>1.544 MHz</td><td>100 Ω</td><td>133~266 ft</td><td>0.6~1.2 dB</td></tr>
<tr><td>0100</td><td>DSX1</td><td>1.544 MHz</td><td>100 Ω</td><td>266~399 ft</td><td>1.2~1.8 dB</td></tr>
<tr><td>0101</td><td>DSX1</td><td>1.544 MHz</td><td>100 Ω</td><td>399~533 ft</td><td>1.8~2.4 dB</td></tr>
<tr><td>0110</td><td>DSX1</td><td>1.544 MHz</td><td>100 Ω</td><td>533~655 ft</td><td>2.4~3.0 dB</td></tr>
<tr><td>0111</td><td>J1</td><td>1.544 MHz</td><td>110 Ω</td><td>0~655 ft</td><td>0~3.0 dB</td></tr>
<tr><td>1000</td><td>DS1</td><td>1.544 MHz</td><td>100 Ω</td><td>0 dB LBO</td><td>0~36 dB</td></tr>
<tr><td>1001</td><td>DS1</td><td>1.544 MHz</td><td>100 Ω</td><td>-7.5 dB LBO</td><td>0~28.5 dB</td></tr>
<tr><td>1010</td><td>DS1</td><td>1.544 MHz</td><td>100 Ω</td><td>-15 dB LBO</td><td>0~21 dB</td></tr>
<tr><td>1011</td><td>DS1</td><td>1.544 MHz</td><td>100 Ω</td><td>-22.5 dB LBO</td><td>0~13.5 dB</td></tr>
<tr><td>11xx</td><td colspan="5">User programmable waveform setting</td></tr>
</table>

1. In internal impedance matching mode, for E1/75 Ω cable impedance, the PULS[3:0] bits (TCF1, X23H) should be set to ‘0000’. In external impedance matching mode, for E1/75 Ω cable impedance, the PULS[3:0] bits should be set to ‘0001’.

© 2019 Renesas Electronics Corporation

Table-41 TCF2: Transmitter Configuration Register 2 for Transmit Path

(R/W, Address = X24H)

Symbol	Bit	Default	Description
-	7-6	00	Reserved
SCAL[5:0]	5-0	100001	SCAL specifies a scaling factor to be applied to the amplitude of the user-programmable arbitrary pulses which is to be transmitted if needed. The default value of SCAL[5:0] is '100001'. Refer to 3.2.3.3 User-Programmable Arbitrary Waveform. = 110110: default value for T1 0~133 ft, T1 133~266 ft, T1 266~399 ft, T1 399~533 ft, T1 533~655 ft, J1 0~655 ft, DS1 0dB LBO. One step change of this value results in 2% scaling up/down against the pulse amplitude. = 010001: default value for DS1 -7.5 dB LBO. One step change of this value results in 6.25% scaling up/down against the pulse amplitude. = 001000: default value for DS1 -15.0 dB LBO. One step change of this value results in 12.5% scaling up/down against the pulse amplitude. = 000100: default value for DS1 -22.5 dB LBO. One step change of this value results in 25% scaling up/down against the pulse amplitude. = 100001: default value for E1 75 Ω and 120 Ω. One step change of this value results in 3% scaling up/down against the pulse amplitude.

Table-42 TCF3: Transmitter Configuration Register 3 for Transmit Path

(R/W, Address = X25H)

Symbol	Bit	Default	Description
DONE	7	0	After '1' is written to this bit, a read or write operation is implemented.
RW	6	0	This bit selects read or write operation = 0: write to RAM = 1: read from RAM
UI[1:0]	5-4	00	These bits specify the unit interval address. There are 4 unit intervals. = 00: UI address is 0 (The most left UI) = 01: UI address is 1 = 10: UI address is 2 = 11: UI address is 3
SAMP[3:0]	3-0	0000	These bits specify the sample address. Each UI has 16 samples. = 0000: sample address is 0 (The most left Sample) = 0001: sample address is 1 = 0010: sample address is 2 ..... = 1110: sample address is 14 = 1111: sample address is 15

Table-43 TCF4: Transmitter Configuration Register 4 for Transmit Path

(R/W, Address = X26H)

Symbol	Bit	Default	Description
-	7	0	Reserved
WDAT[6:0]	6-0	0000000	In Indirect Write operation, the WDAT[6:0] will be loaded to the pulse template RAM, specifying the amplitude of the Sample. After an Indirect Read operation, the amplitude data of the Sample in the pulse template RAM will be output to the WDAT[6:0].

© 2019 Renesas Electronics Corporation

4.3.4 RECEIVE PATH CONTROL REGISTERS

Table-44 RJACF: Jitter Attenuator Configuration Register for Receive Path

(R/W, Address = X27H)

Symbol	Bit	Default	Description
-	7-6	00	Reserved
RJITT_TEST	5	0	This bit selects jitter measure mode = 0: real time mode (update jitter measuring value each received clock cycle) = 1: accumulation mode (measuring p-p value of jitter since last read)
RJA_LIMIT	4	1	Wide Jitter Attenuation bandwidth = 0: normal mode = 1: JA limit mode
RJA_E	3	00	Jitter Attenuator configuration = 0: JA not used = 1: JA enabled
RJA_DP[1:0]	2-1	00	Jitter Attenuator depth selection = 00: 128 bits = 01: 64 bits = 10/11: 32 bits
RJA_BW	0	0	Jitter transfer function bandwidth selection

JABW	T1/J1	E1
0	5 Hz	6.77 Hz
1	1.26 Hz	0.87 Hz

Table-45 RCF0: Receiver Configuration Register 0 for Receive Path

(R/W, Address = X28H)

Symbol	Bit	Default	Description
-	7-5	000	Reserved
R_OFF	4	0	Receiver power down enable = 0: Receiver power up = 1: Receiver power down
RD_INV	3	0	Receive data invert = 0: data on RDn or RDPn/RDNn is active high = 1: data on RDn or RDPn/RDNn is active low
RCLK_SEL	2	0	Receive clock edge select (this bit is ignored in slicer mode) = 0: data on RDn or RDPn/RDNn is updated on the rising edges of RCLKn = 1: data on RDn or RDPn/RDNn is updated on the falling edges of RCLKn
R_MD[1:0]	1-0	00	Receiver path decoding selection = 00: receive data is HDB3 (E1) / B8ZS (T1/J1) decoded and output on RDn with single rail NRZ format = 01: receive data is AMI decoded and output on RDn with single rail NRZ format = 10: decoder is bypassed, re-timed dual rail data with NRZ format output on RDPn/RDNn (dual rail mode with clock recovery) = 11: both CDR and decoder blocks are bypassed, slicer data with RZ format output on RDPn/RDNn (slicer mode)

© 2019 Renesas Electronics Corporation

Table-46 RCF1: Receiver Configuration Register 1 for Receive Path

(R/W, Address = X29H)

Symbol	Bit	Default	Description		
-	7	0	Reserved		
EQ_ON	6	0	= 0: receive equalizer off (short haul receiver) = 1: receive equalizer on (long haul receiver)		
FIXG	5	0	Select fix gain or LOS level detect threshold. Note that this bit is effective only when long haul operation mode is selected (EQ_ON=1). = 0: the receiver operates in adaptive gain mode, in which the maximum receive sensitivity is up to 43 dB for E1 and 36 dB for T1. = 1: fixed gain mode. The receive sensitivity is fixed on the value selected by LOS[4:0].		
LOS[4:0]	4-0	10101		LOS Clear Level (dB)	LOS Declare Level (dB)
			00000	0	<-4
			00001	>-2	<-6
			00010	>-4	<-8
			00011	>-6	<-10
			00100	>-8	<-12
			00101	>-10	<-14
			00110	>-12	<-16
			00111	>-14	<-18
			01000	>-16	<-20
			01001	>-18	<-22
			01010	>-20	<-24
			01011	>-22	<-26
			01100	>-24	<-28
			01101	>-26	<-30
			01110	>-28	<-32
			01111	>-30	<-34
			10000	>-32	<-36
			10001	>-34	<-38
			10010	>-36	<-40
			10011	>-38	<-42
			10100	>-40	<-44
			10101	>-42	<-46
			10110-11111	>-44	<-48

© 2019 Renesas Electronics Corporation

Table-47 RCF2: Receiver Configuration Register 2 for Receive Path

(R/W, Address = X2AH)

Symbol	Bit	Default	Description
-	7-6	00	Reserved
SLICE[1:0]	5-4	01	Receive slicer threshold = 00: The receive slicer generates a mark if the voltage on RTIPn/RRINGn exceeds 40% of the peak amplitude. = 01: The receive slicer generates a mark if the voltage on RTIPn/RRINGn exceeds 50% of the peak amplitude. = 10: The receive slicer generates a mark if the voltage on RTIPn/RRINGn exceeds 60% of the peak amplitude. = 11: The receive slicer generates a mark if the voltage on RTIPn/RRINGn exceeds 70% of the peak amplitude.
UPDW[1:0]	3-2	10	Equalizer observation window = 00: 32 bits = 01: 64 bits = 10: 128 bits = 11: 256 bits
MG[1:0]	1-0	00	Monitor gain setting: these bits select the internal linear gain boost = 00: 0 dB = 01: 22 dB = 10: 26 dB = 11: 32 dB

4.3.5 NETWORK DIAGNOSTICS CONTROL REGISTERS

Table-48 MAINT0: Maintenance Function Control Register 0

(R/W, Address = X2BH)

Symbol	Bit	Default	Description
-	7-4	0000	Reserved
ARLP	3	0	Automatic Remote Loopback Control = 0: disables Automatic Remote Loopback (normal transmit and receive operation) = 1: enables Automatic Remote Loopback
RLP	2	0	Remote loopback enable = 0: disables remote loopback (normal transmit and receive operation) = 1: enables remote loopback
ALP	1	0	Analog loopback enable = 0: disables analog loopback (normal transmit and receive operation) = 1: enables analog loopback
DLP	0	0	Digital loopback enable = 0: disables digital loopback (normal transmit and receive operation) = 1: enables digital loopback

Table-49 MAINT1: Maintenance Function Control Register 1

(R/W, Address = X2CH)

Symbol	Bit	Default	Description
-	7	0	Reserved
PATT[1:0]	6-5	00	These bits select the internal pattern and insert it into the transmit data stream. = 00: normal operation (PATT_CLK = 0) / insert all zeros (PATT_CLK = 1) = 01: insert All Ones = 10: insert PRBS (E1: 2^{15}-1) or QRSS (T1/J1: 2^{20}-1) = 11: insert programmable Inband Loopback activate or deactivate code

© 2019 Renesas Electronics Corporation

Table-49 MAINT1: Maintenance Function Control Register 1 (Continued)

(R/W, Address = X2CH)

Symbol	Bit	Default	Description
PATT_CLK	4	0	Selects reference clock for transmitting internal pattern = 0: uses TCLKn as the reference clock = 1: uses MCLK as the reference clock
PRBS_INV	3	0	Inverts PRBS = 0: PRBS data is not inverted = 1: PRBS data is inverted before transmission and detection
LAC	2	0	The LOS/AIS criterion is selected as below: = 0: G.775 (E1) / T1.231 (T1/J1) = 1: ETSI 300233 & I.431 (E1) / I.431 (T1/J1)
RAISE	1	0	AIS enable during LOS = 0: AIS insertion on RDPn/RDNn/RCLKn is disabled during LOS = 1: AIS insertion on RDPn/RDNn/RCLKn is enabled during LOS
ATAO	0	0	Automatically Transmit All Ones during LOS (enabled only when PATT[1:0] = 00) = 0: disabled = 1: Automatically Transmit All Ones pattern at TTIPn/TRINGn during LOS.

Table-50 MAINT2: Maintenance Function Control Register 2

(R/W, Address = X2DH)

Symbol	Bit	Default	Description
-	7-6	00	Reserved.
TNLP_L[1:0]	5-4	00	Defines the length of the user-programmable transmit Inband Loopback activate/deactivate code contained in TNLP register. The default selection is 5 bits length. = 00: 5-bit activate code in TNLP [4:0] = 01: 6-bit activate code in TNLP [5:0] = 10: 7-bit activate code in TNLP [6:0] = 11: 8-bit activate code in TNLP [7:0]
RNLPA_L[1:0]	3-2	00	Defines the length of the user-programmable receive Inband Loopback activate code contained in RNLPA register. = 00: 5-bit activate code in RNLPA [4:0] = 01: 6-bit activate code in RNLPA [5:0] = 10: 7-bit activate code in RNLPA [6:0] = 11: 8-bit activate code in RNLPA [7:0]
RNLPD_L[1:0]	1-0	01	Defines the length of the user-programmable receive Inband Loopback deactivate code contained in RNLPD register. = 00: 5-bit deactivate code in RNLPD [4:0] = 01: 6-bit deactivate code in RNLPD [5:0] = 10: 7-bit deactivate code in RNLPD [6:0] = 11: 8-bit deactivate code in RNLPD [7:0]

Table-51 MAINT3: Maintenance Function Control Register 3

(R/W, Address = X2EH)

Symbol	Bit	Default	Description
TNLP[7:0]	7-0	(000)00001	Defines the user-programmable transmit Inband Loopback activate/deactivate code. The default selection is 00001. TNLP[7:0] form the 8-bit repeating code TNLP[6:0] form the 7-bit repeating code TNLP[5:0] form the 6-bit repeating code TNLP[4:0] form the 5-bit repeating code

© 2019 Renesas Electronics Corporation

Table-52 MAINT4: Maintenance Function Control Register 4

(R/W, Address = X2FH)

Symbol	Bit	Default	Description
RNLPA[7:0]	7-0	(000)00001	Defines the user-programmable receive Inband Loopback activate code. The default selection is 00001. RNLPA[7:0] form the 8-bit repeating code RNLPA[6:0] form the 7-bit repeating code RNLPA[5:0] form the 6-bit repeating code RNLPA[4:0] form the 5-bit repeating code

Table-53 MAINT5: Maintenance Function Control Register 5

(R/W, Address =X30H)

Symbol	Bit	Default	Description
RNLPD[7:0]	7-0	(00)001001	Defines the user-programmable receive Inband Loopback deactivate code. The default selection is 001001. RNLPD[7:0] form the 8-bit repeating code RNLPD[6:0] form the 7-bit repeating code RNLPD[5:0] form the 6-bit repeating code RNLPD[4:0] form the 5-bit repeating code

Table-54 MAINT6: Maintenance Function Control Register 6

(R/W, Address = X31H)

Symbol	Bit	Default	Description
-	7	0	Reserved.
BPV_INS	6	0	BPV error insertion A ‘0’ to ‘1’ transition on this bit will cause a single bipolar violation error to be inserted into the transmit data stream. This bit must be cleared and set again for a subsequent error to be inserted.
ERR_INS	5	0	PRBS/QRSS logic error insertion A ‘0’ to ‘1’ transition on this bit will cause a single PRBS/QRSS logic error to be inserted into the transmit PRBS/QRSS data stream. This bit must be cleared and set again for subsequent error to be inserted.
EXZ_DEF	4	0	EXZ definition select = 0: ANSI = 1: FCC
ERR_SEL[1:0]	3-2	00	These bits choose which type of error will be counted = 00: the PRBS logic error is counted by a 16-bit error counter. = 01: the EXZ error is counted by a 16-bit error counter. = 10: the Received CV (BPV) error is counted by a 16-bit error counter. = 11: both CV (BPV) and EXZ errors are counted by a 16-bit error counter.
CNT_MD	1	0	Counter operation mode select = 0: Manual Report Mode = 1: Auto Report Mode
CNT_STOP	0	0	= 0: Enable counter. = 1: Counter is latched.

© 2019 Renesas Electronics Corporation

4.3.6 TRANSMIT AND RECEIVE TERMINATION REGISTER

Table-55 TERM: Transmit and Receive Termination Configuration Register

(R/W, Address = X32H)

Symbol	Bit	Default	Description
-	7-6	00	Reserved
T_TERM[2:0]	5-3	000	These bits select the internal termination for transmit line impedance matching. = 000: internal 75 Ω impedance matching = 001: internal 120 Ω impedance matching = 010: internal 100 Ω impedance matching = 011: internal 110 Ω impedance matching =1xx: Selects external impedance matching resistors for E1 mode only. T1/J1 does not require external impedance resistors (see Table-14).
R_TERM[2:0]	2-0	000	These bits select the internal termination for receive line impedance matching. = 000: internal 75 Ω impedance matching = 001: internal 120 Ω impedance matching = 010: internal 100 Ω impedance matching = 011: internal 110 Ω impedance matching = 1xx: Selects external impedance matching resistors (see Table-16).

4.3.7 INTERRUPT CONTROL REGISTERS

Table-56 INTENC0: Interrupt Mask Register 0

(R/W, Address = X33H)

Symbol	Bit	Default	Description
-	7	0	Reserved.
NLPA_IE	6	0	In-band Loopback activate code detect interrupt mask = 1: In-band Loopback activate code detect interrupt enabled = 0: In-band Loopback activate code detect interrupt masked
NLPD_IE	5	0	In-band Loopback deactivate code detect interrupt mask = 1: In-band Loopback deactivate code detect interrupt enabled = 0: In-band Loopback deactivate code detect interrupt masked
PRBS_IE	4	0	PRBS synchronic signal detect interrupt mask = 1: PRBS synchronic signal detect interrupt enabled = 0: PRBS synchronic signal detect interrupt masked
TCLK_IE	3	0	TCLK loss detect interrupt mask = 1: TCLK loss detect interrupt enabled = 0: TCLK loss detect interrupt masked
DF_IE	2	0	Driver failure interrupt mask = 1: Driver failure interrupt enabled = 0: Driver failure interrupt masked
AIS_IE	1	0	Alarm Indication Signal interrupt mask = 1: Alarm Indication Signal interrupt enabled = 0: Alarm Indication Signal interrupt masked
LOS_IE	0	0	Loss Of Signal interrupt mask = 1: Loss Of Signal interrupt enabled = 0: Loss Of Signal interrupt masked

© 2019 Renesas Electronics Corporation

Table-57 INTENC1: Interrupt Mask Register 1

(R/W, Address = X34H)

Symbol	Bit	Default	Description
-	7	0	Reserved.
DAC_IE	6	0	DAC arithmetic overflow interrupt mask = 1: DAC arithmetic overflow interrupt enabled = 0: DAC arithmetic overflow interrupt masked
TJA_IE	5	0	JA in transmit path overflow/underflow interrupt mask = 1: JA overflow interrupt enabled = 0: JA overflow interrupt masked
RJA_IE	4	0	JA in receive path overflow/underflow interrupt mask = 1: JA underflow interrupt enabled = 0: JA underflow interrupt masked
ERR_IE	3	0	PRBS/QRSS logic error detect interrupt mask = 1: PRBS/QRSS logic error detect interrupt enabled = 0: PRBS/QRSS logic error detect interrupt masked
EXZ_IE	2	0	Receive excess zeros interrupt mask = 1: Receive excess zeros interrupt enabled = 0: Receive excess zeros interrupt masked
CV_IE	1	0	Receive error interrupt mask = 1: Receive error interrupt enabled = 0: Receive error interrupt masked
CNT_IE	0	0	Counter overflow interrupt mask = 1: Counter overflow interrupt enabled = 0: Counter overflow interrupt masked

© 2019 Renesas Electronics Corporation

Table-58 INTES: Interrupt Trigger Edges Select Register

(R/W, Address = X35H)

Symbol	Bit	Default	Description
-	7	0	Reserved.
NLPA_IES	6	0	This bit determines the Inband Loopback Activate Code interrupt event. = 0: interrupt event is defined as a '0' to '1' transition of the NLPA_S bit in the STAT0 status register = 1: interrupt event is defined as either a '0' to '1' transition or a '1' to '0' transition of the NLPA_S bit in the STAT0 status register.
NLPD_IES	5	0	This bit determines the Inband Loopback Deactivate Code interrupt event. = 0: interrupt event is defined as a '0' to '1' transition of the NLPD_S bit in the STAT0 status register = 1: interrupt event is defined as either a '0' to '1' transition or a '1' to '0' transition of the NLPD_S bit in the STAT0 status register.
PRBS_IES	4	0	This bit determines the PRBS/QRSS synchronization status interrupt event. = 0: interrupt event is defined as a '0' to '1' transition of the PRBS_S bit in the STAT0 status register = 1: interrupt event is defined as either a '0' to '1' transition or a '1' to '0' transition of the PRBS_S bit in the STAT0 status register.
TCLK_IES	3	0	This bit determines the TCLK Loss interrupt event. = 0: interrupt event is defined as a '0' to '1' transition of the TCLK_LOS bit in the STAT0 status register = 1: interrupt event is defined as either a '0' to '1' transition or a '1' to '0' transition of the TCLK_LOS bit in the STAT0 status register.
DF_IES	2	0	This bit determines the Driver Failure interrupt event. = 0: interrupt event is defined as a '0' to '1' transition of the DF_S bit in the STAT0 status register = 1: interrupt event is defined as either a '0' to '1' transition or a '1' to '0' transition of the DF_S bit in the STAT0 status register.
AIS_IES	1	0	This bit determines the AIS interrupt event. = 0: interrupt event is defined as a '0' to '1' transition of the AIS_S bit in the STAT0 status register = 1: interrupt event is defined as either a '0' to '1' transition or a '1' to '0' transition of the AIS_S bit in the STAT0 status register.
LOS_IES	0	0	This bit determines the LOS interrupt event. = 0: interrupt event is defined as a '0' to '1' transition of the LOS_S bit in the STAT0 status register = 1: interrupt event is defined as either a '0' to '1' transition or a '1' to '0' transition of the LOS_S bit in the STAT0 status register.

© 2019 Renesas Electronics Corporation

4.3.8 LINE STATUS REGISTERS

Table-59 STAT0: Line Status Register 0 (real time status monitor)

(R, Address = X36H)

Symbol	Bit	Default	Description
ARLP_S	7	0	Indicating the auto remote loop back status = 0: The remote loop is inactive. If enabled auto remote loop back by setting bit ARLP, the remote loop is switched off automatically upon detection of the in-band loop deactivate code for at least 5.1 s, according to ANSI T1. 403 requirements. =1: The remote loop is active (closed). If enabled by bit ARLP, the remote loop is switched on automatically upon detection of the in-band loop activate code for at least 5.1 s.
NLPA_S	6	0	Inband Loopback activate code receive status indication = 0: no Inband Loopback activate code is detected = 1: activate code has been detected for more than t ms. Even there is bit error, this bit remains set as long as the bit error rate is less than 10^{-2}. Note1: If automatic remote loop switching is disabled (ARLP = 0), t = 40 ms If automatic remote loop switching is enabled (ARLP = 1), t= 5.1s. The rising edge of this bit actives the remote loop operation in local end. Note2: If NLPA_IE=1, 0 to 1 transition on this bit causes an activate code detected interrupt if NLPA _IES bit is 0; Any change of this bit causes an activate code detected interrupt if NLPA _IES bit is set to 1.
NLPD_S	5	0	Inband Loopback deactivate code receive status indication = 0: no Inband Loopback deactivate code is detected = 1: the Inband Loopback deactivate code has been detected for more than t. Even there is a bit error, this bit remains set as long as the bit error rate is less than 10^{-2}. Note 1: If automatic remote loop switching is disabled (ARLP = 0), t = 40 ms.If automatic remote loop switching is enabled (ARLP = 1), t= 5.1s. The rising edge of this bit disables the remote loop back operation. Note2: If NLPD_IE=1, a 0 to 1 transition on this bit causes a deactivate code detected interrupt if NLPD _IES bit is 0 Any change of this bit causes a deactivate code detected interrupt if NLPD _IES bit is set to 1.
PRBS_S	4	0	Synchronous status indication of PRBS/QRSS (real time) = 0: 2^{15}-1 (E1) PRBS or 2^{20}-1 (T1/J1) QRSS is not detected = 1: 2^{15}-1 (E1) PRBS or 2^{20}-1 (T1/J1) QRSS is detected. Note: If PRBS_IE=1, 0 to 1 transition on this bit causes an Synchronous status detected interrupt if PRBS _IES bit is 0 Any change of this bit causes an interrupt if PRBS_IES bit is set to 1.
TCLK_LOS	3	0	TCLKn loss indication = 0: normal = 1: TCLKn pin has not toggled for more than 70 MCLK cycles. Note: If TCLK_LOS_IE=1, 0 to 1 transition on this bit causes an interrupt if TCLK _IES bit is 0 Any change of this bit causes an interrupt if TCLK_IES bit is set to 1.

© 2019 Renesas Electronics Corporation

Table-59 STAT0: Line Status Register 0 (real time status monitor) (Continued)

(R, Address = X36H)

Symbol	Bit	Default	Description
DF_S	2	0	Line driver status indication = 0: normal operation = 1: line driver short circuit is detected. Note: If DF_IE=1, 0 to 1 transition on this bit causes an interrupt if DF _IES bit is 0. Any change of this bit causes an interrupt if DF_IES bit is set to 1.
AIS_S	1	0	Alarm Indication Signal status detection = 0: no AIS signal is detected in the receive path = 1: AIS signal is detected in the receive path Note: If AIS_IE=1, 0 to 1 transition on this bit causes an interrupt if AIS _IES bit is 0. Any change of this bit causes an interrupt if AIS_IES bit is set to 1.
LOS_S	0	0	Loss of Signal status detection = 0: Loss of signal on RTIP/RRING is not detected = 1: Loss of signal on RTIP/RRING is detected Note: If LOS_IE=1, 0 to 1 transition on this bit causes an interrupt if LOS _IES bit is 0 Any change of this bit causes an interrupt if LOS_IES bit is set to 1

© 2019 Renesas Electronics Corporation

Table-60 STAT1: Line Status Register 1 (real time status monitor)

(R, Address = X37H)

Symbol	Bit	Default	Description	
-	7-6	00	Reserved	
-	5	0	Reserved	
LATT[4:0]	4-0	00000	Line Attenuation Indication in dB relative to a 3 V peak pulse level	
			00000	0 to 2 dB
			00001	2 to 4 dB
			00010	4 to 6 dB
			00011	6 to 8 dB
			00100	8 to 10 dB
			00101	10 to 12 dB
			00110	12 to 14 dB
			00111	14 to 16 dB
			01000	16 to 18 dB
			01001	18 to 20 dB
			01010	20 to 22 dB
			01011	22 to 24 dB
			01100	24 to 26 dB
			01101	26 to 28 dB
			01110	28 to 30 dB
			01111	30 to 32 dB
			10000	32 to 34 dB
			10001	34 to 36 dB
			10010	36 to 38 dB
			10011	38 to 40 dB
			10100	40 to 42 dB
			10101	42 to 44 dB
			10110-11111	>44 dB

Table-61 TJITT: Jitter Measure Value Indicate Register (Transmit Path)

(R/W, Address = X38H)

Symbol	Bit	Default	Description
-	7	0	Reserved
TJITT[6:0]	6-0	000000	When TJITT_TEST=0, these bits indicates current jitter measure value. When TJITT_TEST=1, these bits indicates jitter measure P-P value after last read (reset by a read)

Table-62 TJITT: Jitter Measure Value Indicate Register (Receive Path)

(R/W, Address = X39H)

Symbol	Bit	Default	Description
-	7	0	Reserved
RJITT[6:0]	6-0	000000	When RJITT_TEST=0, these bits indicates current jitter measure value. When RJITT_TEST=1, these bits indicates jitter measure P-P value after last read (reset by a read)

© 2019 Renesas Electronics Corporation

4.3.9 INTERRUPT STATUS REGISTERS

Table-63 INTS0: Interrupt Status Register 0

(This register is cleared if a '1' is written to it.) (R/W, Address = X3AH)

Symbol	Bit	Default	Description
-	7	0	Reserved
NLPA_IS	6	0	This bit indicates the occurrence of the Inband Loopback Activate Code interrupt event. = 0: no Inband Loopback Activate Code interrupt event occurred = 1: Inband Loopback Activate Code Interrupt event occurred
NLPD_IS	5	0	This bit indicates the occurrence of the Inband Loopback Deactivate Code interrupt event. = 0: no Inband Loopback Deactivate Code interrupt event occurred = 1: interrupt event of the received inband loopback deactivate code occurred.
PRBS_IS	4	0	This bit indicates the occurrence of the interrupt event generated by the PRBS/QRSS synchronization status. = 0: no PRBS/QRSS synchronization status interrupt event occurred = 1: PRBS/QRSS synchronization status interrupt event occurred
TCLK_LOS_IS	3	0	This bit indicates the occurrence of the interrupt event generated by the TCLKn loss detection. = 0: no TCLKn loss interrupt event. = 1:TCLKn loss interrupt event occurred.
DF_IS	2	0	This bit indicates the occurrence of the interrupt event generated by the Driver Failure. = 0: There is no status change on the DF_S bit (b2, T1/J1-036H,...). = 1: When the DF_IES bit (b2, T1/J1-035H,...) is '0', the '1' on this bit indicates there is a transition from '0' to '1' on the DF_S bit (b2, T1/J1-036H,...); when the DF_IES bit (b2, T1/J1-035H,...) is '1', the '1' on this bit indicates there is a transition from '0' to '1' or from '1' to '0' on the DF_S bit (b2, T1/J1-036H,...).
AIS_IS	1	0	This bit indicates the Alarm Indication Signal Interrupt Status detection. = 0: No AIS happen since last reset AIS_IS = 1: 0 to 1 transition on bit AIS_S if AIS_IES=0, or any change on bit AIS_S if AIS_IES=1
LOS_IS	0	0	This bit indicates the occurrence of the LOS (Loss of signal) interrupt event. = 0: There is no status change on the LOS_S bit (b0, T1/J1-036H,...). = 1: When the LOS_IES bit (b0, T1/J1-035H,...) is '0', the '1' on this bit indicates there is a transition from '0' to '1' on the LOS_S bit (b0, T1/J1-036H,...); when the LOS_IES bit (b0, T1/J1-035H,...) is '1', the '1' on this bit indicates there is a transition from '0' to '1' or from '1' to '0' on the LOS_S bit (b0, T1/J1-036H,...).

© 2019 Renesas Electronics Corporation

Table-64 INTS1: Interrupt Status Register 1

(This register is cleared if a '1' is written to it.) (R/W, Address = X3BH)

Symbol	Bit	Default	Description
-	7	0	Reserved
DAC_IS	6	0	This bit indicates the occurrence of the pulse amplitude overflow of Arbitrary Waveform Generator interrupt event. = 0: no pulse amplitude overflow of Arbitrary Waveform Generator interrupt event occurred = 1: the pulse amplitude overflow of Arbitrary Waveform Generator interrupt event occurred
TJA_IS	5	0	This bit indicates the occurrence of the Jitter Attenuator Overflow interrupt event. = 0: no JA overflow interrupt event occurred = 1: A overflow interrupt event occurred
RJA_IS	4	0	This bit indicates the occurrence of the Jitter Attenuator Underflow interrupt event. = 0: no JA underflow interrupt event occurred = 1: JA underflow interrupt event occurred
ERR_IS	3	0	This bit indicates the occurrence of the interrupt event generated by the detected PRBS/QRSS logic error. = 0: no PRBS logic error has been received since last reset ERR_IS = 1: PRBS/QRSS logic error interrupt event occurred
EXZ_IS	2	0	This bit indicates the occurrence of the Excessive Zeros interrupt event. = 0: no excessive zeros has been received since last reset. EXZ_IS = 1: EXZ interrupt event occurred
CV_IS	1	0	This bit indicates the occurrence of the Code Violation interrupt event. = 0: no code violation is received since last reset CV_IS = 1: code violation has received and generate an interrupt request if no masked
CNTOV_IS	0	0	This bit indicates the occurrence of the Counter Overflow interrupt event. = 0: counter is not over since last reset CNTOV_IS = 1: counter is over and generate an interrupt request if no masked

4.3.10 COUNTER REGISTERS

Table-65 CNTL: Error Counter L-byte Register 0

(R, Address = X3CH)

Symbol	Bit	Default	Description
CNT_L[7:0]	7-0	00H	This register contains the lower eight bits of the 16-bit error counter. CNT_L[0] is the LSB.

Table-66 CNTH: Error Counter H-byte Register 1

(R, Address = X3D)

Symbol	Bit	Default	Description
CNT_H[7:0]	7-0	00H	This register contains the upper eight bits of the 16-bit error counter. CNT_H[7] is the MSB.

Table-67 REFC: E1 Reference Clock Output Control

(R/W, Address = X3E)

Symbol	Bit	Default	Description
-	7-6	000000	Reserved
REFH_LOS:	0	0	In case of LOS, this bit determines the outputs on the REFA_OUT and REFB_OUT pins. = 0: Output MCLK. = 1: Output high level.

© 2019 Renesas Electronics Corporation

5 IEEE STD 1149.1 JTAG TEST ACCESS PORT

The IDT82P5088 supports the digital Boundary Scan Specification as described in the IEEE 1149.1 standards.

The boundary scan architecture consists of data and instruction registers plus a Test Access Port (TAP) controller. Control of the TAP is performed through signals applied to the Test Mode Select (TMS) and Test Clock (TCK) pins. Data is shifted into the registers via the Test Data Input (TDI) pin, and shifted out of the registers via the Test Data Output (TDO) pin. Both TDI and TDO are clocked at a rate determined by TCK.

The JTAG boundary scan registers include BSR (Boundary Scan Register), IDR (Device Identification Register), BR (Bypass Register) and IR (Instruction Register). These will be described in the following pages. Refer to for architecture.

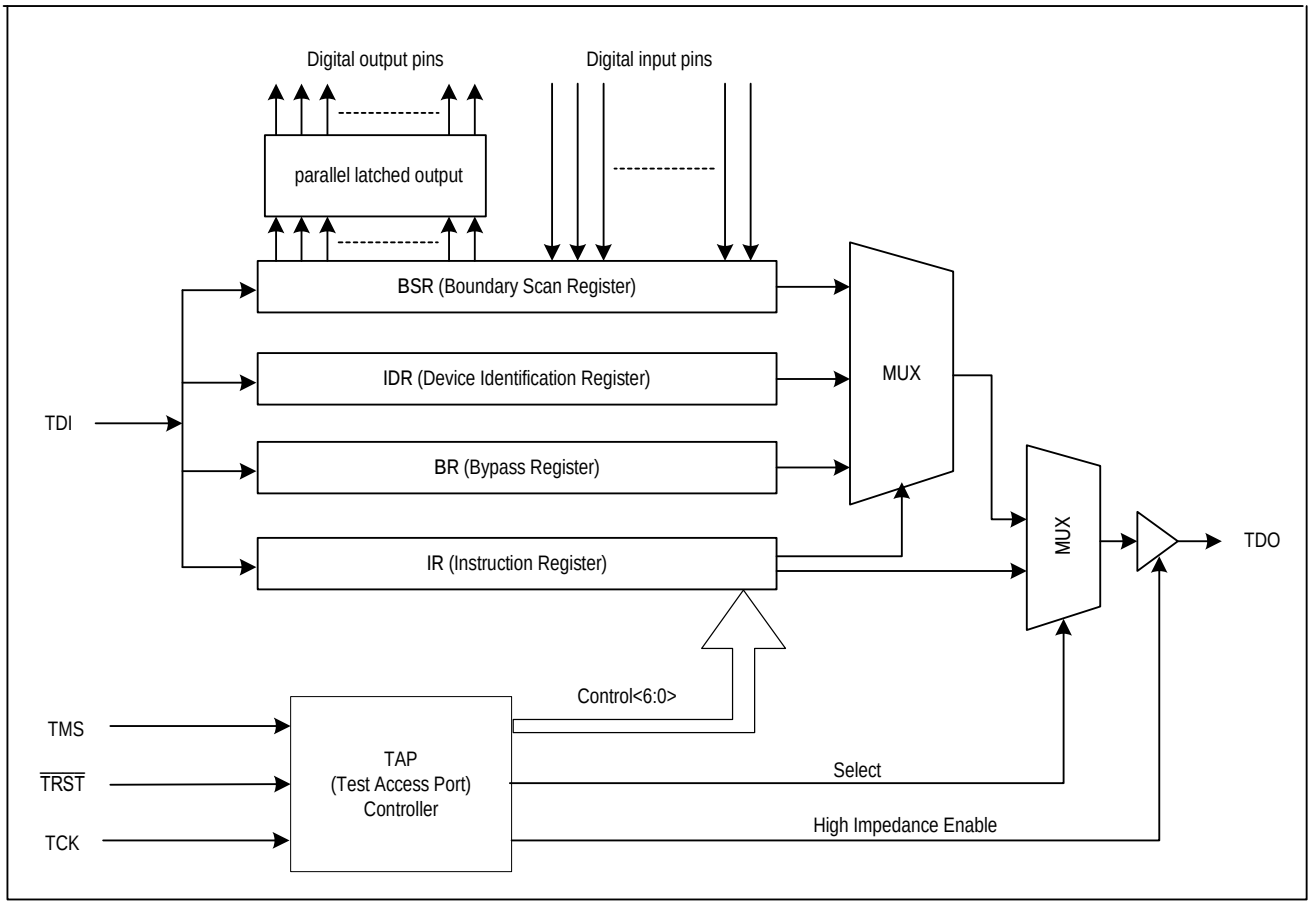


Figure-23 JTAG Architecture

© 2019 Renesas Electronics Corporation

5.1 JTAG INSTRUCTIONS AND INSTRUCTION REGISTER

The IR (Instruction Register) with instruction decode block is used to select the test to be executed or the data register to be accessed or both.

The instructions are shifted in LSB first to this 3-bit register. See Table-68 for details of the codes and the instructions related.

Table-68 Instruction Register Description

IR CODE	INSTRUCTION	COMMENTS
000	Extest	The external test instruction allows testing of the interconnection to other devices. When the current instruction is the EXTEST instruction, the boundary scan register is placed between TDI and TDO. The signal on the input pins can be sampled by loading the boundary scan register using the Capture-DR state. The sampled values can then be viewed by shifting the boundary scan register using the Shift-DR state. The signal on the output pins can be controlled by loading patterns shifted in through input TDI into the boundary scan register using the Update-DR state.
100	Sample / Preload	The sample instruction samples all the device inputs and outputs. For this instruction, the boundary scan register is placed between TDI and TDO. The normal path between IDT82P5088 logic and the I/O pins is maintained. Primary device inputs and outputs can be sampled by loading the boundary scan register using the Capture-DR state. The sampled values can then be viewed by shifting the boundary scan register using the Shift-DR state.
110	Idcode	The identification instruction is used to connect the identification register between TDI and TDO. The device's identification code can then be shifted out using the Shift-DR state.
111	Bypass	The bypass instruction shifts data from input TDI to output TDO with one TCK clock period delay. The instruction is used to bypass the device.

5.2 JTAG DATA REGISTER

5.2.1 DEVICE IDENTIFICATION REGISTER (IDR)

The IDR can be set to define the producer number, part number and the device revision, which can be used to verify the proper version or revision number that has been used in the system under test. The IDR is 32 bits long and is partitioned as in Table-69. Data from the IDR is shifted out to TDO LSB first.

Table-69 Device Identification Register Description

Bit No.	Comments
0	Set to '1'
1-11	Producer Number
12-27	Part Number
28-31	Device Revision

5.2.2 BYPASS REGISTER (BR)

The BR consists of a single bit. It can provide a serial path between the TDI input and TDO output, bypassing the BSR to reduce test access times.

5.2.3 BOUNDARY SCAN REGISTER (BSR)

The BSR can apply and read test patterns in parallel to or from all the digital I/O pins. The BSR is a 98 bits long shift register and is initialized and read using the instruction EXTEST or SAMPLE/PRELOAD. Each pin is related to one or more bits in the BSR. For details, please refer to the BSDL file.

© 2019 Renesas Electronics Corporation

5.2.4 TEST ACCESS PORT CONTROLLER

The TAP controller is a 16-state synchronous state machine. Figure-24 shows its state diagram following the description of each state. Note that the figure contains two main branches to access either the data or instruction registers. The value shown next to each state transition in this figure states the value present at TMS at each rising edge of TCK. Please refer to Table-70 for details of the state description.

Table-70 TAP Controller State Description

STATE	DESCRIPTION
Test Logic Reset	In this state, the test logic is disabled. The device is set to normal operation. During initialization, the device initializes the instruction register with the IDCODE instruction. Regardless of the original state of the controller, the controller enters the Test-Logic-Reset state when the TMS input is held high for at least 5 rising edges of TCK. The controller remains in this state while TMS is high. The device processor automatically enters this state at power-up.
Run-Test/Idle	This is a controller state between scan operations. Once in this state, the controller remains in the state as long as TMS is held low. The instruction register and all test data registers retain their previous state. When TMS is high and a rising edge is applied to TCK, the controller moves to the Select-DR state.
Select-DR-Scan	This is a temporary controller state and the instruction does not change in this state. The test data register selected by the current instruction retains its previous state. If TMS is held low and a rising edge is applied to TCK when in this state, the controller moves into the Capture-DR state and a scan sequence for the selected test data register is initiated. If TMS is held high and a rising edge applied to TCK, the controller moves to the Select-IR-Scan state.
Capture-DR	In this state, the Boundary Scan Register captures input pin data if the current instruction is EXTEST or SAMPLE/PRELOAD. The instruction does not change in this state. The other test data registers, which do not have parallel input, are not changed. When the TAP controller is in this state and a rising edge is applied to TCK, the controller enters the Exit1-DR state if TMS is high or the Shift-DR state if TMS is low.
Shift-DR	In this controller state, the test data register connected between TDI and TDO as a result of the current instruction shifts data on stage toward its serial output on each rising edge of TCK. The instruction does not change in this state. When the TAP controller is in this state and a rising edge is applied to TCK, the controller enters the Exit1-DR state if TMS is high or remains in the Shift-DR state if TMS is low.
Exit1-DR	This is a temporary state. While in this state, if TMS is held high, a rising edge applied to TCK causes the controller to enter the Update-DR state, which terminates the scanning process. If TMS is held low and a rising edge is applied to TCK, the controller enters the Pause-DR state. The test data register selected by the current instruction retains its previous value and the instruction does not change during this state.
Pause-DR	The pause state allows the test controller to temporarily halt the shifting of data through the test data register in the serial path between TDI and TDO. For example, this state could be used to allow the tester to reload its pin memory from disk during application of a long test sequence. The test data register selected by the current instruction retains its previous value and the instruction does not change during this state. The controller remains in this state as long as TMS is low. When TMS goes high and a rising edge is applied to TCK, the controller moves to the Exit2-DR state.
Exit2-DR	This is a temporary state. While in this state, if TMS is held high, a rising edge applied to TCK causes the controller to enter the Update-DR state, which terminates the scanning process. If TMS is held low and a rising edge is applied to TCK, the controller enters the Shift-DR state. The test data register selected by the current instruction retains its previous value and the instruction does not change during this state.
Update-DR	The Boundary Scan Register is provided with a latched parallel output to prevent changes while data is shifted in response to the EXTEST and SAMPLE/PRELOAD instructions. When the TAP controller is in this state and the Boundary Scan Register is selected, data is latched into the parallel output of this register from the shift-register path on the falling edge of TCK. The data held at the latched parallel output changes only in this state. All shift-register stages in the test data register selected by the current instruction retain their previous value and the instruction does not change during this state.
Select-IR-Scan	This is a temporary controller state. The test data register selected by the current instruction retains its previous state. If TMS is held low and a rising edge is applied to TCK when in this state, the controller moves into the Capture-IR state, and a scan sequence for the instruction register is initiated. If TMS is held high and a rising edge is applied to TCK, the controller moves to the Test-Logic-Reset state. The instruction does not change during this state.
Capture-IR	In this controller state, the shift register contained in the instruction register loads a fixed value of '100' on the rising edge of TCK. This supports fault-isolation of the board-level serial test data path. Data registers selected by the current instruction retain their value and the instruction does not change during this state. When the controller is in this state and a rising edge is applied to TCK, the controller enters the Exit1-IR state if TMS is held high, or the Shift-IR state if TMS is held low.
Shift-IR	In this state, the shift register contained in the instruction register is connected between TDI and TDO and shifts data one stage towards its serial output on each rising edge of TCK. The test data register selected by the current instruction retains its previous value and the instruction does not change during this state. When the controller is in this state and a rising edge is applied to TCK, the controller enters the Exit1-IR state if TMS is held high, or remains in the Shift-IR state if TMS is held low.

© 2019 Renesas Electronics Corporation

Table-70 TAP Controller State Description (Continued)

STATE	DESCRIPTION
Exit1-IR	This is a temporary state. While in this state, if TMS is held high, a rising edge applied to TCK causes the controller to enter the Update-IR state, which terminates the scanning process. If TMS is held low and a rising edge is applied to TCK, the controller enters the Pause-IR state. The test data register selected by the current instruction retains its previous value and the instruction does not change during this state.
Pause-IR	The pause state allows the test controller to temporarily halt the shifting of data through the instruction register. The test data register selected by the current instruction retains its previous value and the instruction does not change during this state. The controller remains in this state as long as TMS is low. When TMS goes high and a rising edge is applied to TCK, the controller moves to the Exit2-IR state.
Exit2-IR	This is a temporary state. While in this state, if TMS is held high, a rising edge applied to TCK causes the controller to enter the Update-IR state, which terminates the scanning process. If TMS is held low and a rising edge is applied to TCK, the controller enters the Shift-IR state. The test data register selected by the current instruction retains its previous value and the instruction does not change during this state.
Update-IR	The instruction shifted into the instruction register is latched into the parallel output from the shift-register path on the falling edge of TCK. When the new instruction has been latched, it becomes the current instruction. The test data registers selected by the current instruction retain their previous value.

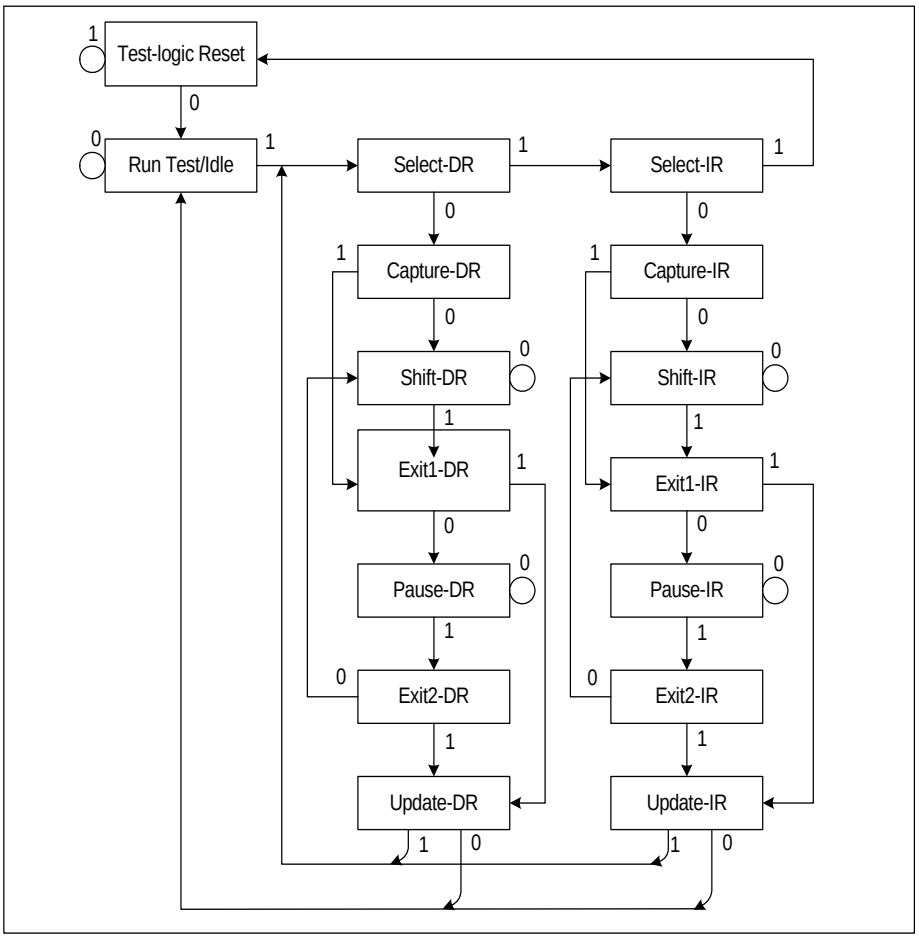


Figure-24 JTAG State Diagram

© 2019 Renesas Electronics Corporation

6 TEST SPECIFICATIONS

6.1 Absolute maximum Ratings

	Min	Max	
Storage Temperature	-65 °C	+150 °C	
Voltage on VDDAR/VDDAT/VDDAX/VDDAB/VDDAP w.r.t. GND	-0.5 V	4.6 V	
Voltage on VDDDIO w.r.t. GND	-0.5 V	4.6 V	
Voltage on VDDDC w.r.t. GND	-0.5 V	2.2 V	
Voltage on Any Input Digital Pin	-0.5 V	6 V	
Voltage on Any Input Analog Pin	-0.5 V	VDDAR/VDDAT/VDDAX/ VDDAB/VDDAP + 0.5	
ESD Performance (HBM)	2000 V		
Latch-up Current on Any Pin	1.5 x Inormal *		
Maximum Junction Temperature	150		
Maximum Allowed Power Dissipation (Package)		2.57W	
Note: * Inormal is the total current in normal operation mode.			

Caution: Long-term exposure to absolute maximum ratings may affect the device's reliability, and permanent damage may occur if the rating is exceeded during operation. Functional operation under these conditions is not implied. The device should be operated under recommended operating conditions.

6.2 Recommended Operating Conditions

Parameter	Description	Min.	Typ.	Max	Unit
Top	Operating Temperature Range	-40	25	85	°C
VDDDIO	Digital IO Power Supply	3.0	3.3	3.6	V
VDDAR/VDDAT/VDDAX/VDDAB/VDDAP	Analog IO Power Supply	3.13	3.3	3.47	V
VDDDC	Digital Core Power	1.68	1.8	1.98	V
VIL	Input Low Voltage	0		0.8	V
VIH	Input High Voltage	2.0		3.3	V

© 2019 Renesas Electronics Corporation

6.3 D.C. Characteristics

@ TA = -40 to +85 °C, VDDDIO = 3.3 V ± 0.3 V, VDDDC = 1.8 ± 10%

Parameter	Description	Min.	Typ.	Max	Unit	Test Conditions
VOL	Output Low Voltage			0.40	V	VDDDIO = min, IOL = 4 mA, 8 mA
VOH	Output High Voltage	2.4			V	VDDDIO = min, IOH = 4 mA, 8 mA
VT+	Schmitt Trigger Input Low to High Threshold Point for IOs with Schmitt Trigger	1.35			V	
VT-	Schmitt Trigger Input High to Low Threshold Point for IOs with Schmitt Trigger			1.02	V	
R_{PU}	Pullup Resistor in Pull-up IOs	50	70	115	KΩ	
IIL	Input Low Current	-1	0	+1	μA	VIL = GNDD
IIH	Input High Current	-1	0	+1	μA	VIH = VDDDIO
IOL_D	Output Low Current	8			mA	VO = VOL, D7 - D0
IOH_D	Output High Current	8			mA	VO = VOH, D7 - D0
IOL	Output Low Current	4			mA	VO = VOL, except D7 - D0
IOH	Output High Current	4			mA	VO = VOH, except D7 - D0
C_{IN}	Input Digital Pin Capacitance			10	pF	
I_{ZL}	Leakage Current of Digital Output in High-Impedance Mode	-10		10	μA	GND < VO < VDDDIO
P	Power Dissipation		800		mW	with the PRBS pattern, excluding Loading Dissipation
P33	Power Dissipation in 3.3 V Domain		650		mW	
P18	Power Dissipation in 1.8 V Domain		150		mW	

© 2019 Renesas Electronics Corporation

6.4 T1/J1 Line Receiver Electrical Characteristics

Parameter	Min.	Typ.	Max	Unit	Test Conditions
Receiver Sensitivity Short haul with cable loss @ 772 kHz: Long haul with cable loss @ 772 kHz:			 10 36	 dB	 with nominal pulse amplitude of 3.0 V for 100 Ω termination
Analog LOS level Short haul: Long haul:	 4	 800 	 48	 mVp-p dB	 A LOS level is programmable for long haul.
Allowable consecutive zeros before LOS T1.231 - 1993: I.431:		 175 1544			
LOS reset	12.5			% 'One's	G.775, ETSI 300233
Receive Intrinsic Jitter 10 Hz - 8 KHz 10 Hz - 40 KHz 8 KHz - 40 KHz Wide Band			 0.02 0.025 0.025 0.05	 U.I. U.I. U.I. U.I.	JA is enabled
Input Jitter Tolerance 0.1 Hz - 1 Hz: 4.9 Hz - 300 Hz: 10 KHz - 100 KHz:	 138.0 28.0 0.4			 U.I. U.I. U.I.	AT&T62411
Receiver Differential Input Impedance	20			KΩ	
Input Termination Resistor Tolerance			±1%		
Receive Return Loss 39 KHz - 77 KHz: 77 KHz - 1.544 MHz: 1.544 MHz - 2.316 MHz	 20 20 20			 dB dB dB	 G.703 Internal Termination

© 2019 Renesas Electronics Corporation

6.5 E1 Line Receiver Electrical Characteristics

Parameter	Min.	Typ.	Max	Unit	Test Conditions
Receiver Sensitivity Short haul with cable loss @ 1024 kHz: Long haul with cable loss @ 1024 kHz:			 10 43	 dB	with nominal pulse amplitude of 3.0 V for 120 Ω and 2.37 V for 75 Ω termination
Analog LOS level Short haul: Long haul:	 4	 800	 48	 mVp-p dB	A LOS level is programmable for long haul.
Allowable consecutive zeros before LOS G.775: I.431 / ETSI300233:		 32 2048			
LOS reset	12.5			% 'One's	G.775, ETSI 300233
Receive Intrinsic Jitter			0.05	U.I.	JA is enabled; wide band
Input Jitter Tolerance 1 Hz - 20 Hz: 20 Hz - 2.4 KHz: 18 KHz - 100 KHz:	 37 5 2			 U.I. U.I. U.I.	G.823, with 6 dB cable attenuation
Receiver Differential Input Impedance	20			KΩ	
Input Termination Resistor Tolerance			±1%		
Receive Return Loss 51 KHz - 102 KHz: 102 KHz - 2.048 MHz: 2.048 MHz - 3.072 MHz	 20 20 20			 dB dB dB	 G.703 Internal Termination

6.6 T1/J1 Line Transmitter Electrical Characteristics

Parameter	Min.	Typ.	Max	Unit
Output pulse amplitudes	2.4	3.0	3.6	V
Zero (space) level	-0.15		0.15	V
Transmit amplitude variation with supply	-1		+1	%
Difference between pulse sequences for 17 consecutive pulses (T1.102)			200	mV
Output pulse width at 50% of nominal amplitude	338	350	362	ns
Pulse width variation at the half amplitude (T1.102)			20	ns
Imbalance between Positive and Negative Pulses amplitude (T1.102)	0.95		1.05	

© 2019 Renesas Electronics Corporation

Parameter	Min.	Typ.	Max	Unit
Transmit Return Loss 39 KHz - 77 KHz: 77 KHz - 1.544 MHz: 1.544 MHz - 2.316 MHz:		 20 15 12		 dB dB dB
Intrinsic Transmit Jitter (TSCK is jitter free) 10 Hz - 8 KHz: 8 KHz - 40 KHz: 10 Hz - 40 KHz: wide band:			 0.020 0.025 0.025 0.050	 U.I.p-p U.I.p-p U.I.p-p U.I.p-p
Line short circuit current		110		mA Ip-p

6.7 E1 Line Transmitter Electrical Characteristics

Parameter	Min.	Typ.	Max	Unit
Output pulse amplitudes E1, 75Ω load: E1, 120Ω load:	 2.14 2.7	 2.37 3.0	 2.60 3.3	 V V
Zero (space) level E1, 75Ω load: E1, 120Ω load:	 -0.237 -0.3		 0.237 0.3	 V V
Transmit amplitude variation with supply	-1		+1	%
Difference between pulse sequences for 17 consecutive pulses (T1.102)			200	mV
Output pulse width at 50% of nominal amplitude	232	244	256	ns
Ratio of the amplitudes of Positive and Negative pulses at the center of the pulse interval (G.703)	0.95		1.05	
Ratio of the width of Positive and Negative pulses at the center of the pulse interval (G.703)	0.95		1.05	
Transmit Return Loss (G.703) E1, 75 Ω / 120 Ω 51 KHz - 102 KHz: 102 KHz - 2.048 MHz: 2.048 MHz - 3.072 MHz:		 20 15 12		 dB dB dB
Intrinsic Transmit Jitter (TSCK is jitter free) 20 Hz - 100 KHz			 0.050	 U.I.
Line short circuit current		110		mA Ip-p

© 2019 Renesas Electronics Corporation

6.8 Transmitter and Receiver Timing Characteristics

Symbol	Parameter		Min	Typ	Max	Unit
	OSCI frequency					
	E1: T1/J1:			2.048 x N (N = 1, 2, 3, 4) 1.544 x N (N = 1, 2, 3, 4)		MHz
	MCLK tolerance		-32		32	ppm
	MCLK duty cycle		30		70	%
Transmit path						
	TCLK frequency					
	E1: T1/J1:			2.048 1.544		MHz
	TCLK tolerance		-50		+50	ppm
	TCLK Duty Cycle		10		90	%
t1	Transmit Data Setup Time		40			ns
t2	Transmit Data Hold Time		40			ns
	Delay time of THZ low to driver high impedance				10	us
	Delay time of TCLK low to driver high impedance			75		U.I.
Receive path						
	Clock recovery capture range [1]	E1		± 80		ppm
		T1/J1		± 180		
	RCLK duty cycle [2]		40	50	60	%
t4	RCLK pulse width [2]					
	E1: T1/J1:		457 607	488 648	519 689	ns
t5	RCLK pulse width low time					
	E1: T1/J1:		203 259	244 324	285 389	ns
t6	RCLK pulse width high time					
	E1: T1/J1:		203 259	244 324	285 389	ns
	Rise/fall time [3]				20	ns
t7	Receive Data Setup Time					
	E1: T1/J1:		200 200	244 324		ns
t8	Receive Data Hold Time					
	E1: T1/J1:		200 200	244 324		ns

1.Relative to nominal frequency, MCLK= ± 32 ppm

2.RCLK duty cycle widths will vary depending on extent of received pulse jitter displacement. Maximum and minimum RCLK duty cycles are for worst case jitter conditions (0.2UI displacement for E1 per ITU G.823).

3.For all digital outputs. C load = 15pF

© 2019 Renesas Electronics Corporation

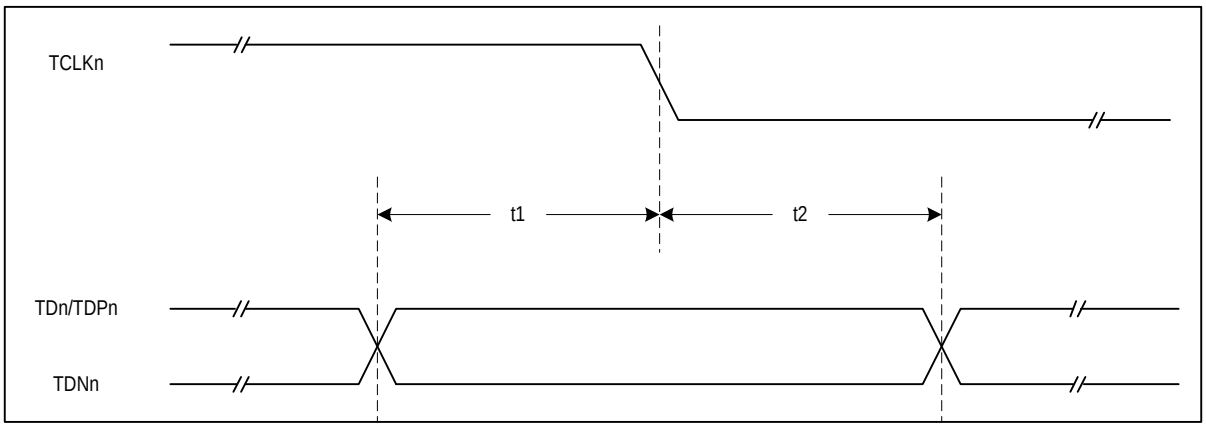


Figure-25 Transmit System Interface Timing

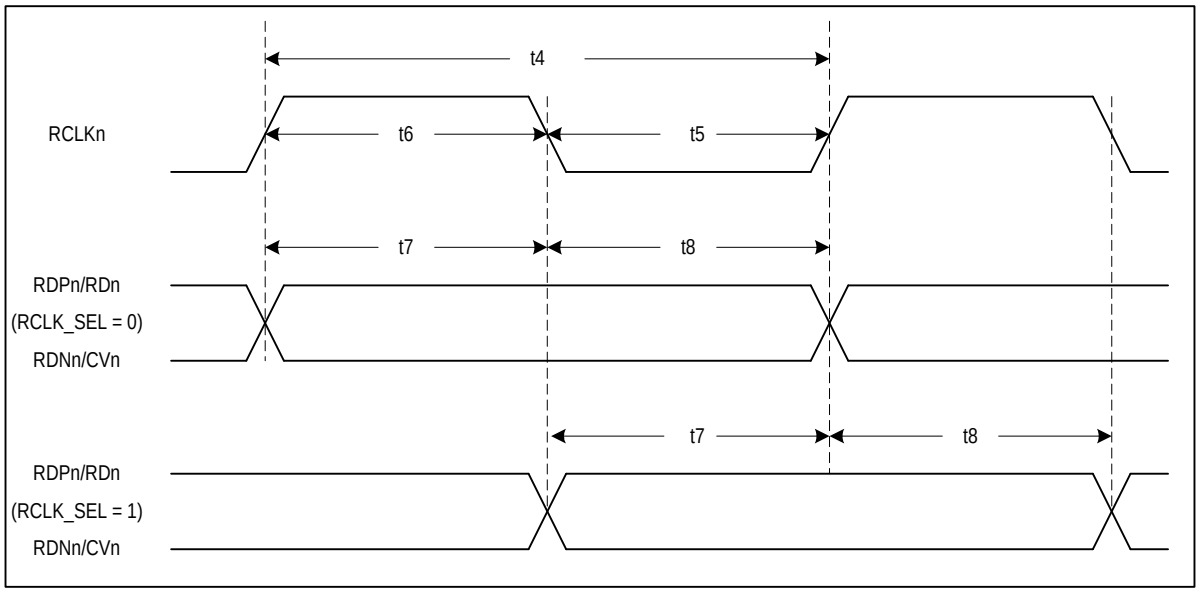


Figure-26 Receive System Interface Timing

6.9 Jitter Tolerance

6.9.1 T1/J1 Mode

Jitter Tolerance	Min.	Typ.	Max	Unit	Standard
1 Hz	138.0			U.I.	AT&T 62411
4.9 Hz - 300 Hz	28.0			U.I.	
10 KHz - 100 KHz	0.4			U.I.	

© 2019 Renesas Electronics Corporation

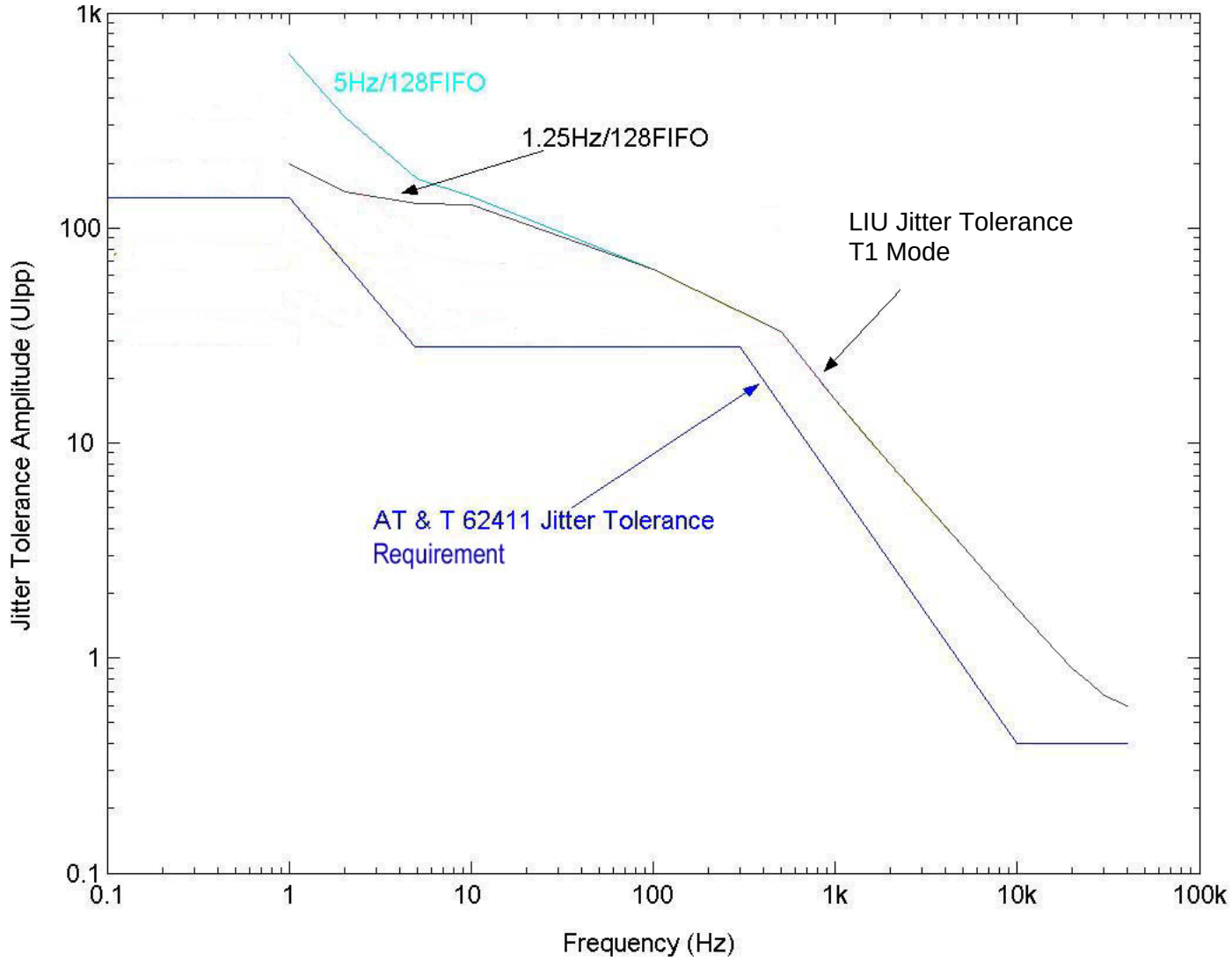


Figure-27 T1/J1 Jitter Tolerance Performance Requirement

6.9.2 E1 Mode

Jitter Tolerance	Min.	Typ.	Max	Unit	Standard
1 Hz	37			U.I.	G.823 Cable attenuation is 6 dB
20 Hz - 2.4 KHz	1.5			U.I.	
18 KHz - 100 KHz	0.2			U.I.	

© 2019 Renesas Electronics Corporation

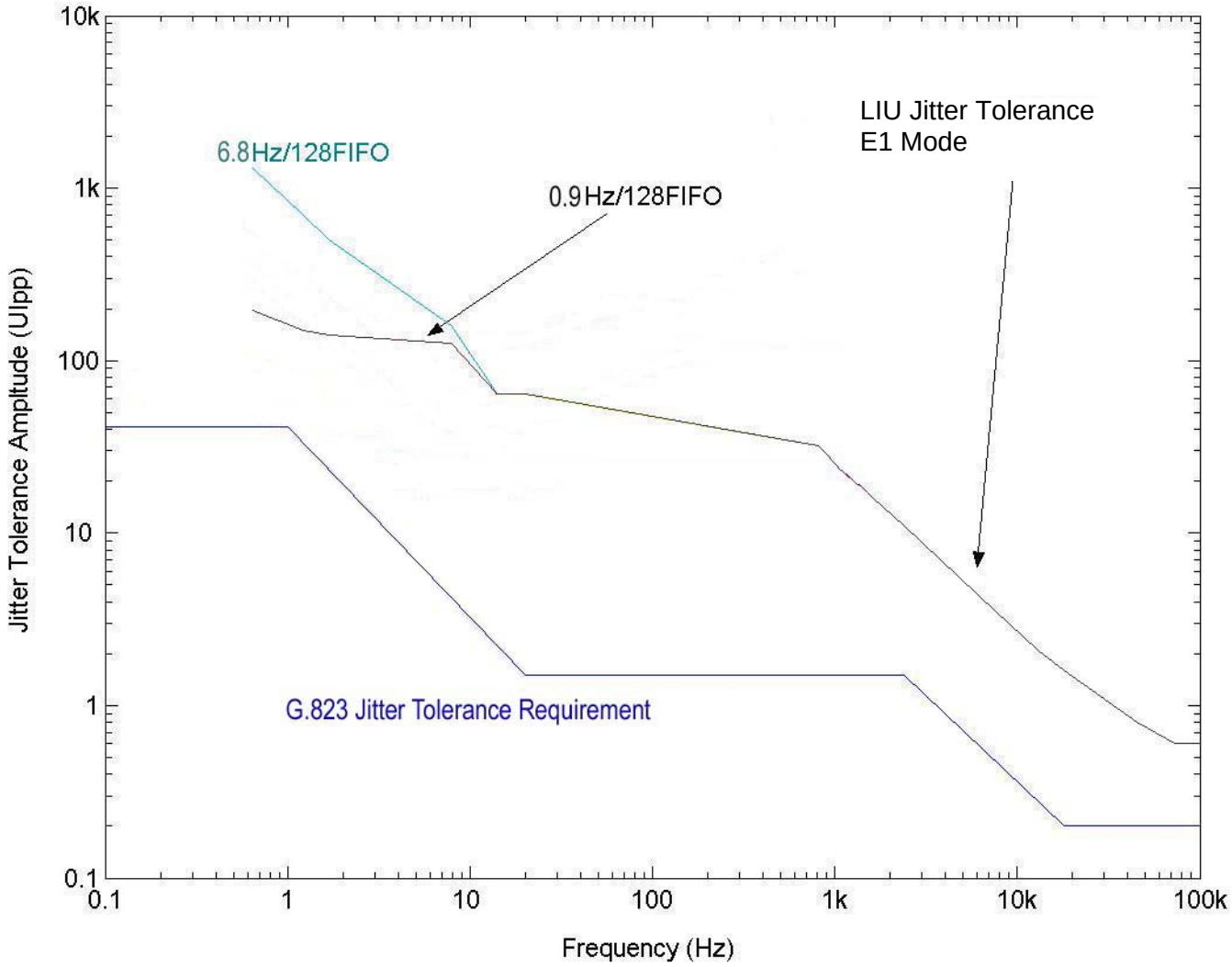


Figure-28 E1 Jitter Tolerance Performance Requirement

© 2019 Renesas Electronics Corporation

6.10 Jitter Transfer

Parameter	Min.	Typ.	Max	Unit
Jitter Attenuator Latency Delay 32-bit FIFO: 64-bit FIFO: 128-bit FIFO:		 16 32 64		 U.I. U.I. U.I.
Input jitter tolerance before FIFO overflow or underflow 32-bit FIFO: 64-bit FIFO: 128-bit FIFO:		 28 58 120		 U.I. U.I. U.I.

6.10.1 T1/J1 Mode

T1/J1 Jitter Transfer performance is required by AT&T pub.62411.

Parameter	Min.	Typ.	Max	Unit
@ 1 Hz	0			dB
@ 20 Hz	0			
@ 1 kHz	+33.3			
@ 1.4 kHz	40			
@ 70 kHz	40			

© 2019 Renesas Electronics Corporation

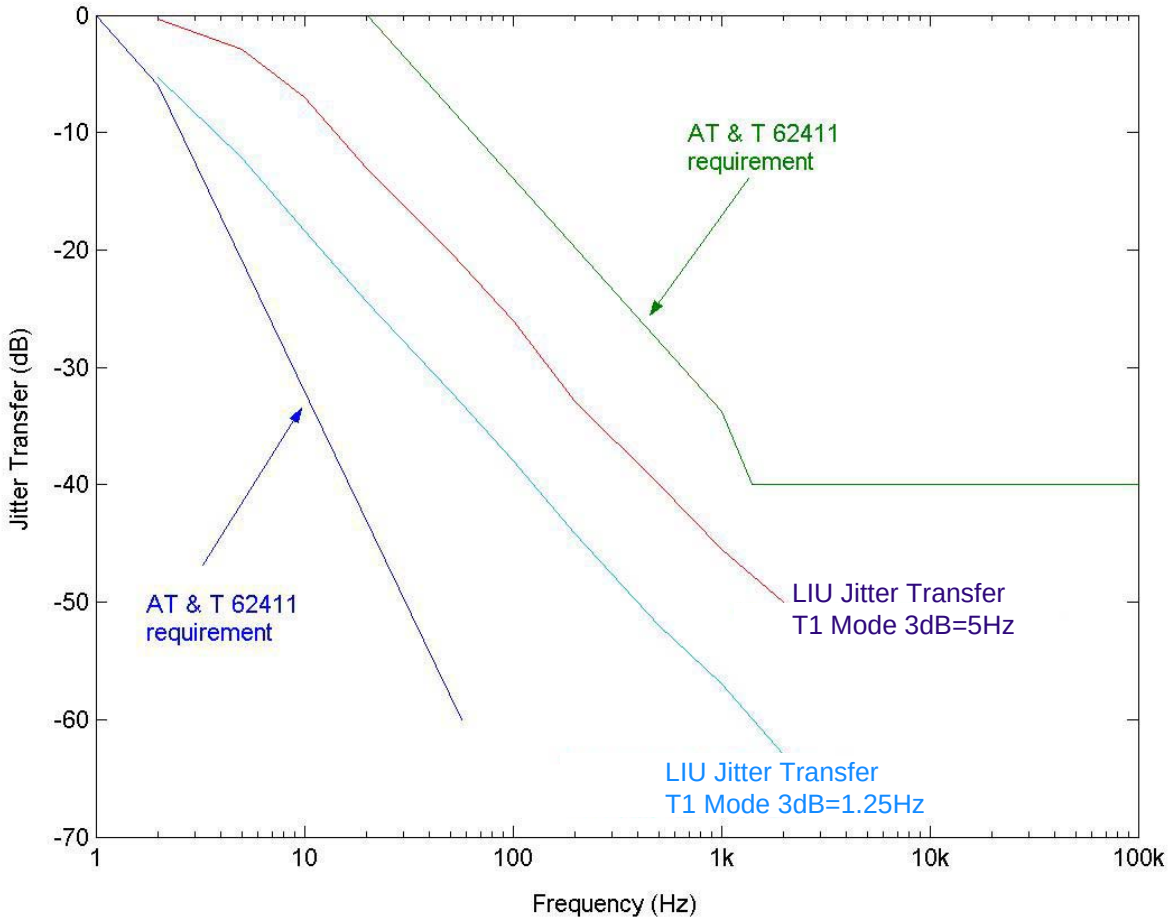


Figure-29 T1/J1 Jitter Transfer Performance Requirement (AT&T62411 / GR-253-CORE / TR-TSY-000009)

6.10.2 E1 Mode

E1 Jitter Transfer performance is required by G.736.

Parameter	Min.	Typ.	Max	Unit
@ 3 Hz	-0.5			dB
@ 40 Hz	-0.5			
@ 400 Hz	+19.5			
@ 100 kHz	+19.5			

© 2019 Renesas Electronics Corporation

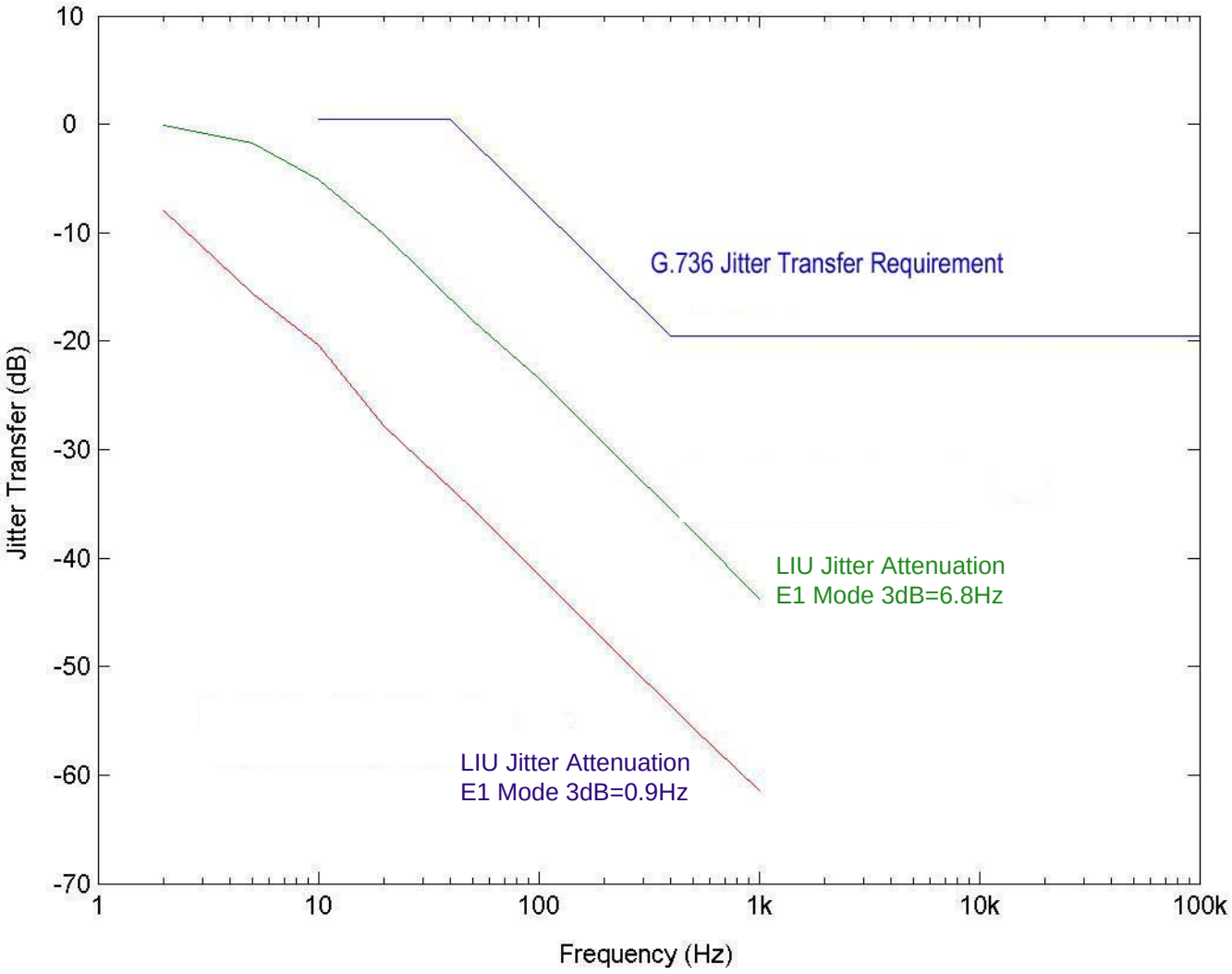


Figure-30 E1 Jitter Transfer Performance Requirement (G.736)

Table-71 JTAG Timing Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
t1	TCK Period	100			ns
t2	TMS to TCK Setup Time TDI to TCK Setup Time	25			ns
t3	TCK to TMS Hold Time TCK to TDI Hold Time	25			ns
t4	TCK to TDO Delay Time			50	ns

© 2019 Renesas Electronics Corporation

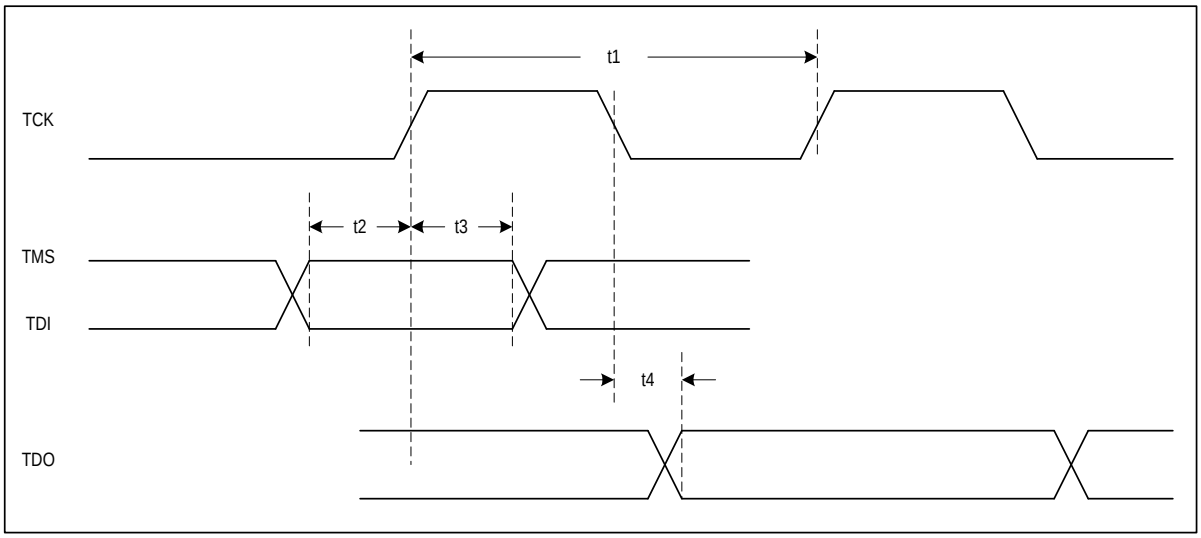


Figure-31 JTAG Interface Timing

© 2019 Renesas Electronics Corporation

7 MICROCONTROLLER INTERFACE TIMING

7.1 Motorola Non-Multiplexed Mode

7.1.1 Read Cycle Specification

Symbol	Parameter	Min	Max	Units
tRC	Read Cycle Time	237		ns
tDW	Valid $\overline{DS}$ Width	232		ns
tRWV	Delay from $\overline{DS}$ to Valid Read Signal		21	ns
tRWH	R$\overline{W}$ to $\overline{DS}$ Hold Time	134		ns
tAV	Delay from $\overline{DS}$ to Valid Address		21	ns
tADH	Address to $\overline{DS}$ Hold Time	134		ns
tPRD	$\overline{DS}$ to Valid Read Data Propagation Delay		206	ns
tDAZ	Delay from Read Data Active to High Z	5	20	ns
tRecovery	Recovery Time from Read Cycle	5		ns

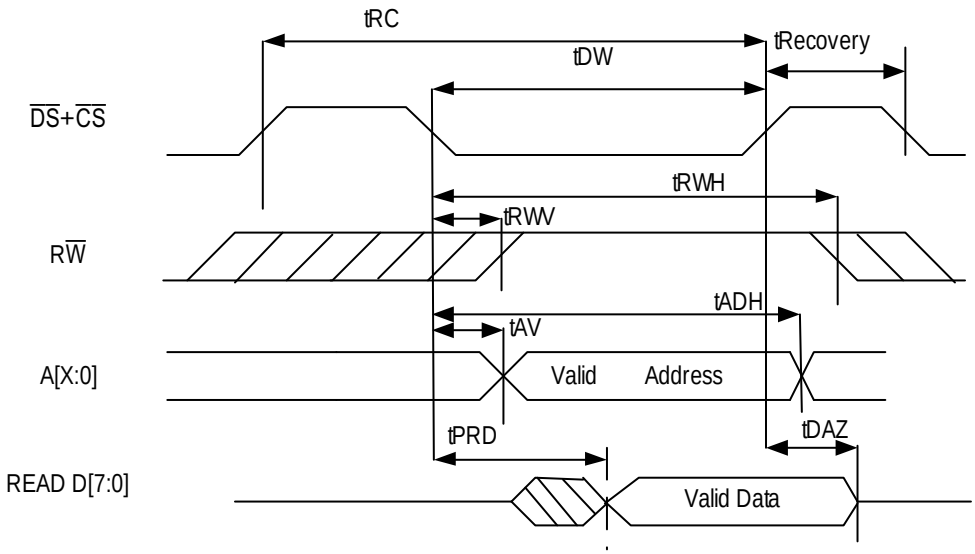


Figure-32 Motorola Non-Multiplexed Mode Read Cycle

7.1.2 Write Cycle Specification

Symbol	Parameter	Min	Max	Units
tWC	Write Cycle Time	237		ns
tDW	Valid $\overline{DS}$ width	232		ns
tRWV	Delay from $\overline{DS}$ to valid write signal		21	ns
tRWH	R$\overline{W}$ to $\overline{DS}$ Hold Time	165		ns
tAV	Delay from $\overline{DS}$ to Valid Address		21	ns

© 2019 Renesas Electronics Corporation

Symbol	Parameter	Min	Max	Units
tAH	Address to $\overline{DS}$ Hold Time	165		ns
tDV	Delay from $\overline{DS}$ to valid write data		83	ns
tDHW	Write Data to $\overline{DS}$ Hold Time	165		ns
tRecovery	Recovery Time from Write Cycle	5		ns

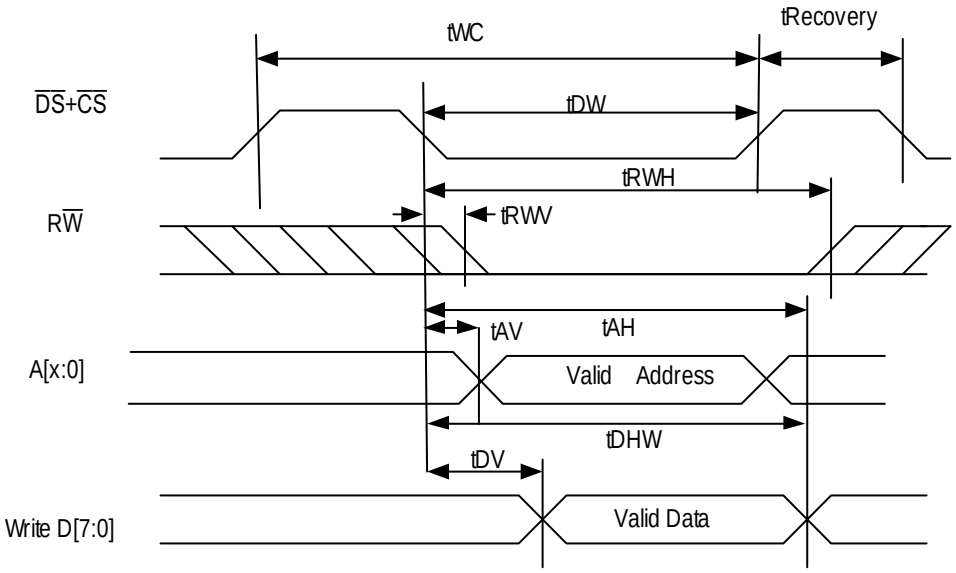


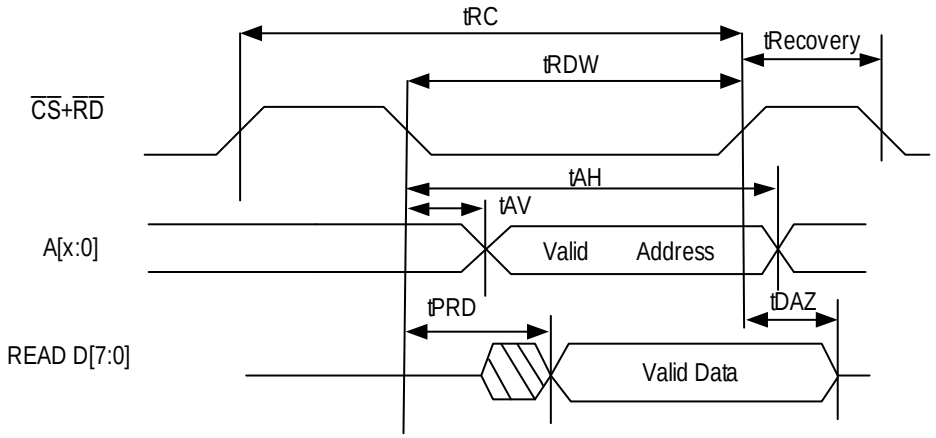
Figure-33 Motorola Non-Multiplexed Mode Write Cycle

7.2 Intel Non-Multiplexed Mode

7.2.1 Read Cycle Specification

Symbol	Parameter	Min	Max	Units
tRC	Read Cycle Time	237		ns
tRDW	Valid $\overline{RD}$ Width	232		ns
tAV	Delay from $\overline{RD}$ to Valid Address		21	ns
tAH	Address to $\overline{RD}$ Hold Time	134		ns
tPRD	$\overline{RD}$ to Valid Read Data Propagation Delay		206	ns
tDAZ	Delay from Read Data Active to High Z	5	20	ns
tRecovery	Recovery Time from Read Cycle	5		ns

© 2019 Renesas Electronics Corporation

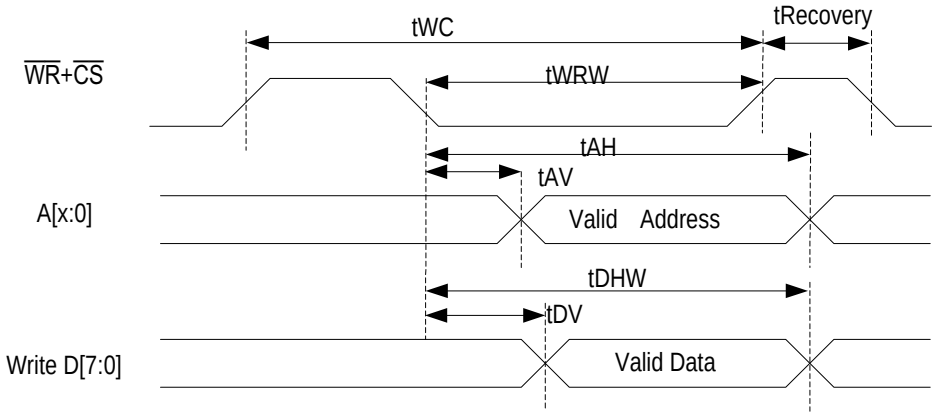


Note: The $\overline{WR}$ pin should be tied to high.

Figure-34 Intel Non-Multiplexed Mode Read Cycle

7.2.2 Write Cycle Specification

Symbol	Parameter	Min	Max	Units
tWC	Write Cycle Time	237		ns
tWRW	Valid $\overline{WR}$ width	232		ns
tAV	Delay from $\overline{WR}$ to Valid Address		21	ns
tAH	Address to $\overline{WR}$ Hold Time	165		ns
tDV	Delay from $\overline{WR}$ to valid write data		83	ns
tDHW	Write Data to $\overline{WR}$ Hold Time	165		ns
tRecovery	Recovery Time from Write Cycle	5		ns



Note: The $\overline{RD}$ pin should be tied to high.

Figure-35 Intel Non-Multiplexed Mode Write Cycle

© 2019 Renesas Electronics Corporation

7.3 SPI Mode

The maximum SPI data transfer clock is 2 MHz.

Symbol	Description	Min.	Max	Units
f_{OP}	SCLK Frequency		2.0	MHz
t_{CSH}	Min. $\overline{CS}$ High Time	100		ns
t_{CSS}	$\overline{CS}$ Setup Time	50		ns
t_{CSD}	$\overline{CS}$ Hold Time	100		ns
t_{CLD}	Clock Disable Time	50		ns
t_{CLH}	Clock High Time	205		ns
t_{CLL}	Clock Low Time	205		ns
t_{DIS}	Data Setup Time	50		ns
t_{DIH}	Data Hold Time	150		ns
t_{PD}	Output Delay		150	ns
t_{DF}	Output Disable Time		50	ns

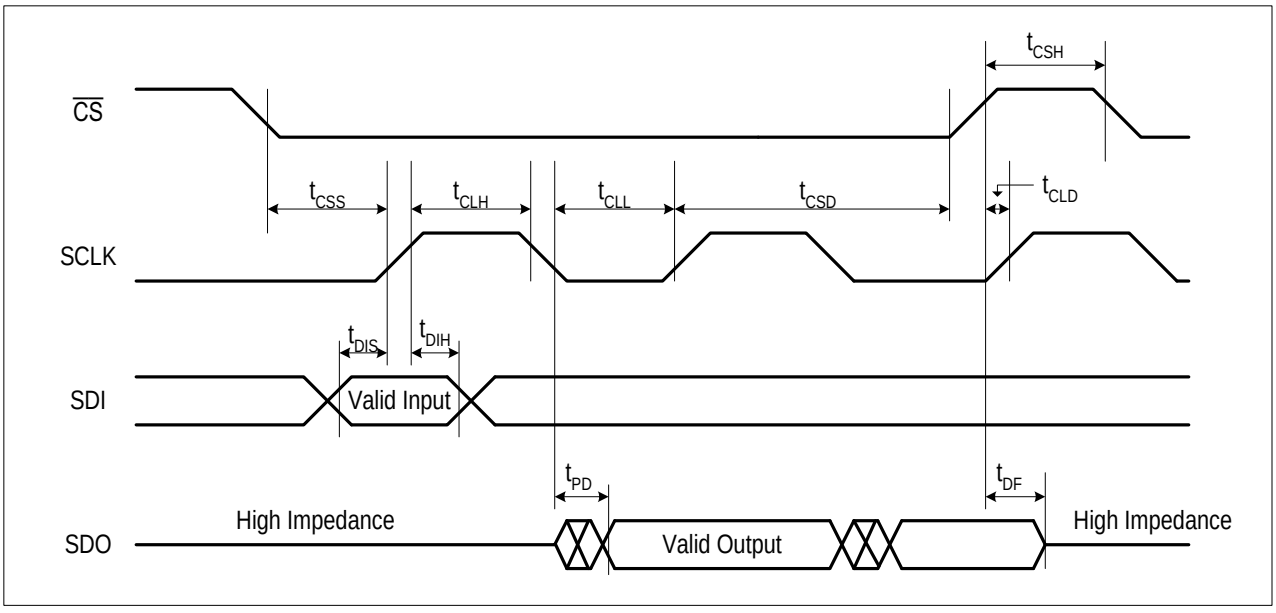


Figure-36 SPI Timing Diagram

© 2019 Renesas Electronics Corporation

8 THERMAL CHARACTERISTICS

Conditions: 4 layer, 0.56mm substrate, Flotherm model

		Thermal Resistance, Junction to Case (θjc)	Thermal Resistance, Junction to Board (θjb)	Thermal Resistance, Junction to Ambient (θja)					
	Airflow	0m/s	0m/s	0m/s	1m/s	2m/s	3m/s	4m/s	5m/s
256 PBGA Package (BBG256)	Thermal Resistance, °C/W	12.31	10.65	21.4	16.9	15.1	14.1	13.5	13.1
256 CABGA Package (BCG256)	Thermal Resistance, °C/W	4.85	11.72	21.8	17.76	15.92	14.48	14.3	13.86

ORDERING INFORMATION

Order Number	Marking	Package	Shipping Package	Temperature
82P5088BBG	IDT82P5088BBG	“Lead-Free” 256 Ball Grid Array	Tray	Industrial (-40°C to 85°C)

NOTE: IDT parts that are ordered with a "G" suffix to the part number are the Pb-free configuration and are RoHS compliant.

DATASHEET DOCUMENT HISTORY

Version 1, 2/5/2009 Initial release.
Version 2, 10/15/2012: Added CABGA package and thermal information. Pg 43, T33: RO2 replaced REFA with REFB, RO1 replaced REFB with REFA
Version 2, 7/29/2014; Ordering information; Removed BCG and leaded BB packages, PDN CQ-13-01.
Version 2, 7/30/2014; Product Discontinuation Notice for BCG package PDN CQ-13-03

© 2019 Renesas Electronics Corporation

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers skilled in the art designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only for development of an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising out of your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Rev.1.0 Mar 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
www.renesas.com/contact/

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

© 2020 Renesas Electronics Corporation. All rights reserved.