QUAD CHANNEL T1/E1/J1 SHORT HAUL LINE INTERFACE UNIT

IDT82V2044E

FEATURES:

- **Four channel T1/E1/J1 short haul line interfaces**
- **Supports HPS (Hitless Protection Switching) for 1+1 protection without external relays**
- **Programmable T1/E1/J1 switchability allowing one bill of material for any line condition**
- **Single 3.3 V power supply with 5 V tolerance on digital interfaces**
- **Meets or exceeds specifications in**
  - ANSI T1.102, T1.403 and T1.408
  - ITU I.431, G.703,G.736, G.775 and G.823
  - ETSI 300-166, 300-233 and TBR 12/13
  - AT&T Pub 62411
- **Per channel software selectable on:**
  - Wave-shaping templates
  - Line terminating impedance (T1:100 Ω, J1:110 Ω, E1:75 Ω/120 Ω)
  - Adjustment of arbitrary pulse shape
  - JA (Jitter Attenuator) position (receive path or transmit path)
  - Single rail/dual rail system interfaces
  - B8ZS/HDB3/AMI line encoding/decoding
  - Active edge of transmit clock (TCLK) and receive clock (RCLK)
  - Active level of transmit data (TDATA) and receive data (RDATA)
  - Receiver or transmitter power down
  - High impedance setting for line drivers
  - PRBS (Pseudo Random Bit Sequence) generation and detection with 2^{15}-1 PRBS polynomials for E1
  - QRSS (Quasi Random Sequence Signals) generation and detection with 2^{20}-1 QRSS polynomials for T1/J1
  - 16-bit BPV (Bipolar Pulse Violation)/Excess Zero/PRBS or QRSS error counter
  - Analog loopback, Digital loopback, Remote loopback and Inband loopback
- **Adaptive receive sensitivity up to -20 dB**
- **Non-intrusive monitoring per ITU G.772 specification**
- **Short circuit protection for line drivers**
- **LOS (Loss Of Signal) detection with programmable LOS levels**
- **AIS (Alarm Indication Signal) detection**
- **JTAG interface**
- **Supports serial control interface, Motorola and Intel Non-Multiplexed interfaces**
- **Package:**
  IDT82V2044E: 128-pin TQFP

DESCRIPTION:

The IDT82V2044E can be configured as a quad T1, quad E1 or quad J1 Line Interface Unit. The IDT82V2044E performs clock/data recovery, AMI/B8ZS/HDB3 line decoding and detects and reports the LOS conditions. An integrated Adaptive Equalizer is available to increase the receive sensitivity and enable programming of LOS levels. In transmit path, there is an AMI/B8ZS/HDB3 encoder and Waveform Shaper. There is one Jitter Attenuator for each channel, which can be placed in either the receive path or the transmit path. The Jitter Attenuator can also be disabled. The IDT82V2044E supports both Single Rail and Dual Rail system interfaces and both serial and parallel control interfaces. To facilitate the network maintenance, a PRBS/QRSS generation/detection circuit is integrated in each channel, and different types of loopbacks can be set on a per channel basis. Four different kinds of line terminating impedance, 75Ω, 100 Ω, 110 Ω and 120 Ω are selectable on a per channel basis. The chip also provides driver short-circuit protection and supports JTAG boundary scanning.

The IDT82V2044E can be used in SDH/SONET, LAN, WAN, Routers, Wireless Base Stations, IADs, IMAs, IMAPs, Gateways, Frame Relay Access Devices, CSU/DSU equipment, etc.

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FUNCTIONAL BLOCK DIAGRAM

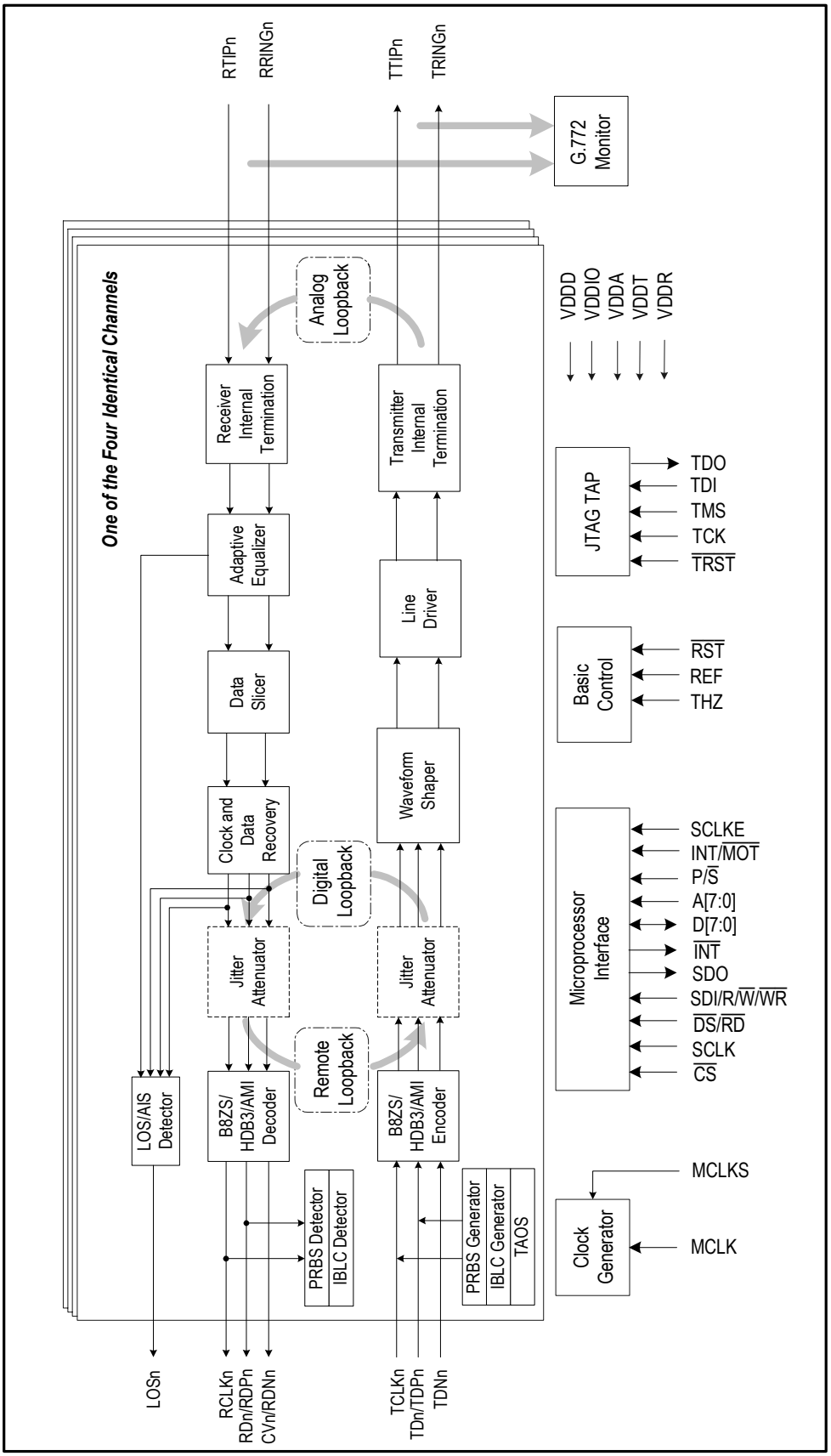


Figure-1 Block Diagram

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1 IDT82V2044E PIN CONFIGURATIONS

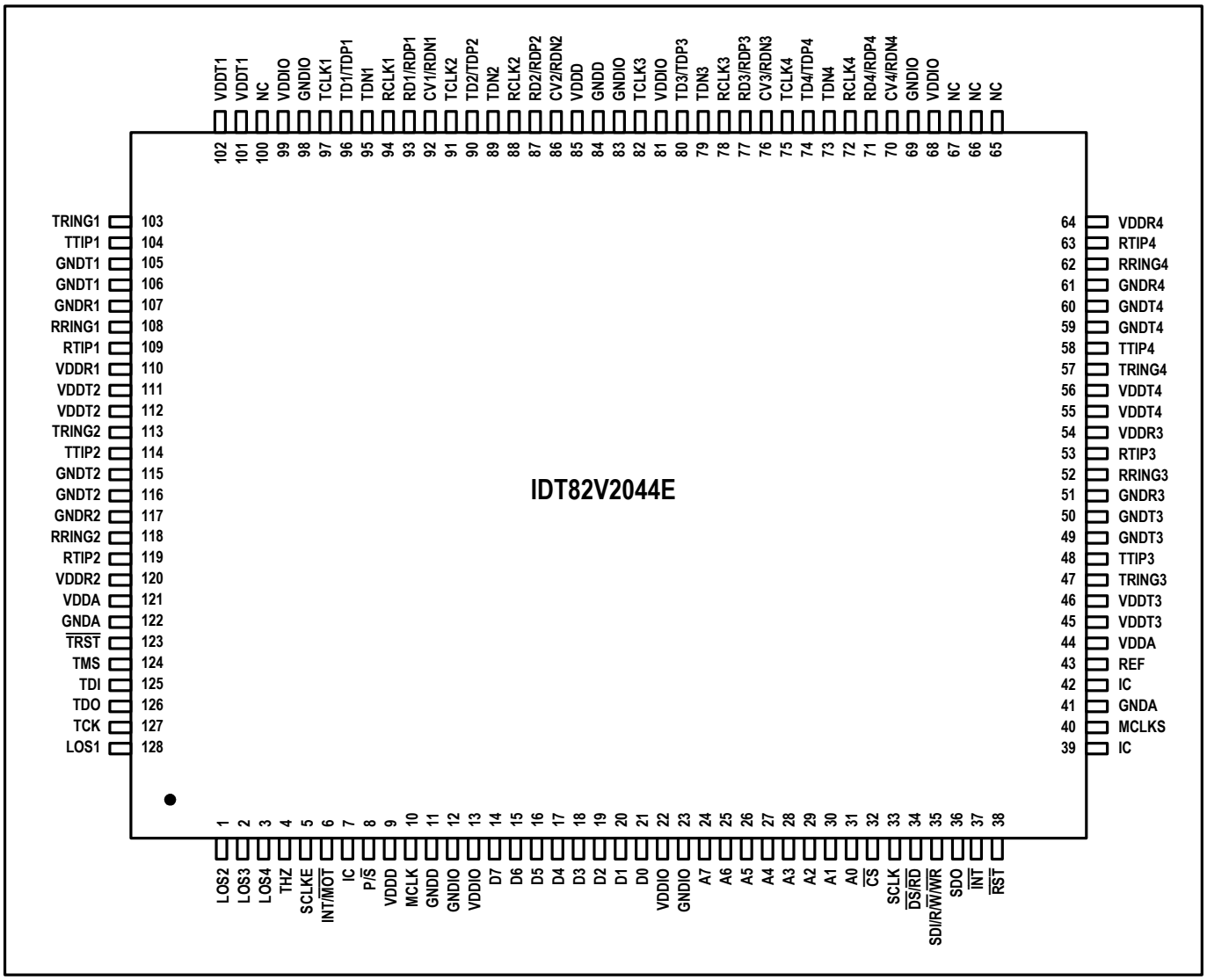


Figure-2 IDT82V2044E TQFP128 Package Pin Assignment

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2 PIN DESCRIPTION

Table-1 Pin Description

<table>
<tr><th>Name</th><th>Type</th><th>TQFP128</th><th>Description</th></tr>
<tr><td colspan="4">Transmit and Receive Line Interface</td></tr>
<tr><td>TTIP1
TTIP2
TTIP3
TTIP4

TRING1
TRING2
TRING3
TRING4</td><td>Output Analog</td><td>104
114
48
58

103
113
47
57</td><td>TTIPn[1]/TRINGn: Transmit Bipolar Tip/Ring for Channel 1~4
These pins are the differential line driver outputs and can be set to high impedance state globally or individually. A logic high on THZ pin turns all these pins into high impedance state. When THZ bit (TCF1, 03H...)[2] is set to ‘1’, the TTIPn/TRINGn in the corresponding channel is set to high impedance state.

In summary, these pins will become high impedance in the following conditions:
• THZ pin is high: all TTIPn/TRINGn enter high impedance.
• THZn bit is set to 1: the corresponding TTIPn/TRINGn become high impedance;
• Loss of MCLK: all TTIPn/TRINGn pins become high impedance;
• Loss of TCLKn: the corresponding TTIPn/TRINGn become high impedance (exceptions: Remote Loopback; Transmit internal pattern by MCLK);
• Transmitter path power down: the corresponding TTIPn/TRINGn become high impedance;
• After software reset; pin reset and power on: all TTIPn/TRINGn enter high impedance.</td></tr>
<tr><td>RTIP1
RTIP2
RTIP3
RTIP4

RRING1
RRING2
RRING3
RRING4</td><td>Input Analog</td><td>109
119
53
63

108
118
52
62</td><td>RTIPn/RRINGn: Receive Bipolar Tip/Ring for Channel 1~4
These pins are the differential line receiver inputs.</td></tr>
<tr><td colspan="4">Transmit and Receive Digital Data Interface</td></tr>
<tr><td>TD1/TDP1
TD2/TDP2
TD3/TDP3
TD4/TDP4

TDN1
TDN2
TDN3
TDN4</td><td>Input</td><td>96
90
80
74

95
89
79
73</td><td>TDn: Transmit Data for Channel 1~4
In Single Rail Mode, the NRZ data to be transmitted is input on these pins. Data on TDn is sampled into the device on the active edge of TCLKn. The active edge of TCLKn is selected by the TCLK_SEL bit (TCF0, 02H...). Data is encoded by AMI, HDB3 or B8ZS line code rules before being transmitted to the line. In this mode, TDNn should be connected to ground.

TDPn/TDNn: Positive/Negative Transmit Data for Channel 1~4
In Dual Rail Mode, the NRZ data to be transmitted is input on these pins. Data on TDPn/TDNn is sampled into the device on the active edge of TCLKn. The active edge of the TCLKn is selected by the TCLK_SEL bit (TCF0, 02H...) The line code in Dual Rail Mode is as follows:
<table>
<tr><th>TDPn</th><th>TDNn</th><th>Output Pulse</th></tr>
<tr><td>0</td><td>0</td><td>Space</td></tr>
<tr><td>0</td><td>1</td><td>Positive Pulse</td></tr>
<tr><td>1</td><td>0</td><td>Negative Pulse</td></tr>
<tr><td>1</td><td>1</td><td>Space</td></tr>
</table></td></tr>
<tr><td>TCLK1
TCLK2
TCLK3
TCLK4</td><td>Input</td><td>97
91
82
75</td><td>TCLKn: Transmit Clock for Channel 1~4
These pins input 1.544 MHz for T1/J1 mode or 2.048 MHz for E1 mode transmit clock. The transmit data on TDn/TDPn or TDNn is sampled into the device on the active edge of TCLKn. If TCLKn is missing[3] and the TCLKn missing interrupt is not masked, an interrupt will be generated.</td></tr>
</table>

Notes:

1. The footprint ‘n’ (n = 1~4) represents one of the four channels.
2. The name and address of the registers that contain the preceding bit. Only the address of channel 1 register is listed, the rest addresses are represented by '...'. Users can find these omitted addresses in the ***Register Description*** section.
3. TCLKn missing: the state of TCLKn continues to be high level or low level over 70 clock cycles.

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Table-1 Pin Description (Continued)

Name	Type	TQFP128	Description
RD1/RDP1 RD2/RDP2 RD3/RDP3 RD4/RDP4	Output	93 87 77 71	**RDn: Receive Data for Channel 1~4** In Single Rail Mode, the NRZ receive data is output on these pins. Data is decoded according to AMI, HDB3 or B8ZS line code rules. The active level on RDn pin is selected by the RD_INV bit (**RCF0, 07H...**). **CVn: Code Violation for Channel 1~4** In Single Rail Mode, the BPV/CV errors in received data streams will be reported by driving pin CVn to high level for a full clock cycle. The B8ZS/HDB3 line code violation can be indicated when the B8ZS/HDB3 decoder is enabled. When AMI decoder is selected, the bipolar violation can be indicated. **RDPn/RDNn: Positive/Negative Receive Data for Channel 1~4** In Dual Rail Mode with Clock & Data Recovery (CDR), these pins output the NRZ data with the recovered clock. An active level on RDPn indicates the receipt of a positive pulse on RTIPn/RRINGn while an active level on RDNn indicates the receipt of a negative pulse on RTIPn/RRINGn. The active level on RDPn/RDNn is selected by the RD_INV bit (RCF0, 07H...). When CDR is disabled, these pins directly output the raw RZ sliced data. The output data on RDn and RDPn/RDNn is updated on the active edge of RCLKn.
CV1/RDN1 CV2/RDN2 CV3/RDN3 CV4/RDN4		92 86 76 70	
RCLK1 RCLK2 RCLK3 RCLK4	Output	94 88 78 72	**RCLKn: Receive Clock for Channel 1~4** These pins output 1.544 MHz for T1/J1 mode or 2.048 MHz for E1 mode receive clock. Under LOS conditions, if AISE bit (**MAINT0, 0AH...**) is '1', RCLKn is derived from MCLK. In clock recovery mode, these pins provide the clock recovered from the signal received on RTIPn/RRINGn. The receive data (RDn in Single Rail Mode or RDPn/RDNn in Dual Rail Mode) is updated on the active edge of RCLKn. The active edge is selected by the RCLK_SEL bit (**RCF0, 07H...**). If clock recovery is bypassed, RCLKn is the exclusive OR(XOR) output of the Dual Rail sliced data RDPn and RDNn. This signal can be used in the applications with external clock recovery circuitry.
MCLK	Input	10	**MCLK: Master Clock** MCLK is an independent, free-running reference clock. It is a single reference for all operation modes and provides selectable 1.544 MHz or 37.056 MHz for T1/J1 operating mode, while 2.048 MHz or 49.152 MHz for E1 operating mode. The reference clock is used to generate several internal reference signals: • Timing reference for the integrated clock recovery unit. • Timing reference for the integrated digital jitter attenuator. • Timing reference for microcontroller interface. • Generation of RCLKn signal during a loss of signal condition. • Reference clock during Transmit All Ones (TAO) and all zeros condition. When sending PRBS/QRSS or Inband Loopback code, either MCLK or TCLKn can be selected as the reference clock. • Reference clock for ATAO and AIS. The loss of MCLK will turn all the four TTIP/TRING into high impedance status.
MCLKS	Input	40	**MCLKS: Master Clock Select** If 2.048 MHz (E1) or 1.544 MHz (T1/J1) is selected as the MCLK, this pin should be connected to ground; and if the 49.152 MHz (E1) or 37.056 MHz (T1/J1) is selected as the MCLK, this pin should be pulled high.
LOS1 LOS2 LOS3 LOS4	Output	128 1 2 3	**LOSn: Loss of Signal Output for Channel 1~4** These pins are used to indicate the loss of received signals. When LOSn pin becomes high, it indicates the loss of received signals in channel n. The LOSn pin will become low automatically when valid received signal is detected again. The criteria of loss of signal are described in 3.5 LOS AND AIS DETECTION.
Control Interface			
P/$\overline{S}$	Input	8	**P/$\overline{S}$: Parallel or Serial Control Interface Select** Level on this pin determines which control mode is selected to control the device as follows: P/$\overline{S}$ | Control Interface High | Parallel Microcontroller Interface Low | Serial Microcontroller Interface The serial microcontroller interface consists of $\overline{CS}$, SCLK, SDI, SDO and SCLKE pins. Parallel microcontroller interface consists of $\overline{CS}$, A[7:0], D[7:0], $\overline{DS}$/$\overline{RD}$ and R/$\overline{W}$/$\overline{WR}$ pins. The device supports non-multiplexed parallel interface as follows: P/$\overline{S}$, INT/$\overline{MOT}$ | Microcontroller Interface 10 | Motorola non-multiplexed 11 | Intel non-multiplexed

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Table-1 Pin Description (Continued)

Name	Type	TQFP128	Description
INT/$\overline{MOT}$	Input	6	**INT/$\overline{MOT}$: Intel or Motorola Microcontroller Interface Select** In microcontroller mode, the parallel microcontroller interface is configured for Motorola compatible microcontrollers when this pin is low, or for Intel compatible microcontrollers when this pin is high.
$\overline{CS}$	Input	32	**$\overline{CS}$: Chip Select** In microcontroller mode, this pin is asserted low by the microcontroller to enable microcontroller interface. For each read or write operation, this pin must be changed from high to low, and will remain low until the operation is over.
SCLK	Input	33	**SCLK: Shift Clock** In serial microcontroller mode, signal on this pin is the shift clock for the serial interface. Configuration data on pin SDI is sampled on the rising edges of SCLK. Configuration and status data on pin SDO is clocked out of the device on the rising edges of SCLK if pin SCLKE is low, or on the falling edges of SCLK if pin SCLKE is high.
$\overline{DS}$/$\overline{RD}$	Input	34	**$\overline{DS}$: Data Strobe** In parallel Motorola microcontroller interface mode, signal on this pin is the data strobe of the parallel interface. During a write operation (R/$\overline{W}$ =0), data on D[7:0] is sampled into the device. During a read operation (R/$\overline{W}$ =1), data is output to D[7:0] from the device. **$\overline{RD}$: Read Operation** In parallel Intel microcontroller interface mode, this pin is asserted low by the microcontroller to initiate a read cycle. Data is output to D[7:0] from the device during a read operation.
SDI/R/$\overline{W}$/$\overline{WR}$	Input	35	**SDI: Serial Data Input** In serial microcontroller mode, data is input on this pin. Input data is sampled on the rising edges of SCLK. **R/$\overline{W}$: Read/Write Select** In parallel Motorola microcontroller interface mode, this pin is low for write operation and high for read operation. **$\overline{WR}$: Write Operation** In parallel Intel microcontroller interface mode, this pin is asserted low by the microcontroller to initiate a write cycle. Data on D[7:0] is sampled into the device during a write operation.
SDO	Output	36	**SDO: Serial Data Output** In serial microcontroller mode, signal on this pin is the output data of the serial interface. Configuration and status data on pin SDO is clocked out of the device on the active edge of SCLK.
$\overline{INT}$	Output	37	**$\overline{INT}$: Interrupt Request** This pin outputs the general interrupt request for all interrupt sources. If INTM_GLB bit (**GCF0, 40H**) is set to '1' all the interrupt sources will be masked. And these interrupt sources also can be masked individually via registers (**INTM0, 11H**) and (**INTM1, 12H**). Interrupt status is reported via byte INT_CH (**INTCH, 80H**), registers (**INTS0, 16H**) and (**INTS1, 17H**). Output characteristics of this pin can be defined to be push-pull (active high or low) or be open-drain (active low) by bits INT_PIN[1:0] (**GCF0, 40H**).
D7 D6 D5 D4 D3 D2 D1 D0	I / O Tri-state	14 15 16 17 18 19 20 21	**Dn: Data Bus 7~0** These pins function as a bi-directional data bus of the microcontroller interface.
A7 A6 A5 A4 A3 A2 A1 A0	Input	24 25 26 27 28 29 30 31	**An: Address Bus 7~0** These pins function as an address bus of the microcontroller interface.
$\overline{RST}$	Input	38	**$\overline{RST}$: Hardware Reset** The chip is reset if a low signal is applied on this pin for more than 100ns. All the drivers output are in high-impedance state, all the internal flip-flops are reset and all the registers are initialized to their default values.

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Table-1 Pin Description (Continued)

<table>
<tr><th>Name</th><th>Type</th><th>TQFP128</th><th>Description</th></tr>
<tr><td>THZ</td><td>Input</td><td>4</td><td>THZ: Transmit Driver Enable
This pin enables or disables all transmitter drivers on a global basis. A low level on this pin enables the drivers while a high level turns all drivers into high impedance state. Note that functionality of internal circuits is not affected by signal on this pin.</td></tr>
<tr><td>REF</td><td>Input</td><td>43</td><td>REF: Reference Resistor
An external resistor (3 KΩ, 1%) is used to connect this pin to ground to provide a standard reference current for internal circuit.</td></tr>
<tr><td>SCLKE</td><td>Input</td><td>5</td><td>SCLKE: Serial Clock Edge Select
Signal on this pin determines the active edge of SCLK to output SDO. The active clock edge is selected as shown below:
<table><tr><th>SCLKE</th><th>SCLK</th></tr><tr><td>Low</td><td>Rising edge is active edge</td></tr><tr><td>High</td><td>Falling edge is active edge</td></tr></table></td></tr>
<tr><td colspan="4">JTAG Signals</td></tr>
<tr><td>$\overline{\text{TRST}}$</td><td>Input
Pullup</td><td>123</td><td>$\overline{\text{TRST}}$: JTAG Test Port Reset
This is the active low asynchronous reset to the JTAG Test Port. This pin has an internal pull-up resistor. To ensure deterministic operation of the test logic, TMS should be held high while the signal applied to $\overline{\text{TRST}}$ changes from low to high.
For normal signal processing, this pin should be connected to ground.</td></tr>
<tr><td>TMS</td><td>Input
Pullup</td><td>124</td><td>TMS: JTAG Test Mode Select
This pin is used to control the test logic state machine and is sampled on the rising edges of TCK. TMS has an internal pull-up resistor.</td></tr>
<tr><td>TCK</td><td>Input</td><td>127</td><td>TCK: JTAG Test Clock
This pin is the input clock for JTAG. The data on TDI and TMS is clocked into the device on the rising edges of TCK while the data on TDO is clocked out of the device on the falling edges of TCK. When TCK is idle at a low level, all stored-state devices contained in the test logic will retain their state indefinitely.</td></tr>
<tr><td>TDO</td><td>Output
Tri-state</td><td>126</td><td>TDO: JTAG Test Data Output
This is a tri-state output signal and used for reading all the serial configuration and test data from the test logic. The data on TDO is clocked out of the device on the falling edges of TCK.</td></tr>
<tr><td>TDI</td><td>Input
Pullup</td><td>125</td><td>TDI: JTAG Test Data Input
This pin is used for loading instructions and data into the test logic and has an internal pullup resistor. The data on TDI is clocked into the device on the rising edges of TCK.</td></tr>
<tr><td colspan="4">Power Supplies and Grounds</td></tr>
<tr><td>VDDIO</td><td>-</td><td>13, 22
68, 81
99</td><td>3.3V I/O Power Supply</td></tr>
<tr><td>GNDIO</td><td>-</td><td>12, 23
69, 83
98</td><td>I/O Ground</td></tr>
<tr><td>VDDT1
VDDT2
VDDT3
VDDT4</td><td>-</td><td>101, 102
111, 112
45, 46
55, 56</td><td>3.3V Power Supply for Transmitter Driver</td></tr>
<tr><td>GNDT1
GNDT2
GNDT3
GNDT4</td><td>-</td><td>105, 106
115, 116
49, 50
59, 60</td><td>Analog Ground for Transmitter Driver</td></tr>
<tr><td>VDDA</td><td>-</td><td>44, 121</td><td>3.3V Analog Core Power Supply</td></tr>
<tr><td>GNDA</td><td>-</td><td>41, 122</td><td>Core Analog Ground</td></tr>
<tr><td>VDDD</td><td>-</td><td>9, 85</td><td>3.3V Digital Core Power Supply</td></tr>
<tr><td>GNDD</td><td>-</td><td>11, 84</td><td>Core Digital Ground</td></tr>
<tr><td>VDDR1
VDDR2
VDDR3
VDDR4</td><td>-</td><td>110
120
54
64</td><td>3.3V Power Supply for Receiver</td></tr>
</table>

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Table-1 Pin Description (Continued)

Name	Type	TQFP128	Description
GNDR1 GNDR2 GNDR3 GNDR4	-	107 117 51 61	**Analog Ground for Receiver**
Others			
IC	-	39 7	**IC: Internal Connection** Internal Use. These pins should be connected to ground when in normal operation.
IC	-	42	**IC: Internal Connection** Internal Use. This pin should be left open when in normal operation.
NC	-	65, 66 67, 100	**NC: No Connection**

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3 FUNCTIONAL DESCRIPTION

3.1 T1/E1/J1 MODE SELECTION

The IDT82V2044E can be used as a four-channel E1 LIU or a four-channel T1/J1 LIU. In E1 application, the T1E1 bit (**GCF0, 40H**) should be set to '0'. In T1/J1 application, the T1E1 bit should be set to '1'.

3.2 TRANSMIT PATH

The transmit path of each channel of the IDT82V2044E consists of an Encoder, an optional Jitter Attenuator, a Waveform Shaper, a Line Driver and a Programmable Transmit Termination.

3.2.1 TRANSMIT PATH SYSTEM INTERFACE

The transmit path system interface consists of TCLKn pin, TDn/TDPn pin and TDNn pin. In E1 mode, the TCLKn is a 2.048 MHz clock. In T1/J1 mode, the TCLKn is a 1.544 MHz clock. If the TCLKn is missing for more than 70 MCLK cycles, an interrupt will be generated if it is not masked.

Transmit data is sampled on the TDn/TDPn and TDNn pins by the active edge of TCLKn. The active edge of TCLKn can be selected by the TCLK_SEL bit (**TCF0, 02H...**). And the active level of the data on TDn/TDPn and TDNn can be selected by the TD_INV bit (**TCF0, 02H...**).

The transmit data from the system side can be provided in two different ways: Single Rail and Dual Rail. In Single Rail mode, only TDn pin is used for transmitting data and the T_MD[1] bit (**TCF0, 02H...**) should be set to '0'. In Dual Rail Mode, both TDPn and TDNn pins are used for transmitting data, the T_MD[1] bit (**TCF0, 02H...**) should be set to '1'.

3.2.2 ENCODER

When T1/J1 mode is selected, in Single Rail mode, the Encoder can be selected to be a B8ZS encoder or an AMI encoder by setting T_MD[0] bit (**TCF0, 02H...**).

When E1 mode is selected, in Single Rail mode, the Encoder can be configured to be a HDB3 encoder or an AMI encoder by setting T_MD[0] bit (**TCF0, 02H...**).

In both T1/J1 mode and E1 mode, when Dual Rail mode is selected (bit T_MD[1] is '1'), the Encoder is by-passed. In the Dual Rail mode, a logic '1' on the TDPn pin and a logic '0' on the TDNn pin results in a negative pulse on the TTIPn/TRINGn; a logic '0' on TDPn pin and a logic '1' on TDNn pin results in a positive pulse on the TTIPn/TRINGn. If both TDPn and TDNn are logic '1' or logic '0', the TTIPn/TRINGn outputs a space (Refer to TDn/TDPn, TDNn Pin Description).

3.2.3 PULSE SHAPER

The IDT82V2044E provides two ways of manipulating the pulse shape before sending it. One is to use preset pulse templates; the other is to use user-programmable arbitrary waveform template.

3.2.3.1 Preset Pulse Templates

For E1 applications, the pulse shape is shown in Figure-3 according to the G.703 and the measuring diagram is shown in Figure-4. In internal impedance matching mode, if the cable impedance is 75 Ω, the PULS[3:0] bits (**TCF1, 03H...**) should be set to '0000'; if the cable impedance is 120 Ω, the PULS[3:0] bits (**TCF1, 03H...**) should be set to '0001'. In external impedance matching mode, for both E1/75 Ω and E1/120 Ω cable impedance, PULS[3:0] should be set to '0001'.

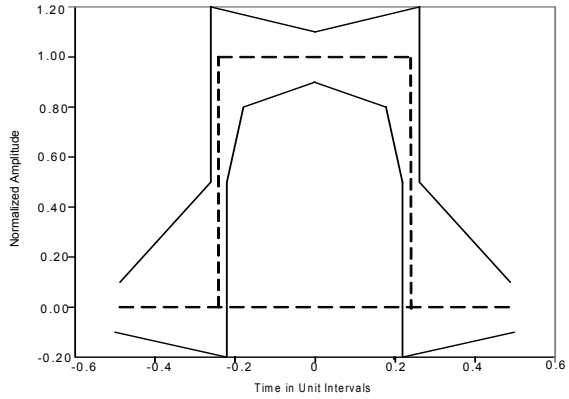


Figure-3 E1 Waveform Template Diagram

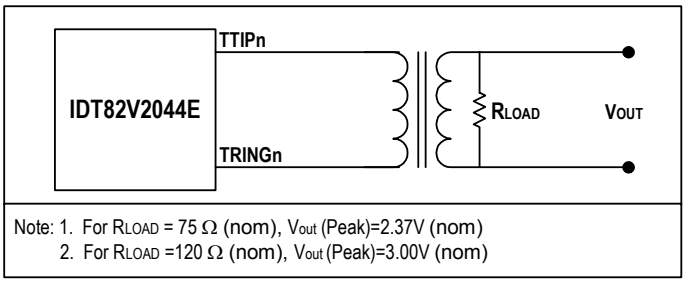


Figure-4 E1 Pulse Template Test Circuit

For T1 applications, the pulse shape is shown in Figure-5 according to the T1.102 and the measuring diagram is shown in Figure-6. This also meets the requirement of G.703, 2001. The cable length is divided into five grades, and there are five pulse templates used for each of the cable length. The pulse template is selected by PULS[3:0] bits (**TCF1, 03H...**).

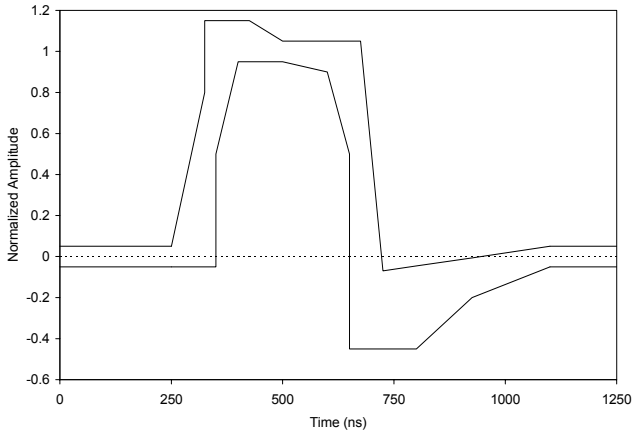


Figure-5 DSX-1 Waveform Template

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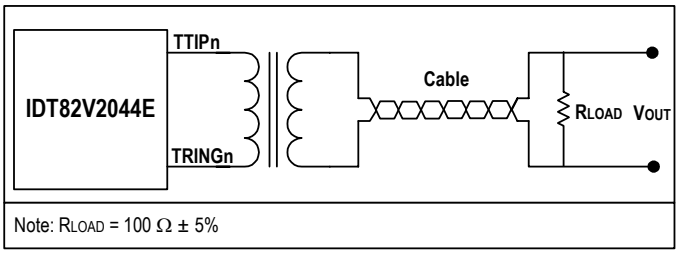


Figure-6 T1 Pulse Template Test Circuit

For J1 applications, the PULS[3:0] (**TCF1, 03H...**) should be set to '0111'. Table-10 lists these values.

3.2.3.2 User-Programmable Arbitrary Waveform

When the PULS[3:0] bits are set to '11xx', user-programmable arbitrary waveform generator mode can be used in the corresponding channel. This allows the transmitter performance to be tuned for a wide variety of line condition or special application.

Each pulse shape can extend up to 4 UIs (Unit Interval), addressed by UI[1:0] bits (**TCF3, 05H...**) and each UI is divided into 16 sub-phases, addressed by the SAMP[3:0] bits (**TCF3, 05H...**). The pulse amplitude of each phase is represented by a binary byte, within the range from +63 to -63, stored in WDAT[6:0] bits (**TCF4, 06H...**) in signed magnitude form. The most positive number +63 (D) represents the maximum positive amplitude of the transmit pulse while the most negative number -63 (D) represents the maximum negative amplitude of the transmit pulse. Therefore, up to 64 bytes are used. For each channel, a 64 bytes RAM is available.

There are eight standard templates which are stored in a local ROM. User can select one of them as reference and make some changes to get the desired waveform.

User can change the wave shape and the amplitude to get the desired pulse shape. In order to do this, firstly, users can choose a set of waveform value from the following eight tables, which is the most similar to the desired pulse shape. Table-2, Table-3, Table-4, Table-5, Table-6, Table-7, Table-8 and Table-9 list the sample data and scaling data of each of the eight templates. Then modify the corresponding sample data to get the desired transmit pulse shape.

Secondly, through the value of SCAL[5:0] bits increased or decreased by 1, the pulse amplitude can be scaled up or down at the percentage ratio against the standard pulse amplitude if needed. For different pulse shapes, the value of SCAL[5:0] bits and the scaling percentage ratio are different. The following eight tables list these values.

Do the followings step by step, the desired waveform can be programmed, based on the selected waveform template:

(1).Select the UI by UI[1:0] bits (**TCF3, 05H...**)

(2).Specify the sample address in the selected UI by SAMP [3:0] bits (**TCF3, 05H...**)

(3).Write sample data to WDAT[6:0] bits (**TCF4, 06H...**). It contains the data to be stored in the RAM, addressed by the selected UI and the corresponding sample address.

(4).Set the RW bit (**TCF3, 05H...**) to '0' to implement writing data to RAM, or to '1' to implement read data from RAM

(5).Implement the Read from RAM/Write to RAM by setting the DONE bit (**TCF3, 05H...**)

Repeat the above steps until all the sample data are written to or read from the internal RAM.

(6).Write the scaling data to SCAL[5:0] bits (**TCF2, 04H...**) to scale the amplitude of the waveform based on the selected standard pulse amplitude

When more than one UI is used to compose the pulse template, the overlap of two consecutive pulses could make the pulse amplitude overflow (exceed the maximum limitation) if the pulse amplitude is not set properly. This overflow is captured by DAC_OV_IS bit (**INTS1, 17H...**), and, if enabled by the DAC_OV_IM bit (**INTM1, 12H...**), an interrupt will be generated.

The following tables give all the sample data based on the preset pulse templates in detail for reference. For preset pulse templates, scaling up/down against the pulse amplitude is not supported.

1.Table-2 Transmit Waveform Value For E1 75 Ω
2.Table-3 Transmit Waveform Value For E1 120 Ω
3.Table-4 Transmit Waveform Value For T1 0~133 ft
4.Table-5 Transmit Waveform Value For T1 133~266 ft
5.Table-6 Transmit Waveform Value For T1 266~399 ft
6.Table-7 Transmit Waveform Value For T1 399~533 ft
7.Table-8 Transmit Waveform Value For T1 533~655 ft
8.Table-9 Transmit Waveform Value For J1 0~655 ft

Table-2 Transmit Waveform Value For E1 75 Ω

Sample	UI 1	UI 2	UI 3	UI 4
1	0000000	0000000	0000000	0000000
2	0000000	0000000	0000000	0000000
3	0000000	0000000	0000000	0000000
4	0001100	0000000	0000000	0000000
5	0110000	0000000	0000000	0000000
6	0110000	0000000	0000000	0000000
7	0110000	0000000	0000000	0000000
8	0110000	0000000	0000000	0000000
9	0110000	0000000	0000000	0000000
10	0110000	0000000	0000000	0000000
11	0110000	0000000	0000000	0000000
12	0110000	0000000	0000000	0000000
13	0000000	0000000	0000000	0000000
14	0000000	0000000	0000000	0000000
15	0000000	0000000	0000000	0000000
16	0000000	0000000	0000000	0000000
SCAL[5:0] = 100001 (default), One step change of this value of SCAL[5:0] results in 3% scaling up/down against the pulse amplitude.				

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Table-3 Transmit Waveform Value For E1 120 Ω

Sample	UI 1	UI 2	UI 3	UI 4
1	0000000	0000000	0000000	0000000
2	0000000	0000000	0000000	0000000
3	0000000	0000000	0000000	0000000
4	0001111	0000000	0000000	0000000
5	0111100	0000000	0000000	0000000
6	0111100	0000000	0000000	0000000
7	0111100	0000000	0000000	0000000
8	0111100	0000000	0000000	0000000
9	0111100	0000000	0000000	0000000
10	0111100	0000000	0000000	0000000
11	0111100	0000000	0000000	0000000
12	0111100	0000000	0000000	0000000
13	0000000	0000000	0000000	0000000
14	0000000	0000000	0000000	0000000
15	0000000	0000000	0000000	0000000
16	0000000	0000000	0000000	0000000

SCAL[5:0] = 100001 (default), One step change of this value of SCAL[5:0] results in 3% scaling up/down against the pulse amplitude.

Table-4 Transmit Waveform Value For T1 0~133 ft

Sample	UI 1	UI 2	UI 3	UI 4
1	0010111	1000010	0000000	0000000
2	0100111	1000001	0000000	0000000
3	0100111	0000000	0000000	0000000
4	0100110	0000000	0000000	0000000
5	0100101	0000000	0000000	0000000
6	0100101	0000000	0000000	0000000
7	0100101	0000000	0000000	0000000
8	0100100	0000000	0000000	0000000
9	0100011	0000000	0000000	0000000
10	1001010	0000000	0000000	0000000
11	1001010	0000000	0000000	0000000
12	1001001	0000000	0000000	0000000
13	1000111	0000000	0000000	0000000
14	1000101	0000000	0000000	0000000
15	1000100	0000000	0000000	0000000
16	1000011	0000000	0000000	0000000

SCAL[5:0] = 110110[1] (default), One step change of this value of SCAL[5:0] results in 2% scaling up/down against the pulse amplitude.

1. In T1 mode, when arbitrary pulse for short haul application is configured, users should write '110110' to SCAL[5:0] bits if no scaling is required.

Table-5 Transmit Waveform Value For T1 133~266 ft

Sample	UI 1	UI 2	UI 3	UI 4
1	0011011	1000011	0000000	0000000
2	0101110	1000010	0000000	0000000
3	0101100	1000001	0000000	0000000
4	0101010	0000000	0000000	0000000
5	0101001	0000000	0000000	0000000
6	0101000	0000000	0000000	0000000
7	0100111	0000000	0000000	0000000
8	0100110	0000000	0000000	0000000
9	0100101	0000000	0000000	0000000
10	1010000	0000000	0000000	0000000
11	1001111	0000000	0000000	0000000
12	1001101	0000000	0000000	0000000
13	1001010	0000000	0000000	0000000
14	1001000	0000000	0000000	0000000
15	1000110	0000000	0000000	0000000
16	1000100	0000000	0000000	0000000

See Table-4

Table-6 Transmit Waveform Value For T1 266~399 ft

Sample	UI 1	UI 2	UI 3	UI 4
1	0011111	1000011	0000000	0000000
2	0110100	1000010	0000000	0000000
3	0101111	1000001	0000000	0000000
4	0101100	0000000	0000000	0000000
5	0101011	0000000	0000000	0000000
6	0101010	0000000	0000000	0000000
7	0101001	0000000	0000000	0000000
8	0101000	0000000	0000000	0000000
9	0100101	0000000	0000000	0000000
10	1010111	0000000	0000000	0000000
11	1010011	0000000	0000000	0000000
12	1010000	0000000	0000000	0000000
13	1001011	0000000	0000000	0000000
14	1001000	0000000	0000000	0000000
15	1000110	0000000	0000000	0000000
16	1000100	0000000	0000000	0000000

See Table-4

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Table-7 Transmit Waveform Value For T1 399~533 ft

Sample	UI 1	UI 2	UI 3	UI 4
1	0100000	1000011	0000000	0000000
2	0111011	1000010	0000000	0000000
3	0110101	1000001	0000000	0000000
4	0101111	0000000	0000000	0000000
5	0101110	0000000	0000000	0000000
6	0101101	0000000	0000000	0000000
7	0101100	0000000	0000000	0000000
8	0101010	0000000	0000000	0000000
9	0101000	0000000	0000000	0000000
10	1011000	0000000	0000000	0000000
11	1011000	0000000	0000000	0000000
12	1010011	0000000	0000000	0000000
13	1001100	0000000	0000000	0000000
14	1001000	0000000	0000000	0000000
15	1000110	0000000	0000000	0000000
16	1000100	0000000	0000000	0000000
See Table-4				

Table-8 Transmit Waveform Value For T1 533~655 ft

Sample	UI 1	UI 2	UI 3	UI 4
1	0100000	1000011	0000000	0000000
2	0111111	1000010	0000000	0000000
3	0111000	1000001	0000000	0000000
4	0110011	0000000	0000000	0000000
5	0101111	0000000	0000000	0000000
6	0101110	0000000	0000000	0000000
7	0101101	0000000	0000000	0000000
8	0101100	0000000	0000000	0000000
9	0101001	0000000	0000000	0000000
10	1011111	0000000	0000000	0000000
11	1011110	0000000	0000000	0000000
12	1010111	0000000	0000000	0000000
13	1001111	0000000	0000000	0000000
14	1001001	0000000	0000000	0000000
15	1000111	0000000	0000000	0000000
16	1000100	0000000	0000000	0000000
See Table-4				

Table-9 Transmit Waveform Value For J1 0~655 ft

Sample	UI 1	UI 2	UI 3	UI 4
1	0010111	1000010	0000000	0000000
2	0100111	1000001	0000000	0000000
3	0100111	0000000	0000000	0000000
4	0100110	0000000	0000000	0000000
5	0100101	0000000	0000000	0000000
6	0100101	0000000	0000000	0000000
7	0100101	0000000	0000000	0000000
8	0100100	0000000	0000000	0000000
9	0100011	0000000	0000000	0000000
10	1001010	0000000	0000000	0000000
11	1001010	0000000	0000000	0000000
12	1001001	0000000	0000000	0000000
13	1000111	0000000	0000000	0000000
14	1000101	0000000	0000000	0000000
15	1000100	0000000	0000000	0000000
16	1000011	0000000	0000000	0000000
SCAL[5:0] = 110110 (default), One step change of this value of SCAL[5:0] results in 2% scaling up/down against the pulse amplitude.				

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3.2.4 TRANSMIT PATH LINE INTERFACE

The transmit line interface consists of TTIPn pin and TRINGn pin. The impedance matching can be realized by the internal impedance matching circuit or the external impedance matching circuit. If T_TERM[2] is set to '0', the internal impedance matching circuit will be selected. In this case, the T_TERM[1:0] bits (**TERM, 1AH...**) can be set to choose 75 Ω, 100 Ω, 110 Ω or 120 Ω internal impedance of TTIPn/TRINGn. If T_TERM[2] is set to '1', the internal impedance matching circuit will be disabled. In this case, the external impedance matching circuit will be used to realize the impedance matching. For T1/J1 mode, the external impedance matching circuit for the transmitter is not supported. Figure-8 shows the appropriate external components to connect with the cable for one channel. Table-10 is the list of the recommended impedance matching for transmitter.

The TTIPn/TRINGn can be turned into high impedance globally by pulling THZ pin to high or individually by setting the THZ bit (**TCF1, 03H...**) to '1'. In this state, the internal transmit circuits are still active.

Besides, in the following cases, TTIPn/TRINGn will also become high impedance:

- Loss of MCLK: all TTIPn/TRINGn pins become high impedance; ·
- Loss of TCLKn: corresponding TTIPn/TRINGn become HZ (exceptions: Remote Loopback; Transmit internal pattern by MCLK);
- Transmit path power down;
- After software reset; pin reset and power on.

Table-10 Impedance Matching for Transmitter

Cable Configuration	Internal Termination			External Termination		
	T_TERM[2:0]	PULS[3:0]	R_T	T_TERM[2:0]	PULS[3:0]	R_T
E1/75 Ω	000	0000	0 Ω	1XX	0001	9.4 Ω
E1/120 Ω	001	0001			0001	
T1/0~133 ft	010	0010		-	-	-
T1/133~266 ft		0011				
T1/266~399 ft		0100				
T1/399~533 ft		0101				
T1/533~655 ft		0110				
J1/0~655 ft	011	0111				

Note: The precision of the resistors should be better than ± 1%

3.2.5 TRANSMIT PATH POWER DOWN

The transmit path can be powered down individually by setting the T_OFF bit (**TCF0, 02H...**) to '1'. In this case, the TTIPn/TRINGn pins are turned into high impedance.

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3.3 RECEIVE PATH

The receive path consists of Receive Internal Termination, Monitor Gain, Amplitude/Wave Shape Detector, Digital Tuning Controller, Adaptive Equalizer, Data Slicer, CDR (Clock and Data Recovery), Optional Jitter Attenuator, Decoder and LOS/AIS Detector. Refer to Figure-7.

3.3.1 RECEIVE INTERNAL TERMINATION

The impedance matching can be realized by the internal impedance matching circuit or the external impedance matching circuit. If R_TERM[2] is set to '0', the internal impedance matching circuit will be selected. In this case, the R_TERM[1:0] bits (**TERM, 1AH...**) can be set to choose 75 Ω, 100 Ω, 110 Ω or 120 Ω internal impedance of RTIPn/RRINGn. If R_TERM[2] is set to '1', the internal impedance matching circuit will be disabled. In this case, the external impedance matching circuit will be used to realize the impedance matching.

Figure-8 shows the appropriate external components to connect with the cable for one channel. Table-11 is the list of the recommended impedance matching for receiver.

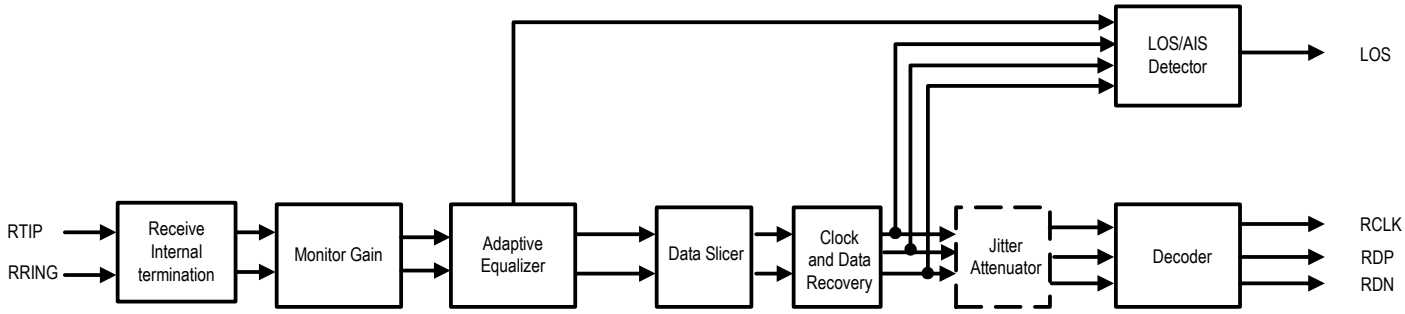
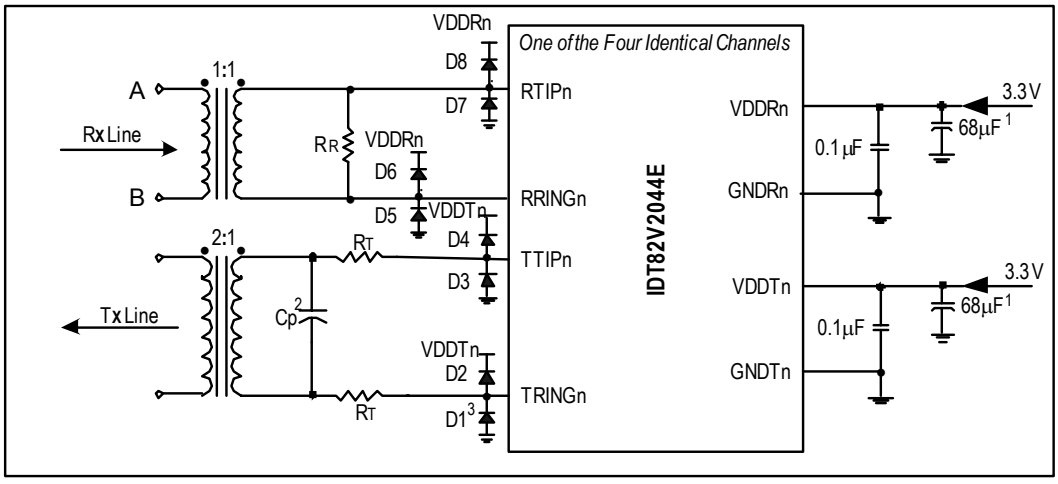


Figure-7 Receive Path Function Block Diagram

Table-11 Impedance Matching for Receiver

Cable Configuration	Internal Termination		External Termination	
	R_TERM[2:0]	R_R	R_TERM[2:0]	R_R
E1/75 Ω	000	120 Ω	1XX	75 Ω
E1/120 Ω	001			120 Ω
T1	010			100 Ω
J1	011			110 Ω



Note: 1. Common decoupling capacitor
2. Cp 0-560 (pF)
3. D1 - D8, Motorola - MBR0540T1; International Rectifier - 11DQ04 or 10BQ060

Figure-8 Transmit/Receive Line Circuit

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3.3.2 LINE MONITOR

In both T1/J1 and E1 short haul applications, the non-intrusive monitoring on channels located in other chips can be performed by tapping the monitored channel through a high impedance bridging circuit. Refer to Figure-9 and Figure-10.

After a high resistance bridging circuit, the signal arriving at the RTIPn/RRINGn is dramatically attenuated. To compensate this attenuation, the Monitor Gain can be used to boost the signal by 22 dB, 26 dB and 32 dB, selected by MG[1:0] bits (**RCF2, 09H...**). For normal operation, the Monitor Gain should be set to 0 dB.

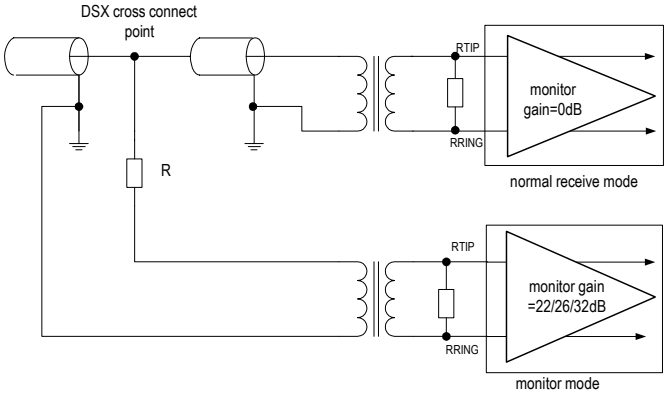


Figure-9 Monitoring Receive Line in Another Chip

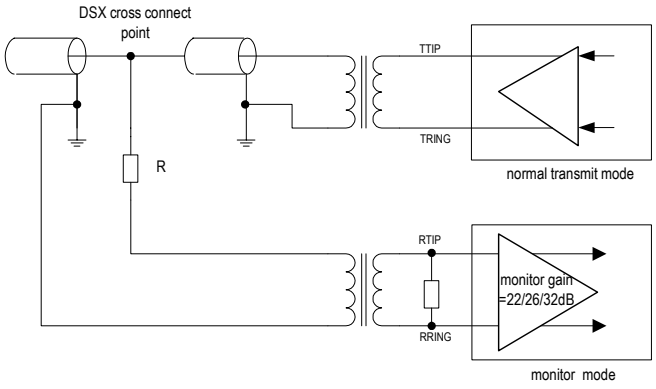


Figure-10 Monitor Transmit Line in Another Chip

3.3.3 ADAPTIVE EQUALIZER

The Adaptive Equalizer can be enabled to increase the receive sensitivity and to allow programming of the LOS level up to -24 dB. See section 3.5 LOS AND AIS DETECTION. It can be enabled or disabled by setting EQ_ON bit to '1' or '0' (**RCF1, 08H...**).

3.3.4 RECEIVE SENSITIVITY

The Receive Sensitivity for both E1 and T1/J1 is -10 dB. With the Adaptive Equalizer enabled, the receive sensitivity will be -20 dB.

3.3.5 DATA SLICER

The Data Slicer is used to generate a standard amplitude mark or a space according to the amplitude of the input signals. The threshold can be 40%, 50%, 60% or 70%, as selected by the SLICE[1:0] bits (**RCF2, 09H...**). The output of the Data Slicer is forwarded to the CDR (Clock & Data Recovery) unit or to the RDPn/RDNn pins directly if the CDR is disabled.

3.3.6 CDR (Clock & Data Recovery)

The CDR is used to recover the clock from the received signals. The recovered clock tracks the jitter in the data output from the Data Slicer and keeps the phase relationship between data and clock during the absence of the incoming pulse. The CDR can also be by-passed in the Dual Rail mode. When CDR is by-passed, the data from the Data Slicer is output to the RDPn/RDNn pins directly.

3.3.7 DECODER

In T1/J1 applications, the R_MD[1:0] bits (**RCF0, 07H...**) is used to select the AMI decoder or B8ZS decoder. In E1 applications, the R_MD[1:0] bits (**RCF0, 07H...**) are used to select the AMI decoder or HDB3 decoder.

3.3.8 RECEIVE PATH SYSTEM INTERFACE

The receive path system interface consists of RCLKn pin, RDn/RDPn pin and RDNn pin. In E1 mode, the RCLKn outputs a recovered 2.048 MHz clock. In T1/J1 mode, the RCLKn outputs a recovered 1.544 MHz clock. The received data is updated on the RDn/RDPn and RDNn pins on the active edge of RCLKn. The active edge of RCLKn can be selected by the RCLK_SEL bit (**RCF0, 07H...**). And the active level of the data on RDn/RDPn and RDNn can also be selected by the RD_INV bit (**RCF0, 07H...**).

The received data can be output to the system side in two different ways: Single Rail or Dual Rail, as selected by R_MD bit [1] (**RCF0, 07H...**). In Single Rail mode, only RDn pin is used to output data and the RDNn/CVn pin is used to report the received errors. In Dual Rail Mode, both RDPn pin and RDNn pin are used for outputting data.

In the receive Dual Rail mode, the CDR unit can be by-passed by setting R_MD[1:0] to '11' (binary). In this situation, the output data from the Data Slicer will be output to the RDPn/RDNn pins directly, and the RCLKn outputs the exclusive OR (XOR) of the RDPn and RDNn.

3.3.9 RECEIVE PATH POWER DOWN

The receive path can be powered down individually by setting R_OFF bit (**RCF0, 07H...**) to '1'. In this case, the RCLKn, RDn/RDPn, RDPn and LOSn will be logic low.

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3.3.10 G.772 NON-INTRUSIVE MONITORING

In applications using only three channels, channel 1 can be configured to monitor the data received or transmitted in any one of the remaining channels. The MON[3:0] bits (**GCF1, 60H**) determine which channel and which direction (transmit/receive) will be monitored. The monitoring is non-intrusive per ITU-T G.772. Figure-11 illustrates the concept.

The monitored line signal (transmit or receive) goes through Channel 1's Clock and Data Recovery. The signal can be observed digitally at the RCLK1, RD1/RDP1 and RDN1. If Channel 1 is configured to Remote Loopback while in the Monitoring mode, the monitored data will be output on TTIP1/TRING1.

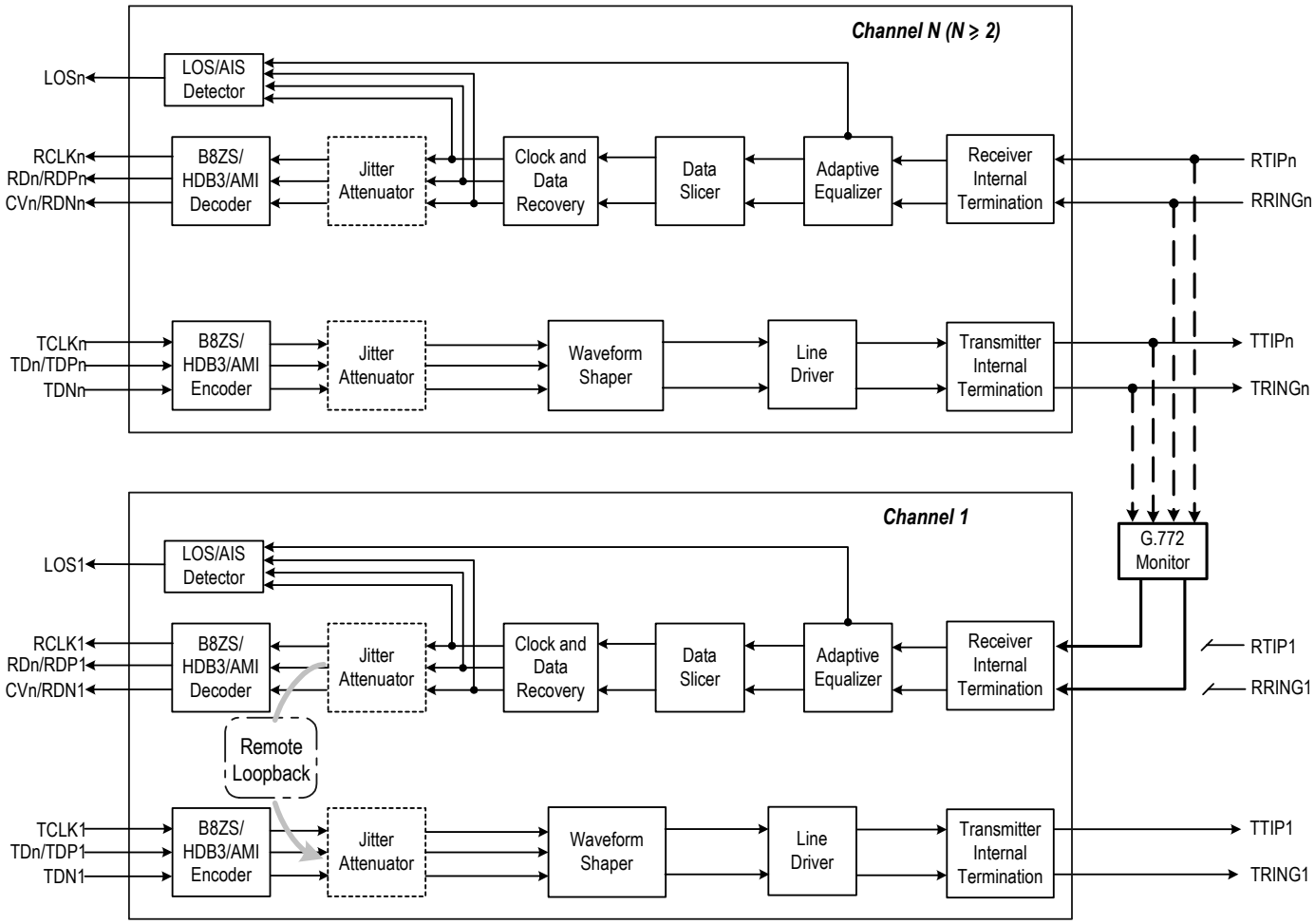


Figure-11 G.772 Monitoring Diagram

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3.4 JITTER ATTENUATOR

There is one Jitter Attenuator in each channel of the LIU. The Jitter Attenuator can be deployed in the transmit path or the receive path, and can also be disabled. This is selected by the JACF[1:0] bits (**JACF, 01H...**).

3.4.1 JITTER ATTENUATION FUNCTION DESCRIPTION

The Jitter Attenuator is composed of a FIFO and a DPLL, as shown in Figure-12. The FIFO is used as a pool to buffer the jittered input data, then the data is clocked out of the FIFO by a de-jittered clock. The depth of the FIFO can be 32 bits, 64 bits or 128 bits, as selected by the JADP[1:0] bits (**JACF, 01H...**). Consequently, the constant delay of the Jitter Attenuator will be 16 bits, 32 bits or 64 bits. Deeper FIFO can tolerate larger jitter, but at the expense of increasing data latency time.

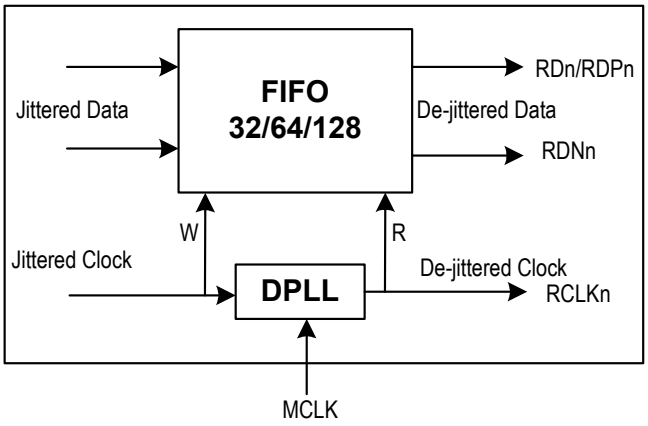


Figure-12 Jitter Attenuator

In E1 applications, the Corner Frequency of the DPLL can be 0.9 Hz or 6.8 Hz, as selected by the JABW bit (**JACF, 01H...**). In T1/J1 applications, the Corner Frequency of the DPLL can be 1.25 Hz or 5.00 Hz, as selected by the JABW bit (**JACF, 01H...**). The lower the Corner Frequency is, the longer time is needed to achieve synchronization.

When the incoming data moves faster than the outgoing data, the FIFO will overflow. This overflow is captured by the JAOV_IS bit (**INTS1, 17H...**). If the incoming data moves slower than the outgoing data, the FIFO will underflow. This underflow is captured by the JAUD_IS bit (**INTS1, 17H...**). For some applications that are sensitive to data corruption, the JA limit mode can be enabled by setting JA_LIMIT bit (**JACF, 01H...**) to '1'. In the JA limit mode, the speed of the outgoing data will be adjusted automatically when the FIFO is close to its full or emptiness. The criteria of starting speed adjustment are shown in Table-12. The JA limit mode can reduce the possibility of FIFO overflow and underflow, but the quality of jitter attenuation is deteriorated.

3.4.2 JITTER ATTENUATOR PERFORMANCE

The performance of the Jitter Attenuator in the IDT82V2044E meets the ITU-T I.431, G.703, G.736-739, G.823, G.824, ETSI 300011, ETSI TBR12/13, AT&T TR62411 specifications. Details of the Jitter Attenuator performance is shown in Table-64 Jitter Tolerance and Table-65 Jitter Attenuator Characteristics.

Table-12 Criteria of Starting Speed Adjustment

FIFO Depth	Criteria for Adjusting Data Outgoing Speed
32 Bits	2 bits close to its full or emptiness
64 Bits	3 bits close to its full or emptiness
128 Bits	4 bits close to its full or emptiness

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3.5 LOS AND AIS DETECTION

3.5.1 LOS DETECTION

The Loss of Signal Detector monitors the amplitude of the incoming signal level and pulse density of the received signal on RTIPn and RRINGn.

- **LOS declare (LOS=1)**

A LOS is detected when the incoming signal has “no transitions”, i.e., when the signal level is less than Q dB below nominal for N consecutive pulse intervals. Here N is defined by LAC bit (**MAINT0, 0AH...**). LOS will be declared by pulling LOSn pin to high (LOS=1) and LOS interrupt will be generated if it is not masked.

- **LOS clear (LOS=0)**

The LOS is cleared when the incoming signal has “transitions”, i.e., when the signal level is greater than P dB below nominal and has an average pulse density of at least 12.5% for M consecutive pulse intervals, starting with the receipt of a pulse. Here M is defined by LAC bit (**MAINT0, 0AH...**). LOS status is cleared by pulling LOSn pin to low.

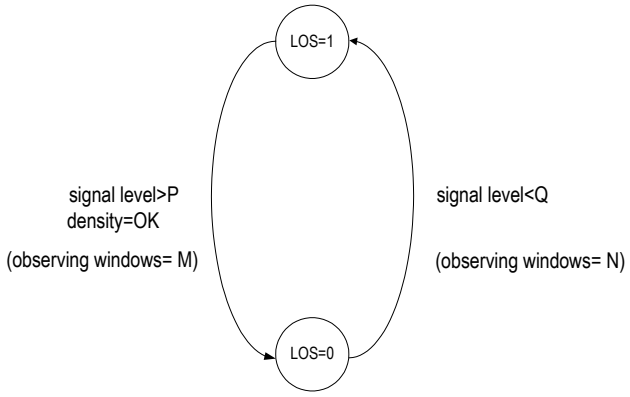


Figure-13 LOS Declare and Clear

- **LOS detect level threshold**

With the Adaptive Equalizer off, the amplitude threshold Q is fixed on 800 mVpp, while P=Q+200 mVpp (200 mVpp is the LOS level detect hysteresis).

With the Adaptive Equalizer on, the value of Q can be selected by LOS[4:0] bit (**RCF1, 08H...**), while P=Q+4 dB (4 dB is the LOS level detect hysteresis). Refer to Table 33, “RCF1: Receiver Configuration Register 1,” on page 40 for LOS[4:0] bit values available.

- **Criteria for declare and clear of a LOS detect**

The detection supports the ANSI T1.231 and I.431 for T1/J1 mode and G.775 and ETSI 300233/I.431 for E1 mode. The criteria can be selected by LAC bit (**MAINT0, 0AH...**) and T1E1 bit **(GCF0, 40H)**.

Table-13 and Table-14 summarize LOS declare and clear criteria for both with and without the Adaptive Equalizer enabled.

- **All Ones output during LOS**

On the system side, the RDPn/RDNn will reflect the input pulse “transition” at the RTIPn/RRINGn side and output recovery clock (but the quality of the output clock can not be guaranteed when the input level is lower than the maximum receive sensitivity) when AISE bit (**MAINT0, 0AH...**) is 0; or output All Ones as AIS when AISE bit (**MAINT0, 0AH...**) is 1. In this case RCLKn output is replaced by MCLK.

On the line side, the TTIPn/TRINGn will output All Ones as AIS when ATAO bit (**MAINT0, 0AH...**) is 1. The All Ones pattern uses MCLK as the reference clock.

LOS indicator is always active for all kinds of loopback modes.

Table-13 LOS Declare and Clear Criteria, Adaptive Equalizer Disabled

Control bit		LOS declare threshold	LOS clear threshold
T1E1	LAC		
1=T1/J1	0=T1.231	Level < 800 mVpp N=175 bits	Level > 1 Vpp M=128 bits 12.5% mark density <100 consecutive zeroes
	1=I.431	Level < 800 mVpp N=1544 bits	Level > 1 Vpp M=128 bits 12.5% mark density <100 consecutive zeroes
0=E1	0=G.775	Level < 800 mVpp N=32 bits	Level > 1 Vpp M=32 bits 12.5% mark density <16 consecutive zeroes
	1=I.431/ETSI	Level < 800 mVpp N=2048 bits	Level > 1 Vpp M=32 bits 12.5% mark density <16 consecutive zeroes

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Table-14 LOS Declare and Clear Criteria, Adaptive Equalizer Enabled

Control bit					LOS declare threshold	LOS clear threshold	Note
T1E1	LAC		LOS[4:0]	Q (dB)			
1=T1/J1	0	T1.231	00000 00001 … 01010 01011 - 11111	-4 -6 … -24 Reserved	Level < Q N=175 bits	Level > Q+ 4dB M=128 bits 12.5% mark density <100 consecutive zeroes	
	1	-	00000 … 00110	-4 -16	Level < Q N=1544 bits	Level > Q+ 4dB M=128 bits 12.5% mark density <100 consecutive zeroes	I.431 Level detect range is -18 to -30 dB.
		I.431	00111 01010 01011 - 11111	-18 -24 Reserved			
0=E1	0	-	00000 … 00010	-4 … -8	Level < Q N=32 bits	Level > Q+ 4dB M=32 bits 12.5% mark density <16 consecutive zeroes	G.775 Level detect range is -9 to -35 dB.
		G.775	00011 … 01010 01011 - 11111	-10 … -24 Reserved			
	1	-	00000	-4	Level < Q N=2048 bits	Level > Q+ 4dB M=32 bits 12.5% mark density <16 consecutive zeroes	I.431 Level detect range is -6 to -20 dB.
		I.431/ ETSI	00001 … 01010 01011 - 11111	-6 … -24 Reserved			

3.5.2 AIS DETECTION

The Alarm Indication Signal can be detected by the IDT82V2044E when the Clock&Data Recovery unit is enabled. The status of AIS detection is reflected in the AIS_S bit (**STAT0, 14H...**). In T1/J1 applications, the criteria for declaring/clearing AIS detection are in compliance with the ANSI T1.231. In E1 applications, the criteria for declaring/clearing AIS detection comply with the ITU G.775 or the ETSI 300233, as selected by the LAC bit (**MAINT0, 0AH...**). Table-15 summarizes different criteria for AIS detection Declaring/Clearing.

Table-15 AIS Condition

	ITU G.775 for E1 (LAC bit is set to '0' by default)	ETSI 300233 for E1 (LAC bit is set to '1')	ANSI T1.231 for T1/J1
AIS detected	Less than 3 zeros contained in each of two consecutive 512-bit streams are received	Less than 3 zeros contained in a 512-bit stream are received	Less than 9 zeros contained in an 8192-bit stream (a ones density of 99.9% over a period of 5.3ms)
AIS cleared	3 or more zeros contained in each of two consecutive 512-bit streams are received	3 or more zeros contained in a 512-bit stream are received	9 or more zeros contained in an 8192-bit stream are received

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3.6 TRANSMIT AND DETECT INTERNAL PATTERNS

The internal patterns (All Ones, All Zeros, PRBS/QRSS pattern and Activate/Deactivate Loopback Code) will be generated and detected by the IDT82V2044E. TCLKn is used as the reference clock by default. MCLK can also be used as the reference clock by setting the PATT_CLK bit (**MAINT0, 0AH...**) to '1'.

If the PATT_CLK bit (**MAINT0, 0AH...**) is set to '0' and the PATT[1:0] bits (**MAINT0, 0AH...**) are set to '00', the transmit path will operate in normal mode.

3.6.1 TRANSMIT ALL ONES

In transmit direction, the All Ones data can be inserted into the data stream when the PATT[1:0] bits (**MAINT0, 0AH...**) are set to '01'. The transmit data stream is output from TTIPn/TRINGn. In this case, either TCLKn or MCLK can be used as the transmit clock, as selected by the PATT_CLK bit (**MAINT0, 0AH...**).

3.6.2 TRANSMIT ALL ZEROS

If the PATT_CLK bit (**MAINT0, 0AH...**) is set to '1', the All Zeros will be inserted into the transmit data stream when the PATT[1:0] bits (**MAINT0, 0AH...**) are set to '00'.

3.6.3 PRBS/QRSS GENERATION AND DETECTION

A PRBS/QRSS will be generated in the transmit direction and detected in the receive direction by IDT82V2044E. The QRSS is 2^{20}-1 for T1/J1 applications and the PRBS is 2^{15}-1 for E1 applications, with maximum zero restrictions according to the AT&T TR62411 and ITU-T O.151.

When the PATT[1:0] bits (**MAINT0, 0AH...**) are set to '10', the PRBS/QRSS pattern will be inserted into the transmit data stream with the MSB first. The PRBS/QRSS pattern will be transmitted directly or invertedly.

The PRBS/QRSS in the received data stream will be monitored. If the PRBS/QRSS has reached synchronization status, the PRBS_S bit (**STAT0, 14H...**) will be set to '1', even in the presence of a logic error rate less than or equal to 10^{-1}. The criteria for setting/clearing the PRBS_S bit are shown in Table-16.

Table-16 Criteria for Setting/Clearing the PRBS_S Bit

PRBS/QRSS Detection	6 or less than 6 bit errors detected in a 64 bits hopping window.
PRBS/QRSS Missing	More than 6 bit errors detected in a 64 bits hopping window.

PRBS data can be inverted through setting the PRBS_INV bit (**MAINT0, 0AH...**).

Any change of PRBS_S bit will be captured by PRBS_IS bit (**INTS0, 16H...**). The PRBS_IES bit (**INTES, 13H...**) can be used to determine whether the '0' to '1' change of PRBS_S bit will be captured by the PRBS_IS bit or any changes of PRBS_S bit will be captured by the PRBS_IS bit. When the PRBS_IS bit is '1', an interrupt will be generated if the PRBS_IM bit (**INTM0, 11H...**) is set to '1'.

The received PRBS/QRSS logic errors can be counted in a 16-bit counter if the ERR_SEL [1:0] bits (**MAINT6, 10H...**) are set to '00'. Refer to Refer to 3.8 ERROR DETECTION/COUNTING AND INSERTION for the operation of the error counter.

3.7 LOOPBACK

To facilitate testing and diagnosis, the IDT82V2044E provides four different loopback configurations: Analog Loopback, Digital Loopback, Remote Loopback and Inband Loopback.

3.7.1 ANALOG LOOPBACK

When the ALP bit (**MAINT1, 0BH...**) is set to '1', the corresponding channel is configured in Analog Loopback mode. In this mode, the transmit signals are looped back to the Receiver Internal Termination in the receive path then output from RCLKn, RDn, RDPn/RDNn. At the same time, the transmit signals are still output to TTIPn/TRINGn in transmit direction. Figure-14 shows the process.

3.7.2 DIGITAL LOOPBACK

When the DLP bit (**MAINT1, 0BH...**) is set to '1', the corresponding channel is configured in Digital Loopback mode. In this mode, the transmit signals are looped back to the jitter attenuator (if enabled) and decoder in receive path, then output from RCLKn, RDn, RDPn/RDNn. At the same time, the transmit signals are still output to TTIPn/TRINGn in transmit direction. Figure-15 shows the process.

Both Analog Loopback mode and Digital Loopback mode allow the sending of the internal patterns (All Ones, All Zeros, PRBS, etc.) which will overwrite the transmit signals. In this case, either TCLKn or MCLK can be used as the reference clock for internal patterns transmission.

3.7.3 REMOTE LOOPBACK

When the RLP bit (**MAINT1, 0BH...**) is set to '1', the corresponding channel is configured in Remote Loopback mode. In this mode, the recovered clock and data output from Clock and Data Recovery on the receive path is looped back to the jitter attenuator (if enabled) and Waveform Shaper in transmit path. Figure-16 shows the process.

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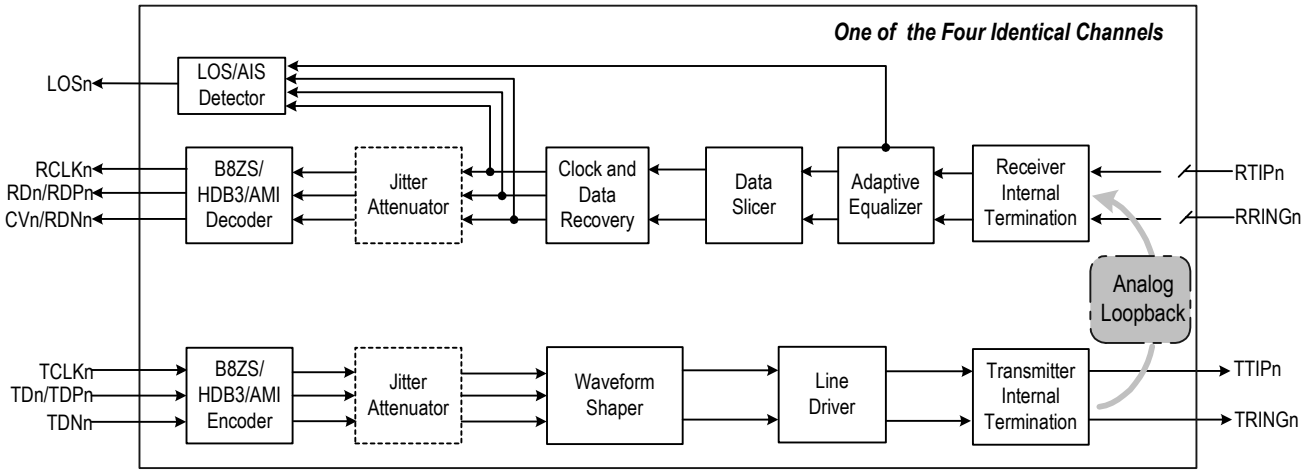


Figure-14 Analog Loopback

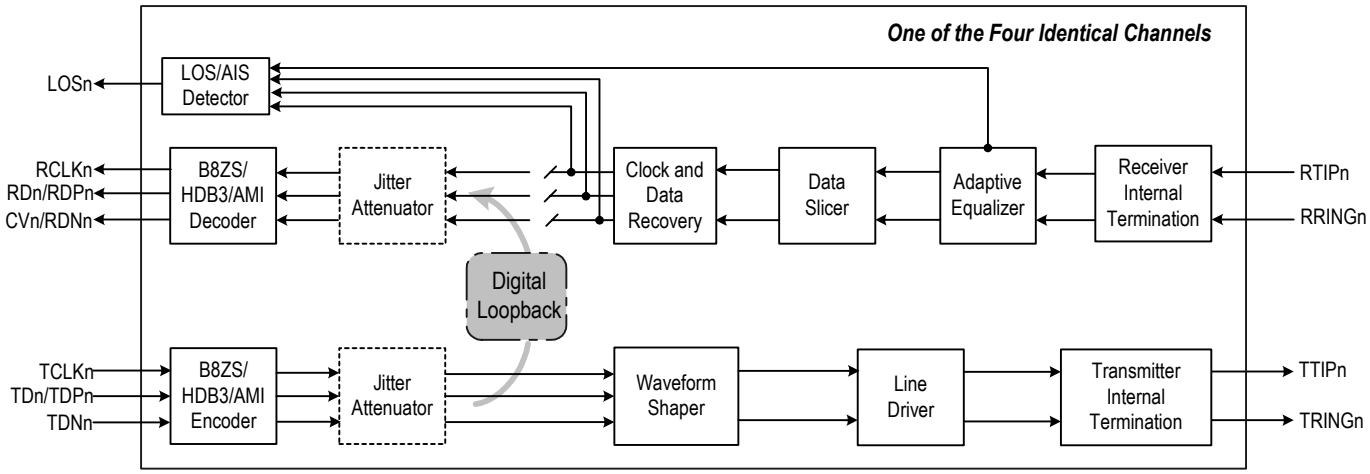


Figure-15 Digital Loopback

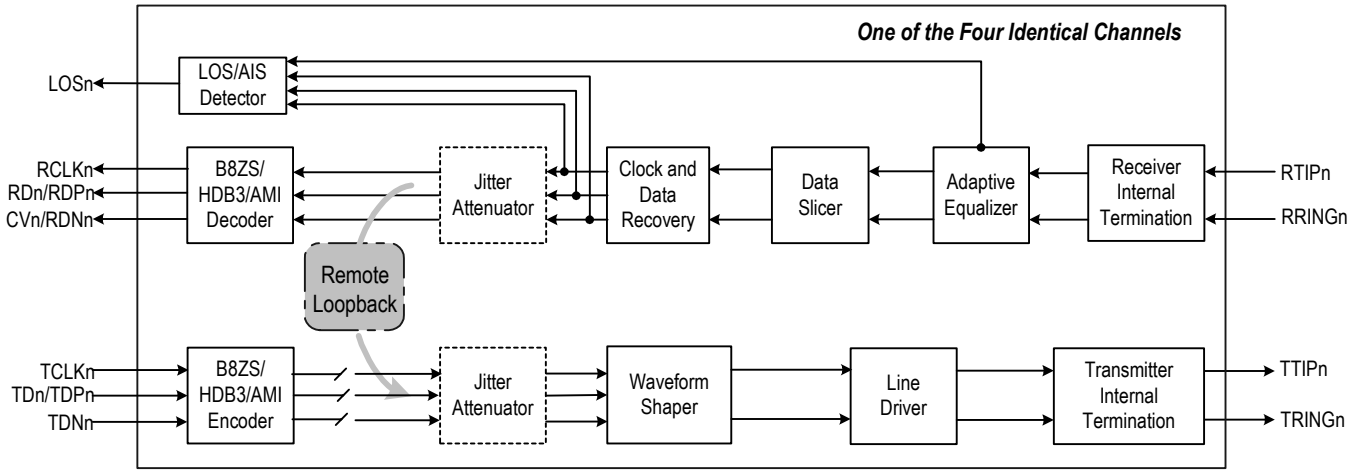


Figure-16 Remote Loopback

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3.7.4 INBAND LOOPBACK

When PATT[1:0] bits (**MAINT0, 0AH...**) are set to '11', the corresponding channel is configured in Inband Loopback mode. In this mode, an unframed activate/Deactivate Loopback Code is generated repeatedly in transmit direction per ANSI T1. 403 which overwrite the transmit signals. In receive direction, the framed or unframed code is detected per ANSI T1. 403, even in the presence of 10^{-2} bit error rate.

If the Automatic Remote Loopback is enabled by setting ARLP bit (**MAINT1, 0BH...**) to '1', the chip will establish/demolish the Remote Loopback based on the reception of the Activate Loopback Code/Deactivate Loopback Code for 5.1 s. If the ARLP bit (**MAINT1, 0BH...)** is set to '0', the Remote Loopback can also be demolished forcedly.

3.7.4.1 Transmit Activate/Deactivate Loopback Code

The pattern of the transmit Activate/Deactivate Loopback Code is defined by the TIBLB[7:0] bits (**MAINT3, 0DH...**). Whether the code represents an Activate Loopback Code or a Deactivate Loopback Code is judged by the far end receiver. The length of the pattern ranges from 5 bits to 8 bits, as selected by the TIBLB_L[1:0] bits (**MAINT2, 0CH...**). The pattern can be programmed to 6-bit-long or 8-bit-long respectively by repeating itself if it is 3-bit-long or 4-bit-long. When the PATT[1:0] bits (**MAINT0, 0AH...**) are set to '11', the transmission of the Activate/Deactivate Loopback Code is initiated. If the PATT_CLK bit (**MAINT0, 0AH...**) is set to '0' and the PATT[1:0] bits (**MAINT0, 0AH...**) are set to '00', the transmission of the Activate/Deactivate Loopback Code will stop.

The local transmit activate/deactivate code setting should be the same as the receive code setting in the remote end. It is the same thing for the other way round.

3.7.4.2 Receive Activate/Deactivate Loopback Code

The pattern of the receive Activate Loopback Code is defined by the RIBLBA[7:0] bits (**MAINT4, 0EH...**). The length of this pattern ranges from 5 bits to 8 bits, as selected by the RIBLBA_L [1:0] bits (**MAINT2, 0CH...**). The pattern can be programmed to 6-bit-long or 8-bit-long respectively by repeating itself if it is 3-bit-long or 4-bit-long.

The pattern of the receive Deactivate Loopback Code is defined by the RIBLBD[7:0] bits (**MAINT5, 0FH...**). The length of the receive Deactivate Loopback Code ranges from 5 bits to 8 bits, as selected by the RIBLBD_L[1:0] bits (**MAINT2, 0CH...**). The pattern can be programmed to 6-bit-long or 8-bit-long respectively by repeating itself if it is 3-bit-long or 4-bit-long.

After the Activate Loopback Code has been detected in the receive data for more than 30 ms (in E1 mode) / 40 ms (in T1/J1 mode), the IBLBA_S bit (**STAT0, 14H...**) will be set to '1' to declare the reception of the Activate Loopback Code.

After the Deactivate Loopback Code has been detected in the receive data for more than 30 ms (In E1 mode) / 40 ms (In T1/J1 mode), the IBLBD_S bit (**STAT0, 14H...**) will be set to '1' to declare the reception of the Deactivate Loopback Code.

When the IBLBA_IES bit (**INTES, 13H...**) is set to '0', only the '0' to '1' transition of the IBLBA_S bit will generate an interrupt and set the IBLBA_IS bit (**INTS0, 16H...**) to '1'. When the IBLBA_IES bit is set to '1', any changes of the IBLBA_S bit will generate an interrupt and set the IBLBA_IS bit (**INTS0, 16H...**) to '1'. The IBLBA_IS bit will be reset to '0' after being read.

When the IBLBD_IES bit (**INTES, 13H...**) is set to '0', only the '0' to '1' transition of the IBLBD_S bit will generate an interrupt and set the IBLBD_IS bit (**INTS0, 16H...**) to '1'. When the IBLBD_IES bit is set to '1', any changes of the IBLBD_S bit will generate an interrupt and set the IBLBD_IS bit (**INTS0, 16H...**) to '1'. The IBLBD_IS bit will be reset to '0' after being read.

3.7.4.3 Automatic Remote Loopback

When ARLP bit (**MAINT1, 0BH...)** is set to '1', the corresponding channel is configured into the Automatic Remote Loopback mode. In this mode, if the Activate Loopback Code has been detected in the receive data for more than 5.1 s, the Remote Loopback (shown as Figure-16) will be established automatically, and the RLP_S bit (**STAT1, 15H...**) will be set to '1' to indicate the establishment of the Remote Loopback. The IBLBA_S bit (**STAT0, 14H...**) is set to '1' to generate an interrupt. In this case, the Remote Loopback mode will still be kept even if the receiver stop receiving the Activate Loopback Code.

If the Deactivate Loopback Code has been detected in the receive data for more than 5.1 s, the Remote Loopback will be demolished automatically, and the RLP_S bit (**STAT1, 15H...**) will set to '0' to indicate the demolishment of the Remote Loopback. The IBLBD_S bit (**STAT0, 14H...**) is set to '1' to generate an interrupt.

The Remote Loopback can also be demolished forcedly by setting ARLP bit (**MAINT1, 0BH...)** to '0'.

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3.8 ERROR DETECTION/COUNTING AND INSERTION

3.8.1 DEFINITION OF LINE CODING ERROR

The following line encoding errors can be detected and counted by the IDT82V2044E:

- Received Bipolar Violation (BPV) Error: In AMI coding, when two consecutive pulses of the same polarity are received, a BPV error is declared.
- HDB3/B8ZS Code Violation (CV) Error: In HDB3/B8ZS coding, a CV error is declared when two consecutive BPV errors are detected, and the pulses that have the same polarity as the previous pulse are not the HDB3/B8ZS zero substitution pulses.
- Excess Zero (EXZ) Error: there are two standards defining the EXZ errors: ANSI and FCC. The EXZ_DEF bit (**MAINT6, 10H...**) chooses which standard will be adopted by the corresponding channel to judge the EXZ error. Table-17 shows definition of EXZ.

Table-17 EXZ Definition

	EXZ Definition	
	ANSI	**FCC**
AMI	More than 15 consecutive 0s are detected	More than 80 consecutive 0s are detected
HDB3	More than 3 consecutive 0s are detected	More than 3 consecutive 0s are detected
B8ZS	More than 7 consecutive 0s are detected	More than 7 consecutive 0s are detected

3.8.2 ERROR DETECTION AND COUNTING

Which type of the receiving errors (Received CV/BPV errors, excess zero errors and PRBS logic errors) will be counted is determined by ERR_SEL[1:0] bits (**MAINT6, 10H...**). Only one type of receiving error can be counted at a time except that when the ERR_SEL[1:0] bits are set to '11', both CV/BPV and EXZ errors will be detected and counted.

The receiving errors are counted in an internal 16-bit Error Counter. Once an error is detected, an error interrupt which is indicated by corresponding bit in (**INTS1, 17H...**) will be generated if it is not masked. This Error Counter can be operated in two modes: Auto Report Mode and Manual Report Mode, as selected by the CNT_MD bit (**MAINT6, 10H...**). In Single Rail mode, once BPV or CV errors are detected, the CVn pin will be driven to high for one RCLK period.

- **Auto Report Mode**

In Auto Report Mode, the internal counter starts to count the received errors when the CNT_MD bit (**MAINT6, 10H...**) is set to '1'. A one-second timer is used to set the counting period. The received errors are counted within one second. If the one-second timer expires, the value in the internal counter will be transferred to (**CNT0, 18H...**) and (**CNT1, 19H...**), then the internal counter will be reset and start to count received errors for the next second. The errors occurred during the transfer will be accumulated to the next round. The expiration of the one-second timer will set TMOV_IS bit (**INTS1, 17H...**) to '1', and will generate an interrupt if the TIMER_IM bit (**INTM1, 12H...**) is set to '0'. The TMOV_IS bit (**INTS1, 17H...**) will be cleared after the interrupt register is read. The content in the (**CNT0, 18H...**) and (**CNT1, 19H...**) should be read within the next second. If the counter overflows, a counter overflow interrupt which is indicated by CNT_OV_IS bit (**INTS1, 17H...**) will be generated if it is not masked by CNT_IM bit (**INTM1, 12H...**).

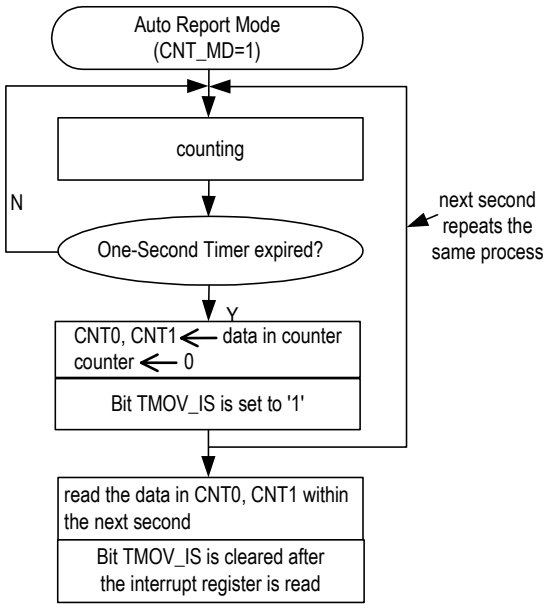


Figure-17 Auto Report Mode

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- **Manual Report Mode**

In Manual Report Mode, the internal Error Counter starts to count the received errors when the CNT_MD bit **(MAINT6, 10H...)** is set to '0'. When there is a '0' to '1' transition on the CNT_TRF bit **(MAINT6, 10H...)**, the data in the counter will be transferred to **(CNT0, 18H...)** and **(CNT1, 19H...)**, then the counter will be reset. The errors occurred during the transfer will be accumulated to the next round. If the counter overflows, a counter overflow interrupt indicated by CNT_OV_IS bit **(INTS1, 17H...)** will be generated if it is not masked by CNT_IM bit **(INTM1, 12H...)**.

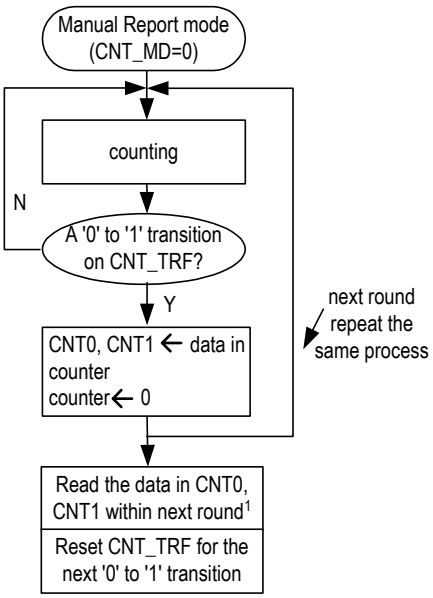


Figure-18 Manual Report Mode

Note: 1. It is recommended that users should do the followings within next round of error counting: Read the data in CNT0 and CNT1; Reset CNT_TRF bit for the next '0' to '1' transition on this bit.

3.8.3 BIPOLAR VIOLATION AND PRBS ERROR INSERTION

Only when three consecutive '1's are detected in the transmit data stream, will a '0' to '1' transition on the BPV_INS bit (**MAINT6, 10H...**) generate a bipolar violation pulse, and the polarity of the second '1' in the series will be inverted.

A '0' to '1' transition on the EER_INS bit (**MAINT6, 10H...**) will generate a logic error during the PRBS/QRSS transmission.

3.9 LINE DRIVER FAILURE MONITORING

The transmit driver failure monitor can be enabled or disabled by setting DFM_OFF bit (**TCF1, 03H...**). If the transmit driver failure monitor is enabled, the transmit driver failure will be captured by DF_S bit (**STAT0, 14H...**). The transition of the DF_S bit is reflected by DF_IS bit (**INTS0, 16H...**), and, if enabled by DF_IM bit (**INTM0, 11H...**), will generate an interrupt. When there is a short circuit on the TTIPn/TRINGn port, the output current will be limited to 100 mA (typical) and an interrupt will be generated.

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3.10 MCLK AND TCLK

3.10.1 MASTER CLOCK (MCLK)

MCLK is an independent, free-running reference clock. MCLK is 1.544 MHz or 37.056 MHz for T1/J1 applications and 2.048 MHz or 49.152 MHz in E1 mode. This reference clock is used to generate several internal reference signals:

- Timing reference for the integrated clock recovery unit.
- Timing reference for the integrated digital jitter attenuator.
- Timing reference for microcontroller interface.
- Generation of RCLK signal during a loss of signal condition if AIS is enabled.
- Reference clock during a blue alarm Transmit All Ones (TAOS), all zeros, PRBS/QRSS and inband loopback patterns if it is selected as the reference clock. For ATAO and AIS, MCLK is always used as the reference clock.

Figure-19 shows the chip operation status in different conditions of MCLK and TCLKn. The missing of MCLK will set all the four TTIP/TRING to high impedance state.

3.10.2 TRANSMIT CLOCK (TCLK)

The TCLKn is used to sample the transmit data on TDn/TDPn, TDNn. The active edge of TCLKn can be selected by the TCLK_SEL bit (**TCF0, 02H...**). During Transmit All Ones, PRBS/QRSS patterns or Inband Loopback Code, either TCLKn or MCLK can be used as the reference clock. This is selected by the PATT_CLK bit (**MAINT0, 0AH...**).

But for Automatic Transmit All Ones and AIS, only MCLK is used as the reference clock and the PATT_CLK bit is ignored. In Automatic Transmit All Ones condition, the ATAO bit (**MAINT0, 0AH**) is set to '1'. In AIS condition, the AISE bit (**MAINT0, 0AH**) is set to '1'.

If TCLKn has been missing for more than 70 MCLK cycles, TCLK_LOS bit (**STAT0, 14H...**) will be set, and the corresponding TTIPn/TRINGn will become high impedance if this channel is not used for remote loopback or is not using MCLK to transmit internal patterns (TAOS, All Zeros, PRBS and in-band loopback code). When TCLKn is detected again, TCLK_LOS bit (**STAT0, 14H...**) will be cleared. The reference frequency to detect a TCLKn loss is derived from MCLK.

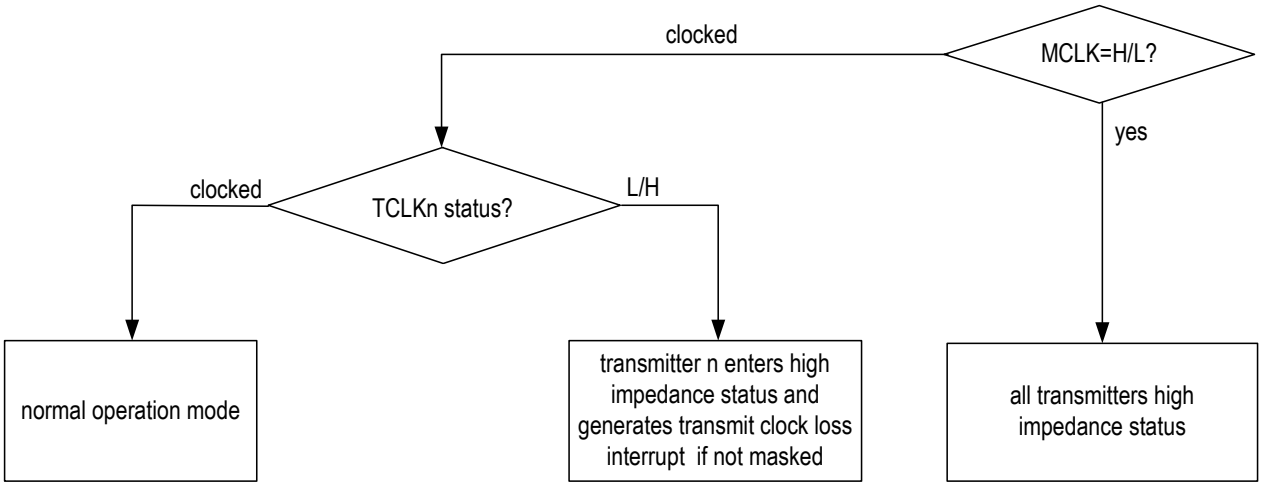


Figure-19 TCLK Operation Flowchart

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3.11 MICROCONTROLLER INTERFACES

The microcontroller interface provides access to read and write the registers in the device. The chip supports serial processor interface and two kinds of parallel processor interface: Motorola non_multiplexed mode and Intel non_multiplexed mode. By pulling pin P/$\overline{S}$ to low or to High, the microcontroller interface can be set to work in serial mode or in parallel mode respectively. Refer to 7 MICROCONTROLLER INTERFACE TIMING CHARACTERISTICS for details.

3.11.1 PARALLEL MICROCONTROLLER INTERFACE

The interface is compatible with Motorola or Intel microcontroller. Pin INT/$\overline{MOT}$ is used to select the operating mode of the parallel microcontroller interface. When pin INT/$\overline{MOT}$ is pulled to Low, the parallel microcontroller interface is configured for Motorola compatible hosts. When High, it is for Intel compatible microcontrollers.

3.11.2 SERIAL MICROCONTROLLER INTERFACE

The serial interface pins include SCLK, SDI, SDO, $\overline{CS}$ as well as SCLKE (control pin for the selection of serial clock active edge). By pulling P/$\overline{S}$ pin to LOW, the device operates in the serial host Mode. In this mode, the registers are programmed through a 24-bit word which contains an 8-bit address byte (A0~A7), a subsequent 8-bit command byte (bit R/$\overline{W}$) and an 8-bit data byte (D0~D7). When bit R/$\overline{W}$ is '1', data is read out from pin SDO. When bit R/$\overline{W}$ is '0', data is written into SDI pin. Refer to Figure-20.

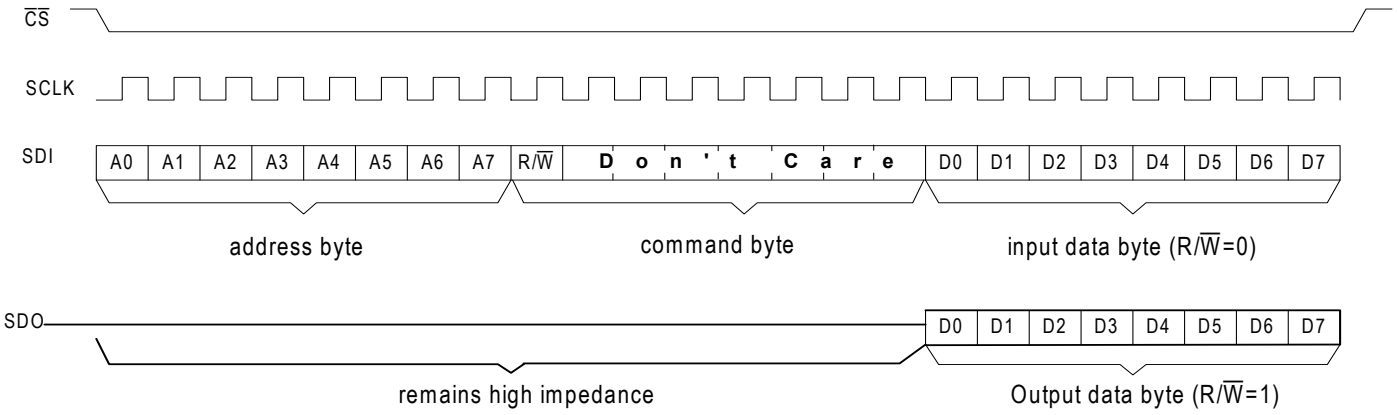


Figure-20 Serial Processor Interface Function Timing

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3.12 INTERRUPT HANDLING

All kinds of interrupt of the IDT82V2044E are indicated by the $\overline{INT}$ pin. When the INT_PIN[0] bit (**GCF0, 40H**) is '0', the $\overline{INT}$ pin is open drain active low, with a 10 KΩ external pull-up resistor. When the INT_PIN[1:0] bits (**GCF0, 40H**) are '01', the $\overline{INT}$ pin is push-pull active low; when the INT_PIN[1:0] bits are '10', the $\overline{INT}$ pin is push-pull active high.

All the interrupt can be disabled by the INTM_GLB bit (**GCF0, 40H**). When the INTM_GLB bit (**GCF0, 40H**) is set to '0', an active level on the $\overline{INT}$ pin represents an interrupt of the IDT82V2044E. The INT_CH[7:0] bits (**INTCH, 80H**) should be read to identify which channel(s) generate the interrupt.

The interrupt event is captured by the corresponding bit in the Interrupt Status Register **(INTS0, 16H...)** or **(INTS1, 17H...)**. Every kind of interrupt can be enabled/disabled individually by the corresponding bit in the register **(INTM0, 11H...)** or **(INTM1, 12H...)**. Some event is reflected by the corresponding bit in the Status Register **(STAT0, 14H...)** or **(STAT1, 15H...)**, and the Interrupt Trigger Edge Selection Register can be used to determine how the Status Register sets the Interrupt Status Register.

After the Interrupt Status Register **(INTS0, 16H...)** or **(INTS1, 17H...)** is read, the corresponding bit indicating which channel generates the interrupt in the **INTCH** register (**80H**) will be reset. Only when all the pending interrupt is acknowledged through reading the Interrupt Status Registers of all the channels **(INTS0, 16H...)** or **(INTS1, 17H...)** will all the bits in the **INTCH** register (**80H**) be reset and the $\overline{INT}$ pin become inactive.

There are totally thirteen kinds of events that could be the interrupt source for one channel:

(1).LOS Detected
(2).AIS Detected
(3).Driver Failure Detected
(4).TCLK Loss
(5).Synchronization Status of PRBS
(6).PRBS Error Detected
(7).Code Violation Received
(8).Excessive Zeros Received
(9).JA FIFO Overflow/Underflow
(10).Inband Loopback Code Status
(11).One-Second Timer Expired
(12).Error Counter Overflow
(13).Arbitrary Waveform Generator Overflow

Table-18 is a summary of all kinds of interrupt and their associated Status bit, Interrupt Status bit, Interrupt Trigger Edge Selection bit and Interrupt Mask bit.

Table-18 Interrupt Event

Interrupt Event	Status bit (STAT0, STAT1)	Interrupt Status bit (INTS0, INTS1)	Interrupt Edge Selection bit (INTES)	Interrupt Mask bit (INTM0, INTM1)
LOS Detected	LOS_S	LOS_IS	LOS_IES	LOS_IM
AIS Detected	AIS_S	AIS_IS	AIS_IES	AIS_IM
Driver Failure Detected	DF_S	DF_IS	DF_IES	DF_IM
TCLKn Loss	TCLK_LOS	TCLK_LOS_IS	TCLK_IES	TCLK_IM
Synchronization Status of PRBS/QRSS	PRBS_S	PRBS_IS	PRBS_IES	PRBS_IM
PRBS/QRSS Error		ERR_IS		ERR_IM
Code Violation Received		CV_IS		CV_IM
Excessive Zeros Received		EXZ_IS		EXZ_IM
JA FIFO Overflow		JAOV_IS		JAOV_IM
JA FIFO Underflow		JAUD_IS		JAUD_IM
Inband Loopback Activate Code Status	IBLBA_S	IBLBA_IS	IBLBA_IES	IBLBA_IM
Inband Loopback Deactivate Code Status	IBLBD_S	IBLBD_IS	IBLBD_IES	IBLBD_IM
One-Second Timer Expired		TMOV_IS		TIMER_IM
Error Counter Overflow		CNT_OV_IS		CNT_IM
Arbitrary Waveform Generator Overflow		DAC_OV_IS		DAC_OV_IM

3.13 5V TOLERANT I/O PINS

All digital input pins will tolerate 5.0 ± 5% volts and are compatible with TTL logic.

3.14 RESET OPERATION

The chip can be reset in two ways:

- Software Reset: Writing to the **RST** register (**20H**) will reset the chip in 1 us.
- Hardware Reset: Asserting the $\overline{RST}$ pin low for a minimum of 100 ns will reset the chip.

After reset, all drivers output are in high impedance state, all the internal flip-flops are reset, and all the registers are initialized to default values.

3.15 POWER SUPPLY

This chip uses a single 3.3 V power supply.

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4 PROGRAMMING INFORMATION

4.1 REGISTER LIST AND MAP

The IDT82V2044E registers can be divided into Global Registers and Local Registers. The operation on the Global Registers affects all the four channels while the operation on Local Registers only affects that specific channel. For different channel, the address of Local Register is different. Table-19 is the map of Global Registers and Table-20 is the map of Local Registers. If the configuration of all the four channels is the same, the COPY bit (**GCF0, 40H**) can be set to '1' to establish the Broadcasting mode. In the Broadcasting mode, the Writing operation on any of the four channels' registers will be copied to the corresponding registers of all the other channels.

Table-19 Global Register List and Map

Address (Hex)	Register	R/W	Map							
			b7	b6	b5	b4	b3	b2	b1	b0
00	ID	R	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
20	RST	W								
40	GCF0	R/W	-	-	-	T1E1	COPY	INTM_GLB	INT_PIN1	INT_PIN0
60	GCF1	R/W	MON3	MON2	MON1	MON0	-	-	-	-
80	INTCH	R	-	INT_CH4	-	INT_CH3	-	INT_CH2	-	INT_CH1
A0	Reserved									
C0	Reserved									
E0	Reserved									

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Table-20 Per Channel Register List and Map

Address (Hex)	Register	R/W	Map							
CH1-CH4			b7	b6	b5	b4	b3	b2	b1	b0
Jitter Attenuation Control Register										
01,41,81,C1	JACF	R/W	-	-	JA_LIMIT	JACF1	JACF0	JADP1	JADP0	JABW
Transmit Path Control Registers										
02,42,82,C2	TCF0	R/W	-	-	-	T_OFF	TD_INV	TCLK_SEL	T_MD1	T_MD0
03,43,83,C3	TCF1	R/W	-	-	DFM_OFF	THZ	PULS3	PULS2	PULS1	PULS0
04,44,84,C4	TCF2	R/W	-	-	SCAL5	SCAL4	SCAL3	SCAL2	SCAL1	SCAL0
05,45,85,C5	TCF3	R/W	DONE	RW	UI1	UI0	SAMP3	SAMP2	SAMP1	SAMP0
06,46,86,C6	TCF4	R/W	-	WDAT6	WDAT5	WDAT4	WDAT3	WDAT2	WDAT1	WDAT0
Receive Path Control Registers										
07,47,87,C7	RCF0	R/W	-	-	-	R_OFF	RD_INV	RCLK_SEL	R_MD1	R_MD0
08,48,88,C8	RCF1	R/W	-	EQ_ON	-	LOS4	LOS3	LOS2	LOS1	LOS0
09,49,89,C9	RCF2	R/W	-	-	SLICE1	SLICE0	-	-	MG1	MG0
Network Diagnostics Control Registers										
0A,4A,8A,CA	MAINT0	R/W	-	PATT1	PATT0	PATT_CLK	PRBS_INV	LAC	AISE	ATAO
0B,4B,8B,CB	MAINT1		-	-	-	-	ARLP	RLP	ALP	DLP
0C,4C,8C,CC	MAINT2	R/W	-	-	TIBLB_L1	TIBLB_L0	RIBLBA_L1	RIBLBA_L0	RIBLBD_L1	RIBLBD_L0
0D,4D,8D,CD	MAINT3	R/W	TIBLB7	TIBLB6	TIBLB5	TIBLB4	TIBLB3	TIBLB2	TIBLB1	TIBLB0
0E,4E,8E,CE	MAINT4	R/W	RIBLBA7	RIBLBA6	RIBLBA5	RIBLBA4	RIBLBA3	RIBLBA2	RIBLBA1	RIBLBA0
0F,4F,8F,CF	MAINT5	R/W	RIBLBD7	RIBLBD6	RIBLBD5	RIBLBD4	RIBLBD3	RIBLBD2	RIBLBD1	RIBLBD0
10,50,90,D0	MAINT6	R/W	-	BPV_INS	ERR_INS	EXZ_DEF	ERR_SEL1	ERR_SEL0	CNT_MD	CNT_TRF
Interrupt Control Registers										
11,51,91,D1	INTM0	R/W	-	IBLBA_IM	IBLBD_IM	PRBS_IM	TCLK_IM	DF_IM	AIS_IM	LOS_IM
12,52,92,D2	INTM1	R/W	DAC_OV_IM	JAOV_IM	JAUD_IM	ERR_IM	EXZ_IM	CV_IM	TIMER_IM	CNT_IM
13,53,93,D3	INTES	R/W	-	IBLBA_IES	IBLBD_IES	PRBS_IES	TCLK_IES	DF_IES	AIS_IES	LOS_IES
Line Status Registers										
14,54,94,D4	STAT0	R	-	IBLBA_S	IBLBD_S	PRBS_S	TCLK_LOS	DF_S	AIS_S	LOS_S
15,55,95,D5	STAT1	R	-	-	RLP_S	-	-	-	-	-
Interrupt Status Registers										
16,56,96,D6	INTS0	R	-	IBLBA_IS	IBLBD_IS	PRBS_IS	TCLK_LOS_IS	DF_IS	AIS_IS	LOS_IS
17,57,97,D7	INTS1	R	DAC_OV_IS	JAOV_IS	JAUD_IS	ERR_IS	EXZ_IS	CV_IS	TMOV_IS	CNT_OV_IS
Counter Registers										
18,58,98,D8	CNT0	R	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
19,59,99,D9	CNT1	R	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8
Transmit and Receive Termination Registers										
1A,5A,9A,DA	TERM	R/W	-	-	T_TERM2	T_TERM1	T_TERM0	R_TERM2	R_TERM1	R_TERM0

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4.2 REGISTER DESCRIPTION

4.2.1 GLOBAL REGISTERS

Table-21 ID: Chip Revision Register

(R, Address = 00H)

Symbol	Bit	Default	Description
ID[7:0]	7-0	01H	00H is for the first version.

Table-22 RST: Reset Register

(W, Address = 20H)

Symbol	Bit	Default	Description
RST[7:0]	7-0	01H	Software reset. A write operation on this register will reset all internal registers to their default values, and the status of all ports are set to the default status. The content in this register can not be changed.

Table-23 GCF0: Global Configuration Register 0

(R/W, Address = 40H)

Symbol	Bit	Default	Description
-	7-6	0	Reserved
-	5	0	Reserved. For normal operation, this bit should be set to '0'.
T1E1	4	0	This bit selects E1 or T1/J1 operation mode globally. = 0: E1 mode is selected. = 1: T1/J1 mode is selected.
COPY	3	0	Enable broadcasting mode. = 0: Broadcasting mode disabled = 1: Broadcasting mode enabled. Writing operation on one channel's register will be copied exactly to the corresponding registers in all the other channels.
INTM_GLB	2	1	Global interrupt enable = 0: Interrupt is globally enabled. But for each individual interrupt, it still can be disabled by its corresponding Interrupt mask Bit. = 1: All the interrupts are disabled for all channels.
INT_PIN[1:0]	1-0	00	Interrupt pin operation mode selection = x0: open drain, active low (with an external pull-up resistor) = 01: push-pull, active low = 11: push-pull, active high

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Table-24 GCF1: Global Configuration Register 1
(R/W, Address = 60H)

Symbol	Bit	Default	Description
MON[3:0]	7-4	0000	MON selects the transmitter or receiver channel to be monitored. = 0000: receiver 1 is in normal operation without monitoring = 0001: reserved = 0010: monitor receiver 2 = 0011: reserved = 0100: monitor receiver 3 = 0101: reserved = 0110: monitor receiver 4 = 0111: reserved = 1000: transmitter 1 is in normal operation without monitoring = 1001: reserved = 1010: monitor transmitter 2 = 1011: reserved = 1100: monitor transmitter 3 = 1101: reserved = 1110: monitor transmitter 4 = 1111: reserved
-	3-0	0000	Reserved

Table-25 INTCH: Interrupt Channel Indication Register
(R, Address = 80H)

Symbol	Bit	Default	Description
INT_CH[7:0]	7-0	00H	INT_CH[0, 2, 4 or 6]=1 indicates that an interrupt was generated by channel 1, 2, 3 or 4 respectively.

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4.2.2 JITTER ATTENUATION CONTROL REGISTER

Table-26 JACF: Jitter Attenuator Configuration Register

(R/W, Address = 01H,41H,81H,C1H)

Symbol	Bit	Default	Description		
-	7-6	00	Reserved		
JA_LIMIT	5	0	Wide Jitter Attenuation bandwidth = 0: normal mode = 1: JA limit mode		
JACF[1:0]	4-3	00	Jitter Attenuator configuration = 00/10: JA not used = 01: JA in transmit path = 11: JA in receive path		
JADP[1:0]	2-1	00	Jitter Attenuator depth selection = 00: 128 bits = 01: 64 bits = 10/11: 32 bits		
JABW	0	0	Jitter transfer function bandwidth selection		
			JABW	T1/J1	E1
			0	5 Hz	6.8 Hz
			1	1.25 Hz	0.9 Hz

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4.2.3 TRANSMIT PATH CONTROL REGISTERS

Table-27 TCF0: Transmitter Configuration Register 0

(R/W, Address = 02H,42H,82H,C2H)

Symbol	Bit	Default	Description
-	7-5	000	Reserved
T_OFF	4	0	Transmitter power down enable = 0: Transmitter power up = 1: Transmitter power down and line driver high impedance
TD_INV	3	0	Transmit data invert = 0: data on TDn or TDPn/TDNn is active high = 1: data on TDn or TDPn/TDNn is active low
TCLK_SEL	2	0	Transmit clock edge select = 0: data on TDn or TDPn/TDNn is sampled on the falling edges of TCLKn = 1: data on TDn or TDPn/TDNn is sampled on the rising edges of TCLKn
T_MD[1:0]	1-0	00	Transmitter operation mode control bits which select different stages of transmit data path = 00: enable HDB3/B8ZS encoder and waveform shaper blocks, input on TDn is single rail NRZ data = 01: enable AMI encoder and waveform shaper blocks, input on pin TDn is single rail NRZ data = 1x: encoder is bypassed, dual rail NRZ transmit data input on pin TDPn/TDNn

Table-28 TCF1: Transmitter Configuration Register 1

(R/W, Address = 03H,43H,83H,C3H)

<table>
<tr><th>Symbol</th><th>Bit</th><th>Default</th><th colspan="6">Description</th></tr>
<tr><td>-</td><td>7-6</td><td>00</td><td colspan="6">Reserved. This bit should be ‘0’ for normal operation.</td></tr>
<tr><td>DFM_OFF</td><td>5</td><td>0</td><td colspan="6">Transmit driver failure monitor disable
= 0: DFM is enabled
= 1: DFM is disabled</td></tr>
<tr><td>THZ</td><td>4</td><td>1</td><td colspan="6">Transmit line driver high impedance enable
= 0: normal state
= 1: transmit line driver high impedance enable (other transmit path still in normal state)</td></tr>
<tr><td rowspan="11">PULS[3:0]</td><td rowspan="11">3-0</td><td rowspan="11">0000</td><td colspan="6">These bits select the transmit template.</td></tr>
<tr><td></td><td>T1/E1/J1</td><td>TCLK</td><td>Cable Impedance</td><td>Cable Range</td><td>Cable Loss</td></tr>
<tr><td>0000[1]</td><td>E1</td><td>2.048 MHz</td><td>75 Ω</td><td>-</td><td>0~24 dB</td></tr>
<tr><td>0001</td><td>E1</td><td>2.048 MHz</td><td>120 Ω</td><td>-</td><td>0~24 dB</td></tr>
<tr><td>0010</td><td>DSX1</td><td>1.544 MHz</td><td>100 Ω</td><td>0~133 ft</td><td>0~0.6 dB</td></tr>
<tr><td>0011</td><td>DSX1</td><td>1.544 MHz</td><td>100 Ω</td><td>133~266 ft</td><td>0.6~1.2 dB</td></tr>
<tr><td>0100</td><td>DSX1</td><td>1.544 MHz</td><td>100 Ω</td><td>266~399 ft</td><td>1.2~1.8 dB</td></tr>
<tr><td>0101</td><td>DSX1</td><td>1.544 MHz</td><td>100 Ω</td><td>399~533 ft</td><td>1.8~2.4 dB</td></tr>
<tr><td>0110</td><td>DSX1</td><td>1.544 MHz</td><td>100 Ω</td><td>533~655 ft</td><td>2.4~3.0 dB</td></tr>
<tr><td>0111</td><td>J1</td><td>1.544 MHz</td><td>110 Ω</td><td>0~655 ft</td><td>0~3.0 dB</td></tr>
<tr><td>1000 - 1011</td><td colspan="5">Reserved</td></tr>
<tr><td>11xx</td><td colspan="5">User programmable waveform setting</td></tr>
</table>

1. In internal impedance matching mode, for E1/75 Ω cable impedance, the PULS[3:0] bits (**TCF1, 03H...**) should be set to ‘0000’. In external impedance matching mode, for E1/75 Ω cable impedance, the PULS[3:0] bits should be set to ‘0001’.

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Table-29 TCF2: Transmitter Configuration Register 2

(R/W, Address = 04H,44H,84H,C4H)

Symbol	Bit	Default	Description
-	7-6	00	Reserved
SCAL[5:0]	5-0	100001	SCAL specifies a scaling factor to be applied to the amplitude of the user-programmable arbitrary pulses which is to be transmitted if needed. The default value of SCAL[5:0] is '100001'. Refer to 3.2.3.2 User-Programmable Arbitrary Waveform. = 110110: default value for T1 0~133 ft, T1 133~266 ft, T1 266~399 ft, T1 399~533 ft, T1 533~655 ft, J1 0~655 ft. One step change of this value results in 2% scaling up/down against the pulse amplitude. = 100001: default value for E1 75 Ω and 120 Ω. One step change of this value results in 3% scaling up/down against the pulse amplitude.

Table-30 TCF3: Transmitter Configuration Register 3

(R/W, Address = 05H,45H,85H,C5H)

Symbol	Bit	Default	Description
DONE	7	0	After '1' is written to this bit, a read or write operation is implemented.
RW	6	0	This bit selects read or write operation = 0: write to RAM = 1: read from RAM
UI[1:0]	5-4	00	These bits specify the unit interval address. There are 4 unit intervals. = 00: UI address is 0 (The most left UI) = 01: UI address is 1 = 10: UI address is 2 = 11: UI address is 3
SAMP[3:0]	3-0	0000	These bits specify the sample address. Each UI has 16 samples. = 0000: sample address is 0 (The most left Sample) = 0001: sample address is 1 = 0010: sample address is 2 ..... = 1110: sample address is 14 = 1111: sample address is 15

Table-31 TCF4: Transmitter Configuration Register 4

(R/W, Address = 06H,46H,86H,C6H)

Symbol	Bit	Default	Description
-	7	0	Reserved
WDAT[6:0]	6-0	0000000	In Indirect Write operation, the WDAT[6:0] will be loaded to the pulse template RAM, specifying the amplitude of the Sample. After an Indirect Read operation, the amplitude data of the Sample in the pulse template RAM will be output to the WDAT[6:0].

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4.2.4 RECEIVE PATH CONTROL REGISTERS

Table-32 RCF0: Receiver Configuration Register 0

(R/W, Address = 07H,47H,87H,C7H)

Symbol	Bit	Default	Description
-	7-5	000	Reserved
R_OFF	4	0	Receiver power down enable = 0: Receiver power up = 1: Receiver power down
RD_INV	3	0	Receive data invert = 0: data on RDn or RDPn/RDNn is active high = 1: data on RDn or RDPn/RDNn is active low
RCLK_SEL	2	0	Receive clock edge select (this bit is ignored in slicer mode) = 0: data on RDn or RDPn/RDNn is updated on the rising edges of RCLKn = 1: data on RDn or RDPn/RDNn is updated on the falling edges of RCLKn
R_MD[1:0]	1-0	00	Receiver path decoding selection = 00: receive data is HDB3 (E1) / B8ZS (T1/J1) decoded and output on RDn with single rail NRZ format = 01: receive data is AMI decoded and output on RDn with single rail NRZ format = 10: decoder is bypassed, re-timed dual rail data with NRZ format output on RDPn/RDNn (dual rail mode with clock recovery) = 11: both CDR and decoder blocks are bypassed, slicer data with RZ format output on RDPn/RDNn (slicer mode)

Table-33 RCF1: Receiver Configuration Register 1

(R/W, Address = 08H,48H,88H,C8H)

Symbol	Bit	Default	Description		
-	7	0	Reserved		
EQ_ON	6	0	= 0: receive equalizer off = 1: receive equalizer on (LOS programming enabled)		
-	5	0	Reserved. Should be 0 for normal operation.		
LOS[4:0]	4-0	10101		LOS Clear Level (dB)	LOS Declare Level (dB)
			00000	0	<-4
			00001	>-2	<-6
			00010	>-4	<-8
			00011	>-6	<-10
			00100	>-8	<-12
			00101	>-10	<-14
			00110	>-12	<-16
			00111	>-14	<-18
			01000	>-16	<-20
			01001	>-18	<-22
			01010	>-20	<-24
			01011 - 11111	Reserved	

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Table-34 RCF2: Receiver Configuration Register 2

(R/W, Address =09H,49H,89H,C9H)

Symbol	Bit	Default	Description
-	7-6	00	Reserved
SLICE[1:0]	5-4	01	Receive slicer threshold = 00: The receive slicer generates a mark if the voltage on RTIPn/RRINGn exceeds 40% of the peak amplitude. = 01: The receive slicer generates a mark if the voltage on RTIPn/RRINGn exceeds 50% of the peak amplitude. = 10: The receive slicer generates a mark if the voltage on RTIPn/RRINGn exceeds 60% of the peak amplitude. = 11: The receive slicer generates a mark if the voltage on RTIPn/RRINGn exceeds 70% of the peak amplitude.
-	3-2	10	Reserved
MG[1:0]	1-0	00	Monitor gain setting: these bits select the internal linear gain boost = 00: 0 dB = 01: 22 dB = 10: 26 dB = 11: 32 dB

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4.2.5 NETWORK DIAGNOSTICS CONTROL REGISTERS

Table-35 MAINT0: Maintenance Function Control Register 0

(R/W, Address = 0AH,4AH,8AH,CAH)

Symbol	Bit	Default	Description
-	7	0	Reserved
PATT[1:0]	6-5	00	These bits select the internal pattern and insert it into the transmit data stream. = 00: normal operation (PATT_CLK = 0) / insert all zeros (PATT_CLK = 1) = 01: insert All Ones = 10: insert PRBS (E1: 2^{15}-1) or QRSS (T1/J1: 2^{20}-1) = 11: insert programmable Inband Loopback activate or deactivate code
PATT_CLK	4	0	Selects reference clock for transmitting internal pattern = 0: uses TCLKn as the reference clock = 1: uses MCLK as the reference clock
PRBS_INV	3	0	Inverts PRBS = 0: PRBS data is not inverted = 1: PRBS data is inverted before transmission and detection
LAC	2	0	The LOS/AIS criterion is selected as below: = 0: G.775 (E1) / T1.231 (T1/J1) = 1: ETSI 300233 & I.431 (E1) / I.431 (T1/J1)
AISE	1	0	AIS enable during LOS = 0: AIS insertion on RDPn/RDNn/RCLKn is disabled during LOS = 1: AIS insertion on RDPn/RDNn/RCLKn is enabled during LOS
ATAO	0	0	Automatically Transmit All Ones (enabled only when PATT[1:0] = 01) = 0: disabled = 1: Automatically Transmit All Ones pattern at TTIPn/TRINGn during LOS.

Table-36 MAINT1: Maintenance Function Control Register 1

(R/W, Address = 0BH,4BH,8BH,CBH)

Symbol	Bit	Default	Description
-	7-4	0000	Reserved
ARLP	3	0	Automatic Remote Loopback Control = 0: disables Automatic Remote Loopback (normal transmit and receive operation) = 1: enables Automatic Remote Loopback
RLP	2	0	Remote loopback enable = 0: disables remote loopback (normal transmit and receive operation) = 1: enables remote loopback
ALP	1	0	Analog loopback enable = 0: disables analog loopback (normal transmit and receive operation) = 1: enables analog loopback
DLP	0	0	Digital loopback enable = 0: disables digital loopback (normal transmit and receive operation) = 1: enables digital loopback

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Table-37 MAINT2: Maintenance Function Control Register 2

(R/W, Address = 0CH,4CH,8CH,CCH)

Symbol	Bit	Default	Description
-	7-6	00	Reserved.
TIBLB_L[1:0]	5-4	00	Defines the length of the user-programmable transmit Inband Loopback activate/deactivate code contained in TIBLB register. The default selection is 5 bits length. = 00: 5-bit activate code in TIBLB [4:0] = 01: 6-bit activate code in TIBLB [5:0] = 10: 7-bit activate code in TIBLB [6:0] = 11: 8-bit activate code in TIBLB [7:0]
RIBLBA_L[1:0]	3-2	00	Defines the length of the user-programmable receive Inband Loopback activate code contained in RIBLBA register. = 00: 5-bit activate code in RIBLBA [4:0] = 01: 6-bit activate code in RIBLBA [5:0] = 10: 7-bit activate code in RIBLBA [6:0] = 11: 8-bit activate code in RIBLBA [7:0]
RIBLBD_L[1:0]	1-0	01	Defines the length of the user-programmable receive Inband Loopback deactivate code contained in RIBLBD register. = 00: 5-bit deactivate code in RIBLBD [4:0] = 01: 6-bit deactivate code in RIBLBD [5:0] = 10: 7-bit deactivate code in RIBLBD [6:0] = 11: 8-bit deactivate code in RIBLBD [7:0]

Table-38 MAINT3: Maintenance Function Control Register 3

(R/W, Address = 0DH,4DH,8DH,CDH)

Symbol	Bit	Default	Description
TIBLB[7:0]	7-0	(000)00001	Defines the user-programmable transmit Inband Loopback activate/deactivate code. The default selection is 00001. TIBLB[7:0] form the 8-bit repeating code TIBLB[6:0] form the 7-bit repeating code TIBLB[5:0] form the 6-bit repeating code TIBLB[4:0] form the 5-bit repeating code

Table-39 MAINT4: Maintenance Function Control Register 4

(R/W, Address = 0EH,4EH,8EH,CEH)

Symbol	Bit	Default	Description
RIBLBA[7:0]	7-0	(000)00001	Defines the user-programmable receive Inband Loopback activate code. The default selection is 00001. RIBLBA[7:0] form the 8-bit repeating code RIBLBA[6:0] form the 7-bit repeating code RIBLBA[5:0] form the 6-bit repeating code RIBLBA[4:0] form the 5-bit repeating code

Table-40 MAINT5: Maintenance Function Control Register 5

(R/W, Address = 0FH,4FH,8FH,CFH)

Symbol	Bit	Default	Description
RIBLBD[7:0]	7-0	(00)001001	Defines the user-programmable receive Inband Loopback deactivate code. The default selection is 001001. RIBLBD[7:0] form the 8-bit repeating code RIBLBD[6:0] form the 7-bit repeating code RIBLBD[5:0] form the 6-bit repeating code RIBLBD[4:0] form the 5-bit repeating code

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Table-41 MAINT6: Maintenance Function Control Register 6

(R/W, Address = 10H,50H,90H,D0H)

Symbol	Bit	Default	Description
-	7	0	Reserved.
BPV_INS	6	0	BPV error insertion A '0' to '1' transition on this bit will cause a single bipolar violation error to be inserted into the transmit data stream. This bit must be cleared and set again for a subsequent error to be inserted.
ERR_INS	5	0	PRBS/QRSS logic error insertion A '0' to '1' transition on this bit will cause a single PRBS/QRSS logic error to be inserted into the transmit PRBS/QRSS data stream. This bit must be cleared and set again for subsequent error to be inserted.
EXZ_DEF	4	0	EXZ definition select = 0: ANSI = 1: FCC
ERR_SEL	3-2	00	These bits choose which type of error will be counted = 00: the PRBS logic error is counted by a 16-bit error counter. = 01: the EXZ error is counted by a 16-bit error counter. = 10: the Received CV (BPV) error is counted by a 16-bit error counter. = 11: both CV (BPV) and EXZ errors are counted by a 16-bit error counter.
CNT_MD	1	0	Counter operation mode select = 0: Manual Report Mode = 1: Auto Report Mode
CNT_TRF	0	0	= 0: Clear this bit for the next '0' to '1' transition on this bit. = 1: Error counting result is transferred to CNT0 and CNT1 and the error counter is reset.

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4.2.6 INTERRUPT CONTROL REGISTERS

Table-42 INTM0: Interrupt Mask Register 0

(R/W, Address = 11H,51H,91H,D1H)

Symbol	Bit	Default	Description
-	7	-	Reserved
IBLBA_IM	6	1	In-band Loopback activate code detect interrupt mask = 0: In-band Loopback activate code detect interrupt enabled = 1: In-band Loopback activate code detect interrupt masked
IBLBD_IM	5	1	In-band Loopback deactivate code detect interrupt mask = 0: In-band Loopback deactivate code detect interrupt enabled = 1: In-band Loopback deactivate code detect interrupt masked
PRBS_IM	4	1	PRBS synchronic signal detect interrupt mask = 0: PRBS synchronic signal detect interrupt enabled = 1: PRBS synchronic signal detect interrupt masked
TCLK_IM	3	1	TCLK loss detect interrupt mask = 0: TCLK loss detect interrupt enabled = 1: TCLK loss detect interrupt masked
DF_IM	2	1	Driver failure interrupt mask = 0: Driver failure interrupt enabled = 1: Driver failure interrupt masked
AIS_IM	1	1	Alarm Indication Signal interrupt mask = 0: Alarm Indication Signal interrupt enabled = 1: Alarm Indication Signal interrupt masked
LOS_IM	0	1	Loss Of Signal interrupt mask = 0: Loss Of Signal interrupt enabled = 1: Loss Of Signal interrupt masked

Table-43 INTM1: Interrupt Mask Register 1

(R/W, Address = 12H,52H,92H,D2H)

Symbol	Bit	Default	Description
DAC_OV_IM	7	1	DAC arithmetic overflow interrupt mask = 0: DAC arithmetic overflow interrupt enabled = 1: DAC arithmetic overflow interrupt masked
JAOV_IM	6	1	JA overflow interrupt mask = 0: JA overflow interrupt enabled = 1: JA overflow interrupt masked
JAUD_IM	5	1	JA underflow interrupt mask = 0: JA underflow interrupt enabled = 1: JA underflow interrupt masked
ERR_IM	4	1	PRBS/QRSS logic error detect interrupt mask = 0: PRBS/QRSS logic error detect interrupt enabled = 1: PRBS/QRSS logic error detect interrupt masked
EXZ_IM	3	1	Receive excess zeros interrupt mask = 0: Receive excess zeros interrupt enabled = 1: Receive excess zeros interrupt masked
CV_IM	2	1	Receive error interrupt mask = 0: Receive error interrupt enabled = 1: Receive error interrupt masked
TIMER_IM	1	1	One-Second Timer expiration interrupt mask = 0: One-Second Timer expiration interrupt enabled = 1: One-Second Timer expiration interrupt masked
CNT_IM	0	1	Counter overflow interrupt mask = 0: Counter overflow interrupt enabled = 1: Counter overflow interrupt masked

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Table-44 INTES: Interrupt Trigger Edges Select Register

(R/W, Address = 13H, 53H,93H,D3H)

Symbol	Bit	Default	Description
-	7	-	Reserved
IBLBA_IES	6	0	This bit determines the Inband Loopback Activate Code interrupt event. = 0: interrupt event is defined as a '0' to '1' transition of the IBLBA_S bit in the STAT0 status register = 1: interrupt event is defined as either a '0' to '1' transition or a '1' to '0' transition of the IBLBA_S bit in the STAT0 status register.
IBLBD_IES	5	0	This bit determines the Inband Loopback Deactivate Code interrupt event. = 0: interrupt event is defined as a '0' to '1' transition of the IBLBD_S bit in the STAT0 status register = 1: interrupt event is defined as either a '0' to '1' transition or a '1' to '0' transition of the IBLBD_S bit in the STAT0 status register.
PRBS_IES	4	0	This bit determines the PRBS/QRSS synchronization status interrupt event. = 0: interrupt event is defined as a '0' to '1' transition of the PRBS_S bit in the STAT0 status register = 1: interrupt event is defined as either a '0' to '1' transition or a '1' to '0' transition of the PRBS_S bit in the STAT0 status register.
TCLK_IES	3	0	This bit determines the TCLK Loss interrupt event. = 0: interrupt event is defined as a '0' to '1' transition of the TCLK_LOS bit in the STAT0 status register = 1: interrupt event is defined as either a '0' to '1' transition or a '1' to '0' transition of the TCLK_LOS bit in the STAT0 status register.
DF_IES	2	0	This bit determines the Driver Failure interrupt event. = 0: interrupt event is defined as a '0' to '1' transition of the DF_S bit in the STAT0 status register = 1: interrupt event is defined as either a '0' to '1' transition or a '1' to '0' transition of the DF_S bit in the STAT0 status register.
AIS_IES	1	0	This bit determines the AIS interrupt event. = 0: interrupt event is defined as a '0' to '1' transition of the AIS_S bit in the STAT0 status register = 1: interrupt event is defined as either a '0' to '1' transition or a '1' to '0' transition of the AIS_S bit in the STAT0 status register.
LOS_IES	0	0	This bit determines the LOS interrupt event. = 0: interrupt event is defined as a '0' to '1' transition of the LOS_S bit in the STAT0 status register = 1: interrupt event is defined as either a '0' to '1' transition or a '1' to '0' transition of the LOS_S bit in the STAT0 status register.

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4.2.7 LINE STATUS REGISTERS

Table-45 STAT0: Line Status Register 0 (real time status monitor)

(R, Address = 14H,54H,94H,D4H)

Symbol	Bit	Default	Description
-	7	-	Reserved
IBLBA_S	6	0	Inband Loopback activate code receive status indication = 0: no Inband Loopback activate code is detected = 1: activate code has been detected for more than t ms. Even there is bit error, this bit remains set as long as the bit error rate is less than 10^{-2}. Note1: Automatic remote loopback switching is disabled (ARLP = 0), t = 40 ms. If automatic remote loopback switching is enabled (ARLP = 1), t = 5.1 s. The rising edge of this bit activates the remote loopback operation in local end. Note2: If IBLBA_IM=0 and IBLBA_IES=0, a '0' to '1' transition on this bit will cause an activate code detect interrupt. If IBLBA_IM=0 and IBLBA_IES=1, any changes on this bit will cause an activate code detect interrupt.
IBLBD_S	5	0	Inband Loopback deactivate code receive status indication = 0: no Inband Loopback deactivate code is detected = 1: the Inband Loopback deactivate code has been detected for more than t. Even there is a bit error, this bit remains set as long as the bit error rate is less than 10^{-2}. Note1: Automatic remote loopback switching is disabled (ARLP = 0), t = 40 ms.If automatic remote loopback switching is enabled (ARLP = 1), t= 5.1 s. The rising edge of this bit disables the remote loopback operation. Note2: If IBLBD_IM=0 and IBLBD_IES=0, a '0' to '1' transition on this bit will cause a deactivate code detect interrupt. If IBLBD_IM=0 and IBLBD_IES=1, any changes on this bit will cause a deactivate code detect interrupt.
PRBS_S	4	0	Synchronous status indication of PRBS/QRSS (real time) = 0: 2^{15}-1 (E1) PRBS or 2^{20}-1 (T1/J1) QRSS is not detected = 1: 2^{15}-1 (E1) PRBS or 2^{20}-1 (T1/J1) QRSS is detected. Note: If PRBS_IM=0 and PRBS_IES=0, a '0' to '1' transition on this bit will cause a synchronous status detect interrupt. If PRBS_IM=0 and PRBS_IES=1, any changes on this bit will cause a synchronous status detect interrupt.
TCLK_LOS	3	0	TCLKn loss indication = 0: normal = 1: TCLKn pin has not toggled for more than 70 MCLK cycles. Note: If TCLK_IM=0 and TCLK_IES=0, a '0' to '1' transition on this bit will cause an interrupt. If TCLK_IM=0 and TCLK_IES=1, any changes on this bit will cause an interrupt.
DF_S	2	0	Line driver status indication = 0: normal operation = 1: line driver short circuit is detected. Note: If DF_IM=0 and DF_IES=0, a '0' to '1' transition on this bit will cause an interrupt. If DF_IM=0 and DF_IES=1, any changes on this bit will cause an interrupt.

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Table-45 STAT0: Line Status Register 0 (real time status monitor) (Continued)

(R, Address = 14H,54H,94H,D4H)

Symbol	Bit	Default	Description
AIS_S	1	0	Alarm Indication Signal status detection = 0: no AIS signal is detected in the receive path = 1: AIS signal is detected in the receive path Note: If AIS_IM=0 and AIS_IES=0, a '0' to '1' transition on this bit will cause an interrupt. If AIS_IM=0 and AIS_IES=1, any changes on this bit will cause an interrupt.
LOS_S	0	0	Loss of Signal status detection = 0: Loss of signal on RTIP/RRING is not detected = 1: Loss of signal on RTIP/RRING is detected Note: IF LOS_IM=0 and LOS_IES=0, a '0' to '1' transition on this bit will cause an interrupt. IF LOS_IM=0 and LOS_IES=1, any changes on this bit will cause an interrupt.

Table-46 STAT1: Line Status Register 1 (real time status monitor)

(R, Address = 15H, 55H,95H, D5H)

Symbol	Bit	Default	Description
-	7-6	00	Reserved
RLP_S	5	0	Indicating the status of Remote Loopback = 0: The remote loopback is inactive. = 1: The remote loopback is active (closed).
-	4-0	00000	Reserved

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4.2.8 INTERRUPT STATUS REGISTERS

Table-47 INTS0: Interrupt Status Register 0

(this register is reset after a read operation) (R, Address = 16H, 56H,96H, D6H)

Symbol	Bit	Default	Description
-	7	0	Reserved
IBLBA_IS	6	0	This bit indicates the occurrence of the Inband Loopback Activate Code interrupt event. = 0: no Inband Loopback Activate Code interrupt event occurred = 1: Inband Loopback Activate Code Interrupt event occurred
IBLBD_IS	5	0	This bit indicates the occurrence of the Inband Loopback Deactivate Code interrupt event. = 0: no Inband Loopback Deactivate Code interrupt event occurred = 1: interrupt event of the received inband loopback deactivate code occurred.
PRBS_IS	4	0	This bit indicates the occurrence of the interrupt event generated by the PRBS/QRSS synchronization status. = 0: no PRBS/QRSS synchronization status interrupt event occurred = 1: PRBS/QRSS synchronization status interrupt event occurred
TCLK_LOS_IS	3	0	This bit indicates the occurrence of the interrupt event generated by the TCLKn loss detection. = 0: no TCLKn loss interrupt event. = 1:TCLKn loss interrupt event occurred.
DF_IS	2	0	This bit indicates the occurrence of the interrupt event generated by the Driver Failure. = 0: no Driver Failure interrupt event occurred = 1: Driver Failure interrupt event occurred
AIS_IS	1	0	This bit indicates the occurrence of the AIS (Alarm Indication Signal) interrupt event. = 0: no AIS interrupt event occurred = 1: AIS interrupt event occurred
LOS_IS	0	0	This bit indicates the occurrence of the LOS (Loss of signal) interrupt event. = 0: no LOS interrupt event occurred = 1: LOS interrupt event occurred

Table-48 INTS1: Interrupt Status Register 1

(this register is reset and relevant interrupt request is cleared after a read) (R, Address = 17H, 57H,97H, D7H)

Symbol	Bit	Default	Description
DAC_OV_IS	7	0	This bit indicates the occurrence of the pulse amplitude overflow of Arbitrary Waveform Generator interrupt event. = 0: no pulse amplitude overflow of Arbitrary Waveform Generator interrupt event occurred = 1: the pulse amplitude overflow of Arbitrary Waveform Generator interrupt event occurred
JAOV_IS	6	0	This bit indicates the occurrence of the Jitter Attenuator Overflow interrupt event. = 0: no JA overflow interrupt event occurred = 1: A overflow interrupt event occurred
JAUD_IS	5	0	This bit indicates the occurrence of the Jitter Attenuator Underflow interrupt event. = 0: no JA underflow interrupt event occurred = 1: JA underflow interrupt event occurred
ERR_IS	4	0	This bit indicates the occurrence of the interrupt event generated by the detected PRBS/QRSS logic error. = 0: no PRBS/QRSS logic error interrupt event occurred = 1: PRBS/QRSS logic error interrupt event occurred
EXZ_IS	3	0	This bit indicates the occurrence of the Excessive Zeros interrupt event. = 0: no excessive zeros interrupt event occurred = 1: EXZ interrupt event occurred
CV_IS	2	0	This bit indicates the occurrence of the Code Violation interrupt event. = 0: no code violation interrupt event occurred = 1: code violation interrupt event occurred
TMOV_IS	1	0	This bit indicates the occurrence of the One-Second Timer Expiration interrupt event. = 0: no one-second timer expiration interrupt event occurred = 1: one-second timer expiration interrupt event occurred
CNT_OV_IS	0	0	This bit indicates the occurrence of the Counter Overflow interrupt event. = 0: no counter overflow interrupt event occurred = 1: counter overflow interrupt event occurred

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4.2.9 COUNTER REGISTERS

Table-49 CNT0: Error Counter L-byte Register 0

(R, Address = 18H, 58H,98H, D8H)

Symbol	Bit	Default	Description
CNT_L[7:0]	7-0	00H	This register contains the lower eight bits of the 16-bit error counter. CNT_L[0] is the LSB.

Table-50 CNT1: Error Counter H-byte Register 1

(R, Address = 19H, 59H,99H,D9H)

Symbol	Bit	Default	Description
CNT_H[7:0]	7-0	00H	This register contains the upper eight bits of the 16-bit error counter. CNT_H[7] is the MSB.

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4.2.10 TRANSMIT AND RECEIVE TERMINATION REGISTER

Table-51 TERM: Transmit and Receive Termination Configuration Register

(R/W, Address = 1AH, 5AH,9AH,DAH)

Symbol	Bit	Default	Description
-	7-6	00	Reserved
T_TERM[2:0]	5-3	000	These bits select the internal termination for transmit line impedance matching. = 000: internal 75 Ω impedance matching = 001: internal 120 Ω impedance matching = 010: internal 100 Ω impedance matching = 011: internal 110 Ω impedance matching =1xx: Selects external impedance matching resistors for E1 mode only. T1/J1 does not require external impedance resistors (see Table-10).
R_TERM[2:0]	2-0	000	These bits select the internal termination for receive line impedance matching. = 000: internal 75 Ω impedance matching = 001: internal 120 Ω impedance matching = 010: internal 100 Ω impedance matching = 011: internal 110 Ω impedance matching = 1xx: Selects external impedance matching resistors (see Table-11).

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5 IEEE STD 1149.1 JTAG TEST ACCESS PORT

The IDT82V2044E supports the digital Boundary Scan Specification as described in the IEEE 1149.1 standards.

The boundary scan architecture consists of data and instruction registers plus a Test Access Port (TAP) controller. Control of the TAP is performed through signals applied to the Test Mode Select (TMS) and Test Clock (TCK) pins. Data is shifted into the registers via the Test Data Input (TDI) pin, and shifted out of the registers via the Test Data Output (TDO) pin. Both TDI and TDO are clocked at a rate determined by TCK.

The JTAG boundary scan registers include BSR (Boundary Scan Register), IDR (Device Identification Register), BR (Bypass Register) and IR (Instruction Register). These will be described in the following pages. Refer to for architecture.

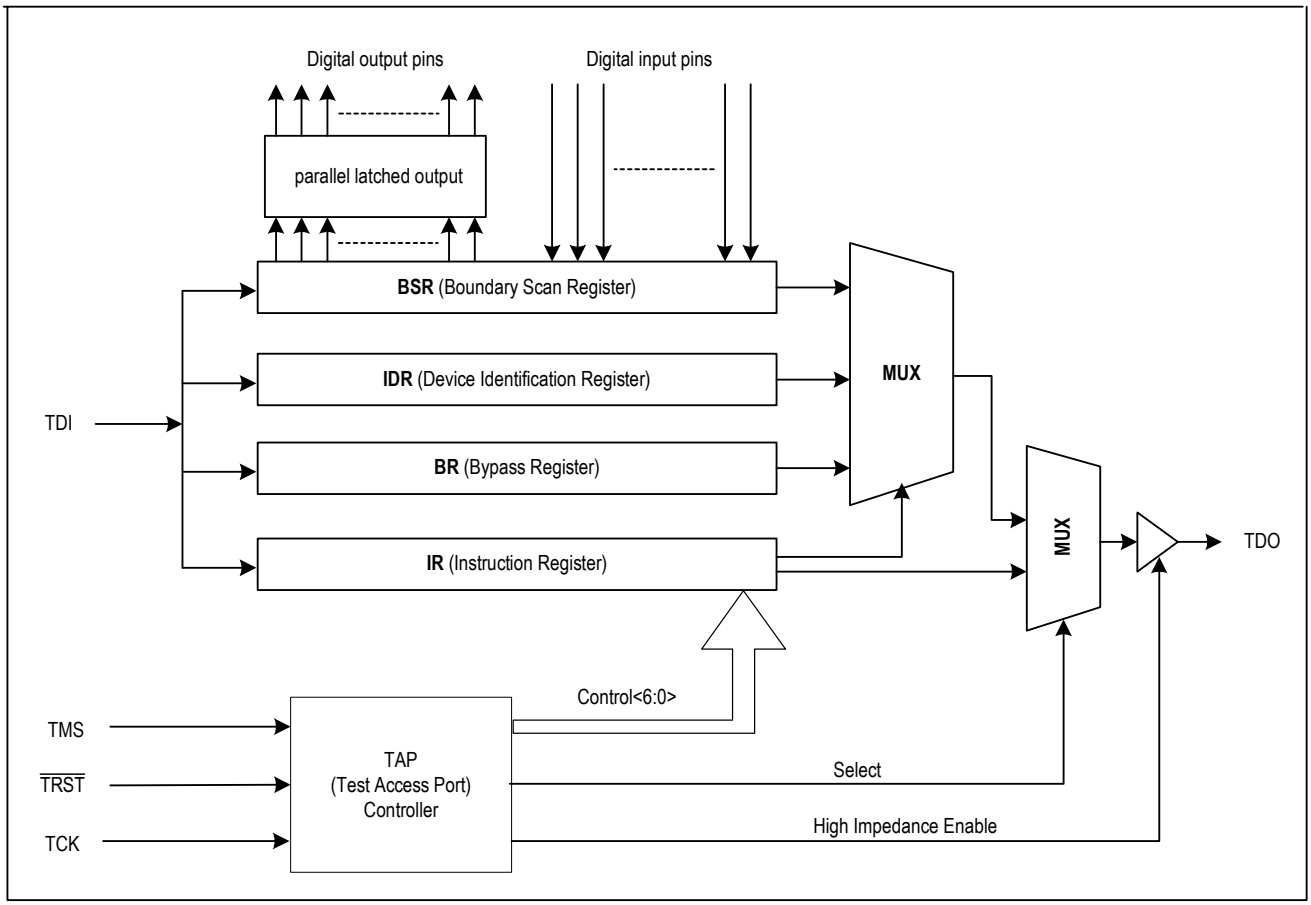


Figure-21 JTAG Architecture

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5.1 JTAG INSTRUCTIONS AND INSTRUCTION REGISTER

The IR (Instruction Register) with instruction decode block is used to select the test to be executed or the data register to be accessed or both.

The instructions are shifted in LSB first to this 3-bit register. See Table-52 for details of the codes and the instructions related.

Table-52 Instruction Register Description

IR CODE	INSTRUCTION	COMMENTS
000	Extest	The external test instruction allows testing of the interconnection to other devices. When the current instruction is the EXTEST instruction, the boundary scan register is placed between TDI and TDO. The signal on the input pins can be sampled by loading the boundary scan register using the Capture-DR state. The sampled values can then be viewed by shifting the boundary scan register using the Shift-DR state. The signal on the output pins can be controlled by loading patterns shifted in through input TDI into the boundary scan register using the Update-DR state.
100	Sample / Preload	The sample instruction samples all the device inputs and outputs. For this instruction, the boundary scan register is placed between TDI and TDO. The normal path between IDT82V2044E logic and the I/O pins is maintained. Primary device inputs and outputs can be sampled by loading the boundary scan register using the Capture-DR state. The sampled values can then be viewed by shifting the boundary scan register using the Shift-DR state.
110	Idcode	The identification instruction is used to connect the identification register between TDI and TDO. The device's identification code can then be shifted out using the Shift-DR state.
111	Bypass	The bypass instruction shifts data from input TDI to output TDO with one TCK clock period delay. The instruction is used to bypass the device.

5.2 JTAG DATA REGISTER

5.2.1 DEVICE IDENTIFICATION REGISTER (IDR)

The IDR can be set to define the producer number, part number and the device revision, which can be used to verify the proper version or revision number that has been used in the system under test. The IDR is 32 bits long and is partitioned as in Table-53. Data from the IDR is shifted out to TDO LSB first.

Table-53 Device Identification Register Description

Bit No.	Comments
0	Set to '1'
1-11	Producer Number
12-27	Part Number
28-31	Device Revision

5.2.2 BYPASS REGISTER (BR)

The BR consists of a single bit. It can provide a serial path between the TDI input and TDO output, bypassing the BSR to reduce test access times.

5.2.3 BOUNDARY SCAN REGISTER (BSR)

The BSR can apply and read test patterns in parallel to or from all the digital I/O pins. The BSR is a 98 bits long shift register and is initialized and read using the instruction EXTEST or SAMPLE/PRELOAD. Each pin is related to one or more bits in the BSR. For details, please refer to the BSDL file.

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5.2.4 TEST ACCESS PORT CONTROLLER

The TAP controller is a 16-state synchronous state machine. Figure-22 shows its state diagram following the description of each state. Note that the figure contains two main branches to access either the data or instruction registers. The value shown next to each state transition in this figure states the value present at TMS at each rising edge of TCK. Please refer to Table-54 for details of the state description.

Table-54 TAP Controller State Description

STATE	DESCRIPTION
Test Logic Reset	In this state, the test logic is disabled. The device is set to normal operation. During initialization, the device initializes the instruction register with the IDCODE instruction. Regardless of the original state of the controller, the controller enters the Test-Logic-Reset state when the TMS input is held high for at least 5 rising edges of TCK. The controller remains in this state while TMS is high. The device processor automatically enters this state at power-up.
Run-Test/Idle	This is a controller state between scan operations. Once in this state, the controller remains in the state as long as TMS is held low. The instruction register and all test data registers retain their previous state. When TMS is high and a rising edge is applied to TCK, the controller moves to the Select-DR state.
Select-DR-Scan	This is a temporary controller state and the instruction does not change in this state. The test data register selected by the current instruction retains its previous state. If TMS is held low and a rising edge is applied to TCK when in this state, the controller moves into the Capture-DR state and a scan sequence for the selected test data register is initiated. If TMS is held high and a rising edge applied to TCK, the controller moves to the Select-IR-Scan state.
Capture-DR	In this state, the Boundary Scan Register captures input pin data if the current instruction is EXTEST or SAMPLE/PRELOAD. The instruction does not change in this state. The other test data registers, which do not have parallel input, are not changed. When the TAP controller is in this state and a rising edge is applied to TCK, the controller enters the Exit1-DR state if TMS is high or the Shift-DR state if TMS is low.
Shift-DR	In this controller state, the test data register connected between TDI and TDO as a result of the current instruction shifts data on stage toward its serial output on each rising edge of TCK. The instruction does not change in this state. When the TAP controller is in this state and a rising edge is applied to TCK, the controller enters the Exit1-DR state if TMS is high or remains in the Shift-DR state if TMS is low.
Exit1-DR	This is a temporary state. While in this state, if TMS is held high, a rising edge applied to TCK causes the controller to enter the Update-DR state, which terminates the scanning process. If TMS is held low and a rising edge is applied to TCK, the controller enters the Pause-DR state. The test data register selected by the current instruction retains its previous value and the instruction does not change during this state.
Pause-DR	The pause state allows the test controller to temporarily halt the shifting of data through the test data register in the serial path between TDI and TDO. For example, this state could be used to allow the tester to reload its pin memory from disk during application of a long test sequence. The test data register selected by the current instruction retains its previous value and the instruction does not change during this state. The controller remains in this state as long as TMS is low. When TMS goes high and a rising edge is applied to TCK, the controller moves to the Exit2-DR state.
Exit2-DR	This is a temporary state. While in this state, if TMS is held high, a rising edge applied to TCK causes the controller to enter the Update-DR state, which terminates the scanning process. If TMS is held low and a rising edge is applied to TCK, the controller enters the Shift-DR state. The test data register selected by the current instruction retains its previous value and the instruction does not change during this state.
Update-DR	The Boundary Scan Register is provided with a latched parallel output to prevent changes while data is shifted in response to the EXTEST and SAMPLE/PRELOAD instructions. When the TAP controller is in this state and the Boundary Scan Register is selected, data is latched into the parallel output of this register from the shift-register path on the falling edge of TCK. The data held at the latched parallel output changes only in this state. All shift-register stages in the test data register selected by the current instruction retain their previous value and the instruction does not change during this state.
Select-IR-Scan	This is a temporary controller state. The test data register selected by the current instruction retains its previous state. If TMS is held low and a rising edge is applied to TCK when in this state, the controller moves into the Capture-IR state, and a scan sequence for the instruction register is initiated. If TMS is held high and a rising edge is applied to TCK, the controller moves to the Test-Logic-Reset state. The instruction does not change during this state.
Capture-IR	In this controller state, the shift register contained in the instruction register loads a fixed value of '100' on the rising edge of TCK. This supports fault-isolation of the board-level serial test data path. Data registers selected by the current instruction retain their value and the instruction does not change during this state. When the controller is in this state and a rising edge is applied to TCK, the controller enters the Exit1-IR state if TMS is held high, or the Shift-IR state if TMS is held low.
Shift-IR	In this state, the shift register contained in the instruction register is connected between TDI and TDO and shifts data one stage towards its serial output on each rising edge of TCK. The test data register selected by the current instruction retains its previous value and the instruction does not change during this state. When the controller is in this state and a rising edge is applied to TCK, the controller enters the Exit1-IR state if TMS is held high, or remains in the Shift-IR state if TMS is held low.
Exit1-IR	This is a temporary state. While in this state, if TMS is held high, a rising edge applied to TCK causes the controller to enter the Update-IR state, which terminates the scanning process. If TMS is held low and a rising edge is applied to TCK, the controller enters the Pause-IR state. The test data register selected by the current instruction retains its previous value and the instruction does not change during this state.

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Table-54 TAP Controller State Description (Continued)

STATE	DESCRIPTION
Pause-IR	The pause state allows the test controller to temporarily halt the shifting of data through the instruction register. The test data register selected by the current instruction retains its previous value and the instruction does not change during this state. The controller remains in this state as long as TMS is low. When TMS goes high and a rising edge is applied to TCK, the controller moves to the Exit2-IR state.
Exit2-IR	This is a temporary state. While in this state, if TMS is held high, a rising edge applied to TCK causes the controller to enter the Update-IR state, which terminates the scanning process. If TMS is held low and a rising edge is applied to TCK, the controller enters the Shift-IR state. The test data register selected by the current instruction retains its previous value and the instruction does not change during this state.
Update-IR	The instruction shifted into the instruction register is latched into the parallel output from the shift-register path on the falling edge of TCK. When the new instruction has been latched, it becomes the current instruction. The test data registers selected by the current instruction retain their previous value.

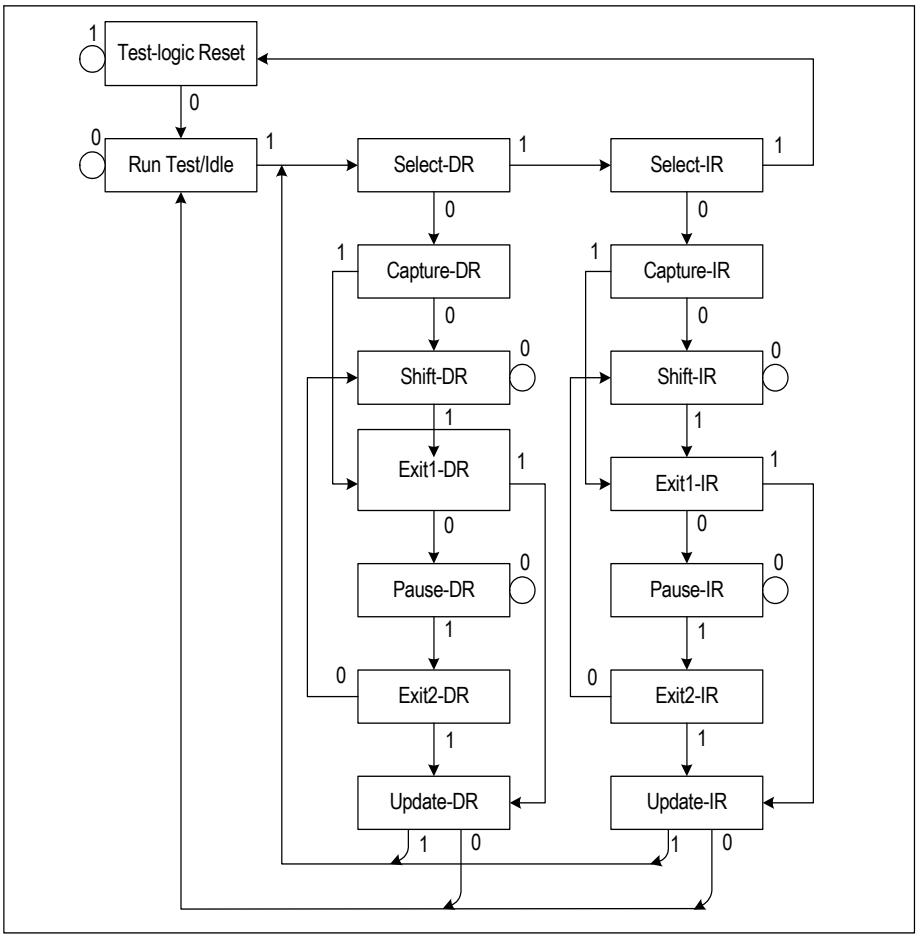


Figure-22 JTAG State Diagram

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6 TEST SPECIFICATIONS

Table-55 Absolute Maximum Rating

Symbol	Parameter	Min	Max	Unit
VDDA, VDDD	Core Power Supply	-0.5	4.6	V
VDDIO	I/O Power Supply	-0.5	4.6	V
VDDT1-4	Transmit Power Supply	-0.5	4.6	V
VDDR1-4	Receive Power Supply	-0.5	4.6	
Vin	Input Voltage, Any Digital Pin	GND-0.5	5.5	V
	Input Voltage, Any RTIP and RRING pin[1]	GND-0.5	VDDR+0.5	V
	ESD Voltage, any pin	2000 [2]		V
		500 [3]		V
Iin	Transient latch-up current, any pin		100	mA
	Input current, any digital pin [4]	-10	10	mA
	DC Input current, any analog pin [4]		±100	mA
Pd	Maximum power dissipation in package		1.69	W
Tc	Case Temperature		120	°C
Ts	Storage Temperature	-65	+150	°C
CAUTION Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.				

1.Reference to ground
2.Human body model
3.Charge device model
4.Constant input current

Table-56 Recommended Operation Conditions

Symbol	Parameter	Min	Typ	Max	Unit
VDDA,VDDD	Core Power Supply	3.13	3.3	3.47	V
VDDIO	I/O Power Supply	3.13	3.3	3.47	V
VDDT	Transmitter Power Supply	3.13	3.3	3.47	V
VDDR	Receive Power Supply	3.13	3.3	3.47	V
TA	Ambient operating temperature	-40	25	85	°C
Total current dissipation[1,2,3]	E1, 75 Ω Load				
	50% ones density data	-	250	270	mA
	100% ones density data	-	300	320	
	E1, 120 Ω Load				
	50% ones density data	-	240	260	mA
	100% ones density data	-	280	300	
	T1, 100 Ω Load				
	50% ones density data	-	270	290	mA
	100% ones density data	-	360	380	
	J1, 110 Ω Load				
	50% ones density data	-	230	250	mA
	100% ones density data	-	300	320	

1.Power consumption includes power consumption on device and load. Digital levels are 10% of the supply rails and digital outputs driving a 50 pF capacitive load.
2.Maximum power consumption over the full operating temperature and power supply voltage range.
3.Internal impedance matching, E1 75Ω power dissipation values are measured with template PULS[3:0] = 0000; E1 120Ω power dissipation values are measured with template PULS[3:0] = 0001; T1 power dissipation values are measured with template PULS[3:0] = 0110; J1 power dissipation values are measured with template PULS[3:0] = 0111.

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Table-57 Power Consumption

Symbol	Parameter	Min	Typ	Max[1,2]	Unit
	E1, 3.3 V, 75 Ω Load				
	50% ones density data:	-	830	-	mW
	100% ones density data:	-	990	1110	
	E1, 3.3 V, 120 Ω Load				
	50% ones density data:	-	790	-	mW
	100% ones density data:	-	920	1050	
	T1, 3.3 V, 100 Ω Load[3]				
	50% ones density data:	-	890	-	mW
	100% ones density data:	-	1190	1320	
	J1, 3.3 V, 110 Ω Load				
	50% ones density data:	-	760		mW
	100% ones density data:	-	990	1110	

1.Maximum power and current consumption over the full operating temperature and power supply voltage range. Includes all channels.
2.Power consumption includes power absorbed by line load and external transmitter components.
3.T1 is measured with maximum cable length.

Table-58 DC Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
V_{IL}	Input Low Level Voltage	-	-	0.8	V
V_{IH}	Input High Voltage	2.0	-	-	V
V_{OL}	Output Low level Voltage (Iout=1.6mA)	-	-	0.4	V
V_{OH}	Output High level Voltage (Iout=400μA)	2.4	-	VDDIO	V
V_{MA}	Analog Input Quiescent Voltage (RTIP, RRING pin while floating)		1.5		V
I_I	Input Leakage Current				
	TMS, TDI, $\overline{TRST}$			50	μA
	All other digital input pins	-10		10	μA
I_{ZL}	High Impedance Leakage Current	-10		10	μA
Ci	Input capacitance			15	pF
Co	Output load capacitance			50	pF
Co	Output load capacitance (bus pins)			100	pF

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Table-59 E1 Receiver Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test conditions
	Receiver sensitivity Adaptive Equalizer disabled: Adaptive Equalizer enabled:			 -10 -20	 dB	
	Analog LOS level Adaptive Equalizer disabled: Adaptive Equalizer enabled:	 -4	 800 	 -24	 mVp-p dB	A LOS level is programmable with Adaptive Equalizer enabled
	Allowable consecutive zeros before LOS G.775: I.431/ETSI300233:		 32 2048			
	LOS reset	12.5			% ones	G.775, ETSI 300 233
	Receive Intrinsic Jitter 20Hz - 100kHz			 0.05	 U.I.	 JA enabled
	Input Jitter Tolerance 1 Hz – 20 Hz 20 Hz – 2.4 KHz 18 KHz – 100 KHz	 37 5 2			 U.I. U.I. U.I.	G.823, with 6 dB cable attenuation
ZDM	Receiver Differential Input Impedance	20			KΩ	Internal mode
	Input termination resistor tolerance			±1%		
RRX	Receive Return Loss 51 KHz – 102 KHz 102 KHz - 2.048 MHz 2.048 MHz – 3.072 MHz	 20 20 20			 dB dB dB	G.703 Internal termination
RPD	Receive path delay Single rail Dual rail		 7 2		 U.I. U.I.	 JA disabled

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Table-60 T1/J1 Receiver Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test conditions
	Receiver sensitivity Adaptive Equalizer disabled: Adaptive Equalizer enabled:			 -10 -20	 dB	
	Analog LOS level Adaptive Equalizer disabled: Adaptive Equalizer enabled:	 -4	 800 	 -24	 mVp-p dB	 A LOS level is programmable with Adaptive Equalizer enabled
	Allowable consecutive zeros before LOS T1.231-1993 I.431		 175 1544			
	LOS reset	12.5			% ones	G.775, ETSI 300 233
	Receive Intrinsic Jitter 10 Hz – 8 KHz 10 Hz – 40 KHz 8 KHz – 40 KHz Wide band			 0.02 0.025 0.025 0.050	 U.I. U.I. U.I. U.I.	JA enabled (in receive path)
	Input Jitter Tolerance 0.1 Hz – 1 Hz 4.9 Hz – 300 Hz 10 KHz – 100 KHz	 138.0 28.0 0.4			 U.I. U.I. U.I.	AT&T62411
ZDM	Receiver Differential Input Impedance	20			KΩ	Internal mode
	Input termination resistor tolerance			±1%		
RRX	Receive Return Loss 39 KHz – 77 KHz 77 KHz - 1.544 MHz 1.544 MHz – 2.316 MHz	 20 20 20			 dB dB dB	 G.703 Internal termination
RPD	Receive path delay Single rail Dual rail		 7 2		 U.I. U.I.	JA disabled

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Table-61 E1 Transmitter Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
Vo-p	Output pulse amplitudes E1, 75Ω load E1, 120Ω load	 2.14 2.7	 2.37 3.0	 2.60 3.3	 V V
Vo-s	Zero (space) level E1, 75 Ω load E1, 120 Ω load	 -0.237 -0.3		 0.237 0.3	 V V
	Transmit amplitude variation with supply	-1		+1	%
	Difference between pulse sequences for 17 consecutive pulses (T1.102)			200	mV
Tpw	Output Pulse Width at 50% of nominal amplitude	232	244	256	ns
	Ratio of the amplitudes of Positive and Negative Pulses at the center of the pulse interval (G.703)	0.95		1.05	
	Ratio of the width of Positive and Negative Pulses at the center of the pulse interval (G.703)	0.95		1.05	
RTX	Transmit Return Loss (G.703)				
	51 KHz – 102 KHz 102 KHz - 2.048 MHz 2.048 MHz – 3.072 MHz		20 15 12		dB dB dB
JTXp-p	Intrinsic Transmit Jitter (TCLK is jitter free)				
	20 Hz – 100 KHz			0.050	U.I.
Td	Transmit path delay (JA is disabled)				
	Single rail Dual rail		8.5 4.5		U.I. U.I.
Isc	Line short circuit current		100		mA

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Table-62 T1/J1 Transmitter Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
Vo-p	Output pulse amplitudes	2.4	3.0	3.6	V
Vo-s	Zero (space) level	-0.15		0.15	V
	Transmit amplitude variation with supply	-1		+1	%
	Difference between pulse sequences for 17 consecutive pulses(T1.102)			200	mV
TPW	Output Pulse Width at 50% of nominal amplitude	338	350	362	ns
	Pulse width variation at the half amplitude (T1.102)			20	ns
	Imbalance between Positive and Negative Pulses amplitude (T1.102)	0.95		1.05	
	Output power level (T1.102) @772kHz @1544kHz (referenced to power at 772kHz)	 12.6 -29		17.9	 dBm dBm
RTX	Transmit Return Loss				
	39 KHz – 77 KHz 77 KHz – 1.544 MHz 1.544 MHz – 2.316 MHz		20 15 12		dB dB dB
JTXP-P	Intrinsic Transmit Jitter (TCLK is jitter free)				
	10 Hz – 8 KHz 8 KHz – 40 KHz 10 Hz – 40 KHz wide band			0.020 0.025 0.025 0.050	U.I.p-p U.I.p-p U.I.p-p U.I.p-p
Td	Transmit path delay (JA is disabled)				
	Single rail Dual rail		8.5 4.5		U.I. U.I.
I_{SC}	Line short circuit current		100		mA

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Table-63 Transmitter and Receiver Timing Characteristics

Symbol	Parameter		Min	Typ	Max	Unit
	MCLK frequency					
	E1: T1/J1:			2.048/49.152 1.544/37.056		MHz
	MCLK tolerance		-100		100	ppm
	MCLK duty cycle		30		70	%
Transmit path						
	TCLK frequency					
	E1: T1/J1:			2.048 1.544		MHz
	TCLK tolerance		-50		+50	ppm
	TCLK Duty Cycle		10		90	%
t1	Transmit Data Setup Time		40			ns
t2	Transmit Data Hold Time		40			ns
	Delay time of THZ low to driver high impedance				10	us
	Delay time of TCLK low to driver high impedance			75		U.I.
Receive path						
	Clock recovery capture range [1]	E1		± 80		ppm
		T1/J1		± 180		
	RCLK duty cycle [2]		40	50	60	%
t4	RCLK pulse width [2]					
	E1: T1/J1:		457 607	488 648	519 689	ns
t5	RCLK pulse width low time					
	E1: T1/J1:		203 259	244 324	285 389	ns
t6	RCLK pulse width high time					
	E1: T1/J1:		203 259	244 324	285 389	ns
	Rise/fall time [3]				20	ns
t7	Receive Data Setup Time					
	E1: T1/J1:		200 200	244 324		ns
t8	Receive Data Hold Time					
	E1: T1/J1:		200 200	244 324		ns

1.Relative to nominal frequency, MCLK= ± 100 ppm
2.RCLK duty cycle widths will vary depending on extent of received pulse jitter displacement. Maximum and minimum RCLK duty cycles are for worst case jitter conditions (0.2UI displacement for E1 per ITU G.823).
3.For all digital outputs. C load = 15pF

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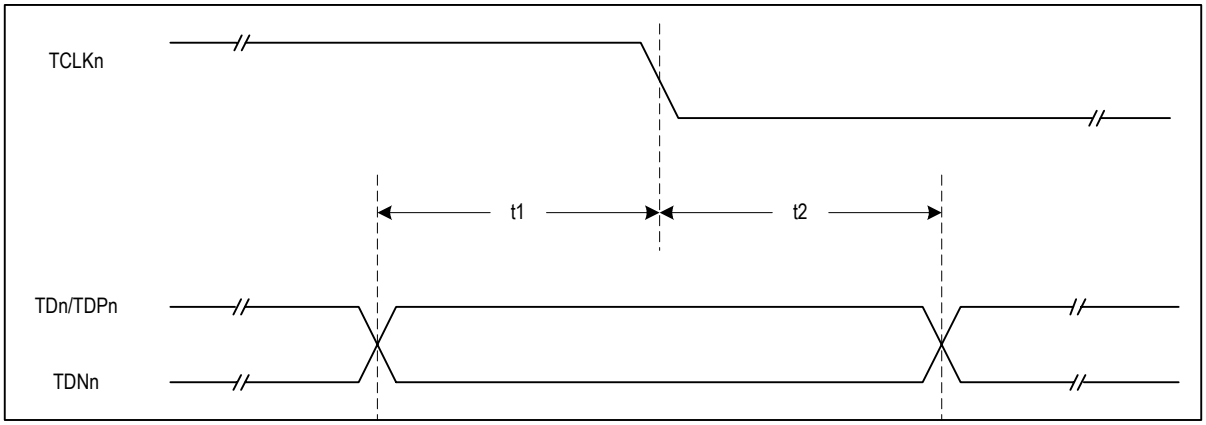


Figure-23 Transmit System Interface Timing

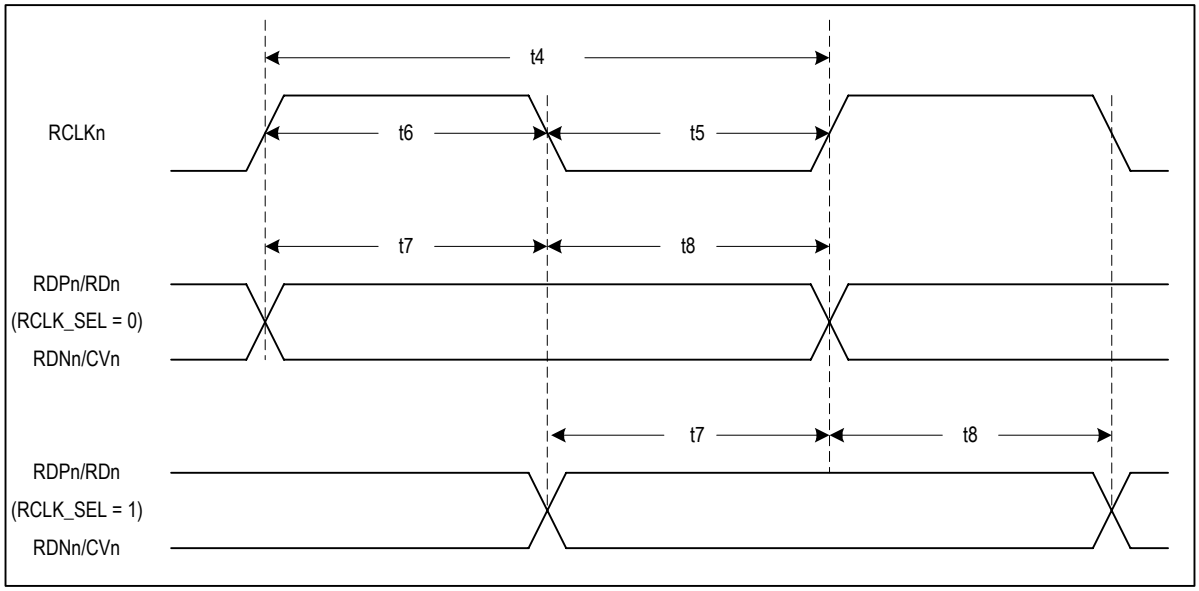


Figure-24 Receive System Interface Timing

Table-64 Jitter Tolerance

Jitter Tolerance	Min	Typ	Max	Unit	Standard
E1: 1 Hz 20 Hz – 2.4 KHz 18 KHz – 100 KHz	37 1.5 0.2			U.I. U.I. U.I.	G.823 Cable attenuation is 6dB
T1/J1: 1 Hz 4.9 Hz – 300 Hz 10 KHz – 100 KHz	138.0 28.0 0.4			U.I. U.I. U.I.	AT&T 62411

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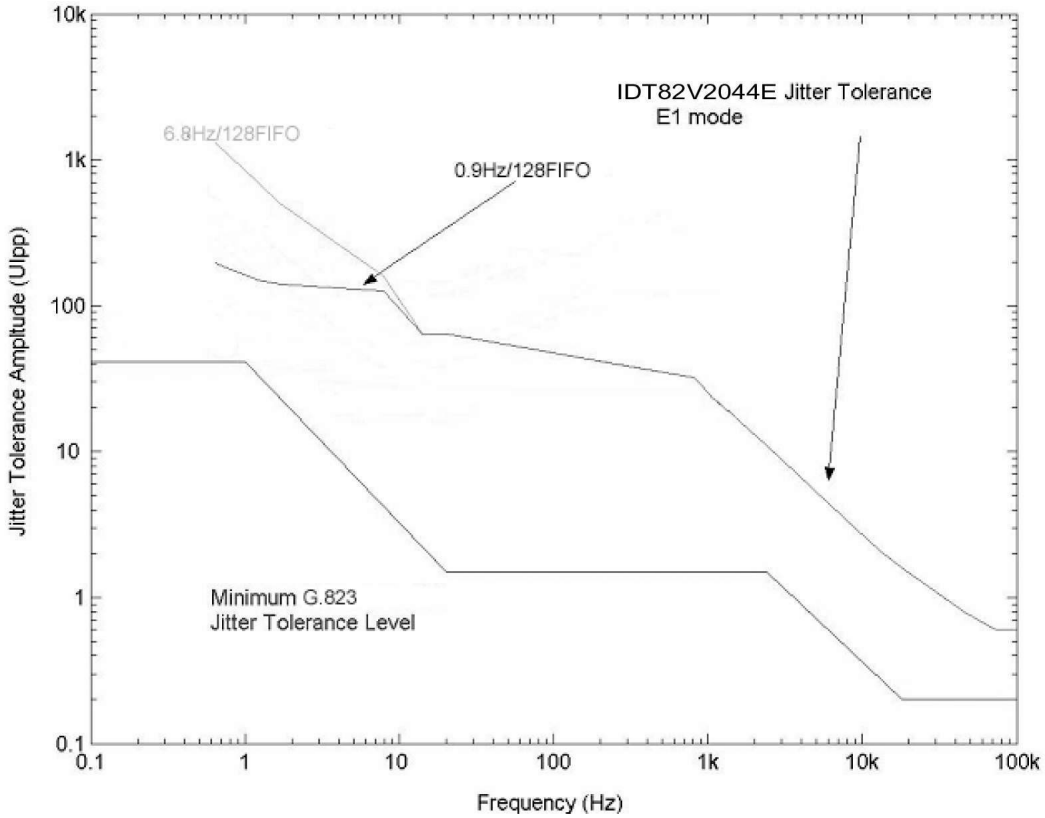


Figure-25 E1 Jitter Tolerance Performance

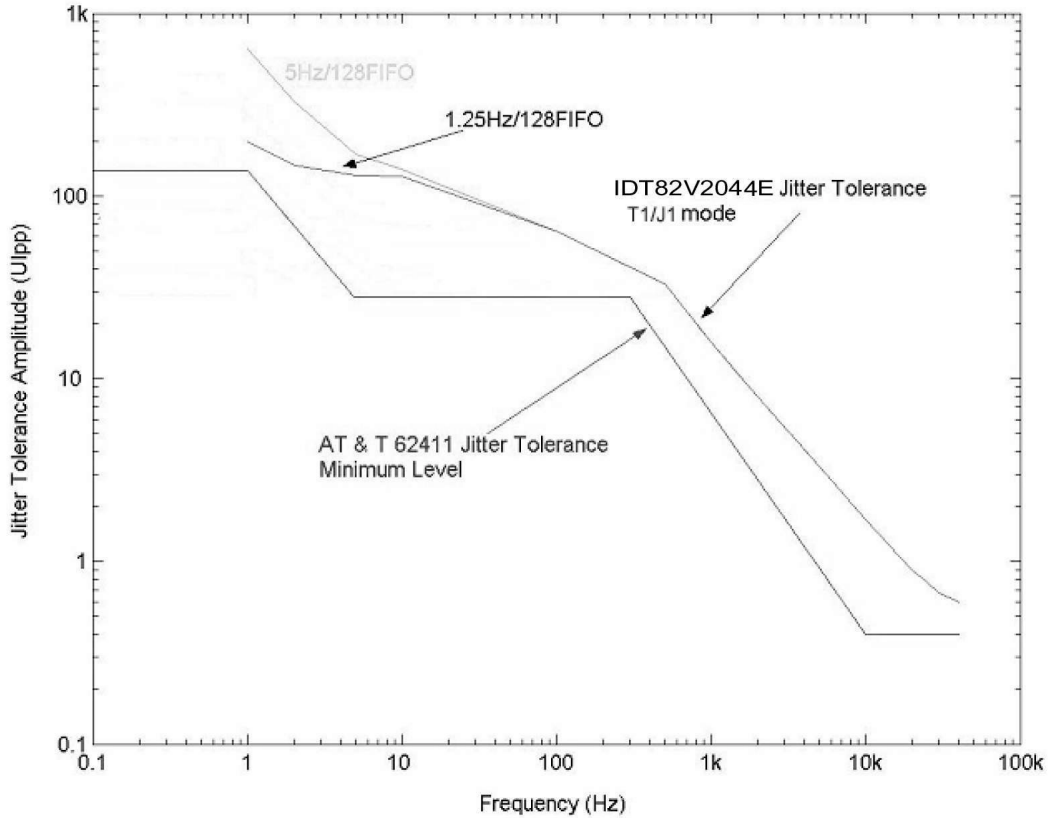


Figure-26 T1/J1 Jitter Tolerance Performance

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Table-65 Jitter Attenuator Characteristics

Parameter		Min	Typ	Max	Unit
Jitter Transfer Function Corner (-3dB) Frequency					
	E1, 32/64/128 bits FIFO JABW = 0: JABW = 1: T1/J1, 32/64/128 bits FIFO JABW = 0: JABW = 1:		 6.8 0.9 5 1.25		 Hz Hz Hz Hz
Jitter Attenuator					
E1: (G.736) @ 3 Hz @ 40 Hz @ 400 Hz @ 100 kHz		 -0.5 -0.5 +19.5 +19.5			 dB
T1/J1: (Per AT&T pub.62411) @ 1 Hz @ 20 Hz @ 1 kHz @ 1.4 kHz @ 70 kHz		 0 0 +33.3 40 40			
Jitter Attenuator Latency Delay					
32 bits FIFO: 64 bits FIFO: 128 bits FIFO:			16 32 64		U.I. U.I. U.I.
Input jitter tolerance before FIFO overflow or underflow 32 bits FIFO: 64 bits FIFO: 128 bits FIFO:			 28 58 120		 U.I. U.I. U.I.

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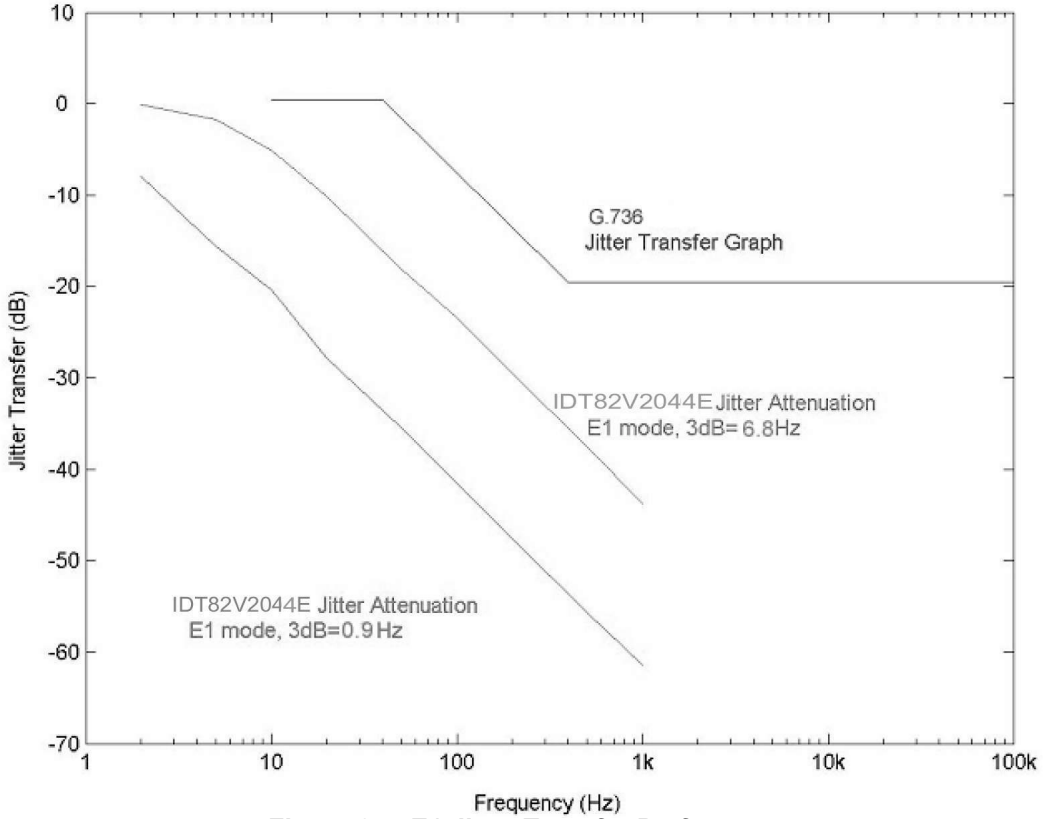


Figure-27 E1 Jitter Transfer Performance

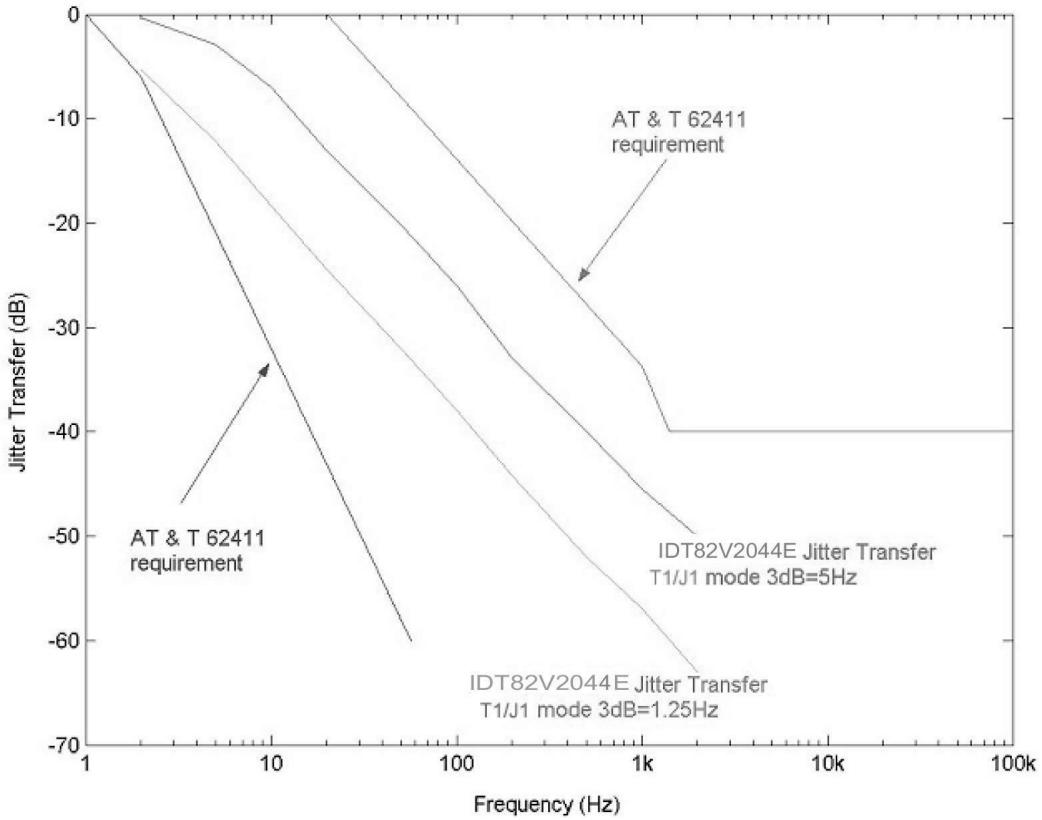


Figure-28 T1/J1 Jitter Transfer Performance

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Table-66 JTAG Timing Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
t1	TCK Period	100			ns
t2	TMS to TCK Setup Time TDI to TCK Setup Time	25			ns
t3	TCK to TMS Hold Time TCK to TDI Hold Time	25			ns
t4	TCK to TDO Delay Time			50	ns

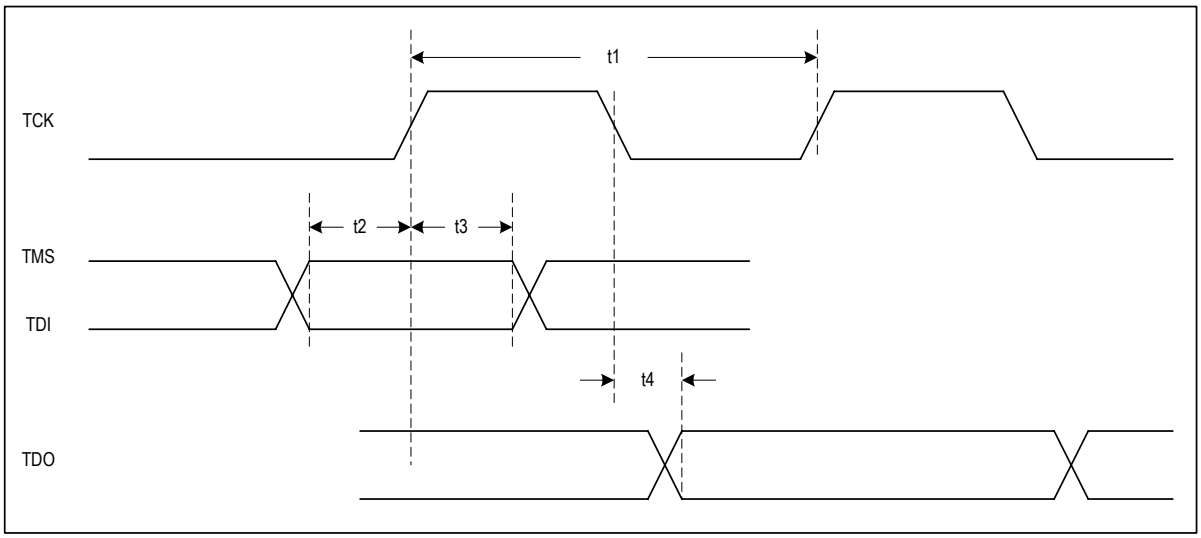


Figure-29 JTAG Interface Timing

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7 MICROCONTROLLER INTERFACE TIMING CHARACTERISTICS

7.1 SERIAL INTERFACE TIMING

Table-67 Serial Interface Timing Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Comments
t1	SCLK High Time	82			ns	
t2	SCLK Low Time	82			ns	
t3	Active $\overline{CS}$ to SCLK Setup Time	5			ns	
t4	Last SCLK Hold Time to Inactive $\overline{CS}$ Time	41			ns	
t5	$\overline{CS}$ Idle Time	41			ns	
t6	SDI to SCLK Setup Time	0			ns	
t7	SCLK to SDI Hold Time	62			ns	
t10	SCLK to SDO Valid Delay Time			75	ns	
t11	Inactive $\overline{CS}$ to SDO High Impedance Hold Time			70	ns	

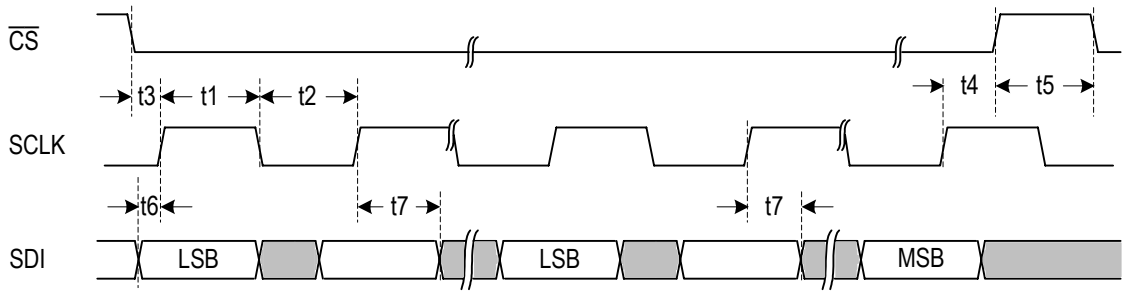


Figure-30 Serial Interface Write Timing

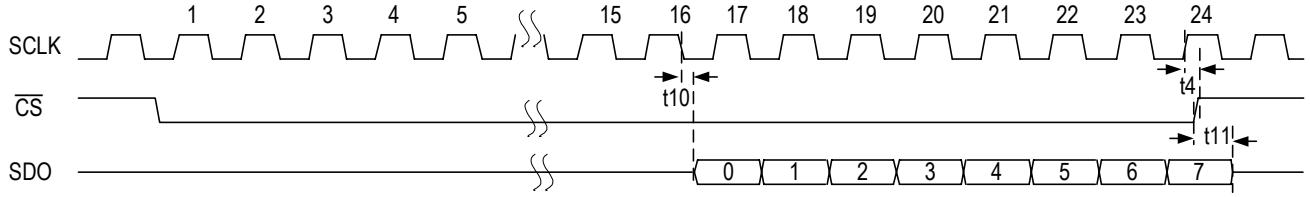


Figure-31 Serial Interface Read Timing with SCLKE=1

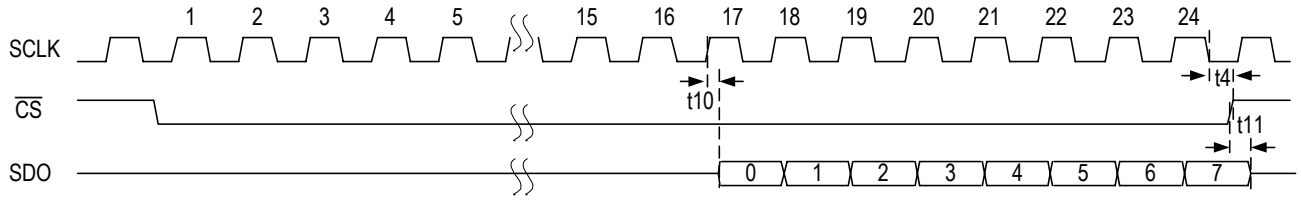


Figure-32 Serial Interface Read Timing with SCLKE=0

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7.2 PARALLEL INTERFACE TIMING

Table-68 Non_multiplexed Motorola Read Timing Characteristics

Symbol	Parameter	Min	Max	Unit
tRC	Read Cycle Time	190		ns
tDW	Valid $\overline{DS}$ Width	180		ns
tRWV	Delay from $\overline{DS}$ to Valid Read Signal		15	ns
tRWH	R/$\overline{W}$ to $\overline{DS}$ Hold Time	65		ns
tAV	Delay from $\overline{DS}$ to Valid Address		15	ns
tADH	Address to $\overline{DS}$ Hold Time	65		ns
tPRD	$\overline{DS}$ to Valid Read Data Propagation Delay		175	ns
tDAZ	Delay from $\overline{DS}$ inactive to data bus High Impedance	5	20	ns
tRecovery	Recovery Time from Read Cycle	5		ns

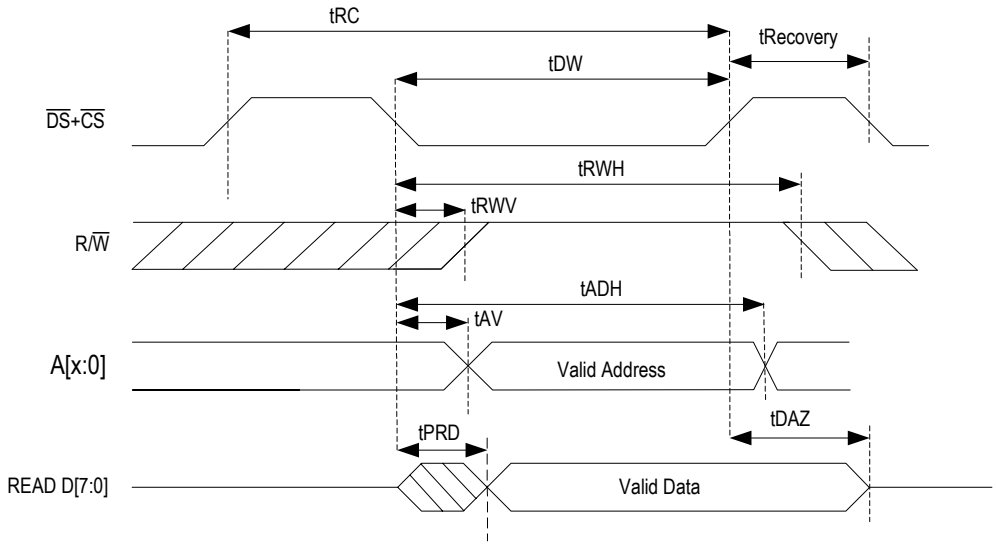


Figure-33 Non_multiplexed Motorola Read Timing

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Table-69 Non_multiplexed Motorola Write Timing Characteristics

Symbol	Parameter	Min	Max	Unit
tWC	Write Cycle Time	120		ns
tDW	Valid $\overline{DS}$ Width	100		ns
tRWV	Delay from $\overline{DS}$ to Valid Write Signal		15	ns
tRWH	R/$\overline{W}$ to $\overline{DS}$ Hold Time	65		ns
tAV	Delay from $\overline{DS}$ to Valid Address		15	ns
tAH	Address to $\overline{DS}$ Hold Time	65		ns
tDV	Delay from $\overline{DS}$ to Valid Write Data		15	ns
tDHW	Write Data to $\overline{DS}$ Hold Time	65		ns
tRecovery	Recovery Time from Write Cycle	5		ns

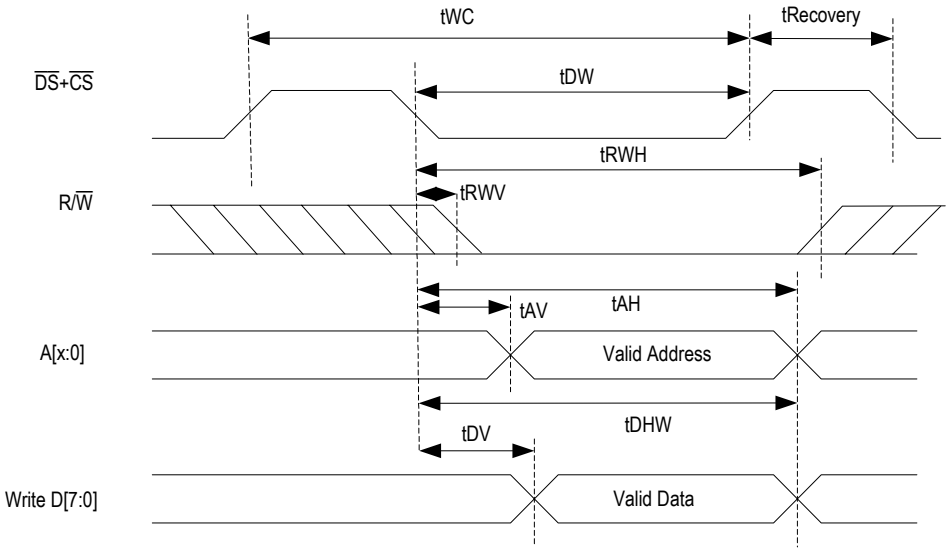
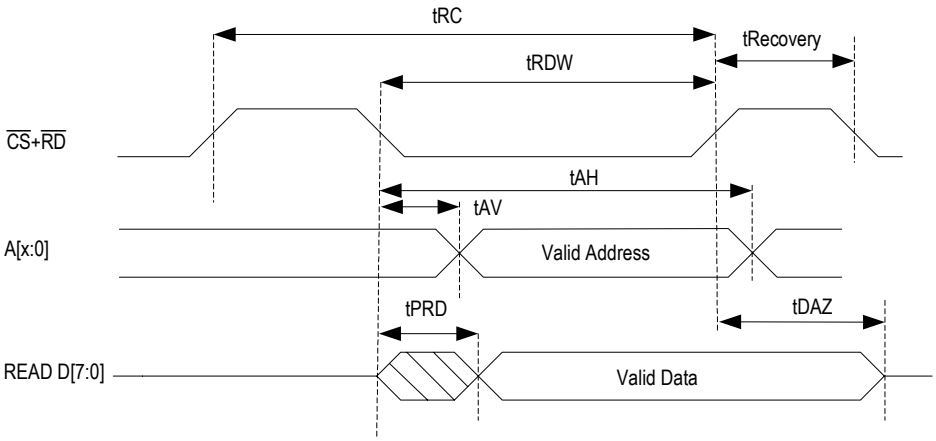


Figure-34 Non_multiplexed Motorola Write Timing

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Table-70 Non_multiplexed Intel Read Timing Characteristics

Symbol	Parameter	Min	Max	Unit
tRC	Read Cycle Time	190		ns
tRDW	Valid $\overline{RD}$ Width	180		ns
tAV	Delay from $\overline{RD}$ to Valid Address		15	ns
tAH	Address to $\overline{RD}$ Hold Time	65		ns
tPRD	$\overline{RD}$ to Valid Read Data Propagation Delay		175	ns
tDAZ	Delay from $\overline{RD}$ inactive to data bus High Impedance	5	20	ns
tRecovery	Recovery Time from Read Cycle	5		ns



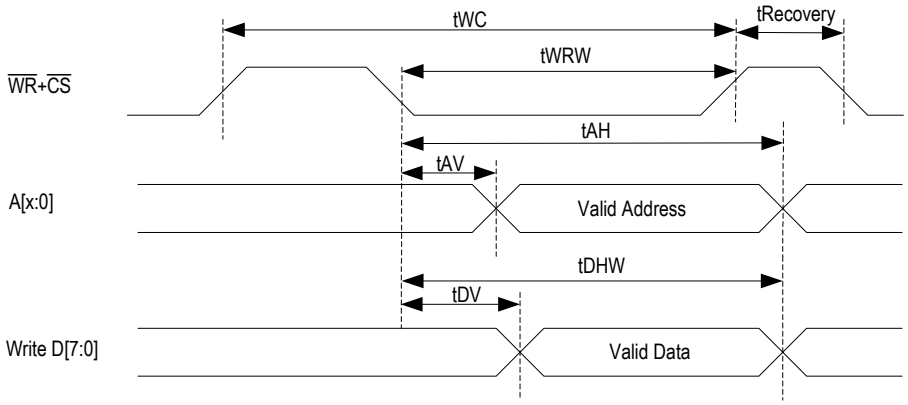
Note: $\overline{WR}$ should be tied to high

Figure-35 Non_multiplexed Intel Read Timing

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Table-71 Non_multiplexed Intel Write Timing Characteristics

Symbol	Parameter	Min	Max	Unit
tWC	Write Cycle Time	120		ns
tWRW	Valid $\overline{WR}$ Width	100		ns
tAV	Delay from $\overline{WR}$ to Valid Address		15	ns
tAH	Address to $\overline{WR}$ Hold Time	65		ns
tDV	Delay from $\overline{WR}$ to Valid Write Data		15	ns
tDHW	Write Data to $\overline{WR}$ Hold Time	65		ns
tRecovery	Recovery Time from Write Cycle	5		ns

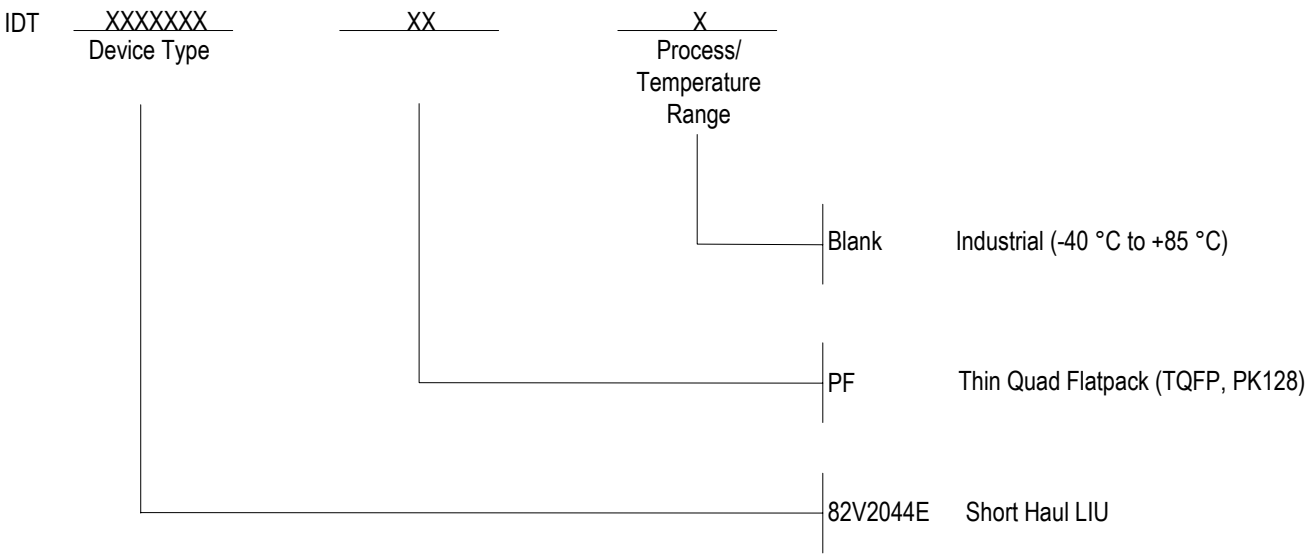


Note: $\overline{RD}$ should be tied to high

Figure-36 Non_multiplexed Intel Write Timing

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

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