SINGLE CHANNEL E1 SHORT HAUL LINE INTERFACE UNIT

IDT82V2051E

FEATURES

- **Single channel E1 short haul line interfaces**
- **Supports HPS (Hitless Protection Switching) for 1+1 protection without external relays**
- **Single 3.3 V power supply with 5 V tolerance on digital interfaces**
- **Meets or exceeds specifications in**
  - ANSI T1.102
  - ITU I.431, G.703, G.736, G.775 and G.823
  - ETSI 300-166, 300-233 and TBR12/13
- **Software programmable or hardware selectable on:**
  - Wave-shaping templates
  - Line terminating impedance (75 Ω/120 Ω)
  - Adjustment of arbitrary pulse shape
  - JA (Jitter Attenuator) position (receive path or transmit path)
  - Single rail/dual rail system interfaces
  - HDB3/AMI line encoding/decoding
  - Active edge of transmit clock (TCLK) and receive clock (RCLK)
  - Active level of transmit data (TDATA) and receive data (RDATA)
  - Receiver or transmitter power down
  - High impedance setting for line drivers
  - PRBS (Pseudo Random Bit Sequence) generation and detection with 2^{15}-1 PRBS polynomials
  - 16-bit BPV (Bipolar Pulse Violation) /Excess Zero/PRBS error counter
  - Analog loopback, Digital loopback, Remote loopback
- **Short circuit protection and internal protection diode for line drivers**
- **AIS (Alarm Indication Signal) detection**
- **Supports serial control interface, Motorola and Intel Multiplexed interfaces and hardware control mode**
- **Pin compatibe to 82V2081 T1/E1/J1 Long Haul/Short Haul LIU and 82V2041E T1/E1/J1 Short Haul LIU**
- **Package:**
  Available in 44-pin TQFP packages
  Green package options available

DESCRIPTION

The IDT82V2051E is a single channel E1 Line Interface Unit. The IDT82V2051E performs clock/data recovery, AMI/HDB3 line decoding and detects and reports the LOS conditions. An integrated Adaptive Equalizer is available to increase the receive sensitivity and enable programming of LOS levels. In transmit path, there is an AMI/HDB3 encoder and Waveform Shaper. There is one Jitter Attenuator, which can be placed in either the receive path or the transmit path. The Jitter Attenuator can also be disabled. The IDT82V2051E supports both Single Rail and Dual Rail system interfaces. To facilitate the network maintenance, a PRBS generation/detection circuit is integrated in the chip, and different types of loopbacks can be set according to the applications. Two different kinds of line terminating impedance, 75 Ω and 120 Ω are selectable. The chip also provides driver short-circuit protection and internal protection diode. The chip can be controlled by either software or hardware.

The IDT82V2051E can be used in LAN, WAN, Routers, Wireless Base Stations, IADs, IMAs, IMAPs, Gateways, Frame Relay Access Devices, CSU/DSU equipment, etc.

IDT and the IDT logo are trademarks of Integrated Device Technology, Inc.

© 2019 Renesas Electronics Corporation

DSC-6528/2

FUNCTIONAL BLOCK DIAGRAM

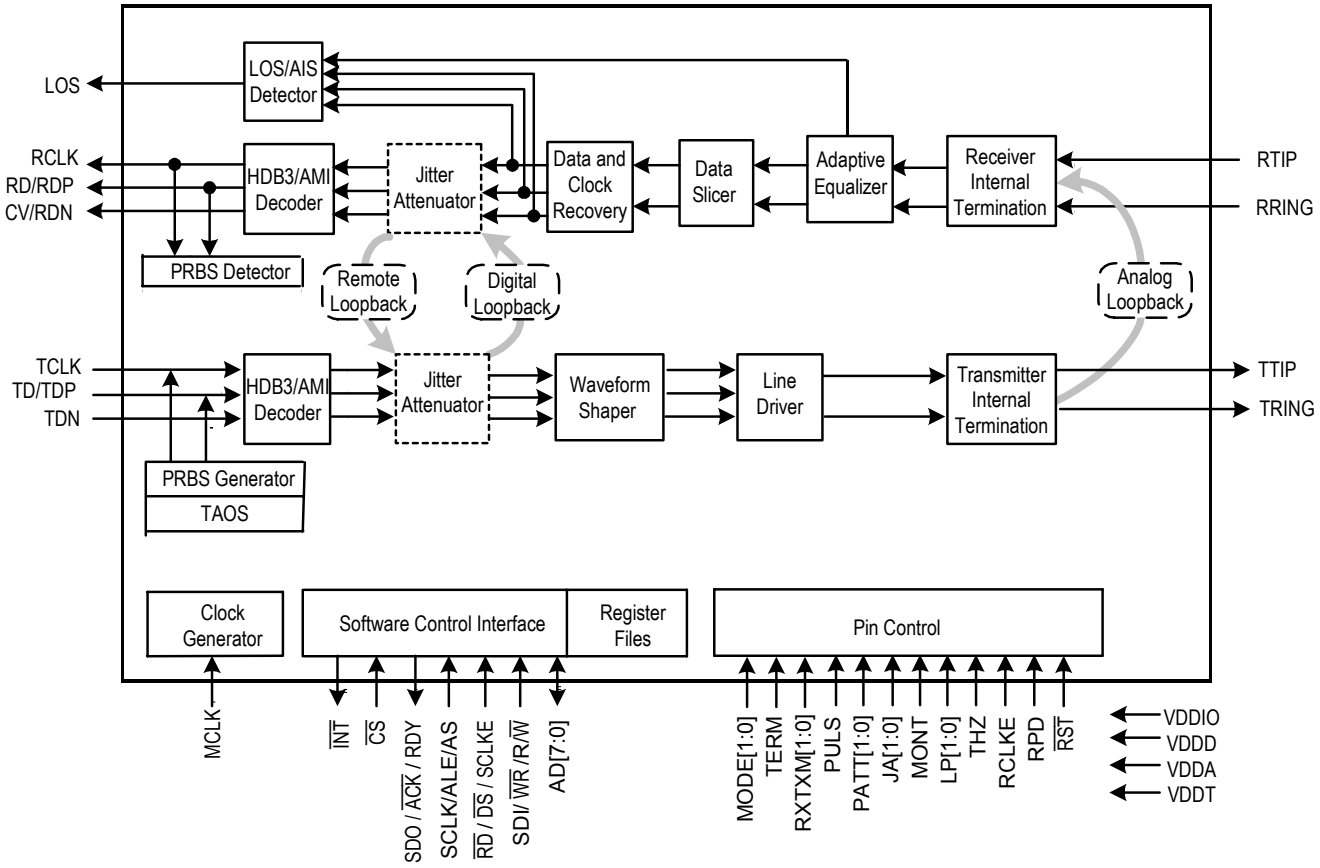


Figure-1 Block Diagram

© 2019 Renesas Electronics Corporation

Table of Contents

1 IDT82V2051E Pin Configurations 8

2 Pin Description 9

3 Functional Description 15

3.1 Control Mode Selection 15

3.2 Transmit Path 15

3.2.1 Transmit Path System Interface 15

3.2.2 Encoder 15

3.2.3 Pulse Shaper 15

3.2.3.1 Preset Pulse Templates 15

3.2.3.2 User-Programmable Arbitrary Waveform 16

3.2.4 Transmit Path Line Interface 17

3.2.5 Transmit Path Power Down 17

3.3 Receive Path 18

3.3.1 Receive Internal Termination 18

3.3.2 Line Monitor 19

3.3.3 Adaptive Equalizer 20

3.3.4 Receive Sensitivity 20

3.3.5 Data Slicer 20

3.3.6 CDR (Clock & Data Recovery) 20

3.3.7 Decoder 20

3.3.8 Receive Path System Interface 21

3.3.9 Receive Path Power Down 21

3.4 Jitter Attenuator 21

3.4.1 Jitter Attenuation Function Descripton 21

3.4.2 Jitter Attenuator Performance 22

3.5 Los And AIS Detection 22

3.5.1 LOS Detection 22

3.5.2 AIS Detection 23

3.6 Transmit And Detect Internal Patterns 24

3.6.1 Transmit All Ones 24

3.6.2 Transmit All Zeros 24

3.6.3 PRBS Generation And Detection 24

3.7 Loopback 24

3.7.1 Analog Loopback 24

3.7.2 Digital Loopback 24

3.7.3 Remote Loopback 24

3.8 Error Detection/Counting And Insertion 27

© 2019 Renesas Electronics Corporation

3.8.1 Definition Of Line Coding Error 27
3.8.2 Error Detection And Counting 27
3.8.3 Bipolar Violation And PRBS Error Insertion 28
3.9 Line Driver Failure Monitoring 28
3.10 MCLK And TCLK 29
3.10.1 Master Clock (MCLK) 29
3.10.2 Transmit Clock (TCLK) 29
3.11 Microcontroller Interfaces 30
3.11.1 Parallel Microcontroller Interface 30
3.11.2 Serial Microcontroller Interface 30
3.12 Interrupt Handling 30
3.13 5V Tolerant I/O Pins 31
3.14 Reset Operation 31
3.15 Power Supply 31
4 Programming Information 32
4.1 Register List And Map 32
4.2 Reserved Registers 32
4.3 Register Description 33
4.3.1 Control Registers 33
4.3.2 Transmit Path Control Registers 35
4.3.3 Receive Path Control Registers 37
4.3.4 Network Diagnostics Control Registers 39
4.3.5 Interrupt Control Registers 41
4.3.6 Line Status Registers 43
4.3.7 Interrupt Status Registers 45
4.3.8 Counter Registers 46
5 Hardware Control Pin Summary 47
6 Test Specifications 49
7 Microcontroller Interface Timing Characteristics 56
7.1 Serial Interface Timing 56
7.2 Parallel Interface Timing 57

© 2019 Renesas Electronics Corporation

List of Tables

Table-1 Pin Description 9
Table-2 Transmit Waveform Value For E1 75 ohm 16
Table-3 Transmit Waveform Value For E1 120 ohm 16
Table-4 Impedance Matching for Transmitter 17
Table-5 Impedance Matching for Receiver 18
Table-6 Criteria of Starting Speed Adjustment 22
Table-7 LOS Declare and Clear Criteria, Adaptive Equalizer Disabled 22
Table-8 LOS Declare and Clear Criteria, Adaptive Equalizer Enabled 23
Table-9 AIS Condition 23
Table-10 Criteria for Setting/Clearing the PRBS_S Bit 24
Table-11 EXZ Definition 27
Table-12 Interrupt Event 31
Table-13 Register List and Map 32
Table-14 ID: Device Revision Register 33
Table-15 RST: Reset Register 33
Table-16 GCF: Global Configuration Register 33
Table-17 TERM: Transmit and Receive Termination Configuration Register 33
Table-18 JACF: Jitter Attenuation Configuration Register 34
Table-19 TCF0: Transmitter Configuration Register 0 35
Table-20 TCF1: Transmitter Configuration Register 1 35
Table-21 TCF2: Transmitter Configuration Register 2 35
Table-22 TCF3: Transmitter Configuration Register 3 36
Table-23 TCF4: Transmitter Configuration Register 4 36
Table-24 RCF0: Receiver Configuration Register 0 37
Table-25 RCF1: Receiver Configuration Register 1 37
Table-26 RCF2: Receiver Configuration Register 2 38
Table-27 MAINT0: Maintenance Function Control Register 0 39
Table-28 MAINT1: Maintenance Function Control Register 1 39
Table-29 MAINT6: Maintenance Function Control Register 6 39
Table-30 INTM0: Interrupt Mask Register 0 41
Table-31 INTM1: Interrupt Masked Register 1 41
Table-32 INTES: Interrupt Trigger Edge Select Register 42
Table-33 STAT0: Line Status Register 0 (real time status monitor) 43
Table-34 STAT1: Line Status Register 1 (real time status monitor) 44
Table-35 INTS0: Interrupt Status Register 0 45
Table-36 INTS1: Interrupt Status Register 1 45
Table-37 CNT0: Error Counter L-byte Register 0 46
Table-38 CNT1: Error Counter H-byte Register 1 46
Table-39 Hardware Control Pin Summary 47
Table-40 Absolute Maximum Rating 49
Table-41 Recommended Operation Conditions 49

© 2019 Renesas Electronics Corporation

Table-42 Power Consumption 50
Table-43 DC Characteristics 50
Table-44 Receiver Electrical Characteristics 50
Table-45 Transmitter Electrical Characteristics 51
Table-46 Transmitter and Receiver Timing Characteristics 52
Table-47 Jitter Tolerance 53
Table-48 Jitter Attenuator Characteristics 54
Table-49 Serial Interface Timing Characteristics 56
Table-50 Multiplexed Motorola Read Timing Characteristics 57
Table-51 Multiplexed Motorola Write Timing Characteristics 58
Table-52 Multiplexed Intel Read Timing Characteristics 59
Table-53 Multiplexed Intel Write Timing Characteristics 60

© 2019 Renesas Electronics Corporation

List of Figures

Figure-1 Block Diagram 2
Figure-2 IDT82V2051E TQFP44 Package Pin Assignment 8
Figure-3 E1 Waveform Template Diagram 15
Figure-4 E1 Pulse Template Test Circuit 15
Figure-5 Receive Monitor Gain Adaptive Equalizer 18
Figure-6 Transmit/Receive Line Circuit 18
Figure-7 Monitoring Receive Line in Another Chip 19
Figure-8 Monitor Transmit Line in Another Chip 19
Figure-9 Jitter Attenuator 21
Figure-10 LOS Declare and Clear 22
Figure-11 Analog Loopback 25
Figure-12 Digital Loopback 25
Figure-13 Remote Loopback 26
Figure-14 Auto Report Mode 27
Figure-15 Manual Report Mode 28
Figure-16 TCLK Operation Flowchart 29
Figure-17 Serial Microcontroller Interface Function Timing 30
Figure-18 Transmit System Interface Timing 52
Figure-19 Receive System Interface Timing 53
Figure-20 E1 Jitter Tolerance Performance 54
Figure-21 E1 Jitter Transfer Performance 55
Figure-22 Serial Interface Write Timing 56
Figure-23 Serial Interface Read Timing with SCLKE=1 56
Figure-24 Serial Interface Read Timing with SCLKE=0 56
Figure-25 Multiplexed Motorola Read Timing 57
Figure-26 Multiplexed Motorola Write Timing 58
Figure-27 Multiplexed Intel Read Timing 59
Figure-28 Multiplexed Intel Write Timing 60

© 2019 Renesas Electronics Corporation

1 IDT82V2051E PIN CONFIGURATIONS

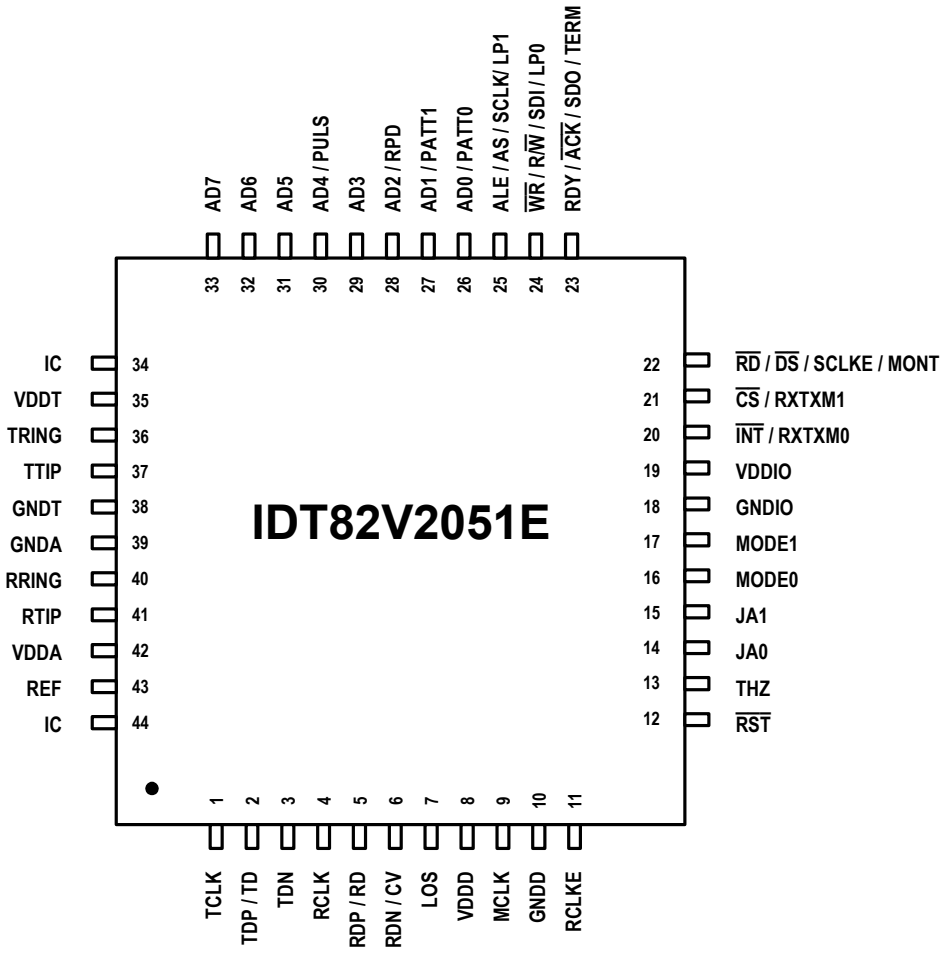


Figure-2 IDT82V2051E TQFP44 Package Pin Assignment

© 2019 Renesas Electronics Corporation

2 PIN DESCRIPTION

Table-1 Pin Description

<table>
<tr><th>Name</th><th>Type</th><th>Pin No.</th><th>Description</th></tr>
<tr><td>TTIP
TRING</td><td>Analog output</td><td>37
36</td><td>TTIP/TRING: Transmit Bipolar Tip/Ring
These pins are the differential line driver outputs. They will be in high impedance state under the following conditions:
• THZ pin is high;
• THZ bit is set to 1;
• Loss of MCLK;
• Loss of TCLK (exceptions: Remote Loopback; transmit internal pattern by MCLK);
• Transmit path power down;
• After software reset; pin reset and power on.</td></tr>
<tr><td>RTIP
RRING</td><td>Analog input</td><td>41
40</td><td>RTIP/RRING: Receive Bipolar Tip/Ring
These signals are the differential receiver inputs.</td></tr>
<tr><td>TD/TDP
TDN</td><td>I</td><td>2
3</td><td>TD: Transmit Data
When the device is in single rail mode, the NRZ data to be transmitted is input on this pin. Data on TD pin is sampled into the device on the active edge of TCLK and is encoded by AMI or HDB3 line code rules before being transmitted. In this mode, TDN should be connected to ground.

TDP/TDN: Positive/Negative Transmit Data
When the device is in dual rail mode, the NRZ data to be transmitted for positive/negative pulse is input on these pins. Data on TDP/TDN pin is sampled into the device on the active edge of TCLK. The line code in dual rail mode is as follows:

<table><tr><th>TDP</th><th>TDN</th><th>Output Pulse</th></tr><tr><td>0</td><td>0</td><td>Space</td></tr><tr><td>0</td><td>1</td><td>Positive Pulse</td></tr><tr><td>1</td><td>0</td><td>Negative Pulse</td></tr><tr><td>1</td><td>1</td><td>Space</td></tr></table></td></tr>
<tr><td>TCLK</td><td>I</td><td>1</td><td>TCLK: Transmit Clock input
This pin inputs a 2.048 MHz transmit clock. The transmit data at TD/TDP or TDN is sampled into the device on the active edge of TCLK. If TCLK is missing[1] and the TCLK missing interrupt is not masked, an interrupt will be generated.</td></tr>
<tr><td>RD/RDP
CV/RDN</td><td>O</td><td>5
6</td><td>RD: Receive Data output
In single rail mode, this pin outputs NRZ data. The data is decoded according to AMI or HDB3 line code rules.

CV: Code Violation indication
In single rail mode, the BPV/CV code violation will be reported by driving the CV pin to high level for a full clock cycle. HDB3 line code violation can be indicated if the HDB3 decoder is enabled. When AMI decoder is selected, bipolar violation will be indicated.
In hardware control mode, the EXZ, BPV/CV errors in received data stream are always monitored by the CV pin if single rail mode is chosen.

RDP/RDN: Positive/Negative Receive Data output
In dual rail mode, this pin outputs the re-timed NRZ data when CDR is enabled, or directly outputs the raw RZ slicer data if CDR is bypassed.

Active edge and level select:
Data on RDP/RDN or RD is clocked with either the rising or the falling edge of RCLK. The active polarity is also selectable.</td></tr>
<tr><td>RCLK</td><td>O</td><td>4</td><td>RCLK: Receive Clock output
This pin outputs a 2.048 MHz receive clock. Under LOS condition with AIS enabled (bit AISE=1), RCLK is derived from MCLK. In clock recovery mode, this signal provides the clock recovered from the RTIP/RRING signal. The receive data (RD in single rail mode or RDP and RDN in dual rail mode) is clocked out of the device on the active edge of RCLK. If clock recovery is bypassed, RCLK is the exclusive OR (XOR) output of the dual rail slicer data RDP and RDN. This signal can be used in applications with external clock recovery circuitry.</td></tr>
</table>

Notes:

1. TCLK missing: the state of TCLK continues to be high level or low level over 70 MCLK cycles.

© 2019 Renesas Electronics Corporation

Table-1 Pin Description (Continued)

<table>
<tr><th>Name</th><th>Type</th><th>Pin No.</th><th>Description</th></tr>
<tr><td>MCLK</td><td>I</td><td>9</td><td>MCLK: Master Clock input
A built-in clock system that accepts a 2.048MHz reference clock. This reference clock is used to generate several internal reference signals:
• Timing reference for the integrated clock recovery unit.
• Timing reference for the integrated digital jitter attenuator.
• Timing reference for microcontroller interface.
• Generation of RCLK signal during a loss of signal condition.
• Reference clock to transmit All Ones, all zeros and PRBS pattern. Note that for ATAO and AIS, MCLK is always used as the reference clock.
• Reference clock during the Transmit All Ones (TAO) condition or sending PRBS in hardware control mode.
The loss of MCLK will turn TTIP/TRING into high impedance status.</td></tr>
<tr><td>LOS</td><td>O</td><td>7</td><td>LOS: Loss of Signal Output
This is an active high signal used to indicate the loss of received signal. When LOS pin becomes high, it indicates the loss of received signal. The LOS pin will become low automatically when valid received signal is detected again. The criteria of loss of signal are described in 3.5 Los And AIS Detection.</td></tr>
<tr><td>REF</td><td>I</td><td>43</td><td>REF: reference resister
An external resistor (3 KΩ, 1%) is used to connect this pin to ground to provide a standard reference current for internal circuit.</td></tr>
<tr><td>MODE1
MODE0</td><td>I</td><td>17
16</td><td>MODE[1:0]: operation mode of Control interface select
The level on this pin determines which control mode is used to control the device as follows:
<table><tr><th>MODE[1:0]</th><th>Control Interface mode</th></tr><tr><td>00</td><td>Hardware interface</td></tr><tr><td>01</td><td>Serial Microcontroller Interface</td></tr><tr><td>10</td><td>Parallel –Multiplexed -Motorola Interface</td></tr><tr><td>11</td><td>Parallel –Multiplexed -Intel Interface</td></tr></table>• The serial microcontroller Interface consists of $\overline{CS}$, SCLK, SCLKE, SDI, SDO and $\overline{INT}$ pins. SCLKE is used for the selection of the active edge of SCLK.
• The parallel multiplexed microcontroller interface consists of $\overline{CS}$, AD[7:0], $\overline{DS}$/$\overline{RD}$, R/$\overline{W}$/$\overline{WR}$, ALE/AS, $\overline{ACK}$/RDY and $\overline{INT}$ pins. (refer to 3.11 Microcontroller Interfaces for details)
• Hardware interface consists of PULS, THZ, RCLKE, LP[1:0], PATT[1:0], JA[1:0], MONT, TERM, RPD, MODE[1:0] and RXTXM[1:0]</td></tr>
<tr><td>RCLKE</td><td>I</td><td>11</td><td>RCLKE: the active edge of RCLK select
In hardware control mode, this pin selects the active edge of RCLK
• L= select the rising edge as the active edge of RCLK
• H= select the falling edge as the active edge of RCLK
In software control mode, this pin should be connected to GNDIO.</td></tr>
<tr><td>$\overline{CS}$

RXTXM1</td><td>I</td><td>21</td><td>$\overline{CS}$: Chip Select
In serial or parallel microcontroller interface mode, this is the active low enable signal. A low level on this pin enables serial or parallel microcontroller interface.

RXTXM[1:0]: Receive and transmit path operation mode select
In hardware control mode, these pins are used to select the single rail or dual rail operation modes as well as AMI or HDB3 line coding:
• 00= single rail with HDB3 coding
• 01= single rail with AMI coding
• 10= dual rail interface with CDR enabled
• 11= slicer mode (dual rail interface with CDR disabled)</td></tr>
</table>

© 2019 Renesas Electronics Corporation

Table-1 Pin Description (Continued)

Name	Type	Pin No.	Description
$\overline{\text{INT}}$	O	20	**$\overline{\text{INT}}$: Interrupt Request** In software control mode, this pin outputs the general interrupt request for all interrupt sources. These interrupt sources can be masked individually via registers (**INTM0, 14H**) and (**INTM1, 15H**). The interrupt status is reported via the registers (**INTS0, 19H**) and (**INTS1, 1AH**). Output characteristics of this pin can be defined to be push-pull (active high or active low) or open-drain (active low) by setting INT_PIN[1:0] (**GCF, 02H**).
RXTXM0	I		**RXTXM0** See RXTXM1 above.
SCLK	I	25	**SCLK: Shift Clock** In serial microcontroller interface mode, this signal is the shift clock for the serial interface. Configuration data on SDI pin is sampled on the rising edge of SCLK. Configuration and status data on SDO pin is clocked out of the device on the falling edge of SCLK if SCLKE pin is high, or on the rising edge of SCLK if SCLKE pin is low.
ALE			**ALE: Address Latch Enable** In parallel microcontroller interface mode with multiplexed Intel interface, the address on AD[7:0] is sampled into the device on the falling edge of ALE.
AS			**AS: Address Strobe** In parallel microcontroller interface mode with multiplexed Motorola interface, the address on AD[7:0] is latched into the device on the falling edge of AS.
LP1			**LP[1:0]: Loopback mode select** When the chip is configured by hardware, this pin is used to select loopback operation modes: • 00= no loopback • 01= analog loopback • 10= digital loopback • 11= remote loopback
SDI	I	24	**SDI: Serial Data Input** In serial microcontroller interface mode, this signal is the input data to the serial interface. Configuration data at SDI pin is sampled by the device on the rising edge of SCLK.
$\overline{\text{WR}}$			**$\overline{\text{WR}}$: Write Strobe** In Intel parallel multiplexed interface mode, this pin is asserted low by the microcontroller to initiate a write cycle. The data on AD[7:0] is sampled into the device in a write operation.
R/$\overline{\text{W}}$			**R/$\overline{\text{W}}$: Read/Write Select** In Motorola parallel multiplexed interface mode, this pin is low for write operation and high for read operation.
LP0			**LP0** See LP1 above.

© 2019 Renesas Electronics Corporation

Table-1 Pin Description (Continued)

<table>
<tr><th>Name</th><th>Type</th><th>Pin No.</th><th>Description</th></tr>
<tr><td>SDO</td><td>O</td><td>23</td><td>SDO: Serial Data Output
In serial microcontroller interface mode, this signal is the output data of the serial interface. Configuration or Status data at SDO pin is clocked out of the device on the falling edge of SCLK if SCLKE pin is high, or on the rising edge of SCLK if SCLKE pin is low.</td></tr>
<tr><td>$\overline{ACK}$</td><td></td><td></td><td>$\overline{ACK}$: Acknowledge Output
In Motorola parallel mode interface, the low level on this pin means:
• The valid information is on the data bus during a read operation.
• The write data has been accepted during a write cycle.</td></tr>
<tr><td>RDY</td><td></td><td></td><td>RDY: Ready signal output
In Intel parallel mode interface, the low level on this pin means a read or write operation is in progress; a high acknowledges a read or write operation has been completed.</td></tr>
<tr><td>TERM</td><td>I</td><td></td><td>TERM: Internal or external termination select in hardware mode
This pin selects internal or external impedance matching for both receiver and transmitter.
• 0 = ternary interface with external impedance matching network
• 1 = ternary interface with internal impedance matching network</td></tr>
<tr><td>SCLKE</td><td>I</td><td>22</td><td>SCLKE: Serial Clock Edge Select
In serial microcontroller interface mode, this signal selects the active edge of SCLK for outputting SDO. The output data is valid after some delay from the active clock edge. It can be sampled on the opposite edge of the clock. The active clock edge which clocks the data out of the device is selected as shown below:
<table><tr><th>SCLKE</th><th>SCLK</th></tr><tr><td>Low</td><td>Rising edge is the active edge.</td></tr><tr><td>High</td><td>Falling edge is the active edge.</td></tr></table></td></tr>
<tr><td>$\overline{RD}$</td><td></td><td></td><td>$\overline{RD}$: Read Strobe
In Intel parallel multiplexed interface mode, the data is driven to AD[7:0] by the device during low level of $\overline{RD}$ in a read operation.</td></tr>
<tr><td>$\overline{DS}$</td><td></td><td></td><td>$\overline{DS}$: Data Strobe
In Motorola parallel multiplexed interface mode, this signal is the data strobe of the parallel interface. In a write operation (R/$\overline{W}$ = 0), the data on AD[7:0] is sampled into the device. In a read operation (R/$\overline{W}$ = 1), the data is driven to AD[7:0] by the device.</td></tr>
<tr><td>MONT</td><td></td><td></td><td>MONT: Receive Monitor gain select
In hardware control mode with ternary interface, this pin selects the receive monitor gain of receiver:
0= 0 dB
1= 26 dB</td></tr>
<tr><td>AD7</td><td>I/O</td><td>33</td><td>AD7: Address/Data Bus bit7
In Intel/Motorola multiplexed interface mode, this signal is the multiplexed bi-directional address/data bus of the microcontroller interface.
In serial microcontroller interface mode, this pin should be connected to ground through a 10 kΩ resistor.

In Hardware mode, this pin has to be tied to GND.</td></tr>
<tr><td>AD6</td><td>I/O</td><td>32</td><td>AD6: Address/Data Bus bit6
In Intel/Motorola multiplexed interface mode, this signal is the multiplexed bi-directional address/data bus of the microcontroller interface.
In serial microcontroller interface mode, this pin should be connected to ground through a 10 kΩ resistor.

In Hardware mode, this pin has to be tied to GND.</td></tr>
</table>

© 2019 Renesas Electronics Corporation

Table-1 Pin Description (Continued)

Name	Type	Pin No.	Description
AD5	I/O	31	**AD5: Address/Data Bus bit5** In Intel/Motorola multiplexed interface mode, this signal is the multiplexed bi-directional address/data bus of the microcontroller interface. In serial microcontroller interface mode, this pin should be connected to ground through a 10 kΩ resistor. In Hardware mode, this pin has to be tied to GND.
AD4	I/O	30	**AD4: Address/Data Bus bit4** In Intel/Motorola multiplexed interface mode, this signal is the multiplexed bi-directional address/data bus of the microcontroller interface. In serial microcontroller interface mode, this pin should be connected to ground through a 10 kΩ resistor. **PULS: this pin is used to select the following functions in hardware control mode:** • Transmit pulse template • Internal termination impedance (75 Ω / 120 Ω) Refer to 5 Hardware Control Pin Summary for details.
AD3	I/O	29	**AD3: Address/Data Bus bit3** In Intel/Motorola multiplexed interface mode, this signal is the multiplexed bi-directional address/data bus of the microcontroller interface. In serial microcontroller interface mode, this pin should be connected to ground through a 10 kΩ resistor.
AD2	I/O	28	**AD2: Address/Data Bus bit2** In Intel/Motorola multiplexed interface mode, this signal is the multiplexed bi-directional address/data bus of the microcontroller interface. In serial microcontroller interface mode, this pin should be connected to ground through a 10 kΩ resistor.
RPD	I		**RPD: Receiver power down control in hardware control mode** • 0= normal operation • 1= receiver power down
AD1	I/O	27	**AD1: Address/Data Bus bit1** In Intel/Motorola multiplexed interface mode, this signal is the multiplexed bi-directional address/data bus of the microcontroller interface. In serial microcontroller interface mode, this pin should be connected to ground through a 10 kΩ resistor.
PATT1	I		**PATT[1:0]: Transmit pattern select** In hardware control mode, this pin selects the transmit pattern • 00 = normal • 01= All Ones • 10= PRBS • 11= transmitter power down
AD0	I/O	26	**AD0: Address/Data Bus bit0** In Intel/Motorola multiplexed interface mode, this signal is the multiplexed bi-directional address/data bus of the microcontroller interface. In serial microcontroller interface mode, this pin should be connected to ground through a 10 kΩ resistor.
PATT0	I		See above.
JA1	I	15	**JA[1:0]: Jitter attenuation position, bandwidth and the depth of FIFO select (only used for hardware control mode)** • 00 = JA is disabled • 01 = JA in receiver, broad bandwidth, FIFO=64 bits • 10 = JA in receiver, narrow bandwidth, FIFO=128 bits • 11 = JA in transmitter, narrow bandwidth, FIFO=128 bits In software control mode, this pin should be connected to ground.
JA0	I	14	See above.

© 2019 Renesas Electronics Corporation

Table-1 Pin Description (Continued)

Name	Type	Pin No.	Description
$\overline{RST}$	I	12	**$\overline{RST}$: Hardware reset** The chip is forced to reset state if a low signal is input on this pin for more than 100 ns. MCLK must be active during reset.
THZ	I	13	**THZ: Transmitter Driver High Impedance Enable** This signal enables or disables transmitter driver. A low level on this pin enables the driver while a high level on this pin places driver in high impedance state. Note that the functionality of the internal circuits is not affected by this signal.
Power Supplies and Grounds			
VDDIO	-	19	**3.3 V I/O power supply**
GNDIO	-	18	**I/O ground**
VDDT	-	35	**3.3 V power supply for transmitter driver**
GNDT	-	38	**Analog ground for transmitter driver**
VDDA	-	42	**3.3 V analog core power supply**
GNDA	-	39	**Analog core ground**
VDDD	-	8	**Digital core power supply**
GNDD	-	10	**Digital core ground**
Others			
IC	-	34	**IC: Internal connection** Internal Use. This pin should be left open when in normal operation.
IC	-	44	**IC: Internal connection** Internal Use. This pin should be connected to ground when in normal operation.

© 2019 Renesas Electronics Corporation

3 FUNCTIONAL DESCRIPTION

3.1 CONTROL MODE SELECTION

The IDT82V2051E can be configured by software or by hardware. The software control mode supports Serial Control Interface, Motorola Multiplexed Control Interface and Intel Multiplexed Control Interface. The Control mode is selected by MODE1 and MODE0 pins as follows:

	Control Interface mode
00	Hardware interface
01	Serial Microcontroller Interface.
10	Parallel –Multiplexed -Motorola Interface
11	Parallel –Multiplexed -Intel Interface

- The serial microcontroller Interface consists of $\overline{CS}$, SCLK, SCLKE, SDI, SDO and $\overline{INT}$ pins. SCLKE is used for the selection of active edge of SCLK.
- The parallel Multiplexed microcontroller Interface consists of $\overline{CS}$, AD[7:0], $\overline{DS}$/$\overline{RD}$, R/$\overline{W}$/$\overline{WR}$, ALE/AS, $\overline{ACK}$/RDY and $\overline{INT}$ pins.
- Hardware interface consists of PULS, THZ, RCLKE, LP[1:0], PATT[1:0], JA[1:0], MONT, TERM, RPD, MODE[1:0] and RXTXM[1:0]. Refer to 5 Hardware Control Pin Summary for details about hardware control.

3.2 TRANSMIT PATH

The transmit path of IDT82V2051E consists of an Encoder, an optional Jitter Attenuator, a Waveform Shaper, a Line Driver and a Programmable Transmit Termination.

3.2.1 TRANSMIT PATH SYSTEM INTERFACE

The transmit path system interface consists of TCLK pin, TD/TDP pin and TDN pin. TCLK is a 2.048 MHz clock. If TCLK is missing for more than 70 MCLK cycles, an interrupt will be generated if it is not masked.

Transmit data is sampled on the TD/TDP and TDN pins by the active edge of TCLK. The active edge of TCLK can be selected by the TCLK_SEL bit (**TCF0, 05H**). And the active level of the data on TD/TDP and TDN can be selected by the TD_INV bit (**TCF0, 05H**). In hardware control mode, the falling edge of TCLK and the active high of transmit data are always used.

The transmit data from the system side can be provided in two different ways: Single Rail and Dual Rail. In Single Rail mode, only TD pin is used for transmitting data and the T_MD[1] bit (**TCF0, 05H**) should be set to '0'. In Dual Rail Mode, both TDP pin and TDN pin are used for transmitting data, the T_MD[1] bit (**TCF0, 05H**) should be set to '1'.

3.2.2 ENCODER

In Single Rail mode, the Encoder can be configured to be a HDB3 encoder or an AMI encoder by setting T_MD[0] bit (**TCF0, 05H**).

In Dual Rail mode, the Encoder is by-passed. In Dual Rail mode, a logic '1' on the TDP pin and a logic '0' on the TDN pin results in a negative pulse on the TTIP/TRING; a logic '0' on TDP pin and a logic '1' on TDN pin results in a positive pulse on the TTIP/TRING. If both TDP and TDN are high or low, the TTIP/TRING outputs a space (Refer to TD/TDP, TDN Pin Description).

In hardware control mode, the operation mode of receive and transmit path can be selected by setting RXTXM1 and RXTXM0 pins. Refer to 5 Hardware Control Pin Summary for details.

3.2.3 PULSE SHAPER

The IDT82V2051E provides two ways of manipulating the pulse shape before sending it. One is to use preset pulse templates, the other is to use user-programmable arbitrary waveform template.

In software control mode, the pulse shape can be selected by setting the related registers.

In hardware control mode, the pulse shape can be selected by setting PULS pin. Refer to 5 Hardware Control Pin Summary for details.

3.2.3.1 PRESET PULSE TEMPLATES

The pulse shape is shown in Figure-3 according to the G.703 and the measuring diagram is shown in Figure-4. In internal impedance matching mode, if the cable impedance is 75 Ω, the PULS[3:0] bits (**TCF1, 06H**) should be set to '0000'; if the cable impedance is 120 Ω, the PULS[3:0] bits (**TCF1, 06H**) should be set to '0001'. In external impedance matching mode, for both E1/75 Ω and E1/120 Ω cable impedance, PULS[3:0] should be set to '0001'.

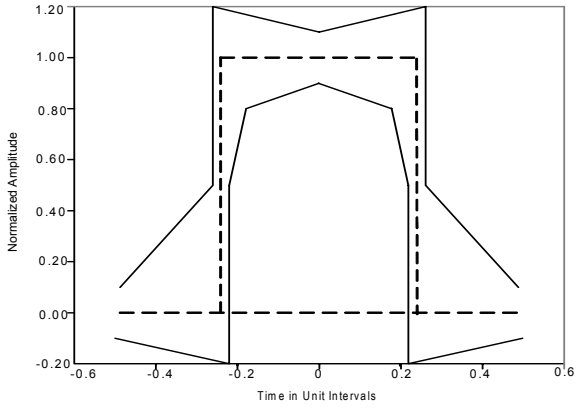


Figure-3 E1 Waveform Template Diagram

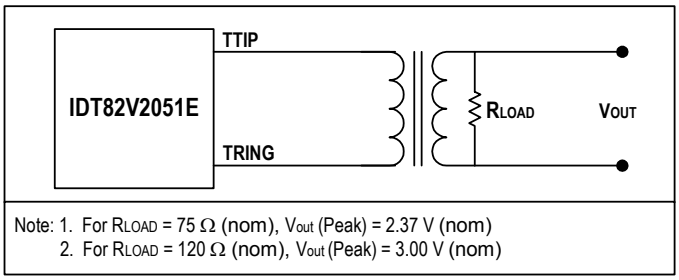


Figure-4 E1 Pulse Template Test Circuit

© 2019 Renesas Electronics Corporation

3.2.3.2 USER-PROGRAMMABLE ARBITRARY WAVEFORM

When the PULS[3:0] bits are set to '11xx', user-programmable arbitrary waveform generator mode can be used. This allows the transmitter performance to be tuned for a wide variety of line condition or special application.

Each pulse shape can extend up to 4 UIs (Unit Interval), addressed by UI[1:0] bits (**TCF3, 08H**) and each UI is divided into 16 sub-phases, addressed by the SAMP[3:0] bits (**TCF3, 08H**). The pulse amplitude of each phase is represented by a binary byte, within the range from +63 to -63, stored in WDAT[6:0] bits (**TCF4, 09H**) in signed magnitude form. The most positive number +63 (D) represents the positive maximum amplitude of the transmit pulse while the most negative number -63 (D) represents the maximum negative amplitude of the transmit pulse. Therefore, up to 64 bytes are used.

There are two standard templates which are stored in an on-chip ROM. User can select one of them as reference and make some changes to get the desired waveform.

User can change the wave shape and the amplitude to get the desired pulse shape. In order to do this, firstly, users can choose a set of waveform value from the following two tables, which is the most similar to the desired pulse shape. Table-2 and Table-3 list the sample data and scaling data of each of the two templates. Then modify the corresponding sample data to get the desired transmit pulse shape.

Secondly, through the value of SCAL[5:0] bits increased or decreased by 1, the pulse amplitude can be scaled up or down at the percentage ratio against the standard pulse amplitude if needed. For different pulse shapes, the value of SCAL[5:0] bits and the scaling percentage ratio are different. The following two tables list these values.

Do the followings step by step, the desired waveform can be programmed, based on the selected waveform template:

(1).Select the UI by UI[1:0] bits (**TCF3, 08H**)

(2).Specify the sample address in the selected UI by SAMP [3:0] bits (**TCF3, 08H**)

(3).Write sample data to WDAT[6:0] bits (**TCF4, 09H**). It contains the data to be stored in the RAM, addressed by the selected UI and the corresponding sample address.

(4).Set the RW bit (**TCF3, 08H**) to '0' to implement writing data to RAM, or to '1' to implement read data from RAM

(5).Implement the Read from RAM/Write to RAM by setting the DONE bit (**TCF3, 08H**)

Repeat the above steps until all the sample data are written to or read from the internal RAM.

(6).Write the scaling data to SCAL[5:0] bits (**TCF2, 07H**) to scale the amplitude of the waveform based on the selected standard pulse amplitude

When more than one UI is used to compose the pulse template, the overlap of two consecutive pulses could make the pulse amplitude overflow (exceed the maximum limitation) if the pulse amplitude is not set properly. This overflow is captured by DAC_OV_IS bit (**INTS1, 1AH**), and, if enabled by the DAC_OV_IM bit (**INTM1, 15H**), an interrupt will be generated.

The following tables give all the sample data based on the preset pulse templates in detail for reference. For preset pulse templates, scaling up/down against the pulse amplitude is not supported.

1.Table-2 Transmit Waveform Value For E1 75 Ω

2.Table-3 Transmit Waveform Value For E1 120 Ω

Table-2 Transmit Waveform Value For E1 75 ohm

Sample	UI 1	UI 2	UI 3	UI 4
1	0000000	0000000	0000000	0000000
2	0000000	0000000	0000000	0000000
3	0000000	0000000	0000000	0000000
4	0001100	0000000	0000000	0000000
5	0110000	0000000	0000000	0000000
6	0110000	0000000	0000000	0000000
7	0110000	0000000	0000000	0000000
8	0110000	0000000	0000000	0000000
9	0110000	0000000	0000000	0000000
10	0110000	0000000	0000000	0000000
11	0110000	0000000	0000000	0000000
12	0110000	0000000	0000000	0000000
13	0000000	0000000	0000000	0000000
14	0000000	0000000	0000000	0000000
15	0000000	0000000	0000000	0000000
16	0000000	0000000	0000000	0000000
SCAL[5:0] = 100001 (default), One step change of this value of SCAL[5:0] results in 3% scaling up/down against the pulse amplitude.				

Table-3 Transmit Waveform Value For E1 120 ohm

Sample	UI 1	UI 2	UI 3	UI 4
1	0000000	0000000	0000000	0000000
2	0000000	0000000	0000000	0000000
3	0000000	0000000	0000000	0000000
4	0001111	0000000	0000000	0000000
5	0111100	0000000	0000000	0000000
6	0111100	0000000	0000000	0000000
7	0111100	0000000	0000000	0000000
8	0111100	0000000	0000000	0000000
9	0111100	0000000	0000000	0000000
10	0111100	0000000	0000000	0000000
11	0111100	0000000	0000000	0000000
12	0111100	0000000	0000000	0000000
13	0000000	0000000	0000000	0000000
14	0000000	0000000	0000000	0000000
15	0000000	0000000	0000000	0000000
16	0000000	0000000	0000000	0000000
SCAL[5:0] = 100001 (default), One step change of this value of SCAL[5:0] results in 3% scaling up/down against the pulse amplitude.				

© 2019 Renesas Electronics Corporation

3.2.4 TRANSMIT PATH LINE INTERFACE

The transmit line interface consists of TTIP pin and TRING pin. The impedance matching can be realized by the internal impedance matching circuit or the external impedance matching circuit. If T_TERM[2] is set to '0', the internal impedance matching circuit will be selected. In this case, the T_TERM[1:0] bits (**TERM, 03H**) can be set to choose 75 Ω or 120 Ω internal impedance of TTIP/TRING. If T_TERM[2] is set to '1', the internal impedance matching circuit will be disabled. In this case, the external impedance matching circuit will be used to realize the impedance matching. Figure-6 shows the appropriate external components to connect with the cable. Table-4 is the list of the recommended impedance matching for transmitter.

In hardware control mode, TERM pin can be used to select impedance matching for both receiver and transmitter. If TERM pin is low, external impedance network will be used for impedance matching. If TERM pin is high, internal impedance will be used for impedance matching and PULS pin will be set to select the specific internal impedance. Refer to 5 Hardware Control Pin Summary for details.

The TTIP/TRING pins can also be turned into high impedance by setting the THZ bit (**TCF1, 06H**) to '1'. In this state, the internal transmit circuits are still active.

In hardware control mode, TTIP/TRING can be turned into high impedance by pulling THZ pin to high. Refer to 5 Hardware Control Pin Summary for details.

Besides, in the following cases, both TTIP/TRING pins will also become high impedance:

- Loss of MCLK;
- Loss of TCLK (exceptions: Remote Loopback; Transmit internal pattern by MCLK);
- Transmit path power down;
- After software reset; pin reset and power on.

Table-4 Impedance Matching for Transmitter

Cable Configuration	Internal Termination			External Termination		
	T_TERM[2:0]	PULS[3:0]	R_T	T_TERM[2:0]	PULS[3:0]	R_T
E1 / 75 Ω	000	0000	0 Ω	1XX	0001	9.4 Ω
E1 / 120 Ω	001	0001				

Note: The precision of the resistors should be better than ± 1%

3.2.5 TRANSMIT PATH POWER DOWN

The transmit path can be powered down by setting the T_OFF bit (**TCF0, 05H**) to '1'. In this case, the TTIP/TRING pins are turned into high impedance.

In hardware control mode, the transmit path can be powered down by pulling both PATT1 and PATT0 pins to high. Refer to 5 Hardware Control Pin Summary for details.

© 2019 Renesas Electronics Corporation

3.3 RECEIVE PATH

The receive path consists of Receive Internal Termination, Monitor Gain, Amplitude/Wave Shape Detector, Digital Tuning Controller, Adaptive Equalizer, Data Slicer, CDR (Clock & Data Recovery), Optional Jitter Attenuator, Decoder and LOS/AIS Detector. Refer to Figure-5.

3.3.1 RECEIVE INTERNAL TERMINATION

The impedance matching can be realized by the internal impedance matching circuit or the external impedance matching circuit. If R_TERM[2] is set to '0', the internal impedance matching circuit will be selected. In this case, the R_TERM[1:0] bits (**TERM, 03H**) can be set to choose 75 Ω or 120 Ω internal impedance of RTIP/RRING. If R_TERM[2] is set to '1', the internal impedance matching circuit will be disabled. In this case, the external impedance matching circuit will be used to realize the impedance matching. Figure-6 shows the appropriate external components to connect with the cable. Table-5 is the list of the recommended impedance matching for receiver.

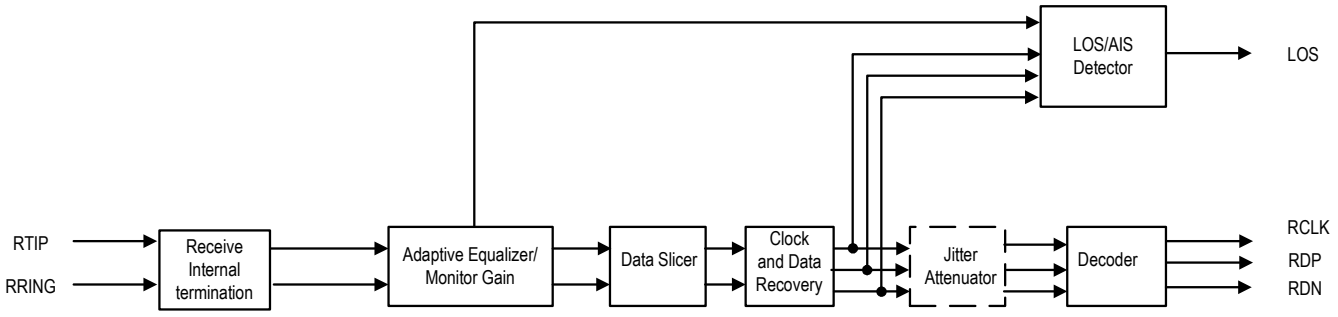
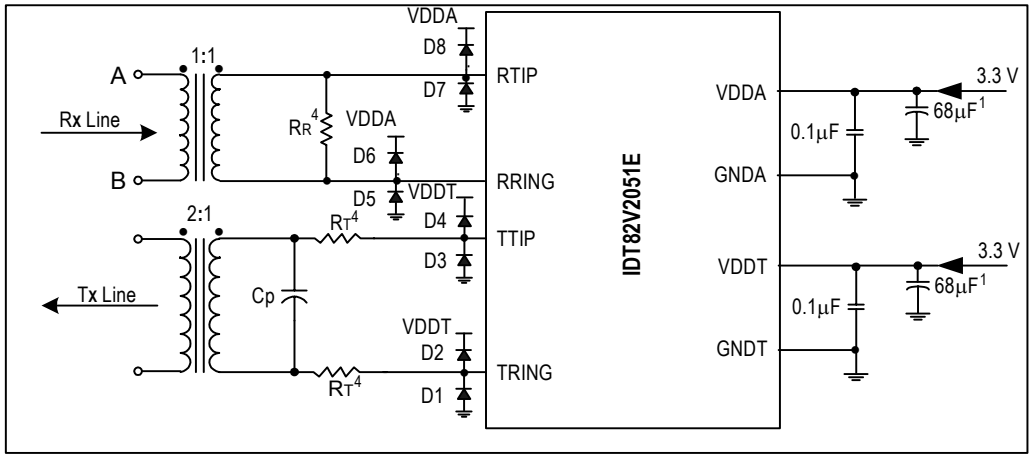


Figure-5 Receive Monitor Gain Adaptive Equalizer

Table-5 Impedance Matching for Receiver

Cable Configuration	Internal Termination		External Termination	
	R_TERM[2:0]	R_R	R_TERM[2:0]	R_R
E1/75 Ω	000	120 Ω	1XX	75 Ω
E1/120 Ω	001			120 Ω



Note: 1. Common decoupling capacitor, one per chip
2. Cp 0-560 (pF)
3. D1 - D8, Motorola - MBR0540T1; International Rectifier - 11DQ04 or 10BQ060
4. R_T/ R_R: refer toTable-4 and Table-5 respecivley for R_T and R_R values

Figure-6 Transmit/Receive Line Circuit

© 2019 Renesas Electronics Corporation

In hardware control mode, TERM and PULS pins can be used to select impedance matching for both receiver and transmitter. If TERM pin is low, external impedance network will be used for impedance matching. If TERM pin is high, internal impedance will be used for impedance matching and PULS pins can be set to select the specific internal impedance. Refer to 5 Hardware Control Pin Summary for details.

3.3.2 LINE MONITOR

The non-intrusive monitoring on channels located in other chips can be performed by tapping the monitored channel through a high impedance bridging circuit. Refer to Figure-7 and Figure-9.

After a high resistance bridging circuit, the signal arriving at the RTIP/ RRING is dramatically attenuated. To compensate this attenuation, the Monitor Gain can be used to boost the signal by 22 dB, 26 dB and 32 dB, selected by MG[1:0] bits (**RCF2, 0CH**). For normal operation, the Monitor Gain should be set to 0 dB.

In hardware control mode, MONT pin can be used to set the Monitor Gain. When MONT pin is low, the Monitor Gain is 0 dB. When MONT pin is high, the Monitor Gain is 26 dB. Refer to 5 Hardware Control Pin Summary for details.

Note that LOS indication is not supported if the device is operated in Line Monitor Mode

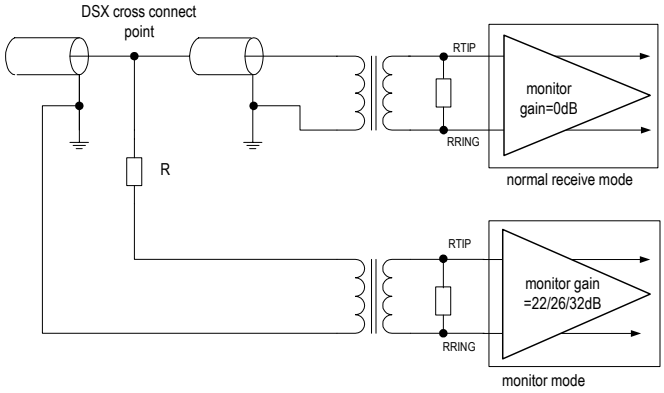


Figure-7 Monitoring Receive Line in Another Chip

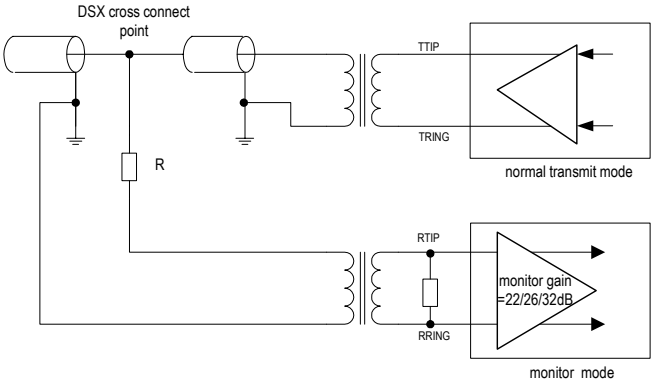


Figure-8 Monitor Transmit Line in Another Chip

© 2019 Renesas Electronics Corporation

3.3.3 ADAPTIVE EQUALIZER

The Adaptive Equalizer can be enabled to increase the receive sensitivity and to allow programming of the LOS level up to -24 dB. See3.5 Los And AIS Detection. It can be enabled or disabled by setting EQ_ON bit to '1' or '0' (**RCF1, 0BH**).

3.3.4 RECEIVE SENSITIVITY

The Receive Sensitivity is -10 dB. With the Adaptive Equalizer enabled, the receive sensitivity will be -20 dB.

In Hardware mode, the Adaptive Equalizer can not be enabled and the receive sensitivity is fixed at -10 dB. Refer to 5 Hardware Control Pin Summary for details.

3.3.5 DATA SLICER

The Data Slicer is used to generate a standard amplitude mark or a space according to the amplitude of the input signals. The threshold can be 40%, 50%, 60% or 70%, as selected by the SLICE[1:0] bits (**RCF2, 0CH**). The output of the Data Slicer is forwarded to the CDR (Clock & Data Recovery) unit or to the RDP/RDN pins directly if the CDR is disabled.

3.3.6 CDR (CLOCK & DATA RECOVERY)

The CDR is used to recover the clock and data from the received signal. The recovered clock tracks the jitter in the data output from the Data Slicer and keeps the phase relationship between data and clock during the absence of the incoming pulse. The CDR can also be by-passed in the Dual Rail mode. When CDR is by-passed, the data from the Data Slicer is output to the RDP/RDN pins directly.

3.3.7 DECODER

The R_MD[1:0] bits (**RCF0, 0AH**) are used to select the AMI decoder or HDB3 decoder.

When the chip is configured by hardware, the operation mode of receive and transmit path can be selected by setting RXTXM1 and RXTXM0 pins. Refer to 5 Hardware Control Pin Summary for details.

© 2019 Renesas Electronics Corporation

3.3.8 RECEIVE PATH SYSTEM INTERFACE

The receive path system interface consists of RCLK pin, RD/RDP pin and RDN pin. The RCLK outputs a recovered 2.048 MHz clock. The received data is updated on the RD/RDP and RDN pins on the active edge of RCLK. The active edge of RCLK can be selected by the RCLK_SEL bit (**RCF0, 0AH**). And the active level of the data on RD/RDP and RDN can be selected by the RD_INV bit (**RCF0, 0AH**).

In hardware control mode, only the active edge of RCLK can be selected. If RCLKE is set to high, the falling edge will be chosen as the active edge of RCLK. If RCLKE is set to low, the rising edge will be chosen as the active edge of RCLK. The active level of the data on RD/RDP and RDN is the same as that in software control mode.

The received data can be output to the system side in two different ways: Single Rail or Dual Rail, as selected by R_MD bit [1] (**RCF0, 0AH**). In Single Rail mode, only RD pin is used to output data and the RDN/CV pin is used to report the received errors. In Dual Rail Mode, both RDP pin and RDN pin are used for outputting data.

In the receive Dual Rail mode, the CDR unit can be by-passed by setting R_MD[1:0] to '11' (binary). In this situation, the output data from the Data Slicer will be output to the RDP/RDN pins directly, and the RCLK outputs the exclusive OR (XOR) of the RDP and RDN. This is called receiver slicer mode. In this case, the transmit path is still operating in Dual Rail mode.

3.3.9 RECEIVE PATH POWER DOWN

The receive path can be powered down by setting R_OFF bit (**RCF0, 0AH**) to '1'. In this case, the RCLK, RD/RDP, RDN and LOS will be logic low.

In hardware control mode, receiver power down can be selected by pulling RPD pin to high. Refer to 5 Hardware Control Pin Summary for more details.

3.4 JITTER ATTENUATOR

There is one Jitter Attenuator in the IDT82V2051E. The Jitter Attenuator can be deployed in the transmit path or the receive path, and can also be disabled. This is selected by the JACF[1:0] bits (**JACF, 04H**).

In hardware control mode, Jitter Attenuator position, bandwidth and the depth of FIFO can be selected by JA[1:0] pins. Refer to 5 Hardware Control Pin Summary for details.

3.4.1 JITTER ATTENUATION FUNCTION DESCRIPTON

The Jitter Attenuator is composed of a FIFO and a DPLL, as shown in Figure-9. The FIFO is used as a pool to buffer the jittered input data, then the data is clocked out of the FIFO by a de-jittered clock. The depth of the FIFO can be 32 bits, 64 bits or 128 bits, as selected by the JADP[1:0] bits (**JACF, 04H**). In hardware control mode, the depth of FIFO can be selected by JA[1:0] pins. Refer to 5 Hardware Control Pin Summary for details. Consequently, the constant delay of the Jitter Attenuator will be 16 bits, 32 bits or 64 bits. Deeper FIFO can tolerate larger jitter, but at the cost of increasing data latency time.

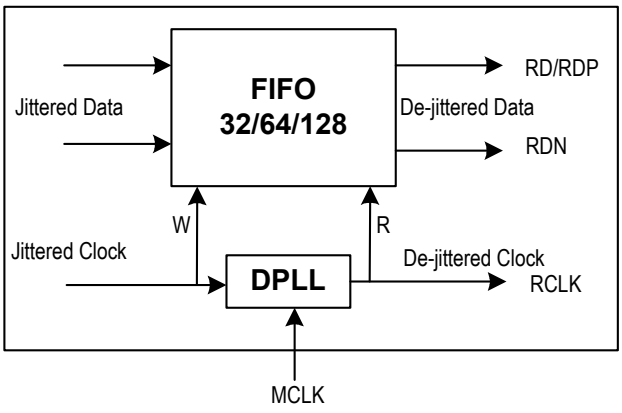


Figure-9 Jitter Attenuator

The Corner Frequency of the DPLL can be 0.9 Hz or 6.8 Hz, as selected by the JABW bit (**JACF, 04H**). The lower the Corner Frequency is, the longer time is needed to achieve synchronization.

When the incoming data moves faster than the outgoing data, the FIFO will overflow. This overflow is captured by the JAOV_IS bit (**INTS1, 1AH**). If the incoming data moves slower than the outgoing data, the FIFO will underflow. This underflow is captured by the JAUD_IS bit (**INTS1, 1AH**). For some applications that are sensitive to data corruption, the JA limit mode can be enabled by setting JA_LIMIT bit (**JACF, 04H**) to '1'. In the JA limit mode, the speed of the outgoing data will be adjusted automatically when the FIFO is close to its full or emptiness. The criteria of starting speed adjustment are shown in Table-6. The JA limit mode can reduce the possibility of FIFO overflow and underflow, but the quality of jitter attenuation is deteriorated.

© 2019 Renesas Electronics Corporation

Table-6 Criteria of Starting Speed Adjustment

FIFO Depth	Criteria for Adjusting Data Outgoing Speed
32 Bits	2 bits close to its full or emptiness
64 Bits	3 bits close to its full or emptiness
128 Bits	4 bits close to its full or emptiness

3.4.2 JITTER ATTENUATOR PERFORMANCE

The performance of the Jitter Attenuator in the IDT82V2051E meets the ITU-T I.431, G.703, G.736-739, G.823, G.824, ETSI 300011 and ETSI TBR12/13 specifications. Details of the Jitter Attenuator performance is shown in Table-47 Jitter Tolerance and Table-48 Jitter Attenuator Characteristics.

3.5 LOS AND AIS DETECTION

3.5.1 LOS DETECTION

The Loss of Signal Detector monitors the amplitude of the incoming signal level and pulse density of the received signal on RTIP and RRING.

- **LOS declare (LOS=1)**

A LOS is detected when the incoming signal has “no transitions”, i.e., when the signal level is less than Q dB below nominal for N consecutive pulse intervals. Here N is defined by LAC bit (**MAINT0, 0DH**). LOS will be declared by pulling LOS pin to high (LOS=1) and LOS interrupt will be generated if it is not masked.

Note that LOS indication is not supported if the device is operated in Line Monitor Mode. Refer to 3.3.2 Line Monitor.

- **LOS clear (LOS=0)**

The LOS is cleared when the incoming signal has “transitions”, i.e., when the signal level is greater than P dB below nominal and has an average pulse density of at least 12.5% for M consecutive pulse intervals, starting with the receipt of a pulse. Here M is defined by LAC bit (**MAINT0, 0DH**). LOS status is cleared by pulling LOS pin to low.

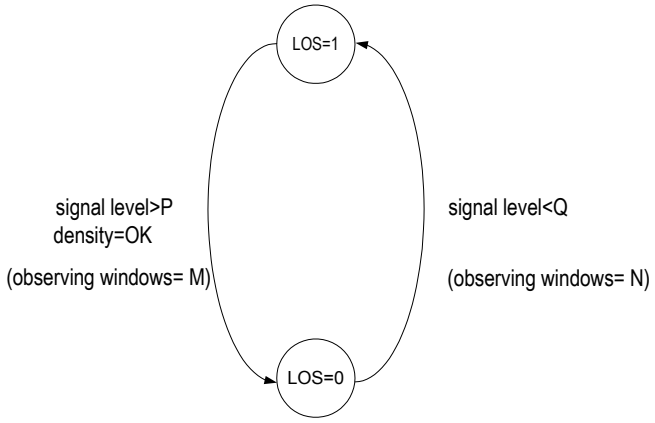


Figure-10 LOS Declare and Clear

- **LOS detect level threshold**

With the Adaptive Equalizer off, the amplitude threshold Q is fixed on 800 mVpp, while P=Q+200 mVpp (200 mVpp is the LOS level detect hysteresis).

With the Adaptive Equalizer on, the value of Q can be selected by LOS[4:0] bit (**RCF1, 0BH**), while P=Q+4 dB (4 dB is the LOS level detect hysteresis). Refer to Table-20 TCF1: Transmitter Configuration Register 1 for LOS[4:0] bit values available.

When the chip is configured by hardware, the Adaptive Equalizer can not be enabled and Programmable LOS levels are not available (pin 29 has to be set to ‘0’).

- **Criteria for declare and clear of a LOS detect**

The detection supports G.775 and ETSI 300233/I.431. The criteria can be selected by LAC bit (**MAINT0, 0DH**).

Table-7 and Table-8 summarize LOS declare and clear criteria for both with and without the Adaptive Equalizer enabled.

- **All Ones output during LOS**

On the system side, the RDP/RDN will reflect the input pulse “transition” at the RTIP/RRING side and output recovered clock (but the quality of the output clock can not be guaranteed when the input level is lower than the maximum receive sensitivity) when AISE bit (**MAINT0, 0DH**) is 0; or output All Ones as AIS when AISE bit (**MAINT0, 0DH**) is 1. In this case, RCLK output is replaced by MCLK.

On the line side, the TTIP/TRING will output All Ones as AIS when ATAO bit (**MAINT0, 0DH**) is 1. The All Ones pattern uses MCLK as the reference clock.

LOS indicator is always active for all kinds of loopback modes.

Table-7 LOS Declare and Clear Criteria, Adaptive Equalizer Disabled

Control bit (LAC)	LOS declare threshold	LOS clear threshold
0 = G.775	Level < 800 mVpp; N=32 bits	Level > 1 Vpp; M=32 bits; 12.5% mark density; <16 consecutive zeroes
1 = I.431/ETSI	Level < 800 mVpp; N=2048 bits	Level > 1 Vpp; M=32 bits; 12.5% mark density; <16 consecutive zeroes

© 2019 Renesas Electronics Corporation

Table-8 LOS Declare and Clear Criteria, Adaptive Equalizer Enabled

Control bit				LOS declare threshold	LOS clear threshold	Note
LAC		LOS[4:0]	Q (dB)			
0	-	00000 … 00010	-4 … -8	Level < Q N=32 bits	Level > Q+ 4 dB M=32 bits 12.5% mark density <16 consecutive zeroes	G.775 Level detect range is -9 to -35 dB.
	G.775	00011 … 01010 01011 - 11111	-10 … -24 Reserved			
1	-	00000	-4	Level < Q N=2048 bits	Level > Q+ 4 dB M=32 bits 12.5% mark density <16 consecutive zeroes	I.431 Level detect range is -6 to -20 dB.
	I.431/ETSI	00001 … 01010 01011 - 11111	-6 … -24 Reserved			

3.5.2 AIS DETECTION

The Alarm Indication Signal can be detected by the IDT82V2051E when the Clock & Data Recovery unit is enabled. The status of AIS detection is reflected in the AIS_S bit (**STAT0, 17H)**. The criteria for declaring/clearing AIS detection comply with the ITU G.775 or the ETSI 300233, as selected by the LAC bit (**MAINT0, 0DH**). Table-9 summarizes different criteria for AIS detection Declaring/Clearing.

Table-9 AIS Condition

	ITU G.775 (LAC bit is set to '0' by default)	ETSI 300233 (LAC bit is set to '1')
AIS detected	Less than 3 zeros contained in each of two consecutive 512-bit streams are received	Less than 3 zeros contained in a 512-bit stream are received
AIS cleared	3 or more zeros contained in each of two consecutive 512-bit streams are received	3 or more zeros contained in a 512-bit stream are received

© 2019 Renesas Electronics Corporation

3.6 TRANSMIT AND DETECT INTERNAL PATTERNS

The internal patterns (All Ones, All Zeros and PRBS pattern) will be generated and detected by IDT82V2051E. TCLK is used as the reference clock by default. MCLK can also be used as the reference clock by setting the PATT_CLK bit (**MAINT0, 0DH**) to '1'.

If the PATT_CLK bit (**MAINT0, 0DH**) is set to '0' and the PATT[1:0] bits (**MAINT0, 0DH**) are set to '00', the transmit path will operate in normal mode.

When the chip is configured by hardware, the transmit path will operate in normal mode by setting PATT[1:0] pins to '00'. Refer to 5 Hardware Control Pin Summary for details.

3.6.1 TRANSMIT ALL ONES

In transmit direction, the All Ones data can be inserted into the data stream when the PATT[1:0] bits (**MAINT0, 0DH**) are set to '01'. The transmit data stream is output from TTIP/TRING. In this case, either TCLK or MCLK can be used as the transmit clock, as selected by the PATT_CLK bit (**MAINT0, 0DH**).

In hardware control mode, the All Ones data can be inserted into the data stream in transmit direction by setting PATT[1:0] pins to '01'. Refer to 5 Hardware Control Pin Summary for details.

3.6.2 TRANSMIT ALL ZEROS

If the PATT_CLK bit (**MAINT0, 0DH**) is set to '1', the All Zeros will be inserted into the transmit data stream when the PATT[1:0] bits (**MAINT0, 0DH**) are set to '00'.

3.6.3 PRBS GENERATION AND DETECTION

A PRBS will be generated in the transmit direction and detected in the receive direction by IDT82V2051E. The PRBS is 2^{15}-1, with maximum zero restrictions according to ITU-T O.151.

When the PATT[1:0] bits (**MAINT0, 0DH**) are set to '10', the PRBS pattern will be inserted into the transmit data stream with the MSB first. The PRBS pattern will be transmitted directly or invertedly.

In hardware control mode, the PRBS data will be generated in the transmit direction and inserted into the transmit data stream by setting PATT[1:0] pins to '10'. Refer to 5 Hardware Control Pin Summary for details.

The PRBS in the received data stream will be monitored. If the PRBS has reached synchronization status, the PRBS_S bit (**STAT0, 17H**) will be set to '1', even in the presence of a logic error rate less than or equal to 10^{-1}. The criteria for setting/clearing the PRBS_S bit are shown in Table-10.

Table-10 Criteria for Setting/Clearing the PRBS_S Bit

PRBS Detection	6 or less than 6 bit errors detected in a 64 bits hopping window.
PRBS Missing	More than 6 bit errors detected in a 64 bits hopping window.

PRBS data can be inverted through setting the PRBS_INV bit (**MAINT0, 0DH)**.

Any change of PRBS_S bit will be captured by PRBS_IS bit (**INTS0, 19H**). The PRBS_IES bit (**INTES, 16H**) can be used to determine whether the '0' to '1' change of PRBS_S bit will be captured by the PRBS_IS bit or any changes of PRBS_S bit will be captured by the PRBS_IS bit. When the PRBS_IS bit is '1', an interrupt will be generated if the PRBS_IM bit (**INTM0, 14H**) is set to '1'.

The received PRBS logic errors can be counted in a 16-bit counter if the ERR_SEL [1:0] bits (**MAINT6, 13H**) are set to '00'. Refer to 3.8 Error Detection/Counting And Insertion for the operation of the error counter.

3.7 LOOPBACK

To facilitate testing and diagnosis, the IDT82V2051E provides three different loopback configurations: Analog Loopback, Digital Loopback and Remote Loopback.

3.7.1 ANALOG LOOPBACK

When the ALP bit (**MAINT1, 0EH**) is set to '1', the chip is configured in Analog Loopback mode. In this mode, the transmit signals are looped back to the Receiver Internal Termination in the receive path then output from RCLK, RD, RDP/RDN. At the same time, the transmit signals are still output to TTIP/TRING in transmit direction. The all-ones pattern can be generated during analog loopback. Figure-11 shows the process.

3.7.2 DIGITAL LOOPBACK

When the DLP bit (**MAINT1, 0EH**) is set to '1', the chip is configured in Digital Loopback mode. In this mode, the transmit signals are looped back to the jitter attenuator (if enabled) and decoder in receive path, then output from RCLK, RD, RDP/RDN. At the same time, the transmit signals are still output to TTIP/TRING in transmit direction. Figure-12 shows the process.

Both Analog Loopback mode and Digital Loopback mode allow the sending of the internal patterns (All Ones, All Zeros, PRBS, etc.) which will overwrite the transmit signals. In this case, either TCLK or MCLK can be used as the reference clock for internal patterns transmission.

In hardware control mode, Digital Loopback can be selected by setting LP[1:0] pins to '10'.

3.7.3 REMOTE LOOPBACK

When the RLP bit (**MAINT1, 0EH**) is set to '1', the chip is configured in Remote Loopback mode. In this mode, the recovered clock and data output from Clock and Data Recovery on the receive path is looped back to the jitter attenuator (if enabled) and Waveform Shaper in transmit path. Figure-13 shows the process.

In hardware control mode, Remote Loopback can be selected by setting LP[1:0] pins to '11'.

© 2019 Renesas Electronics Corporation

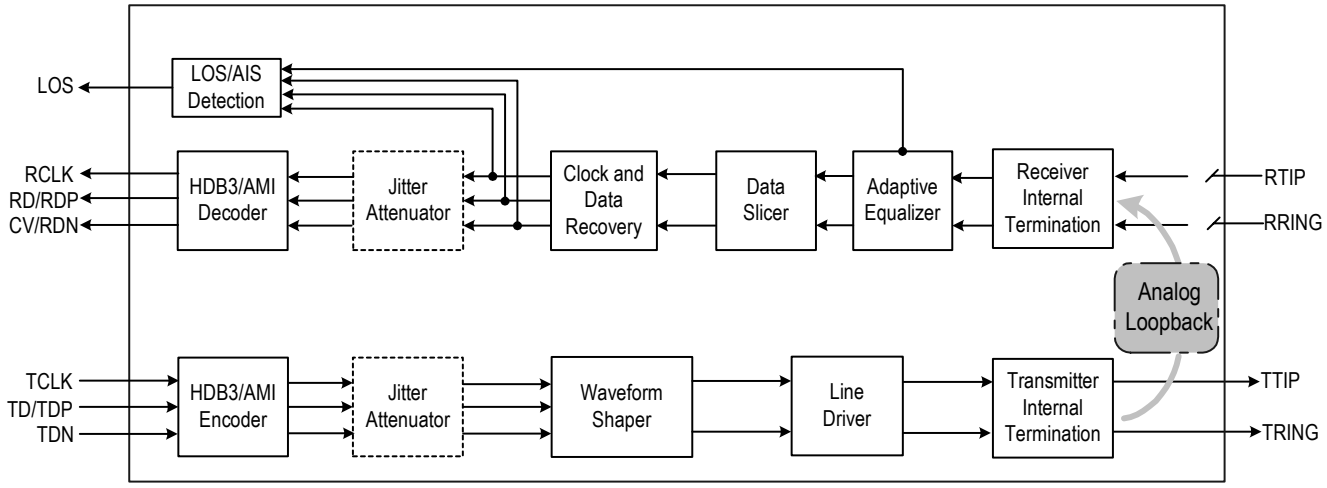


Figure-11 Analog Loopback

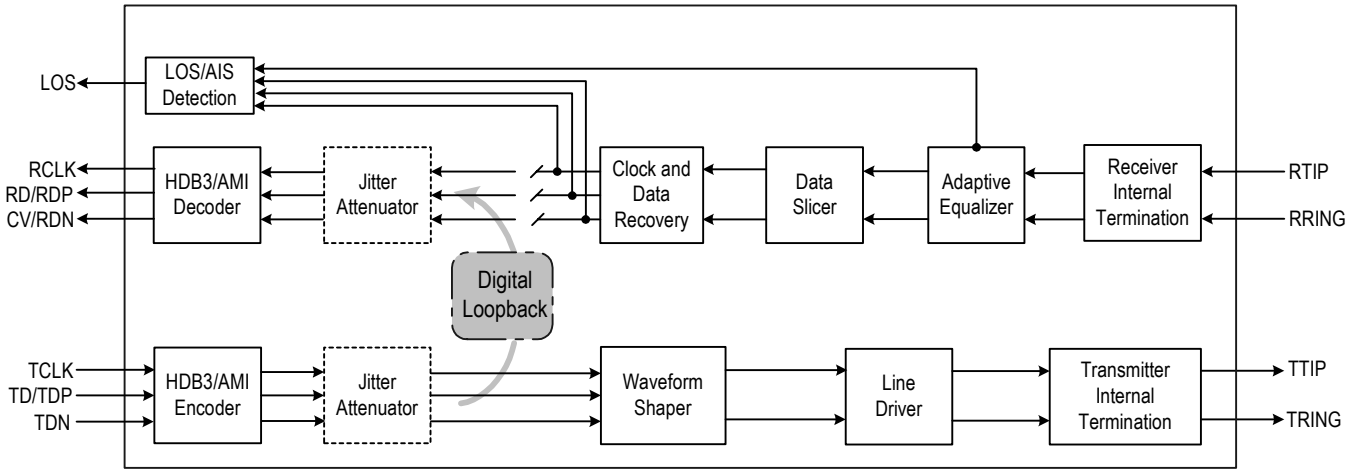


Figure-12 Digital Loopback

© 2019 Renesas Electronics Corporation

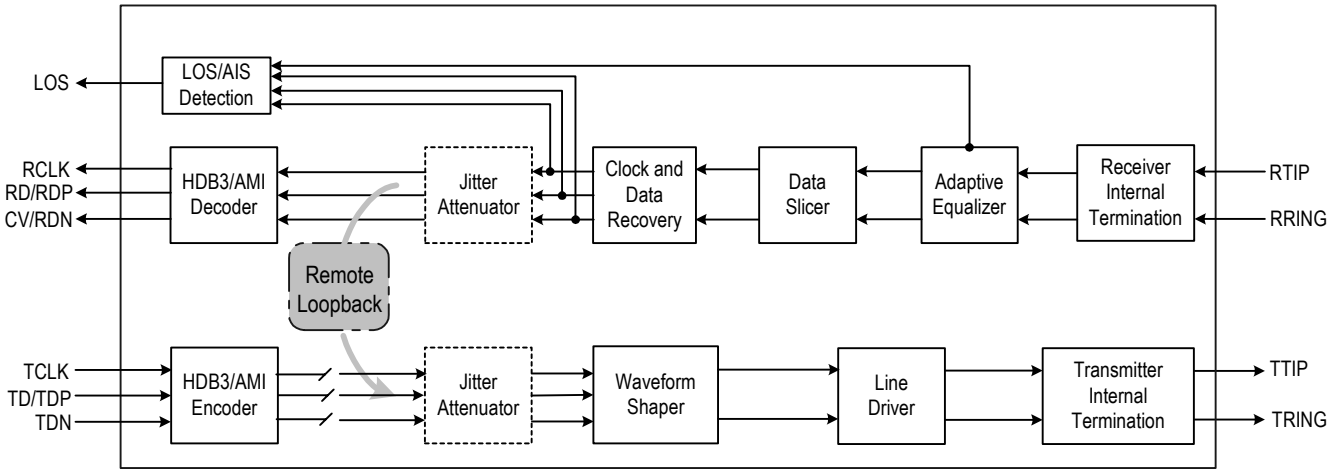


Figure-13 Remote Loopback

© 2019 Renesas Electronics Corporation

3.8 ERROR DETECTION/COUNTING AND INSERTION

3.8.1 DEFINITION OF LINE CODING ERROR

The following line encoding errors can be detected and counted by the IDT82V2051E:

- Received Bipolar Violation (BPV) Error: In AMI coding, when two consecutive pulses of the same polarity are received, a BPV error is declared.
- HDB3 Code Violation (CV) Error: In HDB3 coding, a CV error is declared when two consecutive BPV errors are detected, and the pulses that have the same polarity as the previous pulse are not the HDB3 zero substitution pulses.
- Excess Zero (EXZ) Error: There are two standards defining the EXZ errors: ANSI and FCC. The EXZ_DEF bit (**MAINT6, 13H**) chooses which standard will be adopted by the chip to judge the EXZ error. Table-11 shows definition of EXZ. In hardware control mode, only ANSI standard is adopted.

Table-11 EXZ Definition

	EXZ Definition	
	ANSI	**FCC**
AMI	More than 15 consecutive 0s are detected	More than 80 consecutive 0s are detected
HDB3	More than 3 consecutive 0s are detected	More than 3 consecutive 0s are detected

3.8.2 ERROR DETECTION AND COUNTING

Which type of the receiving errors (Received CV/BPV errors, excess zero errors and PRBS logic errors) will be counted is determined by ERR_SEL[1:0] bits (**MAINT6, 13H**). Only one type of receiving error can be counted at a time except that when the ERR_SEL[1:0] bits are set to '11', both CV/BPV and EXZ errors will be detected and counted.

The selected type of receiving errors is counted in an internal 16-bit Error Counter. Once an error is detected, an error interrupt which is indicated by corresponding bit in (**INTS1, 1AH**) will be generated if it is not masked. This Error Counter can be operated in two modes: Auto Report Mode and Manual Report Mode, as selected by the CNT_MD bit (**MAINT6, 13H**). In Single Rail mode, once BPV or CV errors are detected, the CV pin will be driven to high for one RCLK period.

- **Auto Report Mode**

In Auto Report Mode, the internal counter starts to count the received errors when the CNT_MD bit (**MAINT6, 13H**) is set to '1'. A one-second timer is used to set the counting period. The received errors are counted within one second. If the one-second timer expires, the value in the internal counter will be transferred to (**CNT0, 1BH**) and (**CNT1, 1CH**), then the internal counter will be reset and start to count received errors for the next second. The errors occurred during the transfer will be accumulated to the next round. The expiration of the one-second timer will set TMOV_IS bit (**INTS1, 1AH**) to '1', and will generate an interrupt if the TIMER_IM bit (**INTM1, 15H**) is set to '0'. The TMOV_IS bit (**INTS1, 1AH**) will be cleared after the interrupt register is read. The content in the (**CNT0, 1BH**) and (**CNT1, 1CH**) should be read within the next second. If the counter overflows, a counter overflow interrupt which is indicated by CNT_OV_IS bit (**INTS1, 1AH**) will be generated if it is not masked by CNT_IM bit (**INTM1, 15H**).

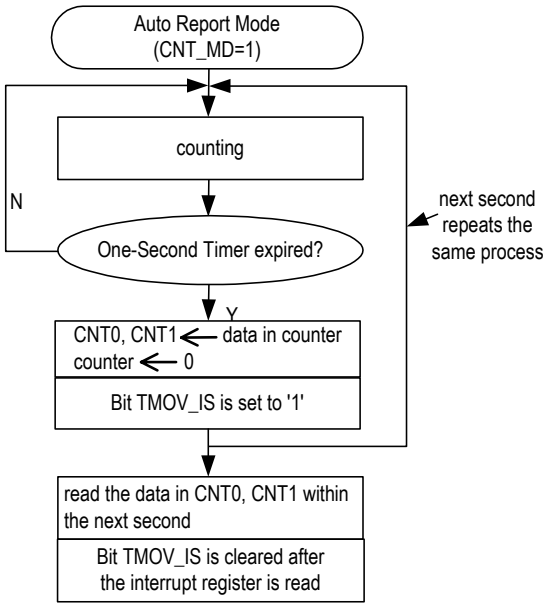


Figure-14 Auto Report Mode

© 2019 Renesas Electronics Corporation

• Manual Report Mode

In Manual Report Mode, the internal Error Counter starts to count the received errors when the CNT_MD bit **(MAINT6, 13H)** is set to '0'. When there is a '0' to '1' transition on the CNT_TRF bit **(MAINT6, 13H)**, the data in the counter will be transferred to **(CNT0, 1BH)** and **(CNT1, 1CH)**, then the counter will be reset. The errors occurred during the transfer will be accumulated to the next round. If the counter overflows, a counter overflow interrupt indicated by CNT_OV_IS bit **(INTS1, 1AH)** will be generated if it is not masked by CNT_IM bit **(INTM1, 15H)**.

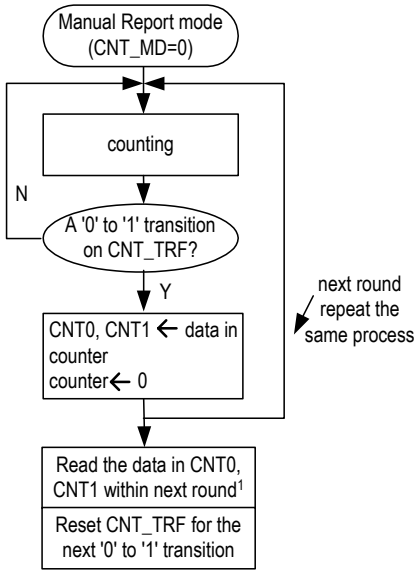


Figure-15 Manual Report Mode

Note: It is recommended that users should do the followings within next round of error counting: Read the data in CNT0 and CNT1; Reset CNT_TRF bit for the next '0' to '1' transition on this bit.

3.8.3 BIPOLAR VIOLATION AND PRBS ERROR INSERTION

Only when three consecutive '1's are detected in the transmit data stream, will a '0' to '1' transition on the BPV_INS bit (**MAINT6, 13H**) generate a bipolar violation pulse, and the polarity of the second '1' in the series will be inverted.

A '0' to '1' transition on the EER_INS bit (**MAINT6, 13H**) will generate a logic error during the PRBS transmission.

3.9 LINE DRIVER FAILURE MONITORING

The transmit driver failure monitor can be enabled or disabled by setting DFM_OFF bit (**TCF1, 06H**). If the transmit driver failure monitor is enabled, the transmit driver failure will be captured by DF_S bit (**STAT0, 17H**). The transition of the DF_S bit is reflected by DF_IS bit (**INTS0, 19H**), and, if enabled by DF_IM bit (**INTM0, 14H**), will generate an interrupt. When there is a short circuit on the TTIP/TRING port, the output current will be limited to 100 mA (typical), and an interrupt will be generated.

In hardware control mode, the transmit driver failure monitor is always enabled.

© 2019 Renesas Electronics Corporation

3.10 MCLK AND TCLK

3.10.1 MASTER CLOCK (MCLK)

MCLK is an independent, free-running reference clock. MCLK is 2.048 MHz. This reference clock is used to generate several internal reference signals:

- Timing reference for the integrated clock recovery unit.
- Timing reference for the integrated digital jitter attenuator.
- Timing reference for microcontroller interface.
- Generation of RCLK signal during a loss of signal condition if AIS is enabled.
- Reference clock during Transmit All Ones, All Zeros and PRBS pattern if it is selected as the reference clock. For ATAO and AIS, MCLK is always used as the reference clock.
- Reference clock during Transmit All Ones (TAO) condition or sending PRBS in hardware control mode.

Figure-16 shows the chip operation status in different conditions of MCLK and TCLK. The missing of MCLK will set the TTIP/TRING to high impedance state.

3.10.2 TRANSMIT CLOCK (TCLK)

TCLK is used to sample the transmit data on TD/TDP and TDN. The active edge of TCLK can be selected by the TCLK_SEL bit (**TCF0, 05H**). During Transmit All Ones or PRBS patterns, either TCLK or MCLK can be used as the reference clock. This is selected by the PATT_CLK bit (**MAINT0, 0DH**).

But for Automatic Transmit All Ones and AIS, only MCLK is used as the reference clock and the PATT_CLK bit is ignored. In Automatic Transmit All Ones condition, the ATAO bit (**MAINT0, 0DH**) is set to '1'. In AIS condition, the AISE bit (**MAINT0, 0DH**) is set to '1'.

If TCLK has been missing for more than 70 MCLK cycles, TCLK_LOS bit (**STAT0, 17H**) will be set, and the TTIP/TRING will become high impedance if the chip is not used for remote loopback or is not using MCLK to transmit internal patterns (TAOS, All Zeros and PRBS). When TCLK is detected again, TCLK_LOS bit (**STAT0, 17H**) will be cleared. The reference frequency to detect a TCLK loss is derived from MCLK.

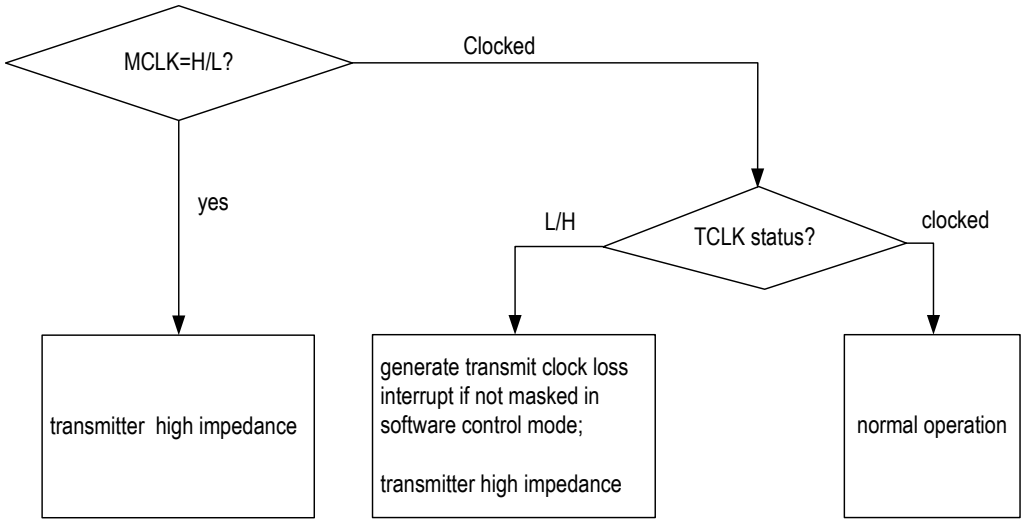


Figure-16 TCLK Operation Flowchart

© 2019 Renesas Electronics Corporation

3.11 MICROCONTROLLER INTERFACES

The microcontroller interface provides access to read and write the registers in the device. The chip supports serial microcontroller interface and two kinds of parallel microcontroller interface: Motorola multiplexed mode and Intel multiplexed mode. Different microcontroller interfaces can be selected by setting MODE[1:0] pins to different values. Refer to MODE1 and MODE0 in pin description and Microcontroller Interface Timing Characteristics for details.

3.11.1 PARALLEL MICROCONTROLLER INTERFACE

The interface is compatible with Motorola or Intel microcontroller. When MODE[1:0] pins are set to '10', Parallel-Multiplexed-Motorola interface is selected. When MODE[1:0] pins are set to '11', Parallel-Multiplexed-Intel Interface is selected.

3.11.2 SERIAL MICROCONTROLLER INTERFACE

When MODE[1:0] pins are set to '01', Serial Interface is selected. In this mode, the registers are programmed through a 16-bit word which contains an 8-bit address/command byte (5 address bits A0~A4 and bit R/$\overline{W}$) and an 8-bit data byte (D0~D7). When bit R/$\overline{W}$ is '1', data is read out from pin SDO. When bit R/$\overline{W}$ is '0', data is written into SDI pin. Refer to Figure-17.

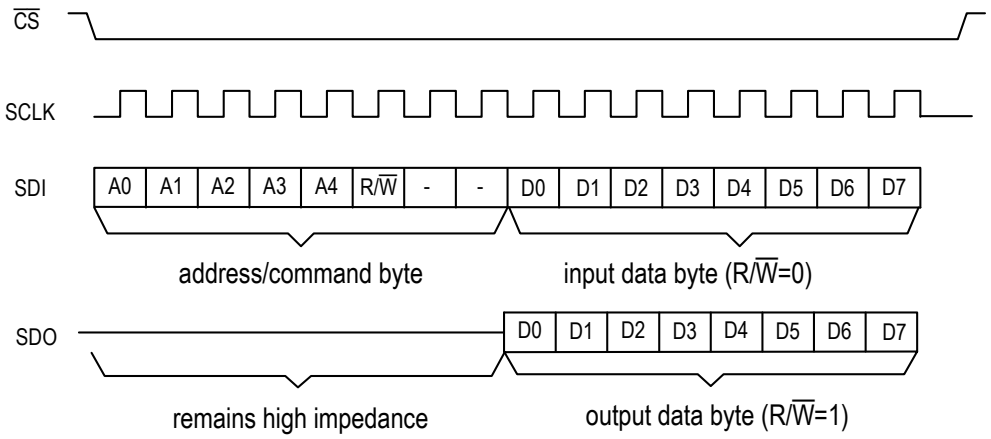


Figure-17 Serial Microcontroller Interface Function Timing

3.12 INTERRUPT HANDLING

All kinds of interrupt of the IDT82V2051E are indicated by the $\overline{INT}$ pin. When the INT_PIN[0] bit (**GCF, 02H**) is '0', the $\overline{INT}$ pin is open drain active low, with a 10 KΩ external pull-up resistor. When the INT_PIN[1:0] bits (**GCF, 02H**) are '01', the $\overline{INT}$ pin is push-pull active low; when the INT_PIN[1:0] bits are '10', the $\overline{INT}$ pin is push-pull active high.

An active level on the $\overline{INT}$ pin represents an interrupt of the IDT82V2051E.

The interrupt event is captured by the corresponding bit in the Interrupt Status Register **(INTS0, 19H)** or **(INTS1, 1AH)**. Every kind of interrupt can be enabled/disabled individually by the corresponding bit in the register **(INTM0, 14H)** or **(INTM1, 15H)**. Some event is reflected by the corresponding bit in the Status Register **(STAT0, 17H**) or **(STAT1, 18H)**, and the Interrupt Trigger Edge Selection Register can be used to determine how the Status Register sets the Interrupt Status Register.

After the Interrupt Status Register **(INTS0, 19H)** or **(INTS1, 1AH)** is read, the $\overline{INT}$ pin become inactive.

There are totally twelve kinds of events that could be the interrupt source:

(1).LOS Detected
(2).AIS Detected
(3).Driver Failure Detected
(4).TCLK Loss
(5).Synchronization Status of PRBS
(6).PRBS Error Detected
(7).Code Violation Received
(8).Excessive Zeros Received
(9).JA FIFO Overflow/Underflow
(10).One-Second Timer Expired
(11).Error Counter Overflow
(12).Arbitrary Waveform Generator Overflow

Table-12 is a summary of all kinds of interrupt and the associated Status bit, Interrupt Status bit, Interrupt Trigger Edge Selection bit and Interrupt Mask bit.

© 2019 Renesas Electronics Corporation

Table-12 Interrupt Event

Interrupt Event	Status bit (STAT0, STAT1)	Interrupt Status bit (INTS0, INTS1)	Interrupt Edge Selection bit (INTES)	Interrupt Mask bit (INTM0, INTM1)
LOS Detected	LOS_S	LOS_IS	LOS_IES	LOS_IM
AIS Detected	AIS_S	AIS_IS	AIS_IES	AIS_IM
Driver Failure Detected	DF_S	DF_IS	DF_IES	DF_IM
TCLK Loss	TCLK_LOS	TCLK_LOS_IS	TCLK_IES	TCLK_IM
Synchronization Status of PRBS	PRBS_S	PRBS_IS	PRBS_IES	PRBS_IM
PRBS Error		ERR_IS		ERR_IM
Code Violation Received		CV_IS		CV_IM
Excessive Zeros Received		EXZ_IS		EXZ_IM
JA FIFO Overflow		JAOV_IS		JAOV_IM
JA FIFO Underflow		JAUD_IS		JAUD_IM
One-Second Timer Expired		TMOV_IS		TIMER_IM
Error Counter Overflow		CNT_OV_IS		CNT_IM
Arbitrary Waveform Generator Overflow		DAC_OV_IS		DAC_OV_IM

3.13 5V TOLERANT I/O PINS

All digital input pins will tolerate 5.0 ± 10% volts and are compatible with TTL logic.

3.14 RESET OPERATION

The chip can be reset in two ways:

- Software Reset: Writing to the **RST** register (**01H**) will reset the chip in 1 us.
- Hardware Reset: Asserting the $\overline{\text{RST}}$ pin low for a minimum of 100 ns will reset the chip.
  During Hardware Reset, the device requires an active clock on MCLK.

After reset, all drivers output are in high impedance state, all the internal flip-flops are reset, and all the registers are initialized to default values.

3.15 POWER SUPPLY

This chip uses a single 3.3 V power supply.

© 2019 Renesas Electronics Corporation

4 PROGRAMMING INFORMATION

4.1 REGISTER LIST AND MAP

The registers banks include control registers, status registers and counter registers.

4.2 RESERVED REGISTERS

When writing to registers with reserved bit locations, the default state must be written to the reserved bits to ensure proper device operation.

Table-13 Register List and Map

Address (hex)	Register	R/W	Map							
			b7	b6	b5	b4	b3	b2	b1	b0
Control Registers										
00	ID	R	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
01	RST	W								
02	GCF	R/W	-	-	-	-	-	-	INT_PIN1	INT_PIN0
03	TERM	R/W	-	-	T_TERM2	T_TERM1	T_TERM0	R_TERM2	R_TERM1	R_TERM0
04	JACF	R/W	-	-	JA_LIMIT	JACF1	JACF0	JADP1	JADP0	JABW
Transmit Path Control Registers										
05	TCF0	R/W	-	-	-	T_OFF	TD_INV	TCLK_SEL	T_MD1	T_MD0
06	TCF1	R/W	-	-	DFM_OFF	THZ	PULS3	PULS2	PULS1	PULS0
07	TCF2	R/W	-	-	SCAL5	SCAL4	SCAL3	SCAL2	SCAL1	SCAL0
08	TCF3	R/W	DONE	RW	UI1	UI0	SAMP3	SAMP2	SAMP1	SAMP0
09	TCF4	R/W	-	WDAT6	WDAT5	WDAT4	WDAT3	WDAT2	WDAT1	WDAT0
Receive Path Control Registers										
0A	RCF0	R/W	-	-	-	R_OFF	RD_INV	RCLK_SEL	R_MD1	R_MD0
0B	RCF1	R/W	-	EQ_ON	-	LOS4	LOS3	LOS2	LOS1	LOS0
0C	RCF2	R/W	-	-	SLICE1	SLICE0	-	-	MG1	MG0
Network Diagnostics Control Registers										
0D	MAINT0	R/W	-	PATT1	PATT0	PATT_CLK	PRBS_INV	LAC	AISE	ATAO
0E	MAINT1	R/W	-	-	-	-	-	RLP	ALP	DLP
1F-12	MAINT2-MAINT5	R/W	-	-	-	-	-	-	-	-
13	MAINT6	R/W	-	BPV_INS	ERR_INS	EXZ_DEF	ERR_SEL1	ERR_SEL0	CNT_MD	CNT_TRF
Interrupt Control Registers										
14	INTM0	R/W	-	-	-	PRBS_IM	TCLK_IM	DF_IM	AIS_IM	LOS_IM
15	INTM1	R/W	DAC_OV_IM	JAOV_IM	JAUD_IM	ERR_IM	EXZ_IM	CV_IM	TIMER_IM	CNT_IM
16	INTES	R/W	-	-	-	PRBS_IES	TCLK_IES	DF_IES	AIS_IES	LOS_IES
Line Status Register										
17	STAT0	R	-	-	-	PRBS_S	TCLK_LOS	DF_S	AIS_S	LOS_S
18	STAT1	R	-	-	RLP_S	-	-	-	-	-
Interrupt Status Register										
19	INTS0	R	-	-	-	PRBS_IS	TCLK_LOS_IS	DF_IS	AIS_IS	LOS_IS
1A	INTS1	R	DAC_OV_IS	JAOV_IS	JAUD_IS	ERR_IS	EXZ_IS	CV_IS	TMOV_IS	CNT_OV_IS
Counter Registers										
1B	CNT0	R	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
1C	CNT1	R	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8

© 2019 Renesas Electronics Corporation

4.3 REGISTER DESCRIPTION

4.3.1 CONTROL REGISTERS

Table-14 ID: Device Revision Register
(R, Address = 00H)

Symbol	Bit	Default	Description
ID[7:0]	7-0	00H	Current silicon chip ID.

Table-15 RST: Reset Register
(W, Address = 01H)

Symbol	Bit	Default	Description
RST[7:0]	7-0	00H	Software reset. A write operation on this register will reset all internal registers to their default values, and the status of all ports are set to the default status. The content in this register can not be changed. After reset, all drivers output are in high impedance state.

Table-16 GCF: Global Configuration Register
(R/W, Address = 02H)

Symbol	Bit	Default	Description
-	7-2	000000	Reserved.
INT_PIN[1:0]	1-0	00	Interrupt pin control = x0: Open drain, active low (with an external pull-up resistor) = 01: Push-pull, active low = 11: Push-pull, active high

Table-17 TERM: Transmit and Receive Termination Configuration Register
(R/W, Address = 03H)

Symbol	Bit	Default	Description
-	7-6	00	Reserved.
T_TERM[2:0]	5-3	000	These bits select the internal termination for transmit line impedance matching. = 000: Internal 75 Ω impedance matching = 001: Internal 120 Ω impedance matching = 1xx: Selects external impedance matching resistors (see Table-4).
R_TERM[2:0]	2-0	000	These bits select the internal termination for receive line impedance matching. = 000: Internal 75 Ω impedance matching = 001: Internal 120 Ω impedance matching = 1xx: Selects external impedance matching resistors (see Table-5).

© 2019 Renesas Electronics Corporation

Table-18 JACF: Jitter Attenuation Configuration Register
(R/W, Address = 04H)

Symbol	Bit	Default	Description
-	7-6	00	Reserved.
JA_LIMIT	5	1	= 0: Normal mode = 1: JA limit mode
JACF[1:0]	4-3	00	Jitter attenuation configuration = 00/10: JA not used = 01: JA in transmit path = 11: JA in receive path
JADP[1:0]	2-1	00	Jitter attenuation depth select = 00: 128 bits = 01: 64 bits = 1x: 32 bits
JABW	0	0	Jitter transfer function bandwidth select = 0: 6.8 Hz = 1: 0.9 Hz

© 2019 Renesas Electronics Corporation

4.3.2 TRANSMIT PATH CONTROL REGISTERS

Table-19 TCF0: Transmitter Configuration Register 0

(R/W, Address = 05H)

Symbol	Bit	Default	Description
-	7-5	000	Reserved.
T_OFF	4	0	Transmitter power down enable = 0: Transmitter power up = 1: Transmitter power down (line driver high impedance)
TD_INV	3	0	Transmit data invert = 0: Data on TD or TDP/TDN is active high = 1: Data on TD or TDP/TDN is active low
TCLK_SEL	2	0	Transmit clock edge select = 0: Data on TDP/TDN is sampled on the falling edge of TCLK = 1: Data on TDP/TDN is sampled on the rising edge of TCLK
T_MD[1:0]	0-1	00	Transmitter operation mode control T_MD[1:0] select different stages of the transmit data path = 00: Enable HDB3 encoder and waveform shaper blocks. Input on pin TD is single rail NRZ data = 01: Enable AMI encoder and waveform shaper blocks. Input on pin TD is single rail NRZ data = 1x: Encoder is bypassed, dual rail NRZ transmit data input on pin TDP/TDN

Table-20 TCF1: Transmitter Configuration Register 1

(R/W, Address = 06H)

<table>
<tr><th>Symbol</th><th>Bit</th><th>Default</th><th colspan="4">Description</th></tr>
<tr><td>-</td><td>7-6</td><td>00</td><td colspan="4">Reserved. This bit should be ‘0’ for normal operation.</td></tr>
<tr><td>DFM_OFF</td><td>5</td><td>0</td><td colspan="4">Transmit driver failure monitor disable
= 0: DFM is enabled
= 1: DFM is disabled</td></tr>
<tr><td>THZ</td><td>4</td><td>1</td><td colspan="4">Transmit line driver high impedance enable
= 0: Normal state
= 1: Transmit line driver high impedance enable (other transmit path still work normally)</td></tr>
<tr><td rowspan="5">PULS[3:0]</td><td rowspan="5">3-0</td><td rowspan="5">0000</td><td colspan="4">These bits select the transmit template:</td></tr>
<tr><td></td><td>TCLK</td><td>Cable impedance</td><td>Allowable Cable loss</td></tr>
<tr><td>0000[1]</td><td>2.048 MHz</td><td>75 Ω</td><td>0-24 dB</td></tr>
<tr><td>0001</td><td>2.048 MHz</td><td>120 Ω</td><td>0-24 dB</td></tr>
<tr><td>0010 - 1011</td><td colspan="3">Reserved</td></tr>
<tr><td></td><td>11XX</td><td colspan="3">User programmable waveform setting</td></tr>
</table>

1. In internal impedance matching mode, for E1/75 Ω cable impedance, the PULS[3:0] bits (**TCF1, 06H**) should be set to ‘0000’. In external impedance matching mode, for E1/75 Ω cable impedance, the PULS[3:0] bits should be set to ‘0001’.

Table-21 TCF2: Transmitter Configuration Register 2

(R/W, Address = 07H)

Symbol	Bit	Default	Description
-	7-6	00	Reserved.
SCAL[5:0]	5-0	100001	SCAL specifies a scaling factor to be applied to the amplitude of the user-programmable arbitrary pulses which is to be transmitted if needed. The default value of SCAL[5:0] is ‘100001’. Refer to 3.2.3.2 User-Programmable Arbitrary Waveform. = 100001: Default value for 75 Ω and 120 Ω. One step change of this value results in 3% scaling up/down against the pulse amplitude.

© 2019 Renesas Electronics Corporation

Table-22 TCF3: Transmitter Configuration Register 3
(R/W, Address = 08H)

Symbol	Bit	Default	Description
DONE	7	0	After '1' is written to this bit, a read or write operation is implemented.
RW	6	0	This bit selects read or write operation = 0: Write to RAM = 1: Read from RAM
UI[1:0]	5-4	00	These bits specify the unit interval address. There are totally 4 unit intervals. = 00: UI address is 0 (The most left UI) = 01: UI address is 1 = 10: UI address is 2 = 11: UI address is 3
SAMP[3:0]	3-0	0000	These bits specify the sample address. Each UI has totally 16 samples. = 0000: Sample address is 0 (The most left sample) = 0001: Sample address is 1 = 0010: Sample address is 2 …… = 1110: Sample address is 14 = 1111: Sample address is 15

Table-23 TCF4: Transmitter Configuration Register 4
(R/W, Address = 09H)

Symbol	Bit	Default	Description
-	7	0	Reserved
WDAT[6:0]	6-0	0000000	In Indirect Write operation, the WDAT[6:0] will be loaded to the pulse template RAM, specifying the amplitude of the Sample. After an Indirect Read operation, the amplitude data of the Sample in the pulse template RAM will be output to the WDAT[6:0].

© 2019 Renesas Electronics Corporation

4.3.3 RECEIVE PATH CONTROL REGISTERS

Table-24 RCF0: Receiver Configuration Register 0

(R/W, Address = 0AH)

Symbol	Bit	Default	Description
-	7-5	000	Reserved
R_OFF	4	0	Receiver power down enable = 0: Receiver power up = 1: Receiver power down
RD_INV	3	0	Receive data invert = 0: Data on RD or RDP/RDN is active high = 1: Data on RD or RDP/RDN is active low
RCLK_SEL	2	0	Receive clock edge select (this bit is ignored in slicer mode) = 0: Data on RD or RDP/RDN is updated on the rising edge of RCLK = 1: Data on RD or RDP/RDN is updated on the falling edge of RCLK
R_MD[1:0]	1-0	00	Receive path decoding selection = 00: Receive data is HDB3 decoded and output on RD pin with single rail NRZ format = 01: Receive data is AMI decoded and output on RD pin with single rail NRZ format = 10: Decoder is bypassed, re-timed dual rail data with NRZ format output on RDP/RDN (dual rail mode with clock recovery) = 11: CDR and decoder are bypassed, slicer data with RZ format output on RDP/RDN (slicer mode)

Table-25 RCF1: Receiver Configuration Register 1

(R/W, Address= 0BH)

Symbol	Bit	Default	Description		
-	7	0	Reserved		
EQ_ON	6	0	= 0: Receive equalizer off = 1: Receive equalizer on (LOS programming enabled)		
-	5	0	Reserved.		
LOS[4:0]	4:0	10101		LOS Clear Level (dB)	LOS Declare Level (dB)
			00000	0	<-4
			00001	>-2	<-6
			00010	>-4	<-8
			00011	>-6	<-10
			00100	>-8	<-12
			00101	>-10	<-14
			00110	>-12	<-16
			00111	>-14	<-18
			01000	>-16	<-20
			01001	>-18	<-22
			01010	>-20	<-24
			01011 - 11111	Reserved	

© 2019 Renesas Electronics Corporation

Table-26 RCF2: Receiver Configuration Register 2
(R/W, Address = 0CH)

Symbol	Bit	Default	Description
-	7-6	00	Reserved.
SLICE[1:0]	5-4	01	Receive slicer threshold = 00: The receive slicer generates a mark if the voltage on RTIP/RRING exceeds 40% of the peak amplitude. = 01: The receive slicer generates a mark if the voltage on RTIP/RRING exceeds 50% of the peak amplitude. = 10: The receive slicer generates a mark if the voltage on RTIP/RRING exceeds 60% of the peak amplitude. = 11: The receive slicer generates a mark if the voltage on RTIP/RRING exceeds 70% of the peak amplitude.
-	3-2	10	Reserved
MG[1:0]	1-0	00	Monitor gain setting: these bits select the internal linear gain boost = 00: 0 dB = 01: 22 dB = 10: 26 dB = 11: 32 dB

© 2019 Renesas Electronics Corporation

4.3.4 NETWORK DIAGNOSTICS CONTROL REGISTERS

Table-27 MAINT0: Maintenance Function Control Register 0

(R/W, Address = 0DH)

Symbol	Bit	Default	Description
-	7	00	Reserved.
PATT[1:0]	6-5	00	These bits select the internal pattern and insert it into transmit data stream. = 00: Normal operation (PATT_CLK = 0) / insert all zeros (PATT_CLK = 1) = 01: Insert All Ones = 10: Insert PRBS (E1: 2^{15}-1) = 11: Reserved
PATT_CLK	4	0	Selects reference clock for transmitting internal pattern = 0: Uses TCLK as the reference clock = 1: Uses MCLK as the reference clock
PRBS_INV	3	0	Inverts PRBS = 0: The PRBS data is not inverted = 1: The PRBS data is inverted before transmission and detection
LAC	2	0	LOS/AIS criterion is selected as below: = 0: G.775 = 1: ETSI 300233& I.431
AISE	1	0	AIS enable during LOS = 0: AIS insertion on RDP/RDN/RCLK is disabled during LOS = 1: AIS insertion on RDP/RDN/RCLK is enabled during LOS
ATAO	0	0	Automatically Transmit All Ones (enabled only when PATT[1:0] = 00) = 0: Disabled = 1: Automatically Transmit All Ones pattern at TTIP/TRING during LOS

Table-28 MAINT1: Maintenance Function Control Register 1

(R/W, Address= 0EH)

Symbol	Bit	Default	Description
-	7-3	00000	Reserved
RLP	2	0	Remote loopback enable = 0: Disables remote loopback (normal transmit and receive operation) = 1: Enables remote loopback
ALP	1	0	Analog loopback enable = 0: Disables analog loopback (normal transmit and receive operation) = 1: Enables analog loopback
DLP	0	0	Digital loopback enable = 0: Disables digital loopback (normal transmit and receive operation) = 1: Enables digital loopback

Table-29 MAINT6: Maintenance Function Control Register 6

(R/W, Address = 13H)

Symbol	Bit	Default	Description
-	7	0	Reserved.
BPV_INS	6	0	BPV error insertion A '0' to '1' transition on this bit will cause a single bipolar violation error to be inserted into the transmit data stream. This bit must be cleared and set again for a subsequent error to be inserted.
ERR_INS	5	0	PRBS logic error insertion A '0' to '1' transition on this bit will cause a single PRBS logic error to be inserted into the transmit PRBS data stream. This bit must be cleared and set again for a subsequent error to be inserted.

© 2019 Renesas Electronics Corporation

Table-29 MAINT6: Maintenance Function Control Register 6 (Continued)
(R/W, Address = 13H)

Symbol	Bit	Default	Description
EXZ_DEF	5	0	EXZ definition select = 0: ANSI = 1: FCC
ERR_SEL	3-2	00	These bits choose which type of error will be counted = 00: The PRBS logic error is counted by a 16-bit error counter. = 01: The EXZ error is counted by a 16-bit error counter. = 10: The Received CV (BPV) error is counted by a 16-bit error counter. = 11: Both CV (BPV) and EXZ errors are counted by a 16-bit error counter.
CNT_MD	1	0	Counter operation mode select = 0: Manual Report mode = 1: Auto Report mode
CNT_TRF	0	0	= 0: Clear this bit for the next '0' to '1' transition on this bit. = 1: Error counting result is transferred to CNT0 and CNT1 and the error counter is reset.

© 2019 Renesas Electronics Corporation

4.3.5 INTERRUPT CONTROL REGISTERS

Table-30 INTM0: Interrupt Mask Register 0
(R/W, Address = 14H)

Symbol	Bit	Default	Description
-	7-5	111	Reserved
PRBS_IM	4	1	PRBS synchronic signal detect interrupt mask = 0: PRBS synchronic signal detect interrupt enabled = 1: PRBS synchronic signal detect interrupt masked
TCLK_IM	3	1	TCLK loss detect interrupt mask = 0: TCLK loss detect interrupt enabled = 1: TCLK loss detect interrupt masked
DF_IM	2	1	Driver Failure interrupt mask = 0: Driver Failure interrupt enabled = 1: Driver Failure interrupt masked
AIS_IM	1	1	Alarm Indication Signal interrupt mask = 0: Alarm Indication Signal interrupt enabled = 1: Alarm Indication Signal interrupt masked
LOS_IM	0	1	Loss Of Signal interrupt mask = 0: Loss Of Signal interrupt enabled = 1: Loss Of Signal interrupt masked

Table-31 INTM1: Interrupt Masked Register 1
(R/W, Address = 15H)

Symbol	Bit	Default	Description
DAC_OV_IM	7	1	DAC arithmetic overflow interrupt mask = 0: DAC arithmetic overflow interrupt enabled = 1: DAC arithmetic overflow interrupt masked
JAOV_IM	6	1	JA overflow interrupt mask = 0: JA overflow interrupt enabled = 1: JA overflow interrupt masked
JAUD_IM	5	1	JA underflow interrupt mask = 0: JA underflow interrupt enabled = 1: JA underflow interrupt masked
ERR_IM	4	1	PRBS logic error detect interrupt mask = 0: PRBS logic error detect interrupt enabled = 1: PRBS logic error detect interrupt masked
EXZ_IM	3	1	Receive excess zeros interrupt mask = 0: Receive excess zeros interrupt enabled = 1: Receive excess zeros interrupt masked
CV_IM	2	1	Receive error interrupt mask = 0: Receive error interrupt enabled = 1: Receive error interrupt masked
TIMER_IM	1	1	One-Second Timer expiration interrupt mask = 0: One-Second Timer expiration interrupt enabled = 1: One-Second Timer expiration interrupt masked
CNT_IM	0	1	Counter overflow interrupt mask = 0: Counter overflow interrupt enabled = 1: Counter overflow interrupt masked

© 2019 Renesas Electronics Corporation

Table-32 INTES: Interrupt Trigger Edge Select Register
(R/W, Address = 16H)

Symbol	Bit	Default	Description
-	7-5	000	Reserved
PRBS_IES	4	0	This bit determines the PRBS synchronization status interrupt event. = 0: Interrupt event is generated as a '0' to '1' transition of the PRBS_S bit in STAT0 status register = 1: Interrupt event is generated as either a '0' to '1' transition or a '1' to '0' transition of the PRBS_S bit in STAT0 status register
TCLK_IES	3	0	This bit determines the TCLK Loss interrupt event. = 0: Interrupt event is generated as a '0' to '1' transition of the TCLK_LOS bit in STAT0 status register = 1: Interrupt event is generated as either a '0' to '1' transition or a '1' to '0' transition of the TCLK_LOS bit in STAT0 status register
DF_IES	2	0	This bit determines the Driver Failure interrupt event. = 0: Interrupt event is generated as a '0' to '1' transition of the DF_S bit in STAT0 status register = 1: Interrupt event is generated as either a '0' to '1' transition or a '1' to '0' transition of the DF_S bit in STAT0 status register
AIS_IES	1	0	This bit determines the AIS interrupt event. = 0: Interrupt event is generated as a '0' to '1' transition of the AIS_S bit in STAT0 status register = 1: Interrupt event is generated as either a '0' to '1' transition or a '1' to '0' transition of the AIS_S bit in STAT0 status register
LOS_IES	0	0	This bit determines the LOS interrupt event. = 0: Interrupt is generated as a '0' to '1' transition of the LOS_S bit in STAT0 status register = 1: Interrupt is generated as either a '0' to '1' transition or a '1' to '0' transition of the LOS_S bit in STAT0 status register

© 2019 Renesas Electronics Corporation

4.3.6 LINE STATUS REGISTERS

Table-33 STAT0: Line Status Register 0 (real time status monitor)
(R, Address = 17H)

Symbol	Bit	Default	Description
-	7-5	000	Reserved
PRBS_S	4	0	Synchronous status indication of PRBS (real time) = 0: 2^{15}-1 PRBS is not detected = 1: 2^{15}-1 PRBS is detected Note: If PRBS_IM=0: A '0' to '1' transition on this bit causes a synchronous status detected interrupt if PRBS _IES bit is '0'. Any changes of this bit causes an interrupt if PRBS_IES bit is set to '1'.
TCLK_LOS	3	0	TCLK loss indication = 0: Normal = 1: TCLK pin has not toggled for more than 70 MCLK cycles. Note: If TCLK_IM=0: A '0' to '1' transition on this bit causes an interrupt if TCLK _IES bit is '0'. Any changes of this bit causes an interrupt if TCLK_IES bit is set to '1'.
DF_S	2	0	Line driver status indication = 0: Normal operation = 1: Line driver short circuit is detected. Note: If DF_IM=0 A '0' to '1' transition on this bit causes an interrupt if DF _IES bit is '0'. Any changes of this bit causes an interrupt if DF_IES bit is set to '1'.
AIS_S	1	0	Alarm Indication Signal status detection = 0: No AIS signal is detected in the receive path = 1: AIS signal is detected in the receive path Note: If AIS_IM=0 A '0' to '1' transition on this bit causes an interrupt if AIS _IES bit is '0'. Any changes of this bit causes an interrupt if AIS_IES bit is set to '1'.
LOS_S	0	0	Loss Of Signal status detection = 0: Loss of signal on RTIP/RRING is not detected. = 1: Loss of signal on RTIP/RRING is detected. Note: If LOS_IM=0 A '0' to '1' transition on this bit causes an interrupt if LOS _IES bit is '0'. Any changes of this bit causes an interrupt if LOS_IES bit is set to '1'.

© 2019 Renesas Electronics Corporation

Table-34 STAT1: Line Status Register 1 (real time status monitor)
(R, Address = 18H)

Symbol	Bit	Default	Description
-	7-6	00	Reserved.
RLP_S	5	0	Indicating the status of Remote Loopback = 0: The remote loopback is inactive. = 1: The remote loopback is active (closed).
-	4-0	00000	Reserved

© 2019 Renesas Electronics Corporation

4.3.7 INTERRUPT STATUS REGISTERS

Table-35 INTS0: Interrupt Status Register 0

(R, Address = 19H) (this register is reset and relevant interrupt request is cleared after a read)

Symbol	Bit	Default	Description
-	7-5	000	Reserved
PRBS_IS	4	0	This bit indicates the occurrence of the interrupt event generated by the PRBS synchronization status. = 0: No PRBS synchronization status interrupt event occurred = 1: PRBS synchronization status interrupt event occurred
TCLK_LOS_IS	3	0	This bit indicates the occurrence of the interrupt event generated by the TCLK loss detection. = 0: No TCLK loss interrupt event. = 1: TCLK loss interrupt event occurred.
DF_IS	2	0	This bit indicates the occurrence of the interrupt event generated by the Driver Failure. = 0: No Driver Failure interrupt event occurred = 1: Driver Failure interrupt event occurred
AIS_IS	1	0	This bit indicates the occurrence of the AIS (Alarm Indication Signal) interrupt event. = 0: No AIS interrupt event occurred = 1: AIS interrupt event occurred
LOS_IS	0	0	This bit indicates the occurrence of the LOS (Loss of signal) interrupt event. = 0: No LOS interrupt event occurred = 1: LOS interrupt event occurred

Table-36 INTS1: Interrupt Status Register 1

(R, Address = 1AH) (this register is reset and the relevant interrupt request is cleared after a read)

Symbol	Bit	Default	Description
DAC_OV_IS	7	0	This bit indicates the occurrence of the pulse amplitude overflow of Arbitrary Waveform Generator interrupt event. = 0: No pulse amplitude overflow of Arbitrary Waveform Generator interrupt event occurred = 1: The pulse amplitude overflow of Arbitrary Waveform Generator interrupt event occurred
JAOV_IS	6	0	This bit indicates the occurrence of the Jitter Attenuator Overflow interrupt event. = 0: No JA Overflow interrupt event occurred = 1: JA Overflow interrupt event occurred
JAUD_IS	5	0	This bit indicates the occurrence of the Jitter Attenuator Underflow interrupt event. = 0: No JA Underflow interrupt event occurred = 1: JA Underflow interrupt event occurred
ERR_IS	4	0	This bit indicates the occurrence of the interrupt event generated by the detected PRBS logic error. = 0: No PRBS logic error interrupt event occurred = 1: PRBS logic error interrupt event occurred
EXZ_IS	3	0	This bit indicates the occurrence of the Excessive Zeros interrupt event. = 0: No Excessive Zeros interrupt event occurred = 1: EXZ interrupt event occurred
CV_IS	2	0	This bit indicates the occurrence of the Code Violation interrupt event. = 0: No Code Violation interrupt event occurred = 1: Code Violation interrupt event occurred
TMOV_IS	1	0	This bit indicates the occurrence of the One-Second Timer Expiration interrupt event. = 0: No One-Second Timer Expiration interrupt event occurred = 1: One-Second Timer Expiration interrupt event occurred
CNT_OV_IS	0	0	This bit indicates the occurrence of the Counter Overflow interrupt event. = 0: No Counter Overflow interrupt event occurred = 1: Counter Overflow interrupt event occurred

© 2019 Renesas Electronics Corporation

4.3.8 COUNTER REGISTERS

Table-37 CNT0: Error Counter L-byte Register 0
(R, Address = 1BH)

Symbol	Bit	Default	Description
CNT_L[7:0]	7-0	00H	This register contains the lower eight bits of the 16-bit error counter. CNT_L[0] is the LSB.

Table-38 CNT1: Error Counter H-byte Register 1
(R, Address = 1CH)

Symbol	Bit	Default	Description
CNT_H[7:0]	7-0	00H	This register contains the upper eight bits of the 16-bit error counter. CNT_H[7] is the MSB.

© 2019 Renesas Electronics Corporation

5 HARDWARE CONTROL PIN SUMMARY

Table-39 Hardware Control Pin Summary

<table>
<tr><th>Pin No.
TQFP</th><th>Symbol</th><th>Description</th></tr>
<tr><td>17
16</td><td>MODE1
MODE0</td><td>MODE[1:0]: Operation mode of control interface select
00= Hardware interface
01= Serial interface
10= Parallel – multiplexed – Motorola Interface
11= Parallel – multiplexed – Intel Interface</td></tr>
<tr><td>23</td><td>TERM</td><td>TERM: Termination interface select
This pin selects internal or external impedance matching for both receiver and transmitter
0= ternary interface with external impedance matching network.
1= ternary interface with internal impedance matching network</td></tr>
<tr><td>21
20</td><td>RXTXM1
RXTXM0</td><td>RXTXM[1:0]: Receive and transmit path operation mode select
00= single rail with HDB3 coding
01= single rail with AMI coding
10= dual rail interface with CDR enable
11= slicer mode</td></tr>
<tr><td>30</td><td>PULS</td><td>PULS: This pin is used to select the following functions:
• Transmit pulse template
• Internal termination impedance (75 Ω / 120Ω)
<table>
<tr><th>PULS</th><th>TCLK</th><th>Cable impedance (internal matching impedance)</th><th>Cable loss</th></tr>
<tr><td>0</td><td>2.048 MHz</td><td>75Ω</td><td>0-24 dB</td></tr>
<tr><td>1</td><td>2.048 MHz</td><td>120Ω</td><td>0-24 dB</td></tr>
</table></td></tr>
<tr><td>28</td><td>RPD</td><td>RPD: Receiver power down control
0= Normal operation
1= receiver power down</td></tr>
<tr><td>27
26</td><td>PATT1
PATT0</td><td>PATT[1:0]: Transmit test pattern select
In hardware control mode, these pins select the transmit pattern
00 = normal
01= All Ones
10= PRBS
11= transmitter power down</td></tr>
<tr><td>15
14</td><td>JA1
JA0</td><td>JA[1:0]: Jitter attenuation position, bandwidth and the depth of FIFO select
00= JA is disabled
01= JA in receiver, broad bandwidth, FIFO=64 bits
10= JA in receiver, narrow bandwidth, FIFO=128 bits
11= JA in transmitter, narrow bandwidth, FIFO=128 bits</td></tr>
<tr><td>22</td><td>MONT</td><td>MONT: Receive monitor n gain select
0= 0 dB
1= up to 26 dB</td></tr>
<tr><td>25
24</td><td>LP1
LP0</td><td>LP[1:0]: Loopback mode select
00= no loopback
01= analog loopback
10= digital loopback
11= remote loopback</td></tr>
<tr><td>13</td><td>THZ</td><td>THZ: Transmitter Driver High Impedance Enable
This signal enables or disables transmitter driver. A low level on this pin enables the driver while a high level on this pin places the driver in high impedance state.</td></tr>
<tr><td>11</td><td>RCLKE</td><td>RCLKE: the active edge of RCLK select when hardware control mode is used
0= select the rising edge as active edge of RCLK
1= select the falling edge as active edge of RCLK</td></tr>
</table>

© 2019 Renesas Electronics Corporation

Table-39 Hardware Control Pin Summary (Continued)

Pin No. TQFP	Symbol	Description
29 31 32 33	-	In Hardware mode, this pin has to be tied to GND.

© 2019 Renesas Electronics Corporation

6 TEST SPECIFICATIONS

Table-40 Absolute Maximum Rating

Symbol	Parameter	Min	Max	Unit
VDDA, VDDD	Core Power Supply	-0.5	4.6	V
VDDIO	I/O Power Supply	-0.5	4.6	V
VDDT	Transmit Power Supply	-0.5	4.6	V
Vin	Input Voltage, Any Digital Pin	GND-0.5	5.5	V
	Input Voltage, Any RTIP and RRING pin[1]	GND-0.5	VDDA+0.5	V
	ESD Voltage, any pin	2000 [2]		V
		500 [3]		V
Iin	Transient latch-up current, any pin		100	mA
	Input current, any digital pin [4]	-10	10	mA
	DC Input current, any analog pin [4]		±100	mA
Pd	Maximum power dissipation in package		1.41	W
Tc	Case Temperature		120	°C
Ts	Storage Temperature	-65	+150	°C
CAUTION: Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.				

1.Reference to ground
2.Human body model
3.Charge device model
4.Constant input current

Table-41 Recommended Operation Conditions

Symbol	Parameter	Min	Typ	Max	Unit
VDDA, VDDD	Core Power Supply	3.13	3.3	3.47	V
VDDIO	I/O Power Supply	3.13	3.3	3.47	V
VDDT	Transmitter Power Supply	3.13	3.3	3.47	V
TA	Ambient operating temperature	-40	25	85	°C
Total current dissipation[1,2,3]	75 Ω load				
	50% ones density data	-	52	58	mA
	100% ones density data	-	64	70	
	120 Ω Load				
	50% ones density data	-	58	64	mA
	100% ones density data	-	70	76	

1.Power consumption includes power consumption on device and load. Digital levels are 10% of the supply rails and digital outputs driving a 50 pF capacitive load.
2.Maximum power consumption over the full operating temperature and power supply voltage range.
3.In short haul mode, if internal impedance matching is chosen, 75 Ω power dissipation values are measured with template PULS[3:0] = 0000; 120 Ω power dissipation values are measured with template PULS[3:0] = 0001.

© 2019 Renesas Electronics Corporation

Table-42 Power Consumption

Symbol	Parameter	Min	Typ	Max[1,2]	Unit
	3.3 V, 75 Ω Load				
	50% ones density data:	-	172	-	mW
	100% ones density data:	-	212	243	
	3.3 V, 120 Ω Load				
	50% ones density data:	-	192	-	mW
	100% ones density data:	-	243	264	

1.Maximum power and current consumption over the full operating temperature and power supply voltage range.
2.Power consumption includes power absorbed by line load and external transmitter components.

Table-43 DC Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
V_{IL}	Input Low Level Voltage	-	-	0.8	V
V_{IH}	Input High Voltage	2.0	-	-	V
V_{OL}	Output Low level Voltage (Iout=1.6mA)	-	-	0.4	V
V_{OH}	Output High level Voltage (Iout=400μA)	2.4	-	VDDIO	V
V_{MA}	Analog Input Quiescent Voltage (RTIP, RRING pin while floating)		1.5		V
I_{ZL}	High Impedance Leakage Current	-10		10	μA
Ci	Input capacitance			15	pF
Co	Output load capacitance			50	pF
Co	Output load capacitance (bus pins)			100	pF

Table-44 Receiver Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test conditions
	Receiver sensitivity					
	Adaptive Equalizer Disabled:			-10	dB	
	Adaptive Equalizer Enabled:			-20		
	Analog LOS level					A LOS level is programmable with Adaptive Equalizer enabled. Not available in Hardware mode.
	Adaptive Equalizer Disabled:		800		mVp-p	
	Adaptive Equalizer Enabled:	-4		-24	dB	

© 2019 Renesas Electronics Corporation

Table-44 Receiver Electrical Characteristics (Continued)

Symbol	Parameter	Min	Typ	Max	Unit	Test conditions
	Allowable consecutive zeros before LOS G.775: I.431/ETSI300233:		 32 2048			
	LOS reset	12.5			% ones	G.775, ETSI 300 233
	Receive Intrinsic Jitter 20 Hz - 100 kHz			 0.05	 U.I.	 JA enabled
	Input Jitter Tolerance 1 Hz – 20 Hz 20 Hz – 2.4 KHz 18 KHz – 100 KHz	 37 5 2			 U.I. U.I. U.I.	 G.823, with 6 dB cable attenuation
ZDM	Receiver Differential Input Impedance	20			KΩ	Internal mode
	Input termination resistor tolerance			±1%		
RRX	Receive Return Loss 51 KHz – 102 KHz 102 KHz – 2.048 MHz 2.048 MHz – 3.072 MHz	 20 20 20			 dB dB dB	 G.703 Internal termination
RPD	Receive path delay Single rail Dual rail		 7 2		 U.I. U.I.	 JA disabled

Table-45 Transmitter Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
Vo-p	Output pulse amplitudes 75 Ω load 120 Ω load	 2.14 2.7	 2.37 3.0	 2.60 3.3	 V V
Vo-s	Zero (space) level 75 Ω load 120 Ω load	 -0.237 -0.3		 0.237 0.3	 V V
	Transmit amplitude variation with supply	-1		+1	%
	Difference between pulse sequences for 17 consecutive pulses (T1.102)			200	mV
Tpw	Output Pulse Width at 50% of nominal amplitude	232	244	256	ns
	Ratio of the amplitudes of Positive and Negative Pulses at the center of the pulse interval (G.703)	0.95		1.05	
	Ratio of the width of Positive and Negative Pulses at the center of the pulse interval (G.703)	0.95		1.05	
RTX	Transmit Return Loss (G.703)				
	51 KHz – 102 KHz 102 KHz - 2.048 MHz 2.048 MHz – 3.072 MHz		20 15 12		dB dB dB
JTXp-p	Intrinsic Transmit Jitter (TCLK is jitter free)				
	20 Hz – 100 KHz			0.050	U.I.
Td	Transmit path delay (JA is disabled)				
	Single rail Dual rail		8.5 4.5		U.I. U.I.
Isc	Line short circuit current (measured on the TTIP/TRING pins)		100		mAp

© 2019 Renesas Electronics Corporation

Table-46 Transmitter and Receiver Timing Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
	MCLK frequency		2.048		MHz
	MCLK tolerance	-100		100	ppm
	MCLK duty cycle	30		70	%
Transmit path					
	TCLK frequency		2.048		MHz
	TCLK tolerance	-50		+50	ppm
	TCLK Duty Cycle	10		90	%
t1	Transmit Data Setup Time	40			ns
t2	Transmit Data Hold Time	40			ns
	Delay time of THZ low to driver high impedance			10	us
	Delay time of TCLK low to driver high impedance		75		U.I.
Receive path					
	Clock recovery capture range [1]		± 80		ppm
	RCLK duty cycle [2]	40	50	60	%
t4	RCLK pulse width [2]	457	488	519	ns
t5	RCLK pulse width low time	203	244	285	ns
t6	RCLK pulse width high time	203	244	285	ns
	Rise/fall time [3]			20	ns
t7	Receive Data Setup Time	200	244		ns
t8	Receive Data Hold Time	200	244		ns

1.Relative to nominal frequency, MCLK= ± 100 ppm
2.RCLK duty cycle widths will vary depending on extent of received pulse jitter displacement. Maximum and minimum RCLK duty cycles are for worst case jitter conditions (0.2 UI displacement for E1 per ITU G.823).
3.For all digital outputs. C load = 15 pF

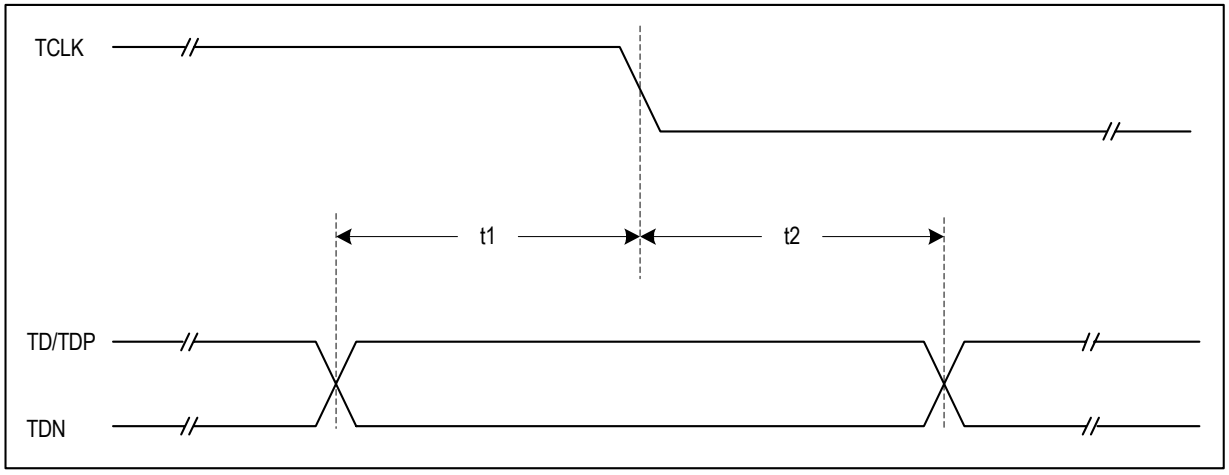


Figure-18 Transmit System Interface Timing

© 2019 Renesas Electronics Corporation

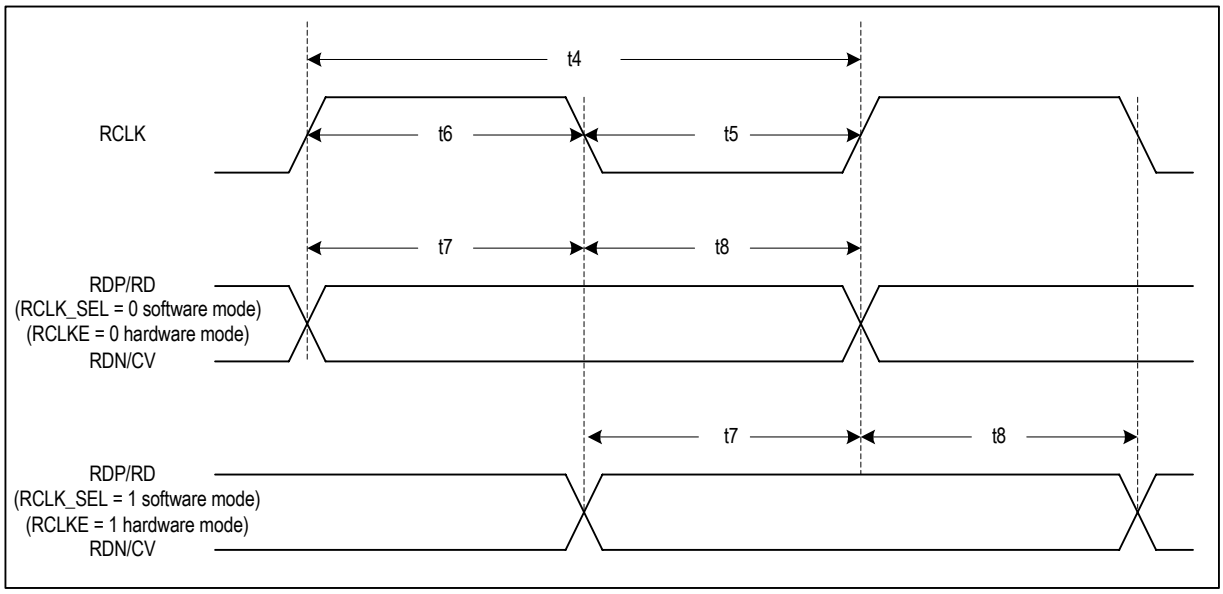


Figure-19 Receive System Interface Timing

Table-47 Jitter Tolerance

Jitter Tolerance	Min	Typ	Max	Unit	Standard
1 Hz	37			U.I.	G.823
20 Hz – 2.4 KHz	1.5			U.I.	Cable attenuation is 6 dB
18 KHz – 100 KHz	0.2			U.I.	

© 2019 Renesas Electronics Corporation

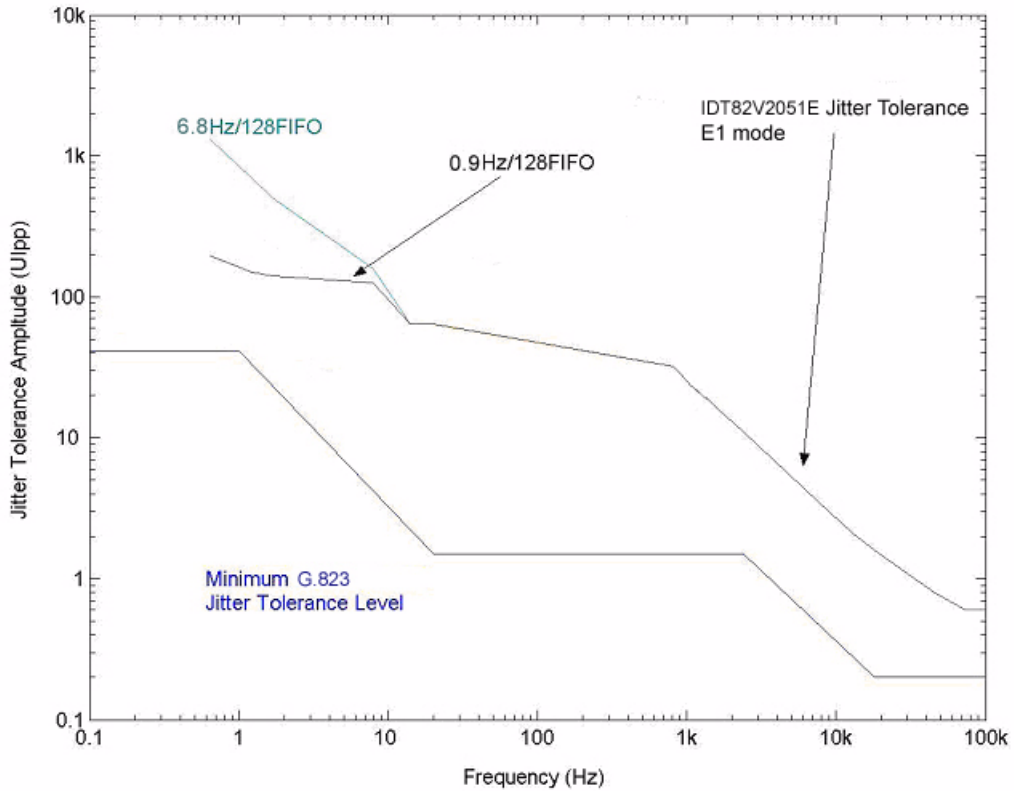


Figure-20 E1 Jitter Tolerance Performance

Table-48 Jitter Attenuator Characteristics

Parameter		Min	Typ	Max	Unit
Jitter Transfer Function Corner (-3 dB) Frequency					
	32/64/128 bits FIFO JABW = 0: JABW = 1:		 6.8 0.9		 Hz Hz
Jitter Attenuator					
(G.736) @ 3 Hz @ 40 Hz @ 400 Hz @ 100 kHz		 -0.5 -0.5 +19.5 +19.5			 dB
Jitter Attenuator Latency Delay					
32 bits FIFO: 64 bits FIFO: 128 bits FIFO:			16 32 64		U.I. U.I. U.I.
Input jitter tolerance before FIFO overflow or underflow 32 bits FIFO: 64 bits FIFO: 128 bits FIFO:			 28 58 120		 U.I. U.I. U.I.

© 2019 Renesas Electronics Corporation

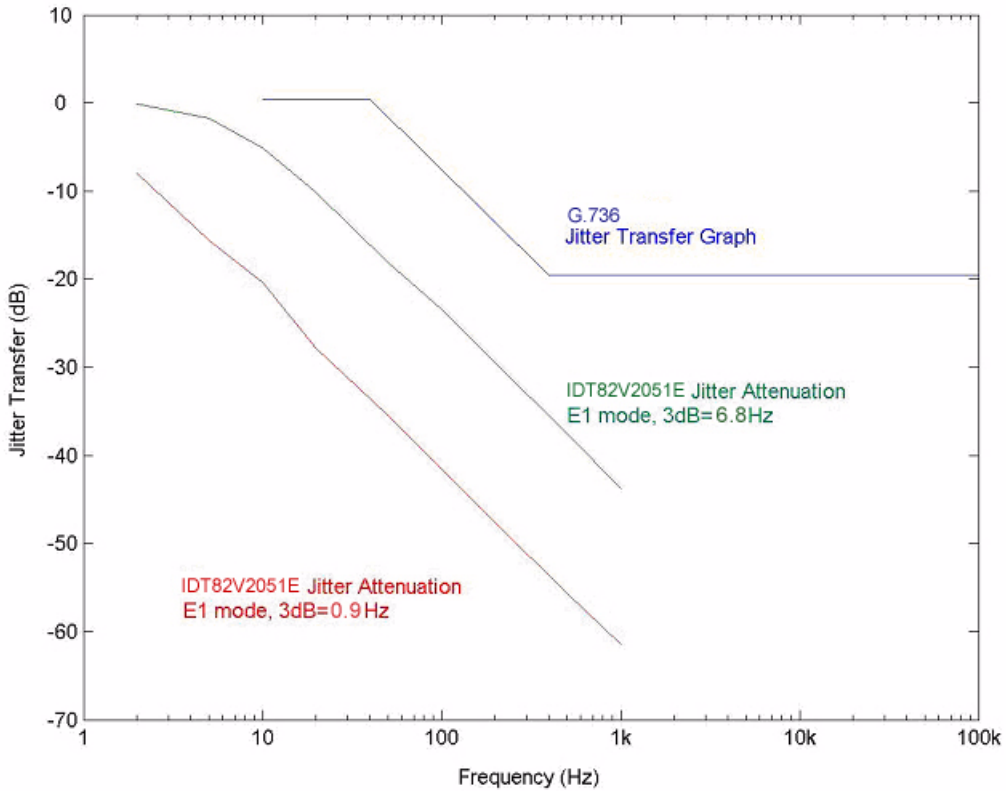


Figure-21 E1 Jitter Transfer Performance

© 2019 Renesas Electronics Corporation

7 MICROCONTROLLER INTERFACE TIMING CHARACTERISTICS

7.1 SERIAL INTERFACE TIMING

Table-49 Serial Interface Timing Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Comments
t1	SCLK High Time	100			ns	
t2	SCLK Low Time	100			ns	
t3	Active $\overline{CS}$ to SCLK Setup Time	5			ns	
t4	Last SCLK Hold Time to Inactive $\overline{CS}$ Time	41			ns	
t5	$\overline{CS}$ Idle Time	41			ns	
t6	SDI to SCLK Setup Time	0			ns	
t7	SCLK to SDI Hold Time	82			ns	
t10	SCLK to SDO Valid Delay Time			95	ns	
t11	Inactive $\overline{CS}$ to SDO High Impedance Hold Time			90	ns	

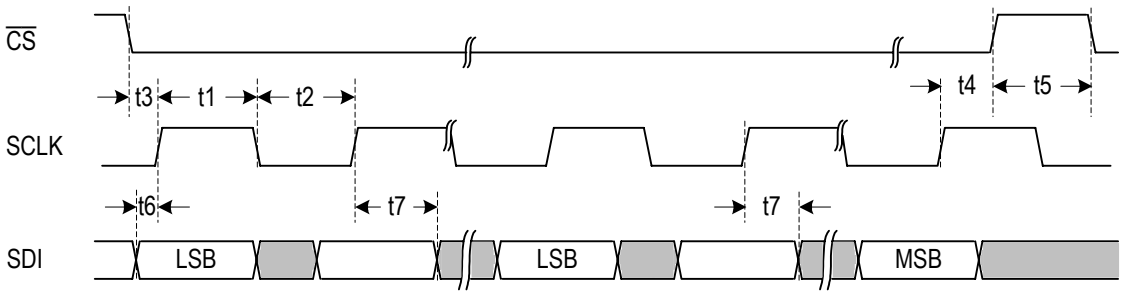


Figure-22 Serial Interface Write Timing

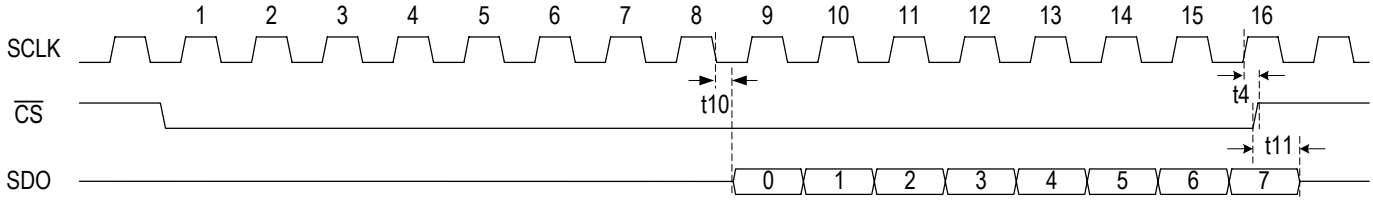


Figure-23 Serial Interface Read Timing with SCLKE=1

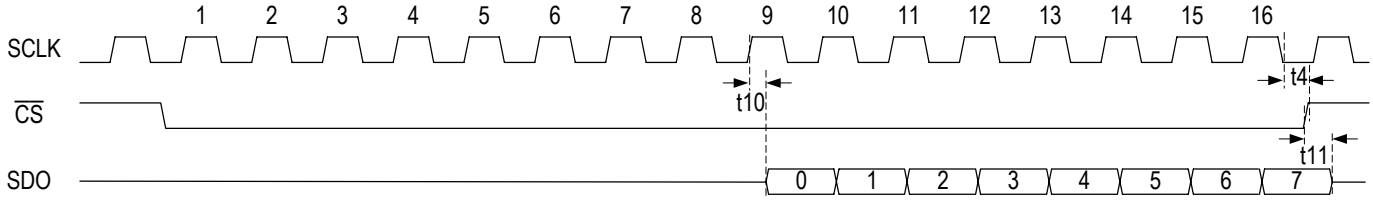


Figure-24 Serial Interface Read Timing with SCLKE=0

© 2019 Renesas Electronics Corporation

7.2 PARALLEL INTERFACE TIMING

Table-50 Multiplexed Motorola Read Timing Characteristics

Symbol	Parameter	Min	Max	Unit
tRC	Read Cycle Time	190		ns
tDW	Valid $\overline{DS}$ Width	180		ns
tRWV	Delay from $\overline{DS}$ to Valid Read		15	ns
tRWH	R/$\overline{W}$ to $\overline{DS}$ Hold Time	65		ns
tASW	Valid AS Width	10		ns
tADD	Delay from $\overline{AS}$ active to $\overline{DS}$ active	0		ns
tADS	Address to AS Setup Time	5		ns
tADH	Address to AS Hold Time	5		ns
tPRD	$\overline{DS}$ to Valid Read Data Propagation Delay		175	ns
tDAZ	Delay from $\overline{DS}$ inactive to data bus High Impedance	5	20	ns
tAKD	Acknowledgement Delay		190	ns
tAKH	Acknowledgement Hold Time	5	15	ns
tAKZ	Acknowledgement Release Time		5	ns
tRecovery	Recovery Time from Read Cycle	5		ns

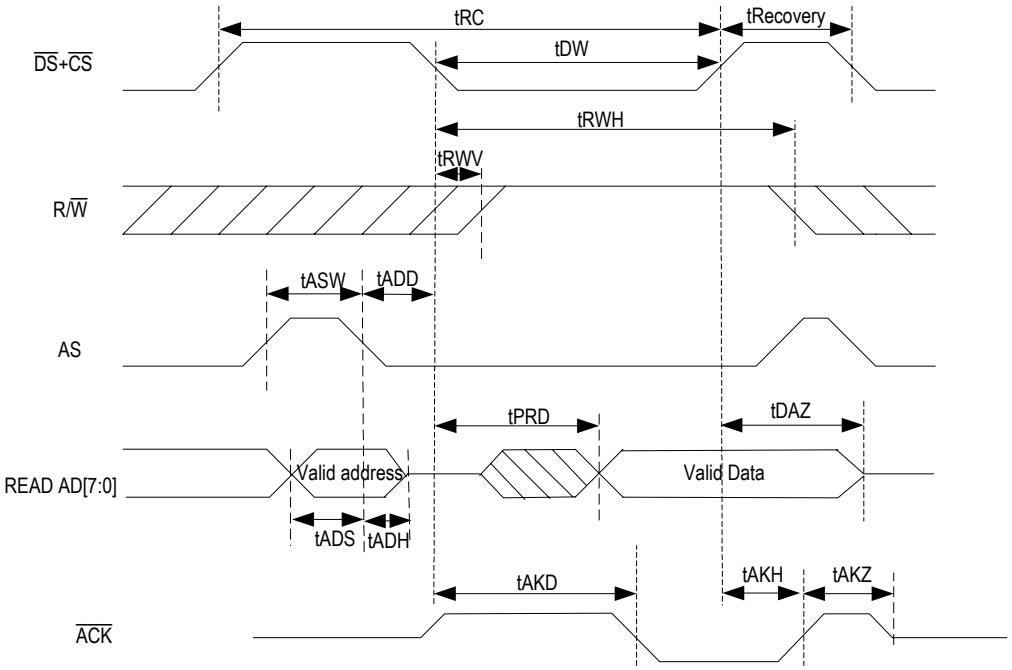


Figure-25 Multiplexed Motorola Read Timing

© 2019 Renesas Electronics Corporation

Table-51 Multiplexed Motorola Write Timing Characteristics

Symbol	Parameter	Min	Max	Unit
tWC	Write Cycle Time	120		ns
tDW	Valid $\overline{DS}$ Width	100		ns
tRWV	Delay from $\overline{DS}$ to Valid Write		15	ns
tRWH	R/$\overline{W}$ to $\overline{DS}$ Hold Time	65		ns
tASW	Valid AS Width	10		ns
tADD	Delay from $\overline{AS}$ active to $\overline{DS}$ active	0		ns
tADS	Address to AS Setup Time	5		ns
tADH	Address to AS Hold Time	5		ns
tDV	Delay from $\overline{DS}$ to Valid Write Data		15	ns
tDHW	Write Data to $\overline{DS}$ Hold Time	65		ns
tAKD	Acknowledgement Delay		150	ns
tAKH	Acknowledgement Hold Time	5	15	ns
tAKZ	Acknowledgement Release Time		5	ns
tRecovery	Recovery Time from Write Cycle	5		

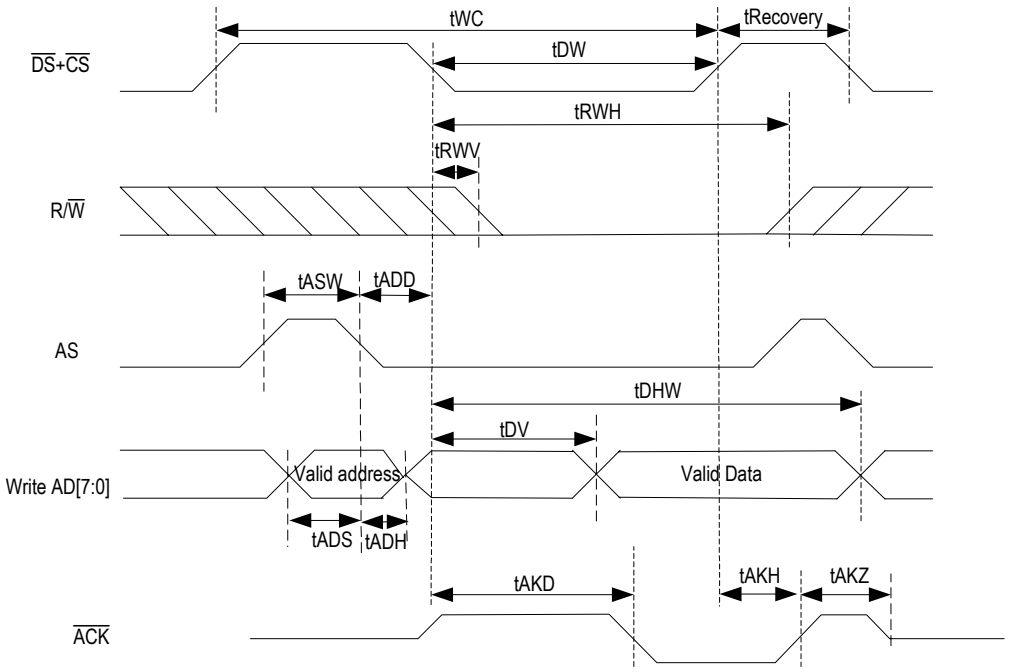


Figure-26 Multiplexed Motorola Write Timing

© 2019 Renesas Electronics Corporation

Table-52 Multiplexed Intel Read Timing Characteristics

Symbol	Parameter	Min	Max	Unit
tRC	Read Cycle Time	190		ns
tRDW	Valid $\overline{RD}$ Width	180		ns
tARD	Delay from ALE to Valid Read	0		ns
tALEW	Valid ALE Width	10		ns
tADS	Address to ALE Setup Time	5		ns
tADH	Address to ALE Hold Time	5		ns
tPRD	$\overline{RD}$ to Valid Read Data Propagation Delay		175	ns
tDAZ	Delay from $\overline{RD}$ inactive to data bus High Impedance	5	20	ns
tAKD	Acknowledgement Delay		190	ns
tAKH	Acknowledgement Hold Time	5	15	ns
tAKZ	Acknowledgement Release Time		5	ns
tRecovery	Recovery Time from Read Cycle	5		

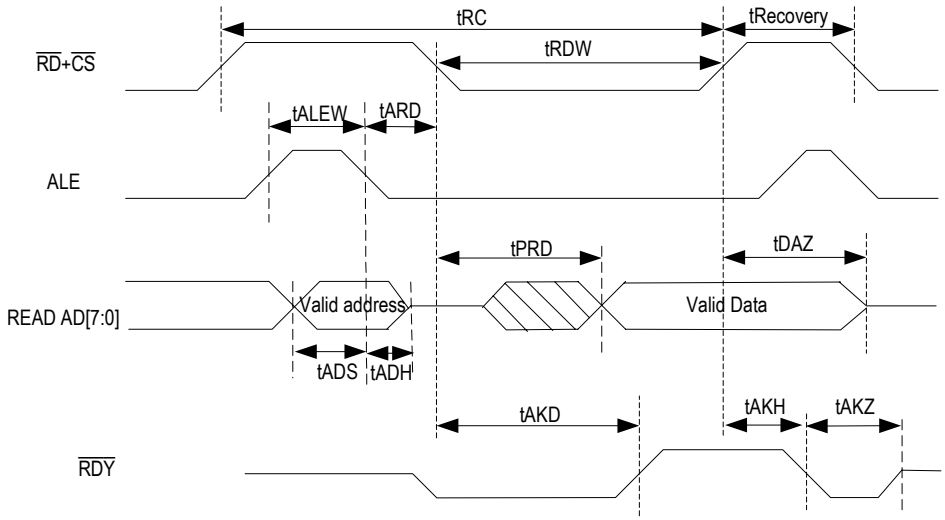


Figure-27 Multiplexed Intel Read Timing

© 2019 Renesas Electronics Corporation

Table-53 Multiplexed Intel Write Timing Characteristics

Symbol	Parameter	Min	Max	Unit
tWC	Write Cycle Time	120		ns
tWRW	Valid $\overline{WR}$ Width	100		ns
tALEW	Valid ALE Width	10		ns
tAWD	Delay from ALE to Valid Write	0		ns
tADS	Address to ALE Setup Time	5		ns
tADH	Address to ALE Hold Time	5		ns
tDV	Delay from $\overline{WR}$ to Valid Write Data		15	ns
tDHW	Write Data to $\overline{WR}$ Hold Time	65		ns
tAKD	Acknowledgement Delay		150	ns
tAKH	Acknowledgement Hold Time	5	15	ns
tAKZ	Acknowledgement Release Time		5	ns
tRecovery	Recovery Time from Write Cycle	5		

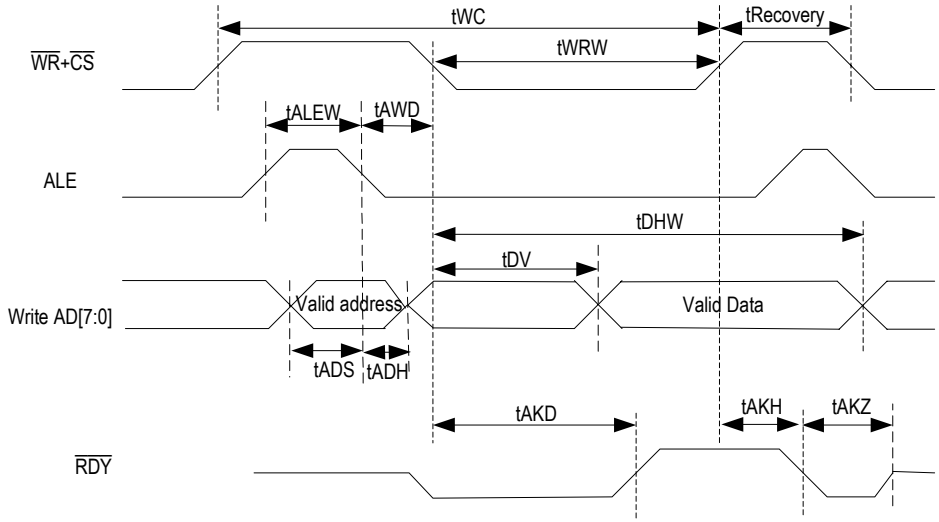
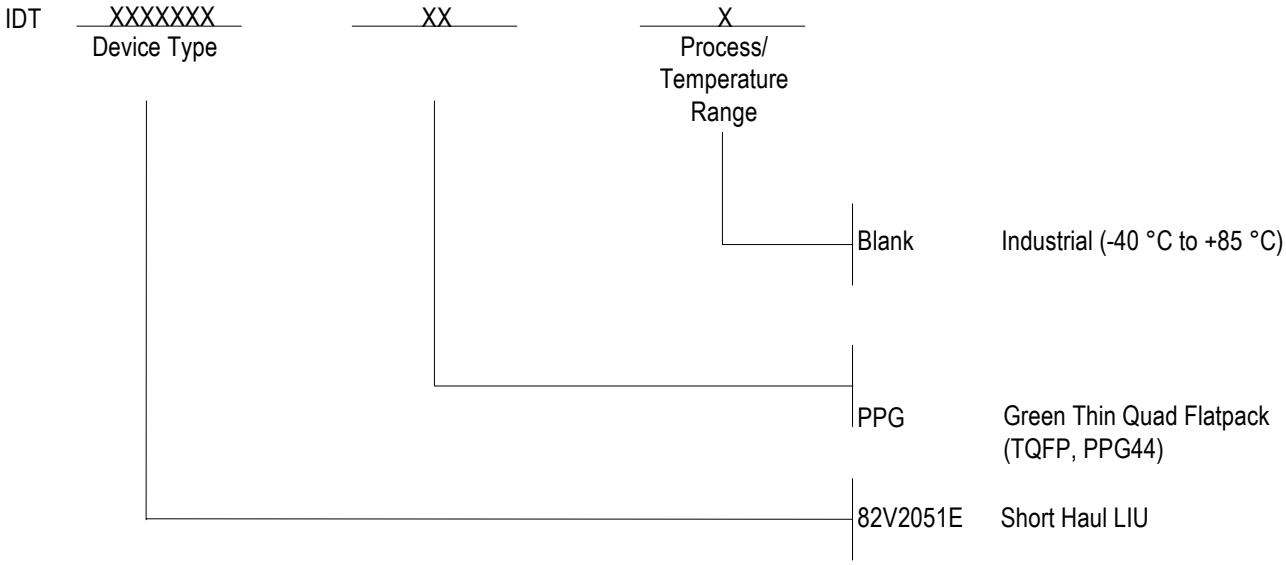


Figure-28 Multiplexed Intel Write Timing

© 2019 Renesas Electronics Corporation

ORDERING INFORMATION



DATASHEET DOCUMENT HISTORY

12/09/2005 pgs. 1, 14, 18, 24, 31, 32, 39, 51, 52, 61

02/23/2015 pg. 61 removed leaded device

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers skilled in the art designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only for development of an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising out of your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Rev.1.0 Mar 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
www.renesas.com/contact/

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

© 2020 Renesas Electronics Corporation. All rights reserved.