T1 / E1 / J1 Octal Framer

IDT82V2108

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T1 / E1 / J1 Octal Framer

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FEATURES

- Octal Framer supporting T1, E1 and J1 formats
- Provides programmable system interface to support Zarlink Semiconductor Inc. ST-BUS®, AT&T® CHI and MVIP bus, supporting data rates of 1.544, 2.048 & 8.192 Mb/s; up to four links can be byte-interleaved on one system bus without external logic
- Provides up to three internal floating HDLC controllers for each framer to support ISDN PRI and V5.X interface. Each HDLC contains 128-byte deep FIFOs in both receive and transmit directions
- Provides jitter attenuation performance exceeding the requirements set by the associated standards for both Rx and Tx path
- Provides payload, line and digital loopbacks
- Provides a floating Pseudo Random Bit Sequence / repetitive pattern generator/detector, which can be assigned to any one of eight framers, the pattern may be inserted / detected on an unframed or Nx64K or Nx56K (T1 only) basis
- Provides signaling insertion / extraction for CCS / CAS and RBS signaling system
- Provides programmable codes insertion, data / sign inversion and digital milliwatt code insertion on a per channel / timeslot basis
- Supports automatic / manual alarming transmit and integration
- Provides performance monitor to count CRC error, framing bit error, far end block CRC error (E1), out of frame event (T1/J1) and change of frame alignment event (T1/J1)
- Provides programmable Inband Loopback Code transmitter/receiver, Bit Oriented Message generator/detector
- Supports polled or interrupt driven processing for all events
- Supports multiplexed or non-multiplexed address/data bus MPU interface for configuration, control and status monitoring
- JTAG boundary scan meets IEEE 1149.1
- Low power 3.3 V CMOS technology with 5 V tolerant inputs
- Operating industrial temperature range: -40 °C to +85 °C
- Package available: 128 pin PQFP
  144 pin PBGA
  Green Package Option available

APPLICATIONS

- High density internet E1 or T1 / J1 interface for routers, multiplexers, switches and digital modems
- Frame relay switches and access devices (FRADS)
- SONET / SDH Add / Drop multiplexers
- Digital private branch exchanges (PBX)
- Channel service units (CSU) and data service units (DSU)
- Channel banks and multiplexers
- Digital Access and Cross-Connect systems (DACS)

STANDARDS

E1 MODE:

ITU-T: G.704, G.706, G.732, G.802, G.737, G.738, G.739, G.742, G.823, G.964, G.965, I.431, O.151, O.152, O.153;
ETSI: ETS 300 011, ETS 300 233, ETS 324-1, ETS 347-1, TBR 4, TBR 12, TBR 13;
GO - MVIP

T1/J1 MODE:

ANSI: T1.107, T1.231, T1.403, T1.408;
TR: TSY-000147, TSY-000191, NWT-000303, TSY-000312, TSY-000-499;
AT&T: TR 54016, TR 62411
TTC: JT-G 703, JT-G 704, JT-G706, JT-G 1431

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DESCRIPTION

The IDT82V2108 is a flexible feature-rich octal T1/E1/J1 Framer. Controlled by software, the IDT82V2108 can be globally configured as an Octal E1 or T1/J1 Framer. When E1 or T1/J1 has been set globally, the operation mode of each of the eight framers can be configured independently. The configuration is performed through a parallel Multiplexed/ Non-Multiplexed microprocessor interface.

The IDT82V2108 realizes frame synchronization, frame generation, signaling extraction and insertion, alarm and test signals generation and detection in a single chip. It also integrates up to three HDLC receivers and HDLC transmitters for each of the eight framers.

In E1 Mode, the receive path of each framer can be configured to be Basic Frame, CRC Multi-Frame and Signaling Multi-Frame. The framing can also be bypassed (unframed mode). It detects and indicates the event of out of Basic Frame Synchronization, out of CRC Multi-Frame and out of Signaling Multi-Frame. It also detects and indicates the Remote Alarm Indication signal and the Remote Signaling Multi-Frame Alarm Indication signal. The Red and AIS alarms are monitored. Basic Frame Alignment Signal errors, Far End Block Errors (FEBE) and CRC errors are counted. Up to three HDLC links are provided to extract the HDLC message on TS16, the Sa National bits and/or any arbitrary time slot. An Elastic Store Buffer that optionally supports slip buffering and adaptation to backplane timing is provided. In E1 receive path, signaling debounce, signaling freezing, idle code substitution, digital milliwatt code insertion, trunk conditioning, data inversion and pattern generation or detection are also supported on a per-timeslot basis.

In E1 mode, the transmit path of each framer can be configured to generate Basic Frame, CRC Multi-Frame and Signaling Multi-Frame. The framing can also be disabled (unframed mode). It can also transmit Remote Alarm Indication signal, Remote Signaling Multi-Frame Alarm Indication signal, AIS signal and FEBE. Up to three HDLC links are provided to insert the HDLC message on TS16, the Sa National bits and/or any arbitrary time slot. The signaling insertion, idle code substitution, data insertion, data inversion and test pattern generation or detection are also supported on a per-timeslot basis.

In E1 mode, any four of the eight framers can be multiplexed or demultiplexed to or from one of the two 8.192M bit/s buses.

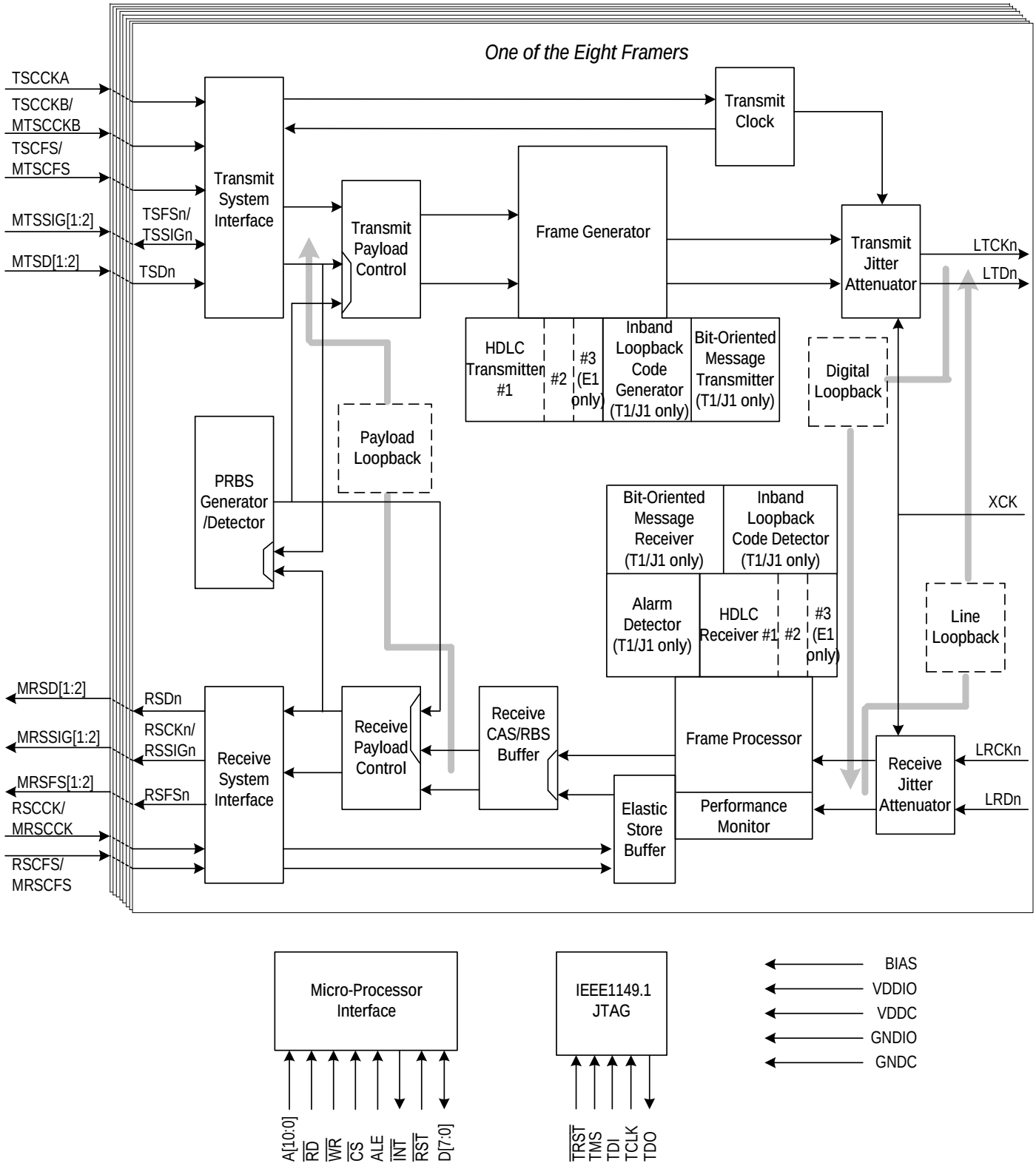
In T1/J1 mode, the receive path of each framer can be configured to be in Super Frame (SF) or Extended Super Frame (ESF) formats. The framing can also be bypassed (unframed mode). It detects and indicates the out of SF/ESF synchronization event, the Yellow, Red and AIS alarms. It also detects the presence of inband loopback codes, bit oriented message. Frame Alignment Signal errors, CRC-6 errors, out of SF/ESF events and Frame Alignment position changes are counted. Up to two HDLC links are provides to extract the HDLC message on the F-bit or any arbitrary channels in ESF format. An Elastic Store Buffer that optionally supports controlled slip and adaptation to backplane timing is provided. In T1/J1 receive path, signaling debounce, signaling freezing, idle code substitution, digital milliwatt code insertion, idle code insertion, data inversion and pattern generation or detection are also supported on a per-channel basis.

In T1/J1 mode, the transmit path of each framer can be configured to generate SF or ESF. The framing can also be disabled (unframed mode). It can also transmit Yellow signal and AIS signal. Inband loopback codes and bit oriented message can also be transmitted. Up to two HDLC links are provided to insert the HDLC message on the F-bit or any arbitrary channels in ESF format. The signaling insertion, idle code substitution, data insertion, data inversion and test pattern generation or detection are also supported on a per-channel basis.

In T1/J1 mode, the data stream of 1.544M bit/s can be converted to/from the data stream of 2.048M bit/s on the system side by software configuration. In addition, any four of the eight framers can be multiplexed or de-multiplexed to or from one of the two 8.192M bit/s buses.

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FUNCTIONAL BLOCK DIAGRAM



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1 PIN ASSIGNMENT

1.1 128 PIN PQFP PACKAGE (TOP VIEW)

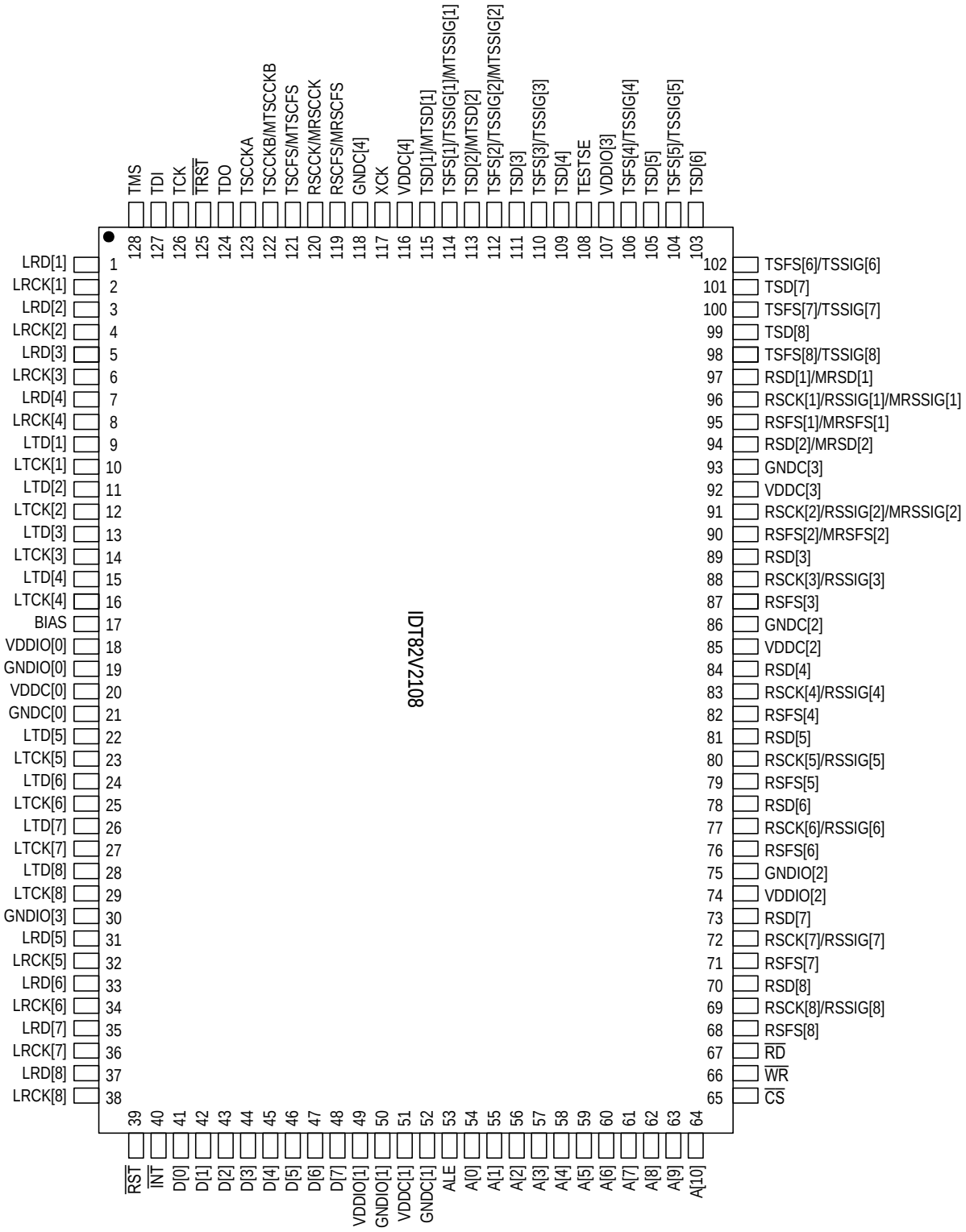


Figure 1. 128-Pin PQFP (Top View)

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1.2 144 PIN PBGA PACKAGE (BOTTOM VIEW)

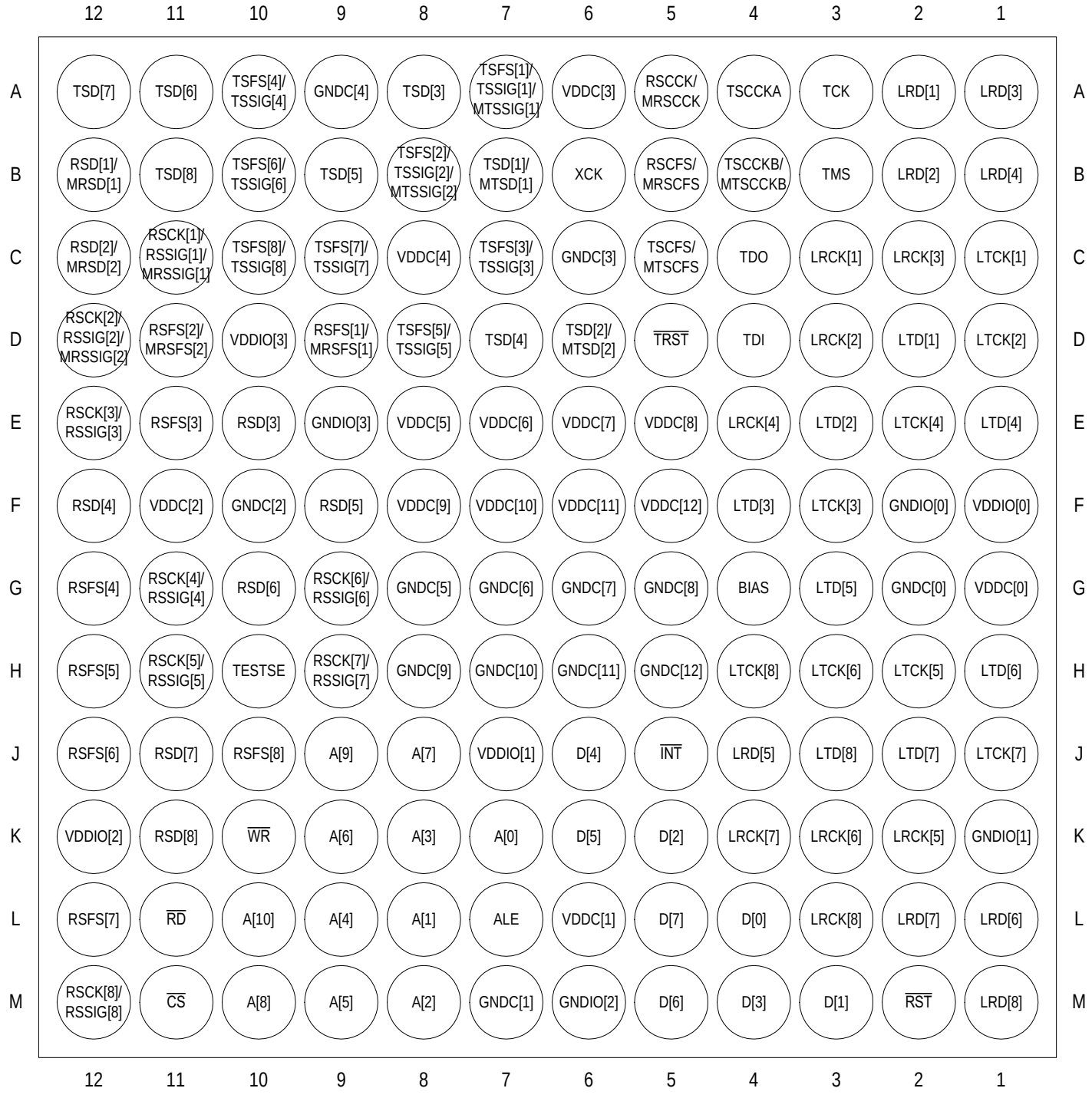


Figure 2. 144-Pin PBGA (Bottom View)

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2 PIN DESCRIPTION

Name	Type	Pin No.		Description
		PQFP	PBGA	
Line and System Interface				
LRD[1] LRD[2] LRD[3] LRD[4] LRD[5] LRD[6] LRD[7] LRD[8]	Input	1 3 5 7 31 33 35 37	A2 B2 A1 B1 J4 L1 L2 M1	LRD[1:8]: Line Receive Data for Framer 1 ~ 8 These pins receive the data stream from line interface units or from a higher demultiplex interface. Data on these pins are sampled on the active edge of the corresponding LRCKn.
LRCK[1] LRCK[2] LRCK[3] LRCK[4] LRCK[5] LRCK[6] LRCK[7] LRCK[8]	Input	2 4 6 8 32 34 36 38	C3 D3 C2 E4 K2 K3 K4 L3	LRCK[1:8]: Line Receive Clock for Framer 1 ~ 8 These pins receive externally recovered line clock (2.048 or 1.544 MHz). The clock is used to sample the data on the corresponding LRDn.
RSCK[1] / RSSIG[1] / MRSSIG[1] RSCK[2] / RSSIG[2] / MRSSIG[2] RSCK[3] / RSSIG[3] RSCK[4] / RSSIG[4] RSCK[5] / RSSIG[5] RSCK[6] / RSSIG[6] RSCK[7] / RSSIG[7] RSCK[8] / RSSIG[8]	Output	96 91 88 83 80 77 72 69	C11 D12 E12 G11 H11 G9 H9 M12	RSCK[1:8]: Receive Side System Clock for Framer 1 ~ 8 In Receive Clock Master Full E1 or T1/J1 mode, the clock is a smoothed version of the corresponding 2.048 or 1.544 MHz Line Receive Clock (LRCKn). The RSCKn is pulsed for each bit in the 256-bit or 193-bit frame. The corresponding RSFSn and RSDn pins are updated on the active edge of RSCKn. In Receive Clock Master Nx64K mode, the clock is a gapped version of the associated smoothed LRCKn. The pulse number of RSCKn in each frame is controllable from 0 to 255 or from 0 to 192 on a per-timeslot/channel basis. The corresponding RSFSn and RSDn pins are updated on the active edge of RSCKn. In Receive Clock Slave RSCK Reference mode, RSCKn can be selected to be either a 2.048/1.544 MHz jitter attenuated version of the corresponding LRCKn or an 8KHz clock divided down from the smoothed line clock LRCKn. RSSIG[1:8]: Receive Side System Signaling for Framer 1 ~ 8 In Receive Clock Slave External Signaling mode, the extracted signaling is output on these pins. The signal on these pins is timeslot/channel-aligned with the data output on the corresponding RSDn pin and is updated on the active edge of RSCCK. The extracted signaling is located in the lower nibble (b5 ~ b8). In E1 mode, the extracted signaling repeats during the entire Signaling Multi-Frame for the same time slot. In T1/J1 mode, the extracted signaling repeats during the entire SF/ESF for the same channel. MRSSIG[1:2]: Multiplexed Receive Side System Signaling When the multiplexed bus structure is configured, the extracted signaling data from the selected framers are multiplexed on these pins using a byte-interleaved multiplexing scheme. The data on MRSSIG[1:2] are updated on the active edge of MRSCCK.
RSD[1] / MRSD[1] RSD[2] / MRSD[2] RSD[3] RSD[4] RSD[5] RSD[6] RSD[7] RSD[8]	Output	97 94 89 84 81 78 73 70	B12 C12 E10 F12 F9 G10 J11 K11	RSD[1:8]: Receive Side System Data for Framer 1 ~ 8 The processed data stream is output on these pins. In Receive Clock Master mode, RSDn is updated on the active edge of the corresponding RSCKn. In Receive Clock Slave mode, RSDn is updated on the active edge of RSCCK. MRSD[1:2]: Multiplexed Receive Side System Data When the multiplexed bus structure is configured, the processed data stream from the selected framers is multiplexed on these pins using the byte-interleaved multiplexing scheme. The data on MRSD[1:2] are updated on the active edge of MRSCCK.

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Name	Type	Pin No.		Description
		PQFP	PBGA	
RSFS[1] / MRSFS[1] RSFS[2] / MRSFS[2] RSFS[3] RSFS[4] RSFS[5] RSFS[6] RSFS[7] RSFS[8]	Output	95 90 87 82 79 76 71 68	D9 D11 E11 G12 H12 J12 L12 J10	RSFS[1:8]: Receive Side System Frame Pulse for Framer 1 ~ 8 In E1 mode, RSFSn can be configured to indicate the beginning of Basic Frame, or CRC Multi-Frame or/and Signaling Multi-Frame for data stream on RSDn. When configured for the Basic Frame, RSFSn will pulse high/low during the first bit of each Basic Frame. When configured for CRC Multi-Frame, RSFSn will pulse during the first bit of the first frame of the CRC Multi-Frame. When configured for the Signaling Multi-Frame, RSFSn will pulse during the first bit of the first frame of the Signaling Multi-Frame. When configured to indicate both Signaling and CRC Multi-Frame, RSFSn will go high/low on the first bit of the first frame of the Signaling Multi-Frame and go the opposite after the first bit of the first frame of the CRC Multi-Frame. In T1/J1 mode, RSFSn can be configured to indicate each F-bit, or the first F-bit of every 12-frame SFs / every 24-frame ESFs. RSFSn pulses during the above F-bit. In both E1 and T1/J1 modes, when Receive Clock Master mode is active, RSFSn is updated on the active edge of the corresponding RSCKn. When Receive Clock Slave mode is active, RSFSn is updated on the active edge of RSCCK. MRSFS[1:2]: Multiplexed Receive Side System Frame Pulse When the multiplexed bus structure is configured, the signals on these pins indicate the beginning of a multiplexed frame. MRSFS[1:2] are updated on the active edge of MRSCCK.
RSCCK / MRSCCK	Input	120	A5	RSCCK: Receive Side System Common Clock RSCCK is used only in Receive Clock Slave mode. In E1 mode, it is a 2.048 or 4.096 MHz clock. In T1 mode, it is a 1.544 or 2.048 or 4.096 MHz clock. In Receive Clock Slave RSCK Reference mode, RSDn and RSFSn are updated and RSCFS is sampled on the active edge of RSCCK. In Receive Clock Slave External Signaling mode, RSDn, RSFSn and RSSIGn are updated and RSCFS is sampled on the active edge of RSCCK. MRSCCK: Multiplexed Receive Side System Common Clock When the multiplexed bus structure is configured, MRSCCK is an 8.192 or 16.384 MHz clock for the receive system multiplexed bus. MRSCFS is sampled and MRSD[1:2], MRSFS[1:2] and MRSSIG[1:2] are updated on the active edge of MRSCCK.
RSCFS / MRSCFS	Input	119	B5	RSCFS: Receive Side System Common Frame Pulse In Receive Clock Slave mode, RSCFS can be selected as a frame alignment reference. It is asserted on the request of each Basic Frame or each Multi-Frame in E1 mode, or it is asserted on the request of F-bit in T1/J1 mode. RSCFS is sampled on the active edge of RSCCK. MRSCFS: Multiplexed Receive Side System Common Frame Pulse When the multiplexed bus structure is configured, the signal on this pin aligns the multiplexed frame to the backplane timing. MRSCFS is sampled on the active edge of MRSCCK.
TSD[1] / MTSD[1] TSD[2] / MTSD[2] TSD[3] TSD[4] TSD[5] TSD[6] TSD[7] TSD[8]	Input	115 113 111 109 105 103 101 99	B7 D6 A8 D7 B9 A11 A12 B11	TSD[1:8]: Transmit Side System Data for Framer 1 ~ 8 The data streams from the system backplane are input on these pins. In Transmit Clock Master mode, TSDn is sampled on the active edge of the corresponding LTCKn. In Transmit Clock Slave mode, TSDn is sampled on the active edge of TSCCKB. MTSD[1:2]: Multiplexed Transmit Side System Data When the multiplexed bus structure is configured, the data stream from the backplane is carried on the multiplexed bus for the selected framers. MTSD[1:2] are sampled on the active edge of MTSCCKB.

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Name	Type	Pin No.		Description
		PQFP	PBGA	
TSFS[1] / TSSIG[1] / MTSSIG[1] TSFS[2] / TSSIG[2] / MTSSIG[2] TSFS[3] / TSSIG[3] TSFS[4] / TSSIG[4] TSFS[5] / TSSIG[5] TSFS[6] / TSSIG[6] TSFS[7] / TSSIG[7] TSFS[8] / TSSIG[8]	Output / Input	114 112 110 106 104 102 100 98	A7 B8 C7 A10 D8 B10 C9 C10	TSFS[1:8]: Transmit Side System Frame Pulse for Framer 1 ~ 8 In Transmit Clock Master mode, TSFSn indicates the beginning of each Basic Frame in E1 mode, or indicates the F-bit of SF/ESF in T1/J1 mode. TSFSn is updated on the active edge of the corresponding LTCKn. In Transmit Clock Slave TSFS Enabled mode, TSFSn indicates the beginning of each Basic Frame in E1 mode, or indicates the F-bit of SF/ESF in T1/J1 mode. TSFSn is updated on the active edge of TSCCKB. TSSIG[1:8]: Transmit Side System Signaling for Framer 1 ~ 8 In Transmit Clock Slave External Signaling mode, these are the TSSIG inputs. The signaling is located in the lower nibble (b5 ~ b8) and sampled on the active edge of TSCCKB. In E1 mode, the signaling repeats during the entire Signaling Multi-Frame for the same time slot. In T1/J1 mode, the signaling repeats during the entire SF/ESF for the same channel. MTSSIG[1:2]: Multiplexed Transmit Side System Signaling When the multiplexed bus structure is configured, the signaling on the bus is organized in a byte-interleaved scheme for the selected framers. MTSSIG[1:2] are sampled on the active edge of MTSCCKB.
TSCCKA	Input	123	A4	TSCCKA: Transmit Side System Common Clock A TSCCKA is one of the reference clocks for the transmit jitter attenuator DPLL. TSCCKA can be configured to input the clock as: 1. 16.384MHz clock; 2. Line rate: 2.048MHz (for E1) or 1.544MHz (for T1); 3. Nx8KHz (N is from 1 to 256) so long as TSCCKA is a jitter-free clock. The IDT82V2108 can be configured to ignore TSCCKA and utilize LRCK and TSCCKB instead. TSCCKA is replaced by LRCK if line loopback is enabled.
TSCCKB / MTSCCKB	Input	122	B4	TSCCKB: Transmit Side System Common Clock B In E1 mode, TSCCKB is a 2.048 or 4.096 MHz clock. In T1/J1 mode, TSCCKB is a 1.544 or 2.048 or 4.096 MHz clock. In Transmit Clock Slave TSFS mode, TSDn and TSCFS are sampled and TSFSn is updated on the active edge of TSCCKB. In Transmit Clock Slave External Signaling mode, TSDn, TSSIGn and TSCFS are sampled on the active edge of TSCCKB. MTSCCKB: Multiplexed Transmit Side System Common Clock B When the multiplexed bus structure is configured, MTSCCKB is an 8.192 or 16.384 MHz reference clock for the transmit system multiplexed bus. MTSCFS, MTSD[1:2] and MTSSIG[1:2] are sampled on the active edge of MTSCCKB.
TSCFS / MTSCFS	Input	121	C5	TSCFS: Transmit Side System Common Frame Pulse In Transmit Clock Slave mode, TSCFS is used to frame align all the framers to the system backplane. In E1 mode, the pulse can be configured to indicate the first bit of a Basic Frame, CRC Multi-Frame / Signaling Multi-Frame. In T1/J1 mode, the pulse can be configured to indicate the first bit of SF/ESF. The width of the pulse must be at least 1 TSCCKB cycle wide. TSCFS is sampled on the active edge of TSCCKB. MTSCFS: Multiplexed Transmit Side System Common Frame Pulse When the multiplexed bus structure is configured, MTSCFS is used to frame align the multiplexed frames to the system backplane. MTSCFS is sampled on the active edge of MTSCCKB.
LTD[1] LTD[2] LTD[3] LTD[4] LTD[5] LTD[6] LTD[7] LTD[8]	Output	9 11 13 15 22 24 26 28	D2 E3 F4 E1 G3 H1 J2 J3	LTD[1:8]: Line Transmit Data for Framer 1 ~ 8 These pins output the data stream to line interface units or a higher multiplex interface. The data on LTDn is updated on the active edge of the corresponding LTCKn.

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Name	Type	Pin No.		Description
		PQFP	PBGA	
LTCK[1] LTCK[2] LTCK[3] LTCK[4] LTCK[5] LTCK[6] LTCK[7] LTCK[8]	Output	10 12 14 16 23 25 27 29	C1 D1 F3 E2 H2 H3 J1 H4	LTCKn: Line Transmit Clock for Framer 1 ~ 8 It is a nominal E1 (2.048MHz) or T1/J1 (1.544MHz) clock. LTCK can be derived from TSCCKA, TSCCKB, LRCK or XCK. On the active edge of LTCKn, the corresponding LTDn is updated.
XCK	Input	117	B6	XCK: Crystal Clock The clock frequency equals 49.152MHz ± 50 ppm 50% duty cycle for E1 and 37.056MHz ± 32 ppm 50% duty cycle for T1/J1.
Microprocessor Interface				
$\overline{RST}$	Input	39	M2	**$\overline{RST}$**: Reset (Active Low) A low signal for at least 100 ns on this pin will reset the device anytime. $\overline{RST}$ is a Schmitt-trigger input with weak pull-up.
$\overline{CS}$	Input	65	M11	**$\overline{CS}$**: Chip Select (Active Low) This pin must be asserted low to enable the microprocessor interface. The signal must be asserted high at least once after power up to clear the internal test modes. A transition from high to low must occur on this pin for each Read/Write operation and can not return to high until the operation is over.
$\overline{INT}$	Output	40	J5	**$\overline{INT}$**: Open-Drain Interrupt Signal (Active Low) This pin will keep low until all the active unmasked interrupt are acknowledged at their sources.
A[0] A[1] A[2] A[3] A[4] A[5] A[6] A[7] A[8] A[9] A[10]	Input	54 55 56 57 58 59 60 61 62 63 64	K7 L8 M8 K8 L9 M9 K9 J8 M10 J9 L10	A[10:0]: Address Bus The signals on these pins select the register for the microprocessor to access.
D[0] D[1] D[2] D[3] D[4] D[5] D[6] D[7]	Output / Input	41 42 43 44 45 46 47 48	L4 M3 K5 M4 J6 K6 M5 L5	D[7:0]: Bi-directional Data Bus Signals on these pins are the data for Read/Write operation.
$\overline{RD}$	Input	67	L11	**$\overline{RD}$**: Read Strobe (Active Low) A low signal on this pin enables a read operation on the selected register.
$\overline{WR}$	Input	66	K10	**$\overline{WR}$**: Write Strobe (Active Low) A low signal on this pin enables a write operation on the selected register.
ALE	Input	53	L7	ALE: Address Latch Enable In non-multiplexed address/data bus, the ALE is connected to High. It is internally pulled-up.
JTAG (per IEEE 1149.1)				

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Name	Type	Pin No.		Description
		PQFP	PBGA	
$\overline{TRST}$	Input	125	D5	**$\overline{TRST}$**: Test Reset (Active Low) A low signal on this pin will reset the JTAG test port anytime. This pin is a Schmitt-triggered input with an internal pull-up resistor. It must be connected to the $\overline{RST}$ pin or ground when JTAG is not used.
TMS	Input	128	B3	TMS: Test Mode Select The signal on this pin controls the JTAG test performance and is clocked into the device on the rising edge of the TCK. This pin has an internal pull-up resistor.
TCK	Input	126	A3	TCK: Test Clock The clock for the JTAG test is input on this pin. The TDI and the TMS are clocked into the device on the rising edge of the TCK and the TDO is clocked out of the device on the falling edge of the TCK.
TDI	Input	127	D4	TDI: Test Input The test data are input on this pin. It is sampled on the rising edge of the TCK. This pin has an internal pull-up resistor.
TDO	Tri-State	124	C4	TDO: Test Output The test data are output on this pin. It is sampled on the falling edge of the TCK. This pin is in tri-state mode, except during the process of scanning of the data.
Power & Ground				
BIAS	Power	17	G4	BIAS: +5V Bias This pin enables +5 V tolerance on the inputs. When +5 V tolerance inputs are required, the BIAS must be connected to a well-decoupled +5 V rail. When +3 V input is required, the BIAS must be connected to a well-decoupled +3.3 V DC supply. During power up, the BIAS pin should be powered no later than any VDDC/VDDIO pin is powered.
VDDIO[0] VDDIO[1] VDDIO[2] VDDIO[3]	Power	18 49 74 107	F1 J7 K12 D10	VDDIO[3:0]: These pins must be connected to a common, well-decoupled +3.3 V DC supply together with the core power pins VDDC[4:0] externally.
VDDC[0] VDDC[1] VDDC[2] VDDC[3] VDDC[4] VDDC[5:12]	Power	20 51 85 92 116 -	G1 L6 F11 A6 C8 E8 E7 E6 E5 F8 F7 F6 F5	VDDC[4:0]: These pins must be connected to a common, well-decoupled +3.3 V DC supply together with the pad ring power pins VDDIO[3:0] externally. The VDDC[5:12] are extra power pins for PBGA.
GNDIO[0] GNDIO[1] GNDIO[2] GNDIO[3]	Ground	19 50 75 30	F2 K1 M6 E9	GNDIO[3:0]: These pins must be connected to a common ground together with the core ground pins GNDC[4:0].

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Name	Type	Pin No.		Description
		PQFP	PBGA	
GNDC[0] GNDC[1] GNDC[2] GNDC[3] GNDC[4] GNDC[5:12]	Ground	21 52 86 93 118 - 	G2 M7 F10 C6 A9 G8 G7 G6 G5 H8 H7 H6 H5	GNDC[4:0]: These pins must be connected to a common ground together with the pad ring ground pins GNDIO[3:0]. The GNDC[5:12] are extra ground pins for PBGA.
TEST				
TESTSE	Input	108	H10	This pin is connected to ground for normal operation and reserved for testing.

Note:
1. All outputs have 4 mA drive capability except for the D[7:0], the LTCK[1:8] and the RSCK[1:8] pins which have 6 mA drive capability.
2. All input and bi-directional pins present minimum capacitive loading.

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3 FUNCTIONAL DESCRIPTION

3.1 T1 / E1 / J1 MODE SELECTION

The IDT82V2108 can be configured as a duplex eight ports E1 framer, or a duplex eight ports T1 framer, or a duplex eight ports J1 framer. When the TMODE (b0, 400H)[1] is set to '0', the device is in E1 mode. When the TMODE (b0, 400H) is set to '1', the device is in T1/J1 mode (default mode). In T1/J1 mode, when the JYEL (b3, T1/J1-020H) and the J1_YEL (b5, T1/J1-02CH) are both set to '0', the receive path of the corresponding framer is in T1 mode; when the JYEL (b3, T1/J1-020H) and the J1_YEL (b5, T1/J1-02CH) are both set to '1', the receive path of the corresponding framer is in J1 mode; when the J1_CRC (b6, T1/J1-044H) and the J1_YEL (b5, T1/J1-044H) are both set to '0', the transmit path of the corresponding framer is in T1 mode; when the J1_CRC (b6, T1/J1-044H) and the J1_YEL (b5, T1/J1-044H) are both set to '1', the transmit path of the corresponding framer is in J1 mode.

3.2 FRAME PROCESSOR (FRMP)

The Frame Processor of each framer operates independently.

3.2.1 E1 MODE

In E1 mode, the Frame Processor searches for Basic Frame synchronization, CRC Multi-Frame synchronization, and Channel Associated Signaling (CAS) Multi-Frame synchronization in the received data stream. Figure 3 shows the searching process.

Once the frame is synchronized, the Frame Processor keeps on monitoring the received data stream. The Frame Processor will indicate framing bit errors, CAS Multi-Frame alignment pattern errors, CRC Multi-Frame alignment pattern errors or CRC errors, if any. The status of loss of frame, loss of Signaling Multi-Frame and loss of CRC Multi-Frame can also be detected and declared based on user-selectable criteria. The reframe operation can be initiated by excessive CRC errors, or the CRC Multi-Frame alignment is not found within 400ms. A software reset will also make the Frame Processor reframe.

The Frame Processor can extract the data stream in TS16, and output the extracted data on a separate pin. The Frame Processor also extracts the contents of the International bits (from both the FAS and the NFAS frames), the National bits and the Extra bits (from TS16 in the frame 0 of the Signaling Multi-Frame), and stores these data in registers. The CRC Sub Multi-Frame alignment 4-bit codeword in the National bit positions Sa4 to Sa8 can also be extracted and stored in registers, and updated every CRC Sub Multi-Frame.

The Framer Processor identifies the Remote Alarm bit (bit 3 of TS0 of NFAS frames) and Remote Signaling Multi-Frame Alarm (bit 6 of TS16 of frame 0 of Signaling Multi-Frame). The "de-bounced" Remote Alarm and Remote Signaling Multi-Frame Alarm can be indicated if the corresponding bit has been a certain logic for consecutive 2 or 3 times. The AIS (Alarm Indication Signal) can also be detected, and if the AIS condition has persisted for at least 100 ms, an AIS Alarm is declared. The Frame Processor can also declare a Red Alarm if the out-of-frame condition has persisted for at least 100 ms.

An interrupt output is provided to indicate status changes and the occurrence of some events. The interrupts may be generated every Basic Frame, CRC Sub Multi-Frame, CRC Multi-Frame or Signaling Multi-Frame.

The Frame Processor can also be bypassed to receive unframed data.

Note:

1. The contents in the brackets indicate the position of this bit and the address of the register. If more than one register contains the same bit, the address is only for the first register, the addresses of the remaining registers are listed together with the first register in the Register Description paragraph.

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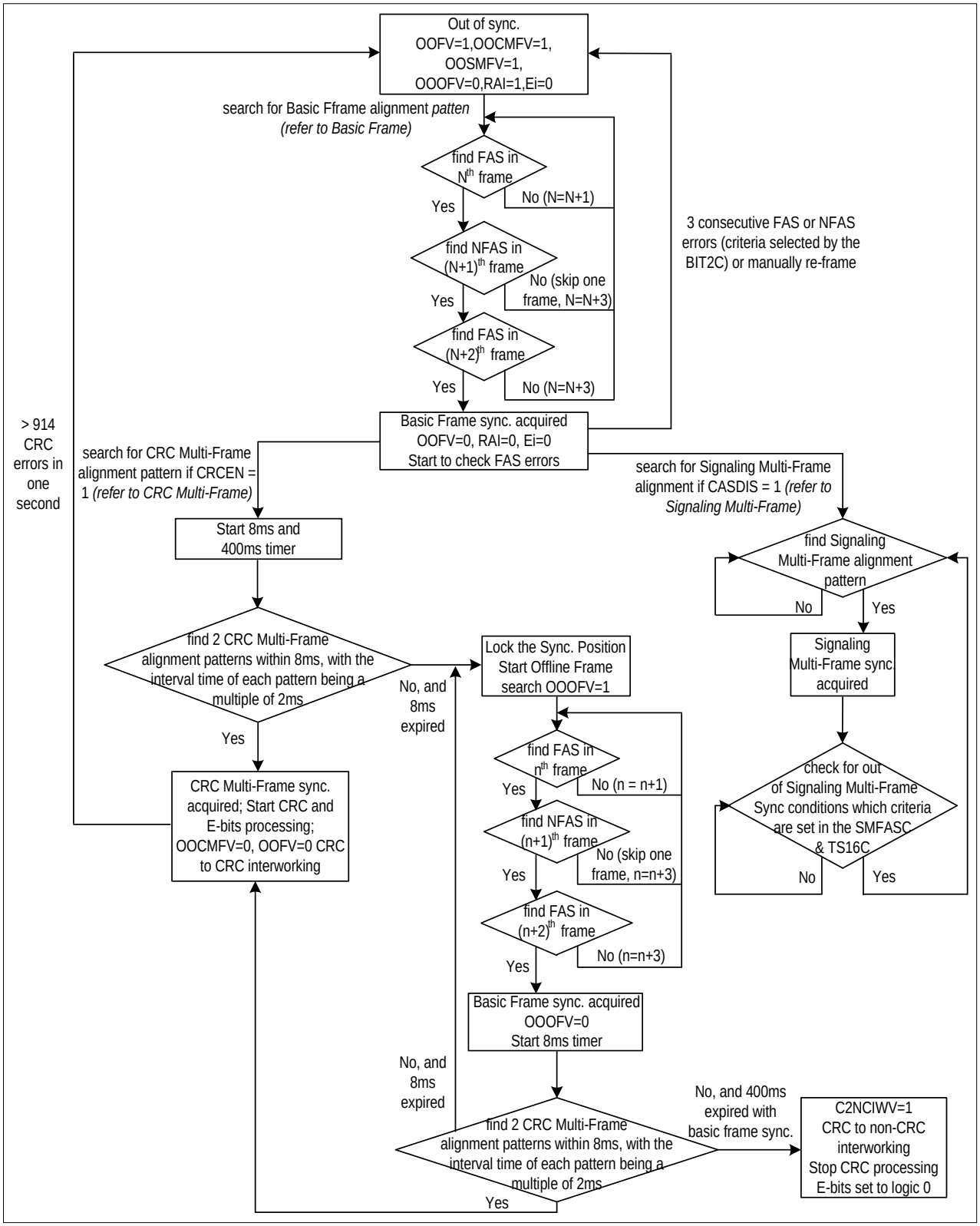


Figure 3. E1 Frame Searching Process

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3.2.1.1 Synchronization Searching

All the frame synchronization functions can only be executed when the UNF (b6, E1-000H) is '0'.

3.2.1.1.1 Basic Frame

The algorithm of searching for the E1 Basic Frame alignment pattern (as shown in Figure 4) meets the ITU-T Recommendation G.706 4.1.2 and 4.2.

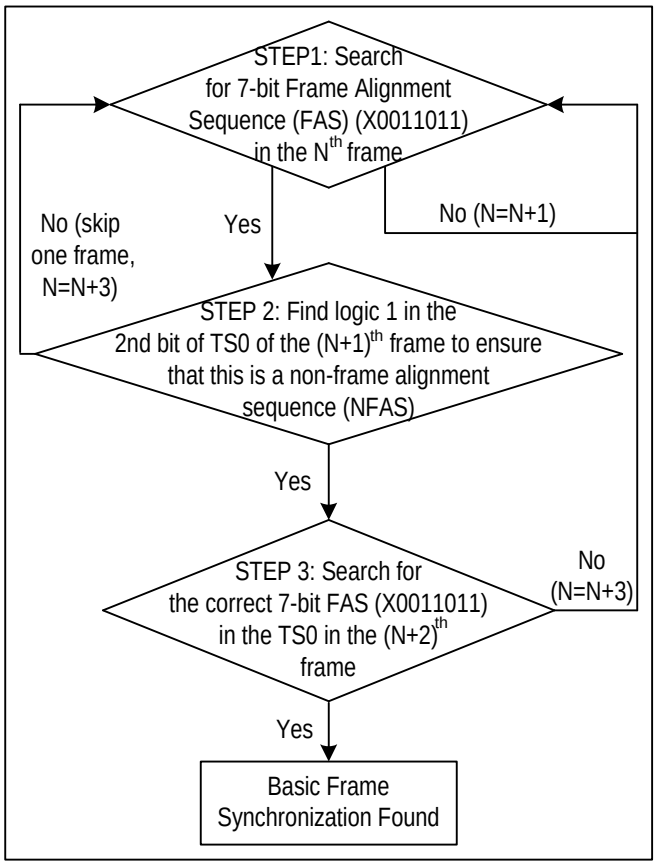


Figure 4. Basic Frame Searching Process

Generally, it is performed by detecting a successive FAS/NFAS/FAS sequence. If STEP 2 is not met, a new search will start after the following frame is skipped. If STEP 3 is not met, a new search will start immediately in the next frame. Once the Basic Frame alignment pattern is detected in the received PCM data stream, the Basic Frame synchronization is acquired and the OOFV (b6, E1-036H) will be set to '0' for indication. Then, this block goes on monitoring the received data stream. If the received Basic Frame alignment signal does not meet its pattern, the FERI (b2, E1-034H) will be set to '1'. The criteria of out of Basic Frame synchronization are determined by the BIT2C (b6, E1-031H). If one of the conditions set in the BIT2C (b6, E1-031H) is met, the search process will restart when the REFRDIS (b0, E1-030H) is '0'. Excessive CRC errors will also lead to re-searching for Basic Frame (refer to Chapter 3.2.1.1.2 CRC Multi-Frame for details).

However, the Basic Frame synchronization can also be forced to re-search for a new Basic Frame any time when there is a transition from '0' to '1' on the REFR (b2, E1-030H).

3.2.1.1.2 CRC Multi-Frame

The CRC Multi-Frame is provided to enhance the ability of verifying data stream. The structure of TS0 of CRC Multi-Frame is illustrated in Table 1:

A CRC Multi-Frame consists of 16 continuous Basic Frames (No. 0 ~ 15), which are numbered from a Basic Frame with FAS. Each CRC Multi-Frame can be divided into two Sub Multi-Frames (SMF I & SMF II).

The first bit of TS0 of each frame is called International (Si) bit. The Si bit in each even frame is the CRC bit. Thus, there are C1, C2, C3, C4 in each SMF. The C1 is the most significant bit, while the C4 is the least significant bit. The Si bits in the first six odd frames are the CRC Multi-Frame alignment pattern. The pattern is '001011'. The Si bits in Frame 13 and Frame 15 are E1 and E2 bits respectively. The E bits' value indicates the Far End Block Errors (FEBE).

After the Basic Frame has been synchronized, the Frame Processor initiates an 8 and 400ms timer to check the CRC Multi-Frame alignment signal if the CRCEN (b7, E1-030H) is '1'. The CRC Multi-Frame synchronization is declared with a '0' in the OOCMFV (b4, E1-036H) only if at least two CRC Multi-Frame alignment patterns are found within 8ms, with the interval time of each pattern being a multiple of 2ms. Then if the received CRC Multi-Frame alignment signal does not meet its pattern, the CMFERI (b0, E1-034H) will be set to '1'. The Frame Processor calculates the data in the SMF(N) per the algorithm in G.704 and G.706 to get a four-bit remainder, then compares the four-bit remainder with the C1, C2, C3, C4 in the next SMF. If there is a difference between them, bit errors exist in SMF(N) and a CRC error is counted. The CRCERR[9:0] (b7~0, E1-039H & b1~0, E1-03AH) are used to indicate the CRC error numbers and are updated every second. Once the CRCERR[9:0] (b7~0, E1-039H & b1~0, E1-03AH) are updated, a '1' will be set in the NEWDATA (b6, E1-03AH) for indication. If the CRCERR[9:0] are over-written, the OVR (b7, E1-03AH) will be asserted. When more than 914 CRC errors occur in one second which is indicated in the EXCRCERR (b0, E1-031H), a new search for the Basic Frame alignment pattern will start if the REFCRCE (b1, E1-030H) is set to '1' and the REFRDIS (b0, E1-030H) is set to '0'.

If the 2 CRC Multi-Frame alignment patterns can not be found within 8ms with the interval time being a multiple of 2ms, an offline search for the Basic Frame alignment pattern will start which is indicated in the OOOFV (b3, E1-036H). The process is the same as shown in Figure 4. This offline operation searches in parallel with the pre-found Basic Frame synchronization searching process. After the new Basic Frame synchronization is acquired by this offline search, the 8ms timer is restarted to check whether the two CRC Multi-Frame alignment patterns are found within 8ms, with the interval time of each pattern being a multiple of 2ms again. If the condition can not be met, the procedure will go on until the 400ms timer ends. If the condition still can not be met at that time and the Basic Frame is still synchronized, the device declares by the C2NCIWV (b7, E1-036) to run under the CRC to non-CRC interworking process. In this process, the CRC Multi-Frame alignment pattern can still be searched if the C2NCIWCK (b5, E1-030H) is set to '1'.

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Table 1: Structure of TS0 of CRC Multi-Frame

	SMF	Basic Frame No. / Type	the Eight Bits in Time Slot 0							
			1 (Si bit)	2	3	4	5	6	7	8
CRC-4 Multi-Frame	SMF I	0 / FAS	C1	0	0	1	1	0	1	1
		1 / NFAS	0	1	A	Sa4	Sa5	Sa6	Sa7	Sa8
		2 / FAS	C2	0	0	1	1	0	1	1
		3 / NFAS	0	1	A	Sa4	Sa5	Sa6	Sa7	Sa8
		4 / FAS	C3	0	0	1	1	0	1	1
		5 / NFAS	1	1	A	Sa4	Sa5	Sa6	Sa7	Sa8
		6 / FAS	C4	0	0	1	1	0	1	1
		7 / NFAS	0	1	A	Sa4	Sa5	Sa6	Sa7	Sa8
	SMF II	8 / FAS	C1	0	0	1	1	0	1	1
		9 / NFAS	1	1	A	Sa4	Sa5	Sa6	Sa7	Sa8
		10 / FAS	C2	0	0	1	1	0	1	1
		11 / NFAS	1	1	A	Sa4	Sa5	Sa6	Sa7	Sa8
		12 / FAS	C3	0	0	1	1	0	1	1
		13 / NFAS	E1	1	A	Sa4	Sa5	Sa6	Sa7	Sa8
		14 / FAS	C4	0	0	1	1	0	1	1
		15 / NFAS	E2	1	A	Sa4	Sa5	Sa6	Sa7	Sa8

3.2.1.1.3 CAS Signaling Multi-Frame

If the CRCEN (E1-030H) is '1', after the CRC Multi-Frame has been found, the Frame Processor starts to search for Signaling Multi-Frame alignment pattern when the CASDIS (E1-030H) is '0'. If the CRCEN is '0', after the Basic Frame has been found, the Frame Processor starts to search for Signaling Multi-Frame alignment signal when the CASDIS (E1-030H) is '0'. Refer to Figure 3.

The Signaling Multi-Frame alignment pattern is located in the 1 – 4 bits of TS16 of Frame 0 of Signaling Multi-Frame. The pattern is '0000'. Once the pattern is detected, the Signaling Multi-Frame synchronization is acquired which is indicated with a logic '0' in the OOSMFV (b5, E1-036H). If the received Signaling Multi-Frame alignment signal does not meet its pattern, the SMFERI (b1, E1-034H) will be set to '1'. The entire content in TS16 of Frame 0 of Signaling Multi-Frame is '0000XYXX'. The 'Y' is for remote Signaling Multi-Frame alarm indication and the 'X's are extra bits.

A new search of Signaling Multi-Frame alignment pattern is initiated when the out of the Signaling Multi-Frame criteria set in the SMFASC (b5, E1-031H) and the TS16C (b4, E1-031H) are met or when it is out of Basic Frame synchronization.

3.2.1.2 Alarms & Bit Extraction

3.2.1.2.1 RED Alarm

RED alarm is declared when the out of Basic Frame synchronization condition has persisted for 100 ms. RED alarm is removed when the out of Basic Frame synchronization condition has been absent for 100 ms. The RED alarm status is reflected in the RED (b3, E1-037H).

The received data stream is out of Basic Frame synchronization when any of the following conditions is met:

1) The Basic Frame has not been synchronized.

2) The received data stream meets the out of Basic Frame synchronization criteria set in the BIT2C (b6, E1-031H).

3) There are excessive CRC errors in the received data stream.

Any one of the three conditions will be indicated by the OOFV (b6, E1-036H).

The integration of RED alarm uses the following algorithm: The algorithm monitors the occurrence of out of Basic Frame over a 4 ms interval. A valid out of Basic Frame presence is accumulated when one or more out of Basic Frame indications occurred during the 4 ms interval. Each valid out of Basic Frame presence increases one accumulation. An invalid out of Basic Frame presence is also accumulated when there is no out of Basic Frame indication occurring during the 4 ms inverval. Each invalid out of Basic Frame indication decreases one accumulation (until the accumulation is zero). The RED alarm is declared when 25 valid out of Basic Frame presences have been accumulated. The RED alarm is removed when the out of Basic Frame presences reaches 0.

3.2.1.2.2 AIS Alarm

The AIS density criteria are determined by the AISC (b1, E1-031H). That is, if it is out of Basic Frame synchronization and less than 3 zeros are detected in a 512-bit stream, or if it is out of Basic Frame synchronization and less than 3 zeros are detected in each of 2 consecutive 512-bit streams, the status will be reported by the AISD (b5, E1-037H).

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When the above status has lasted for 100 ms, AIS alarm is declared with a logic '1' in the AIS (b2, E1-037H). However, in unframed mode, the detection of AIS alarm is disabled.

3.2.1.2.3 Bit Extraction

The Frame Processor extracts the National Bit codeword (Sa4[1:4] to Sa8[1:4] in the CRC Sub Multi-Frame), the International bit (Si), the National bit (Sa), the Remote Alarm Indication bit (A), the Extra bits (X) and the Remote Signaling Multi-Frame Alarm Indication bit (Y).

- National Bit Codeword

The Frame Processor extracts one of the National Bit codewords (Sa4[1:4] to Sa8[1:4] in the CRC Sub Multi-Frame) to the SaX[1:4] (b3~0, E1-03DH). Here the 'X' is selected from 4 to 8 by the SaSEL[2:0] (b7~5, E1-03BH). The SaX[1:4] (b3~0, E1-03DH) are debounced. They are updated only when two consecutive codewords are the same.

- International Bit

The International bits (Si) are extracted to the Si[1:0] (b7~6, E1-038H). The Si[1:0] (b7~6, E1-038H) are updated on the boundary of the associated FAS/NFAS frame and are not updated when out of frame is reported.

- National Bit

The National bits (Sa) are extracted to the Sa[4:8] (b4~0, E1-038H). The Sa[4:8] (b4~0, E1-038H) are updated on the boundary of the associated NFAS frame and are not updated when out of frame is reported.

- Remote Alarm Indication Bit

The Remote Alarm Indication bit (A) is extracted to the A (b5, E1-038H). The A (b5, E1-038H) is updated on the boundary of the associated NFAS frame.

- Extra Bit

The Extra bits (X) are extracted to the X[0:2] (b5 & b3~2, E1-03AH). The X[0:2] (b5 & b3~2, E1-03AH) are updated on the beginning of the Frame1 (next NFAS frame).

- Remote Signaling Multi-Frame Alarm Indication Bit

The Remote Signaling Multi-Frame Alarm Indication bit (Y) is extracted to the Y (b4, E1-03AH). The Y (b4, E1-03AH) is updated on the beginning of the Frame1 (next NFAS frame).

3.2.1.2.4 V5.2 Link

The V5.2 link ID signal, i.e. 2 out of 3 Sa7 bits being logic 0, is detected with the indication in the V52LINKV (b0, E1-036H).

3.2.1.3 Interrupt Sources

24 kinds of interrupts are derived from this block as shown in Table 2. When there are conditions meeting the interrupt sources, the corresponding Status bit will be asserted high. When there is a transition ('1' to '0' or '0' to '1') on the Status bit, the corresponding Status Interrupt Indication bit will be set to logic 1 (If the Status bit does not exist, the source will cause its Status Interrupt Indication bit to logic 1 directly) and the Status Interrupt Indication bit will be cleared when it is read. A logic 1 in the Status Interrupt Indication bit means an interrupt occurred. The interrupt will be reported by the $\overline{INT}$ pin if its Status Interrupt Enable bit is logic 1.

Table 2: Interrupt Sources in the E1 Frame Processor

No.	Sources	Status Bit	Interrupt Indication Bit	Interrupt Enable Bit
1	The received Basic Frame alignment signal does not meet its pattern once Basic Frame synchronization is achieved.	-	FERI (b2, E1-034H)	FERE (b2, E1-032H)
2	The received CRC Multi-Frame alignment signal does not meet its pattern once CRC Multi-Frame synchronization is achieved.	-	CMFERI (b0, E1-034H)	CMFERE (b0, E1-032H)
3	The received Signaling Multi-Frame alignment signal does not meet its pattern once Signaling Multi-Frame synchronization is achieved.	-	SMFERI (b1, E1-034H)	SMFERE (b1, E1-032H)
4	The received data stream is out of Basic Frame synchronization when any of the following conditions is met: 1) The Basic Frame has not been synchronized. 2) The received data stream meets the out of Basic Frame synchronization criteria set in the BIT2C (b6, E1-031H). 3) There are excessive CRC errors in the received data stream.	OOFV (b6, E1-036H)	OOFI (b6, E1-034H)	OOFE (b6, E1-032H)
5	The received data stream is out of CRC Multi-Frame synchronization when any of the following conditions is met: 1) The CRC Multi-Frame has not been synchronized. 2) There are excessive CRC errors in the received data stream.	OOCMFV (b4, E1-036H)	OOCMFI (b4, E1-034H)	OOCMFE (b4, E1-032H)
6	The received data stream is out of Signaling Multi-Frame synchronization when any of the following conditions is met: 1) The received data stream is out of Basic Frame synchronization. 1) The received data stream meets the out of Signaling Multi-Frame synchronization criteria set in the SMFASC (b5, E1-031H) and the TS16C (b4, E1-031H).	OOSMFV (b5, E1-036H)	OOSMFI (b5, E1-034H)	OOSMFE (b5, E1-032H)

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Table 2: Interrupt Sources in the E1 Frame Processor

No.	Sources	Status Bit	Interrupt Indication Bit	Interrupt Enable Bit
7	The out of Basic Frame synchronization condition has lasted for 100 ms. (e.g., the condition in Item No. 4 has lasted for 100 ms.)	RED (b3, E1-037H)	REDI (b3, E1-035H)	REDE (b3, E1-033H)
8	The calculated CRC remainder is not equal to the received C[1:4] bits.	-	CRCEI (b0, E1-035H)	CRCEE (b0, E1-033H)
9	It is out of Basic Frame synchronization and less than 3 zeros are detected in a 512-bit stream, or it is out of Basic Frame synchronization and less than 3 zeros are detected in each of 2 consecutive 512-bit stream. These two criteria are determined by the AISC (b1, E1-031H).	AISD (b5, E1-037H)	AISDI (b5, E1-035H)	AISDE (b5, E1-033H)
10	The condition in Item No. 9 has lasted for 100 ms.	AIS (b2, E1-037H)	AISI (b2, E1-035H)	AISE (b2, E1-033H)
11	Logic 1 is received in the A bit for a certain period. The criteria are defined in the RAIC (b3, E1-031H).	RAIV (b7, E1-037H)	RAII (b7, E1-035H)	RAIE (b7, E1-033H)
12	Logic 0 is received in any of the CRC error indication (E1 and E2) bits.	-	FEBEI (b1, E1-035H)	FEBEE (b1, E1-033H)
13	A logic 1 is received in the A bit and a logic 0 is received in any of the E1 and E2 bits for 10 ms.	RAICCRCV (b2, E1-036H)	RAICCRCI (b6, E1-03FH)	RAICCRCE (b6, E1-03EH)
14	A logic 0 is received in any of the E1 and E2 bits on ≥ 990 occasions per second for the latest 5 consecutive seconds.	CFEBEV (b1, E1-036H)	CFEBEI (b5, E1-03FH)	CFEBEE (b5, E1-03EH)
15	Logic 1 is received in the Y bit for 3 consecutive Signaling Multi-Frames.	RMAIV (b6, E1-037H)	RMAII (b6, E1-035H)	RMAIE (b6, E1-033H)
16	The device is operating in the CRC to non-CRC inter working mode.	C2NCIWV (b7, E1-036H)	C2NCIWI (b7, E1-034H)	C2NCIWE (b7, E1-032H)
17	The position of the Basic Frame alignment pattern is changed.	-	COFAI (b3, E1-034H)	COFAE (b3, E1-032H)
18	The device is in the procedure of the offline Basic Frame searching.	OOOFV (b3, E1-036H)	OOOFI (b7, E1-03FH)	OOOFE (b7, E1-03EH)
19	The first bit of each Basic Frame is received.	-	IFPI (b3, E1-03FH)	IFPE (b3, E1-03EH)
20	The first bit of each CRC Sub Multi-Frame is received.	-	ICSMFPI (b2, E1-03FH)	ICSMFPE (b2, E1-03EH)
21	The first bit of each CRC Multi-Frame is received.	-	ICMFPI (b1, E1-03FH)	ICMFPE (b1, E1-03EH)
22	The first bit of each Signaling Multi-Frame is received.	-	ISMFPI (b0, E1-03FH)	ISMFPE (b0, E1-03EH)
23	2 out of 3 Sa7 bits are received as logic 0.	V52LINKV (b0, E1-036H)	V52LINKI (b4, E1-03FH)	V52LINKE (b4, E1-03EH)
24	There is change in the corresponding SaX[1:4] (b3~0, E1-03DH).	-	Sa4I, Sa5I, Sa6I, Sa7I, Sa8I (b4~0, E1-03CH)	Sa4E, Sa5E, Sa6E, Sa7E, Sa8E (b4~0, E1-03BH)

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3.2.2 T1/J1 MODE

In T1/J1 Mode, the Frame Processor searches for the frame alignment patterns in standard Super-Frame (SF) or in Extended Super-Frame (ESF) framing formats. The format is chosen by the ESF (b4, T1/J1-020H). The searching algorithm of T1 or J1 is determined by the JYEL (b3, T1/J1-020H). The Frame Processor acquires frame alignment per ITU-T requirement.

When frame alignment is achieved, the Framer Processor continues to monitor the received data stream. The Frame Processor declares the framing bit errors and bit error events, if any. The Frame Processor can also detect out-of-frame events based on selectable criteria.

The Frame Processor can also be disabled to receive unframed data.

3.2.2.1 Synchronization Searching

All the frame synchronization function can only be executed when the UNF (b6, T1/J1-000H) is logic 0.

3.2.2.1.1 Super Frame (SF) Format

The structure of T1/J1 SF format is illustrated in Table 3. The SF is made up of 12 frames. Each frame consists of a one-bit overhead - F Bit and 24 8-bit channels. If two consecutive valid Frame Alignment Patterns - '100011011100' for T1 or '10001101110X' for J1 - are received in the F-Bit in the received data stream, the SF synchronization is acquired. The same pattern is a mimic pattern if it is received in the data stream other than F-bit. If a mimic pattern exists during the frame searching procedure, the synchronization will not be declared and the MFP (b1, T1/J1-022H) will be set to indicate the presence of a mimic pattern.

Table 3: SF Format

Frame No. in SF	F-Bit (Frame Alignment)	the Bit in Each Channel	
		Data Bit	Signaling Bit
1	1	1 - 8	-
2	0	1 - 8	-
3	0	1 - 8	-
4	0	1 - 8	-
5	1	1 - 8	-
6	1	1 - 7	A (bit 8)
7	0	1 - 8	-
8	1	1 - 8	-
9	1	1 - 8	-
10	1	1 - 8	-
11	0	1 - 8	-
12	X*	1 - 7	B (bit 8)

Note:
* 'X' should be logic 0 in T1 FAS.
'X' can be logic 0 or 1 in J1 FAS because this position is used as Yellow Alarm Indication bit.

3.2.2.1.2 Extended Super Frame (ESF) Format

The structure of T1/J1 ESF format is illustrated in Table 4. The ESF is made up of 24 frames. Each frame consists of a one-bit overhead - F Bit and 24 8-bit channels.

The pattern of the Frame Alignment Pattern is '001011', which is located from Frame 4 in every 4th F-bit position.

When the ESFFA (b5, T1/J1-020H) is set to '0', the ESF synchronization is acquired if four consecutive Frame Alignment Patterns are detected in the F-Bit in the received data stream. The same pattern is a mimic pattern if it is received in the data stream other than F-bit. If a mimic pattern exists during the frame searching procedure, the synchronization will not be declared and the MFP (b1, T1/J1-022H) will be set to indicate the presence of a mimic pattern.

When the ESFFA (b5, T1/J1-020H) is set to '1', the synchronization will be declared when 6 consecutive Frame Alignment Patterns are received error free and the CRC-6 checksum is also error free. In this condition, the existence of mimic patterns will not be considered.

Table 4: ESF Format

Frame No. in ESF	F-Bit Assignment			the Bit in Each Channel	
	FAS	DL	CRC	Data Bit	Signaling Bit
1	-	DL	-	1 - 8	-
2	-	-	C1	1 - 8	-
3	-	DL	-	1 - 8	-
4	0	-	-	1 - 8	-
5	-	DL	-	1 - 8	-
6	-	-	C2	1 - 7	A (bit 8)
7	-	DL	-	1 - 8	-
8	0	-	-	1 - 8	-
9	-	DL	-	1 - 8	-
10	-	-	C3	1 - 8	-
11	-	DL	-	1 - 8	-
12	1	-	-	1 - 7	B (bit 8)
13	-	DL	-	1 - 8	-
14	-	-	C4	1 - 8	-
15	-	DL	-	1 - 8	-
16	0	-	-	1 - 8	-
17	-	DL	-	1 - 8	-
18	-	-	C5	1 - 7	C (bit 8)
19	-	DL	-	1 - 8	-
20	1	-	-	1 - 8	-
21	-	DL	-	1 - 8	-
22	-	-	C6	1 - 8	-
23	-	DL	-	1 - 8	-
24	1	-	-	1 - 7	D (bit 8)

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3.2.2.2 Out Of Synchronization Detection & Interrupt

A 4-frame capacity buffer is used to store the data when the Frame Processor is searching for SF/ESF synchronization. Once the SF/ESF is synchronized, the buffer is relinquished by the Frame Processor and the Frame Processor continues to monitor the errors. When the FAS error ratio exceeds the criteria configured in the M2O[1:0] (b7~6, T1/J1-020H), it is out of frame.

The interrupt sources in this block are summarized in Table - 5. When there are conditions meeting the interrupt sources, the corresponding Status bit will be asserted high. When there is a transition ('1' to '0' or '0' to '1') on the Status bit, the corresponding Status Interrupt Indication bit will be set to logic 1 (If the Status bit does not exist, the source will cause its Status Interrupt Indication bit to be logic 1 directly) and the Status Interrupt Indication bit will be cleared when it is read. A logic 1 in the Status Interrupt Indication bit indicates an interrupt occurred. The interrupt is reported by the $\overline{INT}$ pin if its Status Interrupt Enable bit was set to logic 1.

Table 5: Interrupt Sources in the T1/J1 Frame Processor

No.	Sources	Status Bit	Interrupt Indication Bit	Interrupt Enable Bit
1	The frame alignment mimic pattern is detected in the received data stream.	MFP (b1, T1/J1-022H)	MFPI (b3, T1/J1-022H)	MFPE (b1, T1/J1-021H)
2	The SF / ESF synchronization is acquired.	INFR (b0, T1/J1-022H)	INFRI (b2, T1/J1-022H)	INFRE (b0, T1/J1-021H)
3	The position of the new frame alignment pattern differs from the position of the previous one.	-	COFAI (b7, T1/J1-022H)	COFAE (b5, T1/J1-021H)
4	One bit error is detected in frame alignment pattern.	-	FERI (b6, T1/J1-022H)	FERE (b4, T1/J1-021H)
5	Two or more bit errors are detected in one frame alignment pattern.	-	SFEI (b4, T1/J1-022H)	SFEE (b2, T1/J1-021H)
6	In the SF format, one bit error is detected in frame alignment pattern. In the ESF format, the received CRC-6 is not equal to the local calculated CRC-6.	-	BEEI (b5, T1/J1-022H)	BEEE (b3, T1/J1-021H)

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3.3 PERFORMANCE MONITOR (PMON)

The Performance Monitor is used to count various performance events in the received data stream within defined intervals. The Performance Monitor of each framer operates independently.

3.3.1 E1 MODE

The PMON block counts the Basic Frame alignment pattern errors. The method of counting the errors is defined by the WORDERR (b5, E1-000H) and CNTNFAS (b4, E1-000H) as shown in Table 6. The number of the Basic Frame alignment pattern errors counted during the interval is reflected in the FER[6:0] (b6~0, E1-069H).

Table 6: Basic Frame Alignment Pattern Error Counter

WORDERR (b5, E1-000H)	CNTNFAS (b4, E1-000H)	One Error is Counted
0	0	One bit error in FAS
0	1	One bit error in FAS or a logic 0 in bit 2 of TS0 of NFAS
1	0	One or more than one bit error in a FAS
1	1	Any bit error in a FAS and the 2nd bit of TS0 of the following NFAS

The PMON block counts the Far End Block Error (FEBE) which is detected in the E1 and E2 bits. The number of the FEBE counted during the interval is stored in the FEBE[9:0] (b1~0, E1-06BH & b7~0, E1-06AH).

The block also counts the CRC errors which mean the local calculated CRC remainders are not equal to the received CRC. The number of the CRC errors counted during the interval is indicated in the CRCE[9:0] (b1~0, E1-06DH & b7~0, E1-06CH).

The above three kinds of PMON Error Count registers are deactivated when the framer is out of Basic Framer synchronization. The latter two kinds of PMON Error Count registers are also deactivated when it is out of CRC Multi-Frame synchronization.

These PMON Error Count registers in a framer can be updated as a group. The intervals are typically 1 second when the AUTOUPDATE (b0, E1-000H) of the current framer is set. They can also be updated by writing to any of these PMON Error Count registers. The PMON Error Count registers in eight framers can also be updated together by writing to the Revision / Chip ID / Global PMON Update register (E1-009H). Once the PMON Error Count registers are updated, the XFER (b1, E1-068H) will be set to logic 1 and an interrupt can be asserted on the $\overline{INT}$ pin if the INTE (b2, E1-068H) is logic 1.

If the performance number counted in the next interval is latched in its PMON Error Count register without the previous one being read, the PMON Error Count register is over-written. Any over-writing of the three kinds of PMON Error Count registers will be indicated in the OVR (b0, E1-068H).

3.3.2 T1/J1 MODE

In the SF format, the Performance Monitor counts three kinds of events:

1. Every one-bit error in a frame alignment pattern is counted. The number of the errors counted during the interval is reflected in the FER[8:0] (b0, T1/J1-04DH & b7~0, T1/J1-04CH) (In SF format, the usage of the BEE[11:0] (b3~0, T1/J1-04BH & b7~0, T1/J1-04AH) is the same as that of the FER[8:0]);

2. The out of SF synchronization event is counted. The number counted during the interval is reflected in the OOF[4:0] (b4~0, T1/J1-04EH);

3. The number of changes of the frame alignment position during the interval is counted and is reflected in the COFA[2:0] (b2~0, T1/J1-04FH).

In the ESF format, the Performance Monitor counts four kinds of events:

1. The block counts the CRC-6 errors which mean the local calculated CRC-6 remainders are not equal to the received CRC-6. The number of the errors counted during the interval is indicated in the BEE[11:0] (b3~0, T1/J1-04BH & b7~0, T1/J1-04AH);

2 ~ 4. (The same events as 1 ~ 3 in the SF format, described above.)

These PMON Error Count registers in a framer can be updated as a group. The intervals are typically 1 second when the AUTOUPDATE (b0, T1/J1-000H) of the framer is set. They can also be updated by writing to any of these PMON Error Count registers. The PMON Error Count registers of eight framers can also be updated together by writing to the Revision / Chip ID / Global PMON Update register (T1/J1-00CH). Once the PMON Error Count registers are updated, the XFER (b1, T1/J1-049H) will be logic 1 and an interrupt can be asserted on the $\overline{INT}$ pin if the INTE (b2, T1/J1-049H) is logic 1.

If the performance number counted in the next interval is latched in its PMON register without the previous one being read, the PMON Error Count register is over-written. Any over-writing of the four kinds of PMON Error Count registers will be indicated in the OVR (b0, T1/J1-049H).

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3.4 ALARM DETECTOR (ALMD) - T1/J1 ONLY

The Alarm Detector block exists in T1/J1 mode only. It detects the Yellow signal and the AIS (Blue Alarm) signal in SF/ESF in T1/J1 data stream and declares the Yellow alarm, the Red alarm and the AIS alarm. The T1 or J1 mode is selected by the J1_YEL (b5, T1/J1-02CH) while the SF or ESF format is selected by the ESF (b4, T1/J1-02CH).

The Yellow signal is declared differently in each format:

- In T1 SF format: The Yellow signal occupies the 2nd bit of each channel. When the occurrence of logic 1 in this bit position is less than 16 times (including 16 times) during a 40 ms period, the Yellow signal is declared.

- In J1 SF format: The Yellow signal occupies the F-bit of the 12th frame. When the occurrence of logic 0 on this bit position is less than 2 times (including 2 times) during a 40 ms period, the Yellow signal is declared.

- In T1/J1 ESF format: The Yellow signal occupies the DL of the F-bit (refer to Table 4). The pattern is 'FF00' in T1 mode and 'FFFF' in J1 mode. When the AVC (b1, T1/J1-02AH) is logic 0, the Yellow signal is declared if 8 out of 10 successive patterns match the 'FF00' (in T1) or 'FFFF' (in J1) on the DL bit position. When the AVC (b1, T1/J1-02AH) is logic 1, the Yellow signal is declared if 4 out of 5 successive patterns match the 'FF00' (in T1) or 'FFFF' (in J1) on the DL bit position.

Any of the above conditions will be indicated by the YELD (b1, T1/J1-02FH).

The AIS signal is declared when the received data is out of SF/ESF synchronization for 60 ms and the received logic 0 is less than 127 times in the same period. Then the AIS signal will be indicated by the AISD (b0, T1/J1-02FH).

The Red signal is declared when one or more out of SF/ESF sync event occurs in 40 ms. Then the Red signal will be indicated by the REDD (b2, T1/J1-02FH).

The Yellow alarm, AIS alarm and Red alarm will be declared or cleared when the corresponding alarm signal is present or absent for a certain period as summarized in Table 7.

The Yellow alarm, AIS alarm and Red alarm are also the interrupt sources in the ALMD block. When the alarm occurs, the corresponding Interrupt Status Register (YEL, AIS or RED in b2, b0, b1 of T1/J1-02EH respectively) will indicate the alarm. When there is any transition (from '0' to '1' or from '1' to '0') on the Interrupt Status Register, its corresponding Interrupt Indication Register (YELI, AISI or REDI in b5, b3, b4 of T1/J1-02EH respectively) will be logic 1. A transition on the Interrupt Indication Register can cause an interrupt on the $\overline{INT}$ pin if the corresponding Interrupt Enabled Register (YELE, AISE or REDE in b2, b0, b1 of T1/J1-02DH respectively) is logic 1.

Table 7: Alarm Summary in ALMD

	Declaring	Clearing
Yellow Alarm	the Yellow signal is present for 425 ms (± 50 ms)	the Yellow signal is absent for 425 ms (± 50 ms)
AIS Alarm	the AIS signal is present for 1.5 sec (± 100 ms)	the AIS signal is absent for 16.8 sec (± 500 ms); or the AIS signal is absent for 180 ms if the FASTD (b4, T1/J1-02DH) is set
Red Alarm	the Red signal is present for 2.55 sec (± 40 ms)	the Red signal is absent for 16.6 sec (± 500 ms); or the Red signal is absent for 120 ms if the FASTD (b4, T1/J1-02DH) is set

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3.5 HDLC RECEIVER (RHDLC)

The HDLC extraction is performed in this block. The HDLC Receiver #1, #2 and #3 in E1 mode or the HDLC Receiver #1 and #2 in T1/J1 ESF mode of each framer operate independently.

3.5.1 E1 MODE

Three HDLC Receiver blocks (#1, #2 and #3) are employed for each framer to extract the HDLC link from the received data stream. Before the HDLC link is selected, the TXCISEL (b3, E1-00AH) should be set to '0'. Thus, the configuration of the Link Control and Bits Select registers (addressed from 028H to 02DH) is for RHDLC. Next, select one of the three HDLC Receiver blocks by setting the appropriate bits in the RHDLCSEL[1:0] (b7~6, E1-00AH). The #2 and #3 blocks can also be disabled by setting the V52DIS (b3, E1-007H). Then the position of the HDLC link is defined as follows:

1. Set the DL_EVEN (b7, E1-028H or b7, E1-02AH or b7, E1-02CH) and/or the DL_ODD (b6, E1-028H or b6, E1-02AH or b6, E1-02CH) to choose the even and/or odd frames (the even frames are FAS frames while the odd frames are NFAS frames);
2. Set the DL_TS[4:0] (b4~0, E1-028H or b4~0, E1-02AH or b4~0, E1-02CH) to define the time slot of the assigned frame (or to set the TS16_EN (b5, E1-028H) to choose the TS16 of the assigned frame);
3. Set the DL_BIT[7:0] (b7~0, E1-029H or b7~0, E1-02BH or b7~0, E1-02DH) to select the bits of the assigned time slot.

Three HDLC standards for E1 are defined and one is selected as follows:

1. Common Channel Signaling (CCS) data link (extract the bits in the TS16);
2. V5.1 / V5.2 D-channel and C-channels (extract the bits in any time slot except TS16);
3. Sa-bit data link.

All the functions of the selected HDLC Receiver block is enabled only if the EN (b0, E1-048H) is set to logic 1.

A normal HDLC packet consists of the following parts as shown in Figure 5:

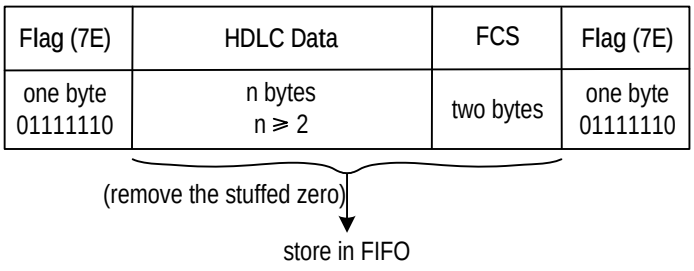


Figure 5. HDLC Packet

Every HDLC packet starts with a 7E (Hex) opening flag sequence and ends with the same flag. Before the closing flag sequence, two bytes of CRC-CCITT frame check sequences (FCS) are provided to check all the HDLC data. The received FCS will be compared with the local calculated FCS.

A FIFO buffer is used to store the HDLC packet, that is, to store the data whose stuffed zeros have been removed and the FCS. However, when the address matching is enabled, the first and/or second byte compares with the address setting in the PA[7:0] (b7~0, E1-04CH) and the SA[7:0] (b7~0, E1-04DH), and only the data matching the address mode set in the MEN (b3, E1-048H) and the MM (b2, E1-048H) is stored into the FIFO. When address matching is disabled, all the HDLC data are stored. The first 7E opening flag which activates the HDLC link and the 7F (Hex) abort sequence which deactivates the HDLC link will also be converted to dummy bytes and stored into the FIFO regardless of the address being matched or not. These two types of flags will also assert the COLS (b5, E1-04AH) to indicate the HDLC link status change. The content in the FIFO is read in the RD[7:0] (b7~0, E1-04BH), and the status of the bytes will be reflected in the PBS[2:0] (b3~1, E1-04AH). Both of these registers (RD[7:0] (b7~0, E1-04BH) and PBS[2:0] (b3~1, E1-04AH)) can not be accessed at a rate greater than 1/15 of the XCK rate.

The depth of the FIFO is 128 bytes. When the FIFO is empty, the FE (b7, E1-04AH) will be set. If data is still written into the FIFO when the FIFO is already full, the FIFO will be over-written. The over-written condition will be indicated by the OVR (b6, E1-04AH) and forces the FIFO to be cleared.

A logic 1 in the PKIN (b4, E1-04AH) indicates a non-abort HDLC packet was received. The PKIN (b4, E1-04AH) is set regardless of the status of the FCS condition or there being an integer or non-integer number of bytes stored in the FIFO.

The HDLC packet will be forced to terminate for four reasons:

1. The 7F abort sequence is received;
2. More than 15 successive logic ones are received in the data stream;
3. Set the TR (b1, E1-048H) to logic 1;
4. Set the EN (b0, E1-048H) from logic 1 to logic 0 and back to logic 1.

All the above methods will deactivate the HDLC link immediately and the latter two means will also clean the FIFO and interrupts. A new search for the 7E opening flag is also initiated.

The interrupt sources in this block are:

1. Receiving the first 7E opening flag sequence which terminates all ones data and activates the HDLC link;
2. Receiving the 7E closing flag sequence;
3. Receiving the abort sequence;
4. Exceeding the set point of the FIFO which is defined in the INTC[6:0] (b6~0, E1-049);
5. Over-writing the FIFO.

Any one of the interrupt sources will assert the INTR (b0, E1-04AH) high. Then the $\overline{INT}$ pin will be low to report the interrupt if the INTE (b7, E1-049H) is logic 1.

3.5.2 T1/J1 MODE

In the SF format, there is no HDLC link.

In the ESF format, two HDLC Receiver blocks (#1 and #2) are employed for each framer to extract the HDLC link. Before the HDLC link is selected, the TXCISEL (b3, T1/J1-00DH) should be set to '0'. Thus, the configuration of the Link Control and Bits Select registers (addressed from 070H to 071H) is for the RHDLC. Then, selected by the

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RHDLCSEL[1:0] (b7~6, T1/J1-00DH), one of the two HDLC Receiver blocks is accessible to the microprocessor. The HDLC#1 extracts the HDLC link in the DL of the F-bit (its position is shown in Table 4). The HDLC#2 extracts the HDLC link from one of the channels which position is defined as follows:

1. Set the DL2_EVEN (b7, T1/J1-070H) and/or the DL2_ODD (b6, T1/J1-070H) to choose the even and/or odd frames;

2. Set the DL2_TS[4:0] (b4~0, T1/J1-070H) to define the channel of the assigned frame;

3. Set the DL2_BIT[7:0] (b7~0, T1/J1-071H) to select the bits of the assigned channel.

All the functions of the selected HDLC Receiver block will be enabled only if the EN (b0, T1/J1-054H) is set to logic 1.

The structure of the HDLC packet is the same as it is described in the E1 mode (refer to Figure 5).

A FIFO buffer is used to store the HDLC packet, that is, to store the data whose stuffed zeros have been removed and the FCS. However, when the address matching is enabled, the first and/or second byte compares with the address setting in the PA[7:0] (b7~0, T1/J1-058H) and the SA[7:0] (b7~0, T1/J1-059H) and only the data matching the address mode set in the MEN (b3, T1/J1-054H) and the MM (b2, T1/J1-054H) is stored into the FIFO. When the address matching is disabled, the entire HDLC packet is stored. The first 7E opening flag which activates the HDLC link and the 7F abort sequence which deactivates the HDLC link will also be converted into dummy bytes and stored in the FIFO. These two types of flags will also assert the COLS (b5, T1/J1-056H) to indicate the HDLC link status change. The content in the FIFO is read in the RD[7:0] (b7~0, T1/J1-057H), and the status of the bytes will be reflected in the PBS[2:0] (b3~1, T1/J1-056H). Both of the two registers can not be accessed at a rate greater than 1/15 of the XCK rate.

The depth of the FIFO is 128 bytes. When the FIFO is empty, the FE (b7, T1/J1-056H) will be set. If data is still written into the FIFO when the FIFO is already full, the FIFO will be over-written. The over-written condition will be indicated by the OVR (b6, T1/J1-056H) and force the FIFO to be cleared.

A logic 1 in the PKIN (b4, T1/J1-056H) indicates a non-abort HDLC packet was received whether there were FCS errors or non-integer number of bytes errors in it or not.

The HDLC packet can be forced to terminate by four means:

1. The 7F abort sequence is received;

2. More than 15 successive logic ones are received in the data stream;

3. Set the TR (b2, T1/J1-054H) to logic 1;

4. Set the EN (b1, T1/J1-054H) from logic 1 to logic 0 and back to logic 1.

All the above methods will deactivate the HDLC link immediately and the latter two methods will also clear the FIFO and interrupts. A new search for the 7E opening flag is also initiated.

The interrupt sources in this block are:

1. Receiving the first 7E opening flag sequence which terminates the all ones data and activates the HDLC link;

2. Receiving the 7E closing flag sequence;

3. Receiving the abort sequence;

4. Exceeding the set point of the FIFO which is defined in the INTC[6:0] (b6~0, T1/J1-055H);

5. Over-writing the FIFO.

Any one of the interrupt sources will assert the INTR (b0, T1/J1-056H) high. Then the $\overline{INT}$ pin will be driven low to report the interrupt if the INTE (b7, T1/J1-055H) is logic 1.

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3.6 BIT-ORIENTED MESSAGE RECEIVER (RBOM) - T1/J1 ONLY

The Bit Oriented Message (BOM) can only be received in the ESF format in T1/J1 mode. The standard of BOM is defined in ANSI T1.403 and in TR-TSY-000194. This block of each framer operates independently.

The BOM pattern is '111111110XXXXXX0' which occupies the DL of the F-bit in the ESF format (refer to Table 4). The six 'X's represent the message. The BOM is declared only when the pattern is matched and the received message is identical 4 out of 5 times or 8 out of 10 times. The identification time is determined by the AVC (b1, T1/J1-02AH). After the BOM is declared, the BOM is loaded into the BOC[5:0] (b5~0, T1/J1-02BH). However, the BOM does not include all ones code in both T1 and J1 mode.

When the BOM is converted into non-BOM, the received data will be idle code. The pattern of the idle code is 'FFFF' in T1 mode and 'FF7E' in J1 mode. When the received data is 4 out of 5 times or 8 out of 10 times identical with the pattern, the idle code is declared. The identification time is determined by the AVC (b1, T1/J1-02AH).

There are two interrupt sources in this block. When the BOM is declared, the BOCI (b6, T1/J1-02BH) will be set. When the idle code is declared, the IDLEI (b7, T1/J1-02BH) will be set. If the BOCE (b0, T1/J1-02AH) and IDLE (b2, T1/J1-02AH) are set to '1' respectively, the corresponding condition will cause an interrupt on the $\overline{\text{INT}}$ pin.

3.7 INBAND LOOPBACK CODE DETECTOR (IBCD) - T1/J1 ONLY

The Inband Loopback Code Detector can track loopback activate/deactivate codes only in framed or unframed T1/J1 data stream. The Inband Loopback Code Detector of each framer operates independently.

The received data stream is compared with the target activate/deactivate code whose length and the content are programmed in the ASEL[1:0] (b1~0, T1/J1-03CH) / DSEL[1:0] (b3~2, T1/J1-03CH) and the ACT[7:0] (b7~0, T1/J1-03EH) / DACT[7:0] (b7~0, T1/J1-03FH) respectively. In framed mode, the F-bit can be chosen by the IBCD_IDLE (b5, T1/J1-000H) to compare with the target activate/deactivate code or not. In unframed mode, all 193 bits are compared with the target activate/deactivate code. If the received data stream matches the target activate or deactivate code and repeats for a 39.8 ms period, the LBACP (b7, T1/J1-03DH) or LBDCP (b6, T1/J1-03DH) will indicate the appearance of the corresponding code. 2, 20 or 200 bit-error tolerance within each 39.8 ms period is permitted by setting the IBCD_ERR[1:0] (b5~4, T1/J1-03CH). However, even if the F-bit is compared, whether it is matched or not, the result will not cause bit errors, that is, the comparison result of the F-bit is passed over.

When the received data stream matches the target activate/deactivate code and repeats for 5.1 sec, the LBA (b1, T1/J1-03DH) / LBD (b0, T1/J1-03DH) will indicate the detection of the inband loopback code. The code sequences detection and timing is compatible with the specifications in T1.403, TA-TSY-000312 and TR-TSY-000303.

The status changes of the activate or deactivate code are the interrupt sources in the IBCD block. That is, when the value in the Status Register (LBA [b1, T1/J1-03DH] or LBD [b0, T1/J1-03DH]) changes, its corresponding Interrupt Indication Register (LBAI [b3, T1/J1-03DH] or LBDI [b2, T1/J1-03DH]) will be logic 1. A logic 1 on the Interrupt Indication Register will cause an interrupt on the $\overline{\text{INT}}$ pin if the corresponding Interrupt Enable Register (LBAE [b5, T1/J1-03DH] or LBDE [b4, T1/J1-03DH]) is logic 1.

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3.8 ELASTIC STORE BUFFER (ELSB)

The Elastic Store Buffer of each framer operates independently.

3.8.1 E1 MODE

In Receive Clock Slave mode, a 2-basic-frame depth Elastic Store Buffer is used to synchronize the incoming frames to the Receive Side System Common Clock derived from the RSCCK pin, and to the Receive Side System Common Frame Pulse derived from the RSCFS pin. A write pointer is used to write the data to the Elastic Store Buffer, while a read pointer is used to read the data from the Elastic Store Buffer.

When the average frequency of the incoming data is greater than that of the Receive Side System Common Clock (RSCCK), the write pointer will be faster than the read pointer and the Elastic Store Buffer will be filled. So a frame will be deleted after its prior frame is read. When the read pointer crosses the frame boundary, a controlled slip will occur with a logic 1 indicated in the SLIPD (b1, E1-059H).

When the average frequency of the incoming data is less than that of RSCCK, the write pointer will be slower than the read pointer and the Elastic Store Buffer will be empty. The frame will be repeated after it is read. When the read pointer crosses the next frame boundary, a controlled slip will occur with a logic 0 indicated in the SLIPD (b1, E1-059H).

When the slip occurs, the SLIPI (b0, E1-059H) will indicate. An interrupt on the $\overline{INT}$ pin will also occur if the SLIPE (b2, E1-059H) is set to logic 1.

In Receive Clock Slave mode, if it is out of Basic Frame synchronization, the idle code programmed in the D[7:0] (b7~0, E1-05AH) in the Elastic Store Buffer can be set to replace the data if the TRKEN (b1, E1-001H) is set to logic 1.

In Receive Clock Master mode, the Elastic Store Buffer is bypassed unless the device is in the Payload Loopback diagnosis mode. (Refer to Chapter 3.23.3 Payload Loopback for details).

3.8.2 T1/J1 MODE

In Receive Clock Slave mode, a 2-basic-frame depth Elastic Store Buffer is used to synchronize the incoming frames to the Receive Side System Common Clock derived from the RSCCK pin, and to the Receive Side System Common Frame Pulse derived from the RSCFS pin. A write pointer is used to write the data to the Elastic Store Buffer, while a read pointer is used to read the data from the Elastic Store Buffer.

When the average frequency of the incoming data is greater than that of the Receive Side System Common Clock (RSCCK), the write pointer will be faster than the read pointer and the Elastic Store Buffer will be filled. So a frame will be deleted after its prior frame is read. When the read pointer crosses the frame boundary, a controlled slip will occur with a logic 1 indicated in the SLIPD (b1, T1/J1-01DH).

When the average frequency of the incoming data is less than that of RSCCK, the write pointer will be slower than the read pointer and the Elastic Store Buffer will be empty. The frame will be repeated after it is read. When the read pointer crosses the next frame boundary, a controlled slip will occur with a logic 0 indicated in the SLIPD (b1, T1/J1-01DH).

When the slip occurs, the SLIPI (b0, T1/J1-01DH) will indicate. An interrupt on the $\overline{INT}$ pin will also occur if the SLIPE (b2, T1/J1-01DH) is logic 1.

In Receive Clock Slave mode, if it is out of SF/ESF synchronization, the idle code programmed in the D[7:0] (b7~0, T1/J1-01EH) in the Elastic Store Buffer will replace the data of all channels automatically.

In Receive Clock Master mode, the Elastic Store Buffer is bypassed unless the device is in the payload loopback diagnosis mode. (Refer to Chapter 3.23.3 Payload Loopback for details).

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3.9 RECEIVE CAS/RBS BUFFER (RCRB)

The Receive CAS/RBS Buffer of each framer operates independently.

3.9.1 E1 MODE

In the Signaling Multi-Frame synchronization condition, the signaling bits are located in TS16, which is Channel Associated Signaling (CAS). Their arrangement in TS16 is shown in Figure 6.

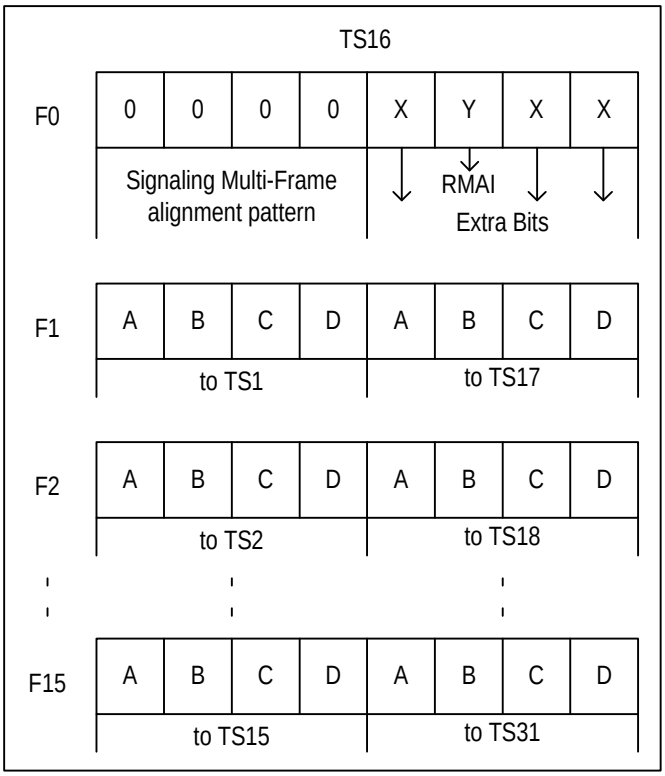


Figure 6. TS16 Arrangement in Signaling Multi-Frame

When the RSCKn/RSSIGn/MRSSIG[1:2] pins are used as the signaling output, i.e. in Receive Clock Slave External Signaling mode or in Receive Multiplex mode, the signaling codeword (ABCD) is clocked out in the lower nibble of the time slot with its corresponding data serializing on the RSDn/MRSD[1:2] pins (as shown in the Figure 7).

When the COSS (b6, E1-064H) is logic 1, all the COSS[30:1] (b5~0, E1-064H and b7~0, E1-065H and b7~0, E1-066H and b7~0, E1-067H) in the Receive CAS/RBS Buffer registers will reflect the change of the signaling of each time slot respectively (excluding the TS0 and TS16).

When the COSS (b6, E1-064H) is logic 0, the Receive CAS/RBS Buffer indirect registers (from 01H to 5FH of RCRB indirect registers) can be accessed by the microprocessor. The address of the indirect register is specified by the A[6:0] (b6~0, E1-066H). Whether the data is read from or written into the specified indirect register is determined by the R/WB (b7, E1-066H) and the data is in the D[7:0] (b7~0, E1-067H). The indirect registers have a read/write cycle. Before the read/write operation is completed, the BUSY (b7, E1-065H) will be set. New operations on the indirect registers can only be implemented when the BUSY (b7, E1-065H) is cleared. The read/write cycle is 490 ns.

The indirect registers are divided into three segments: two segments (from 01H to 1FH & from 21H to 3FH) contain the signaling bits of each time slot; another segment (from 40H to 5FH) contains the signaling debounce configuration of each time slot.

A three-Signaling-Multi-Frame capacity buffer is used for signaling debounce and signaling freezing.

Signaling debounce will be performed by setting the DEB (b0, E1-RCRB-indirect registers - 41~5FH). The DEB (b0, E1-RCRB-indirect registers - 41~5FH) is activated when the PCCE (b0, E1-064H) is set. The signaling bits are updated only when 2 consecutive signalings of a time slot are the same.

Signaling freeze will remain the signaling automatically when it is out of Signaling Multi-Frame synchronization or in unframed mode.

The signaling bits are extracted to the A, B, C, D (b3~0, E1-RCRB-indirect registers - 01~1FH or b3~0, E1-RCRB-indirect registers - 21~3FH).

There is a maximum 2 ms delay between the transition of the COSS[n] (E1-064H and E1-065H and E1-066H and E1-067H) and the updating of the A, B, C, D code in the corresponding indirect registers (b3~0, E1-RCRB-indirect registers - 21~3FH). To avoid this 2 ms delay, users can read the corresponding b3~0 in the E1-RCRB-indirect registers - (01~1FH) first. If the value of these four bits are different from the previous A, B, C, D code, then the content of b3~0 in the E1-RCRB-indirect registers - (01~1FH) is the updated A, B, C, D code. If the content of the four bits is the same as the previous A, B, C, D code, then users should read the b3~0 in the E1-RCRB-indirect registers - (21~3FH) to get the updated A, B, C, D code.

Any one of the 30-timeslot's signaling change will cause an interrupt on the $\overline{INT}$ pin if the SIGE (b5, E1-064H) is set.

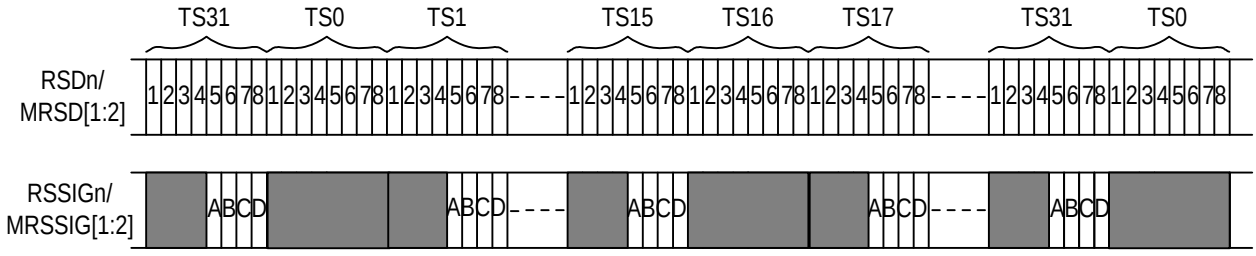


Figure 7. Signaling Output in E1 Mode

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3.9.2 T1/J1 MODE

When the frame is synchronized, the signaling is located in the Bit 8 of Frame 6 (A bit) and Frame 12 (B bit) in SF format, and is located in the Bit 8 of Frame 6 (A bit), Frame 12 (B bit), Frame 18 (C bit) and Frame 24 (D bit) in ESF format (refer to Table 3 & Table 4). The SF/ESF signaling format is chosen by the ESF (b2, T1/J1-040H).

When the RSCKn/RSSIGn/MRSSIG[1:2] pins are used as the signaling output, i.e. in Receive Clock Slave External Signaling mode or in Receive Multiplex mode, the signaling codeword (AB or ABCD) is clocked out in the lower nibble of the channel with its corresponding data serializing on the RSDn/MRSD[1:2] pins (as shown in the Figure - 6). However, in SF format, the signaling C and D are the repetition of signaling A and B.

When the COSS (b6, T1/J1-040H) bit is logic 1, all the COSS[24:1] (b7~0, T1/J1-041H and b7~0, T1/J1-042H and b7~0, T1/J1-043H) in the Receive CAS/RBS Buffer registers will reflect the change of the signaling of each channel respectively.

When the COSS (b6, T1/J1-040H) bit is logic 0, the Receive CAS/RBS Buffer indirect registers (from 01H to 58H of RCRB indirect registers) can be accessed by the microprocessor. The address of the indirect register is specified by the A[6:0] (b6~0, T1/J1-042H). Whether the data is read from or written into the specified indirect register is determined by the R/WB (b7, T1/J1-042H) and the data is in the D[7:0] (b7~0, T1/J1-043H). The indirect registers have a read/write cycle. Before the read/write operation is completed, the BUSY (b7, T1/J1-041H) will be set. New operations on the indirect registers can only be done when the BUSY (b7, T1/J1-041H) is cleared. The read/write cycle is 650 ns.

The indirect registers are divided into three segments: two segments (from 01H to 18H & from 21H to 38H) contain the signaling bits of each channel; another segment (from 41H to 58H) contains the signaling debounce configuration of each channel.

A three-superframe capacity buffer is used for signaling debounce and signaling freezing.

Signaling debounce will be performed by setting the DEB (b0, T1/J1-RCRB-indirect registers - 41~58H). The DEB (b0, T1/J1-RCRB-indirect registers - 41~58H) is activated when the PCCE (b0, T1/J1-040H) is set. The signaling bits are updated only when 2 consecutive SF/ESF signaling bits of a channel are the same.

Signaling freeze will remain the signaling automatically when it is out of SF/ESF sync or in unframed mode.

The signaling bits are extracted to the A, B, C, D (b3~0, T1/J1-RCRB-indirect registers - 01~18H or b3~0, T1/J1-RCRB-indirect registers - 21~38H).

There is a maximum 2 ms delay between the transition of the COSS[n] (T1/J1-041H and T1/J1-042H and T1/J1-043H) and the updating of the A, B, C, D code in the corresponding indirect registers (b3~0, T1/J1-RCRB-indirect registers - 21~38H). To avoid this 2 ms delay, users can read the corresponding b3~0 in the T1/J1-RCRB-indirect registers - (01~18H) first. If the value of these four bits are different from the previous A, B, C, D code, then the content of b3~0 in the T1/J1-RCRB-indirect registers - (01~18H) is the updated A, B, C, D code. If the content of the four bits is the same as the previous A, B, C, D code, then users should read the b3~0 in the T1/J1-RCRB-indirect registers - (21~38H) to get the updated A, B, C, D code.

Any one of the 24-channels signaling change will cause an interrupt on the $\overline{INT}$ pin if the SIGE (b5, T1/J1-040H) is set.

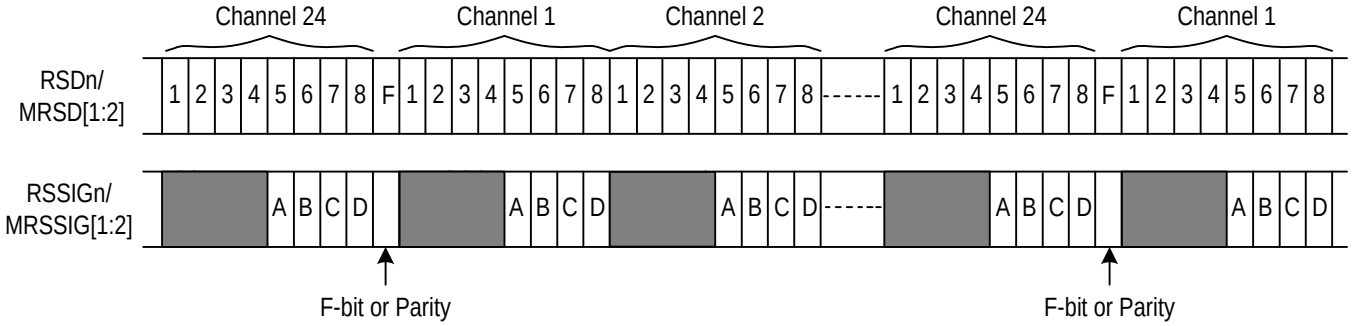


Figure 8. Signaling Output in T1/J1 Mode

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3.10 RECEIVE PAYLOAD CONTROL (RPLC)

Different test patterns can be inserted in the received data stream or the received data stream can be extracted to the PRBS Generator/ Detector for test in this block. The Receive Payload Control of each framer operates independently.

3.10.1 E1 MODE

To enable the test for the received data stream, the PCCE (b0, E1-05CH) must be set to activate the setting in the indirect registers (from 20H to 7FH of RPLC indirect registers). The following methods can be executed for test on a per-TS basis:

- Selected by the PRGDSEL[2:0] (b7~5, E1-00CH), the received data of one of the eight framers will be extracted to the PRBS Generator/ Detector when the RXPATGEN (b2, E1-00CH) is '0'. The received data can be extracted in framed or unframed mode, as determined by the UNF_DET (b0, E1-00CH). In unframed mode, all the 32 time slots are extracted and the per-timeslot configuration in the TEST (b7, E1-RPLC-indirect registers - 20~3FH) is ignored. In framed mode, the received data will only be extracted on the time slot configured by the TEST (b7, E1-RPLC-indirect registers - 20~3FH). Refer to Chapter 3.12 PRBS Generator / Detector (PRGD) for details.

- Replace the data that will be output on the RSDn/MRSD pin with the value in the DTRK[7:0] (b7~0, E1-RPLC-indirect registers - 40~5FH) when the DTRKC/NxTS (b6, E1-RPLC-indirect registers - 20~3FH) of the corresponding time slot is logic 1. (When it is out of Basic Frame synchronization, the value in the DTRK[7:0] [b7~0, E1-RPLC-indirect registers - 40~5FH] will replace the data automatically if the AUTOOOF [b1, E1-000H] is set. Or, when it is out of Basic Frame synchronization for 100 ms, the value in the DTRK[7:0] [b7~0, E1-RPLC-indirect registers - 40~5FH] will replace the data automatically if the AUTORED (b2, 000H) is set. These two kinds of data replacements can be executed even if the PCCE [b0, E1-05CH] is disabled and they replace all the time slots.)

- Replace the data that will be output on the RSDn/MRSD pin with the μ-law or A-law milliwatt pattern when the DMW (b4, E1-RPLC-indirect register - 20~3FH) of the corresponding time slot is logic 1. (The milliwatt pattern can be A-law or μ-law, as chosen by the DMWALAW [b3, E1-RPLC-indirect register - 20~3FH]. Refer to Table 8 & Table 9.)

- Selected by the PRGDSEL[2:0] (b7~5, E1-00CH), the test pattern from the PRBS Generator/Detector will replace the received data of one of the eight framers when the RXPATGEN (b2, E1-00CH) is '1'. The test pattern can replace the received data in framed or unframed mode, as determined by the UNF_GEN (b1, E1-00CH). In unframed mode, all 32 time slots are replaced and the per-timeslot configuration in the TEST (b7, E1-RPLC-indirect registers - 20~3FH) is ignored. In framed mode, the received data will only replace the time slot configured by the TEST (b7, E1-RPLC-indirect registers - 20~3FH). Refer to the section of PRBS GENERATOR / DETECTOR (PRGD) for details.

- Invert the most significant bit, the even bits and/or odd bits that will be output on the RSDn pin when the SIGNINV and the RINV[1:0] (b2~0, E1-RPLC-indirect registers - 20~3FH) of the corresponding time slot are set.

(The above methods are arranged from highest to lowest in priority.)

- Replace the signaling that will be output on the RSSIGn pin with the value in the A, B, C, D (b3~0, E1-RPLC-indirect registers - 61~7FH) when the STRKC (b5, E1-RPLC-indirect registers - 20~3FH) of the corresponding time slot allows.

The data and signaling of all time slots will be replaced with the setting in the DTRK[7:0] (b7~0, E1-RPLC-indirect registers - 40~5FH) and the A, B, C, D (b3~0, E1-RPLC-indirect registers - 61~7FH) respectively when the RXMTKC (b0, E1-001H) is set. To enable this function, PCCE (b0, E1-05CH) must be set to '1'.

Addressed by the A[6:0] (b6~0, E1-05EH), the data read from or written into the indirect registers is in the D[7:0] (b7~0, E1-05FH). The read or write operation is determined by the R/WB (b7, E1-05EH). The indirect registers have a read/write cycle. Before the read/write operation is completed, the BUSY (b7, E1-05DH) will be set. New operations on the indirect registers can only be implemented when the BUSY (b7, E1-05DH) is cleared. The read/write cycle is 490 ns.

Table 8: A-Law Digital Milliwatt Pattern

Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
0	0	1	1	0	1	0	0
0	0	1	0	0	0	0	1
0	0	1	0	0	0	0	1
0	0	1	1	0	1	0	0
1	0	1	1	0	1	0	0
1	0	1	0	0	0	0	1
1	0	1	0	0	0	0	1
1	0	1	1	0	1	0	0

Table 9: μ-Law Digital Milliwatt Pattern

Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
0	0	0	1	1	1	1	0
0	0	0	0	1	0	1	1
0	0	0	0	1	0	1	1
0	0	0	1	1	1	1	0
1	0	0	1	1	1	1	0
1	0	0	0	1	0	1	1
1	0	0	0	1	0	1	1
1	0	0	1	1	1	1	0

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3.10.2 T1/J1 MODE

To enable the test for the received data stream, the PCCE (b0, T1/J1-050H) must be set to activate the setting in the indirect registers (from 01H to 48H). The following methods can be used for test on a per-channel basis:

- Selected by the PRGDSEL[2:0] (b7~5, T1/J1-00FH), the received data of one of the eight framers will be extracted to the PRBS Generator/Detector when the RXPATGEN (b2, T1/J1-00FH) is '0'. The received data can be extracted in framed or unframed mode, as determined by the UNF_DET (b0, T1/J1-00FH). In unframed mode, all the 24 channels and the F-bit are extracted and the per-channel configuration in the TEST (b3, T1/J1-RPLC-indirect registers - 01~18H) is ignored. In framed mode, the received data will only be extracted on the channel specified by the TEST (b3, T1/J1-RPLC-indirect registers - 01~18H). Fractional T1/J1 signal can also be extracted in the specified channel when the Nx56k_DET (b3, T1/J1-00FH) is set. Refer to Chapter 3.12 PRBS Generator / Detector (PRGD) for details.

- Replace the data that will be output on the RSDn/MRSD pin with the value in the DTRK[7:0] (b7~0, T1/J1-RPLC-indirect registers - 19~30H) when the DTRKC (b6, T1/J1-RPLC-indirect registers - 01~18H) of the corresponding channel is logic 1. (When it is out of SF/ESF synchronization, the value in the DTRK[7:0] (b7~0, T1/J1-RPLC-indirect registers - 19~30H) will replace the data automatically if the AUTOOOF (b1, T1/J1-000H) is set. Or, when the RED alarm is declared, the value in the DTRK[7:0] (b7~0, T1/J1-RPLC-indirect registers - 19~30H) will replace the data automatically if the AUTORED (b2, T1/J1-000H) is set. These two kinds of data replacements can be executed even if the PCCE (b0, T1/J1-050H) is disabled and they replace all the channels.)

- Replace the data that will be output on the RSDn/MRSD pin with the milliwatt pattern when the DMW (b5, T1/J1-RPLC-indirect register - 01~18H) of the corresponding channel allows. (The milliwatt is μ-law. Refer to Table 9.)

- Selected by the PRGDSEL[2:0] (b7~5, T1/J1-00FH), the test pattern from the PRBS Generator/Detector will replace the received data of one of the eight framers when the RXPATGEN (b2, T1/J1-00FH) is '1'. The test pattern can replace the received data in framed or unframed mode, as determined by the UNF_GEN (b1, T1/J1-00FH). In unframed mode, all the 24 channels and the F-bit are replaced and the per-channel configuration in the TEST (b3, T1/J1-RPLC-indirect registers - 01~18H) is ignored. In framed mode, the received data will only be replaced on the channel specified by the TEST (b3, T1/J1-RPLC-indirect registers - 01~18H). Fractional T1/J1 signal can also be replaced in the specified channel when the Nx56k_GEN (b4, T1/J1-00FH) is set. Refer to Chapter 3.12 PRBS Generator / Detector (PRGD) for details.

- Invert the most significant bit and/or the other bits in a channel that will be output on the RSDn/MRSD pin when the SIGNINV and the INVERT (b4 & b7, T1/J1-RPLC-indirect registers - 01~18H) of the corresponding channel are set.

- Fix the signaling bit with the value in the POL (b0, T1/J1-RPLC-indirect registers - 01~18H) when the FIX (b1, T1/J1-RPLC-indirect registers - 01~18H) of the corresponding channel is logic 1.

(The above methods are arranged from highest to lowest in priority.)

- Replace the signaling that will be output on the RSSIGn/MRSSIG pin with the value in the A, B, C, D (b3~0, T1/J1-RPLC-indirect registers - 31~48H) when the STRKC (b7, T1/J1-RPLC-indirect registers - 31~48H) of the corresponding channel is logic 1.

The data and signaling of all channels will be replaced with the setting in the DTRK[7:0] (b7~0, T1/J1-RPLC-indirect registers - 19~30H) and the A, B, C, D (b3~0, T1/J1-RPLC-indirect registers - 31~48H) respectively when the IMTKC (b0, T1/J1-001H) is set. To enable this function, the PCCE (b0, T1/J1-050H) must be set to '1'.

Addressed by the A[6:0] (b6~0, T1/J1-052H), the data read from or written into the indirect registers is in the D[7:0] (b7~0, T1/J1-053H). The read or write operation is determined by the R/WB (b7, T1/J1-052H). Before the read/write operation is completed, the BUSY (b7, T1/J1-051H) will be set. New operations on the indirect registers can only be implemented when the BUSY (b7, T1/J1-051H) is cleared. The read/write cycle is 650 ns.

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3.11 RECEIVE SYSTEM INTERFACE (RESI)

The Receive System Interface determines how to output the received data to the system back-plane. The data from the eight framers can be aligned with each other or be output independently. The timing clocks and framing pulses can be provided by the system back-plane common to eight framers, or obtained from the far end of the individual eight framers. The Receive System Interface supports various configurations to meet various requirements in different applications.

3.11.1 E1 MODE

In E1 mode, the Receive System Interface can be set in Non-multiplexed Mode or Multiplexed Mode. In the Non-multiplexed Mode, the RSDn pin is used to output the received data from each framer at a bit rate of 2.048 Mb/s. While in the Multiplexed Mode, the received data from the eight framers is byte-interleaved to form two high speed data streams and outputs on the MRSD1 and MRSD2 pins at a bit rate of 8.192 Mb/s.

In the Non-multiplexed Mode, if the timing signal for clocking data on RSDn pin is provided by the system side and shared by all eight framers, the Receive System Interface should be set in Receive Clock Slave mode. If the timing signal for clocking data on each RSDn pin is received from each line side, the Receive System Interface should be set in Receive Clock Master mode.

In the Receive Clock Slave mode, if the multi-function pin RSCKn/RSSIGn is used to output a reference clock, the Receive System Interface is in Receive Clock Slave RSCK Reference Mode. If the RSCKn/RSSIGn pin is used to output the extracted signaling bits, the Receive System Interface is in Receive Clock Slave External Signaling mode.

In the Receive Clock Master mode, if the data in all 32 time slots in an E1 basic frame is clocked out by RSCKn, the Receive System Interface is in Receive Clock Master Full E1 mode. If the data in only some of the time slots in an E1 frame is clocked out by RSCKn, the Receive System Interface is in Receive Clock Master Fractional E1 (with F-bit) Mode.

Table 10 summarizes the receive system interface in different operation modes. To set the receive system interface of each framer into various operation modes, the registers must be configured as Table 11.

Table 10: E1 Mode Receive System Interface in Different Operation Modes

Operation Mode			Data Pin	Clock Pin	Framing Pin	Signaling Pin	Reference Clock Pin
Non-Multiplexed Mode	Clock Slave Mode	RSCK Reference	RSDn	RSCCK	RSCFS & RSFSn *	No	RSCKn
		External Signaling	RSDn	RSCCK	RSCFS & RSFSn *	RSSIGn	No
	Clock Master Mode	Full E1	RSDn	RSCKn	RSFSn	No	No
		Fractional E1 (with F-bit)	RSDn	RSCKn	RSFSn	No	No
Multiplexed Mode			MRSD	MRSCCK	MRSCFS & MRSFS *	MRSSIG	No

Note:
* In the Receive Clock Slave mode and Receive Multiplexed mode, there are two framing signals. In the Receive Clock Slave mode, the framing pulses on RSCFS can be ignored for some framers by setting the FPMODE (b5, E1-011H) to '0'. However, in the Receive Multiplexed mode, when the FPMODE (b5, E1-011H) of any of the eight framers is configured as logic 1, all the others are taken as logic 1. Only when all the FPMODE (b5, E1-011H) of the eight framers are configured as logic 0, the frame pulses on MRSCFS can be ignored. That is, the FPMODE (b5, E1-011H) should be configured to the same value in the Receive Multiplexed mode.

Table 11: Operation Mode Selection in E1 Receive Path

RATE[1:0] (b1~0, E1-010H)	RSCKSLV (b5, E1-010H)	RSSIG_EN (b6, E1-001H)	FRACTN[1:0] (b7~6, E1-010H)	Operation Mode
0 1	1	0	-	Receive Clock Slave RSCK Reference
		1	-	Receive Clock Slave External Signaling
	0	-	0 0	Receive Clock Master Full E1
			1 0	Receive Clock Master Fractional E1
			1 1	Receive Clock Master Fractional E1 with F-bit
1 1 (all the eight framers should be set)	1	1	-	Receive Multiplexed

3.11.1.1 Receive Clock Slave Mode

In the Receive Clock Slave Mode, the Receive Side System Common Clock (RSCCK) is provided by the system side. It is used as a common timing clock for all eight framers. The speed of RSCCK can be chosen by the CMS (b2, E1-010H) to be the same as the received data (2.048MHz), or double of the received data (4.096 MHz). The CMS (b2, E1-010H) of the eight framers should be set to the same value. If the speed of RSCCK is double that of the received data stream, there will be two active edges in one bit duration. In this case, the RSD_RSCFS_EDGE (b5, E1-014H) determines the active edge to update the signal on the RSDn, RSSIGn and RSFSn pins; however, the pulse on RSCFS (if exists) is always samples on its first active edge.

In the Receive Clock Slave Mode, the Receive Side System Common Frame Pulse (RSCFS) is used as a common framing signal to align

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the data streams for all eight framers. RSCFS asserts on each Basic Frame and its valid polarity is configured by the FPINV (b6, E1-011H). The framing signals on RSCFS can also be ignored by setting the FPMODE (b5, E1-011H) to '0'.

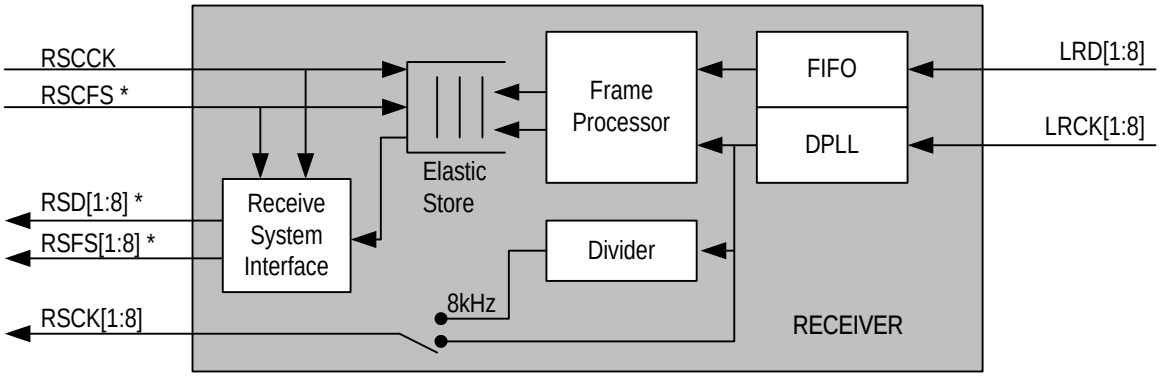
In the Receive Clock Slave Mode, the bit rate on the RSDn pin is 2.048Mb/s.

In the Receive Clock Slave Mode, the Receive Side System Frame Pulse (RSFSn) can be configured by the PERTS_RSFS (b3, E1-00EH) and REF_MRSFS (b2, E1-00EH) to output all zeros, to indicate the frame position or to output the same pulse as RSCFS. When it is defined to indicate the frame position, it can indicate the first bit of a Basic Frame, Signaling Multi-Frame, CRC-Multiframe, or both the Signaling and CRC-multiframe. This selection is made by the ROHM, BRXSMFP, BRXCMFP, ALTIFP (b3, b2, b1, b0, E1-011H). When RSFSn is for framing pulse indication, the valid polarity of it is configured by the FPINV (b6, E1-011H). In this case, if the FPMODE (b5, E1-011H) is low, RSFSn can only indicate the Basic Frame no matter what the setting in the ROHM, BRXSMFP, BRXCMFP, ALTIFP (b3, b2, b1, b0, E1-011H) is.

The Receive Clock Slave Mode includes two sub-modes: Receive Clock Slave RSCK Reference Mode and Receive Clock Slave External Signaling Mode.

3.11.1.1.1 Receive Clock Slave RSCK Reference Mode

In this mode (refer to Figure 9), the data on the system interface is clocked by RSCCK. The active edge of RSCCK to sample the pulse on RSCFS or to update the data on the RSDn and RSFSn pins is determined by the following bits in the registers (refer to Table 12).



Note: * RSCFS, RSD, RSFS are timed to RSCCK

Figure 9. Receive Clock Slave RSCK Reference Mode

Table 12: Active Edge Selection of RSCCK (in E1 Receive Clock Slave RSCK Reference Mode)

	Bit Determining the Active Edge of RSCCK
RSCFS	FE (b3, E1-010H)
RSFSn	
RSDn	DE (b4, E1-010H)

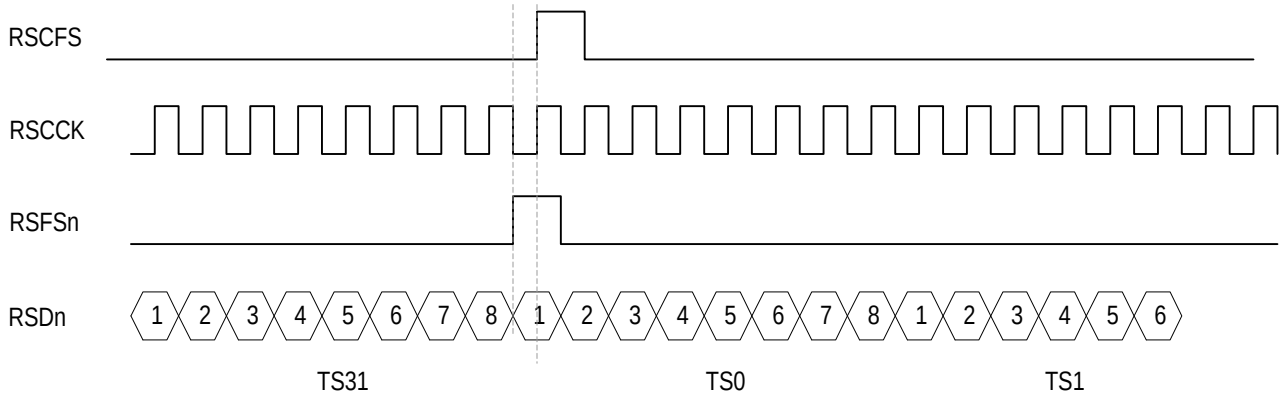
Note:
If the setting of the FE (b3, E1-010H) and DE (b4, E1-010H) is different, RSFSn will be one clock edge ahead of RSDn.
The FE (b3, E1-010H) of the eight framers should be set to the same value to ensure RSCFS for the eight framers is sampled on the same active edge.
There is a special case when the CMS (b2, E1-010H) is logic 1 and the DE (b4, E1-010H) is equal to FE (b3, E1-010H). The RSD_RSCFS_EDGE (b5, E1-014H) is invalid and the signal on the RSDn and the RSFSn pins are updated on the first active edge of RSCCK.

Figure 10 & Figure 11 show the functional timing examples. Bit 1 of each time slot is the first bit to be output.

Besides all the common functions described in the Receive Clock Slave mode, the special feature in this mode is that the multi-functional pin RSCKn/RSSIGn is used as RSCKn to output a reference clock. RSCKn can be chosen by the RSCKSEL (b5, E1-001H) to output a jitter attenuated 2.048MHz (i.e., smoothed LRCKn) or 8KHz clock (smoothed LRCKn divided by 256).

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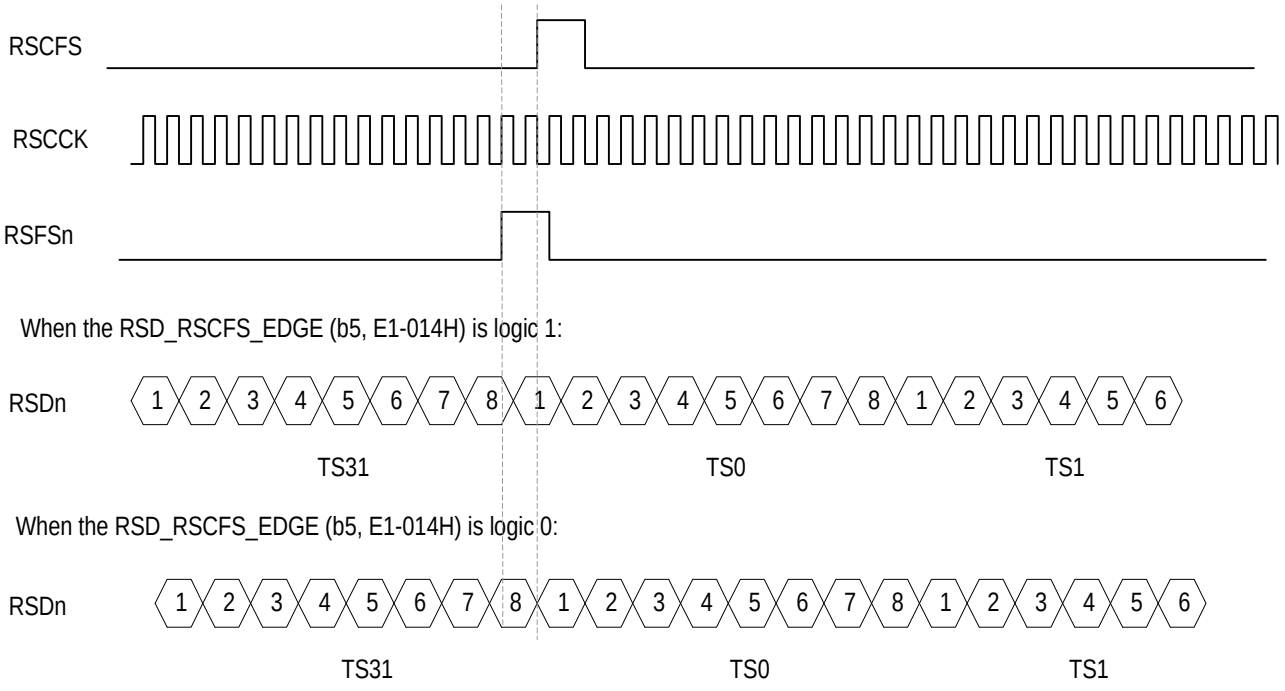
The CMS (b2, E1-010H) is logic 0, i.e., the backplane clock rate is 2.048Mbit/s.
The DE (b4, E1-010H) is logic 0 and the FE (b3, E1-010H) is logic 0. The timeslot offset and the bit offset enable are both 0:



(The RSCKn is selected by the RSCKSEL (b5, E1-001H) to output a jitter attenuated 2.048MHz (i.e., smoothed LRCKn) or 8KHz clock (smoothed LRCKn divided by 256).)

Figure 10. E1 Receive Clock Slave RSCK Reference Mode - Functional Timing Example 1

The CMS (b2, E1-010H) is logic 1, i.e., the backplane clock rate is 4.096Mbit/s.
The DE (b4, E1-010H) is logic 0 and the FE (b3, E1-010H) is logic 1.



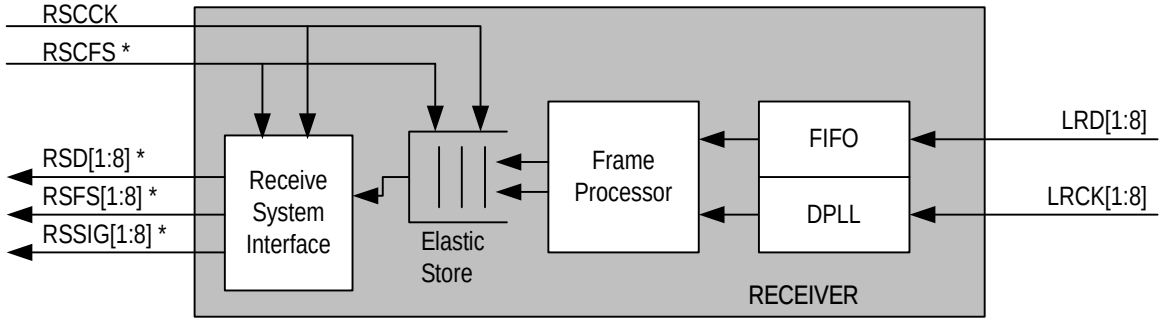
(The RSCKn is selected by the RSCKSEL (b5, E1-001H) to output a jitter attenuated 2.048MHz (i.e., smoothed LRCKn) or 8KHz clock (smoothed LRCKn divided by 256).)

Figure 11. E1 Receive Clock Slave RSCK Reference Mode - Functional Timing Example 2

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3.11.1.1.2 Receive Clock Slave External Signaling Mode

In this mode (refer to Figure 12), the data on the system interface is clocked by RSCCK. The active edge of RSCCK used to sample the pulse on RSCFS or to update the data on RSDn, RSFSn and RSSIGn is determined by the following bits in the registers (refer to Table 13).



Note: * RSCFS, RSD, RSSIG, RSFS are timed to RSCCK

Figure 12. Receive Clock Slave External Signaling Mode

Table 13: Active Edge Selection of RSCCK (in E1 Receive Clock Slave External Signaling Mode)

	Bit Determining the Active Edge of RSCCK
RSCFS	FE (b3, E1-010H)
RSFSn	
RSDn	DE (b4, E1-010H)
RSSIGn	

Note:
If the setting of the FE (b3, E1-010H) and DE (b4, E1-010H) is different, RSFSn will be one clock edge ahead of RSDn.
The FE (b3, E1-010H) of the eight framers should be set to the same value to ensure RSCFS for the eight framers is sampled on the same active edge.
There is a special case when the CMS (b2, E1-010H) is logic 1 and the DE (b4, E1-010H) is equal to FE (b3, E1-010H). The RSD_RSCFS_EDGE (b5, E1-014H) is invalid and the signal on the RSDn, RSSIGn and RSFSn pins are updated on the first active edge of RSCCK.

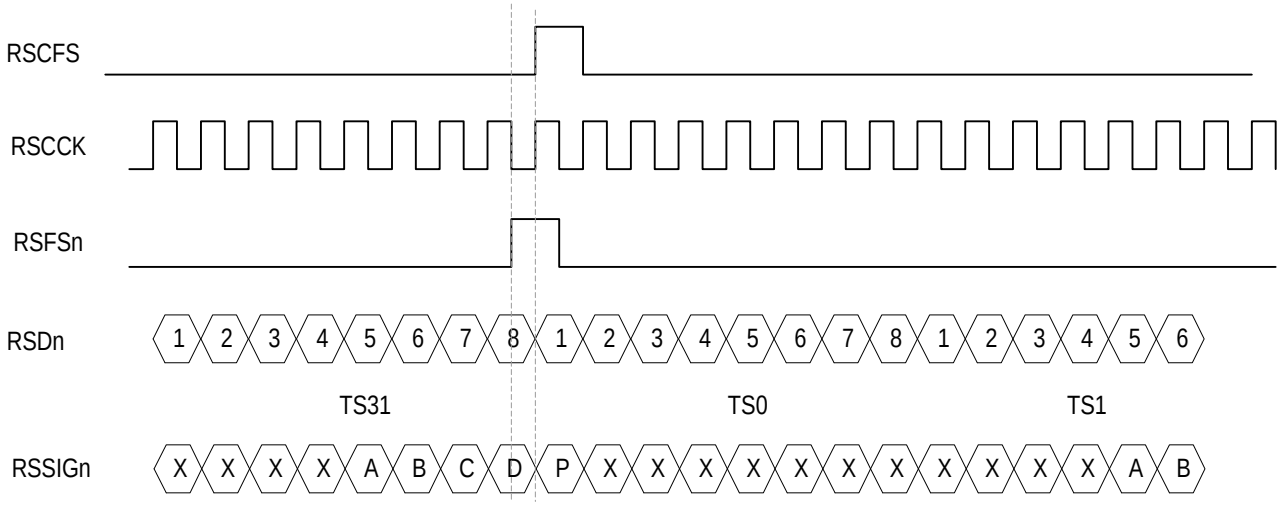
Figure 13 & Figure 14 show the functional timing examples. Bit 1 of each time slot is the first bit to be output.

Besides all the common functions described in the Receive Clock Slave mode, the special feature in this mode is that the multi-functional pin RSCKn/RSSIGn is used as RSSIGn to output the extracted signaling bits. The extracted signaling bits are time slot aligned with the data on the RSDn pin (refer to Figure 7).

In the Out of Signaling Multi-Frame condition, the output signaling bits ABCD on the RSSIGn pin can be forced to be all ones if the OOSMFAIS (b2, E1-001H) is set to '1'.

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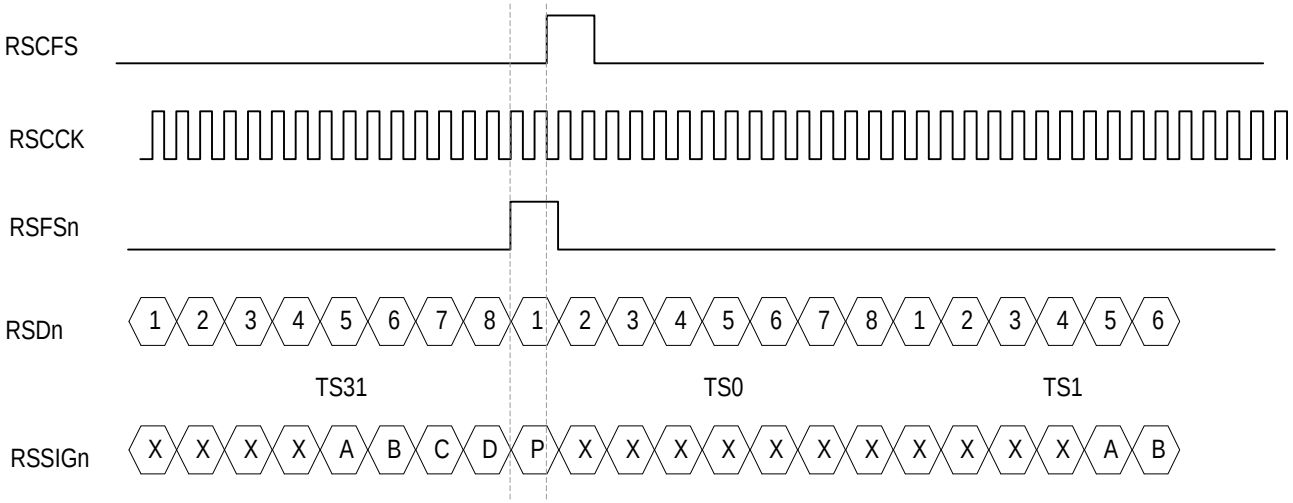
The CMS (b2, E1-010H) is logic 0, i.e., the bankplane rate is 2.048Mbit/s. The DE (b4, E1-010H) is logic 1 and the FE (b3, E1-010H) is logic 0. The timeslot offset and the bit offset enable are both 0:



(The 'X' represents the filled bits and has no meaning. The 'P' represents the Parity bit..)

Figure 13. E1 Receive Clock Slave External Signaling Mode - Functional Timing Example 1

The CMS (b2, E1-010H) is logic 1, i.e., the bankplane rate is 4.096Mbit/s.
The DE (b4, E1-010H) is logic 1 and the FE (b3, E1-010H) is logic 1. * The timeslot offset and the bit offset enable are both 0:



(The 'X' represent the filled bits and has no meaning. The 'P' represents the Parity bit..)

Note:
** It is a special case when the CMS (b2, E1-010H) is logic 1 and the DE (b4, E1-010H) is equal to FE (b3, E1-010H). The signal on the RSDn, RSSIGn and RSFSn are updated on the first active edge of RSCCK.*

Figure 14. E1 Receive Clock Slave External Signaling Mode - Functional Timing Example 2

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3.11.1.2 Receive Clock Master Mode

In the Receive Clock Master mode, each framer uses its own clock signal on the RSCKn pin and framing signal on the RSFSn pin to output the data on each RSDn pin. As the common framing signal RSCFS is not used, the FPMODE bit (b5, E1-011H) must be set to '0'.

In the Receive Clock Master Mode, the bit rate on the RSDn pin is 2.048Mb/s.

In the Receive Clock Master Mode, RSFSn can be configured by the PERTS_RSFS (b3, E1-00EH) and REF_MRSFS (b2, E1-00EH) to output all zeros, to indicate the frame position or to output the same pulse as RSCFS. When it is defined to indicate the frame position, it can indicate the first bit of a Basic Frame, Signaling Multi-Frame, CRC-Multi-frame, or both the Signaling and CRC-multiframe. This selection is made by the ROHM, BRXSMFP, BRXCMFP, ALTIFP (b3, b2, b1, b0, E1-011H). When RSFSn is used for framing pulse indication, the valid polarity of it is configured by the FPINV (b6, E1-011H). In this case, if the FPMODE (b5, E1-011H) is low, RSFSn can only indicate the Basic Frame no matter what the setting in the ROHM, BRXSMFP, BRXCMFP, ALTIFP (b3, b2, b1, b0, E1-011H) is.

In the Receive Clock Master Mode, the data on the system interface is clocked by RSCKn. The active edge of RSCKn used to update the data on RSDn and RSFSn is determined by the DE (b4, E1-010H) and the FE (b3, E1-010H) respectively as shown in Table 14.

The Receive Clock Master Mode includes two sub-modes: Receive Clock Master Full E1 Mode and Receive Clock Master Fractional E1 (with F-bit) Mode.

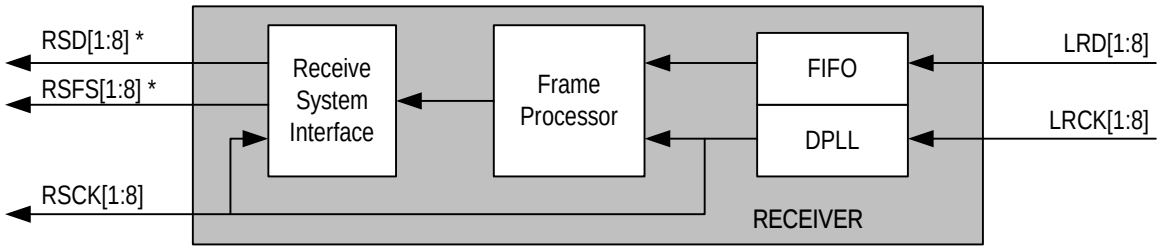
Table 14: Active Edge Selection of RSCK (in E1 Receive Clock Master Mode)

	the Bit Determining the Active Edge of RSCKn
RSFSn	FE (b3, E1-010H)
RSDn	DE (b4, E1-010H)
Note: If the setting in the FE (b3, E1-010H) and DE (b4, E1-010H) is different, RSFSn will be one clock edge ahead of RSDn.	

3.11.1.2.1 Receive Clock Master Full E1 Mode

Besides all the common functions described in the Receive Clock Master mode, the special feature in this mode (refer to Figure 15) is that RSCKn is a standard 2.048MHz clock, and the data in all 32 time slots in a standard E1 frame is clocked out by RSCKn.

Figure 16 shows the functional timing examples. Bit 1 of each time slot is the first bit to be output.



Note: * RSD, RSFS are timed to RSCK

Figure 15. Receive Clock Master Full E1 or T1/J1 Mode

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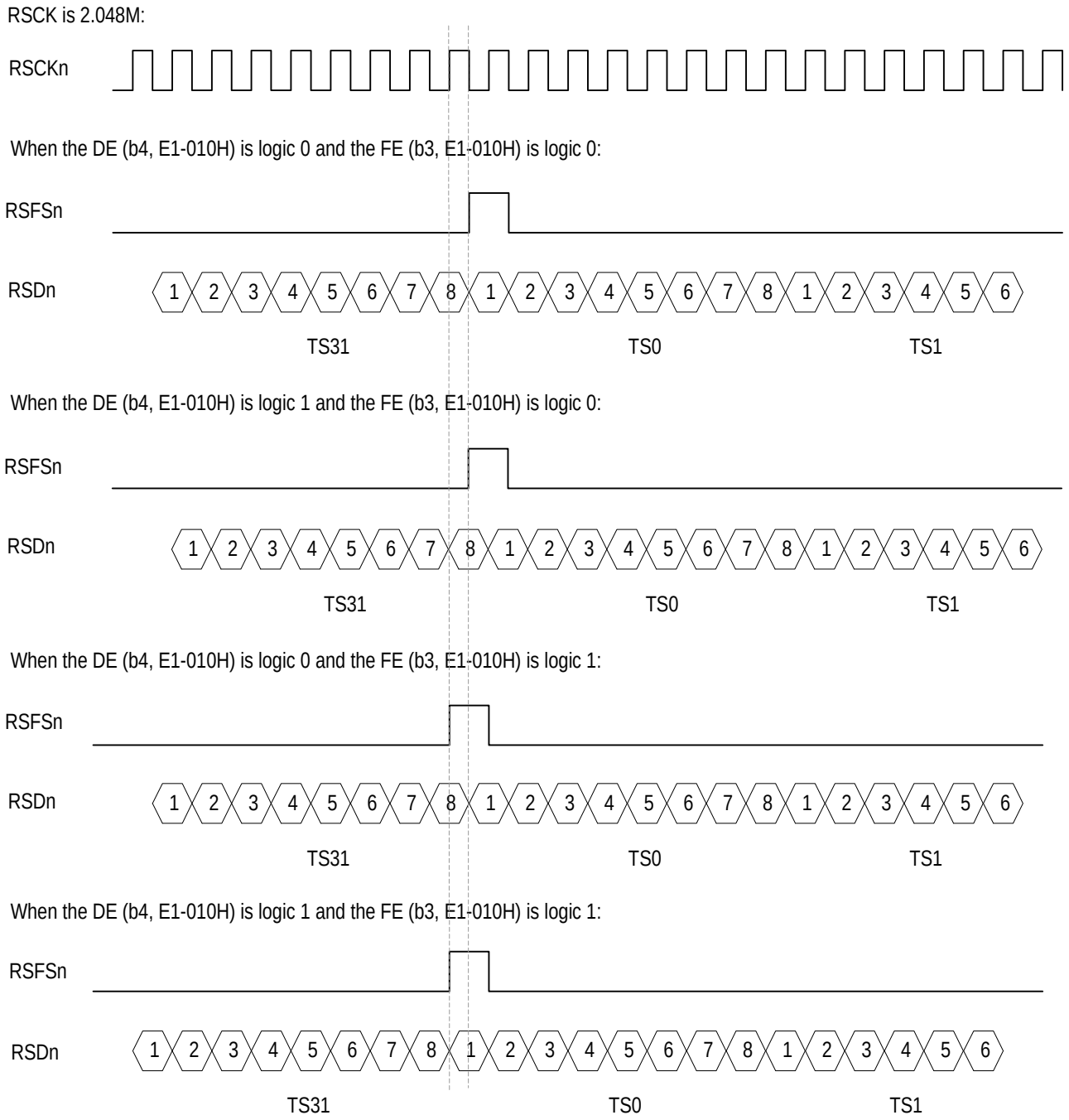
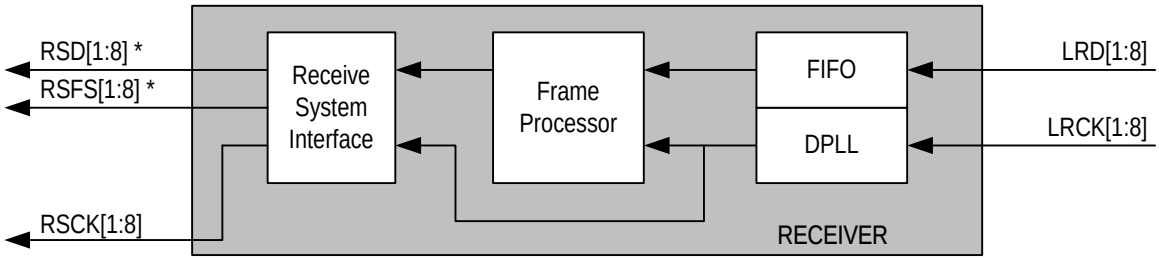


Figure 16. E1 Receive Clock Master Full E1 Mode - Functional Timing Example

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3.11.1.2.2 Receive Clock Master Fractional E1 (with F-bit) Mode

Besides all the common functions described in the Receive Clock Master mode, the special feature in this mode (refer to Figure 17) is that RSCKn is a gapped 2.048MHz clock (no clock signal during the selected time slot).



Note: * RSD, RSFS are timed to gapped RSCK

Figure 17. Receive Clock Master Fractional E1 or T1/J1 Mode

In the Receive Clock Master Fractional E1 mode, RSCKn is gapped during those time slots with their DTRKC/NxTS (b6, E1-RPLC-indirect register - 20~3FH) in Receive Payload Control are logic 1. It clocks out during those time slots with their DTRKC/NxTS_IDLE (b6, E1-RPLC-indirect register - 20~3FH) set to logic 0. The data in the corresponding gapped time slot is a don't-care. Figure 18 shows the functional timing examples. Bit 1 of each time slot is the first bit to be output.

The Receive Clock Master Fractional E1 with F-bit mode supports ITU recommendation G.802 where an E1 clock is output as a 193-bit T1 clock. In this mode, the RSCKn that starts from the 2nd bit of TS26 and ends at the last bit of the same Basic Frame are gapped, and the TS16 is also gapped. Thus, the DTRKC/NxTS (b6, E1-RPLC-indirect register - 20~3FH) of the time slots whose clock is gapped are invalid. The gapping of the remaining time slots is still determined by the DTRKC/NxTS (b6, E1-RPLC-indirect register - 20~3FH), and the data in the corresponding gapped time slot is a don't-care.

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RSCK is 2.048M. In this example, RSCK is supposed to be held in an inactive state during TS0.

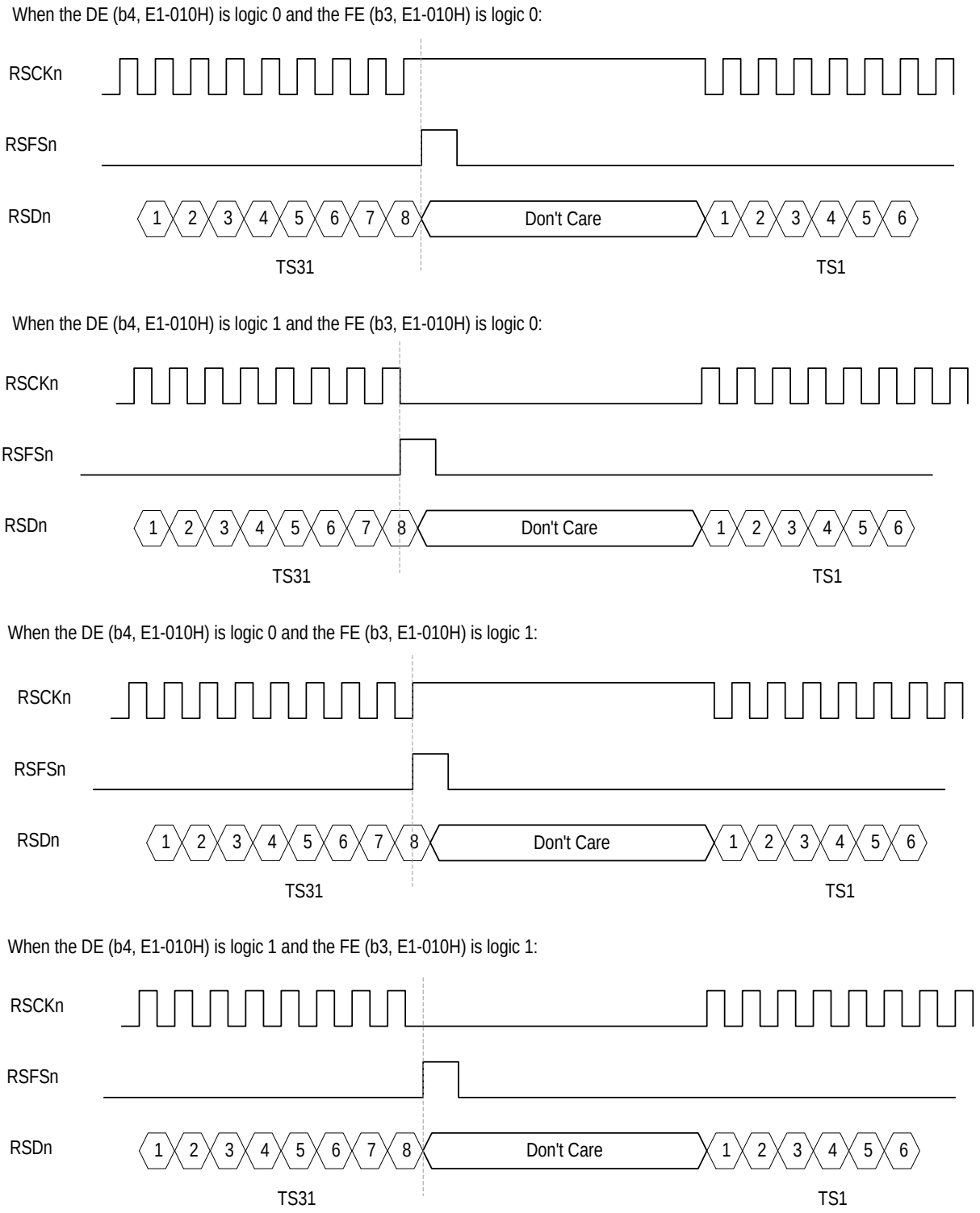
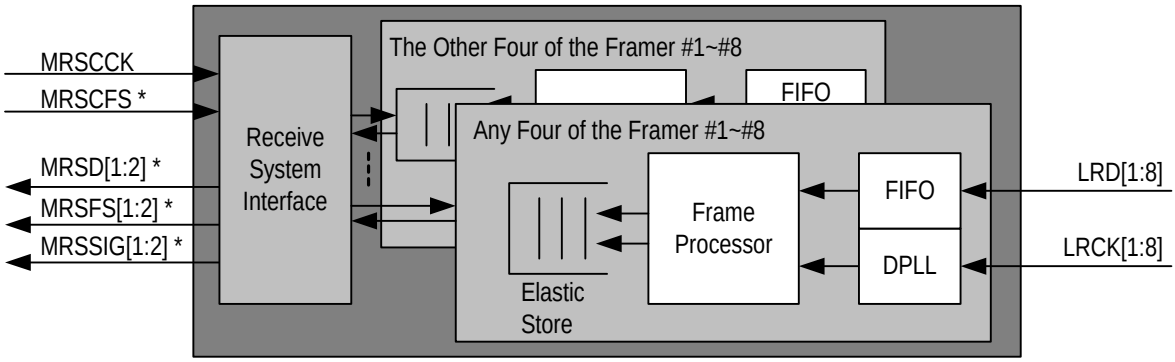


Figure 18. E1 Receive Clock Master Fractional E1 Mode - Functional Timing Example

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3.11.1.3 Receive Multiplexed Mode

In this mode (refer to Figure 19), two multiplexed buses are used to receive data from all eight framers. The data from up to four framers is byte-interleaved and output on one of the two multiplexed buses. The multiplexed bus is chosen by the MRBS (b4, E1-001H). When the data from four framers is output on one multiplexed bus, the sequence of the data is arranged by setting the time slot offset TSOFF[6:0] (b6~0, E1-013H). The data from different framers on one multiplexed bus must be shifted by a different time slot offset to avoid data mixing. Then the received data of each framer can be controlled by the MRBC (b3, E1-001H) to output to the selected multiplexed bus or not. The MRBC (b3, E1-001H) of the framers that are output to the same multiplexed bus must be set to the same value.



Note: * MRSCFS, MRSD, MRSFS, MRSSIG are timed to MRSCCK

Figure 19. Receive Multiplexed Mode

In the Receive Multiplexed mode, the data on the system interface is clocked by MRSCCK. The active edge of MRSCCK to sample the pulse on MRSCFS and to update the data on MRSD, MRSFS and MRSSIG is determined by the following bits in the registers (refer to Table 15).

Table 15: Active Edge Selection of MRSCCK (in E1 Receive Multiplexed Mode)

	the Bit Determining the Active Edge of MRSCCK
MRSCFS	FE (b3, E1-010H)
MRSFS	
MRSD	DE (b4, E1-010H)
MRSSIG	

Note:
If the setting in the FE (b3, E1-010H) and DE (b4, E1-010H) is different, MRSFS will be one clock edge ahead of MRSD.
The FE (b3, E1-010H) and DE (b4, E1-010H) of all eight framers should be configured to the same value.
There is a special case when the CMS (b2, E1-010H) is logic 1 and the DE (b4, E1-010H) is equal to FE (b3, E1-010H). The RSD_RSCFS_EDGE (b5, E1-014H) is invalid and the signals on the MRSD, MRSSIG and MRSFS pins are updated on the first active edge of MRSCCK.

In the Receive Multiplexed mode, the Multiplexed Receive Side System Common Clock (MRSCCK) is provided by the system side. It is used as a common timing clock for all eight framers. The frequency of RSCCK can be chosen by the CMS (b2, E1-010H) to be the same as the bit rate of the received data stream (8.192Mb/s), or double the bit rate of the received data stream (16.384 Mb/s). If the frequency of RSCCK is double the bit rate of the received data stream, there will be two active edges in one bit time. In this case, the RSD_RSCFS_EDGE (b5, E1-014H) determines the active edge to update the signals on the MRSD, MRSSIG and MRSFS pins; however, the pulse on MRSCFS (if it exists) is always sampled on its first active edge. However, if the CMS (b2, E1-010H) or the RSD_RSCFS_EDGE (b5, E1-014H) of any of the eight framers is configured as logic 1, all the others are taken as logic 1. That is, the CMS (b2, E1-010H) and the RSD_RSCFS_EDGE (b5, E1-014H) of the eight framers should be configured to the same value in the Receive Multiplexed mode.

In the Receive Multiplexed mode, the Multiplexed Receive Side System Common Frame Pulse (MRSCFS) is used as a common framing signal to align the data streams on the two multiplexed buses. MRSCFS asserts on each first bit of Basic Frame of the selected first framer. The valid polarity of MRSCFS is configured by the FPINV (b6, E1-011H). The framing signals on MRSCFS will also be ignored by setting the FPMODE (b5, E1-011H) to '0'. The FPINV (b6, E1-011H) and the FPMODE (b5, E1-011H) of the eight framers should be set to the same value.

In the Receive Multiplexed mode, the bit rate on the MRSD pin is 8.192Mb/s.

In the Receive Multiplexed mode, MRSFS can be configured by the PERTS_RSFS (b3, E1-00EH) and REF_MRSFS (b2, E1-00EH) to output all zeros, to indicate the frame position or to output the same pulse as MRSCFS. The PERTS_RSFS (b3, E1-00EH) and REF_MRSFS (b2, E1-00EH) of the eight framers should be set to the same value. When it is defined to indicate the frame position, MRSFS can only indicate the first bit of a Basic Frame of the selected first framer no matter what is set in the ROHM, BRXSMFP, BRXCMFP, ALTIFP (b3, b2, b1, b0, E1-011H).

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When it is for framing pulse indication, the valid polarity of MRSFS is configured by the FPINV (b6, E1-011H). The FPINV (b6, E1-011H) of the eight framers should be set to the same value.

In the Receive Multiplexed mode, MRSSIG outputs extracted signaling. The extracted signaling bits are time slot aligned with the data output on MRSD. In the Out of Signaling Multi-Frame condition, the output signaling ABCD on the MRSSIG pin will be forced to be all ones if the OOSMFAIS (b2, E1-001H) is set.

Figure 20 & Figure 21 show the functional timing examples. Bit 1 of each time slot is the first bit to be output.

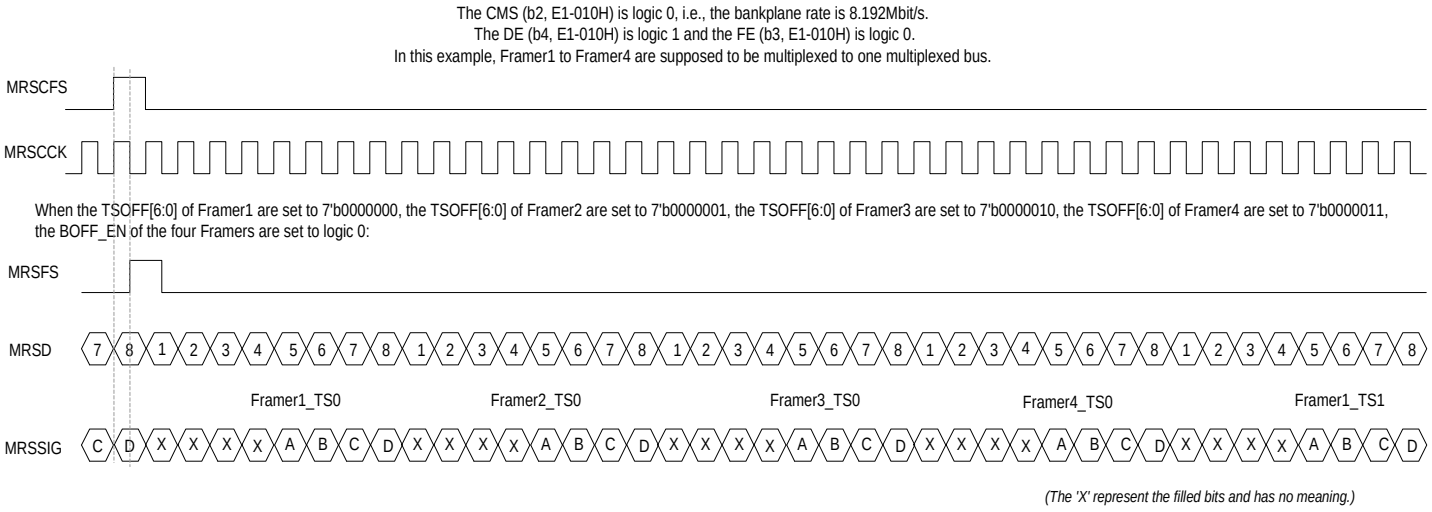


Figure 20. E1 Receive Multiplexed Mode - Functional Timing Example 1

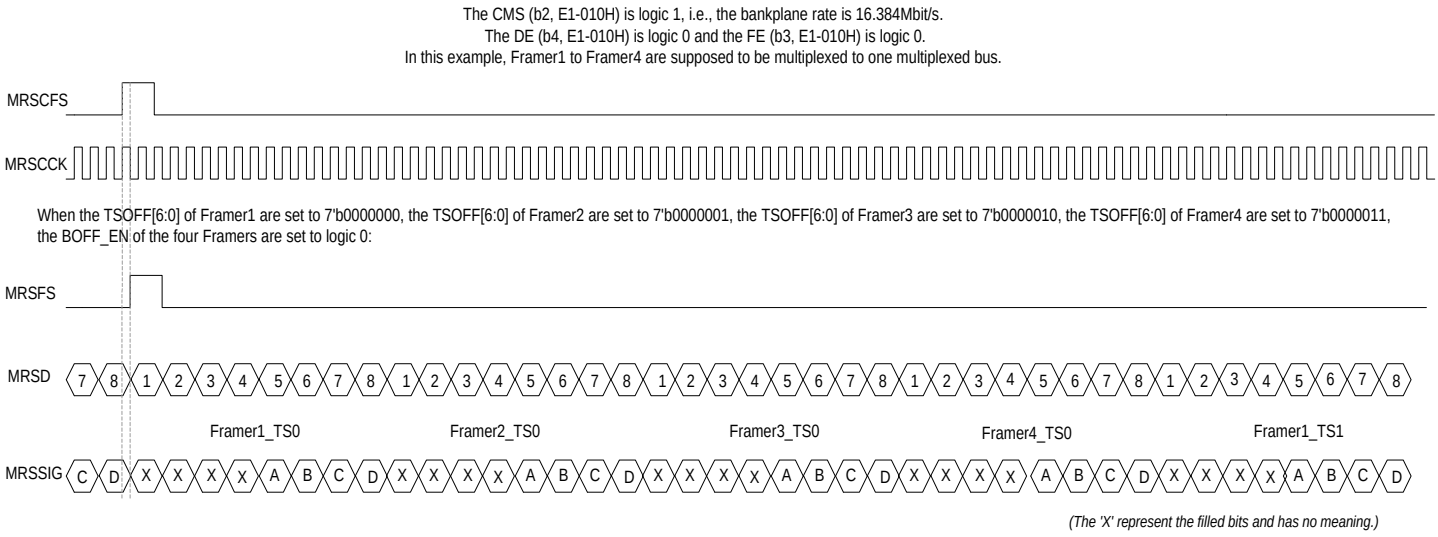


Figure 21. E1 Receive Multiplexed Mode - Functional Timing Example 2

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3.11.1.4 Parity Check & Polarity Fix

In all the above modes except for the Receive Clock Slave Fractional E1 (with F-bit) mode, if the RPTYE (b6, E1-012H) is logic 1, parity check will be conducted over the bits in the previous Basic Frame and the result is inserted into the first bit (MSB) of TS0 on the RSDn/MRSD pin. The even parity or odd parity is chosen by the RPTYP (b7, E1-012H) and whether the first bit of TS0 is calculated or not is determined by the PTY_EXTD (b3, E1-012H). Alternatively this first bit of TS0 can be forced to be logic 0 or 1 by setting the value in the FIXPOL (b4, E1-012H) when the FIXF (b5, E1-012H) is set. The priority of the FIXF (b5, E1-012H) is lower than the RPTYE (b6, E1-012H).

3.11.1.5 Offset

In the above five modes, time slot offset and/or bit offset can be configured. If the offset is configured, the offset between different operation modes is summarized in Table 16. Bit offset is disabled when the CMS (b2, E1-010H) is logic 1.

Table 16: Offset in Different Operation Modes

Operation Mode	FPMODE (b5, E1-011H)	Offset
Receive Clock Slave mode	1	The offset is between RSCFS and the start of the corresponding frame on RSDn (and RSSIGn).
	0	The offset is between RSFSn and the start of the corresponding frame on RSDn (and RSSIGn).
Receive Clock Master mode	0 (must be zero)	The offset is between RSFSn and the start of the corresponding frame on RSDn.
Receive Multiplexed mode	1 (in any of the eight framers)	The offset is between MRSCFS and the start of the corresponding frame on MRSD and MRSSIG.
	0	The offset is between MRSFS and the start of the corresponding frame on MRSD and MRSSIG.

The time slot offset is configured in the TSOFF[6:0] (b6~0, E1-013H). The TSOFF[6:0] (b6~0, E1-013H) give a binary representation.

Enabled by the BOFF_EN (b3, E1-014H), the bit offset is configured in the BOFF[2:0] (b2~0, E1-014H). The bit offset follows the Concentration Highway Interface (CHI) specification (refer to Table 17 & Table 18). When the bit offset is between RSCFS/MRSCFS and the start of the corresponding frame on RSDn/MRSD, the CET (clock edge transmit) is counted from the active edge of RSCFS/MRSCFS (refer to the example in Figure 22). The pulse on RSFSn/MRSFS and the signal on RSSIGn/MRSSIG (if it exists) are aligned to RSDn/MRSD. When the bit offset is between RSFSn/MRSFS and the start of the corresponding frame on RSDn/MRSD, the CET is counted from the active edge of RSFSn/MRSFS (refer to the example in Figure 23). The signal on RSSIGn/MRSSIG (if it exists) is aligned to RSDn/MRSD.

Note that it is a special case when the BRXSMFP and the ALTIFP (b2, b0, E1-011H) are both set to logical 1. In this case, there is bit offset between the output on RSFSn and RSDn. Refer to Table 19 for the details.

Table 17: Receive System Interface Bit Offset (FPMODE [b5, E1-011H] = 0)

FE (b3, E1-010H)	DE (b4, E1-010H)	BOFF[2:0] (b2~0, E1-014H)								
		000	001	010	011	100	101	110	111	
0	0	4	6	8	10	12	14	16	18	CET
0	1	3	5	7	9	11	13	15	17	
1	0	3	5	7	9	11	13	15	17	
1	1	4	6	8	10	12	14	16	18	

Table 18: Receive System Interface Bit Offset (FPMODE [b5, E1-011H] = 1)

FE (b3, E1-010H)	DE (b4, E1-010H)	BOFF[2:0] (b2~0, E1-014H)								
		000	001	010	011	100	101	110	111	
0	0	2	4	6	8	10	12	14	16	CET
0	1	1	3	5	7	9	11	13	15	
1	0	1	3	5	7	9	11	13	15	
1	1	2	4	6	8	10	12	14	16	

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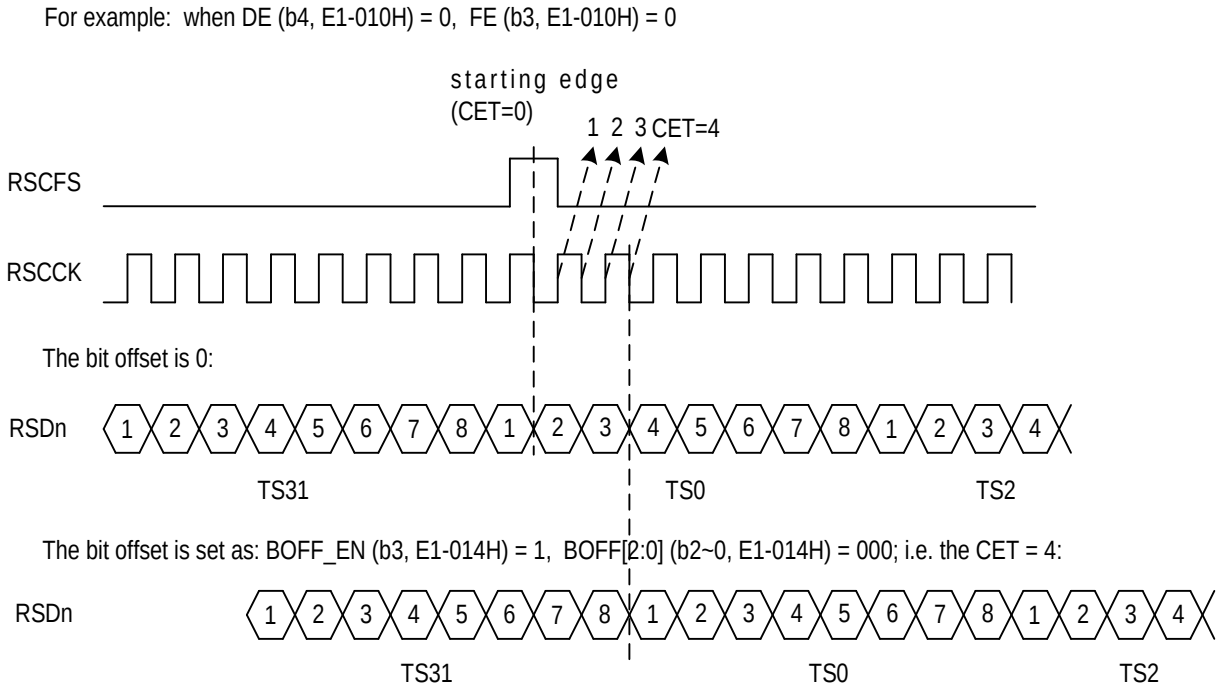


Figure 22. Receive Bit Offset - Between RSCFS & RSDn

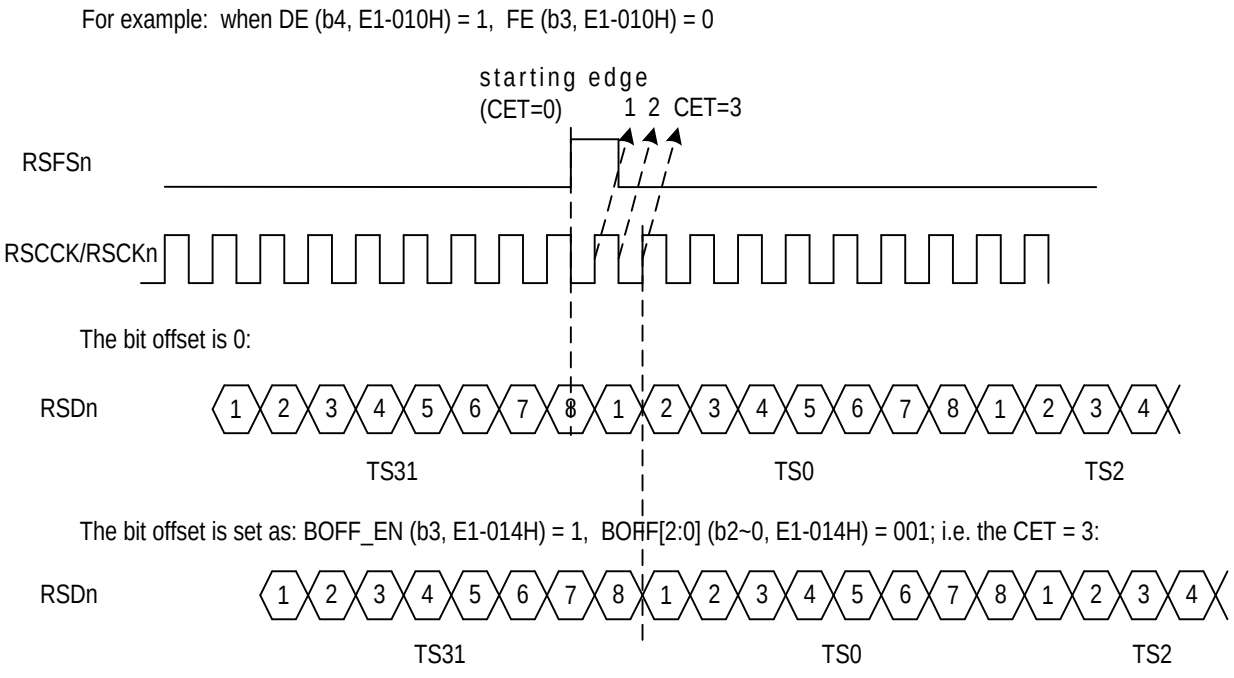


Figure 23. Receive Bit Offset - Between RSFSn & RSDn

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Table 19: Bit Offset Between RSFSn and RSDn When the BRXSMFP and the ALTIFP (b2, b0, E1-011H) are Both Set To Logical 1

BOFF_EN (b3, E1-014H)	FPMODE (b5, E1-011H)	DE (b4, E1-010H) & FE (b3, E1-010H)	Bit Offset Between RSFSn and RSDn
0	X	Same	1 bit offset. RSFSn is ahead.
		Difference	1.5 bit offset. RSFSn is ahead.
1	1	Same	1 bit offset. RSFSn is ahead.
		Difference	1.5 bit offset. RSFSn is ahead.
	0	Same	CHI specification (Table 17)
		Difference	

3.11.1.6 Output On RSDn/MRSD & RSSIGn/MRSSIG

In all the five modes, the RSDn/MRSD and the RSSIGn/MRSSIG pins can be configured by the TRI[1:0] (b1~0, E1-012H) of the corresponding framer to be in high impedance state or to output the processed data stream. However, in the Receive Multiplexed Mode, the TRI[1:0] (b1~0, E1-012H) of the framers that are output to the same multiplexed bus must be set to the same value.

The data output on the RSDn/MRSSIG pin will be forced to be all ones, and the signaling output on the RSSIGn/MRSSIG pin (if it exists) will be forced to be frozen at the current valid signaling when the RAIS (b1, E1-007H) is set.

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3.11.2 T1/J1 MODE

In T1/J1 mode, the Receive System Interface can be set in Non-multiplexed Mode or Multiplexed Mode. In the Non-multiplexed Mode, the RSDn pin is used to output the received data from each framer at a bit rate of 1.544 Mb/s or 2.048 Mb/s (T1/J1 mode E1 rate). While in the Multiplexed Mode, the received data from the eight framers is converted to 2.048 Mb/s format and byte-interleaved to form two high speed data streams and outputs on the MRSD1 and MRSD2 pins at a bit rate of 8.192 Mb/s.

In the Non-multiplexed Mode, if the timing signal for clocking data on the RSDn pin is provided by the system side and shared by all eight framers, the Receive System Interface should be set in Receive Clock Slave mode. If the timing signal for clocking data on each RSDn pin is received from each line side, the Receive System Interface should be set in Receive Clock Master mode.

In the Receive Clock Slave mode, if the multi-function pin RSCKn/RSSIGn is used to output a reference clock, the Receive System Interface is in Receive Clock Slave RSCK Reference Mode. If the RSCKn/RSSIGn pin is used to output the extracted signaling bits, the Receive System Interface is in Receive Clock Slave External Signaling mode.

The T1/J1 mode E1 rate, which means the system clock rate is 2.048 MHz in T1/J1 mode, can only be supported in the Receive Clock Slave mode.

In the Receive Clock Master mode, if the data in all 24 channels of a T1/J1 basic frame is clocked out by RSCKn, the Receive System Interface is in Receive Clock Master Full T1/J1 mode. If the data in only some time slots of a T1/J1 frame is clocked out by RSCKn, the Receive System Interface is in Receive Clock Master Fractional T1/J1 Mode.

Table 20 summarizes the receive system interface in different operating modes. To set the receive system interface of each framer into various operating modes, the registers must be configured as Table 21.

Table 20: T1/J1 Mode Receive System Interface in Different Operation Modes

Operation Mode			Data Pin	Clock Pin	Framing Pin	Signaling Pin	Reference Clock Pin
Non-Multiplexed Mode	Clock Slave Mode	RSCK Reference	RSDn	RSCCK	RSCFS/RSFSn	No	RSCKn
		External Signaling	RSDn	RSCCK	RSCFS/RSFSn	RSSIGn	No
	Clock Master Mode	Full T1/J1	RSDn	RSCKn	RSFSn	No	No
		Fractional T1/J1	RSDn	RSCKn	RSFSn	No	No
Multiplexed Mode			MRSD	MRSCCK	MRSCFS/MRSFS	MRSSIG	No

Table 21: Operation Mode Selection in T1/J1 Receive Path

RSCCK2M / RSCCK8M (b4, T1/J1-001H) / (b3, T1/J1-001H)	IMODE[1:0] (b7~6, T1/J1-001H)	Operation Mode
00 / 10 *	10	Receive Clock Slave RSCK Reference
	11	Receive Clock Slave External Signaling
00	01	Receive Clock Master Full T1/J1
	00	Receive Clock Master Fractional T1/J1
01 (in any of the eight framers)	11	Receive Multiplexed

Note:
* When the RSCCK2M / RSCCK8M are '00', the system clock rate is 1.544MHz.
When the RSCCK2M / RSCCK8M are '10', the system clock rate is 2.048MHz, i.e., T1/J1 mode E1 rate.

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3.11.2.1 Receive Clock Slave Mode

In the Receive Clock Slave Mode, the bit rate on the RSDn pin is 1.544Mb/s. However, if the system clock rate is 2.048MHz, the received data stream (1.544 Mb/s) should be converted to the same rate as the system side, that is, to work in T1/J1 mode E1 rate. Thus, the RSCCK2M (b4, T1/J1-001H) and the RSCCK8M (b3, T1/J1-001H) should be set to logic 1 and 0 respectively. The conversion complies as follows: One dummy byte is inserted in the system side before 3 bytes of Frame N from the device are converted. This process repeats 8 times and the conversion of Frame N of 1.544M bit/s data rate to 2.048M bit/s data rate is completed. However, the F-bit of Frame N of the 1.544M bit/s data rate is inserted as the 8th bit of the N of the 2.048M bit/s data rate (refer to Figure 24).

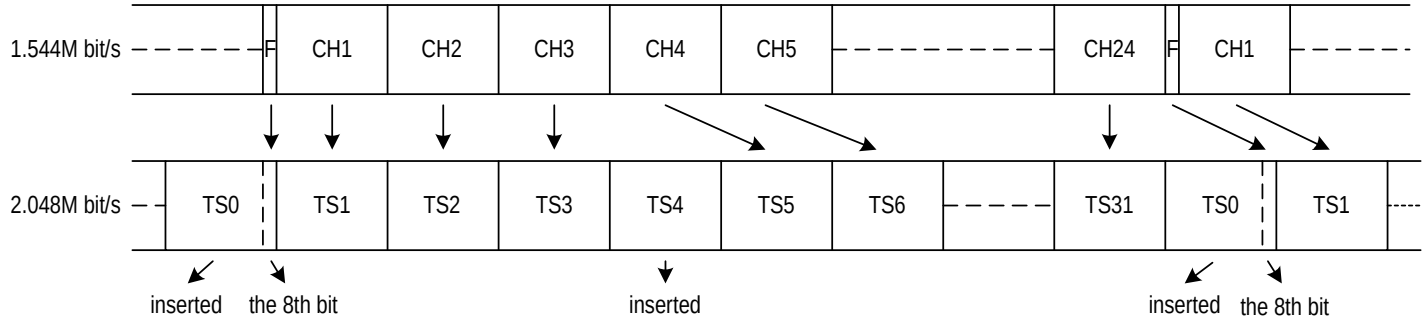


Figure 24. T1/J1 To E1 Format Conversion

In the Receive Clock Slave Mode, the Receive Side System Common Clock (RSCCK) is provided by the system side. It is used as a common timing clock for all eight framers. The speed of RSCCK can be 1.544MHz or 2.048MHz. When it is 2.048MHz, RSCCK can be chosen by the CMS (b4, T1/J1-078H) to be the same as the received data (2.048Mb/s), or double the received data (4.096 Mb/s). The CMS (b4, T1/J1-078H) of the eight framers should be set to the same value. If the speed of RSCCK is double the received data stream, there will be two active edges in one bit duration. In this case, the RSD_RSCFS_EDGE (b5, T1/J1-078H) determines the active edge to update the signal on the RSDn, RSSIGn and RSFSn pins; however, the pulse on RSCFS is always sampled on its first active edge.

In the Receive Clock Slave Mode, the Receive Side System Common Frame Pulse (RSCFS) is used as a common framing signal to align the data stream for all eight framers. RSCFS asserts on each F-bit and its valid polarity is configured by the FPINV (b6, T1/J1-078H).

In the Receive Clock Slave Mode, RSFSn can indicate each F-bit of SF/ESF, every second F-bit, the first F-bit of every 12 frames (in SF format) or every 24 frames (in ESF format). All the indications are selected by the RSFSP (b2, T1/J1-001H) and ALTIFP (b1, T1/J1-001H). The valid polarity of RSFSn is configured by the FPINV (b6, T1/J1-078H).

The Receive Clock Slave Mode includes two sub-modes: Receive Clock Slave RSCK Reference Mode and Receive Clock Slave External Signaling Mode. Note that if the receive system interface is configured to operate in T1/J1 mode E1 rate, framer 1, 3, 5, 7 must be configured in the same sub-mode and framer 2, 4, 6, 8 must be configured in the same sub-mode.

3.11.2.1.1 Receive Clock Slave RSCK Reference Mode

In this mode (refer to Figure 9), the data on the system interface is clocked by RSCCK. The active edge of RSCCK to sample the data on the RSCFS pin or to update the data on the RSDn and RSFSn pins is determined by the following bits in the registers (refer to Table 22).

Table 22: Active Edge Selection of RSCCK (in T1/J1 Receive Clock Slave RSCK Reference Mode)

	the Bit Determining the Active Edge of RSCCK
RSCFS	RSCFSFALL (b1, T1/J1-003H)
RSFSn	RSCCKRISE (b0, T1/J1-003H)
RSDn	

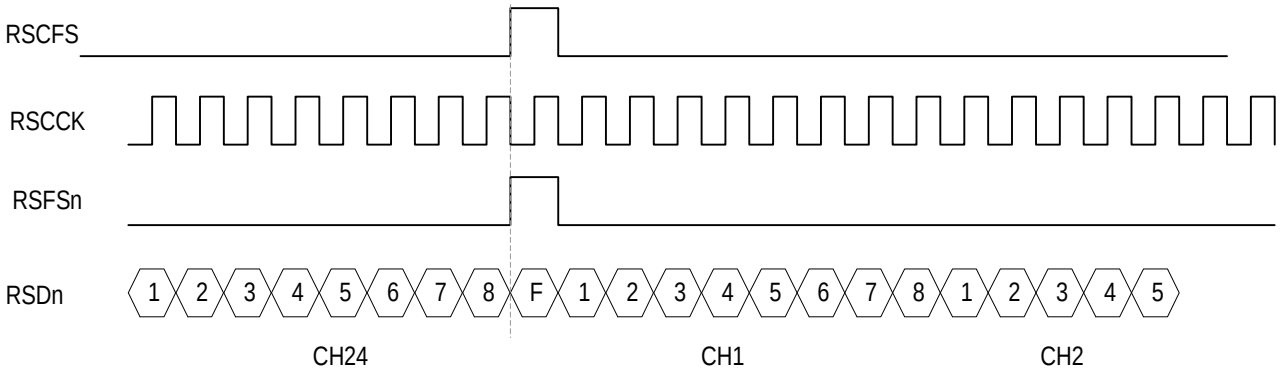
Note:
The RSCFSFALL (b1, T1/J1-003H) of the eight framers should be set to the same value to ensure RSCFS for the eight framers is sampled on the same active edge.
It is a special case when the CMS (b4, T1/J1-078H) is logic 1 and the RSCFSFALL (b1, T1/J1-003H) is not equal to RSCCKRISE (b0, T1/J1-003H). The RSD_RSCFS_EDGE (b5, T1/J1-078H) is invalid and the signals on the RSDn and the RSFSn pins are updated on the first active edge of RSCCK.

Figure 25 to Figure 27 show the functional timing examples. Bit 1 of each channel is the first bit to be output.

Besides all the common functions described in the Receive Clock Slave mode, the special feature in this mode is that the multi-functional pin RSCKn/RSSIGn is used as RSCKn to output a reference clock. RSCKn can be chosen by the RSCKSEL (b5, T1/J1-001H) to output a jitter attenuated 1.544MHz (i.e., smoothed LRCKn) or 8KHz clock (smoothed LRCKn divided by 193).

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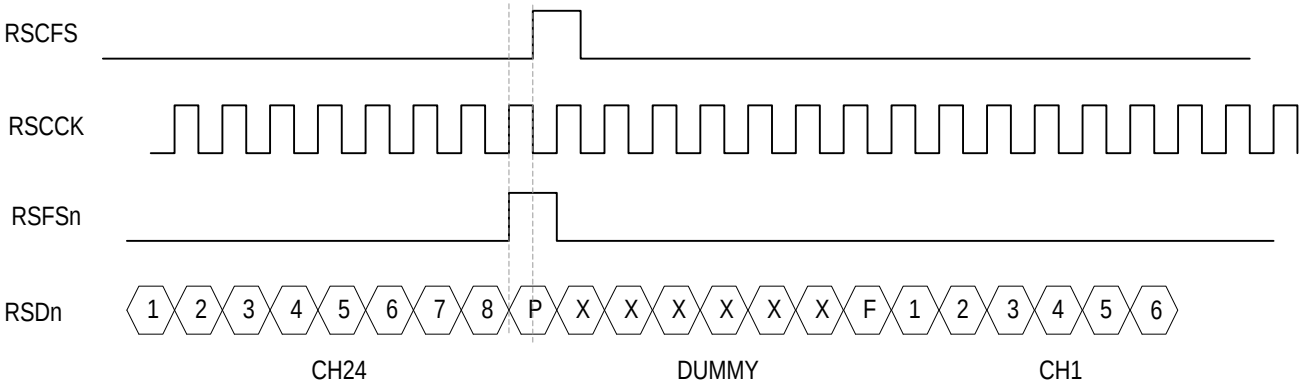
The CMS (b4, T1/J1-078H) is logic 0 and the bankplane rate is 1.544Mbit/s.
The RSCFSFALL (b1, T1/J1-003H) is logic 0 and the RSCCKRISE (b0, T1/J1-003H) is logic 0.
The channel offset and the bit offset enable are both 0:



(The RSCKn is selected by the RSCKSEL (b5, T1/J1-001H) to output a jitter attenuated 1.544MHz (i.e., smoothed LRCKn) or 8KHz clock (smoothed LRCKn divided by 193).)

Figure 25. T1/J1 Receive Clock Slave RSCK Reference Mode - Functional Timing Example 1

The CMS (b4, T1/J1-078H) is logic 0 and the bankplane clock rate is 2.048Mbit/s.
The RSCFSFALL (b1, T1/J1-003H) is logic 0 and the RSCCKRISE (b0, T1/J1-003H) is logic 1.
The channel offset and the bit offset enable are both 0:



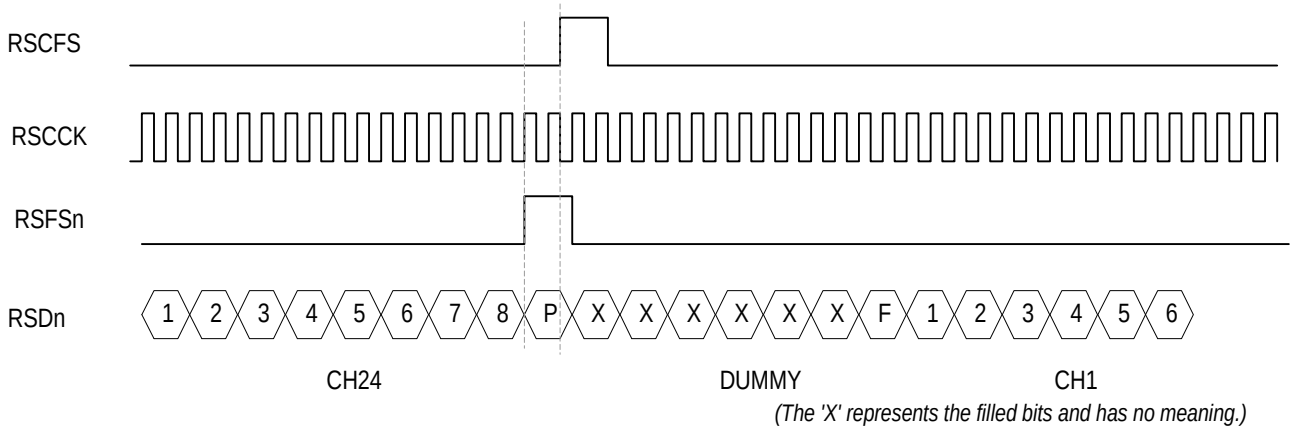
(The 'X' represent the filled bits and has no meaning.)

(The RSCKn is selected by the RSCKSEL (b5, T1/J1-001H) to output a jitter attenuated 1.544MHz (i.e., smoothed LRCKn) or 8KHz clock (smoothed LRCKn divided by 193).)

Figure 26. T1/J1 Receive Clock Slave RSCK Reference Mode - Functional Timing Example 2

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The CMS (b4, T1/J1-078H) is logic 1, i.e., the bankplane clock rate is 4.096Mbit/s.
The RSCFSFALL (b1, T1/J1-003H) is logic 0 and the RSCCKRISE (b0, T1/J1-003H) is logic 1.
When the channel offset and the bit offset enable are both 0:



(The 'X' represents the filled bits and has no meaning.)

(The RSCKn is selected by the RSCKSEL (b5, T1/J1-001H) to output a jitter attenuated 1.544MHz (i.e., smoothed LRCKn) or 8KHz clock (smoothed LRCKn divided by 193).)

Figure 27. T1/J1 Receive Clock Slave RSCK Reference Mode - Functional Timing Example 3

3.11.2.1.2 Receive Clock Slave External Signaling Mode

In this mode (refer to Figure 12), the data on the system interface is clocked by RSCCK. The active edge of RSCCK to sample the pulse on RSCFS or to update the data on the RSDn, RSFSn and RSSIGn pins is determined by the following bits in the registers (refer to Table 23).

Table 23: Active Edge Selection of RSCCK (in T1/J1 Receive Clock Slave External Signaling Mode)

	the Bit Determining the Active Edge of RSCCK
RSCFS	RSCFSFALL (b1, T1/J1-003H)
RSFSn	RSCCKRISE (b0, T1/J1-003H)
RSDn	
RSSIGn	

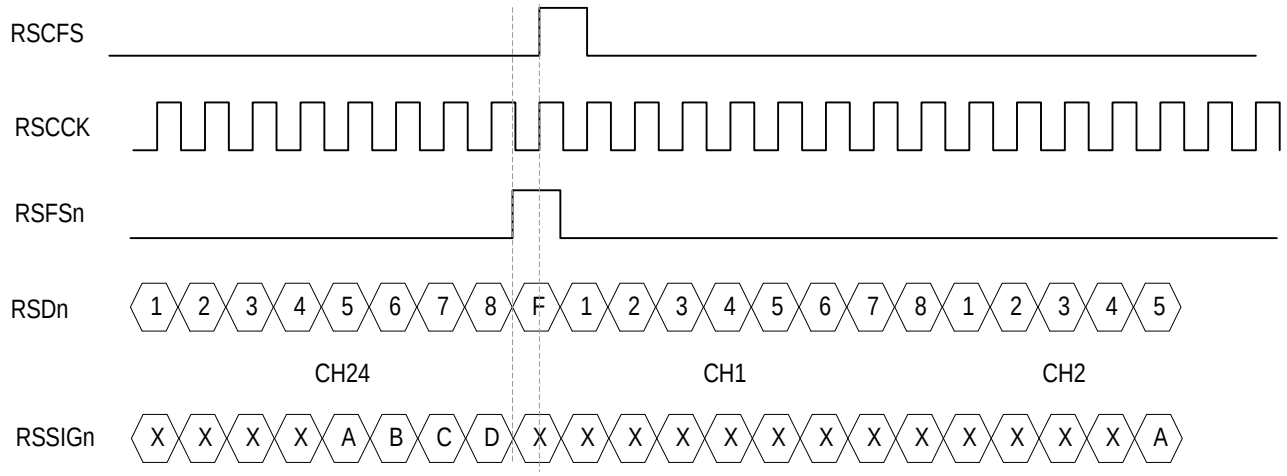
Note:
The RSCFSFALL (b1, T1/J1-003H) of the eight framers should be set to the same value to ensure RSCFS for the eight framers is sampled on the same active edge.
It is a special case when the CMS (b4, T1/J1-078H) is logic 1 and the RSCFSFALL (b1, T1/J1-003H) is not equal to RSCCKRISE (b0, T1/J1-003H). The RSD_RSCFS_EDGE (b5, T1/J1-078H) is invalid and the signals on the RSDn, RSSIGn and the RSFSn pins are updated on the first active edge of RSCCK.

Figure 28 to Figure 30 show the functional timing examples. Bit 1 of each channel is the first bit to be output.

Besides all the common functions described in the Receive Clock Slave mode, the special feature in this mode is that the multi-functional pin RSCKn/RSSIGn is used as RSSIGn to output the extracted signaling bits. The extracted signaling bits are channel aligned with the data on the RSDn pin (refer to Figure 8).

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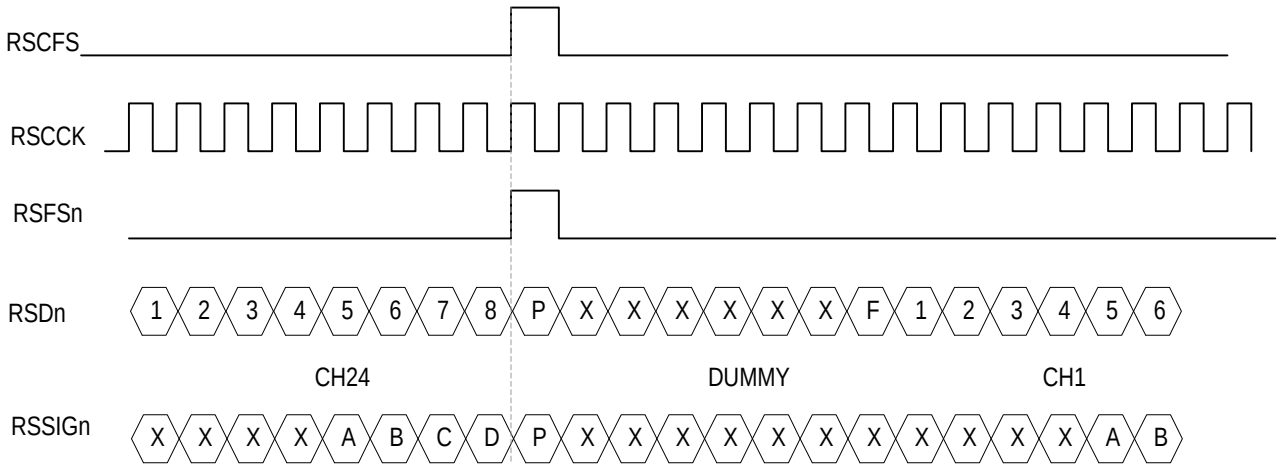
The CMS (b4, T1/J1-078H) is logic 0 and the bankplane clock rate is 1.544Mbit/s.
The RSCFSFALL (b1, T1/J1-003H) is logic 1 and the RSCCKRISE (b0, T1/J1-003H) is logic 0.
The channel offset and the bit offset enable are both 0:



(The 'X' represent the filled bits and has no meaning.)

Figure 28. T1/J1 Receive Clock Slave External Signaling Mode - Functional Timing Example 1

The CMS (b4, T1/J1-078H) is logic 0 and the bankplane clock rate is 2.048Mbit/s.
The RSCFSFALL (b1, T1/J1-003H) is logic 1 and the RSCCKRISE (b0, T1/J1-003H) is logic 1.
The channel offset and the bit offset enable are both 0:



(The 'X' represents the filled bits and has no meaning.)

Figure 29. T1/J1 Receive Clock Slave External Signaling Mode - Functional Timing Example 2

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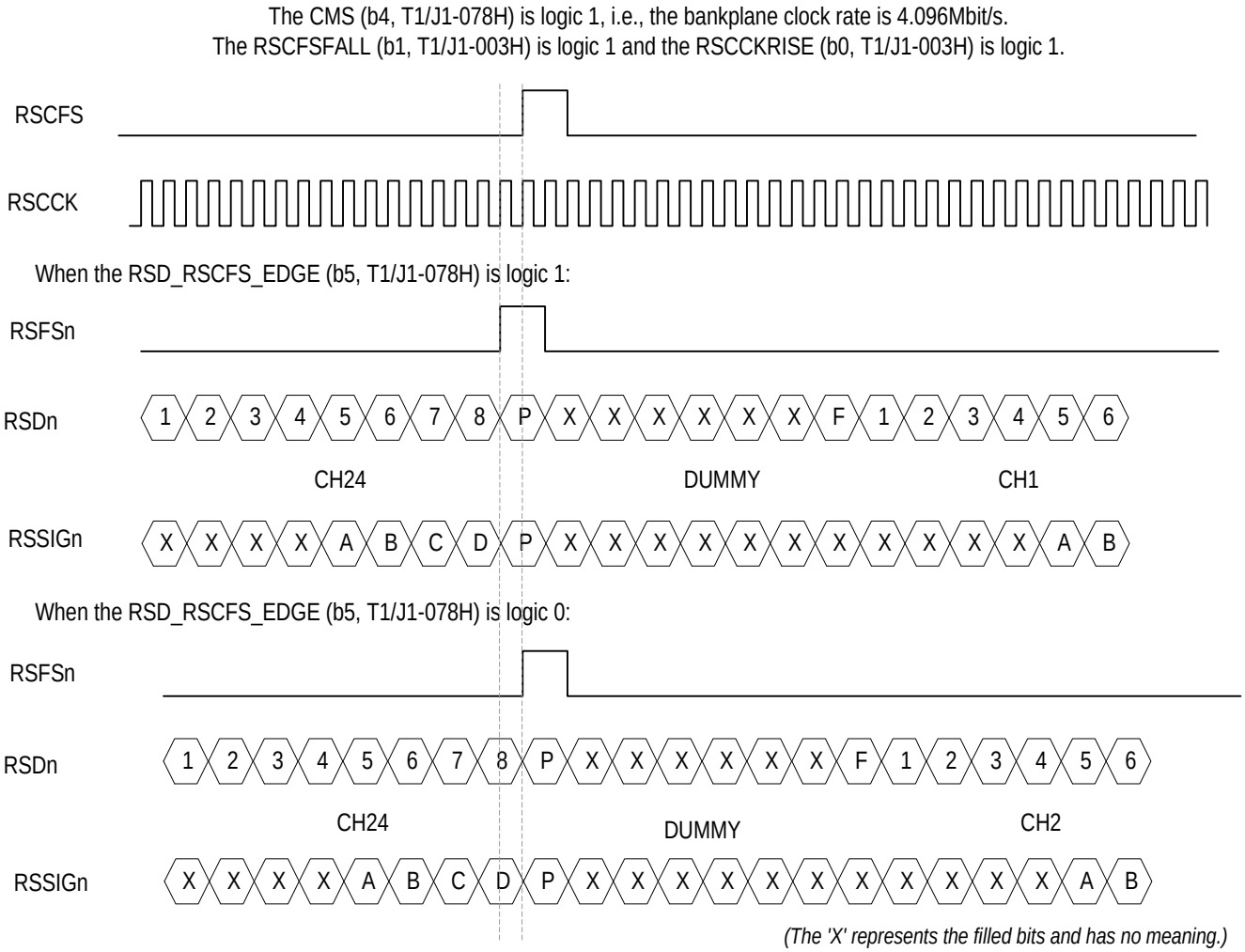


Figure 30. T1/J1 Receive Clock Slave External Signaling Mode - Functional Timing Example 3

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3.11.2.2 Receive Clock Master Mode

In the Receive Clock Master mode, each framer uses its own clock signal on the RSCKn pin and framing signal on the RSFSn pin to output the data on each RSDn pin.

In the Receive Clock Master Mode, the bit rate on the RSDn pin is 1.544Mb/s.

In the Receive Clock Master Mode, RSFSn can indicate each F-bit of SF/ESF, every second F-bit, the first F-bit of every 12 frames (in SF format) or every 24 frames (in ESF format). All the indications are selected by the RSFSP (b2, T1/J1-001H) and ALTIFP (b1, T1/J1-001H). The valid polarity of RSFSn is configured by the FPINV (b6, T1/J1-078H).

In the Receive Clock Master Mode, the data on the system interface is clocked by RSCKn. The active edge of RSCKn to update the data on RSDn and RSFSn is determined by the RSCKRISE(b3, T1/J1-003H).

The Receive Clock Master Mode includes two sub-modes: Receive Clock Master Full T1/J1 Mode and Receive Clock Master Fractional T1/J1 Mode.

3.11.2.2.1 Receive Clock Master Full T1/J1 Mode

Besides all the common functions described in the Receive Clock Master mode, the special feature in this mode (refer to Figure 15) is that RSCKn is a standard 1.544MHz clock, and the data in all 24 channels in a standard T1/J1 frame is clocked out by RSCKn.

Figure 31 shows the functional timing examples. Bit 1 of each channel is the first bit to be output.

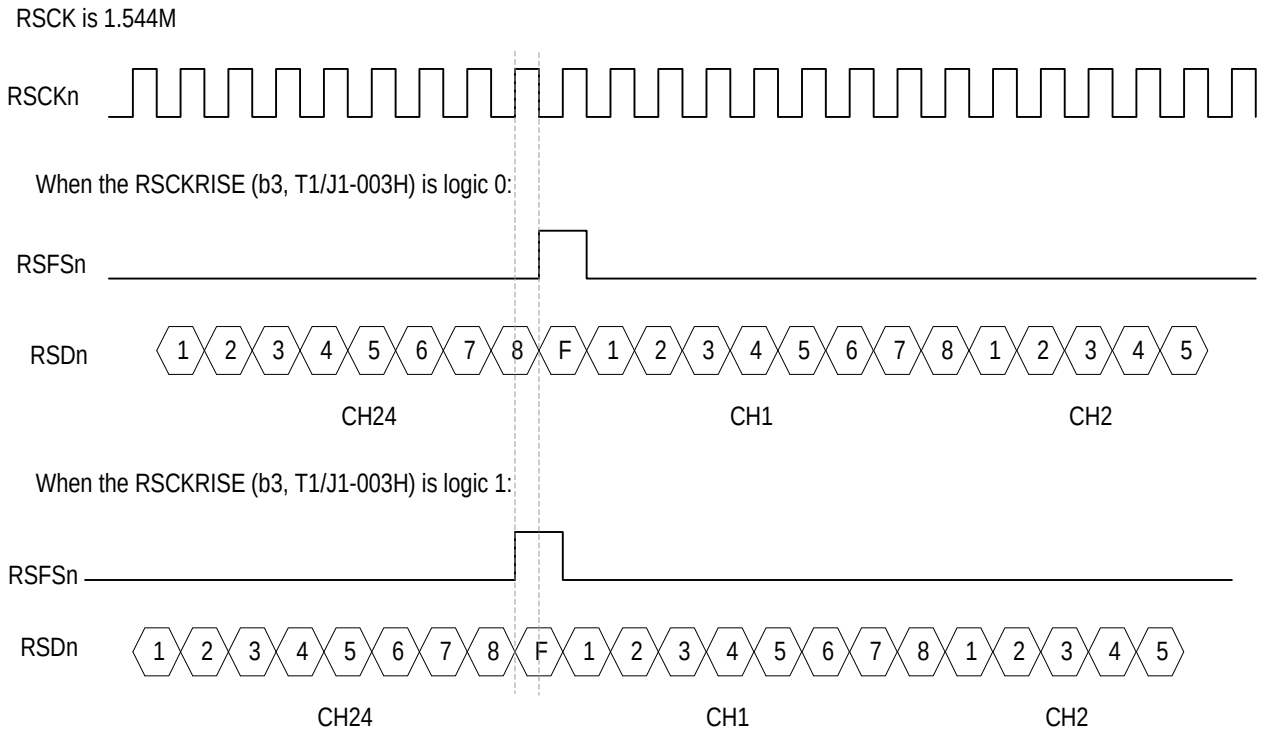


Figure 31. T1/J1 Receive Clock Master Full T1/J1 Mode - Functional Timing Example

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3.11.2.2.2 Receive Clock Master Fractional T1/J1 Mode

Besides all the common functions described in the Receive Clock Master mode, the special feature in this mode (refer to Figure 17) is that RSCKn is a gapped 1.544MHz clock (no clock signal during the selected channel).

RSCKn is gapped during those channels with their EXTRACT (b2, T1/J1-RPLC-indirect registers - 01~18H) in Receive Payload Control are logic 0, and clocks out during those channels with their EXTRACT (b2, T1/J1-RPLC-indirect registers - 01~18H) are logic 1. The data in the corresponding gapped channel is a don't care condition.

Figure 32 shows the functional timing examples. Bit 1 of each channel is the first bit to be output.

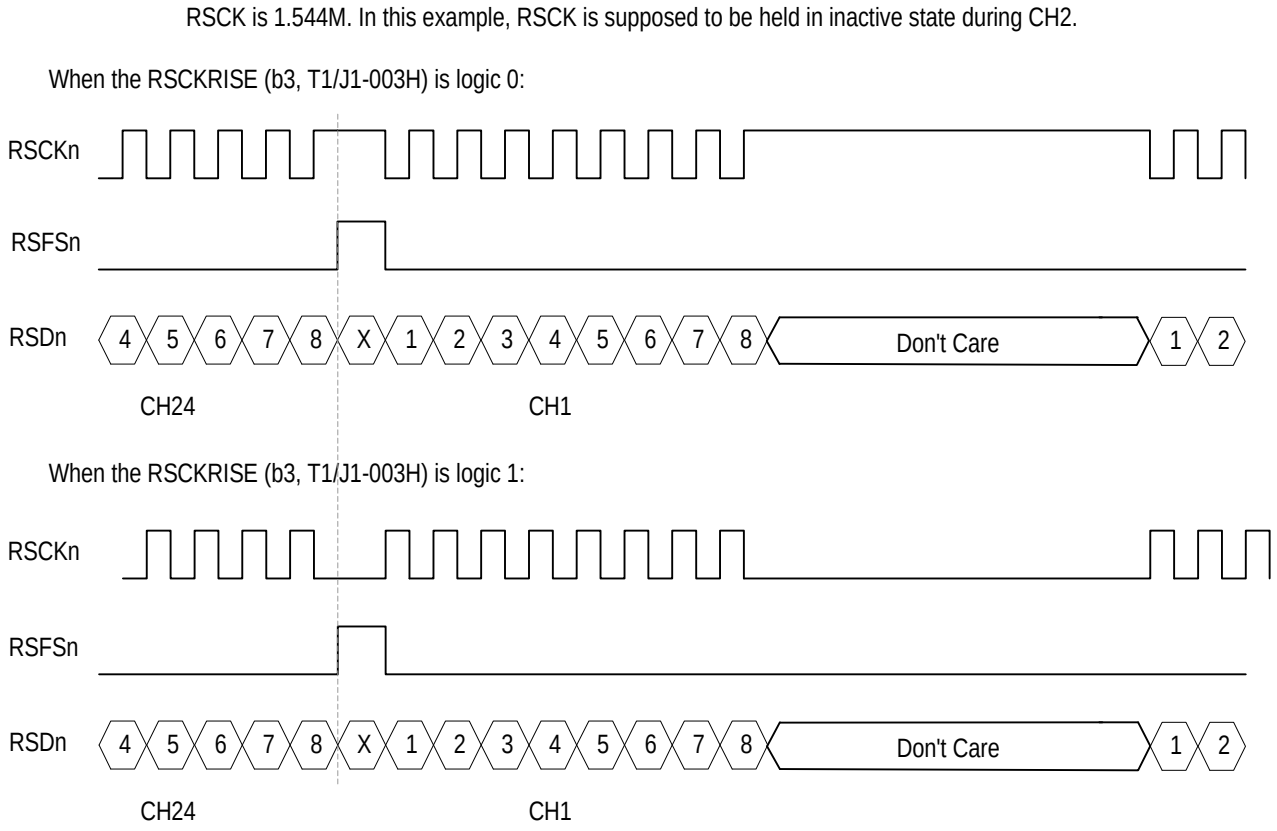


Figure 32. T1/J1 Receive Clock Master Fractional T1/J1 Mode - Functional Timing Example

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3.11.2.3 Receive Multiplexed Mode

In this mode (refer to Figure 19), two multiplexed buses are used to receive the data from all eight framers. The data from up to four framers is byte-interleaved output on one of the two multiplexed buses. The multiplexed bus is chosen by the MRBS (b7, T1/J1-003H). When the data from four framers is output on one multiplexed bus, the sequence of data is arranged by setting the channel offset TSOFF[6:0] (b6~0, T1/J1-077H). The data from different framers on one multiplexed bus must be shifted at a different channel offset to avoid data mixing. Then the received data of each framer can be controlled by the MRBC (b6, T1/J1-003H) to output to the selected multiplexed bus or not. The MRBC (b6, T1/J1-003H) of the framers that are output to the same multiplexed bus must be set to the same value.

In the Receive Multiplexed mode, the data on the system interface is clocked by MRSCCK. The active edge of MRSCCK to sample the pulse on MRSCFS and to update the data on MRSD, MRSFS and MRSSIG is determined by the following bits in the registers (refer to Table 24).

Table 24: Active Edge Selection of MRSCCK (in T1/J1 Receive Multiplexed Mode)

	the Bit Determining the Active Edge of MRSCCK
MRSCFS	RSCFSFALL (b1, T1/J1-003H)
MRSFS	RSCCKRISE (b0, T1/J1-003H)
MRSD	
MRSSIG	

Note:
When the RSCFSFALL/RSCCKRISE of any of the eight framers is configured as logic 1, all the others are taken as logic 1. That is, the RSCFSFALL/RSCCKRISE should be configured to the same value in Receive Multiplexed mode.
It is a special case when the CMS (b4, T1/J1-078H) is logic 1 and the RSCFSFALL (b1, T1/J1-003H) is not equal to RSCCKRISE (b0, T1/J1-003H). The RSD_RSCFS_EDGE (b5, T1/J1-078H) is invalid and the signals on the MRSD, MRSSIG and the MRSFS pins are updated on the first active edge of RSCCK.

In the Receive Multiplexed mode, the Multiplexed Receive Side System Common Clock (MRSCCK) is provided by the system side. It is used as a common timing clock for all eight framers. The frequency of MRSCCK can be chosen by the CMS (b4, T1/J1-078H) to be the same as the bit rate of the received data stream (8.192Mb/s), or double the bit rate of the received data stream (16.384 Mb/s). If the frequency of RSCCK is double the bit rate of the received data stream, there will be two active edges in one bit duration. In this case, the RSD_RSCFS_EDGE (b5, T1/J1-078H) determines the active edge to update the signal on the MRSD, MRSSIG and MRSFS pins; however, the pulse on MRSCFS is always sampled on its first active edge. If the CMS (b4, T1/J1-078H) or the RSD_RSCFS_EDGE (b5, T1/J1-078H) of any of the eight framers is configured as logic 1, all the others are taken as logic 1. That is, the CMS (b4, T1/J1-078H) and the RSD_RSCFS_EDGE (b5, T1/J1-078H) of the eight framers should be configured to the same value in the Receive Multiplexed mode.

In the Receive Multiplexed mode, the Multiplexed Receive Side System Common Frame Pulse (MRSCFS) is used as a common framing signal to align the data streams on the two multiplexed buses. MRSCFS is asserted on the F-bit. The valid polarity of MRSCFS is configured by the FPINV (b6, T1/J1-078H). The FPINV (b6, T1/J1-078H) of the eight framers should be set to the same value.

In the Receive Multiplexed mode, the bit rate on the MRSD pin is 8.192Mb/s.

In the Receive Multiplexed mode, regardless of the setting in the RSFSP (b2, T1/J1-001H) and ALTIFP (b1, T1/J1-001H), MRSFS can only indicate each F-bit of SF/ESF of the selected first framer. The valid polarity of RSFSn is configured by the FPINV (b6, T1/J1-078H). The FPINV (b6, T1/J1-078H) of the eight framers should be set to the same value.

In the Receive Multiplexed mode, MRSSIG outputs extracted signaling. The extracted signaling bits are channel aligned with the data output on MRSD.

Figure 33 & Figure 34 show the functional timing examples. Bit 1 of each channel is the first bit to be output.

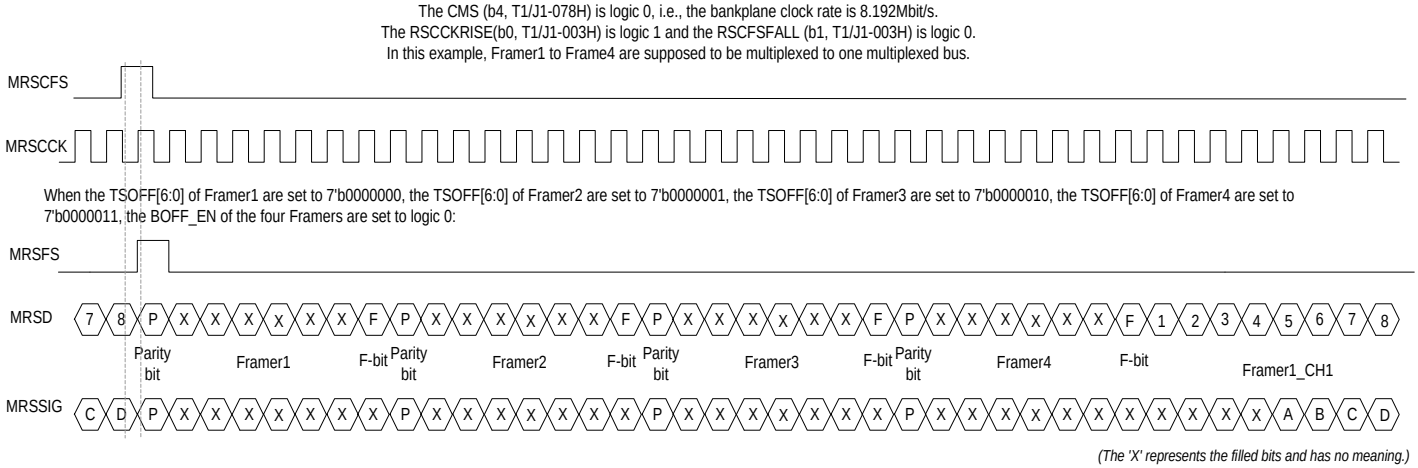


Figure 33. T1/J1 Receive Multiplexed Mode - Functional Timing Example 1

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Figure 34. T1/J1 Receive Multiplexed Mode - Functional Timing Example 2

3.11.2.4 Parity Check

In all the above modes except for the Receive Clock Slave Fractional T1/J1 mode, if the RPRTYE (b0, T1/J1-002H) is logic 1, parity check will be conducted over the bits in the previous frame and the result is inserted into the F-bit on the RSDn/MRSD and RSSIGn/MRSSIG pins. The even parity or odd parity is chosen by the RPTYP (b1, T1/J1-002H) and whether the F-bit is calculated or not is determined by the PTY_EXTD (b3, T1/J1-002H).

3.11.2.5 Offset

When the system clock rate is 2.048MHz (in Receive Clock Slave T1/J1 mode E1 rate mode) or 8.192MHz (in Receive Multiplexed mode), channel offset and/or bit offset between RSCFS and the start of the corresponding frame on RSDn/MRSD (and RSSIGn/MRSSIG) can be configured. Bit offset is disabled when the CMS (b4, T1/J1-078H) is logic 1.

The channel offset is configured in the TSOFF[6:0] (b6~0, T1/J1-077H). The TSOFF[6:0] (b6~0, E1-013H) give a binary representation.

Enabled by the BOFF_EN (b3, T1/J1-078H), the bit offset is configured in the BOFF[2:0] (b2~0, T1/J1-078H). The bit offset follows the Concentration Highway Interface (CHI) specification (refer to Table 25). The CET (clock edge transmit) is counted from the active edge of RSCFS/MRSCFS (refer to the example in Figure 34). The pulse on RSFSn/MRSFS and the signal on RSSIGn/MRSSIG (if it exists) are aligned to RSDn/MRSD.

Table 25: Receive System Interface Bit Offset

RSCFSFALL (b1, T1/J1-003)	RSCCKRISE (b0, T1/J1-003H)	BOFF[2:0] (b2~0, T1/J1-078H)								
		000	001	010	011	100	101	110	111	
1	0	2	4	6	8	10	12	14	16	CET
1	1	1	3	5	7	9	11	13	15	
0	0	1	3	5	7	9	11	13	15	
0	1	2	4	6	8	10	12	14	16	

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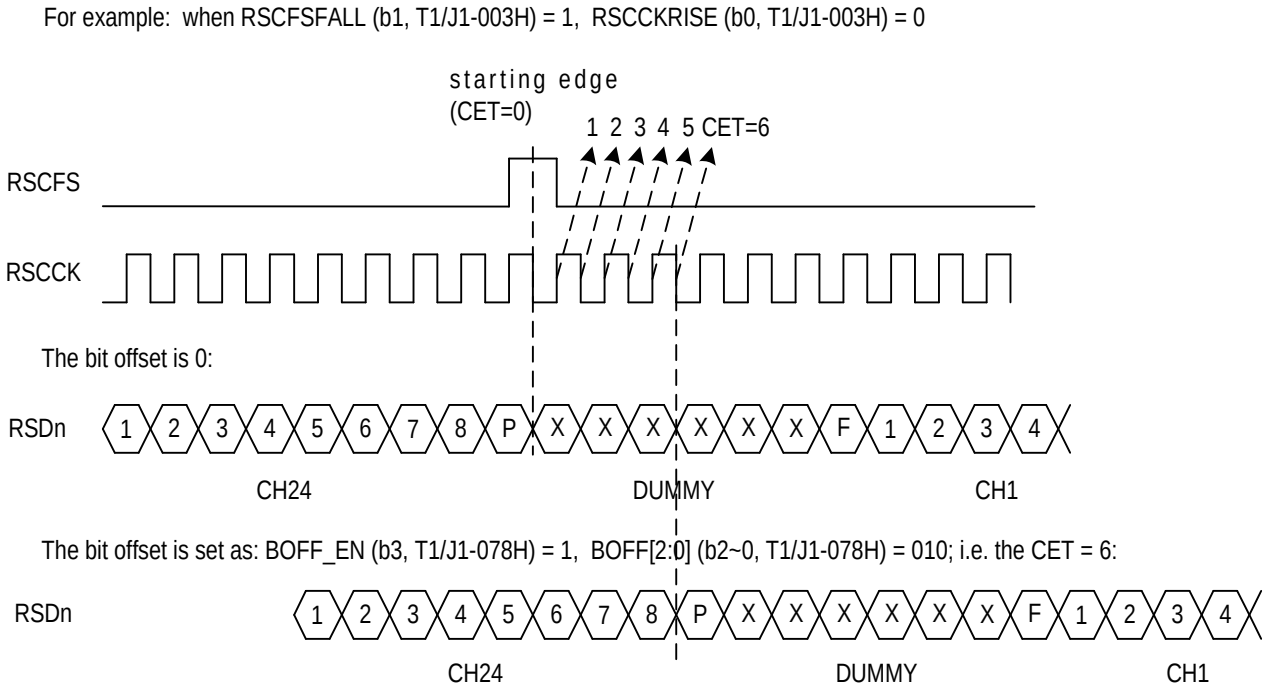


Figure 35. Receive Bit Offset in T1/J1 Mode

3.11.2.6 Output On RSDn/MRSD & RSSIGn/MRSSIG

In all the five modes, the RSDn/MRSD and the RSSIGn/MRSSIG pins can be configured by the TRI[1:0] (b5~4, T1/J1-003H) of the corresponding framer to be in high impedance state or to output the processed data stream. However, in the Receive Multiplexed Mode, the TRI[1:0] (b~4, T1/J1-003H) of the framers that are output to the same multiplexed bus must be set to the same value.

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3.12 PRBS GENERATOR / DETECTOR (PRGD)

The PRBS Generator/Detector is shared by eight framers. It can be assigned to any of the 8 framers at one time. The PRGD, together with the Receive / Transmit Payload Control blocks, is used to test the data stream.

3.12.1 E1 MODE

The PRBS Generator/Detector is a global control block. Any one of the eight framers can be linked to the pattern generator or detector by the PRGDSEL[2:0] (b7~5, E1-00CH). The pattern can be inserted in either the transmit or receive direction, and detected in the opposite direction. The direction is determined by the RXPATGEN (b2, E1-00CH). The pattern can be generated and detected in unframed or framed mode. The selection is made by the UNF_GEN (b1, E1-00CH) and UNF_DET (b0, E1-00CH) respectively. In unframed mode, all 32 time slots are replaced or extracted and the specification in the TEST (b7, E1-RPLC-indirect registers - 20~3FH or b3, E1-TPLC-indirect registers - 20~3FH) in Receive / Transmit Payload Control blocks is ignored. In framed mode, the time slot is specified by the TEST (b7, E1-RPLC-indirect registers - 20~3FH or b3, E1-TPLC-indirect registers - 20~3FH).

3.12.1.1 Pattern Generator

The repetitive or pseudo-random pattern chosen by the PS (b4, E1-070H) is located in the PI[31:0] (b7~0, E1-078H & b7~0, E1-079H & b7~0, E1-07AH & b7~0, E1-07BH). However, the length of the valid data in the PI[31:0] is determined by the PL[4:0] (b4~0, E1-072H). If the repetitive pattern is chosen, the valid PI[X:0] ('X' is equal to one number of the 31 to 1) reflect its content directly. If the pseudo-random pattern is chosen, the valid PI[X:0] are its initial value and the feedback tap position (refer to Figure 36) is determined by the PT[4:0] (b4~0, E1-073H). A single bit error will be inserted by setting the EVENT (b3, E1-074H) to '1', or continuous bit errors will be inserted at a bit error rate determined by the EIR[2:0] (b2~0, E1-074H). Before replacing the data in the assigned direction, the pattern can be inverted by setting the TINV (b3, E1-070H).

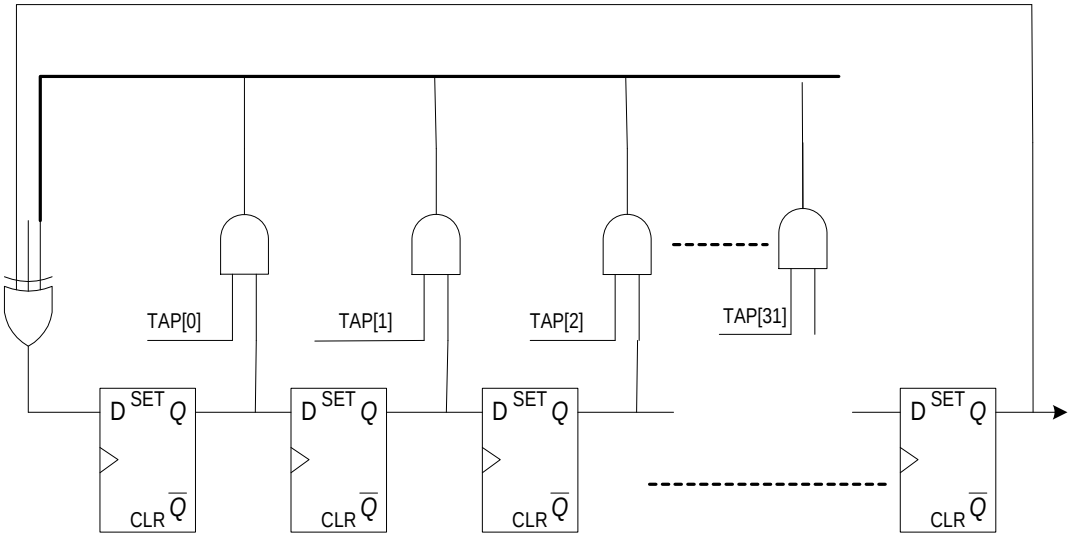


Figure 36. PRBS Pattern Generator

3.12.1.2 Pattern Detector

The extracted data from the assigned direction is compared with a repetitive or pseudo-random pattern, as chosen by the PS (b4, E1-070H). Before being compared, the data can be inverted by setting the RINV (b2, E1-070H). The extracted data is then compared with a 48-bit fixed window loaded with the pattern. This process goes on until the data coincides with the pattern. When they are synchronized, it is indicated by the SYNCV (b4, E1-071H). Bit errors in the synchronized data stream are indicated in the BEI (b2, E1-071H). When there are more than 10-bit errors in the fixed 48-bit window, the extracted data is out of synchronization. Automatic search for the re-synch will be done with the AUTOSYNC (b1, E1-070H) configured, or manual search will be done when there is a transition from low to high on the MANSYNC (b0, E1-070H). A manual search is recommended to execute to ensure the PRGD operates correctly when there is any setting change of the PRGD registers or the detector data source changes.

Selected by the PDR[1:0] (b7~6, E1-070H), the PD[31:0] (b7~0, E1-07CH & b7~0, E1-07DH & b7~0, E1-07EH & b7~0, E1-07FH) can contain the received pattern, the total error count or the total number of received bits. They update when the defined intervals are initiated. The intervals equal 1 second when the AUTOUPDATE (b0, E1-000H) is set in the corresponding framer. They can also be updated by writing to any of the PD[31:0] (b7~0, E1-07CH & b7~0, E1-07DH & b7~0, E1-07EH & b7~0, E1-07FH), or to the E1 Chip ID / Global PMON Update register (E1-009H). The update will be indicated by the XFERI (b1, E1-071H). If they are not read in the defined intervals, the PD[31:0] (b7~0, E1-07CH & b7~0, E1-07DH & b7~0, E1-07EH & b7~0, E1-07FH) will be overwritten with new data. The overwritten condition is indicated by the OVR (b0, E1-071H).

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3 kinds of interrupts can be generated by this block:

- bit errors;
- synchronization status change (indicated in the SYNCI [b3, E1-071H]);
- the PD[31:0] (b7~0, E1-07CH & b7~0, E1-07DH & b7~0, E1-07EH & b7~0, E1-07FH) are updated.

When the interrupts are enabled by the BEE (b6, E1-071H), SYNCE (b7, E1-071H) and XFERE (b5, E1-071H) respectively, the $\overline{INT}$ pin is asserted.

3.12.2 T1/J1 MODE

The PRBS Generator/Detector is a global control block. Any one of the eight framers can be linked to pattern generator or detector by the PRGDSEL[2:0] (b7~5, T1/J1-00FH). The pattern can be inserted in either the transmit or receive direction, and detected in the opposite direction. The direction is determined by the RXPATGEN (b2, T1/J1-00FH). The pattern can be generated and detected in unframed or framed mode. The selection is made by the UNF_GEN (b1, T1/J1-00FH) and UNF_DET (b0, T1/J1-00FH) respectively. In unframed mode, all 24 channels are replaced or extracted and the specification in the TEST (b3, T1/J1-RPLC-indirect registers - 01~18H or b3, T1/J1-TPLC-indirect registers - 01~18H) in Receive / Transmit Payload Control blocks is ignored. In framed mode, the channel is specified by the TEST (b3, T1/J1-RPLC-indirect registers - 01~18H or b3, T1/J1-TPLC-indirect registers - 01~18H). However, fractional T1/J1 signal will be replaced or extracted in the specified channel when the Nx56k_GEN (b4, T1/J1-00FH) or Nx56k_DET (b3, T1/J1-00FH) is set respectively.

3.12.2.1 Pattern Generator

The repetitive or pseudo-random pattern chosen by the PS (b4, T1/J1-060H) is located in the PI[31:0] (b7~0, T1/J1-068H & b7~0, T1/J1-069H & b7~0, T1/J1-06AH & b7~0, T1/J1-06BH). However, the length of the valid data in the PI[31:0] is determined by the PL[4:0] (b4~0, T1/J1-062H). If the repetitive pattern is chosen, the valid PI[X:0] ('X' is valid for 1 to 31) reflect its content directly. If the pseudo-random pattern is chosen, the valid PI[X:0] are its initial value and the feedback tap position (refer to Figure 36) is determined by the PT[4:0] (b4~0, T1/J1-063H). A single bit error will be inserted by setting the EVENT (b3, T1/J1-064H), or continuous bit errors will be inserted at a bit error rate determined by the EIR[2:0] (b2~0, T1/J1-064H). Before replacing the data in the assigned direction, the pattern can be inverted by setting the TINV (b3, T1/J1-060H).

3.12.2.2 Pattern Detector

The extracted data from the assigned direction is compared with a repetitive or pseudo-random pattern, as chosen by the PS (b4, T1/J1-060H). Before being compared, the data can be inverted by setting the RINV (b2, T1/J1-060H). The extracted data is then compared with a 48-bit fixed window loaded with the pattern. This process continues until the data coincides with the pattern. They are then synchronized with an indication in the SYNCV (b4, T1/J1-061H). Bit errors in the synchronized data are indicated in the BEI (b2, T1/J1-061H). When there are more than 10-bit errors in the fixed 48-bit window, the extracted data is out of synchronization. Automatic search for the re-synch will be done with the AUTOSYNC (b1, T1/J1-060H) configured, or manual search will be done when there is a transition from low to high on the MANSYNC (b0, T1/J1-060H). A manual search is recommended to execute to ensure the PRGD operates correctly when there is any setting change of the PRGD registers or the detector data source changes.

Selected by the PDR[1:0] (b7~6, T1/J1-060H), the PD[31:0] (b7~0, T1/J1-06CH & b7~0, T1/J1-06DH & b7~0, T1/J1-06EH & b7~0, T1/J1-06FH) can contain the received pattern, the total error count or the total number of received bits. They update when the defined intervals are initiated. The intervals equal 1 second when the AUTOUPDATE (b0, T1/J1-000H) is set in the corresponding framer. They can also be updated by writing to any of the PD[31:0] (b7~0, T1/J1-06CH & b7~0, T1/J1-06DH & b7~0, T1/J1-06EH & b7~0, T1/J1-06FH), or to the T1/J1 Chip ID / Global PMON Update register (T1/J1-00CH). The update will be indicated by the XFERI (b1, T1/J1-061H). If they are not read in the defined intervals, the PD[31:0] (b7~0, T1/J1-06CH & b7~0, T1/J1-06DH & b7~0, T1/J1-06EH & b7~0, T1/J1-06FH) will be overwritten with new data. The overwritten condition is indicated by the OVR (b0, T1/J1-061H).

3 kinds of interrupts can be generated by this block:

- bit errors;
- synchronization status change (indicated in the SYNCI [b3, T1/J1-061H]);
- the PD[31:0] (b7~0, T1/J1-06CH & b7~0, T1/J1-06DH & b7~0, T1/J1-06EH & b7~0, T1/J1-06FH) are updated.

When the interrupts are enabled by the BEE (b6, T1/J1-061H) SYNCE (b7, T1/J1-061H) and XFERE (b5, T1/J1-061H) respectively, the $\overline{INT}$ pin is asserted.

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3.13 TRANSMIT SYSTEM INTERFACE (TRSI)

The Transmit System Interface determines how to input the data to the chip. The input data to the eight framers can be aligned with each other or inputted independently. The timing clocks and framing pulses can be provided by the system back-plane common to eight framers or provided for eight framers individually. The Transmit System Interface supports various configurations to meet various requirements in different applications.

3.13.1 E1 MODE

In E1 mode, the Transmit System Interface can be set in Non-multiplexed Mode or Multiplexed Mode. In the Non-multiplexed Mode, the TSDn pin is used to input the data to each framer at a bit rate of 2.048 Mb/s. While in the Multiplexed Mode, the data input to the eight framers is byte-interleaved from two high speed data streams and inputs on the MTSD1 and MTSD2 pins at a bit rate of 8.192 Mb/s.

In the Non-multiplexed Mode, if the timing signal for clocking data on the TSDn pin is provided by the system side and shared by all eight framers, the Transmit System Interface should be set in Transmit Clock Slave mode. If the timing signal for clocking data on each TSDn pin is provided from each line side (processed timing signal), the Transmit System Interface should be set in Transmit Clock Master mode.

In the Non-multiplexed Mode, if there is a common framing pulse provided by the system side for the eight framers, the Transmit System Interface should be set in Transmit Clock Slave mode. If there is no common framing pulse, the Transmit System Interface should be set in Transmit Clock Master mode.

In the Transmit Clock Slave mode, if the multi-function pin TSFSn/TSSIGn is used to output the framing indication pulse, the Transmit System Interface is in Transmit Clock Slave TSFS Enable mode. If TSFSn/TSSIGn is used to input the signaling bits to be inserted, the Transmit System Interface is in Transmit Clock Slave External Signaling mode.

In the Transmit Clock Master mode, the multi-function pin TSFSn/TSSIGn is used as TSFSn to input the framing indication pulse.

Table 26 summarizes the transmit system interface in different operation modes. To set the transmit system interface of each framer into various operation modes, the registers must be configured as Table 27.

Table 26: E1 Mode Transmit System Interface in Different Operation Modes

Operation Mode			Data Pin	Clock Pin	Framing Pin	Signaling Pin	Reference Clock Pin
Non-Multiplexed Mode	Clock Slave Mode	TSFS Enable	TSDn	TSCCKB	TSCFS & TSFSn	No	TSCCKA
		External Signaling	TSDn	TSCCKB	TSCFS	TSSIGn	TSCCKA
	Clock Master Mode		TSDn	LTCKn	TSFSn	No	TSCCKA & TSCCKB
Multiplexed Mode			MTSD	MTSCCKB	MTSCFS	MTSSIG	TSCCKA

Table 27: Operation Mode Selection in E1 Transmit Path

RATE[1:0] (b1~0, E1-018H)	TSCKSLV (b5, E1-018H)	TSSIG_EN (b6, E1-003H)	Operation Mode
01	1	0	Transmit Clock Slave TSFS Enable
		1	Transmit Clock Slave External Signaling
	0	-	Transmit Clock Master
11(All the eight framers should be set)	1	1	Transmit Multiplexed

3.13.1.1 Transmit Clock Slave Mode

In the Transmit Clock Slave mode, the Transmit Side System Common Clock B (TSCCKB) is provided by the system side. It is used as a common timing clock for all eight framers. The speed of TSCCKB can be chosen by the CMS (b2, E1-018H) to be the same as the data to be transmitted (2.048MHz), or twice the data (4.096MHz). The CMS (b2, E1-018H) of the eight framers should be set to the same value. If the speed of TSCCKB is twice the data to be transmitted, there will be two active edges in one bit time. In this case, the COFF (b4, E1-01CH) determines the active edge to sample the signal on the TSDn and TSSIGn pins and the active edge to update the pulse on the TSFSn pin; however, the pulse on TSCFS is always sampled on its first active edge.

In the Transmit Clock Slave mode, the Transmit Side System Common Clock A (TSCCKA) is provided by the system side. It is used as one of the reference clocks for the transmit jitter attenuator DPLL for all eight framers (refer to Chapter 3.20 Transmit Clock for details).

In the Transmit Clock Slave mode, the Transmit Side System Common Frame Pulse (TSCFS) is used as a common framing signal to align the data streams for the eight framers. TSCFS is asserted on each Basic Frame or Multi-Frame indicated by the FPTYP (b1, E1-019H). The valid polarity is configured by the FPINV (b3, E1-019H).

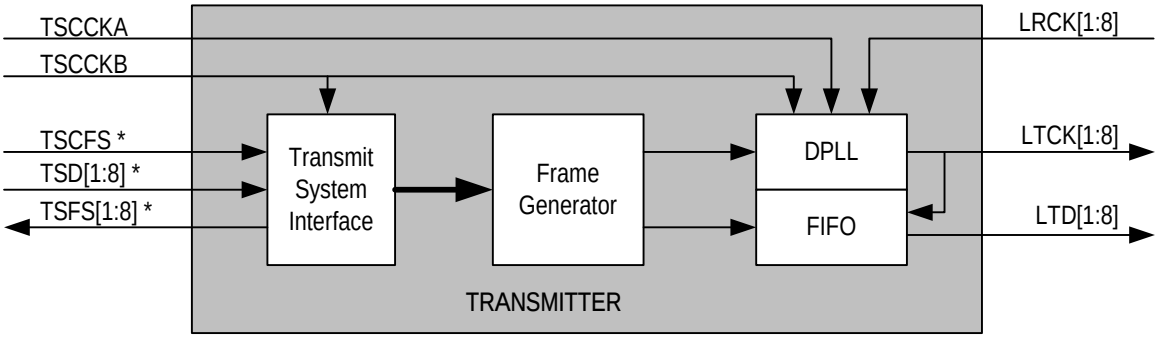
In the Transmit Clock Slave mode, the bit rate on the TSDn pin is 2.048Mb/s.

The Transmit Clock Slave Mode includes two sub-modes: Transmit Clock Slave TSFS Enable Mode and Transmit Clock Slave External Signaling Mode.

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3.13.1.1.1 Transmit Clock Slave TSFS Enable Mode

In this mode (refer to Figure 37), the data on the system interface is clocked by TSCCKB. The active edge of TSCCKB used to sample the pulse on TSCFS and the data on TSDn and TSFSn is determined by the following bits in the registers (refer to Table 28).



Note: * TSCFS, TSD, TSFS are timed to TSCCKB

Figure 37. Transmit Clock Slave TSFS Enable Mode

Table 28: Active Edge Selection of TSCCKB (in E1 Transmit Clock Slave TSFS Enable Mode)

	the Bit Determining the Active Edge of TSCCKB
TSCFS	FE (b3, E1-018H)
TSDn	DE (b4, E1-018H)
TSFSn	TSFSRISE (b2, E1-002H)

Note:
If the FE is not equal to the DE, the active edge decided by the FE is one clock edge before the active edge decided by the DE.
The FE (b3, E1-018H) of the eight framers should be set to the same value to ensure TSCFS for the eight framers is sampled on the same active edge.

Figure 38 & Figure 39 show the functional timing examples. Bit 1 of each time slot is the first bit to be transmitted.

Besides all the common functions described in the Transmit Clock Slave mode, the special feature in this mode is that the multi-functional pin TSFSn/TSSIGn is used as TSFSn to output a framing pulse to indicate the first bit of each Basic Frame.

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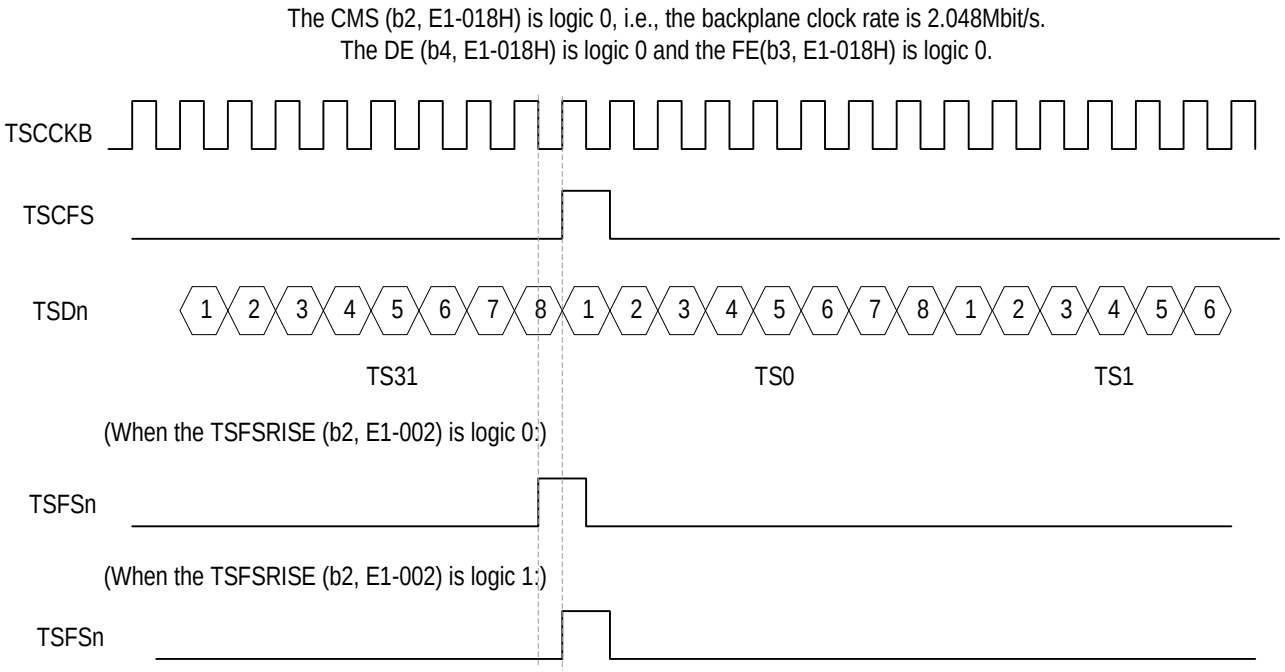


Figure 38. E1 Transmit Clock Slave TSFS Enable Mode - Functional Timing Example 1

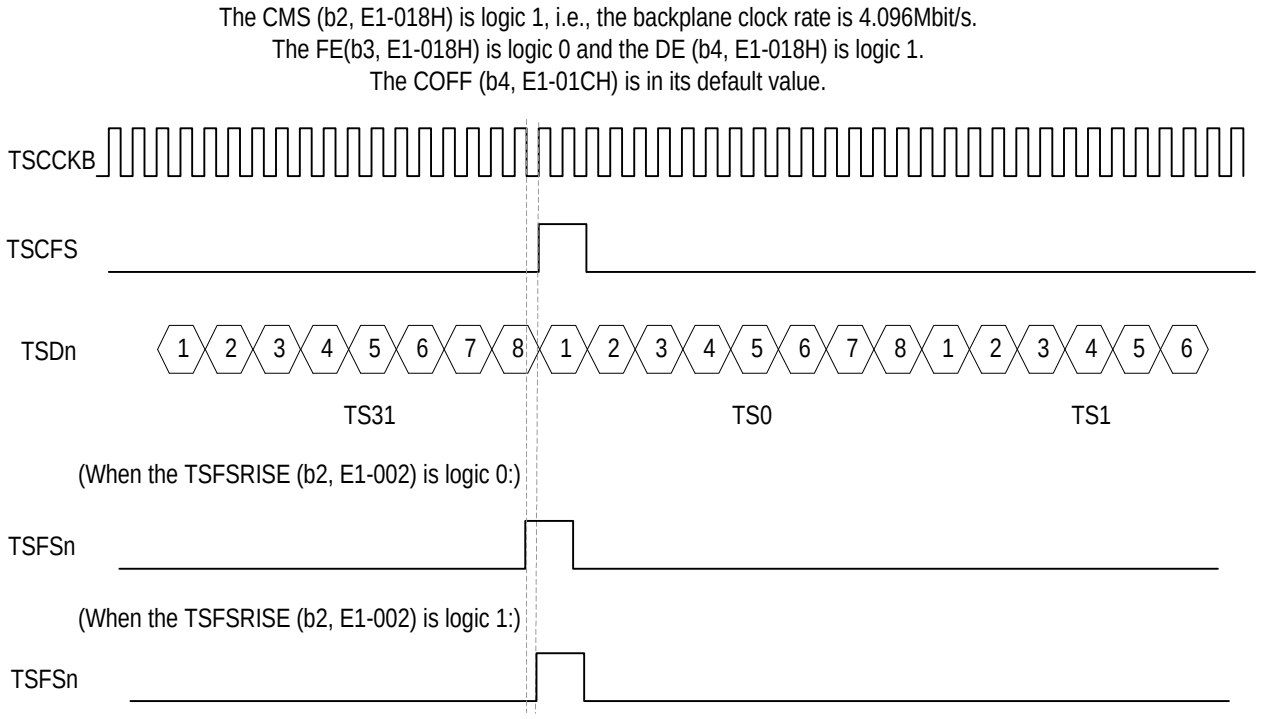
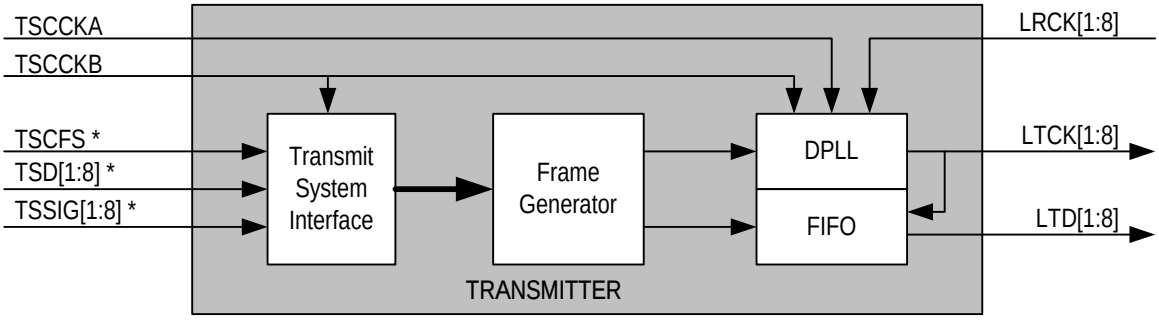


Figure 39. E1 Transmit Clock Slave TSFS Enable Mode - Functional Timing Example 2

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3.13.1.1.2 Transmit Clock Slave External Signaling Mode

In this mode (refer to Figure 40), the data on the system interface is clocked by TSCCKB. The active edge of TSCCKB used to sample the pulse on TSCFS and the data on TSDn and TSSIGn is determined by the following bits in the registers (refer to Table 29).



Note: * TSCFS, TSD, TSSIG are timed to TSCCKB

Figure 40. Transmit Clock Slave External Signaling Mode

Table 29: Active Edge Selection of TSCCKB (in E1 Transmit Clock Slave External Signaling Mode)

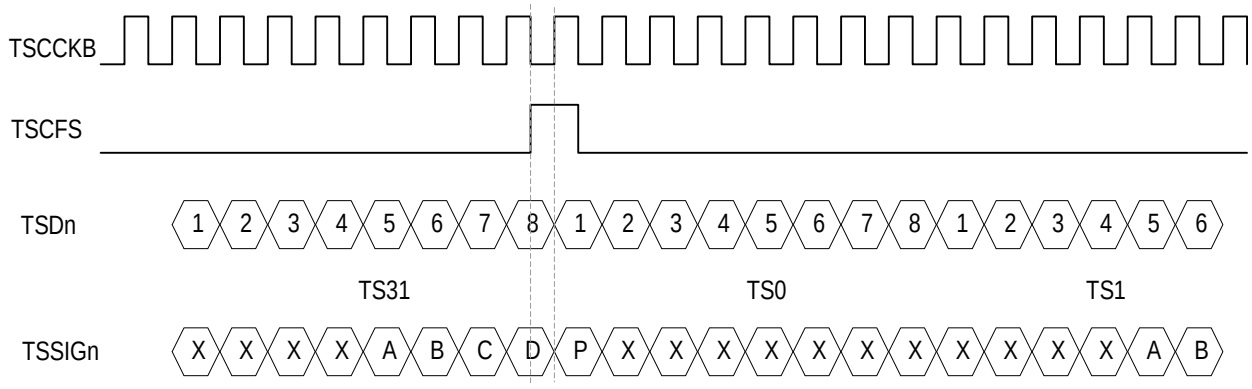
	the Bit Determining the Active Edge of TSCCKB
TSCFS	FE (b3, E1-018H)
TSDn	DE (b4, E1-018H)
TSSIGn	

Note:
If the FE is not equal to the DE, the active edge decided by the FE is one clock edge before the active edge decided by the DE.
The FE (b3, E1-018H) of the eight framers should be set to the same value to ensure TSCFS for the eight framers is sampled on the same active edge.

Figure 41 & Figure 42 show the functional timing examples. Bit 1 of each time slot is the first bit to be transmitted.

Besides all the common functions described in the Transmit Clock Slave mode, the special feature in this mode is that the multi-functional pin TSFSn/TSSIGn is used as TSSIGn to input the signaling. The signaling on the TSSIGn pin may replace the data on TS16 when the CCS is disabled and the SIGSRC (b4, E1-TPLC-indirect registers - 61~7FH) in the TPLC block is logic 0.

The CMS (b2, E1-018H) is logic 0, i.e., the bankplane clock rate is 2.048Mbit/s.
The DE (b4, E1-018H) is logic 0 and the FE(b3, E1-018H) is logic 1.

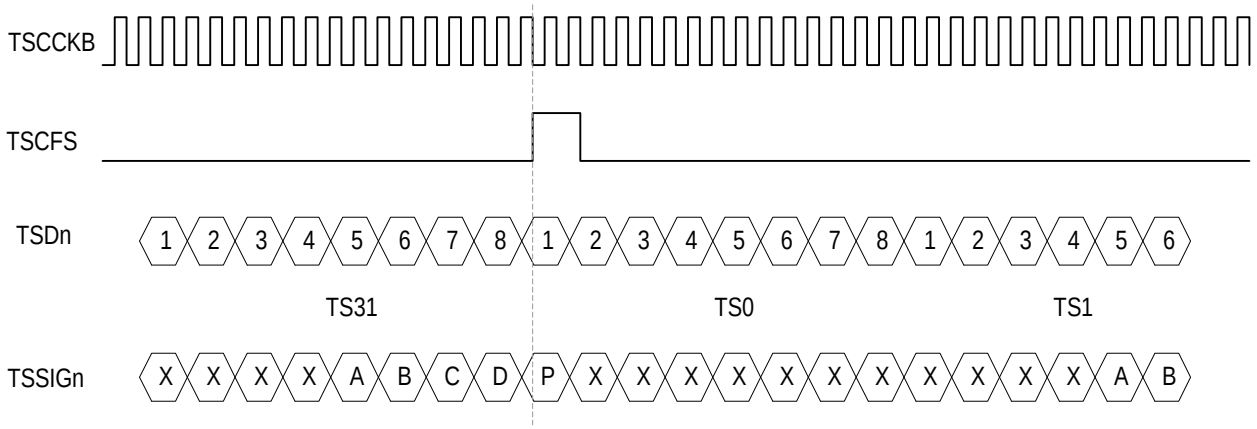


(The 'X' represent the filled bits and has no meaning.)

Figure 41. E1 Transmit Clock Slave External Signaling Mode - Functional Timing Example 1

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The CMS (b2, E1-018H) is logic 1, i.e., the bankplane clock rate is 4.096Mbit/s.
The FE(b3, E1-018H) is logic 1 and the DE (b4, E1-018H) is logic 1.
The COFF (b4, E1-01CH) is in its default value.

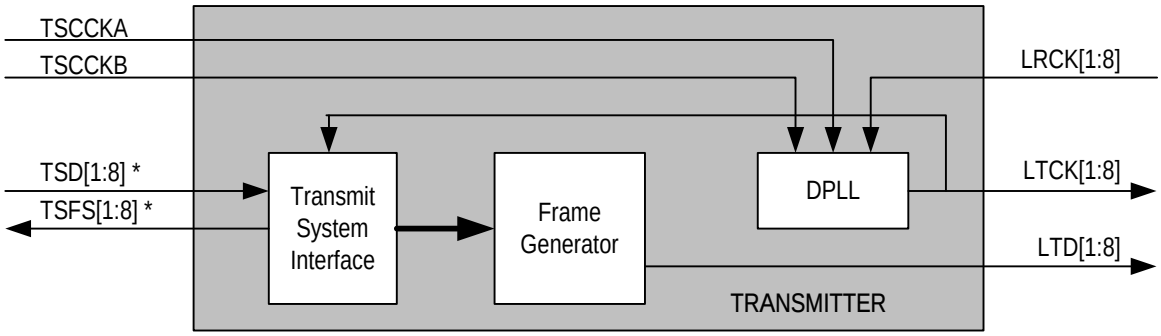


(The 'X' represent the filled bits and has no meaning.)

Figure 42. E1 Transmit Clock Slave External Signaling Mode - Functional Timing Example 2

3.13.1.2 Transmit Clock Master Mode

In the Transmit Clock Master mode (refer to Figure 43), the Transmit Side System Common Clock A (TSCCKA) and Transmit Side System Common Clock B (TSCCKB) provided by the system side are used as one of the reference clocks for the transmit jitter attenuator DPLL for all eight framers (refer to Chapter 3.20 Transmit Clock for details).



Note: * TSD, TSFS are timed to LTCK

Figure 43. Transmit Clock Master Mode

In the Transmit Clock Master mode, the multi-functional pin TSFSn/TSSIGn is used as TSFSn to output a framing pulse to indicate the first bit of each Basic Frame.

In the Transmit Clock Master mode, the bit rate on the TSDn pin is 2.048Mb/s.

In the Transmit Clock Master mode, each framer uses its own processed clock signal on the LTCKn pin to sample/update the data on the system interface. The active edge of LTCKn to sample the data on the TSDn pin is determined by the DE (b4, E1-018H). The active edge of LTCKn to update the pulse on the TSFSn pin is determined by the TSFSRISE (b2, E1-002H).

Figure - 42 shows the functional timing examples. Bit 1 of each time slot is the first bit to be transmitted.

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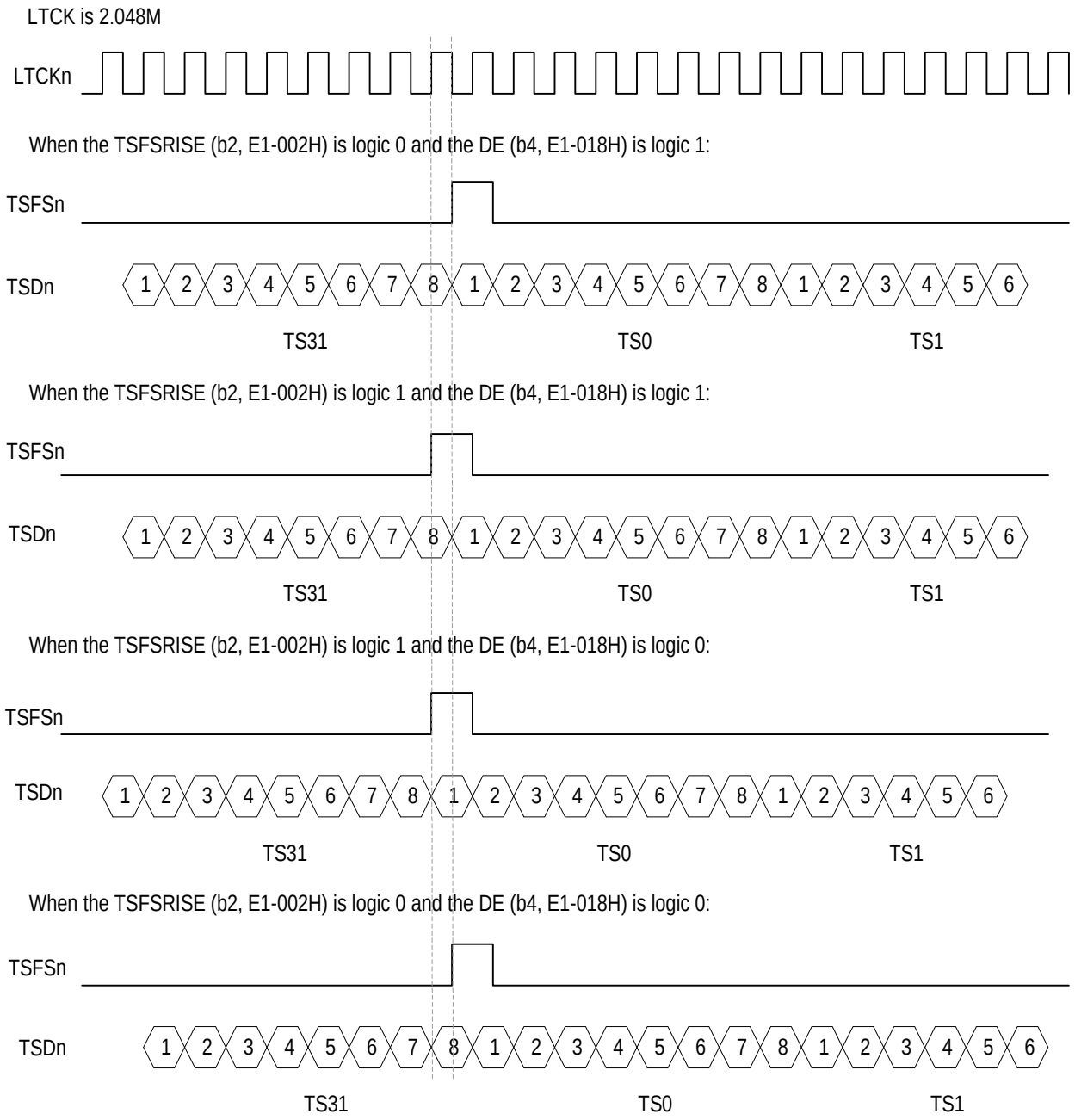
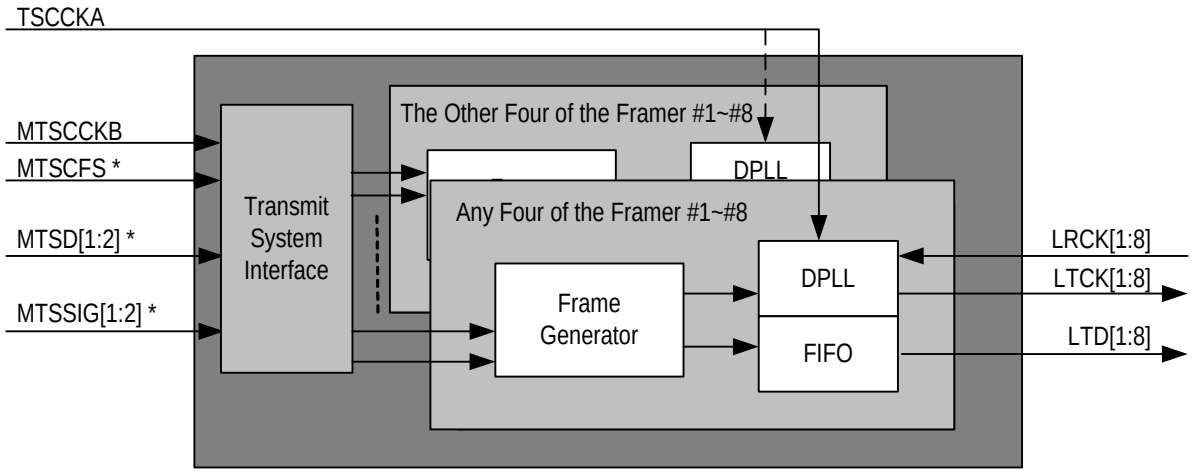


Figure 44. E1 Transmit Clock Master Mode - Functional Timing Example

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3.13.1.3 Transmit Multiplexed Mode

In this mode (refer to Figure 45), two multiplexed buses are used to input the data to all eight framers. Chosen by the MTBS (b4, E1-003H) in each framer, the data on one of the two multiplexed buses is byte-interleaved input to up to four framers. When a group of four framers is selected, the input sequence of the data on the multiplexed bus is arranged by setting the time slot offset TSOFF[6:0] (b6~0, E1-01BH). The data to different framers from one multiplexed bus must be shifted to a different time slot offset to avoid data mixing. Then the data on the multiplexed bus will be input to each of the four selected framers with a byte-interleaved manner.



Note: * MTSCFS, MTSD, MTSSIG are timed to MTSCCKB

Figure 45. Transmit Multiplexed Mode

In the Transmit Multiplexed mode, the data on the system interface is clocked by MTSCCKB. The active edge of MTSCCKB to sample the data on MTSCFS, MTSD and MTSSIG is determined by the following bits in the registers (refer to Table 30).

Table 30: Active Edge Selection of MTSCCKB (in E1 Transmit Multiplexed Mode)

	the Bit Determining the Active Edge of MTSCCKB
MTSCFS	FE (b3, E1-018H)
MTSD	DE (b4, E1-018H)
MTSSIG	
Note: If the FE is not equal to the DE, the active edge decided by the FE is one clock edge before the active edge decided by the DE. The FE and the DE of the eight framers should be set to the same value respectively.	

In the Transmit Multiplexed mode, the Multiplexed Transmit Side System Common Clock B (MTSCCKB) is provided by the system side. It is used as a common timing clock for all eight framers. The speed of MTSCCKB can be chosen by the CMS (b2, E1-018H) to be the same as the data to be transmitted (8.192MHz), or double the data (16.384MHz). If the speed of MTSCCKB is double the data to be transmitted, there will be two active edges in one bit duration. In this case, the COFF (b4, E1-01CH) determines the active edge to sample the signals on the MTSD and MTSSIG pins and the active edge to update the pulse on the MTSFS pin; however, the pulse on MTSCFS is always sampled on its first active edge. However, if the CMS (b2, E1-018H) or the COFF (b4, E1-01CH) of any of the eight framers is configured as logic 1, all the others are taken as logic 1. That is, the CMS (b2, E1-018H) and the COFF (b4, E1-01CH) of the eight framers should be configured to the same value in the Transmit Multiplexed mode.

In the Transmit Multiplexed mode, the Transmit Side System Common Clock A (TSCCKA) is provided by the system side. It is used as one of the reference clocks for the transmit jitter attenuator DPLL for all eight framers (refer to Chapter 3.20 Transmit Clock for details).

In the Transmit Multiplexed mode, the Multiplexed Transmit Side System Common Frame Pulse (MTSCFS) is used as a common framing signal to align data streams on the two multiplexed buses. MTSCFS is asserted on each Basic Frame of the selected first framer. The valid polarity of MTSCFS is configured by the FPINV (b3, E1-019H). The FPINV (b3, E1-019H) of the eight framers should be set to the same value.

In the Transmit Multiplexed mode, the bit rate on the MTSD pin is 8.192Mb/s.

In the Transmit Multiplexed mode, MTSSIG inputs the signaling bits to be inserted. The signaling bits are time slot aligned with the data input from MTSD. The signaling bits may replace the data on TS16 when the CCS is disabled and the SIGSRC (b4, E1-TPLC-indirect registers - 61~7FH) in the TPLC block is logic 0.

Figure 46 & Figure 47 show the functional timing examples. Bit 1 of each time slot is the first bit to be transmitted.

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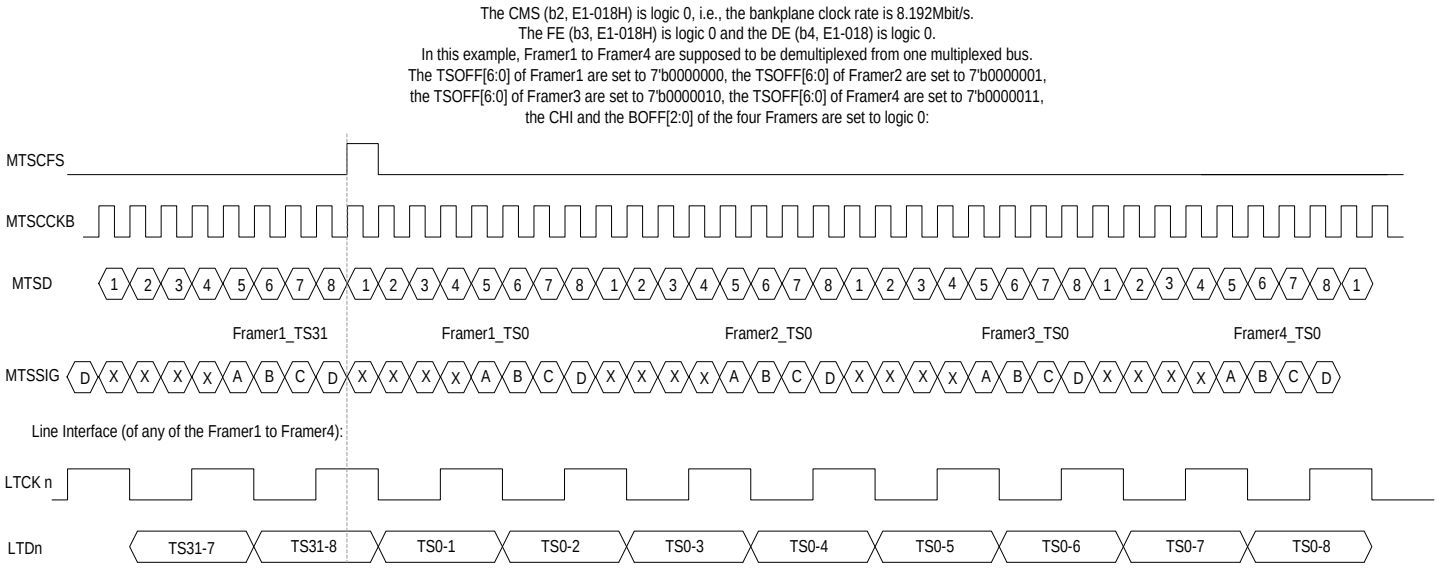


Figure 46. E1 Transmit Multiplexed Mode - Functional Timing Example 1

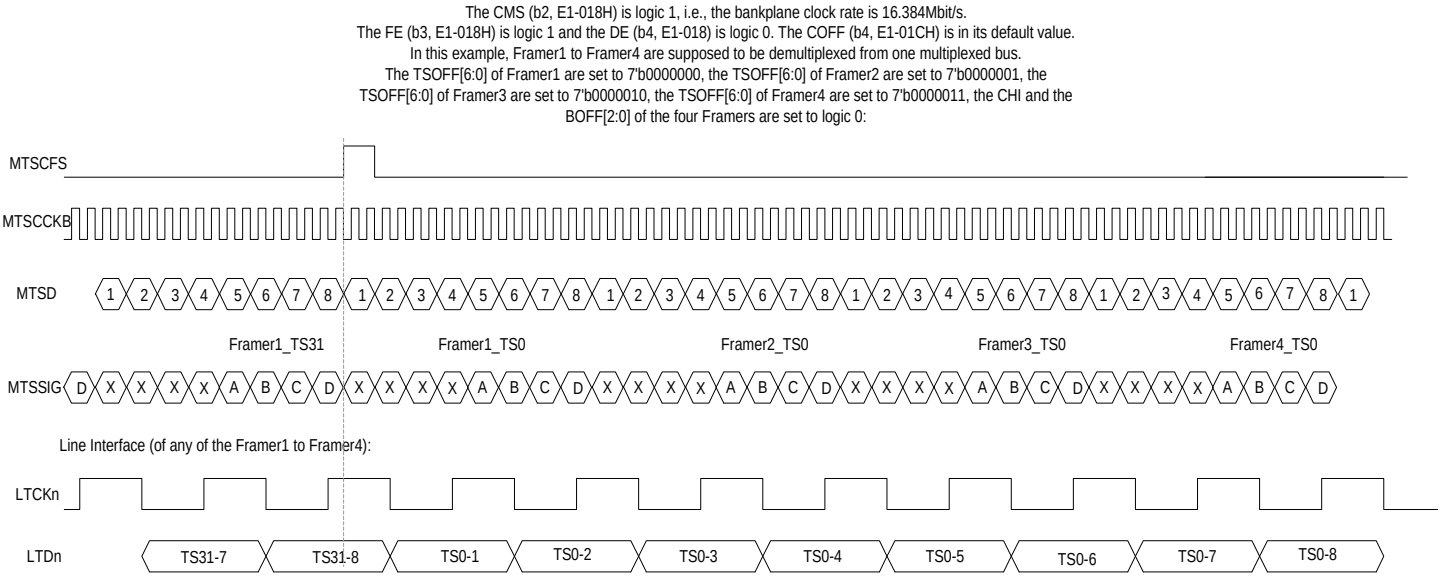


Figure 47. E1 Transmit Multiplexed Mode - Functional Timing Example 2

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3.13.1.4 Parity Check

In all the above four modes, parity check is calculated over the bits in the previous Basic Frame and the result is inserted into the first bit (MSB) of TS0 on the TSDn/MTSD pin. The even parity or odd parity is chosen by the TPTYP (b7, E1-01AH) and whether the first bit of TS0 is calculated or not is determined by the PTY_EXTD (b3, E1-01AH). The parity error event will be captured by the TDI (b5, E1-01AH). The parity error will cause an interrupt on the $\overline{INT}$ pin if the TPTYE (b6, E1-01AH) is enabled.

3.13.1.5 Offset

In the Transmit Clock Slave mode and Transmit Multiplexed mode, time slot offset is enabled by setting a non-zero value into the TSOFF[6:0] (b6~0, E1-01BH). The time slot offset is between TSCFS/MTSCFS and the start of the corresponding frame to be transmitted on TSDn/MTSD. The time slot offset can be set in both single clock mode (CMS [b2, E1-018H] = 0) and double clock mode (CMS [b2, E1-018H] = 1).

In all the above four modes, bit offset is enabled by setting a non-zero value into the BOFF[2:0] (b2~0, E1-01CH). In the Transmit Clock Slave mode and Transmit Multiplexed mode, the bit offset is between TSCFS/MTSCFS and the start of the corresponding frame to be transmitted on TSDn/MTSD. The bit offset can be set in both single clock mode (CMS [b2, E1-018H] = 0) and double clock mode (CMS [b2, E1-018H] = 1). However, if the CHI (b3, E1-01CH) is logic 0, the bit offset value equals the setting in the BOFF[2:0] (b2~0, E1-01CH). That is, '000' in the BOFF[2:0] (b2~0, E1-01CH) means no bit offset; '001' in the BOFF[2:0] (b2~0, E1-01CH) means one bit offset, and so on (refer to the examples in Figure 48 and Figure 49). If the CHI (b3, E1-01CH) is logic 1, the bit offset configured in the BOFF[2:0] (b2~0, E1-01CH) meets the Concentration Highway Interface (CHI) specification (refer to Table 31 and Table 32). The CER (clock edge receive) is counted from the active edge of TSCFS/MTSCFS (refer to the examples in Figure 50 and Figure 51). When the bit offset is configured, the signal on TSSIGn/MTSSIG or the pulse on TSFSn is aligned to RSDn/MRSD. In Transmit Clock Master mode, the bit offset is between TSFSn and the start of the corresponding frame to be transmitted on TSDn. In this case, the CHI specification is not supported and the bit offset value equals the setting in the BOFF[2:0] (b2~0, E1-01CH) (refer to the example in Figure 52).

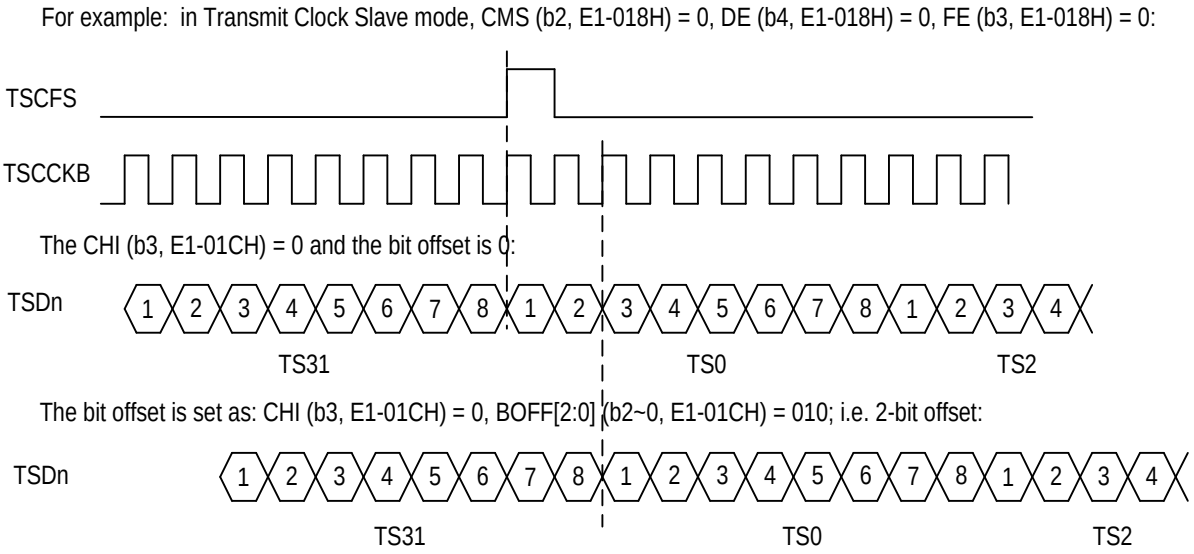


Figure 48. Transmit Bit Offset in E1 Mode - 1

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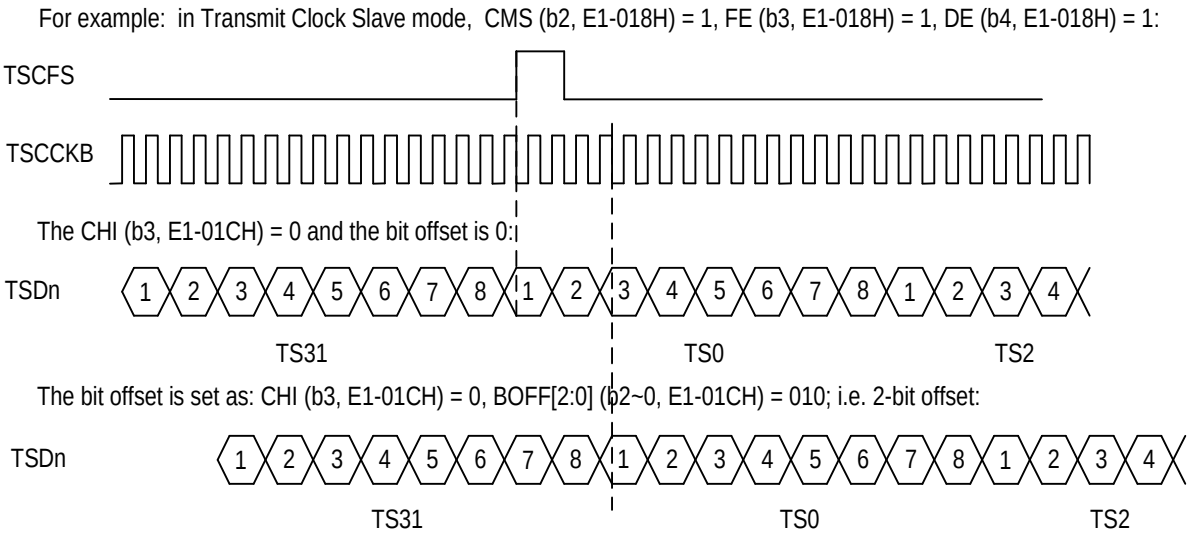


Figure 49. Transmit Bit Offset in E1 Mode - 2

Table 31: Transmit System Interface Bit Offset (CHI [b3, E1-01CH] = 1, CMS [b2, E1-018H] = 0)

FE (b3, E1-018H)	DE (b4, E1-018H)	BOFF[2:0] (b2~0, E1-01CH)								
		000	001	010	011	100	101	110	111	
0	0	4	6	8	10	12	14	16	18	CER
0	1	3	5	7	9	11	13	15	17	
1	0	3	5	7	9	11	13	15	17	
1	1	4	6	8	10	12	14	16	18	

Table 32: Transmit System Interface Bit Offset (CHI [b3, E1-01CH] = 1, CMS [b2, E1-018H] = 1)

FE (b3, E1-018H)	DE (b4, E1-018H)	BOFF[2:0] (b2~0, E1-01CH)								
		000	001	010	011	100	101	110	111	
0	0	6	10	14	18	22	26	30	34	CER
0	1	7	11	15	19	23	27	31	35	
1	0	7	11	15	19	23	27	31	35	
1	1	6	10	14	18	22	26	30	34	

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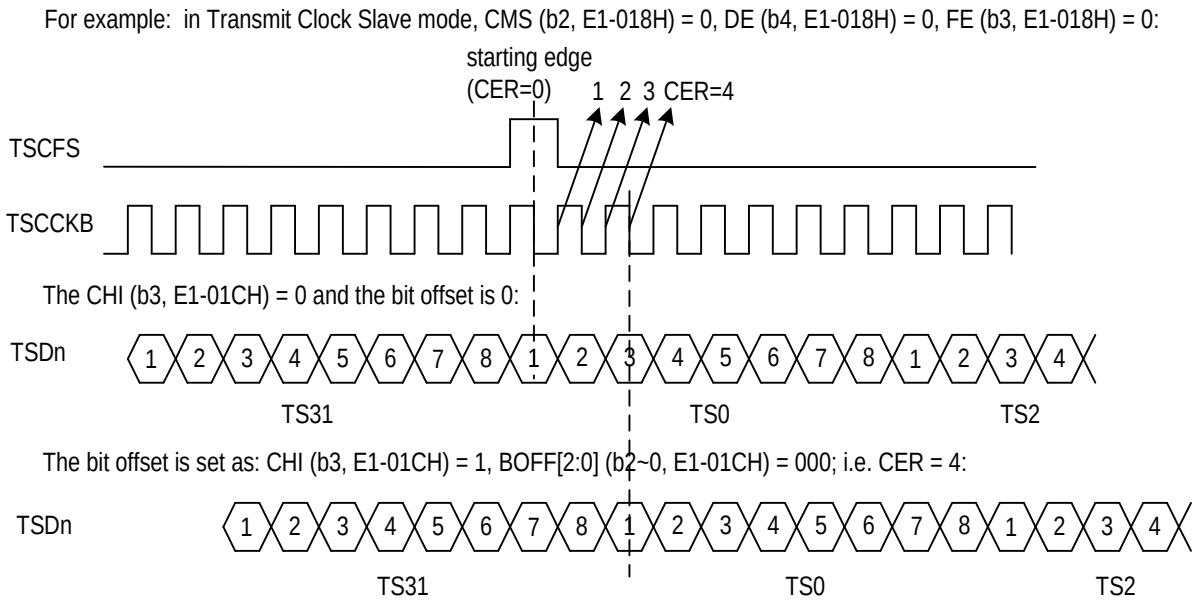


Figure 50. Transmit Bit Offset in E1 Mode - 3

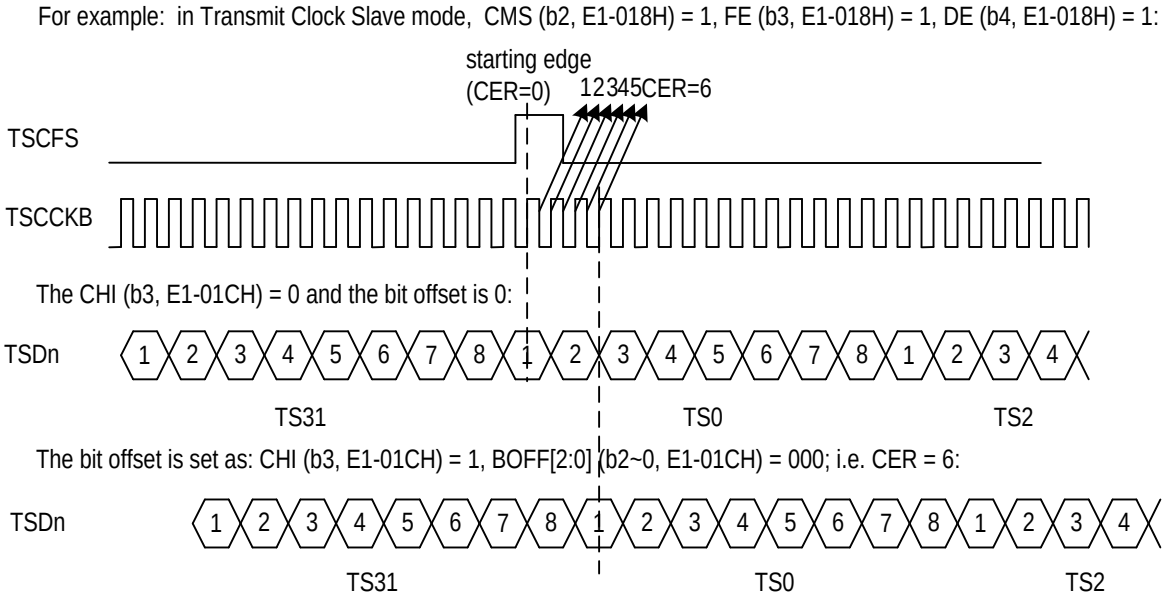


Figure 51. Transmit Bit Offset in E1 Mode - 4

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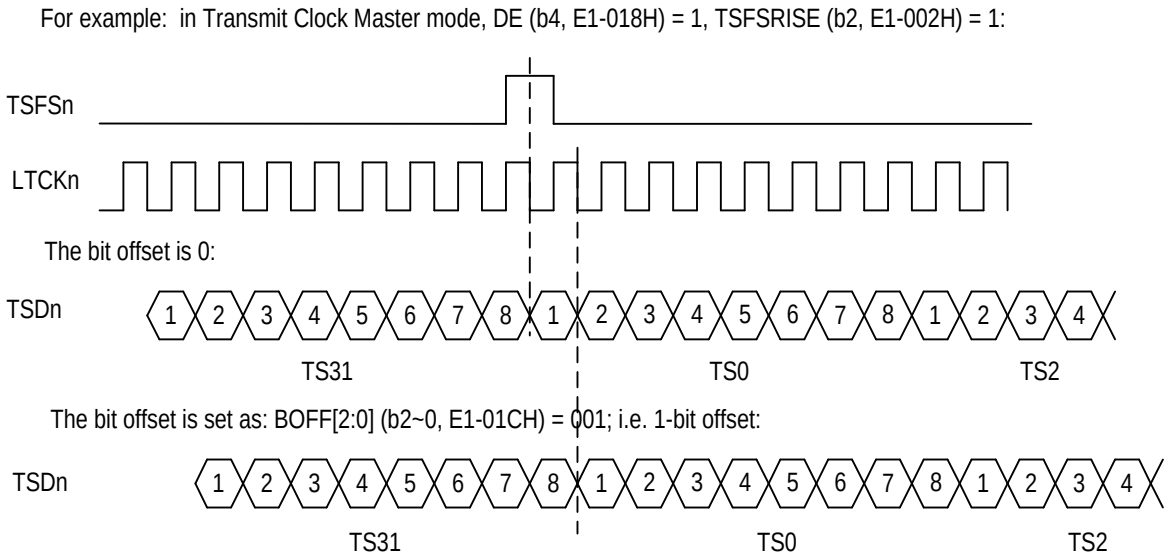


Figure 52. Transmit Bit Offset in E1 Mode - 5

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3.13.2 T1/J1 MODE

In T1/J1 mode, the Transmit System Interface can be set in Non-multiplexed Mode or Multiplexed Mode. In the Non-multiplexed Mode, the TSDn pin is used to input the data to each framer at a bit rate of 1.544 Mb/s or 2.048 Mb/s (T1/J1 mode E1 rate). While in the Multiplexed Mode, the data input to the eight framers is converted to 2.048 Mb/s format and byte-interleaved from two high speed data streams and inputs on the MTSD1 and MTSD2 pins at a bit rate of 8.192 Mb/s.

In the Non-multiplexed Mode, if the timing signal for clocking data on the TSDn pin is provided by the system side and shared by all eight framers, the Transmit System Interface should be set in Transmit Clock Slave mode. If the timing signal for clocking data on each TSDn pin is provided from each line side (processed timing signal), the Transmit System Interface should be set in Transmit Clock Master mode.

In the Non-multiplexed Mode, if there is a common framing pulse provided by the system side for the eight framers, the Transmit System Interface should be set in Transmit Clock Slave mode. If there is not a common framing pulse, the Transmit System Interface should be set in Transmit Clock Master mode.

In the Transmit Clock Slave mode, if the multi-function pin TSFSn/TSSIGn is used to output the framing indication pulse, the Transmit System Interface is in Transmit Clock Slave TSFS Enable mode. If the TSFSn/TSSIGn pin is used to input the signaling bits to be inserted, the Transmit System Interface is in Transmit Clock Slave External Signaling mode.

The T1/J1 mode E1 rate, which means the system clock rate is 2.048 MHz in T1/J1 mode, can only be supported in the Transmit Clock Slave mode.

In the Transmit Clock Master mode, the multi-function pin TSFSn/TSSIGn is used as TSFSn to input the framing indication pulse.

Table 33 summarizes the transmit system interface in different operation modes. To set the transmit system interface of each framer into various operation modes, the registers must be configured as Table 34.

Table 33: T1/J1 Mode Transmit System Interface in Different Operation Modes

Operation Mode			Data Pin	Clock Pin	Framing Pin	Signaling Pin	Reference Clock Pin
Non-Multiplexed Mode	Clock Slave Mode	TSFS Enable	TSDn	TSCCKB	TSCFS & TSFSn	No	TSCCKA
		External Signaling	TSDn	TSCCKB	TSCFS	TSSIGn	TSCCKA
	Clock Master Mode		TSDn	LTCKn	TSFSn	No	TSCCKA & TSCCKB
Multiplexed Mode			MTSD	MTSCCKB	MTSCFS	MTSSIG	TSCCKA

Table 34: Operation Mode Selection in T1/J1 Transmit Path

RATE[1:0] (b3~2, T1/J1-005H)	EMODE[1:0] (b7~6, T1/J1-005H)	Operation Mode
00 / 01 *	10	Transmit Clock Slave TSFS Enable
	11	Transmit Clock Slave External Signaling
00	01	Transmit Clock Master
11 (in any of the eight framers)	11	Transmit Multiplexed

Note:
* When the RATE[1:0] are '00', the system clock rate is 1.544MHz.
When the RATE[1:0] are '01', the system clock rate is 2.048MHz, i.e., T1/J1 mode E1 rate.

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3.13.2.1 Transmit Clock Slave Mode

In the Transmit Clock Slave mode, the bit rate on the TSDn pin is 1.544 Mb/s. However, if the system clock rate is 2.048MHz, the data to be transmitted should be converted into the same rate as the line side, that is, to work in T1/J1 mode E1 rate. Thus the RATE[1:0] (b3~2, T1/J1-005H) should be set to '01'. The conversion complies as follows: The last bit of Frame N of the system side is the F-bit of Frame N in the device. Then one byte of the system side is discarded after the previous three bytes are converted into the device. This process repeats eight times and the conversion of one frame is completed. Then the process goes on (refer to Figure 53).

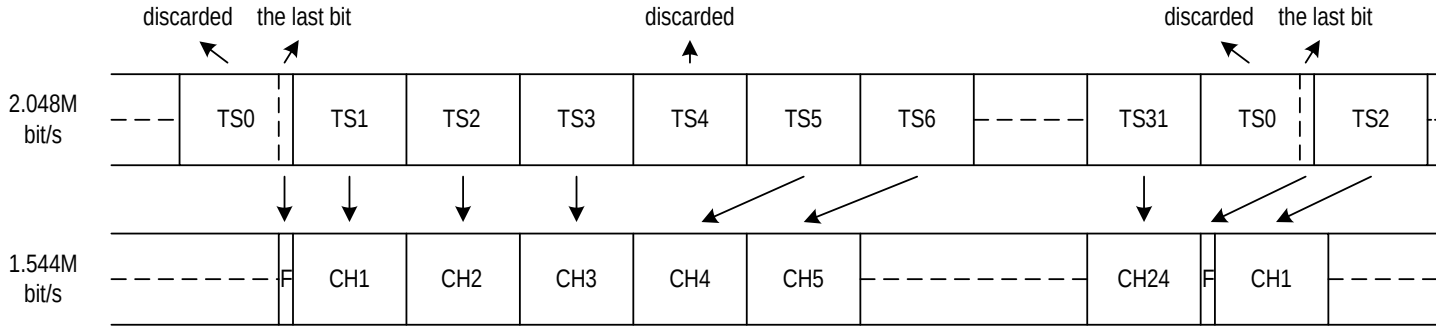


Figure 53. E1 To T1/J1 Format Conversion

In the Transmit Clock Slave mode, the Transmit Side System Common Clock B (TSCCKB) is provided by the system side. It is used as a common timing clock for all eight framers. The speed of TSCCKB can be 1.544MHz or 2.048MHz. When it is 2.048MHz, TSCCKB can be chosen by the CMS (b5, T1/J1-015H) to be the same as the data (2.048Mb/S), or double the data (4.096Mb/s). The CMS (b5, T1/J1-015H) of the eight framers should be set to the same value. If the speed of TSCCKB is double of the data, there will be two active edges in one bit duration. In this case, the COFF (b4, T1/J1-015H) determines the active edge to sample the signal on the TSDn and TSSIGn pins and the active edge to update the pulse on the TSFSn pin; however, the pulse on TSCFS is always sampled on its first active edge.

In the Transmit Clock Slave mode, the Transmit Side System Common Clock A (TSCCKA) is provided by the system side. It is used as one of the reference clocks for the transmit jitter attenuator DPLL for all eight framers (refer to Chapter 3.20 Transmit Clock for details).

In the Transmit Clock Slave mode, the Transmit Side System Common Frame Pulse (TSCFS) is used as a common framing signal to align data streams for the eight framers. TSCFS is asserted on the request of each F-bit, the first F-bit of every 12 SFs or every 24 ESFs, as indicated by the TSCFSP (b1, T1/J1-005H). The valid polarity of TSCFS is configured by the FPINV (b5, T1/J1-005H).

The Transmit Clock Slave Mode includes two sub-modes: Transmit Clock Slave TSFS Enable Mode and Transmit Clock Slave External Signaling Mode.

3.13.2.1.1 Transmit Clock Slave TSFS Enable Mode

In this mode (refer to Figure 37), the data on the system interface is clocked by TSCCKB. The active edge of TSCCKB to sample the pulse on TSCFS and the data on TSDn and TSFSn is determined by the following bits in the registers (refer to Table - 35).

Table 35: Active Edge Selection of TSCCKB (in T1/J1 Transmit Clock Slave TSFS Enable Mode)

	the Bit Determining the Active Edge of TSCCKB
TSCFS	TSCCKBFALL (b3, T1/J1-004H)
TSD	
TSFS	TSFSRISE (b5, T1/J1-004H)

Note:
The TSCCKBFALL (b3, T1/J1-004H) of the eight framers should be set to the same value to ensure TSCFS for the eight framers is sampled on the same active edge.

Figure 54 to Figure 56 show the functional timing examples. Bit 1 of each channel is the first bit to be transmitted.

Besides all the common functions described in the Transmit Clock Slave mode, the special feature in this mode is that the multi-functional pin TSFSn/TSSIGn is used as TSFSn to output a framing pulse to indicate every F-bit.

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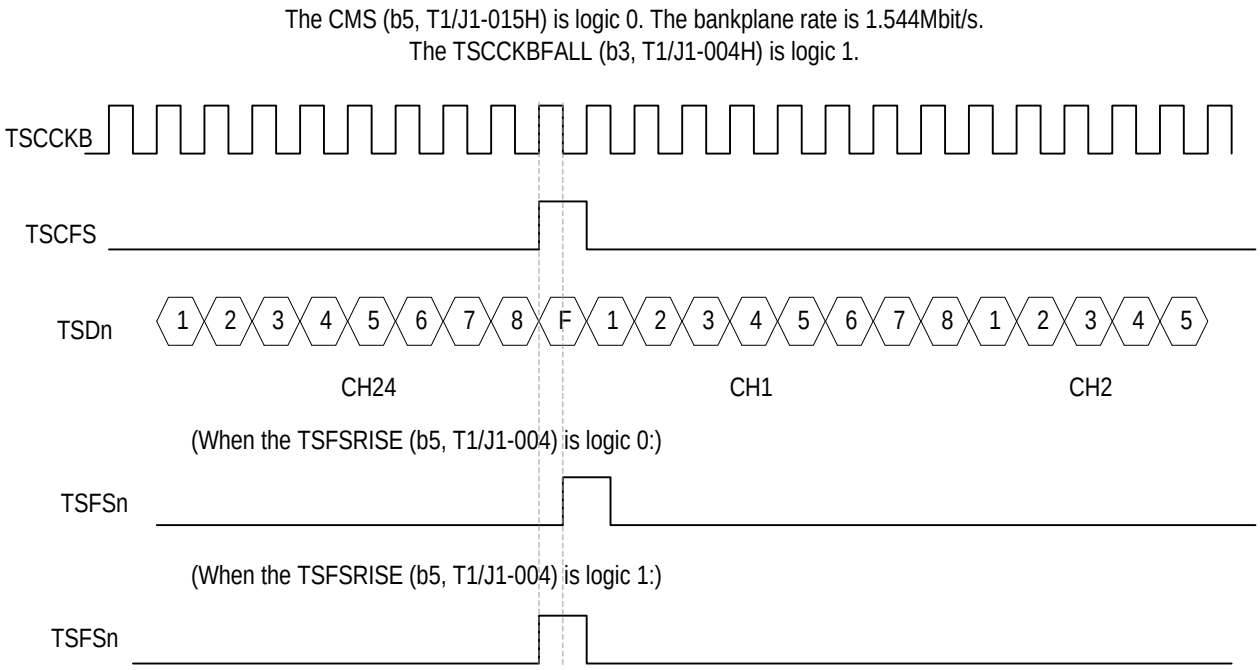


Figure 54. T1/J1 Transmit Clock Slave TSFS Enable Mode - Functional Timing Example 1

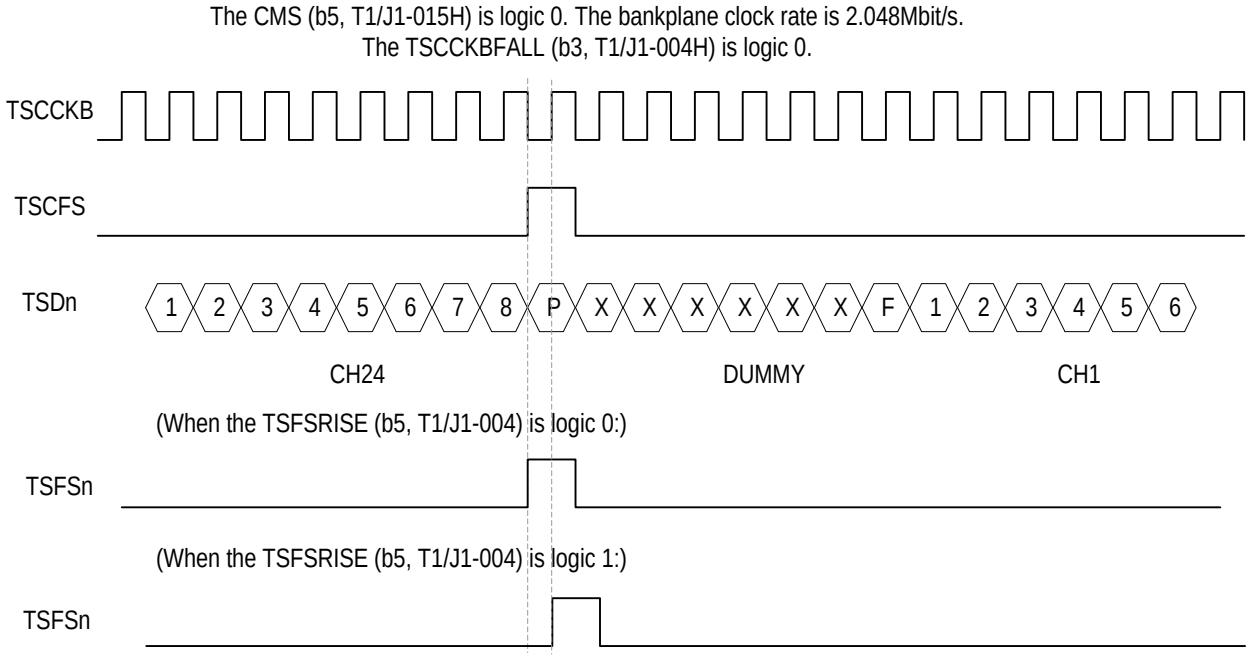


Figure 55. T1/J1 Transmit Clock Slave TSFS Enable Mode - Functional Timing Example 2

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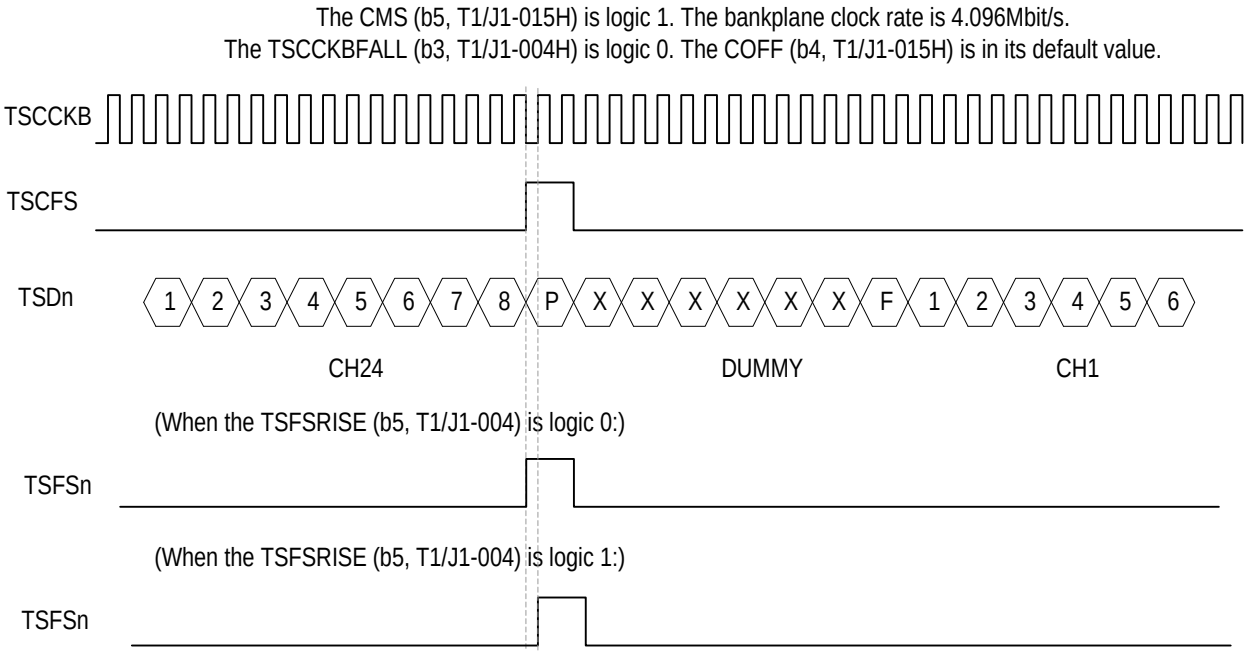


Figure 56. T1/J1 Transmit Clock Slave TSFS Enable Mode - Functional Timing Example 3

3.13.2.1.2 Transmit Clock Slave External Signaling Mode

In this mode (refer to Figure 40), the data on the system interface is clocked by TSCCKB. The active edge of TSCCKB to sample the pulse on TSCFS and the data on TSDn and TSSIGn is determined by the TSCCKBFALL (b3, T1/J1-004H). The TSCCKBFALL (b3, T1/J1-004H) of the eight framers should be set to the same value to ensure TSCFS for the eight framers is sampled on the same active edge.

Figure 57 to Figure 59 show the functional timing examples. Bit 1 of each channel is the first bit to be transmitted.

Besides all the common functions described in the Transmit Clock Slave mode, the special feature in this mode is that the multi-functional pin TSFSn/TSSIGn is used as TSSIGn to input the signaling. The signaling on the TSSIGn pin may be configured by the ABXXEN (b4, T1/J1-005H) to be valid only in the upper two-bit positions of the lower nibble of each channel (i.e. XXXXABXX) in T1 ESF mode.

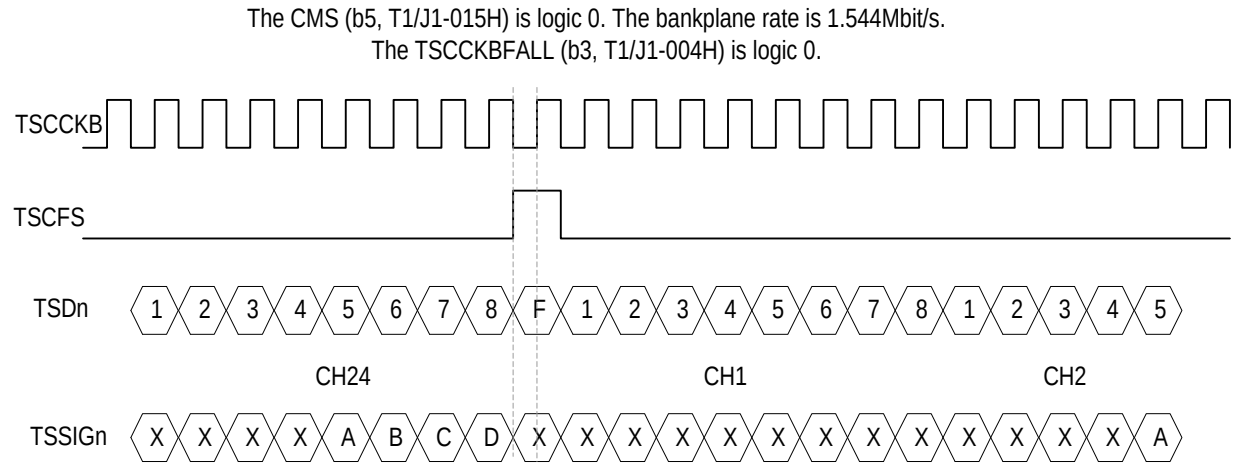


Figure 57. T1/J1 Transmit Clock Slave External Signaling Mode - Functional Timing Example 1

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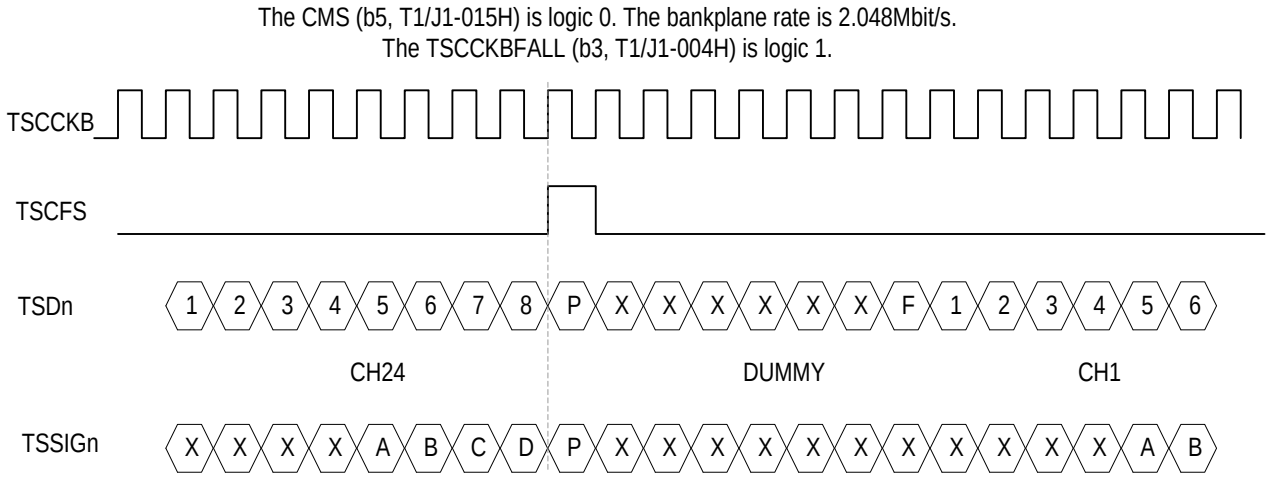


Figure 58. T1/J1 Transmit Clock Slave External Signaling Mode - Functional Timing Example 2

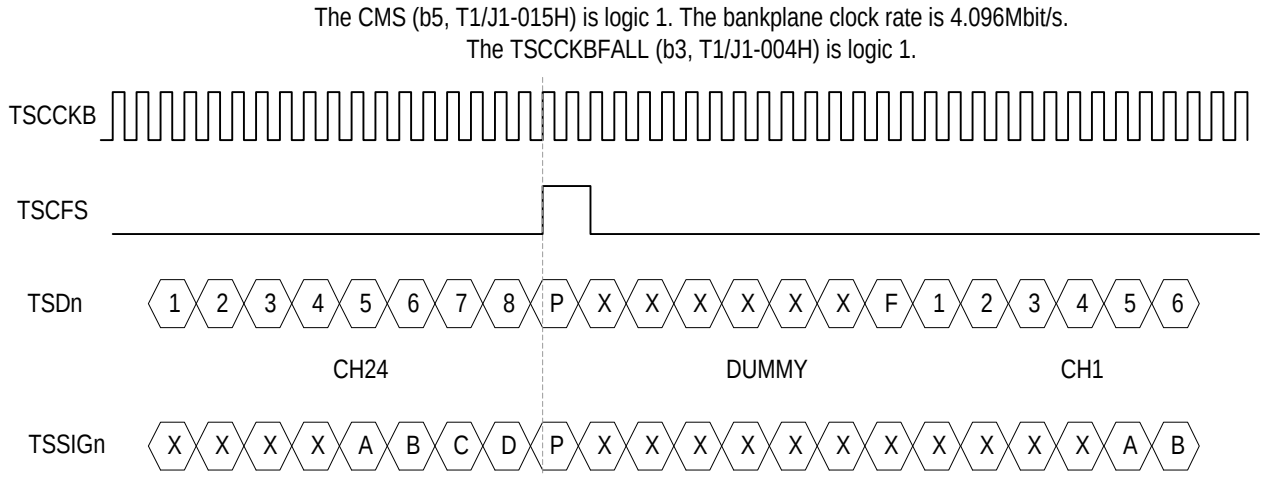


Figure 59. T1/J1 Transmit Clock Slave External Signaling Mode - Functional Timing Example 3

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3.13.2.2 Transmit Clock Master Mode

In the Transmit Clock Master mode (refer to Figure 43), the Transmit Side System Common Clock A (TSCCKA) and Transmit Side System Common Clock B (TSCCKB) provided by the system side are used as one of the reference clocks for the transmit jitter attenuator DPLL for all eight framers (refer to Chapter 3.20 Transmit Clock for details).

In the Transmit Clock Master mode, the multi-functional pin TSFSn/TSSIGn is used as TSFSn to output a framing pulse to indicate every F-bit.

In the Transmit Clock Master mode, the bit rate on the TSDn pin is 1.544Mb/s.

In the Transmit Clock Master mode, each framer uses its own processed clock signal on the LTCKn pin to sample/update the data on the system interface. The active edge of LTCKn to sample the data on the TSDn pin is determined by the TSDFALL (b1, T1/J1-004H). The active edge of LTCKn to update the pulse on the TSFSn pin is determined by the TSFSRISE (b5, T1/J1-004H).

Figure 60 shows the functional timing examples. Bit 1 of each channel is the first bit to be transmitted.

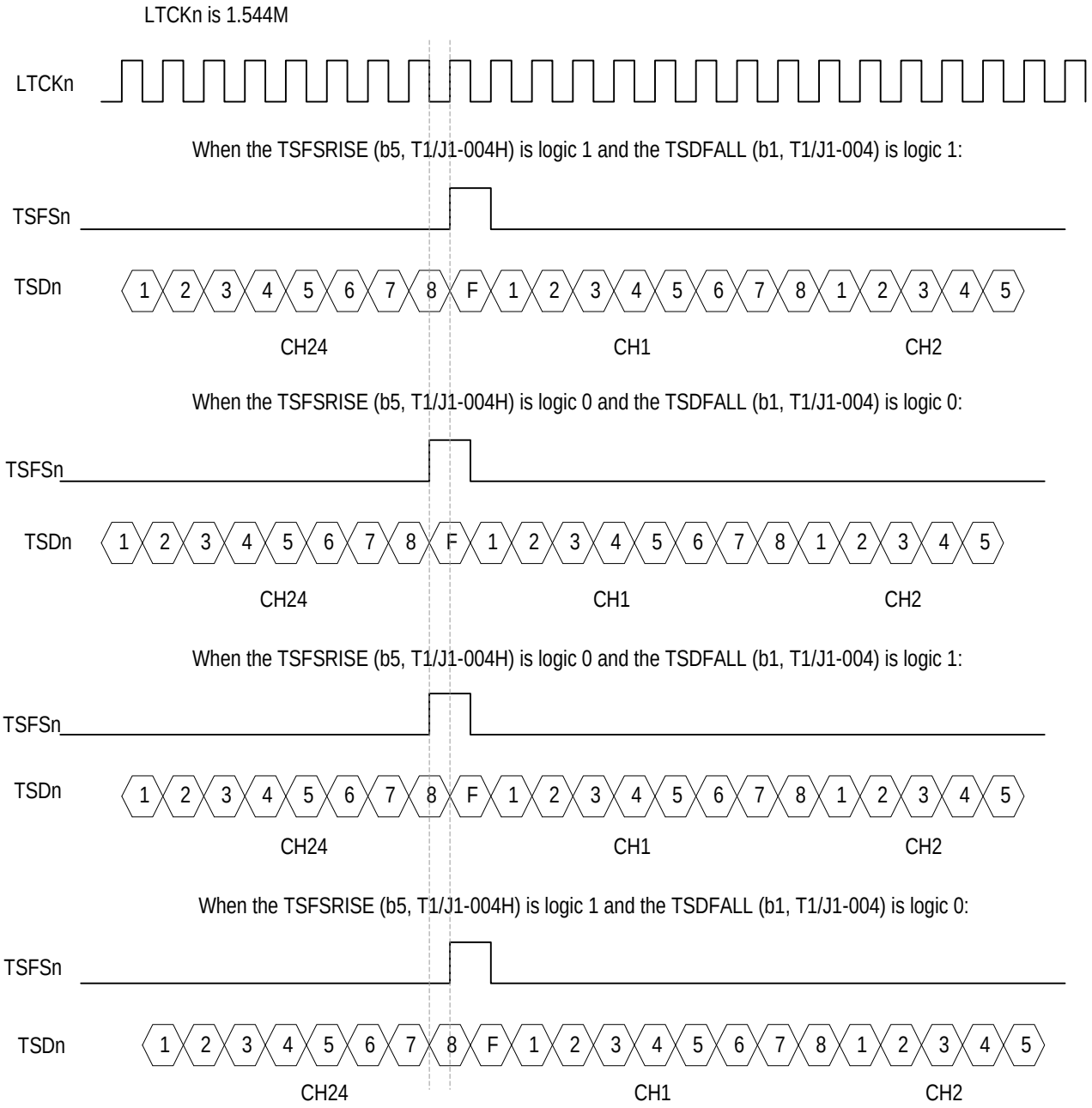


Figure 60. T1/J1 Transmit Clock Master Mode - Functional Timing Example

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3.13.2.3 Transmit Multiplexed Mode

In this mode (refer to Figure 45), two multiplexed buses are used to input the data to all eight framers. Chosen by the MTBS (b6, T1/J1-015H) in each framer, the data on one of the two multiplexed buses is byte-interleaved input to up to four framers. When each four framers is selected, the input sequence of the data on one multiplexed bus is arranged by setting the channel offset TSOFF[6:0] (b6~0, T1/J1-014H). The data for a different framer from one multiplexed bus must be shifted by a different channel offset to avoid data mixing. Then the data on the multiplexed bus will be input to each of the four selected framers with a byte-interleaved manner.

In the Transmit Multiplexed mode, the data on the system interface is clocked by MTSCCKB. The active edge of MTSCCKB to sample the data on the MTSCFS, MTSD and MTSSIG pins is determined by the TSCCKBFALL (b3, T1/J1-004H). The TSCCKBFALL (b3, T1/J1-004H) of the eight framers should be set to the same value.

In the Transmit Multiplexed mode, the Multiplexed Transmit Side System Common Clock B (MTSCCKB) is provided by the system side. It is used as a common timing clock for all eight framers. The speed of MTSCCKB can be chosen by the CMS (b5, T1/J1-015H) to be the same as the data to be transmitted (8.192MHz), or double the data (16.384MHz). If the speed of MTSCCKB is double the data to be transmitted, there will be two active edges in one bit duration. In this case, the COFF (b4, T1/J1-015H) determines the active edge to sample the signal on the MTSD and MTSSIG pins and the active edge to update the pulse on the MTSFS pin; however, the pulse on MTSCFS is always sampled on its first active edge. If the CMS (b5, T1/J1-015H) or the COFF (b4, T1/J1-015H) of any of the eight framers is configured as logic 1, all the others are taken as logic 1. That is, the CMS (b5, T1/J1-015H) and the COFF (b4, T1/J1-015H) of the eight framers should be configured to the same value in the Transmit Multiplexed mode.

In the Transmit Multiplexed mode, the Transmit Side System Common Clock A (TSCCKA) is provided by the system side. It is used as one of the reference clocks for the transmit jitter attenuator DPLL for all eight framers (refer to Chapter 3.20 Transmit Clock for details).

In the Transmit Multiplexed mode, the Multiplexed Transmit Side System Common Frame Pulse (MTSCFS) is used as a common framing signal to align data streams on the two multiplexed buses. MTSCFS is asserted on the F-bit of the selected first framer. The valid polarity of MTSCFS is configured by the FPINV (b5, T1/J1-005H). The FPINV (b5, T1/J1-005H) of the eight framers should be the same value.

In the Transmit Multiplexed mode, the bit rate on the MTSD pin is 8.192Mb/s.

In the Transmit Multiplexed mode, MTSSIG input the signaling bits to be inserted. The signaling bits are channel aligned with the data input from MTSD. The signaling on the MTSSIG pin may be configured by the ABXXEN (b4, T1/J1-005H) to be valid only in the upper two-bit positions of the lower nibble of each channel (i.e. XXXXABXX) in T1 ESF mode.

Figure 61 & Figure 62 show the functional timing examples. Bit 1 of each channel is the first bit to be transmitted.

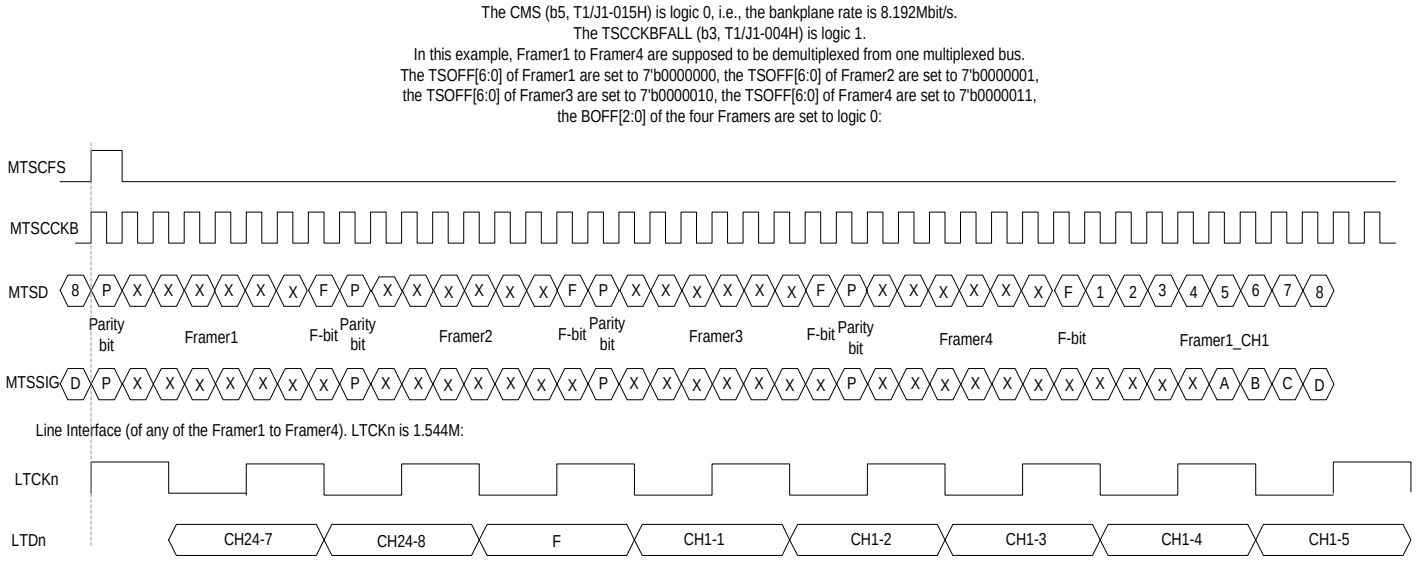


Figure 61. T1/J1 Transmit Multiplexed Mode - Functional Timing Example 1

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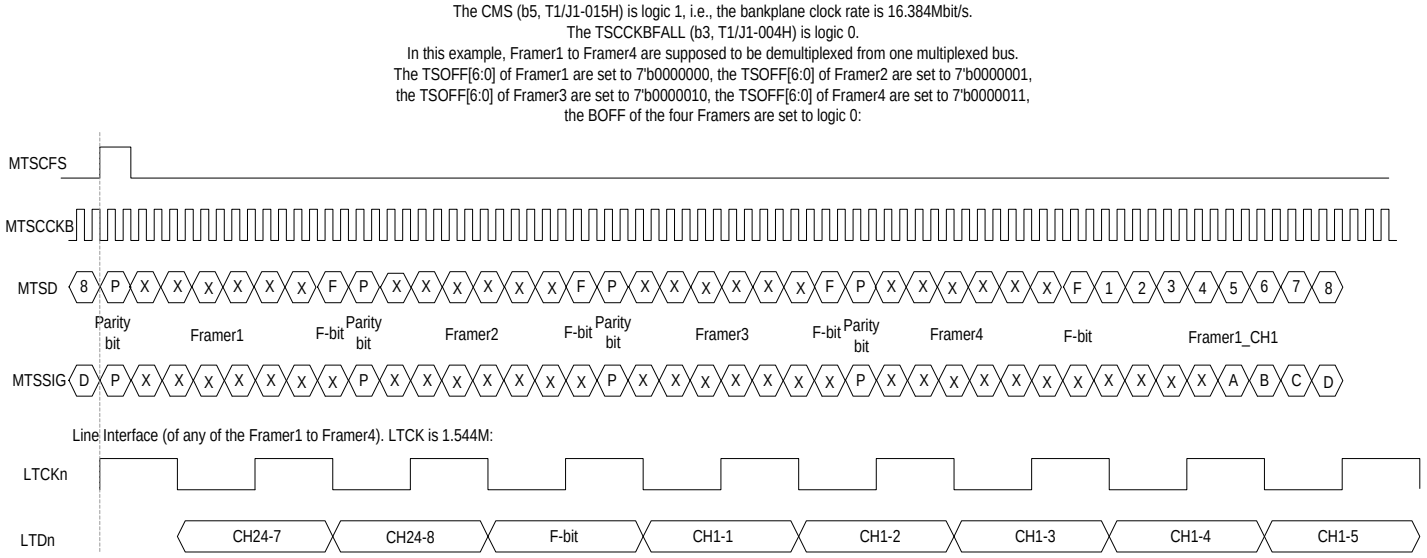


Figure 62. T1/J1 Transmit Multiplexed Mode - Functional Timing Example 2

3.13.2.4 Parity Check

In the above four modes, parity check is calculated over the bits in the previous frame and the result is input into the F-bit on the TSDn/MTSD and TSSIGn/MTSSIG pins. The even parity or odd parity is chosen by the TPTYP (b7, T1/J1-002H) and whether the F-bit is calculated or not is determined by the PTY_EXTD (b3, T1/J1-002H). The parity error event on the TSDn pin will be captured by the TSDI (b5, T1/J1-002H) and the parity error event on the TSSIGn pin will be captured by the TSSIGI (b4, T1/J1-002H). The TSDI (b5, T1/J1-002H) and TSSIGI (b4, T1/J1-002H) will be cleared after being read. The parity error will cause an interrupt on the $\overline{\text{INT}}$ pin if the TPRTYE (b6, T1/J1-002H) is enabled.

3.13.2.5 Offset

When the system clock rate is 2.048MHz (in Transmit Clock Slave T1/J1 mode E1 rate mode) or 8.192MHz (in Transmit Multiplexed mode), the channel offset and/or bit offset between TSCFS/MTSCFS and the start of the corresponding frame on TSDn/MTSD can be configured. The channel offset and bit offset can be set in both single clock mode (CMS [b5, T1/J1-015H] = 0) and double clock mode (CMS [b5, T1/J1-015H] = 1).

The channel offset is enabled by setting a non-zero value into the TSOFF[6:0] (b6~0, T1/J1-014H). The TSOFF[6:0] (b6~0, T1/J1-014H) give a binary representation.

The bit offset is enabled by setting a non-zero value into the BOFF[2:0] (b2~0, T1/J1-015H). The bit offset value equals the setting in the BOFF[2:0] (b2~0, T1/J1-015H). That is, '000' in the BOFF[2:0] (b2~0, T1/J1-015H) means no bit offset; '001' in the BOFF[2:0] (b2~0, T1/J1-015H) means one bit offset, and so on (refer to the examples in Figure 63 and Figure 64). When the bit offset is configured, the signal on TSSIGn/MTSSIG or the pulse on TSFSn is aligned to RSDn/MRSD.

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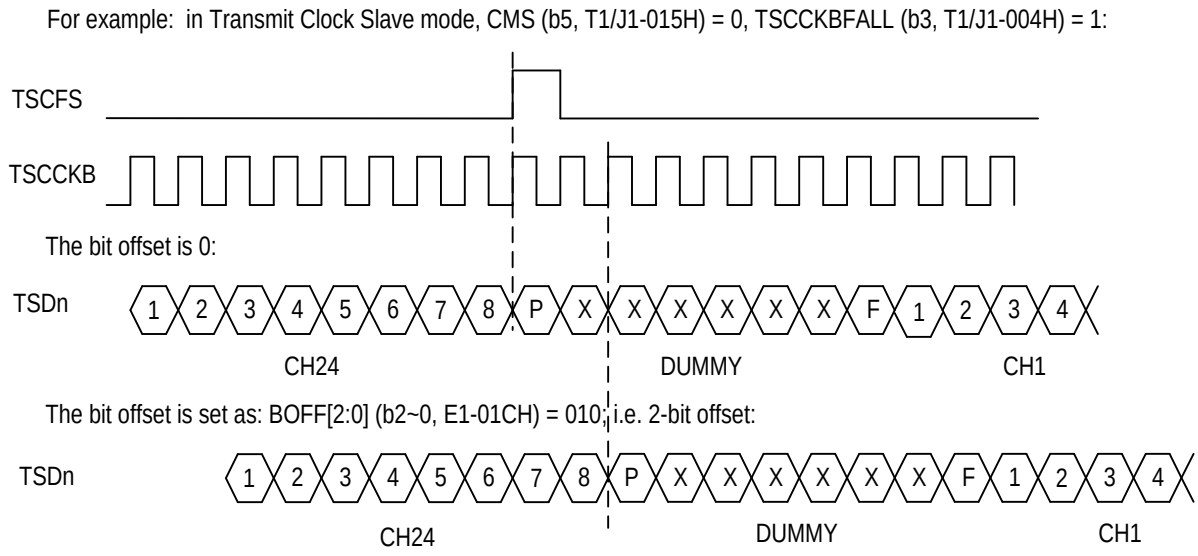


Figure 63. Transmit Bit Offset in T1/J1 Mode - 1

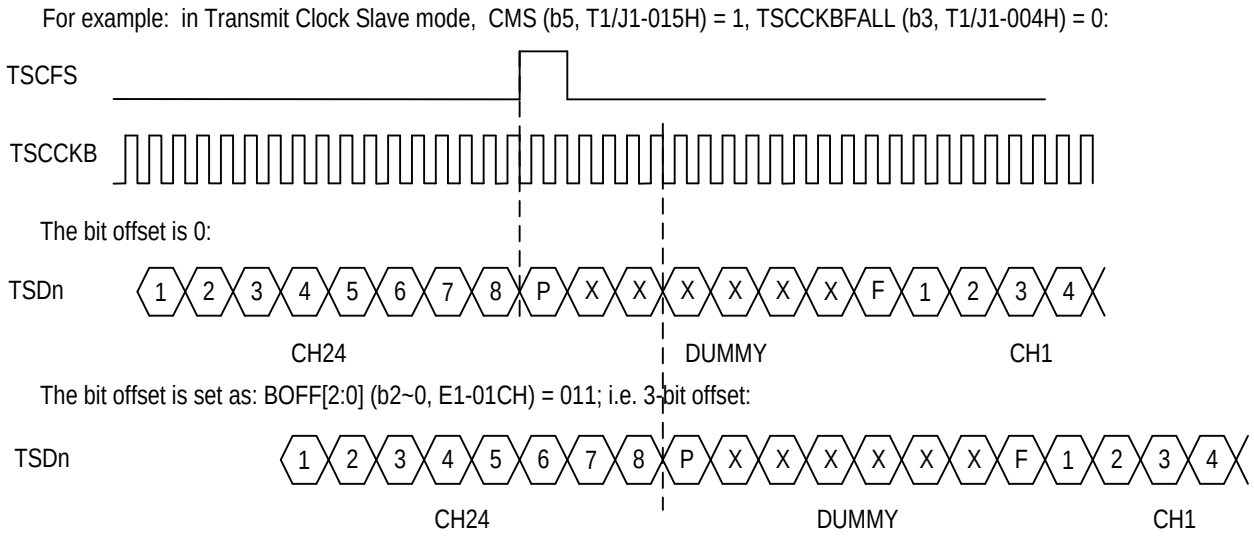


Figure 64. Transmit Bit Offset in T1/J1 Mode - 2

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3.14 TRANSMIT PAYLOAD CONTROL (TPLC)

Different test patterns can be inserted in the data to be transmitted or the data to be transmitted can be extracted to the PRBS Generator/Detector for test in this block. The Transmit Payload Control of each framer operates independently.

3.14.1 E1 MODE

To enable the test for the data to be transmitted, the PCCE (b0, E1-060H) must be set to activate the setting in the indirect registers (from 20H to 7FH of TPLC indirect registers). The following methods can be used for test on a per-TS basis:

- Selected by the PRGDSEL[2:0] (b7~5, E1-00CH), the data to be transmitted on one of the eight framers will be extracted to the PRBS Generator/Detector when the RXPATGEN (b2, E1-00CH) is '1'. The data can be extracted in framed or unframed mode, as determined by the UN_DET (b0, E1-00CH). In unframed mode, all 32 time slots are extracted and the per-timeslot configuration in the TEST (b3, E1-TPLC-indirect registers - 20~3FH) is ignored. In framed mode, the data to be transmitted will only be extracted on the time slot configured by the TEST (b3, E1-TPLC-indirect registers - 20~3FH). Refer to Chapter 3.12 PRBS Generator / Detector (PRGD) for details.

- Enable the payload loopback by setting the LOOP (b2, E1-TPLC-indirect registers - 20~3FH) (refer to Chapter 3.23.3 Payload Loopback).

- Replace the data input from the TSDn/MTSD pin with the A-law or μ-law milliwatt pattern (refer to Table 8 & Table 9) when the SUBS (b7, E1-TPLC-indirect registers - 20~3FH), the DS0 (b4, E1-TPLC-indirect registers - 20~3FH) and the DS1 (b5, E1-TPLC-indirect registers - 20~3FH) are logic 1,1,1 or 1,1,0 respectively.

- Selected by the PRGDSEL[2:0] (b7~5, E1-00CH), the test pattern from the PRBS Generator/Detector will replace the data input from the TSDn/MTSD pin of one of the eight framers when the RXPATGEN (b2, E1-00CH) is '0'. The test pattern can replace the data in framed or unframed mode, as determined by the UN_GEN (b1, E1-00CH). In unframed mode, all 32 time slots are replaced and the per-timeslot configuration in the TEST (b3, E1-TPLC-indirect registers - 20~3FH) is ignored. In framed mode, the received data will only be replaced on the time slot configured by the TEST (b3, E1-TPLC-indirect registers - 20~3FH). Refer to Chapter 3.12 PRBS Generator / Detector (PRGD) for details.

- Replace the data input from the TSDn/MTSD pin with the value in the IDLE[7:0] (b7~0, E1-TPLC-indirect registers - 40~5FH) when the SUBS (b7, E1-TPLC-indirect registers - 20~3FH) and the DS0 (b4, E1-TPLC-indirect registers - 20~3FH) are logic 1,0.

- Invert the odd bits, even bits or all bits input from the TSDn/MTSD pin when the SUBS (b7, E1-TPLC-indirect registers - 20~3FH), the DS0 (b4, E1-TPLC-indirect registers - 20~3FH) and the DS1 (b5, E1-TPLC-indirect registers - 20~3FH) are logic 0,0,1 or 0,1,0 or 0,1,1 respectively.

(The above methods are arranged from highest to lowest in priority.)

- Replace the signaling input from the TSSIGn pin with the value in the A, B, C, D (b3~0, E1-TPLC-indirect registers - 61~7FH) when the SIGSRC (b4, E1-TPLC indirect registers - 61~7FH) is logic 1 and the Channel Associated Signaling (CAS) is chosen by the SIGEN (b6, E1-040H) & DLEN (b5, E1-040H).

Addressed by the A[6:0] (b6~0, E1-062H), the data read from or written into the indirect registers is in the D[7:0] (b7~0, E1-063H). The read or write operation is determined by the R/WB (b7, E1-062H). The indirect registers have a read/write cycle. Before the read/write operation is completed, the BUSY (b7, E1-061H) will be set. New operations on the indirect registers can only be implemented when the BUSY (b7, E1-061H) is cleared. The read/write cycle is 490 ns.

3.14.2 T1/J1 MODE

To enable the test for the data to be transmitted, the PCCE (b0, T1/J1-030H) must be set to activate the setting in the indirect registers (from 01H to 48H of TPLC indirect registers). The following methods can be executed for test on a per-channel basis:

- Selected by the PRGDSEL[2:0] (b7~5, T1/J1-00FH), the data to be transmitted on one of the eight framers will be extracted to the PRBS Generator/Detector when the RXPATGEN (b2, T1/J1-00FH) is '1'. The data can be extracted in framed or unframed mode, as determined by the UN_DET (b0, T1/J1-00FH). In unframed mode, all 24 channels and the F-bit are extracted and the per-channel configuration in the TEST (b3, T1/J1-TPLC-indirect registers - 01~18H) is ignored. In framed mode, the data to be transmitted will only be extracted on the channel specified by the TEST (b3, T1/J1-TPLC-indirect registers - 01~18H). Fractional T1/J1 data can also be extracted in the specified channel when the Nx56k_DET (b3, T1/J1-00FH) is set. Refer to Chapter 3.12 PRBS Generator / Detector (PRGD) for details.

- Enable three types of Zero Code Suppression when the ZCS[1:0] (b1~0, T1/J1-TPLC-indirect registers - 01~18H) is configured.

- Enable the payload loopback by setting the LOOP (b2, T1/J1-TPLC-indirect registers - 01~18H) (refer to Chapter 3.23.3 Payload Loopback).

- Replace the data input from the TSDn/MTSD pin with the milliwatt pattern when the DMW (b5, T1/J1-TPLC-indirect registers - 01~18H) is logic 1. (The milliwatt is μ-law. Refer to Table 9.)

- Selected by the PRGDSEL[2:0] (b7~5, T1/J1-00FH), the test pattern from the PRBS Generator/Detector will replace the data input from the TSDn pin of one of the eight framers when the RXPATGEN (b2, T1/J1-00FH) is '0'. The test pattern can replace the data in framed of unframed mode, as determined by the UN_GEN (b1, T1/J1-00FH). In unframed mode, all 24 channels and the F-bit are replaced and the per-channel configuration in the TEST (b3, T1/J1-TPLC-indirect registers - 01~18H) is ignored. In framed mode, the received data will only be replaced on the channel specified by the TEST (b3, T1/J1-TPLC-indirect registers - 01~18H). Fractional T1/J1 signal will also be replaced in the specified channel when the Nx56k_GEN (b4, T1/J1-00FH) is set. Refer to Chapter 3.12 PRBS Generator / Detector (PRGD) for details.

- Replace the data input from the TSDn/MTSD pin with the value in the IDLE[7:0] (b7~0, T1/J1-TPLC-indirect registers - 19~30H) when the IDLE_DS0 (b6, T1/J1-TPLC-indirect registers - 01~18H) is set.

- Invert the most significant bit and/or the other bits in a channel input from the TSDn pin when the SIGNINV and the INVERT (b4 & b7, T1/J1-TPLC-indirect registers - 01~18H) are set.

(The above methods are arranged from highest to lowest in priority.)

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- Replace the signaling input from the TSSIGn pin with the value in the A, B, C, D (b3~0, T1/J1-TPLC-indirect registers - 31~48H) when the SIGC[1:0] (b7~6, T1/J1-TPLC-indirect registers - 31~48H) is configured.

The data of all channels can be set by the GZCS[1:0] (b1~0, T1/J1-044H) to be in GTE and Bell Zero Code Suppression when the bits in a channel are all zeros. The setting in the GZCS[1:0] (b1~0, T1/J1-044H) is logically ORed with the setting in the ZCS[1:0] (b1~0, T1/J1-TPLC-indirect registers - 01~18H).

Addressed by the A[6:0] (b6~0, T1/J1-032H), the data read from or written into the indirect registers is in the D[7:0] (b7~0, T1/J1-033H). The read or write operation is determined by the R/WB (b7, T1/J1-032H). Before the read/write operation is completed, the BUSY (b7, T1/J1-031H) will be set. New operations on the indirect registers can only be implemented when the BUSY (b7, T1/J1-031H) is cleared The read/write cycle is 650 ns.

3.15 FRAME GENERATOR (FRMG)

The Frame Generator of each framer operates independently.

3.15.1 E1 MODE

In E1 mode, the Frame Generator can generate Basic Frame, CRC-4 Multi-Frame and Channel Associated Signaling (CAS) Multi-Frame. The Frame Generator can also transmit alarm indication signal when special conditions occurs in the received data stream. International bits, National bits and Extra bits replacement and data inversion are all supported in the Frame Generator.

3.15.1.1 Generation

In E1 mode, the data to be transmitted can be formed to be Basic Frame, CRC-4 Multi-Frame and Signaling Multi-Frame.

The Basic Frame is generated when the FDIS (b3, E1-040H) is logic 0. The Basic Frame alignment sequence (FAS) - X0011011 will replace the data on the TS0 of each even frame and a logic 1 should be fixed in the 2nd bit of each odd frame.

The CRC-4 Multi-Frame is generated by setting the GENCRC (b4, E1-040H) when the INDIS (b1, E1-040H) is logic 0. The CRC-4 Multi-Frame alignment pattern - 001011 will replace the data on the International bits of the odd basic frames 1~11, and the calculated CRC bits will replace the data on the International bits of the even Basic Frames. The CRC bits are calculated every Sub Multi-Frame (SMF) and located in the next SMF. If the data input from the TSDn pin has already been in CRC Multi-Frame format, the CRC bits can be modified by setting the PATHCRC (b4, E1-002H) to transmit the CRC-4 transparently or modify the CRC-4 bits.

The Signaling Multi-Frame is generated by setting the SIGEN (b6, E1-040H) & the DLEN (b5, E1-040H) to logic 1 (CAS enable). The Signaling Multi-Frame alignment pattern - 0000 will replace the higher nibble (b1 ~ b4) of TS16 of Basic Frame 0, and the signaling source selected by the SIGSRC (b4, E1-TPLC-indirect registers - 61~7FH) will replace the data on TS16 of Basic Frame 1~15 (refer to Chapter 3.14 Transmit Payload Control (TPLC)). When the Signaling Multi-Frame is not generated, setting a logic 1 in the MTRK (b7, E1-041H) will substitute the IDLE code set in the IDLE[7:0] (b7~0, E1-TPLC-indirect registers - 40~5FH) for all the data on TS1 ~ 31. When the Signaling Multi-Frame is generated, the setting will only substitute the IDLE code for TS1~15 and TS17~31. TS16 is occupied by signaling. However, the MTRK (b7, E1-041H) takes effect only when the PCCE (b0, E1-060H) in the Transmit Payload Control is logic 1.

3.15.1.2 Alarm Indication

When special conditions occurs in the received data stream, alarm indication will be transmitted automatically. The alarm indication can also be transmitted manually.

A logic 1 in the 3rd bit of NFAS (A bit) is the Remote Alarm Indication (RAI) signal. It is controlled by the REMAIS (b3, E1-041H), the AUTOYELLOW (b3, E1-000H) and the G706RAI (b0, E1-00EH) as illustrated in Table 36.

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Table 36: Remote Alarm Indication

REMAIS(b3, E1-041H)	AUTOYELLOW(b3, E1-000H)	G706RAI(b0, E1-00EH)	Remote Alarm Indication Signal
1	-	-	Manually force the remote alarm indication signal to be logic 1.
0	1	0	(per ETSI) The RAI is transmitted when any of the four conditions occurs in the received data stream: 1. out of Basic Frame; 2. during AISD; 3. in CRC-4 to non-CRC-4 interworking; 4. the offline searching is out of Basic Frame synchronization.
		1	(per Annex B of G.706) The RAI is transmitted when any of the two conditions occurs in the received data stream: 1. out of Basic Frame; 2. during AISD.
0	0	-	The RAI is not transmitted, that is, logic 0 is forced to transmit in its position.

When CRC-4 Multi-Frame is generated, the International bits of Frame 13 & 15 (E1 & E2 bits) are used for FEBE indication only if the FEBEDIS (b2, E1-040H) is logic 0. When there are CRC calculated errors in SMF I or SMF II in the received data stream, a logic 0 will be automatically replaced in the E1 or the E2 bit for indication respectively. When the received data is out of CRC-4 Multi-Frame synchronization, the E1 and E2 bits can be forced to be logic 0 or logic 1, as determined by the OOCMFE0 (b1, E1-00EH).

When Signaling Multi-Frame is generated, the 6th bit of TS16 of frame 0 (Y bit) is for Signaling Multi-Frame Alarm Indication. A logic 1 in the Y bit means the Signaling Multi-Frame Alarm. However, the value of the Y bit can be forced to be logic 0 or logic 1 by the MFAIS (b2, E1-041H).

3.15.1.3 Control Over International / National / Extra Bits

After the Basic Frame is generated, the International bits (the first bit in TS0) can be replaced when the INDIS (b1, E1-040H) is logic 0.

The setting in the Si[1:0] (b7~6, E1-042H), the CRC-4 Multi-Frame and FEBE signal can all replace the International bits. Their priorities are controlled by the GENCRC (b4, E1-040H) and the FEBEDIS (b2, E1-040H) and illustrated in Table 37.

Table 37: Content in International Bits (when the INDIS [b1, E1-040H] is logic 0)

GENCRC(b4, E1-040H)	FEBEDIS(b2, E1-040H)	Data on the International Bits
0	-	The international bits of the FAS frame represent the setting in the Si[1] (b7, E1-042H), while the international bits of the NFAS frame represent the setting in the Si[0] (b6, E1-042H).
1	0	The international bits of the FAS frame represent the calculated CRC-4 bits; the international bits of the former six NFAS frames represent the CRC-4 alignment sequence (001011). The other two international bits in Frame 13 & 15 represent whether there are CRC-4 calculated errors in the received data stream (FEBE).
1	1	The international bits of the FAS frame represent the calculated CRC-4 bits; the international bits of the former six NFAS frames represent the CRC-4 alignment sequence (001011). The other two international bits in Frame 13 & 15 represent the setting in the Si[1:0] (b7~6, E1-042H) respectively.

When the setting in the SaX[1:4] (b3~0, E1-047H) is activated by the corresponding SaX_EN[1:4] (b7~4, E1-047H), it will replace the data on the National bits whose position is selected by the SaSEL[2:0] (b7~5, E1-046H).

When Signaling Multi-Frame is generated, the extra bits (bits 4, 6 & 7 in TS16 of Frame 0 of the Signaling Multi-Frame) will be replaced with the setting in the X[2:0] (b0~1 & b3, E1-043H) if the XDIS (b0, E1-040H) is logic 0.

3.15.1.4 Diagnostics

For diagnostic purposes, three kinds of data inversion can be executed:

1. When Basic Frame is generated, the FAS can be inverted from '0011011' to '1100100' by setting the FPATINV (b6, E1-041H);

2. When Basic Frame is generated, the 2nd bit of the NFAS can be inverted from '1' to '0' by setting the SPLRINV (b5, E1-041H);

3. When Signaling Multi-Frame is generated, the Signaling Multi-Frame alignment pattern can be inverted from '0000' to '1111' by setting the SPATINV (b4, E1-041H).

Of all the operations, transmitting all ones take the highest priority. All ones will be transmitted only in TS16 when the TS16AIS (b1, E1-041H) is set. All ones will also be transmitted on all the time slots when the AIS (b0, E1-041H) is set.

A FIFO is employed in the Frame Generator to store the data stream to be transmitted. The FIFO can be initiated by setting the FRESH (b7, E1-040H).

3.15.1.5 Interrupt Summary

The interrupt sources are summarized in Table 38. When the conditions are met, the corresponding Interrupt Status bit will be logic 1. Then the interrupt will occur on the $\overline{INT}$ pin if the Interrupt Enable bit is logic 1.

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Table 38: Interrupt Summary in E1 Mode

No.	Interrupt Sources	Indication Bits	Interrupt Mask Bits
1	The end of the first frame of a Signaling Multi-Frame is input to the Frame Generator when Signaling Multi-Frame is generated and coincides with the CRC Multi-Frame.	SIGMFI(b4, E1-045H)	SIGMFE(b4, E1-044H)
2	The end of the first frame of a CRC-4 Multi-Frame is input to the Frame Generator when CRC Multi-Frame is generated.	MFI(b2, E1-045H)	MFE(b4, E1-044H)
3	The end of the first frame of a CRC-4 Sub Multi-Frame is input to the Frame Generator when CRC Multi-Frame is generated.	SMFI(b1, E1-045H)	SMFE(b4, E1-044H)
4	The boundary of a FAS is input to the Frame Generator when Basic Frame is generated.	FASI (b3, E1-045H)	FASE(b4, E1-044H)

3.15.2 T1/J1 MODE

In T1/J1 mode, the data to be transmitted can be either the Super Frame (SF) or the Extended Super Frame (ESF) format. The selection is made by the ESF (b4, T1/J1-044H).

The SF/ESF is generated on the base of the UF (b6, T1/J1-046H) and the FDIS (b3, T1/J1-006H) are logic 0, that is, the F-bit can be replaced with the Frame Alignment Pattern, DL and CRC-6 (the DL and CRC-6 bits only exist in the ESF format). Thus, the FAS can be replaced in its position when the FBITBYP (b2, T1/J1-006H) is logic 0. In the SF format, the Frame Alignment Pattern is '10001101110X' and replaces the F-bit of each frame input from the TSDn pin (refer to Table 3). In the ESF format, the Frame Alignment Pattern is '001011' and replaces the F-bit in every 4th frame starting with Frame 4. The CRC-6 will replace the F-bit in every 4th frame starting with Frame 2 if the CRCBYP (b1, T1/J1-006H) is logic 0. The CRC-6 algorithm is chosen between the T1 standard and the J1 standard by the J1_CRC (b6, T1/J1-044H). The DL bits will replace the F-bit in every other frame starting with Frame 1 when the FDLBYP (b0, T1/J1-006H) is logic 0 (refer to Table 4).

Before the data coming into the Frame Generator, if the SIGC[1:0] (b7~6, T1/J1-TPLC-indirect registers - 31~48H) select the signaling bit input from the TSDn pin to be replaced with the signaling input from the TSSIGn pin, the signaling bit of all channels can be replaced with the signaling of the 1st frame when the SIGAEN (b5, T1/J1-006H) is set. This configuration is to avoid the signaling change in the middle of a SF/ESF.

The data input from the TSDn pin will be replaced by the code set in the IDLE[7:0] (b7~0, T1/J1-TPLC-indirect registers - 19~30H) when the MTRK (b7, T1/J1-044H) is set. When the MTRK (b7, T1/J1-044H) is set, the signaling bits of all channels may also be replaced by the signaling input from the TSSIGn pin or the data set in the A, B, C, D (b3~0, T1/J1-TPLC-indirect registers - 31~48H) according to the setting in the SIGC[1:0] (b7~6, T1/J1-TPLC-indirect registers - 31~48H). The MTRK (b7, T1/J1-044H) takes effect only when the PCCE (b0, T1/J1-030H) in the TPLC is logic 1.

Configured by the TXMFP (b1, T1/J1-00AH), a mimic pattern can be inserted in the 1st bit of each channel. The content of the mimic pattern is the same as the F-bit. The mimic pattern insertion is for diagnostic purposes.

The Yellow alarm signal can be inserted in the data stream to be transmitted when the XYEL (b2, T1/J1-045H) is enabled. The alarm signal pattern is chosen between the T1 and J1 mode by the J1_YEL (b5, T1/J1-044H). The pattern is:

- In T1 SF format: Transmit the logic 0 on the 2nd bit of each channel.
- In J1 SF format: Transmit the logic 1 on the 12th F-bit.
- In T1 ESF format: Transmit the 'FF00' on each DL of F-bit.
- In J1 ESF format: Transmit the 'FFFF' on each DL of F-bit.

The Yellow alarm signal can also be inserted automatically by setting the AUTOYELLOW (b3, T1/J1-000H) when Red alarm is declared in the received data stream.

In the ESF format, if the Yellow alarm signal is stopped by setting the XYEL (b2, T1/J1-045H) to be logic 0, a Yellow alarm disabled pattern will be transmitted automatically. In T1 mode, the pattern is 'FFFF'. In J1 mode, the pattern is 'FF7E'. The disable pattern should be repeated 16 times before the BOC (refer to Chapter 3.17 Bit-Oriented Message Transmitter (TBOM) - T1/J1 Only) or the HDLC bits (refer to Chapter 3.16 HDLC Transmitter (THDLC)) are inserted in the DL bit. The Yellow alarm takes the highest priority in these three kinds of insertion.

If there are no Yellow alarm signal, no BOC, no HDLC bits or no TPLC insertion in the DL of the F-bit, the DL position will be forced to transmit 'FFFF' in T1 mode or '7E7E' in J1 mode continuously.

A FIFO is employed in the Frame Generator to store the data stream to be transmitted. The FIFO can be initiated by setting the FRESH (b7, T1/J1-006H).

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3.16 HDLC TRANSMITTER (THDLC)

The HDLC data insertion is performed in this block. The HDLC Transmitters #1, #2 and #3 in E1 mode or the HDLC Transmitter #1 and #2 in T1/J1 mode ESF format of each framer operate independently.

3.16.1 E1 MODE

Three HDLC Transmitter blocks are provided for each framer to transmit a HDLC link. Before selecting the HDLC link, the TXCISEL (b3, E1-0AH) should be set to '1'. Thus, the configuration of Link Control and Bits Select registers (addressed from 028H to 02DH) is for THDLC. The THDLCSEL[1:0] (b5~4, E1-00AH) select one of the three HDLC controllers to be accessed by the microcontroller. The #2 and #3 blocks can also be disabled by setting the V52DIS (b3, E1-007H). The functionality of the HDLC link can be defined as the follows:

1. Set the DL_EVEN (b7, E1-028H or b7, E1-02AH or b7, E1-02CH) and/or the DL_ODD (b6, E1-028H or b6, E1-02AH or b6, E1-02CH) to select the even and/or odd frames (the even frames are FAS frames while the odd frames are NFAS frames);

2. Set the DL_TS[4:0] (b4~0, E1-028H or b4~0, E1-02AH or b4~0, E1-02CH) to select the time slot of the assigned frame or to set the TS16_EN (b5, E1-028H) to define TS16 of the assigned frame (this HDLC link can only be set in the #1 block and is enabled when the CCS is selected by the SIGEN [b6, E1-040H] and the DLEN [b5, E1-040H]);

3. Set the DL_BIT[7:0] (b7~0, E1-029H or b7~0, E1-02BH or b7~0, E1-02DH) to select the bit of the assigned time slot.

Thereafter, the HDLC packet will replace the data on the assigned data link. All the functions of the selected HDLC Transmitter block are realized only if the EN (b0, E1-050H) is set to logic 1; otherwise, all ones will be transmitted on the assigned data link.

A normal HDLC packet (refer to Figure 5) is started with a 7E (Hex) flag, then the HDLC data is transmitted. Before closing, two bytes of CRC-CCITT frame check sequences (FCS) are added if the CRC (b1, E1-050H) is enabled. The HDLC packet is closed with another 7E flag. However, if the FLGSHARE (b7, E1-050H) is set, the closing flag of the current HDLC packet and the opening flag of the next HDLC packet are shared.

A FIFO buffer is used to store the HDLC data written to the TD[7:0] (b7~0, E1-055H). The UTHR[6:0] (b6~0, E1-051H) set the upper threshold of the FIFO. When the data exceeds the fill level, the data will be transmitted. The opening flag will be prepended before the data automatically. The transmission will not stop until the entire HDLC data is transmitted and the data in the FIFO is below the upper threshold. The end of the current entire HDLC frame is set by the EOM (b3, E1-050H). When it is set, the HDLC data should be transmitted even if it does not exceed the upper threshold of the FIFO. The FCS, if enabled, will be added before the closing flag automatically. Zero stuffing is automatically performed to the serial output data when there are five consecutive ones in the HDLC data or in the FCS. A 7F (Hex) abort sequence which deactivates the current HDLC packet can be inserted anytime the ABT (b2, E1-050H) is set. When the ABT (b2, E1-050H) is set, the current byte in the TD[7:0] (b7~0, E1-055H) is still transmitted, and then the FIFO is cleared and the 7F abort sequence is transmitted continuously. The low threshold of the FIFO can be set in the LINT[6:0] (b6~0, E1-052H), which should always be less than the value of the UTHR[6:0] (b6~0, E1-051H). The FIFO can be cleared anytime the FIFOCLR (b6, E1-050H) is set. Flags (7E) will consecutively be transmitted when there is no HDLC data to be transmitted if the data link is activated.

Four interrupt sources can be derived from this block.

1. When the data in the FIFO is empty or less than the setting in the LINT[6:0] (b6~0, E1-052H), the BLFILL (b5, E1-054H) will indicate. A transition from logic 0 to 1 on the BLFILL (b5, E1-054H) will cause a logic 1 in the LFILLI (b0, E1-054H). The interrupt on the $\overline{INT}$ pin will occur when the LFILLE (b0, E1-053H) is enabled;

2. When the data in the FIFO reaches its maximum capacity - 128 bytes, the FULL (b6, E1-054H) will be set for indication. A transition from logic 0 to 1 on the FULL (b6, E1-054H) will cause a logic 1 in the FULLI (b3, E1-054H). The interrupt on the $\overline{INT}$ pin will occur when the FULLE (b3, E1-053H) is enabled;

3. When the FIFO has already been filled with 128 bytes and new data is still written to it, the FIFO will overflow and the OVRI (b2, E1-054H) will be set for indication. The interrupt on the $\overline{INT}$ pin will occur when the OVRE (b2, E1-053H) is enabled.

4. When the transmission is in process and it is out of data to be transmitted in the FIFO, the FIFO is underrun and the UDRI (b1, E1-054H) will be set for indication. The interrupt on the $\overline{INT}$ pin will occur when the UDRE (b1, E1-053H) is enabled.

3.16.2 T1/J1 MODE

In the SF format, there is no HDLC link.

In the ESF format, two HDLC Transmitter blocks (#1 and #2) are employed for each framer to transmit the HDLC link. Before selecting the HDLC link, the TXCISEL (b3, T1/J1-00DH) should be set to '1'. Thus, the configuration of the Link Control and Bits Select registers (addressed from 070H to 071H) is for THDLC. Selected by the THDLCSEL[1:0] (b5~4, T1/J1-00DH), registers in one of the two HDLC Transmitter blocks are accessible to the microprocessor. The #1 block transmits the HDLC link in the DL of F-bit (its position is shown in the Table 4). The #2 block transmits the HDLC link in a channel and its position is selected as follows:

1. Set the DL2_EVEN (b7, T1/J1-070H) and/or the DL2_ODD (b6, T1/J1-070H) to select the even and/or odd frames;

2. Set the DL2_TS[4:0] (b4~0, T1/J1-070H) to select the channel of the assigned frame;

3. Set the DL2_BIT[7:0] (b7~0, T1/J1-071H) to select the bit of the assigned channel.

All the functions of the selected HDLC Transmitter block are realized only if the EN (b0, T1/J1-034H) is enabled; otherwise, all ones will be transmitted on the assigned data link.

The structure of the HDLC packet (refer to Figure 5) is the same as it is described in the E1 mode. When the FLGSHARE (b7, T1/J1-034H) is set, the closing flag of the current HDLC and the opening flag of the next HDLC are shared.

A FIFO buffer is used to store the HDLC data written to the TD[7:0] (b7~0, T1/J1-039H). The UTHR[6:0] (b6~0, T1/J1-035H) limit the upper threshold of the FIFO. When the data exceeds the fill level, the data will be transmitted. The opening flag will be added before the data automatically. The transmission will not stop until an entire HDLC frame is transmitted and the data in the FIFO is below the upper threshold. The end of

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the current entire HDLC frame is indicated by the EOM (b3, T1/J1-034H). When it is set, the HDLC data should be transmitted even if it does not exceed the upper threshold of the FIFO. The FCS, if enabled by the CRC (b1, T1/J1-034H), will be added before the closing flag automatically. Zero stuffing is automatically performed to the serial output data when there are five consecutive ones in the HDLC data or in the FCS. A 7F abort sequence which deactivates the current HDLC packet can be inserted anytime the ABT (b2, T1/J1-034H) is set. When the ABT (b2, T1/J1-034H) is set, the current byte in the TD[7:0] (b7~0, T1/J1-039H) is still transmitted, and then the FIFO is cleared and the 7F abort sequence is transmitted continuously. The low threshold of the FIFO can be set in the LINT[6:0] (b6~0, T1/J1-036H), which should always be less than the value of the UTHR[6:0] (b6~0, T1/J1-035H). The FIFO can be cleared anytime the FIFOCLR (b6, T1/J1-034H) is set. Flags (7E) will consecutively be transmitted when there is no HDLC data to be transmitted during the data link activating.

Four interrupt sources can be derived from this block.

1. When the FIFO is empty or the data in the FIFO is less than the setting in the LINT[6:0] (b6~0, T1/J1-036H), the BLFILL (b5, T1/J1-038H) will be set for indication. A transition from logic 0 to 1 on the BLFILL (b5, T1/J1-038H) will cause a logic 1 in the LFILLI (b0, T1/J1-038H). The interrupt on the $\overline{INT}$ pin will occur when the LFILLE (b0, T1/J1-037H) is enabled;

2. When the data in the FIFO reaches its maximum capacity - 128 bytes, the FULL (b6, T1/J1-038H) will be set for indication. A transition from logic 0 to 1 on the FULL (b6, T1/J1-038H) will cause a logic 1 in the FULLI (b3, T1/J1-038H). The interrupt on the $\overline{INT}$ pin will occur when the FULLE (b3, T1/J1-037H) is enabled;

3. When the FIFO has been filled with 128 bytes already and new data is still written to it, the FIFO will overflow and the OVRI (b2, T1/J1-038H) will be set for indication. The interrupt on the $\overline{INT}$ pin will occur when the OVRE (b2, T1/J1-037H) is enabled.

4. When the transmission is in process and it is out of data to be transmitted in the FIFO, the FIFO is underrun and the UDRI (b1, T1/J1-038H) will be set for indication. The interrupt on the $\overline{INT}$ pin will occur when the UDRE (b1, T1/J1-037H) is enabled.

3.17 BIT-ORIENTED MESSAGE TRANSMITTER (TBOM) - T1/J1 ONLY

The Bit Oriented Message (BOM) can only be transmitted in the ESF format in T1/J1 mode. The standard of the BOM is defined in the ANSI T1.403-1989. The Bit Oriented Message (BOM) of each framer operates independently.

The BOM pattern is '111111110XXXXXX0' which occupies the DL of the F-bit in the ESF format (refer to Table 4). The six 'X's represent the code that can be programmed in the BOC[5:0] (b5~0, T1/J1-05DH). When the BOC[5:0] (b5~0, T1/J1-05DH) are written with the bits other than the '111111', they will occupy the six 'X's' positions and the BOM will be transmitted.

If the BOM transmission is stopped by setting all ones in the BOC[5:0] (b5~0, T1/J1-05DH), a BOM disabled pattern will be transmitted automatically. In T1 mode, the pattern is 'FFFF'. In J1 mode, the pattern is 'FF7E'. The disable pattern should be repeated 16 times before the HDLC bits (refer to Chapter 3.16 HDLC Transmitter (THDLC)) are inserted in the DL bit. The transmission of the BOM takes priority over any other substitutions of the DL bit except for the Yellow alarm signal.

3.18 INBAND LOOPBACK CODE GENERATOR (IBCG) - T1/J1 ONLY

The Inband Loopback Code Generator can only transmit inband loopback code in a framed or unframed T1/J1 data stream. The Inband Loopback Code Generator of each framer operates independently.

The length and the content of the inband loopback code are programmed in the CL[1:0] (b1~0, T1/J1-046H) and the IBC[7:0] (b7~0, T1/J1-047H) respectively. The code can only be transmitted when the EN (b7, T1/J1-046H) is enabled. In framed mode, which is configured by the UF (b6, T1/J1-046H), the F-bit can be replaced by the Frame Alignment Pattern, DL and CRC-6 which are set in the Frame Generator block and the 24 channels are replaced with the inband loopback code. In unframed mode, which is configured by the UF (b6, T1/J1-046H), all 193 bits are replaced with the inband loopback code.

It is recommended that the setting of the EN (b7, T1/J1-046H) and the UF (b6, T1/J1-046H) should be the same.

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3.19 JITTER ATTENUATOR (RJAT/TJAT)

The Jitter Attenuator of each framer operates independently

3.19.1 E1 MODE

Two Jitter Attenuators are provided independently in the receive path and the transmit path.

The Jitter Attenuator integrates a FIFO and a DPLL. The smoothed clock output from the jitter attenuator is generated by adaptively dividing the 49.152MHz XCK according to the phase difference between the output smoothed clock and the input reference clock. The ratio between the frequency of the input reference clock and the frequency applied to the phase discriminator input is equal to the (N1 + 1) (the N1 is in b7~0, E1-021H for receive path and in b7~0, E1-025H for transmit path). The ratio between the frequency of the output smoothed clock and the frequency applied to the phase discriminator input is equal to the (N2 + 1) (the N2 is in b7~0, E1-022H for receive path and in b7~0, E1-026H for transmit path). The phase fluctuations of the input reference clock are attenuated by dividing the input reference clock and output smoothed clock by the (N1 + 1) and the (N2 + 1) respectively in the DPLL so that the frequency of the output smoothed clock is equal to the average frequency of the input reference clock. The phase fluctuations with a jitter frequency above 8.8 Hz are attenuated by 6 dB per octave when the N1 (b7~0, E1-021H for receive path and b7~0, E1-025H for transmit path) and the N2 (b7~0, E1-022H for receive path and b7~0, E1-026H for transmit path) are set to their default value. It will change when the N1 and the N2 are changed. Generally, when the N1 and the N2 increase, the curves of the Jitter Tolerance and Jitter Transfer in the graph will left-shift and when N1 and N2 decrease, they will right-shift. The phase fluctuations (wander) with frequency below 8.8 Hz are tracked by the output smoothed clock. The output smoothed clock is used to clock the data out of the FIFO.

The FIFO is 48 bits deep. If data is still written into the FIFO when the FIFO is already full, overflow will occur and the OVRI (b1, E1-020H for receive path and b1, E1-024H for transmit path) will indicate. If data is still read from the FIFO when the FIFO is already empty, under-run will occur and the UNDI (b0, E1-020H for receive path and b0, E1-024H for transmit path) will indicate. Thus, if the OVRE (b2, E1-023H for receive path and b2, E1-027H for transmit path) and the UNDE (b3, E1-023H for receive path and b3, E1-027H for transmit path) are set respectively, the interrupts on the $\overline{INT}$ pin will occur. The jitter attenuation can be limited by setting the LIMIT (b0, E1-023H for receive path and b0, E1-027H for transmit path) to keep the FIFO 1 UI away from being full or empty. Thus, the DPLL will track the jitter of the input reference clock by increasing or decreasing the frequency of the output smoothed clock to prevent the FIFO being empty or full. The FIFO can also self-center its read pointer by setting the CENT (b4, E1-023H for receive path and b4, E1-027H for transmit path). The FIFO can be set to be bypassed by the FIFOBYP (b7, E1-000H for receive path and b7, E1-002H for transmit path).

However, in the Transmit Clock Master mode, the TJAT should be bypassed.

3.19.1.1 Jitter Characteristics

Each Jitter Attenuator block provides excellent jitter tolerance and jitter attenuation while generating minimal residual jitter. It can accommodate up to 43 UIpp of input jitter at jitter frequencies above 9 Hz. For jitter frequencies below 9 Hz, which can be correctly called wander, the tolerance increases 20 dB per decade. In most applications the each Jitter Attenuator block will limit jitter tolerance at lower jitter frequencies only. For high frequency jitter, above 10 kHz for example, other factors such as clock and data recovery circuitry may limit jitter tolerance and must be considered. For low frequency wander, below 10 Hz for example, other factors such as slip buffer hysteresis may limit wander tolerance and must be considered. The Jitter Attenuator blocks meet the low frequency jitter tolerance requirements ITU-T Recommendation G.823.

The Jitter Attenuator exhibits negligible jitter gain for jitter frequencies below 9 Hz, and attenuates jitter at frequencies above 9 Hz by 20 dB per decade. In most applications the Jitter Attenuator blocks will determine jitter attenuation for higher jitter frequencies only. Wander, below 10 Hz for example, will essentially be passed unattenuated through the Jitter Attenuator. Jitter, above 10 Hz for example, will be attenuated as specified, however, outgoing jitter may be dominated by the generated residual jitter in cases where incoming jitter is insignificant. This generated residual jitter is directly related to the use of 24X (49.152 MHz) digital phase locked loop for transmit clock generation.

The Jitter Attenuator meets the jitter transfer requirements of ITU-T Recommendations G.737, G.738, G.739, and G.742.

3.19.1.2 Jitter Tolerance

Jitter tolerance is the maximum input phase jitter at a given jitter frequency that a device can accept without exceeding its linear operating range, or corrupting data. For the Jitter Attenuator, the input jitter tolerance is 43 UIpp with no frequency offset. The frequency offset is the difference between the frequency of XCK divided by 24 and that of the input reference clock.

Refer to Figure 65 for the Jitter Tolerance.

3.19.1.3 Jitter Transfer

The output jitter for jitter frequencies from 0 to 9 Hz is no more than 0.1 dB greater than the input jitter. Jitter frequencies above 9 Hz are attenuated at a level of 6 dB per octave, as shown in Figure 66.

3.19.1.4 Frequency Range

In the non-attenuating mode, that is, when the FIFO is within 1 UI of overrunning or under running, the tracking range is 1.963 to 2.133 MHz. The guaranteed linear operating range is 2.048 MHz ± 1278 Hz with no jitter or XCK frequency offset.

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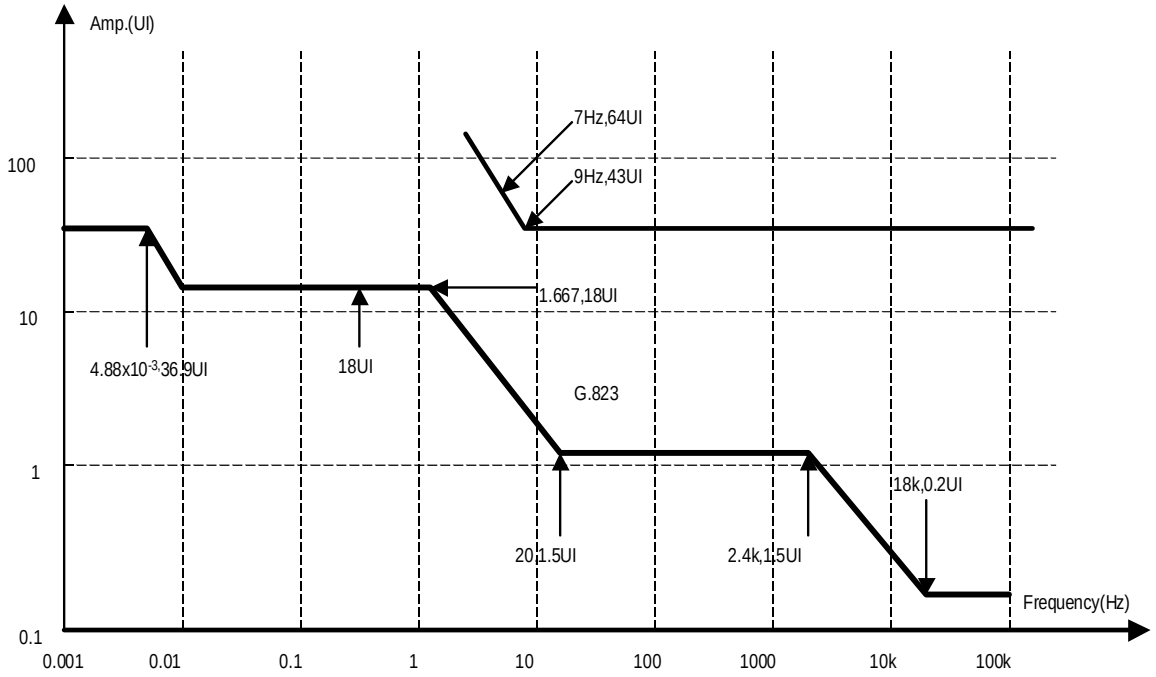


Figure 65. E1 Mode Jitter Tolerance (N1 = N2 = 2fH)

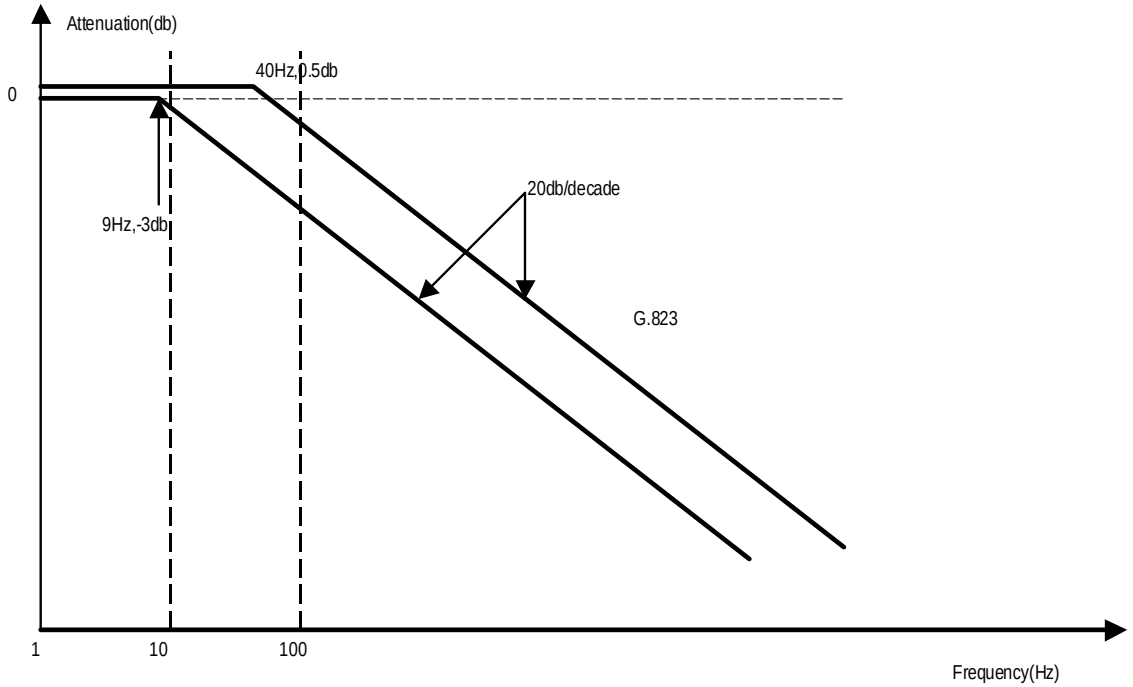


Figure 66. E1 Mode Jitter Transfer (N1 = N2 = 2fH)

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3.19.2 T1/J1 MODE

Two Jitter Attenuators are provided independently in the receive path and the transmit path.

The Jitter Attenuator integrates a FIFO and a DPLL. The smoothed clock output from the jitter attenuator is generated by adaptively dividing the 37.056 MHz XCK according to the phase difference between the output smoothed clock and the input reference clock. The ratio between the frequency of the input reference clock and the frequency applied to the phase discriminator input is equal to the (N1 + 1) (the N1 is in b7~0, T1/J1-011H for receive path and in b7~0, T1/J1-019H for transmit path). The ratio between the frequency of the output smoothed clock and the frequency applied to the phase discriminator input is equal to the (N2 + 1) (the N2 is in b7~0, T1/J1-012H for receive path and in b7~0, T1/J1-01AH for transmit path). The phase fluctuations of the input reference clock are attenuated by dividing the input reference clock and output smoothed clock by the (N1 + 1) and the (N2 + 1) respectively in the DPLL so that the frequency of the output smoothed clock is equal to the average frequency of the input reference clock. The phase fluctuations with a jitter frequency above 6.6 Hz are attenuated by 6 dB per octave when the N1 (b7~0, T1/J1-011H for receive path and b7~0, T1/J1-019H for transmit path) and the N2 (b7~0, T1/J1-012H for receive path and b7~0, T1/J1-01AH for transmit path) are in their default value. It will change when the N1 and the N2 are changed. Generally, when the N1 and the N2 increase, the curves of the Jitter Tolerance and Jitter Transfer in the graph will left-shift and When N1 and N2 decrease, they will right-shift. The phase fluctuations (wander) with frequency below 6.6 Hz are tracked by the output smoothed clock. The output smoothed clock is used to clock the data out of the FIFO.

The FIFO is 48 bits deep. If data is still written into the FIFO when the FIFO is already full, overflow will occur and the OVRI (b1, T1/J1-010H for receive path and b1, T1/J1-018H for transmit path) will indicate. If data is still read from the FIFO when the FIFO is already empty, underrun will occur and the UNDI (b0, T1/J1-010H for receive path and b0, T1/J1-018H for transmit path) will indicate. Thus, if the OVRE (b2, T1/J1-013H for receive path and b2, T1/J1-01BH for transmit path) and the UNDE (b3, T1/J1-013H for receive path and b3, T1/J1-01BH for transmit path) are set respectively, the interrupts on the $\overline{\text{INT}}$ pin may occur. The jitter attenuation can be limited by setting the LIMIT (b0, T1/J1-013H for receive path and b0, T1/J1-01BH for transmit path) to keep the FIFO 1 UI away from being full or empty,. Thus, the DPLL will track the jitter of the input reference clock by increasing or decreasing the frequency of the output smoothed clock to prevent the FIFO being empty or full. The FIFO can also self-center its read pointer by setting the CENT (b4, T1/J1-013H for receive path and b4, T1/J1-01BH for transmit path). The FIFO can be set to be bypassed by the FIFOBYP (b7, T1/J1-000H for receive path and b7, T1/J1-004H for transmit path).

However, in the Transmit Clock Master mode, the TJAT should be bypassed.

3.19.2.1 Jitter Characteristics

Each Jitter Attenuator block provides excellent jitter tolerance and jitter attenuation while generating minimal residual jitter. It can accommodate up to 45 UI of input jitter at jitter frequencies above 12 Hz. For jitter frequencies below 9 Hz, which can be correctly called wander, the tolerance increases 20 dB per decade. In most applications the each Jitter Attenuator block will limit jitter tolerance at lower jitter frequencies only. For high frequency jitter, above 10 kHz for example, other factors such as clock and data recovery circuitry may limit jitter tolerance and must be considered. For low frequency wander, below 10 Hz for example, other factors such as slip buffer hysteresis may limit wander tolerance and must be considered. The Jitter Attenuator blocks meet the low frequency jitter tolerance requirements AT&T TR 62411 for T1.

The Jitter Attenuator exhibits negligible jitter gain for jitter frequencies below 7 Hz, and attenuates jitter at frequencies above 7 Hz by 20 dB per decade. In most applications the Jitter Attenuator blocks will determine jitter attenuation for higher jitter frequencies only. Wander, below 10 Hz for example, will essentially be passed unattenuated through DJAT. Jitter, above 10 Hz for example, will be attenuated as specified, however, outgoing jitter may be dominated by the generated residual jitter in cases where incoming jitter is insignificant. This generated residual jitter is directly related to the use of 24X (37.056 MHz) digital phase locked loop for transmit clock generation.

The Jitter Attenuator meets the jitter transfer requirements of AT&T TR 62411. The block allows to meet the implied jitter attenuation requirements for a TE or NT1 given in ANSI Standard T1.408, and the implied jitter attenuation requirements for a type II customer interface given in ANSI T1.403.

3.19.2.2 Jitter Tolerance

Jitter tolerance is the maximum input phase jitter at a given jitter frequency that a device can accept without exceeding its linear operating range, or corrupting data. For the Jitter Attenuator, the input jitter tolerance is 48 UIpp with no frequency offset. The frequency offset is the difference between the frequency of XCK divided by 24 and that of the input reference clock.

Refer to Figure - 65 for the Jitter Tolerance.

3.19.2.3 Jitter Transfer

The output jitter for jitter frequencies from 0 to 7 Hz is no more than 0.1 dB greater than the input jitter. Jitter frequencies above 7 Hz are attenuated at a level of 6 dB per octave, as shown in Figure - 66.

3.19.2.4 Frequency Range

In the non-attenuating mode, that is, when the FIFO is within 1 UI of overrunning or under running, the tracking range is 1.48 to 1.608 MHz. The guaranteed linear operating range is 1.544 MHz ± 963 Hz (for T1) with no jitter or XCK frequency offset.

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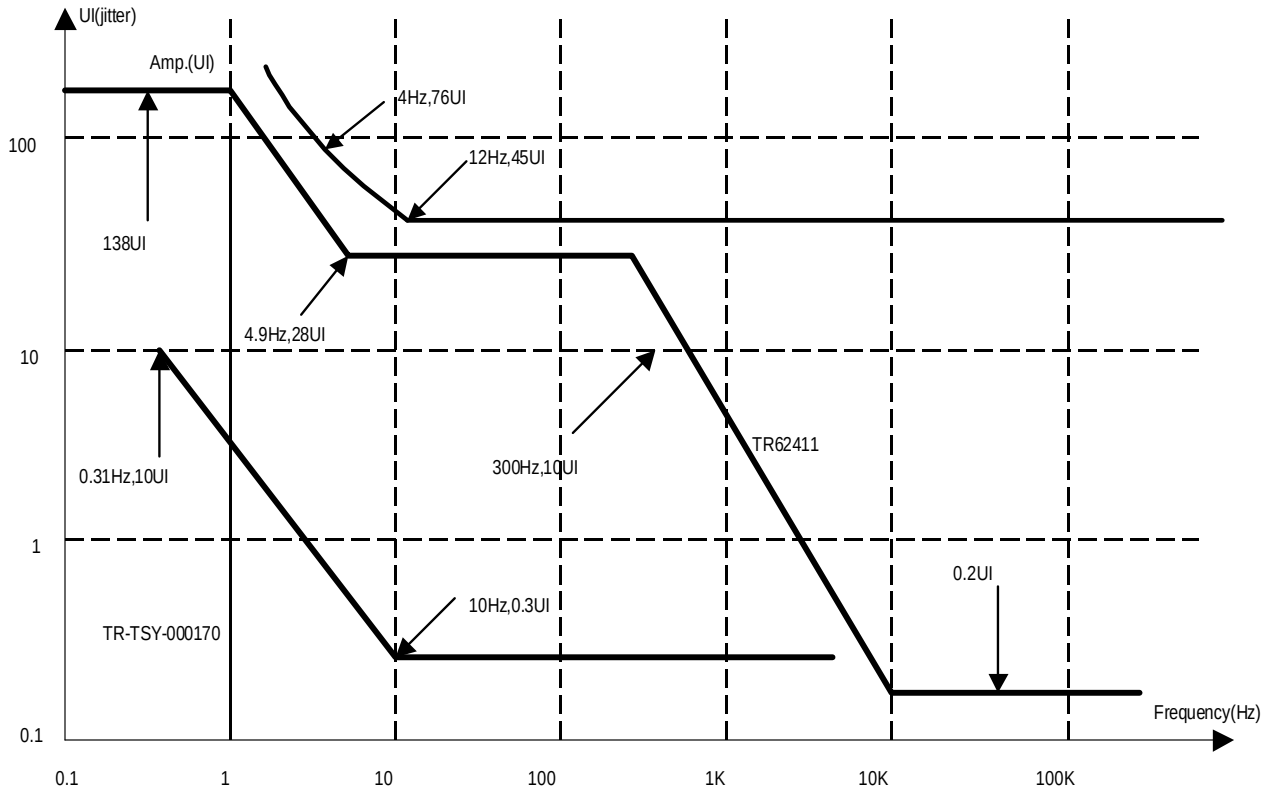


Figure 67. T1/J1 Mode Jitter Tolerance (N1 = N2 = 2fH)

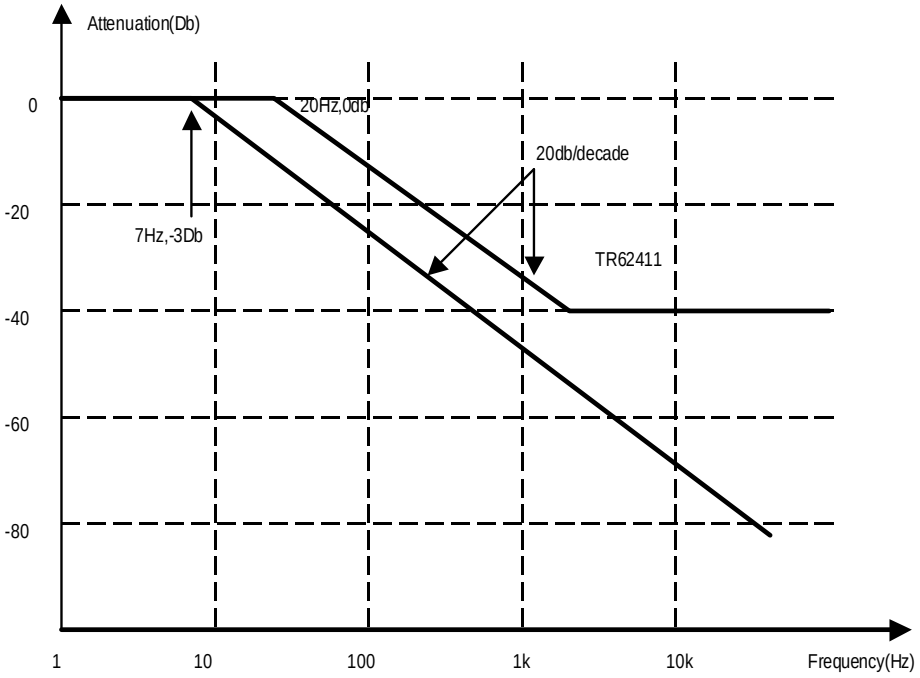


Figure 68. T1/J1 Mode Jitter Transfer (N1 = N2 = 2fH)

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3.20 TRANSMIT CLOCK

The Transmit Clock of each framer operates independently.

3.20.1 E1 MODE

The Transmit Clock helps the Transmit Jitter Attenuator to select the source of the input reference clock for the DPLL, and selects the clock source used to drive the clock to be output on the LTCKn pin. Refer to Figure 69 for details.

3.20.2 T1/J1 MODE

The Transmit Clock helps the Transmit Jitter Attenuator to select the source of the input reference clock for the DPLL, and selects the clock source used to drive the clock to be output on the LTCKn pin. Refer to Figure 69 for details.

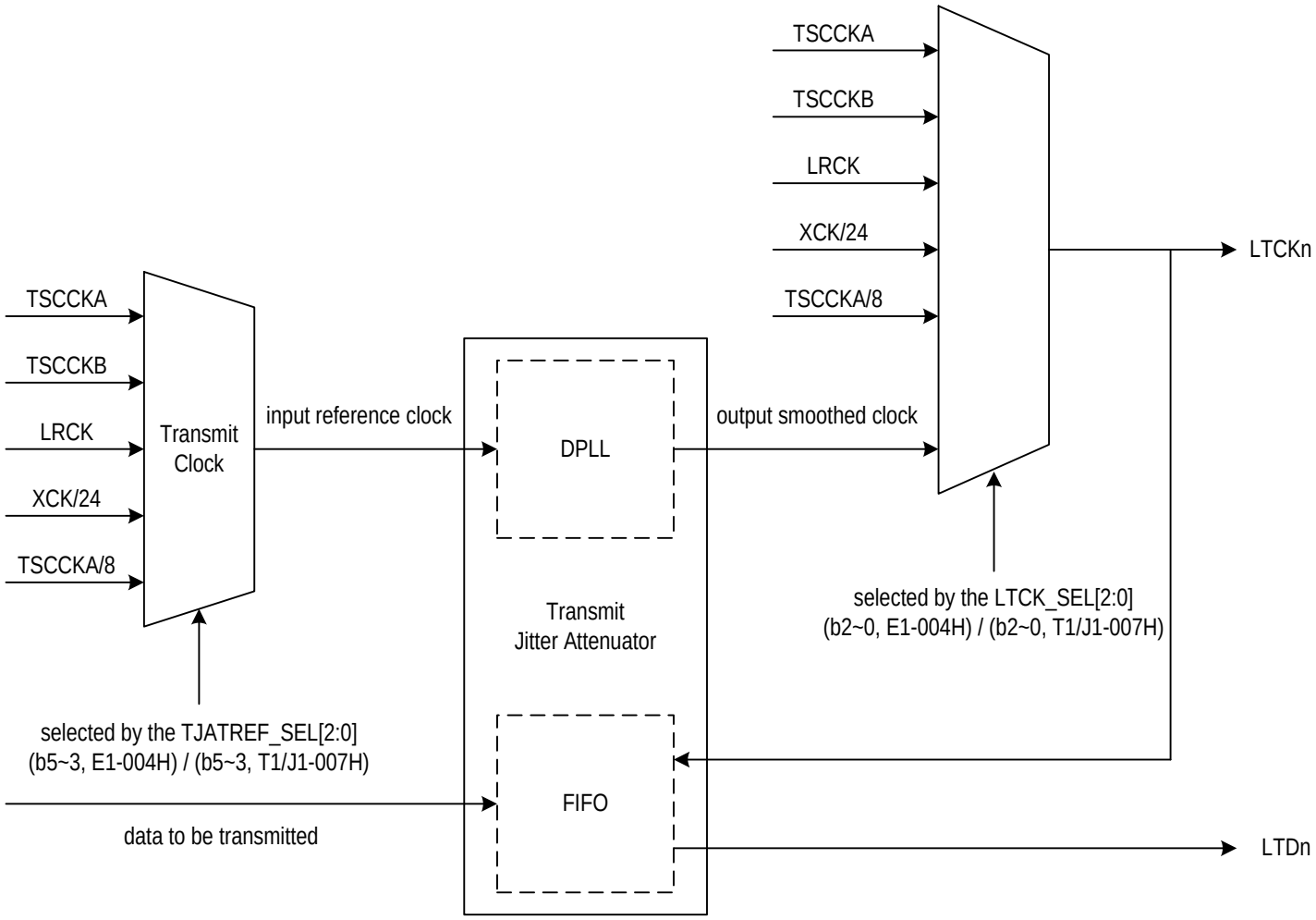


Figure 69. Transmit Clock Select

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3.21 LINE INTERFACE

3.21.1 E1 MODE

On the receive line interface, the received data on the LRDn pin is sampled on the active edge of LRCKn. The active edge of LRCKn is chosen by the RCKFALL (b7, E1-001H).

On the transmit line interface, the data to be transmitted on the LTDn pin is updated on the active edge of LTCKn. The active edge of LTCKn is chosen by the LTCKRISE (b0, E1-002H). All ones will be forced to transmit on the LTDn pin when the TAISEN (b6, E1-002H) is configured. All zeros will also be forced to transmitted when the TXDIS (b0, E1-007H) is configured.

3.21.2 T1/J1 MODE

On the receive line interface, the received data on the LRDn pin is sampled on the active edge of LRCKn. The active edge of LRCKn is chosen by the LRCKFALL (b2, T1/J1-003H).

On the transmit line interface, the data to be transmitted on the LTDn pin is updated on the active edge of LTCKn. The active edge of LTCKn is chosen by the LTCKRISE (b0, T1/J1-004H). All ones will be forced to transmitted on the LTDn pin when the TAISEN (b6, T1/J1-004H) is configured. All zeros will also be forced to transmit when the TXDIS (b0, T1/J1-00AH) is configured.

3.22 INTERRUPT SUMMARY

3.22.1 E1 MODE

When the $\overline{INT}$ pin asserts low, which means at least one interrupt has occurred in the device, reading the INT[8:1] (b7~0, E1-00BH) will find in which framer the interrupt occurs. After reading the INT register, the interrupt source bits from the interrupting framer are read. The Interrupt Source bits (PMON [b7, E1-005H], FRMG [b6, E1-005H], FRMP [b5, E1-005H], PRGD [b4, E1-005H], ELSB [b3, E1-005H], RHDLC#1 [b2, E1-005H], RHDLC#2 [b1, E1-005H], RHDLC#3 [b0, E1-005H], TRSI [b7, E1-006H], TJAT [b5, E1-006H], RJAT [b4, E1-006H], THDLC#1 [b3, E1-006H], THDLC#2 [b2, E1-006H], THDLC#3 [b1, E1-006H] and RCRB [b0, E1-006H]) will be logic 1 if there are interrupts in the corresponding block. To find the eventual interrupt sources, the interrupt Indication and Status bits in the block are polled if their Interrupt Enable bits are enabled. Then the sources are served after they are found.

3.22.2 T1/J1 MODE

When the $\overline{INT}$ pin asserts low, which means at least one interrupt has occurred in the device, reading the INT[8:1] (b7~0, T1/J1-00EH) will find that in which framer the interrupt occurs. After reading the INT register, the interrupt source bits from the interrupting framer are read. The Interrupt Source bits (PMON [b7, T1/J1-008H], IBCD [b6, T1/J1-008H], FRMP [b5, T1/J1-008H], PRGD [b4, T1/J1-008H], ELSB [b3, T1/J1-008H], RHDLC#1 [b2, T1/J1-008H], RBOM [b1, T1/J1-008H], ALMD [b0, T1/J1-008H], RHDLC#2 [b7, T1/J1-009H], TJAT [b5, T1/J1-009H], RJAT [b4, T1/J1-009H], THDLC#1 [b3, T1/J1-009H], THDLC#2 [b2, T1/J1-009H] and RCRB [b0, T1/J1-009H]) will be logic 1 if there are interrupts in the corresponding block. To find the eventual interrupt sources, the interrupt Indication and Status bits in the block are polled if their Interrupt Enable bits are enabled. Then the sources are served after they are found.

However, another Interrupt Source bit PRTY (b6, T1/J1-009H) is provided to route to the pending parity error.

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3.23 LOOPBACK MODE

There are three diagnostic loopback modes: Line Loopback, Digital Loopback and Payload Loopback are provided in this device.

3.23.1 LINE LOOPBACK

By programming the LINEB (b4, E1-007H / b4, T1/J1-00AH), each framer can be set in the Line Loopback mode. In this configuration, the jitter-attenuated clock and data from the Receive Jitter Attenuator are looped internally to the Line Transmit Clock and Data (LTDn and LTCKn). However, the Receive Jitter Attenuator can be bypassed if required. The received data stream is still output to the system side while the data stream input from the system side is ignored. Figure 70 shows the process.

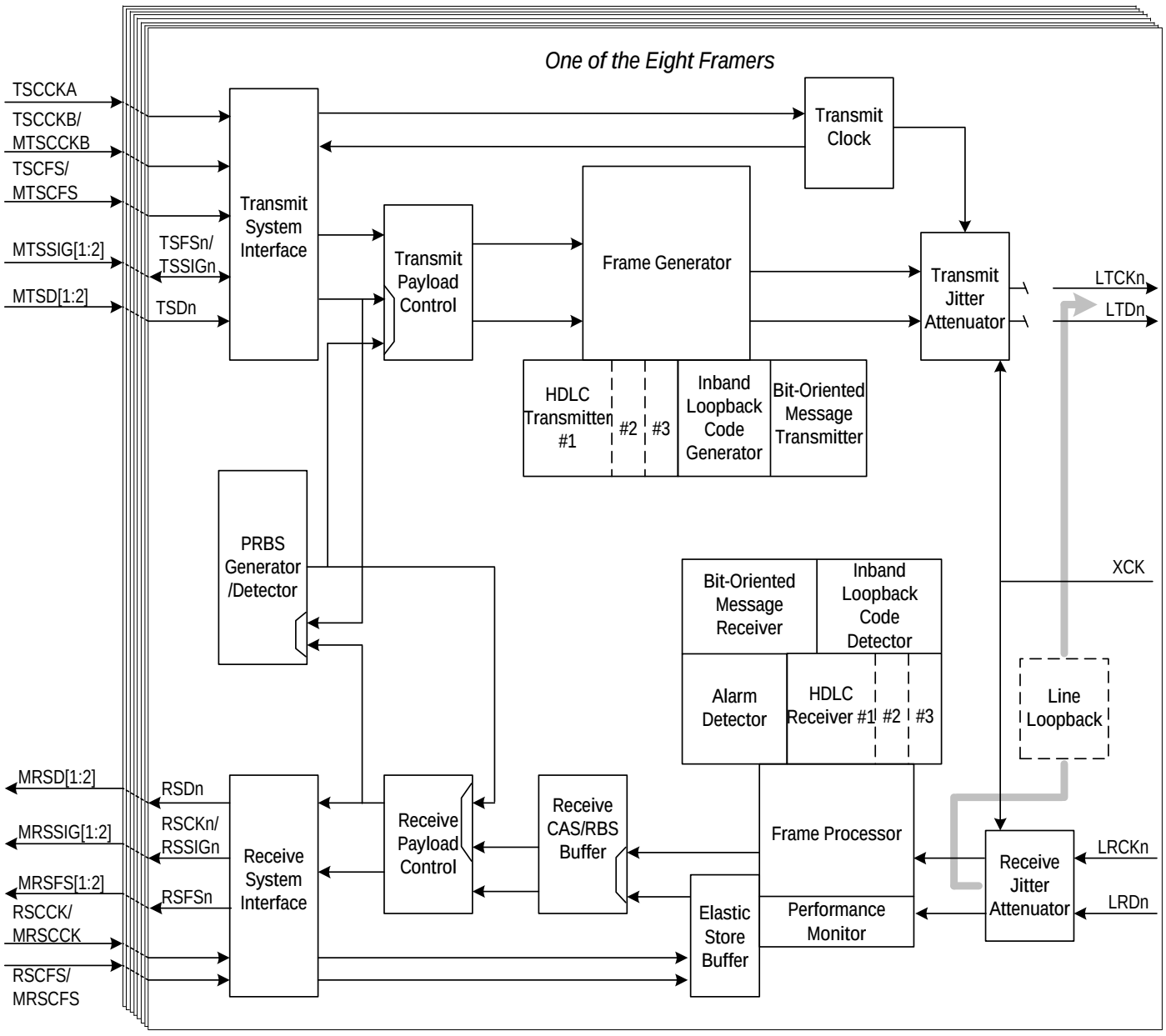


Figure 70. Line Loopback

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3.23.2 DIGITAL LOOPBACK

By programming the DDLB (b2, E1-007H / b2, T1/J1-00AH), each framer can be set in the Digital Loopback mode. In this configuration, the data to be transmitted on LTCKn and LTDn is looped internally to the Line Receive Clock and Data (LRDn and LRCKn). The data stream to be transmitted is still output to the line side while the data stream received from the line side is ignored. Figure 71 shows the process.

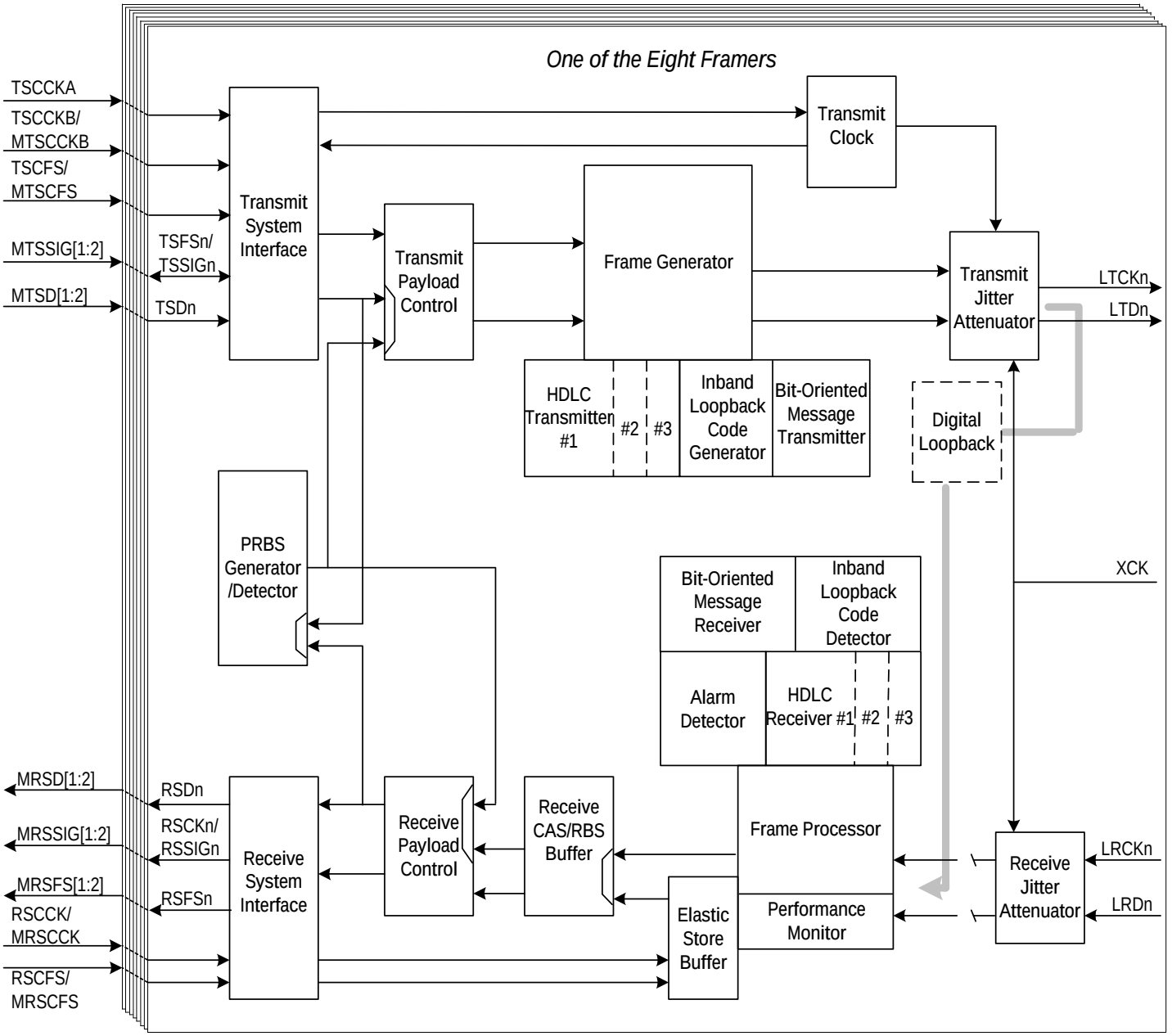


Figure 71. Digital Loopback

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3.23.3 PAYLOAD LOOPBACK

By programming the LOOP (b2, E1-TPLC-indirect registers-20~3FH / b2, T1/J1-TPLC-indirect registers-10~18H) (the PCCE [b0, E1-060H / b0, T1/J1-030H] in the TPLC must be logic 1), each framer can be set in the Payload Loopback mode. When the Receive Clock Master modes are enabled, the Elastic Store is used to align the line received data to the frame to be transmitted. When the Receive Clock Slave modes are enabled, the Elastic Store is unavailable to implement the payload loopbacks, and loopback functionality is provided only when the Transmit System Interfaces are also in a Transmit Clock Slave mode, and the received and transmitting clocks and frame alignment are identical (RSCCK = TSCCKB, RSCFS = TSCFS). Thus, the selected time slot/channel in the transmit path will be overwritten by the corresponding received time slot/channel. The remaining time slots/channels in the transmit path are intact. Figure 72 shows the process.

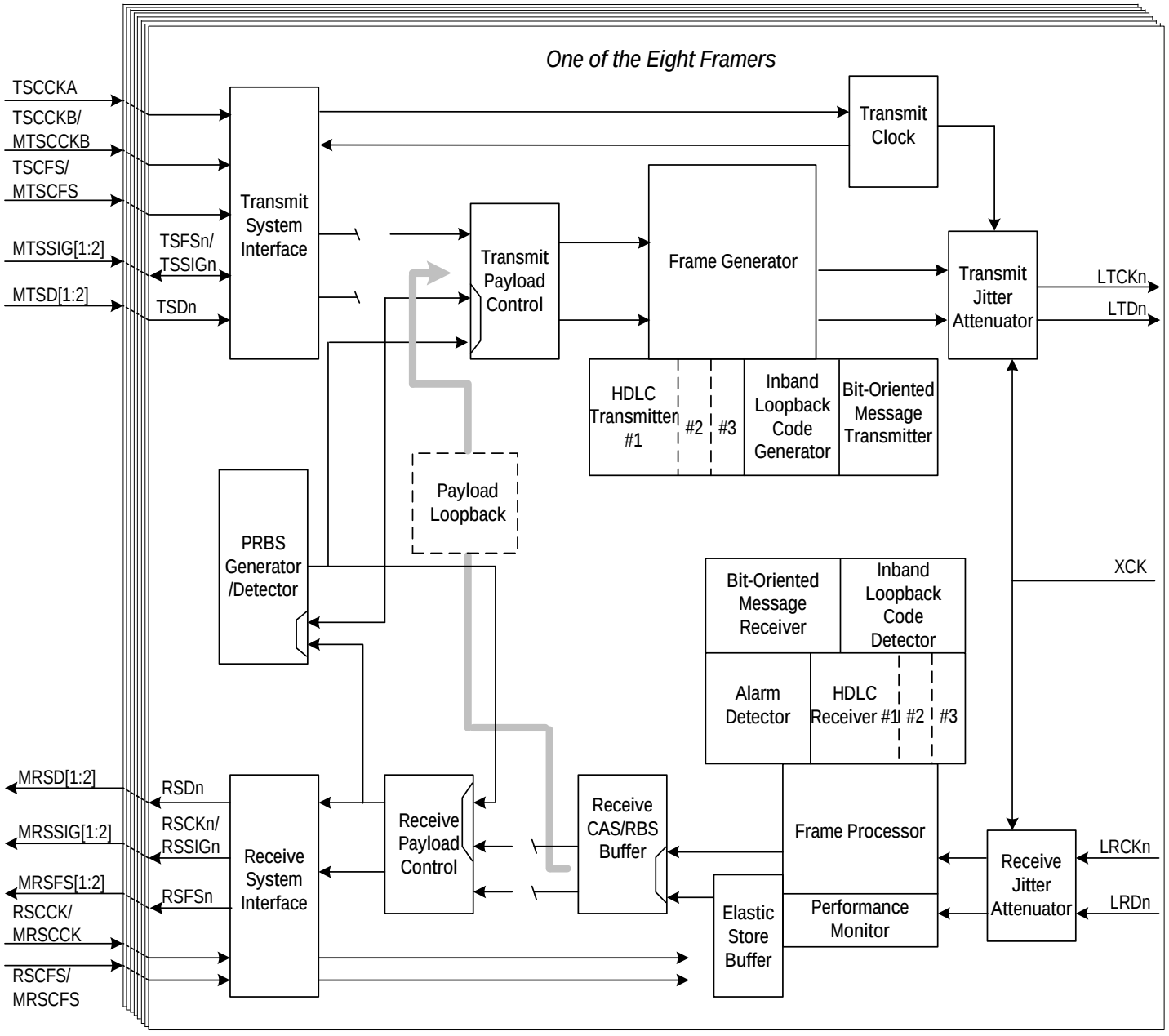


Figure 72. Payload Loopback

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3.24 CLOCK MONITOR

The transition from low to high of the Crystal Clock (XCK), the Transmit Side System Common Clock #A (TSCCKA), the Transmit Side System Common Clock #B (TSCCKB), the Receive Side System Common Clock (RSCCK) and the Line Receive Clock (LRCK) are monitored and are reported by the XCK (b4, E1-00DH / b4, T1/J1-027H), the TSCCKB (b3, E1-00DH / b3, T1/J1-027H), the TSCCKA (b2, E1-00DH / b2, T1/J1-027H), the RSCCK (b1, E1-00DH / b1, T1/J1-027H) and the LRCK (b0, E1-00DH / b0, T1/J1-027H) respectively.

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4 OPERATION

4.1 E1 MODE

4.1.1 DEFAULT SETTING

When the device is powered-up, all the registers contain their default values.

Any of the eight framers can be reset anytime when the RESET (b0, E1-00AH / b0, T1/J1-00DH) in its framer is set. The device can also be reset anytime when the $\overline{RST}$ pin is low for at least 100 ns.

After the hardware reset, the IDT82V2108 will default to the following settings:

- Mode: the default operation mode of the device is T1 mode. When the E1 mode is desired, the TEMODE (b0, 400H) must be set to logic 0.
- Receive Path: the default setting of each block in the receive path is illustrated in Table 39.
- Transmit Path: the default setting of each block in the transmit path is illustrated in Table 40.

Table 39: Default Setting in Receive Path in E1 Mode

Function Block	Default Setting Description
Line Interface	- LRDn inputs Non-Return to Zero (NRZ) data and is sampled on the rising edge of LRCKn. - The RJAT Clock Divisors (N1, N2) are set to '2F'.
Frame Processor	- Basic Frame per G.704 with CRC Multi-Frame is enabled. - Channel Associated Signaling is enabled.
HDLC Receiver #1, #2, #3	- RHDLCs are disabled.
Receive System Interface	- In the Receive Clock Slave External Signaling Mode. - The data on the RSDn, RSSIGn pins is updated on the rising edge of RSCCK. - RSCFS indicates Basic Frame Alignment. - The RSDn, RSSIGn, RSFSn pins are held in high-impedance state.
PRGD	- The PRGD is configured to monitor the extracted data patterns in Frame 1.

Table 40: Default Setting in Transmit Path in E1 Mode

Function Block	Default Setting Description
PRGD	- The PRGD is configured to insert test patterns to Frame 1.
Transmit System Interface	- In the Transmit Clock Slave External Signaling Mode. - The data on the TSDn and TSSIGn pins is sampled on the rising edge of TSCCKB.
Frame Generator	- CRC Multi-Frame is disabled. - Channel Associated Signaling is enabled.
HDLC Transmitter #1, #2, #3	- THDLCs are disabled.
Line Interface	- LTDn outputs Non-Return to Zero (NRZ) data and is updated on the falling edge of LTCKn. - TJAT Clock Divisors (N1, N2) are set to '2F'. - Digital jitter attenuation is enabled. The PLL is synchronized to the TSCCKB clock. The smoothed clock output from the PLL is selected as LTCKn.

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4.1.2 VARIOUS OPERATION MODES CONFIGURATION

Five operation modes can be set in the receive path and four operation modes can be set in the transmit path. In each operation mode, the configurations in Table 41 and Table 42 are illustrated for reference.

Table 41: Various Operation Modes in Receive Path for Reference

Mode	Register [1]	Value (from Bit7 to Bit0)	Description [2]
Receive Clock Slave RSCK Reference Mode	001H	00000000	In the Receive Clock Slave RSCK Reference mode. RSCK is 8 KHZ.
	00EH	00001000	The output on the RSFSn pin is determined by the ROHM, BRXSMFP, BRCMFP and ALTIFP.
	010H	00100001	In the Receive Clock Slave mode. The FE and DE are both 0. The receive backplane rate is 2.048 Mbit/s.
	011H	00100000	RSCFS is used.
	012H	00000001	Enable the normal operation of the RSDn pin.
Receive Clock Slave External Signaling Mode	001H	01000000	In the Receive Clock Slave External Signaling mode.
	00EH	00001000	The output on the RSFSn pin is determined by the ROHM, BRXSMFP, BRCMFP and ALTIFP.
	010H	00100001	In the Receive Clock Slave mode. The FE and DE are both 0. The receive backplane rate is 2.048 Mbit/s.
	011H	00100000	RSCFS is used.
	012H	00000001	Enable the normal operation of the RSDn and RSSIGn pins.
Receive Clock Master Full E1	010H	00001001	In the Receive Clock Master Full E1 Mode. The FE is logic 1 and the DE is logic 0.
	011H	00000000	RSCFS is un-used.
	012H	00000001	Enable the normal operation of the RSDn pin.
Receive Clock Master Fractional E1 Mode	010H	10001001	In the Receive Clock Master Nx64K Mode. The FE is logic 1 and the DE is logic 0.
	011H	00000000	RSCFS is un-used.
	012H	00000001	Enable the normal operation of the RSDn pin.
	05CH	00000011	Enable the Receive Payload Control.
	20H - 3FH (RPLC indirect registers)	01000000	The code in the DTRK[7:0] replaces the data output on the RSDn pin in the corresponding channel.
Receive Multiplexed Mode	001H	01001000	Multiplex the data stream of these four framers to the multiplexed bus 1.
	081H	01001000	
	101H	01001000	
	181H	01001000	
	201H	01011000	Multiplex the data stream of these four framers to the multiplexed bus 2.
	281H	01011000	
	301H	01011000	
	381H	01011000	
	010H	00111011	In Receive Multiplexed mode. The receive backplane rate is 8.192Mbit/s. The FE is logic 1 and the DE is logic 1.
	090H	00111011	
	110H	00111011	
	190H	00111011	
	210H	00111011	
	290H	00111011	
	310H	00111011	
	390H	00111011	

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Table 41: Various Operation Modes in Receive Path for Reference (Continued)

Mode	Register [1]	Value (from Bit7 to Bit0)	Description [2]
Receive Multi-plexed Mode (Continued)	011H	00100000	The MRSCFS is used.
	091H	00100000	
	111H	00100000	
	191H	00100000	
	211H	00100000	
	291H	00100000	
	311H	00100000	
	391H	00100000	
	012H	00000001	Enable the normal operation of the MRSD and MRSSIG pins.
	092H	00000001	
	112H	00000001	
	192H	00000001	
	212H	00000001	
	292H	00000001	
	312H	00000001	
	392H	00000001	
	013H	00000000	TSOFF[6:0] = 0. The time slot offset is 0.
	093H	00000001	TSOFF[6:0] = 1. The time slot offset is 1.
	113H	00000010	TSOFF[6:0] = 2. The time slot offset is 2.
	193H	00000011	TSOFF[6:0] = 3. The time slot offset is 3.
	213H	00000000	TSOFF[6:0] = 0. The time slot offset is 0.
	293H	00000001	TSOFF[6:0] = 1. The time slot offset is 1.
	313H	00000010	TSOFF[6:0] = 2. The time slot offset is 2.
	393H	00000011	TSOFF[6:0] = 3. The time slot offset is 3.

Note:
1. In the 'Register' column, except for the Receive Multiplexed mode, the register position of the Framer 1 is listed to represent the set of the registers of eight framers. The other registers positions are tabulated in 'Register Map'. However, in Receive Multiplexed mode, the register positions of eight framers are all listed.
2. The 'Description' illustrates the fundamental function of the operation mode. The others can be configured as desired.

Table 42: Various Operation Modes in Transmit Path for Reference

Mode	Register [1]	Value (from Bit7 to Bit0)	Description [2]
Transmit Clock Slave External Signaling Mode	018H	00100001	In the Transmit Clock Slave mode. The FE is logic 0 and the DE is logic 0.
	003H	01000000	In the Transmit Clock Slave External Signaling mode.
	040H	01110000	Channel Associated Signaling (CAS) is enabled. The CRC Multi-Frame is generated.
	004H	00001111	TSCCKB is selected as TJAT input reference clock. Smoothed clock is selected as Line Transmit Clock (LTCK).
	027H	00010000	The FIFO is set to self-center its read pointer.
Transmit Clock Slave TSFS Enable Mode	018H	00100001	In the Transmit Clock Slave mode. The FE is logic 0 and the DE is logic 0.
	003H	00000000	In the Transmit Clock Slave TSFS Enable mode.
	040H	01110000	Channel Associated Signaling (CAS) is enabled. The CRC Multi-Frame is generated.
	004H	00001111	TSCCKB is selected as TJAT input reference clock. Smoothed clock is selected as Line Transmit Clock (LTCK).
	027H	00010000	The FIFO is set to self-center its read pointer.

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Table 42: Various Operation Modes in Transmit Path for Reference (Continued)

Mode	Register [1]	Value (from Bit7 to Bit0)	Description [2]
Transmit Clock Master Mode	018H	00011001	In the Transmit Clock Master Full E1 mode.
	040H	01110000	Channel Associated Signaling (CAS) is enabled. The CRC Multi-Frame is generated.
	004H	00100100	XCK/24 is selected as TJAT input reference clock. XCK/24 is selected as Line Transmit Clock (LTCK).
Transmit Multi-plexed Mode	003H	01000000	The data stream is taken from the multiplexed bus 1.
	083H	01010000	The data stream is taken from the multiplexed bus 2.
	103H	01000000	The data stream is taken from the multiplexed bus 1.
	183H	01010000	The data stream is taken from the multiplexed bus 2.
	203H	01000000	The data stream is taken from the multiplexed bus 1.
	283H	01010000	The data stream is taken from the multiplexed bus 2.
	303H	01000000	The data stream is taken from the multiplexed bus 1.
	383H	01010000	The data stream is taken from the multiplexed bus 2.
	018H	00110011	In the Transmit Multiplexed mode. The FE is logic 0 and the DE is logic 1.
	098H	00110011	
	118H	00110011	
	198H	00110011	
	218H	00110011	
	298H	00110011	
	318H	00110011	
	398H	00110011	
	01BH	00000000	TSOFF[6:0] = 0. The time slot offset is 0.
	09BH	00000000	
	11BH	00000001	TSOFF[6:0] = 1. The time slot offset is 1.
	19BH	00000001	
	21BH	00000010	TSOFF[6:0] = 2. The time slot offset is 2.
	29BH	00000010	
	31BH	00000011	TSOFF[6:0] = 3. The time slot offset is 3.
	39BH	00000011	
	040H	01110000	Channel Associated Signaling (CAS) is enabled. The CRC Multi-Frame is generated.
	0C0H	01110000	
	140H	01110000	
	1C0H	01110000	
	240H	01110000	
	2C0H	01110000	
	340H	01110000	
	3C0H	01110000	
	004H	00011101	TSCCKA is selected as TJAT input reference clock. Smoothed clock is selected as Line Transmit Clock (LTCK).
	084H	00011101	
	104H	00011101	
	184H	00011101	
	204H	00011101	
	284H	00011101	
	304H	00011101	
	384H	00011101	

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Table 42: Various Operation Modes in Transmit Path for Reference (Continued)

Mode	Register [1]	Value (from Bit7 to Bit0)	Description [2]
Transmit Multi-plexed Mode (Continued)	027H	00010000	The FIFO is set to self-center its read pointer.
	0A7H	00010000	
	127H	00010000	
	1A7H	00010000	
	227H	00010000	
	2A7H	00010000	
	327H	00010000	
	3A7H	00010000	

Note:
1. In the 'Register' column, except for the Transmit Multiplexed mode, the register position of the Framer 1 is listed to represent the set of the registers of eight framers. The other registers positions are tabulated in the 'Register Map'. However, in the Transmit Multiplexed mode, the registers positions of eight framers are all listed.
2. The 'Description' illustrates the fundamental function of the operation mode. The others can be configured as desired.

4.1.3 OPERATION EXAMPLE

In this chapter, some common operation examples are given for reference.

4.1.3.1 Using HDLC Receiver

Before using the HDLC Receiver, the TXCISEL (b3, E1-00AH) must be set to '0' to enable the HDLC data link position for receive path.

Since three HDLC Receive data links are integrated in one framer, one of the three HDLC Receive data links must be selected in the RHDLCSEL[1:0] (b7~6, E1-00AH). Then the HDLC data link can be configured to extract from even and/or odd frames, from any time slot, and from any bit. The following examples show how to select the HDLC Receiver data link positions:

a. Extract the HDLC data link from all bits of TS16 in HDLC Receive #1:

- set the TXCISEL (b3, E1-00AH) to '0';
- set the RHDLCSEL[1:0] (b7~6, E1-00AH) to '00';
- set the DL1_EVEN (b7, E1-028H) to '0';
- set the DL1_ODD (b6, E1-028H) to '0';
- set the TS16_EN (b5, E1-028H) to '1'.

b. Extract the HDLC data link from the Sa8 National bit in HDLC Receive #1:

- set the TXCISEL (b3, E1-00AH) to '0';
- set the RHDLCSEL[1:0] (b7~6, E1-00AH) to '00';
- set the DL1_EVEN (b7, E1-028H) to '0';
- set the DL1_ODD (b6, E1-028H) to '1';
- set the TS16_EN (b5, E1-028H) to '0';
- set the DL1_TS[4:0] (b4~0, E1-028H) to '00000';
- set the DL1_BIT[7:0] (b7~0, E1-029H) to '00000001'.

c. Extract the HDLC data link from all bits of TS20 of all frames in HDLC Receive #2:

- set the TXCISEL (b3, E1-00AH) to '0';
- set the RHDLCSEL[1:0] (b7~6, E1-00AH) to '01';
- set the DL2_EVEN (b7, E1-02AH) to '1';
- set the DL2_ODD (b6, E1-02AH) to '1';
- set the DL2_TS [4:0] (b4~0, E1-02AH) to '10100';
- set the DL2_BIT [7:0] (b7~0, E1-02BH) to '11111111'.

After setting the HDLC data link position properly, the selected HDLC Receiver should be enabled by setting the EN (b0, E1-048H) to logic 1. If needed, set the MEN (b3, E1-048H) and the MM (b2, E1-048H) to determine which Address Matching Mode to be used (refer to Chapter 5.2 Register Description for details). After setting these 3 bits, the RHDLC Primary Address Match register and the RHDLC Secondary Address Match register should be set to proper values. If the INTC[6:0] (b6~0, E1-049H) are set, whenever the number of bytes in the RHDLC FIFO exceeds the value set in the INTC[6:0] (b6~0, E1-049H), the INTR (b0, E1-04AH) will be set to logic 1. This interrupt will persist until the RHDLC FIFO becomes empty. Setting the INTE (b7, E1-049H) to logic 1 allows the internal interrupt status to be propagated to the $\overline{INT}$ output pin.

After setting these registers properly, the HDLC data can be received in a polled or interrupt driven mode.

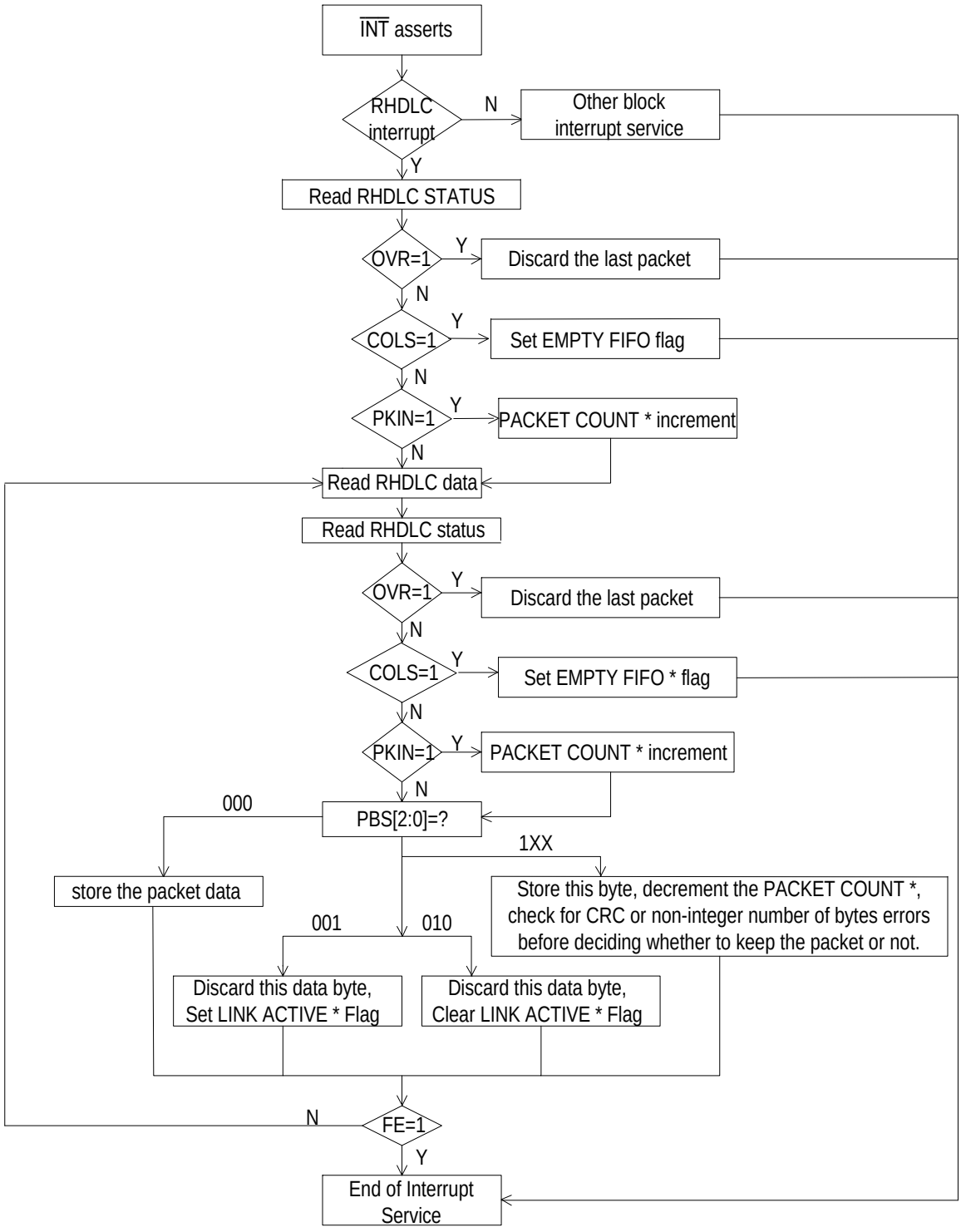
- Interrupt Driven Mode

When the INTE (b7, E1-049H) is set to logic 1, if the $\overline{INT}$ pin is asserted, the source of the interrupt should be first identified by reading the Interrupt ID register and Interrupt Source registers. If the source of the interrupt is HDLC Receive, the Interrupt Service procedure will be carried out as shown in Figure 73.

- Polling Mode

In polling mode, the operation procedure is the same as Figure 73, except that the entry of the service is from a local timer rather than an interrupt.

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Note:
* The PACKET COUNT, EMPTY FIFO and LINK ACTIVE are local software variable.

Figure 73. Interrupt Service in E1 Mode HDLC Receiver

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To summarize the procedure of using HDLC Receive, a complete example is shown in Table 43.

Table 43: Example for Using HDLC Receiver

Register	Value	Description
00AH	50H	RHDLC #2 is selected. The HDLC Receive is accessible to the CPU interface.
02AH	C4H	The TS4 of even frames and odd frames is selected.
02BH	FFH	All 8 bits are selected.
048H	0DH	The function of the RHDLC #2 is enabled. Set the address match mode.
049H	8FH	Set the INTE to '1'. When the number of bytes in the RHDLC FIFO exceeds 15, an interrupt is generated.
04CH	13H	The primary address is set to '13H'.
04DH	FFH	The secondary address is set to 'FFH'.
Then read the data status in register 04AH. Until a complete packet is received, read the data from register 04BH.		

4.1.3.2 Using HDLC Transmitter

Before using the HDLC Transmit, the TXCISEL (b3, E1-00AH) must be set to '1' to enable the HDLC data link position for transmit path.

Since three HDLC Transmit data links are integrated in one framer, one of the three HDLC Transmit data links must be selected in the THDLCSEL[1:0] (b5~4, E1-00AH). Then the HDLC data link can be configured to insert to even and/or odd frames, to any time slot, and to any bit. The following examples show how to select the HDLC Transmit data link positions:

a. Insert the HDLC data link to all bits of TS16 in HDLC Transmit #1:

- set the TXCISEL (b3, E1-00AH) to '1';
- set the THDLCSEL [1:0] (b5~4, E1-00AH) to '00';
- set the DL1_EVEN (b7, E1-028H) to '0';
- set the DL1_ODD (b6, E1-028H) to '0';
- set the TS16_EN (b5, E1-028H) to '1'.

b. Insert the HDLC data link to the Sa4-Sa8 National bits in HDLC Transmit #1:

- set the TXCISEL (b3, E1-00AH) to '1';
- set the THDLCSEL [1:0] (b5~4, E1-00AH) to '00';
- set the DL1_EVEN (b7, E1-028H) to '0';
- set the DL1_ODD (b6, E1-028H) to '1';
- set the TS16_EN (b5, E1-028H) to '0';
- set the DL1_TS[4:0] (b4~0, E1-028H) to '00000';
- set the DL1_BIT[7:0] (b7~0, E1-029H) to '00011111'.

c. Insert the HDLC data link to all bits of TS20 of all frames in HDLC Transmit #3:

- set the TXCISEL (b3, E1-00AH) to '1';
- set the THDLCSEL [1:0] (b5~4, E1-00AH) to '10';
- set the DL3_EVEN (b7, E1-02CH) to '1';
- set the DL3_ODD (b6, E1-02CH) to '1';
- set the DL3_TS [4:0] (b4~0, E1-02CH) to '10100';
- set the DL3_BIT [7:0] (b7~0, E1-02DH) to '11111111'.

After setting the HDLC data link position properly, the selected HDLC Transmit should be enabled by setting the EN (b0, E1-050H) to logic 1. The FIFOCLR (b6, E1-050H) should be set and then cleared to initialize the THDLC FIFO.

Set the CRC (b1, E1-050H) to logic 1 if the Frame Check Sequences (FCS) generation is desired. Set the FULLE (b3, E1-053H), OVRE (b2, E1-053H), UDRE (b1, E1-053H) and LFILLE (b0, E1-053H) to logic 1 if interrupt driven mode is used. Set THDLC Upper Transmit Threshold and THDLC Lower Transmit Threshold registers to the desired values. If a complete packet has been written into THDLC FIFO, the EOM (b3, E1-050H) should be set.

After setting these registers properly, the HDLC data can be transmitted in a polled or interrupt driven mode.

- Interrupt Driven Mode

Writing HDLC data to THDLC FIFO, the THDLC will transmit the HDLC data if the end of a packet was written or if the THDLC FIFO fill level reaches the Upper Transmit Threshold. The writing procedure is shown in Figure 74.

When the FULLE (b3, E1-053H), OVRE (b2, E1-053H), UDRE (b1, E1-053H) and LFILLE (b0, E1-053H) are set to logic 1, the source of the interrupt should be identified firstly by reading the Interrupt ID register and Interrupt Source registers if the $\overline{INT}$ pin is asserted. If the source of the interrupt is HDLC Transmit, the Interrupt Service procedure will be carried out as shown in Figure 75.

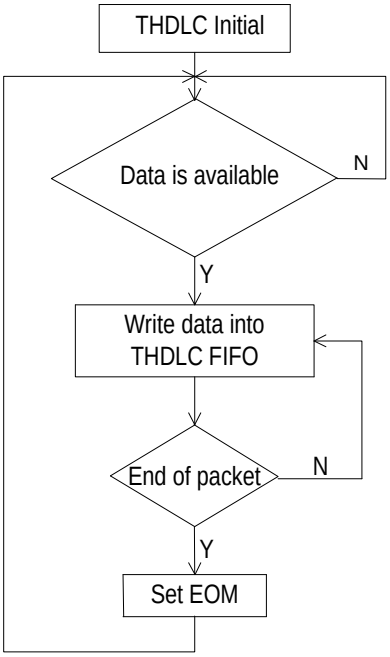
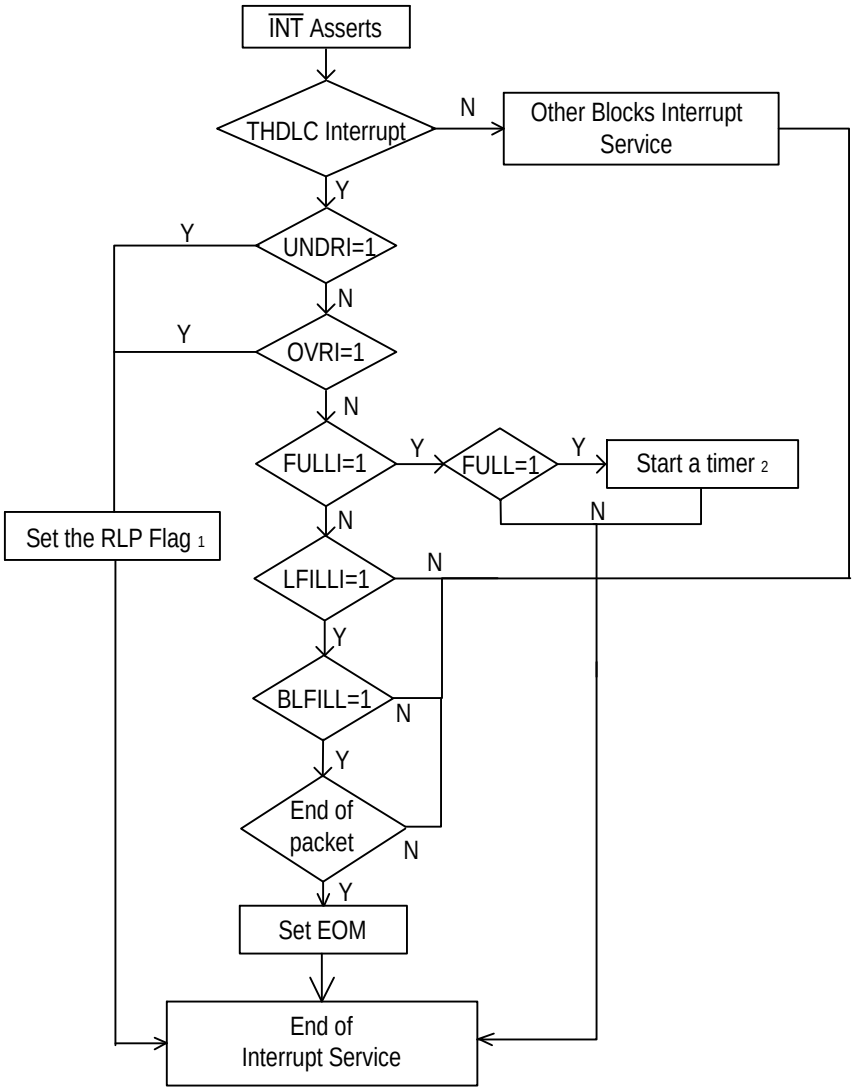


Figure 74. Writing Data to E1 Mode THDLC FIFO

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Note:
1. RLP-Retransmit the last packet, a local software variable.
2. A local timer to wait for a certain time until the Full = 0 or the BLFILL = 1.

Figure 75. Interrupt Service in E1 Mode HDLC Transmitter

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- Polling Mode

In the packet transmission polling mode, the FULLE (b3, E1-053H), OVRE (b2, E1-053H), UDRE (b1, E1-053H) and LFILLE (b0, E1-053H) should be set to logic 0. The THDLC Lower Transmit Threshold should be set to such a value that sufficient warning of an underrun is given. The procedure shown in Figure 76 should be followed.

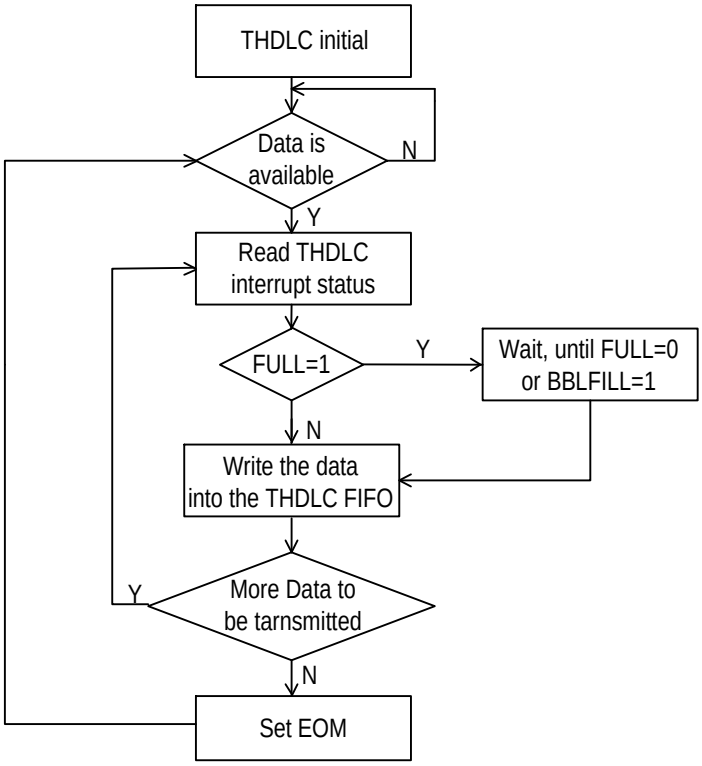


Figure 76. Polling Mode in E1 Mode HDLC Transmitter

To summarize the procedure of using HDLC Transmit, a complete example is shown in Table 44.

Table 44: Example for Using HDLC Transmitter

Register	Value	Description
00AH	58H	THDLC #2 is selected. The HDLC Transmit is accessible to the CPU interface.
02AH	C4H	TS4 of even frames and odd frames is selected.
02BH	FFH	All the 8 bits are selected.
050H	C3H	The function of the THDLC #2 is enabled. The FCS is enabled and the THDLC FIFO is reset.
050H	83H	
053H	0FH	Enable the THDLC Interrupt Enable bits.
055H	12H	Write data into THDLC FIFO.
055H	34H	
055H	56H	
055H	78H	
055H	9AH	
055H	BCH	
055H	DEH	
055H	FFH	
050H	8BH	End of packet and set the EOM to '1'.

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4.1.3.3 Using PRBS Generator / Detector

The IDT82V2108 provides one PRBS generator/detector block to generate and detect an enormous variety of pseudo-random and repetitive patterns to diagnose E1 data stream of all eight framers. The common test patterns are shown in tabular form in Table 45.

Table 45: Test Pattern in E1 Mode

Pseudo-Random Pattern Generation (the PS[b4, E1-070H] is logic 0)								
Pattern Type	TR [1]	LR [2]	IR#1 [3]	IR#2 [4]	IR#3 [5]	IR#4 [6]	TINV [7]	RINV [7]
2^3 - 1	00	02	FF	FF	FF	FF	0	0
2^4 - 1	00	03	FF	FF	FF	FF	0	0
2^5 - 1	01	04	FF	FF	FF	FF	0	0
2^6 - 1	04	05	FF	FF	FF	FF	0	0
2^7 - 1 (Fractional T1 LB Activate)	00	06	FF	FF	FF	FF	0	0
2^7 - 1(Fractional T1 LB Activate)	03	06	FF	FF	FF	FF	0	0
2^7 - 1	03	06	FF	FF	FF	FF	1	1
2^9 - 1 (O.153)	04	08	FF	FF	FF	FF	0	0
2^{10} - 1	02	09	FF	FF	FF	FF	0	0
2^{11} - 1 (O.152, O.153)	08	0A	FF	FF	FF	FF	0	0
2^{15} - 1 (O.151)	0D	0E	FF	FF	FF	FF	1	1
2^{17} - 1	02	10	FF	FF	FF	FF	0	0
2^{18} - 1	06	11	FF	FF	FF	FF	0	0
2^{20} - 1 (O.153)	02	13	FF	FF	FF	FF	0	0
2^{21} - 1	01	14	FF	FF	FF	FF	0	0
2^{22} - 1	00	15	FF	FF	FF	FF	0	0
2^{23} - 1 (O.151)	11	16	FF	FF	FF	FF	1	1
2^{25} - 1	02	18	FF	FF	FF	FF	0	0
2^{28} - 1	02	1B	FF	FF	FF	FF	0	0
2^{29} - 1	01	1C	FF	FF	FF	FF	0	0
2^{31} - 1	02	1E	FF	FF	FF	FF	0	0
Repetitive Pattern Generation (the PS [b4, E1-070H] is logic 1)								
Pattern Type	TR [1]	LR [2]	IR#1 [3]	IR#2 [4]	IR#3 [5]	IR#4 [6]	TINV [7]	RINV [7]
All ones	00	00	FF	FF	FF	FF	0	0
All zeros	00	00	FE	FF	FF	FF	0	0
Alternating ones/zeros	00	01	FE	FF	FF	FF	0	0
Double alternating ones/zeros	00	03	FC	FF	FF	FF	0	0
3 in 24	00	17	22	00	20	FF	0	0
1 in 16	00	0F	01	00	FF	FF	0	0
1 in 8	00	07	01	FF	FF	FF	0	0
1 in 4	00	03	F1	FF	FF	FF	0	0
DS1 Inband Loopback activate	00	04	F0	FF	FF	0F	0	0
DS1 Inband Loopback deactivate	00	02	FC	FF	FF	FF	0	0

Note:
1. TR - Tap Register. 2. LR - Shift Register Length Register. 3. IR#1 - PRGD Pattern Insertion #1 Register. 4. IR#2 - PRGD Pattern Insertion #2 Register. 5. IR#3 - PRGD Pattern Insertion #3 Register. 6. IR#4 - PRGD Pattern Insertion #4 Register. 7. TINV, RINV - contained in the PRGD Control register.

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The PRBS generator/detector block can be used to test E1 line transmit-receive integrity and system backplane integrity.

- Example For Testing E1 Line Transmit-Receive Integrity

To monitor the errors in Framer 2 without taking the entire E1 span off line, the following procedure should be done:

- Use the PRGD block to test Framer 2;
- Configure the PRGD register;
- Chose a desired set of time slots (for example TS2, TS4, TS5) for insertion/extraction of PRGD test data;
- Set the far end of the line to loop back at least the selected time slots;
- Monitor the E1 line transmit-receive integrity.

To realize the above function, the configuration in Table 46 to Table 48 should be set.

Table 46 is the configuration for PRGD and loopback. Table 47 shows the process to initialize the TPLC. Table 48 shows the process to initialize the RPLC.

Table 46: Setting of PRGD

Register	Value	Description
00CH	20H	Select Framer 2 to be tested by the PRGD block. The PRGD pattern is inserted in the TPLC and detected in the RPLC.
070H	82H	Set Pattern Detector registers as error counter register. Enable automatic resynchronization.
072H	18H	Set the pattern length.
073H	02H	Set the feedback tap position.
078H	FFH	Set the Pattern Insertion registers.
07BH	FFH	Load the data in the Pattern Insertion registers to generate the pattern.
087H	04H	Set diagnostic digital loopback mode.
0E0H	01H	Enable the TPLC indirect registers to be accessible.
0DCH	01H	Enable the RPLC indirect registers to be accessible.

Table 47: Initialization of TPLC

Register	Value
0E3H	00H
0E2H	20H
0E3H	00H
0E2H	21H
0E3H	00H
0E2H	22H
0E3H	00H
0E2H	23H
0E3H	00H
0E2H	24H
0E3H	00H

Table 47: Initialization of TPLC (Continued)

Register	Value
0E2H	25H
0E3H	00H
0E2H	26H
0E3H	00H
0E2H	27H
0E3H	00H
0E2H	28H
0E3H	00H
0E2H	29H
0E3H	00H
0E2H	2AH
0E3H	00H
0E2H	2BH
0E3H	00H
0E2H	2CH
0E3H	00H
0E2H	2DH
0E3H	00H
0E2H	2EH
0E3H	00H
0E2H	2FH
0E3H	00H
0E2H	30H
0E3H	00H
0E2H	31H
0E3H	00H
0E2H	32H
0E3H	00H
0E2H	33H
0E3H	00H
0E2H	34H
0E3H	00H
0E2H	35H
0E3H	00H
0E2H	36H
0E3H	00H
0E2H	37H
0E3H	00H
0E2H	38H
0E3H	00H
0E2H	39H
0E3H	00H
0E2H	3AH
0E3H	00H
0E2H	3BH
0E3H	00H
0E2H	3CH

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Table 47: Initialization of TPLC (Continued)

Register	Value
0E3H	00H
0E2H	3DH
0E3H	00H
0E2H	3EH
0E3H	00H
0E2H	3FH
0E3H	00H
0E2H	60H
0E3H	00H
0E2H	61H
0E3H	00H
0E2H	62H
0E3H	00H
0E2H	63H
0E3H	00H
0E2H	64H
0E3H	00H
0E2H	65H
0E3H	00H
0E2H	66H
0E3H	00H
0E2H	67H
0E3H	00H
0E2H	68H
0E3H	00H
0E2H	69H
0E3H	00H
0E2H	6AH
0E3H	00H
0E2H	6BH
0E3H	00H
0E2H	6CH
0E3H	00H
0E2H	6DH
0E3H	00H
0E2H	6EH
0E3H	00H
0E2H	6FH
0E3H	00H
0E2H	70H
0E3H	00H
0E2H	71H
0E3H	00H
0E2H	72H
0E3H	00H
0E2H	73H
0E3H	00H

Table 47: Initialization of TPLC (Continued)

Register	Value
0E2H	74H
0E3H	00H
0E2H	75H
0E3H	00H
0E2H	76H
0E3H	00H
0E2H	77H
0E3H	00H
0E2H	78H
0E3H	00H
0E2H	79H
0E3H	00H
0E2H	7AH
0E3H	00H
0E2H	7BH
0E3H	00H
0E2H	7CH
0E3H	00H
0E2H	7DH
0E3H	00H
0E2H	7EH
0E3H	00H
0E2H	7FH

Then set the TEST in TPLC Payload Control register for TS2, TS4 and TS5. The process is:

Register	Value	Description
0E3H	08H	Set the TEST in TPLC Payload Control register for TS2.
0E2H	22H	
0E3H	08H	Set the TEST in TPLC Payload Control register for TS4.
0E2H	24H	
0E3H	08H	Set the TEST in TPLC Payload Control register for TS5.
0E2H	25H	

Table 48: Initialization of RPLC

Register	Value
0DFH	00H
0DEH	20H
0DFH	00H
0DEH	21H
0DFH	00H
0DEH	22H
0DFH	00H
0DEH	23H

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Table 48: Initialization of RPLC (Continued)

Register	Value
0DFH	00H
0DEH	24H
0DFH	00H
0DEH	25H
0DFH	00H
0DEH	26H
0DFH	00H
0DEH	27H
0DFH	00H
0DEH	28H
0DFH	00H
0DEH	29H
0DFH	00H
0DEH	2AH
0DFH	00H
0DEH	2BH
0DFH	00H
0DEH	2CH
0DFH	00H
0DEH	2DH
0DFH	00H
0DEH	2EH
0DFH	00H
0DEH	2FH
0DFH	00H
0DEH	30H
0DFH	00H
0DEH	31H
0DFH	00H
0DEH	32H
0DFH	00H
0DEH	33H
0DFH	00H
0DEH	34H
0DFH	00H
0DEH	35H
0DFH	00H
0DEH	36H
0DFH	00H
0DEH	37H
0DFH	00H
0DEH	38H
0DFH	00H
0DEH	39H
0DFH	00H
0DEH	3AH
0DFH	00H

Table 48: Initialization of RPLC (Continued)

Register	Value
0DEH	3BH
0DFH	00H
0DEH	3CH
0DFH	00H
0DEH	3DH
0DFH	00H
0DEH	3EH
0DFH	00H
0DEH	3FH

Then set the TEST in RPLC Payload Control register for TS2, TS4 and TS5. The process is:

Register	Value	Description
0DFH	80H	Set the TEST in RPLC Payload Control register for TS2.
0DEH	22H	
0DFH	80H	Set the TEST in RPLC Payload Control register for TS4.
0DEH	24H	
0DFH	80H	Set the TEST in RPLC Payload Control register for TS5.
0DEH	25H	

After the above settings, read the PRGD Interrupt Enable/Status (071H) register twice. If the SYNCV (b4, E1-071H) is logic 1 and the BEI (b2, E1-071H) is logic 0, the pattern detector is in synchronization state.

Then insert errors into this link. Here suppose to insert 3 errors, then the configuration is shown in Table 49.

Table 49: Error Insertion

Register	Value
074H	08H
074H	00H
074H	08H
074H	00H
074H	08H
074H	00H

Then write 00H into the 07CH register to update the error counter registers. Then read the registers from 07CH to 07FH to check the error numbers.

- Example For Testing E1 System Backplane Integrity

To test the E1 system backplane integrity, the RXPATGEN (b2, E1-00CH) should be set to logic 1 and the other registers are set as above. Then the PRGD can be used to test the system backplane integrity.

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4.1.3.4 Using Payload Control and Receive CAS/RBS Buffer

Before using the Receive/Transmit Payload Control and Receive CAS/RBS Buffer, the indirect registers of these blocks must be initialized to eliminate erroneous control data. The PCCE (b0, E1-05CH & b0, E1-060H & b0, E1-064H) of these blocks must be set to logic 1 to enable these blocks.

Then the BUSY (b7, E1-05DH & b7, E1-061H & b7, E1-065H) must be checked before a new access request to the RPLC, TPLC and RCRB indirect registers. When the BUSY is logic 0, the new reading and writing access operations can be performed.

Figure 77 shows the writing sequence of the RPLC, TPLC and RCRB indirect registers. Figure 78 shows the reading sequence of the RPLC, TPLC and RCRB indirect registers.

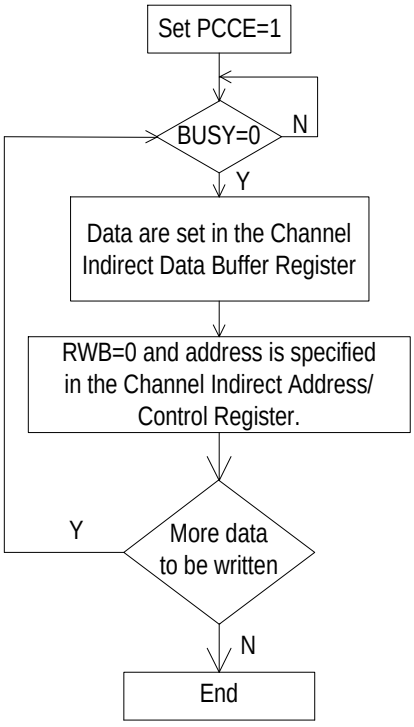


Figure 77. Writing Sequence of Indirect Register in E1 Mode

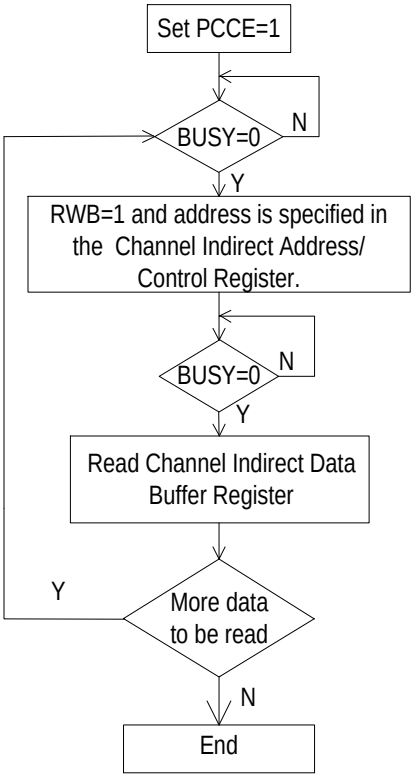


Figure 78. Reading Sequence of Indirect Register in E1 Mode

4.1.3.5 Using TJAT / Timing Option

In different operation modes, the Timing Options and Clock Divisor Control registers can be set as the follows:

- Transmit Clock Slave Mode (System Backplane Rate: 2.048 Mbit/s)

TSCCKA or TSCCKB is selected as the TJAT DPLL input reference clock. TSCCKA and TSCCKB are both equal to 2.048 M. The N1 (b7~0, E1-025H) and N2 (b7~0, E1-026H) are set to their default value (2FH).

The smoothed clock output from the TJAT is selected as LTCK.

- Transmit Clock Slave Mode (System Backplane Rate: 4.096 Mbit/s)

TSCCKA is selected as the TJAT DPLL input reference clock. TSCCKA is equal to 2.048 M. The N1 (b7~0, E1-025H) and N2 (b7~0, E1-026H) are set to their default value (2FH).

The smoothed clock output from the TJAT is selected as LTCK.

- Transmit Clock Master Mode

XCK/24 is selected as the TJAT DPLL input reference clock.

XCK/24 is selected as LTCK.

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- Transmit Multiplexed Mode (System Backplane Rate: 8.192 Mbit/s)

TSCCKA is selected as the TJAT DPLL input reference clock. TSCCKA is equal to 2.048 M. The N1 (b7~0, E1-025H) and N2 (b7~0, E1-026H) are set to their default value (2FH).

The smoothed clock output from the TJAT is selected as LTCK.

- Transmit Multiplexed Mode (System Backplane Rate: 16.384 Mbit/s)

TSCCKA or TSCCKA/8 is selected as the TJAT DPLL input reference clock. TSCCKA is equal to 2.048 M or 16.384 M. The N1 (b7~0, E1-025H) and N2 (b7~0, E1-026H) are set to their default value (2FH).

The smoothed clock output from the TJAT is selected as LTCK.

4.2 T1/J1 MODE

4.2.1 DEFAULT SETTING

When the device is powered-up, all the registers are in their default values.

Any of the eight framers can be reset anytime when the RESET (b0, E1-00AH / b0, T1/J1-00DH) in its framer is set. The device can also be reset anytime when the $\overline{RST}$ pin is low for at least 100 ns.

After the hardware reset, the IDT82V2108 will default to the following settings:

- Mode: the default operation mode of the device is T1 mode.
- Receive Path: the default setting of each block in the receive path is illustrated in Table 50.
- Transmit Path: the default setting of each block in the transmit path is illustrated in Table 51.

Table 50: Default Setting in Receive Path in T1/J1 Mode

Function Block	Default Setting Description
Line Interface	- LRDn inputs Non-Return to Zero (NRZ) data and is sampled on the rising edge of LRCKn. - The RJAT Clock Divisors (N1, N2) are set to '2F'.
Frame Processor	- Super Frame (SF) format is enabled.
HDLC Receiver #1, #2	- RHDLCs are disabled.
Receive System Interface	- In the Receive Clock Slave External Signaling Mode. - The data on the RSDn, RSSIGn pins are updated on the falling edge of RSCCK. - RSCFS indicates each F-bit. - The data on the RSDn, RSSIGn, RSFSn pins are held in high-impedance state.
Receive Payload Control	- The RPLC is disabled.
PRGD	- The PRGD is configured to monitor the extracted data patterns in Frame 1.

Table 51: Default Setting in Transmit Path in T1/J1 Mode

Function Block	Default Setting Description
PRGD	- The PRGD is configured to insert test patterns to Frame 1.
Transmit System Interface	- In the Transmit Clock Slave External Signaling Mode. - The data on the TSDn and TSSIGn pins are sampled on the rising edge of TSCCKB.
Transmit Payload Control	- The TPLC is disabled.
Frame Generator	- Super Frame (SF) format is enabled.
HDLC Transmitter #1, #2	- The THDLCs are disabled.
Bit-Oriented Message Transmitter	- The BOMT is disabled.
Inband Loop-back Code Generator	- The Inband Loop-back Code Generator is disabled.
Line Interface	- LTDn outputs Non-Return to Zero (NRZ) data and is updated on the falling edge of LTCKn. - TJAT Clock Divisors (N1, N2) are set to '2F'. - Digital jitter attenuation is enabled. The PLL is synchronized to the TSCCKB clock. The smoothed clock output from the PLL is selected as LTCKn.

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4.2.2 OPERATION IN J1 MODE

The IDT82V2108 can also be operated in J1 mode when the TEMODE (b0, 400H) is set to logic 1. Except for the setting of the JYEL in bit 3 of FRMP Configuration registers (020H, 0A0H, 120H, 1A0H, 220H, 2A0H, 320H, 3A0H), the J1_YEL in bit 5 of ALMD Configuration registers (02CH, 0ACH, 12CH, 1ACH, 22CH, 2ACH, 32CH, 3ACH) and the J1_YEL in bit 5 and the J1_CRC in bit 6 of FRMG Configuration registers (044H, 0C4H, 144H, 1C4H, 244H, 2C4H, 344H, 3C4H), the setting of the other registers is the same as the setting in T1 mode.

The follows illustrate the setting in the J1 mode which is different from the setting in the T1 mode.

In receive path, set the JYEL in bit 3 of FRMP Configuration registers (020H, 0A0H, 120H, 1A0H, 220H, 2A0H, 320H, 3A0H) to logic 1, the Frame Processor will operate in J1 mode. Set the J1_YEL in bit 5 of ALMD Configuration registers (02CH, 0ACH, 12CH, 1ACH, 22CH, 2ACH, 32CH, 3ACH) to logic 1, the Alarm Detector will operate in J1 mode.

In transmit path, set the J1_CRC in bit 6 of FRMG Configuration registers (044H, 0C4H, 144H, 1C4H, 244H, 2C4H, 344H, 3C4H) to logic 1, the Frame Generator will generate J1 frame. Set the J1_YEL in bit 5 of FRMG Configuration registers (044H, 0C4H, 144H, 1C4H, 244H, 2C4H, 344H, 3C4H) to logic 1, the IDT82V2108 will transmit the Yellow alarm in J1 format if Yellow alarm transmission is enabled.

4.2.3 VARIOUS OPERATION MODES CONFIGURATION

Five operation modes can be set in the receive path and four operation modes can be set in the transmit path. In each operation modes, the configurations in Table 52 and Table 53 are illustrated for reference.

Table 52: Various Operation Modes in Receive Path for Reference

Mode	Register [1]	Value (from Bit7 to Bit0)	Description [2]
Receive Clock Slave RSCK Reference Mode	001H	10000000	In the Receive Clock Slave RSCK Reference mode.
	003H	00010011	Enable the normal operation of the RSDn pin. The data on RSDn is updated on the rising edge of RSCCK. The data on RSCFS is sampled on the falling edge of RSCCK.
	020H	00110000	The Frame Processor is set in the ESF format. The CRC-6 calculation is performed when mimic framing pattern is present.
	02CH	00010000	The Alarm Detector is set in the ESF format.
	040H	00000100	The Receive CAS/RBS Buffer is set in the ESF format.
Receive Clock Slave External Signaling Mode (1.544 Mbit/s)	001H	11000000	In the Receive Clock Slave External Signaling mode. The backplane rate is 1.544 Mbit/s.
	003H	00010011	Enable the normal operation of the RSDn and RSSIGn pins. The data on RSDn and RSSIGn is updated on the rising edge of RSCCK. The data on RSCFS is sampled on the falling edge of RSCCK.
	020H	00110000	The Frame Processor is set in the ESF format. The CRC-6 calculation is performed when mimic framing pattern is present.
	02CH	00010000	The Alarm Detector is set in the ESF format.
	040H	00000100	The Receive CAS/RBS Buffer is set in the ESF format.
Receive Clock Slave External Signaling Mode (2.048 Mbit/s)	001H	11010000	In the Receive Clock Slave External Signaling mode. The backplane rate is 2.048 Mbit/s.
	003H	00010011	Enable the normal operation of the RSDn and RSSIGn pins. The data on RSDn and RSSIGn is updated on the rising edge of RSCCK. The data on RSCFS is sampled on the falling edge of RSCCK.
	020H	00110000	The Frame Processor is set in the ESF format. The CRC-6 calculation is performed when mimic framing pattern is present.
	02CH	00010000	The Alarm Detector is set in the ESF format.
	040H	00000100	The Receive CAS/RBS Buffer is set in the ESF format.
Receive Clock Master Full T1/ J1 Mode	001H	01000000	In the Receive Clock Master Full T1/J1 mode.
	003H	00010000	Enable the normal operation of the RSDn pin. The data on RSDn and RSFSn is updated on the rising edge of RSCK.
	020H	00000000	The Frame Processor is set in the SF format.
	02CH	00000000	The Alarm Detector is set in the SF format.
	040H	00000000	The Receive CAS/RBS Buffer is set in the SF format.

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Table 52: Various Operation Modes in Receive Path for Reference (Continued)

Mode	Register [1]	Value (from Bit7 to Bit0)	Description [2]
Receive Clock Master Fractional T1/J1 Mode	001H	00000000	In the Receive Clock Master Nx64k mode.
	003H	00010000	Enable the normal operation of the RSDn pin. The data on RSDn and RSFSn is updated on the rising edge of RSCK.
	020H	00110000	The Frame Processor is set in the ESF format. The CRC-6 calculation is performed when mimic framing pattern is present
	02CH	00010000	The Alarm Detector is set in the ESF format.
	040H	00000100	The Receive CAS/RBS Buffer is set in the ESF format.
	050H	00000001	Enable the Receive Payload Control.
	01H-18H (RPLC Indirect Registers)	01000000	The code in the DTRK[7:0] replaces the data output on the RSDn pin in the corresponding channel.
Receive Multiplexed Mode	001H	11001000	In the Receive Multiplexed mode. The receive backplane rate is 8.192 Mbit/s.
	081H	11001000	
	101H	11001000	
	181H	11001000	
	201H	11001000	
	281H	11001000	
	301H	11001000	
	381H	11001000	
	003H	01010011	Multiplex the data stream of these four framers to the multiplexed bus 1. Enable the normal operation of the MRSD and MRSSIG pins.The data on MRSD and MRSSIG is updated on the rising edge of MRSCCK. The data on MRSCFS is sampled on the falling edge of MRSCCK.
	083H	01010011	
	103H	01010011	
	183H	01010011	
	203H	11010011	Multiplex the data stream of these four framers to the multiplexed bus 2. Enable the normal operation of the MRSD and MRSSIG pins.The data on MRSD and MRSSIG is updated on the rising edge of MRSCCK. The data on MRSCFS is sampled on the falling edge of MRSCCK.
	283H	11010011	
	303H	11010011	
	383H	11010011	
	077H	00000000	TSOFF[6:0] = 0. The time slot offset is 0.
	0F7H	00000001	TSOFF[6:0] = 1. The time slot offset is 1.
	177H	00000010	TSOFF[6:0] = 2. The time slot offset is 2.
	1F7H	00000011	TSOFF[6:0] = 3. The time slot offset is 3.
	277H	00000000	TSOFF[6:0] = 0. The time slot offset is 0.
	2F7H	00000001	TSOFF[6:0] = 1. The time slot offset is 1.
	377H	00000010	TSOFF[6:0] = 2. The time slot offset is 2.
	3F7H	00000011	TSOFF[6:0] = 3. The time slot offset is 3.
	020H	00110000	The Frame Processor is set in the ESF format. The CRC-6 calculation is performed when mimic framing pattern is present.
	0A0H	00110000	
	120H	00110000	
	1A0H	00110000	
	220H	00110000	
	2A0H	00110000	
	320H	00110000	
	3A0H	00110000	

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Table 52: Various Operation Modes in Receive Path for Reference (Continued)

Mode	Register [1]	Value (from Bit7 to Bit0)	Description [2]
Receive Multi-plexed Mode (Continued)	02CH	00010000	The Alarm Detector is set in the ESF format.
	0ACH	00010000	
	12CH	00010000	
	1ACH	00010000	
	22CH	00010000	
	2ACH	00010000	
	32CH	00010000	
	3ACH	00010000	
	040H	00000100	The Receive CAS/RBS Buffer is set in the ESF format.
	0C0H	00000100	
	140H	00000100	
	1C0H	00000100	
	240H	00000100	
	2C0H	00000100	
	340H	00000100	
	3C0H	00000100	

Note:
1. In the 'Register' column, except for the Receive/Transmit Multiplexed mode, the register position of Framer 1 is listed to represent the set of the registers of eight framers. The other registers positions are tabulated in the 'Register Map'. However, in the Receive/Transmit Multiplexed mode, the registers positions of eight framers are all listed.
2. The 'Description' illustrates the fundamental function of the operation mode. The others can be configured as desired.

Table 53: Various Operation Modes in Transmit Path for Reference

Mode	Register [1]	Value (from Bit7 to Bit0)	Description [2]
Transmit Clock Slave TSFS Enable Mode	004H	00001000	The data on the TSDn and TSCFS pins is sampled on the falling edge of TSCCKB. The data on TSFSn is updated on the falling edge of TSCCKB.
	005H	10000000	In the Transmit Clock Slave TSFS Enabled mode. The backplane rate is 1.544 Mbit/s.
	044H	00010000	The Frame Generator is set in the ESF format.
	007H	00001101	TSCCKB is selected as the TJAT input reference clock. Smoothed clock is selected as Line Transmit Clock (LTCK).
	01BH	00010000	The FIFO is set to self-center its read pointer.
Transmit Clock Slave External Signaling Mode (1.544 Mbit/s)	004H	00001000	The data on the TSDn, TSSIGn and TSCFS pins is sampled on the falling edge of TSCCKB.
	005H	11000000	In the Transmit Clock Slave External Signaling mode. The backplane rate is 1.544 Mbit/s.
	044H	00010000	The Frame Generator is set in the ESF format.
	007H	00001101	TSCCKB is selected as TJAT input reference clock. Smoothed clock is selected as Line Transmit Clock (LTCK).
	01BH	00010000	The FIFO is set to self-center its read pointer.
Transmit Clock Slave External Signaling Mode (2.048 Mbit/s)	004H	00001000	The data on the TSDn, TSSIGn and TSCFS pins is sampled on the falling edge of TSCCKB.
	005H	11000100	In the Transmit Clock Slave External Signaling mode. The backplane rate is 2.048 Mbit/s.
	044H	00010000	The Frame Generator is set in the ESF format.
	007H	00001101	TSCCKB is selected as the TJAT input reference clock. Smoothed clock is selected as Line Transmit Clock (LTCK).
	019H	11111111	Set the Reference Clock Divisor(N1) to '255'.
	01AH	11000000	Set the Output Clock Divisor(N2) to '192'.
	01BH	00010000	The FIFO is set to self-center its read pointer.

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Table 53: Various Operation Modes in Transmit Path for Reference (Continued)

Mode	Register [1]	Value (from Bit7 to Bit0)	Description [2]
Transmit Clock Master Mode	004H	00000110	The data on the TSFSn pin is updated on the rising edge of LTCK. The data on the TSDn pin is sampled on the falling edge of LTCK.
	005H	01000000	In the Transmit Clock Master Full T1/J1 mode. The backplane rate is 1.544 Mbit/s.
	044H	00000000	The Frame Generator is set in the SF format.
	007H	00100100	XCK/24 is selected as TJAT input reference clock and Line Transmit Clock
Transmit Multiplexed Mode	004H	00001000	The data on the TSDn, TSSIGn and TSCFS pins is sampled on the falling edge of TSCCKB.
	084H	00001000	
	104H	00001000	
	184H	00001000	
	204H	00001000	
	284H	00001000	
	304H	00001000	
	384H	00001000	
	005H	11001100	In the Transmit Multiplexed mode. The backplane rate is 8.192 Mbit/s.
	085H	11001100	
	105H	11001100	
	185H	11001100	
	205H	11001100	
	285H	11001100	
	305H	11001100	
	385H	11001100	
	014H	00000000	TSOFF[6:0] = 0. The time slot offset is 0.
	094H	00000000	
	114H	00000001	TSOFF[6:0] = 1. The time slot offset is 1.
	194H	00000001	
	214H	00000010	TSOFF[6:0] = 2. The time slot offset is 2.
	294H	00000010	
	314H	00000011	TSOFF[6:0] = 3. The time slot offset is 3.
	394H	00000011	
	015H	00000000	The data stream is taken from multiplexed bus 1.
	095H	01000000	The data stream is taken from multiplexed bus 2.
	115H	00000000	The data stream is taken from multiplexed bus 1.
	195H	01000000	The data stream is taken from multiplexed bus 2.
	215H	00000000	The data stream is taken from multiplexed bus 1.
	295H	01000000	The data stream is taken from multiplexed bus 2.
	315H	00000000	The data stream is taken from multiplexed bus 1.
	395H	01000000	The data stream is taken from multiplexed bus 2.
	044H	00010000	The Frame Generator is set in the ESF format.
	0C4H	00010000	
	144H	00010000	
	1C4H	00010000	
	244H	00010000	
	2C4H	00010000	
	344H	00010000	
	3C4H	00010000	

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Table 53: Various Operation Modes in Transmit Path for Reference (Continued)

Mode	Register [1]	Value (from Bit7 to Bit0)	Description [2]
Transmit Multi-plexed Mode (Continued)	007H	00011101	TSCCKA is selected as TJAT input reference clock. Smoothed clock is selected as Line Transmit Clock (LTCK).
	087H	00011101	
	107H	00011101	
	187H	00011101	
	207H	00011101	
	287H	00011101	
	307H	00011101	
	387H	00011101	
	019H	11111111	Set the Reference Clock Divisor(N1) to '255'.
	099H	11111111	
	119H	11111111	
	199H	11111111	
	219H	11111111	
	299H	11111111	
	319H	11111111	
	399H	11111111	
	01AH	11000000	Set the Output Clock Divisor(N2) to '192'.
	09AH	11000000	
	11AH	11000000	
	19AH	11000000	
	21AH	11000000	
	29AH	11000000	
	31AH	11000000	
	39AH	11000000	
	01BH	00010000	The FIFO is set to self-center its read pointer.
	09BH	00010000	
	11BH	00010000	
	19BH	00010000	
	21BH	00010000	
	29BH	00010000	
	31BH	00010000	
	39BH	00010000	

Note:
1. In the 'Register' column, except for the Receive/Transmit Multiplexed mode, the register position of Framer 1 is listed to represent the set of the registers of eight framers. The other registers positions are tabulated in the 'Register Map'. However, in the Receive/Transmit Multiplexed mode, the registers positions of the eight framers are all listed.
2. The 'Description' illustrates the fundamental function of the operation mode. The others can be configured as desired.

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4.2.4 OPERATION EXAMPLE

In this chapter, some common operation examples are given for reference.

4.2.4.1 Using HDLC Receiver

In T1/J1 mode, the HDLC Receive can only be used in the ESF format. Before using the HDLC#2 Receive, the TXCISEL (b3, T1/J1-00DH) must be set to '0' to enable the HDLC data link position for receive path.

Since two HDLC Receive data links are integrated in one framer, one of the two HDLC Receive data links must be chosen in the RHDLCSEL[1:0] (b7~6, T1/J1-00DH). The RHDLC #1 can only extract from F-bit of each odd frame. The RHDLC #2 can be set to extract from even and/or odd frames, from any channel, and from any bit. The follow is an example for selecting the HDLC Receive data link positions in RHDLC #2:

a. Extract the HDLC data link from all bits of channel 20 of all framers in HDLC Receive #2:

- set the TXCISEL (b3, T1/J1-00DH) to '0';
- set the RHDLCSEL[1:0] (b7~6, T1/J1-00DH) to '01';
- set the DL2_EVEN (b7, T1/J1-070H) to '1';
- set the DL2_ODD (b6, T1/J1-070H) to '1';
- set the DL2_TS[4:0] (b4~0, T1/J1-070H) to '10100';
- set the DL2_BIT[7:0] (b7~0, T1/J1-071H) to '11111111'.

After setting the HDLC data link position properly, the selected HDLC Receive should be enabled by setting the EN (b0, T1/J1-054H) to logic 1. If needed, set the MEN (b3, T1/J1-054H) and the MM (b2, T1/J1-054H) to determine which Address Matching Mode is used (refer to Chapter 5.2 Register Description for details). After setting these 3 bits, the RHDLC Primary Address Match register and the RHDLC Secondary Address Match register should be set to proper values. If the INTC[6:0] (b6~0, T1/J1-055H) are set, whenever the number of bytes in the RHDLC FIFO exceeds the value set in the INTC[6:0] (b6~0, T1/J1-055H), the INTR (b0, T1/J1-056H) will be set to logic 1. This interrupt will persist until the RHDLC FIFO becomes empty. Setting the INTE (b7, T1/J1-055H) to logic 1 allows the internal interrupt status to be propagated to the $\overline{\text{INT}}$ output pin.

After setting these registers properly, the HDLC data can be received in a polled or interrupt driven mode.

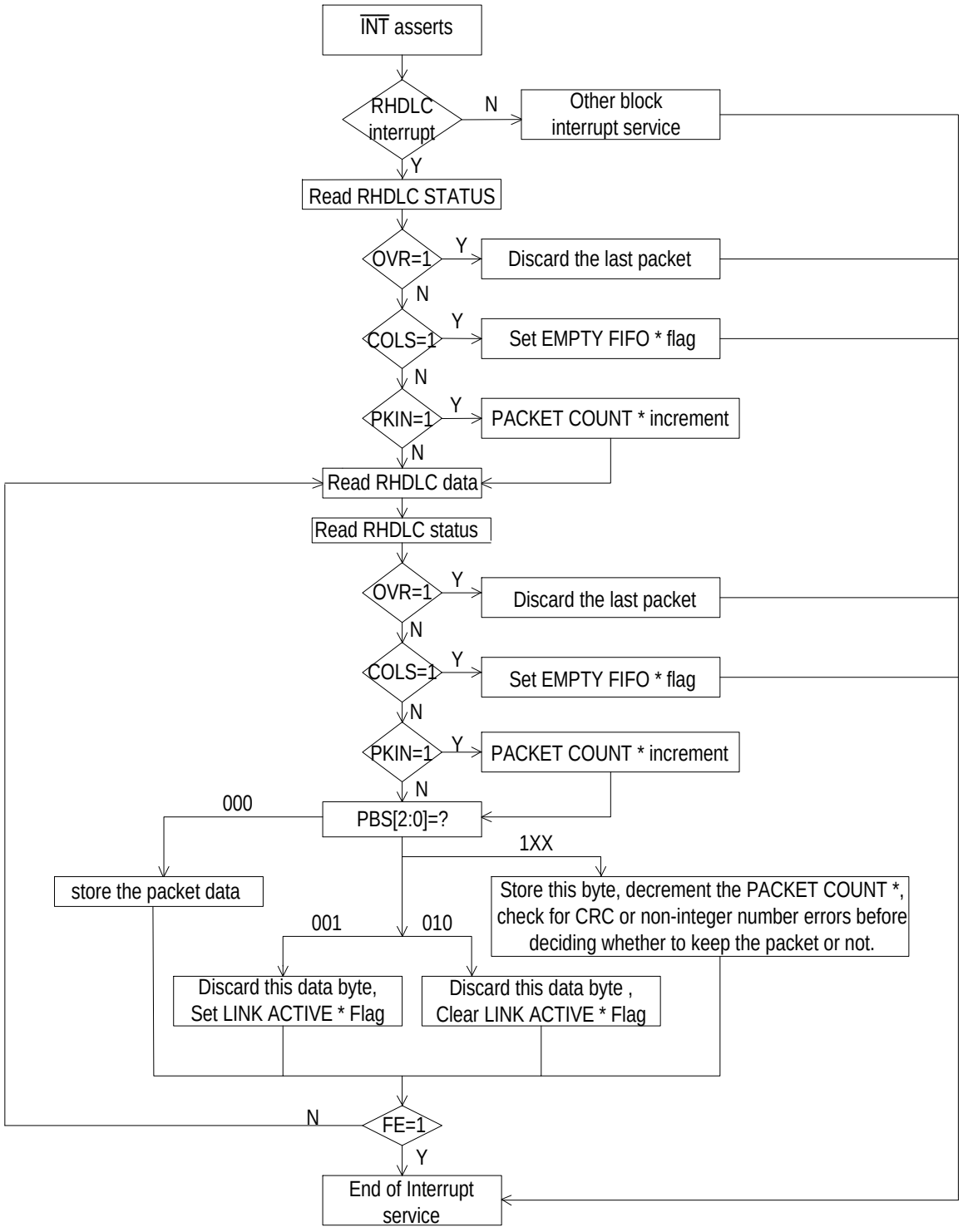
- Interrupt Driven Mode

When the INTE (b7, T1/J1-055H) is set to logic 1, if the $\overline{\text{INT}}$ pin is asserted, the source of the interrupt should be identified firstly by reading the Interrupt ID register and Interrupt Source registers. If the source of the interrupt is HDLC Receive, the Interrupt Service procedure will be carried out as shown in Figure 79.

- Polling Mode

In the polling mode, the operation procedure is the same as Figure 79, except that the entry of the service is from a local timer rather than an interrupt.

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Note:
* The PACKET COUNT ,EMPTY FIFO and LINK ACTIVE is a local software variable

Figure 79. Interrupt Service in T1/J1 Mode HDLC Receiver

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To summarize the procedure of using HDLC Receive, a complete example is shown in Table 54.

Table 54: Example for Using HDLC Receiver

Register	Value	Description
00DH	50H	RHDLC #2 is selected. The HDLC Receive is accessible to the CPU interface.
070H	C4H	TS4 of even frames and odd frames is selected.
071H	FFH	All 8 bits are selected.
054H	0DH	The function of the RHDLC #2 is enabled. Set the address match mode.
055H	8FH	Set the INTE to '1'. When the number of bytes in the RHDLC FIFO exceeds 15, an interrupt is generated.
058H	13H	The primary address is set to 13H.
059H	FFH	The secondary address is set to FFH.
Then read the data status in register 056H. Until a complete packet is received, read the data from register 057H.		

4.2.4.2 Using HDLC Transmitter

In T1/J1 mode, the HDLC Transmit can only be used in the ESF format. Before using the HDLC#2 Transmit, the TXCISEL (b3, T1/J1-00DH) must be set to '1' to enable the HDLC data link position for transmit path.

Since two HDLC Transmit data links are integrated in one framer, one of the two HDLC Transmit data links must be chosen in the THDLCSEL[1:0] (b5~4, T1/J1-00DH). The THDLC #1 can only insert to F-bit of each odd frame. The THDLC #2 can be set to insert to even and/or odd frames, to any channel, and to any bit. The follow is an example for selecting the HDLC Transmit data link positions in THDLC #2:

a. Insert the HDLC data link to all bits of channel 20 of all framers in HDLC Transmit #2:

- set the TXCISEL (b3, T1/J1-00DH) to '1';
- set the THDLCSEL[1:0] (b5~4, T1/J1-00DH) to '01';
- set the DL2_EVEN (b7, T1/J1-070H) to '1';
- set the DL2_ODD (b6, T1/J1-070H) to '1';
- set the DL2_TS[4:0] (b4~0, T1/J1-070H) to '10100';
- set the DL2_BIT[7:0] (b7~0, T1/J1-071H) to '11111111'.

After setting the HDLC data link position properly, the selected HDLC Transmit should be enabled by setting the EN (b0, T1/J1-034H) to logic 1. The FIFOCLR (b6, T1/J1-034H) should be set and then cleared to initialize the THDLC FIFO.

Set the CRC (b1, T1/J1-034H) to logic 1 if the Frame Check Sequences (FCS) generation is desired. Set the FULLE (b3, T1/J1-037H), OVRE (b2, T1/J1-037H), UDRE (b1, T1/J1-037H) and LFILLE (b0, T1/J1-037H) to logic 1 if interrupt driven mode is used. Set THDLC Upper Transmit Threshold and THDLC Lower Transmit Threshold registers to the desired values. If a complete packet has been written into THDLC FIFO, the EOM (b3, T1/J1-034H) should be set.

After setting these registers properly, the HDLC data can be transmitted in a polled or interrupt driven mode.

- Interrupt Driven Mode

Writing HDLC data to THDLC FIFO, the THDLC will transmit the HDLC data if the end of a packet was written or if the THDLC FIFO fill level reaches the Upper Transmit Threshold. The writing procedure is shown in Figure 80.

When the FULLE (b3, T1/J1-037H), OVRE (b2, T1/J1-037H), UDRE (b1, T1/J1-037H) and LFILLE (b0, T1/J1-037H) are set to logic 1, the source of the interrupt should be identified firstly by reading the Interrupt ID register and Interrupt Source registers if the $\overline{INT}$ pin is asserted. If the source of the interrupt is HDLC Transmit, the Interrupt Service procedure will be carried out as shown in Figure 81.

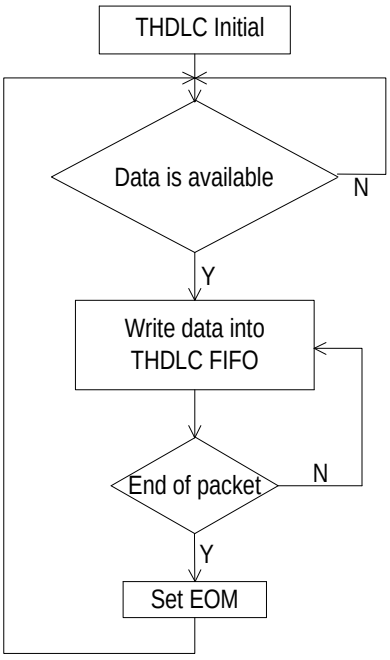
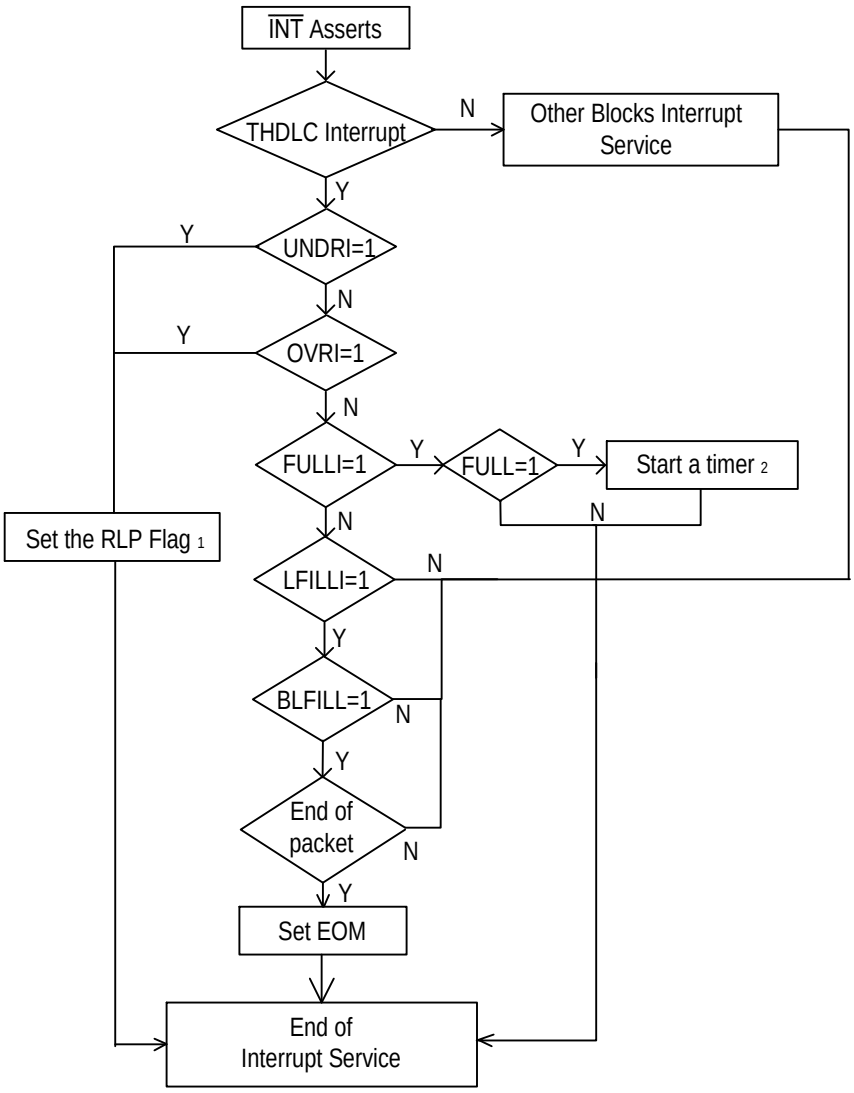


Figure 80. Writing Data to T1/J1 Mode THDLC FIFO

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Note:
1. RLP-Retransmit the last packet, a local software variable.
2. A local timer to wait for a certain time until the Full = 0 or the BLFILL = 1.

Figure 81. Interrupt Service in T1/J1 Mode HDLC Transmitter

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- Polling Mode

In packet transmission polling mode, the FULLE (b3, T1/J1-037H), OVRE (b2, T1/J1-037H), UDRE (b1, T1/J1-037H) and LFILLE (b0, T1/J1-037H) should be set to logic 0. The THDLC Lower Transmit Threshold should be set to such a value that sufficient warning of an underrun is given. The procedure shown in Figure 82 should be followed.

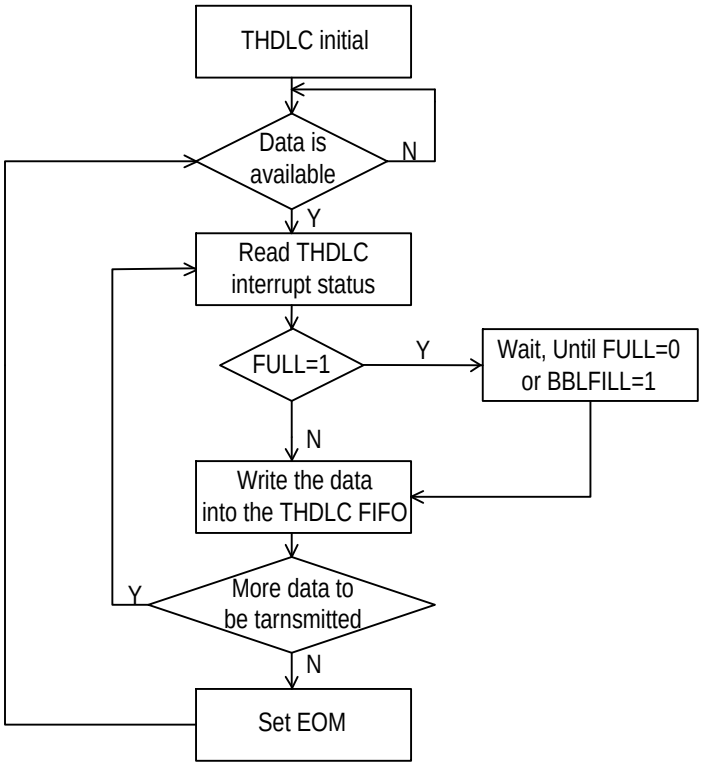


Figure 82. Polling Mode in T1/J1 Mode HDLC Transmitter

To summarize the procedure of using HDLC Transmit, a complete example is shown in Table 55.

Table 55: Example for Using HDLC Transmitter

Register	Value	Description
00DH	58H	THDLC #2 is selected. The HDLC Transmit is accessible to the CPU interface.
070H	C4H	TS4 of even frames and odd frames is selected
071H	FFH	All 8 bits are selected.
034H	C3H	The function of the THDLC #2 is enabled. The FCS is enabled and the THDLC FIFO is reset.
034H	83H	
037H	0FH	Enable the THDLC Interrupt Enable bits.
039H	12H	Write data into THDLC FIFO.
039H	34H	
039H	56H	
039H	78H	
039H	9AH	
039H	BCH	
039H	DEH	
039H	FFH	
034H	8BH	End of packet and set the EOM to ‘1’.

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4.2.4.3 Using PRBS Generator / Detector

The IDT82V2108 provides one PRBS generator/detector block to generate and detect an enormous variety of pseudo-random and repetitive patterns to diagnose T1/J1 data stream of eight framers. The common test patterns are tabularized in Table 56.

Table 56: Test Pattern in T1/J1 Mode

Pseudo-Random Pattern Generation (the PS [b4, T1/J1-060H] is logic 0)								
Pattern Type	TR [1]	LR [2]	IR#1 [3]	IR#2 [4]	IR#3 [5]	IR#4 [6]	TINV [7]	RINV [7]
2^3 - 1	00	02	FF	FF	FF	FF	0	0
2^4 - 1	00	03	FF	FF	FF	FF	0	0
2^5 - 1	01	04	FF	FF	FF	FF	0	0
2^6 - 1	04	05	FF	FF	FF	FF	0	0
2^7 - 1 (Fractional T1 LB Activate)	00	06	FF	FF	FF	FF	0	0
2^7 - 1 (Fractional T1 LB Activate)	03	06	FF	FF	FF	FF	0	0
2^7 - 1	03	06	FF	FF	FF	FF	1	1
2^9 - 1 (O.153)	04	08	FF	FF	FF	FF	0	0
2^{10} - 1	02	09	FF	FF	FF	FF	0	0
2^{11} - 1 (O.152,O.153)	08	0A	FF	FF	FF	FF	0	0
2^{15} - 1 (O.151)	0D	0E	FF	FF	FF	FF	1	1
2^{17} - 1	02	10	FF	FF	FF	FF	0	0
2^{18} - 1	06	11	FF	FF	FF	FF	0	0
2^{20} - 1 (O.153)	02	13	FF	FF	FF	FF	0	0
2^{21} - 1	01	14	FF	FF	FF	FF	0	0
2^{22} - 1	00	15	FF	FF	FF	FF	0	0
2^{23} - 1 (O.151)	11	16	FF	FF	FF	FF	1	1
2^{25} - 1	02	18	FF	FF	FF	FF	0	0
2^{28} - 1	02	1B	FF	FF	FF	FF	0	0
2^{29} - 1	01	1C	FF	FF	FF	FF	0	0
2^{31} - 1	02	1E	FF	FF	FF	FF	0	0
Repetitive Pattern Generation (the PS [b4, T1/J1-060H] is logic 1)								
Pattern Type	TR [1]	LR [2]	IR#1 [3]	IR#2 [4]	IR#3 [5]	IR#4 [6]	TINV [7]	RINV [7]
All ones	00	00	FF	FF	FF	FF	0	0
All zeros	00	00	FE	FF	FF	FF	0	0
Alternating ones/zeros	00	01	FE	FF	FF	FF	0	0
Double alternating ones/zeros	00	03	FC	FF	FF	FF	0	0
3 in 24	00	17	22	00	20	FF	0	0
1 in 16	00	0F	01	00	FF	FF	0	0
1 in 8	00	07	01	FF	FF	FF	0	0
1 in 4	00	03	F1	FF	FF	FF	0	0
DS1 Inband Loopback activate	00	04	F0	FF	FF	0F	0	0
DS1 Inband Loopback deactivate	00	02	FC	FF	FF	FF	0	0

Note:
1. TR - Tap Register. 2. LR - Shift Register Length Register. 3. IR#1 - PRGD Pattern Insertion #1 Register. 4. IR#2 - PRGD Pattern Insertion #2 Register. 5. IR#3 - PRGD Pattern Insertion #3 Register. 6. IR#4 - PRGD Pattern Insertion #4 Register. 7. TINV, RINV - contained in the PRGD Control register.

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The PRBS generator/detector block can be used to test T1/J1 line transmit-receive integrity and system backplane integrity.

- Example For Testing T1/J1 Line Transmit-Receive Integrity

Suppose to monitor the errors in Framer 2 without taking the entire T1/J1 offline. Following procedure should be done.

- Select Framer 2 to be tested by the PRGD block;
- Configure the PRGD register;
- Chose a desired set of channels (for example CH2, CH4, CH5) for insert/extract PRGD test data;
- Set the far end of the line to loop back at least the selected channels;
- Monitor the T1/J1 line transmit-receive integrity.

To realize the above function, the configuration in Table 57 to Table 59 should be set.

Table 57 is the configuration for PRGD and loopback. Table 58 shows the process to initialize the TPLC. Table 59 shows the process to initialize the RPLC.

Table 57: Setting of PRGD

Register	Value	Description
00FH	20H	Select Framer 2 to be tested by the PRGD block. The PRGD pattern is inserted in the TPLC and detected in the RPLC.
060H	82H	Set Pattern Detector registers as error counter registers. Enable automatic resynchronization.
062H	18H	Set the pattern length.
063H	02H	Set the feedback tap position.
068H	FFH	Set the Pattern Insertion registers.
06BH	FFH	Load the data in the Pattern Insertion registers to generate the pattern.
08AH	04H	Set diagnostic digital loopback mode.
0B0H	01H	Enable the TPLC indirect registers to be accessible.
0D0H	01H	Enable the RPLC indirect registers to be accessible.

Table 58: Initialization of TPLC

Register	Value
0B3H	00H
0B2H	01H
0B3H	00H
0B2H	02H
0B3H	00H
0B2H	03H
0B3H	00H
0B2H	04H
0B3H	00H
0B2H	05H
0B3H	00H

Table 58: Initialization of TPLC (Continued)

Register	Value
0B2H	06H
0B3H	00H
0B2H	07H
0B3H	00H
0B2H	08H
0B3H	00H
0B2H	09H
0B3H	00H
0B2H	0AH
0B3H	00H
0B2H	0BH
0B3H	00H
0B2H	0CH
0B3H	00H
0B2H	0DH
0B3H	00H
0B2H	0EH
0B3H	00H
0B2H	0FH
0B3H	00H
0B2H	10H
0B3H	00H
0B2H	11H
0B3H	00H
0B2H	12H
0B3H	00H
0B2H	13H
0B3H	00H
0B2H	14H
0B3H	00H
0B2H	15H
0B3H	00H
0B2H	16H
0B3H	00H
0B2H	17H
0B3H	00H
0B2H	18H
0B3H	00H
0B2H	31H
0B3H	00H
0B2H	32H
0B3H	00H
0B2H	33H
0B3H	00H
0B2H	34H
0B3H	00H
0B2H	35H

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Table 58: Initialization of TPLC (Continued)

Register	Value
0B3H	00H
0B2H	36H
0B3H	00H
0B2H	37H
0B3H	00H
0B2H	38H
0B3H	00H
0B2H	39H
0B3H	00H
0B2H	3AH
0B3H	00H
0B2H	3BH
0B3H	00H
0B2H	3CH
0B3H	00H
0B2H	3DH
0B3H	00H
0B2H	3EH
0B3H	00H
0B2H	3FH
0B3H	00H
0B2H	40H
0B3H	00H
0B2H	41H
0B3H	00H
0B2H	42H
0B3H	00H
0B2H	43H
0B3H	00H
0B2H	44H
0B3H	00H
0B2H	45H
0B3H	00H
0B2H	46H
0B3H	00H
0B2H	47H
0B3H	00H
0B2H	48H

Then set the TEST in TPLC Payload Control register for CH2, CH4 and CH5. The process is:

Register	Value	Description
0B3H	08H	Set the TEST in TPLC Payload Control register for CH2.
0B2H	02H	
0B3H	08H	Set the TEST in TPLC Payload Control register for CH4.
0B2H	04H	

Table 58: Initialization of TPLC (Continued)

Register		Value
0B3H	08H	Set the TEST in TPLC Payload Control register for CH5.
0B2H	05H	

Table 59: Initialization of RPLC

Register	Value
0D3H	00H
0D2H	01H
0D3H	00H
0D2H	02H
0D3H	00H
0D2H	03H
0D3H	00H
0D2H	04H
0D3H	00H
0D2H	05H
0D3H	00H
0D2H	06H
0D3H	00H
0D2H	07H
0D3H	00H
0D2H	08H
0D3H	00H
0D2H	09H
0D3H	00H
0D2H	0AH
0D3H	00H
0D2H	0BH
0D3H	00H
0D2H	0CH
0D3H	00H
0D2H	0DH
0D3H	00H
0D2H	0EH
0D3H	00H
0D2H	0FH
0D3H	00H
0D2H	10H
0D3H	00H
0D2H	11H
0D3H	00H
0D2H	12H
0D3H	00H
0D2H	13H
0D3H	00H
0D2H	14H

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Table 59: Initialization of RPLC (Continued)

Register	Value
0D3H	00H
0D2H	15H
0D3H	00H
0D2H	16H
0D3H	00H
0D2H	17H
0D3H	00H
0D2H	18H

Then set the TEST in RPLC Payload Control register for CH2, CH4 and CH5. The process is:

Register	Value	Description
0D3H	08H	Set the TEST in RPLC Payload Control register for CH2.
0D2H	02H	
0D3H	08H	Set the TEST in RPLC Payload Control register for CH4
0D2H	04H	
0D3H	08H	Set the TEST in RPLC Payload Control register for CH5
0D2H	05H	

After the above setting, read the 061H register twice. If the SYNCV (b4, T1/J1-061H) is logic 1 and the BEI (b2, T1/J1-061H) is logic 0, the pattern detector is in synchronization state.

Then insert errors into this link. Here suppose to insert 3 errors, then the configuration is shown in Table 60.

Table 60: Error Insertion

Register	Value
064H	08H
064H	00H
064H	08H
064H	00H
064H	08H
064H	00H

Then write 00H into the 06CH register to update the error counter registers. Then read the registers from 06CH to 06FH to check the error numbers.

- Example For Testing T1/J1 System Backplane Integrity

To test the T1/J1 system backplane integrity, the RXPATGEN (b2, T1/J1-00FH) should be set to logic 1 and the other registers are set as above. Then the PRGD can be used to test the system backplane integrity.

4.2.4.4 Using Payload Control and Receive CAS/RBS Buffer

Before using the Receive/Transmit Payload Control and Receive CAS/RBS Buffer, the indirect registers of these blocks must be initialized to eliminate erroneous control data. The PCCE (b0, T1/J1-050H & b0, T1/J1-030H & b0, T1/J1-040H) of these blocks must be set to logic 1 to enable these blocks.

Then the BUSY (b7, T1/J1-051H & b7, T1/J1-031H & b7, T1/J1-041H) must be checked before a new access request to the RPLC, TPLC and RCRB indirect registers. When the BUSY is logic 0, the new reading and writing access operations can be performed.

Figure 83 shows the writing sequence of the RPLC, TPLC and RCRB indirect registers. Figure 84 shows the reading sequence of the RPLC, TPLC and RCRB indirect registers.

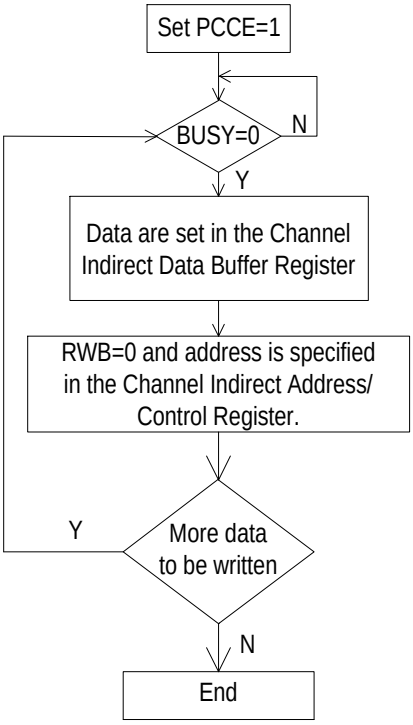


Figure 83. Writing Sequence of Indirect Register in T1/J1 Mode

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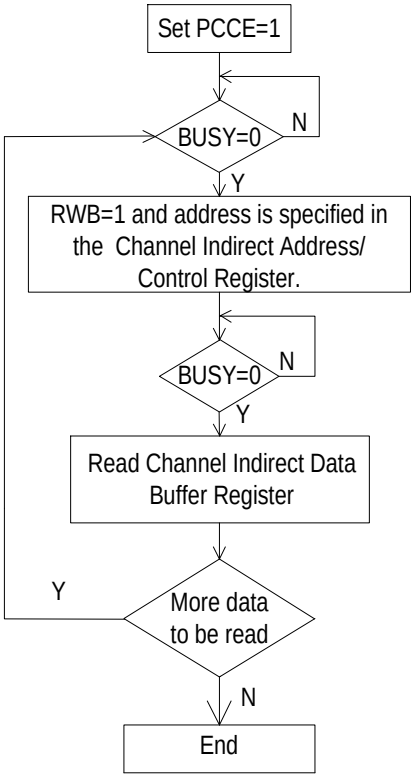


Figure 84. Reading Sequence of Indirect Register in T1/ J1 Mode

4.2.4.5 Using TJAT / Timing Option

In different operation modes, the Timing Options and Clock Divisor Control registers can be set as the follows:

- Transmit Clock Slave Mode (System Backplane Rate: 1.544 Mbit/s)

TSCCKA or TSCCKB is selected as the TJAT DPLL input reference clock. TSCCKA and TSCCKB are both equal to 1.544 M. The N1 (b7~0, T1/J1-019H) and N2 (b7~0, T1/J1-01AH) are set to their default value (2FH).

The smoothed clock output from the TJAT is selected as LTCK.

- Transmit Clock Slave Mode (System Backplane Rate: 2.048 Mbit/s)

TSCCKA or TSCCKB is selected as the TJAT DPLL input reference clock. TSCCKA and TSCCKB are both equal to 2.048 M. The N1 (b7~0, T1/J1-019H) is set to ‘b11111111 and the N2 (b7~0, T1/J1-01AH) is set to ‘b11000000.

The smoothed clock output from the TJAT is selected as LTCK.

- Transmit Clock Slave Mode (System Backplane Rate: 4.096 Mbit/s)

TSCCKA is selected as the TJAT DPLL input reference clock. TSCCKA is equal to 2.048 M. The N1 (b7~0, T1/J1-019H) is set to ‘b11111111 and the N2 (b7~0, T1/J1-01AH) is set to ‘b11000000.

The smoothed clock output from the TJAT is selected as LTCK.

- Transmit Clock Master Mode

XCK/24 is selected as the TJAT DPLL input reference clock.

XCK/24 is selected as LTCK.

- Transmit Multiplexed Mode (System Backplane Rate: 8.192 Mbit/s)

TSCCKA is selected as the TJAT DPLL input reference clock. TSCCKA is equal to 2.048 M. The N1 (b7~0, T1/J1-019H) is set to ‘b11111111 and the N2 (b7~0, T1/J1-01AH) is set to ‘b11000000.

The smoothed clock output from the TJAT is selected as LTCK.

- Transmit Multiplexed Mode (System Backplane Rate: 16.384 Mbit/s)

TSCCKA or TSCCKA/8 is selected as the TJAT DPLL input reference clock. TSCCKA is equal to 2.048 M or 16.384 M. The N1 (b7~0, T1/J1-019H) is set to ‘b11111111 and the N2 (b7~0, T1/J1-01AH) is set to ‘b11000000.

The smoothed clock output from the TJAT is selected as LTCK.

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5 PROGRAMMING INFORMATION

The Micro-Processor Interface provides the logic to connect the microprocessor interface. For all accesses, $\overline{CS}$ must be low. The data bus and address bus of the interface can work in the multiplexed on non-multiplexed mode. In the non-multiplexed mode, the ALE pin should be connected to high. In the multiplexed mode, data bus and address bus should be externally connected.

5.1 REGISTER MAP

The registers are divided into two parts: E1 part and T1/J1 part. Before operation, the TEMODE (b0, 400H) must be set to specify which part to be accessed by the microprocessor.

Table 61: T1/J1 Mode Selection Register

Address	Register
400	T1/E1 Mode Selection

5.1.1 E1 MODE REGISTER MAP

When the TEMODE (b0, 400H) is logic 0, the E1 mode registers are accessed.

Table 62: E1 Mode Register Map - Direct Register

E1 Address								Register
Framer 1	Framer 2	Framer 3	Framer4	Framer 5	Framer 6	Framer 7	Framer8	
000	080	100	180	200	280	300	380	Receive Path Line Options
001	081	101	181	201	281	301	381	Receive Side System Interface Options
002	082	102	182	202	282	302	382	Transmit Path Configuration
003	083	103	183	203	283	303	383	Transmit Side System Interface Options
004	084	104	184	204	284	304	384	Transmit Timing Options
005	085	105	185	205	285	305	385	Interrupt Source #1
006	086	106	186	206	286	306	386	Interrupt Source #2
007	087	107	187	207	287	307	387	Diagnostic
008	088	108	188	208	288	308	388	Reserved
009								Chip ID/ Global PMON Update
00A	08A	10A	18A	20A	28A	30A	38A	HDLC Micro Select/Framer Reset
00B								Framer Interrupt ID
00C								PRGD Positioning/Control
00D	08D	10D	18D	20D	28D	30D	38D	Clock Monitor
00E	08E	10E	18E	20E	28E	30E	38E	Receive Path Frame Pulse Configuration
00F	08F	10F	18F	20F	28F	30F	38F	Reserved
010	090	110	190	210	290	310	390	RESI Configuration
011	091	111	191	211	291	311	391	RESI Frame Pulse Configuration
012	092	112	192	212	292	312	392	RESI Parity Configuration
013	093	113	193	213	293	313	393	RESI Time Slot Offset
014	094	114	194	214	294	314	394	RESI Bit Offset
015 ~ 017	095 ~ 097	115 ~ 117	195 ~ 197	215 ~ 217	295 ~ 297	315 ~ 317	395 ~ 397	Reserved
018	098	118	198	218	298	318	398	TRSI Configuration
019	099	119	199	219	299	319	399	TRSI Frame Pulse Configuration
01A	09A	11A	19A	21A	29A	31A	39A	TRSI Parity Configuration and Status
01B	09B	11B	19B	21B	29B	31B	39B	TRSI Time Slot Offset
01C	09C	11C	19C	21C	29C	31C	39C	TRSI Bit Offset
01D ~ 01F	09D ~ 09F	11D ~ 11F	19D ~ 19F	21D ~ 21F	29D ~ 29F	31D ~ 31F	39D ~ 39F	Reserved

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Table 62: E1 Mode Register Map - Direct Register (Continued)

E1 Address								Register
Framer 1	Framer 2	Framer 3	Framer4	Framer 5	Framer 6	Framer 7	Framer8	
020	0A0	120	1A0	220	2A0	320	3A0	RJAT Interrupt Status
021	0A1	121	1A1	221	2A1	321	3A1	RJAT Reference Clock Divisor (N1)
022	0A2	122	1A2	222	2A2	322	3A2	RJAT Reference Clock Divisor (N2)
023	0A3	123	1A3	223	2A3	323	3A3	RJAT Configuration
024	0A4	124	1A4	224	2A4	324	3A4	TJAT Interrupt Status
025	0A5	125	1A5	225	2A5	325	3A5	TJAT Reference Clock Divisor (N1)
026	0A6	126	1A6	226	2A6	326	3A6	TJAT Reference Clock Divisor (N2)
027	0A7	127	1A7	227	2A7	327	3A7	TJAT Configuration
028	0A8	128	1A8	228	2A8	328	3A8	RHDLC 1 (TXCISEL = 0) Link Control / THDLC 1 (TXCISEL = 1) Link Control
029	0A9	129	1A9	229	2A9	329	3A9	RHDLC 1 (TXCISEL = 0) bits select / THDLC 1 (TXCISEL = 1) bits select
02A	0AA	12A	1AA	22A	2AA	32A	3AA	RHDLC 2 (TXCISEL = 0) Link Control / THDLC 2 (TXCISEL = 1) Link Control
02B	0AB	12B	1AB	22B	2AB	32B	3AB	RHDLC 2 (TXCISEL = 0) bits select / THDLC 2 (TXCISEL = 1) bits select
02C	0AC	12C	1AC	22C	2AC	32C	3AC	RHDLC 3 (TXCISEL = 0) Link Control / THDLC 3 (TXCISEL = 1) Link Control
02D	0AD	12D	1AD	22D	2AD	32D	3AD	RHDLC 3 (TXCISEL = 0) bits select / THDLC 3 (TXCISEL = 1) bits select
02E ~ 02F	0AE ~ 0AF	12E ~ 12F	1AE ~ 1AF	22E ~ 22F	2AE ~ 2AF	32E ~ 32F	3AE ~ 3AF	Reserved
030	0B0	130	1B0	230	2B0	330	3B0	FRMP Frame Alignment Option
031	0B1	131	1B1	231	2B1	331	3B1	FRMP Maintenance Mode Options
032	0B2	132	1B2	232	2B2	332	3B2	FRMP Framing Status Interrupt Enable
033	0B3	133	1B3	233	2B3	333	3B3	FRMP Maintenance/Alarm Status Interrupt Enable
034	0B4	134	1B4	234	2B4	334	3B4	FRMP Framing Status Interrupt Indication
035	0B5	135	1B5	235	2B5	335	3B5	FRMP Maintenance/Alarm Status Interrupt Indication
036	0B6	136	1B6	236	2B6	336	3B6	FRMP Framing Status
037	0B7	137	1B7	237	2B7	337	3B7	FRMP Maintenance/Alarm Status
038	0B8	138	1B8	238	2B8	338	3B8	FRMP TS0 International/National Bits
039	0B9	139	1B9	239	2B9	339	3B9	FRMP CRC Error Counter-LSB
03A	0BA	13A	1BA	23A	2BA	33A	3BA	FRMP CRC Error Counter-MSB/TS16 Extra Bits
03B	0BB	13B	1BB	23B	2BB	33B	3BB	FRMP National Bit Code-word Interrupt Enable
03C	0BC	13C	1BC	23C	2BC	33C	3BC	FRMP National Bit Code-word Interrupts
03D	0BD	13D	1BD	23D	2BD	33D	3BD	FRMP National Bit Code-word
03E	0BE	13E	1BE	23E	2BE	33E	3BE	FRMP Frame pulse/Alarm/V5.2 Link ID Interrupt Enable
03F	0BF	13F	1BF	23F	2BF	33F	3BF	FRMP Frame Pulse/Alarm Interrupts
040	0C0	140	1C0	240	2C0	340	3C0	FRMG Configuration
041	0C1	141	1C1	241	2C1	341	3C1	FRMG Alarm/Diagnostic Control
042	0C2	142	1C2	242	2C2	342	3C2	FRMG International Bits
043	0C3	143	1C3	243	2C3	343	3C3	FRMG Extra Bits
044	0C4	144	1C4	244	2C4	344	3C4	FRMG Interrupt Enable
045	0C5	145	1C5	245	2C5	345	3C5	FRMG Interrupt Status
046	0C6	146	1C6	246	2C6	346	3C6	FRMG National Bit Code-word Select
047	0C7	147	1C7	247	2C7	347	3C7	FRMG National Bit Code-word
048	0C8	148	1C8	248	2C8	348	3C8	RHDLC #1, 2, 3 Configuration

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Table 62: E1 Mode Register Map - Direct Register (Continued)

E1 Address								Register
Framer 1	Framer 2	Framer 3	Framer4	Framer 5	Framer 6	Framer 7	Framer8	
049	0C9	149	1C9	249	2C9	349	3C9	RHDLC #1, 2, 3 Interrupt Control
04A	0CA	14A	1CA	24A	2CA	34A	3CA	RHDLC #1, 2, 3 Status
04B	0CB	14B	1CB	24B	2CB	34B	3CB	RHDLC #1, 2, 3 Data
04C	0CC	14C	1CC	24C	2CC	34C	3CC	RHDLC #1, 2, 3 Primary Address Match
04D	0CD	14D	1CD	24D	2CD	34D	3CD	RHDLC #1, 2, 3 Secondary Address Match
04E ~ 04F	0CE ~ 0CF	14E ~ 14F	1CE ~ 1CF	24E ~ 24F	2CE ~ 2CF	34E ~ 34F	3CE ~ 3CF	Reserved
050	0D0	150	1D0	250	2D0	350	3D0	THDLC #1, 2, 3 Configuration
051	0D1	151	1D1	251	2D1	351	3D1	THDLC #1, 2, 3 Upper Transmit Threshold
052	0D2	152	1D2	252	2D2	352	3D2	THDLC #1, 2, 3 Lower Transmit Threshold
053	0D3	153	1D3	253	2D3	353	3D3	THDLC #1, 2, 3 Interrupt Enable
054	0D4	154	1D4	254	2D4	354	3D4	THDLC #1, 2, 3 interrupt Status
055	0D5	155	1D5	255	2D5	355	3D5	THDLC #1, 2, 3 Transmit Data
056 ~ 058	0D6 ~ 0D8	156 ~ 158	1D6 ~ 1D8	256 ~ 258	2D6 ~ 2D8	356 ~ 358	3D6 ~ 3D8	Reserved
059	0D9	159	1D9	259	2D9	359	3D9	ELSB Interrupt Enable/ Status
05A	0DA	15A	1DA	25A	2DA	35A	3DA	ELSB Idle Code
05B	0DB	15B	1DB	25B	2DB	35B	3DB	Reserved
05C	0DC	15C	1DC	25C	2DC	35C	3DC	RPLC Configuration
05D	0DD	15D	1DD	25D	2DD	35D	3DD	RPLC µP Access Status
05E	0DE	15E	1DE	25E	2DE	35E	3DE	RPLC Channel Indirect Address/Control
05F	0DF	15F	1DF	25F	2DF	35F	3DF	RPLC Channel Indirect Data Buffer
060	0E0	160	1E0	260	2E0	360	3E0	TPLC Configuration
061	0E1	161	1E1	261	2E1	361	3E1	TPLC µP Access Status
062	0E2	162	1E2	262	2E2	362	3E2	TPLC Channel Indirect Address/Control
063	0E3	163	1E3	263	2E3	363	3E3	TPLC Channel Indirect Data Buffer
064	0E4	164	1E4	264	2E4	364	3E4	RCRB Configuration (COSS = 0) / RCRB COSS[30:25] (COSS = 1)
065	0E5	165	1E5	265	2E5	365	3E5	RCRB µP Access Status (COSS = 0) / RCRB COSS[24:17] (COSS = 1)
066	0E6	166	1E6	266	2E6	366	3E6	RCRB CH IND Addr/Control (COSS = 0) / RCRB COSS[16:9] (COSS = 1)
067	0E7	167	1E7	267	2E7	367	3E7	RCRB CH Indirect Data Buffer (COSS = 0) / RCRB COSS[8:1] (COSS = 1)
068	0E8	168	1E8	268	2E8	368	3E8	PMON Interrupt Enable/Status
069	0E9	169	1E9	269	2E9	369	3E9	PMON FER Count
06A	0EA	16A	1EA	26A	2EA	36A	3EA	PMON FEBE Count (LSB)
06B	0EB	16B	1EB	26B	2EB	36B	3EB	PMON FEBE Count (MSB)
06C	0EC	16C	1EC	26C	2EC	36C	3EC	PMON CRC Count (LSB)
06D	0ED	16D	1ED	26D	2ED	36D	3ED	PMON CRC Count (MSB)
06E ~ 06F	0EE ~ 0EF	16E ~ 16F	1EE ~ 1EF	26E ~ 26F	2EE ~ 2EF	36E ~ 36F	3EE ~ 3EF	Reserved
070								PRGD Control
071								PRGD Interrupt Enable/Status
072								PRGD Shift Register Length
073								PRGD Tap
074								PRGD Error Insertion
075 ~ 077								Reserved
078								PRGD Pattern Insertion #1

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Table 62: E1 Mode Register Map - Direct Register (Continued)

E1 Address								Register
Framer 1	Framer 2	Framer 3	Framer4	Framer 5	Framer 6	Framer 7	Framer8	
079								PRGD Pattern Insertion #2
07A								PRGD Pattern Insertion #3
07B								PRGD Pattern Insertion #4
07C								PRGD Pattern Detector #1
07D								PRGD Pattern Detector #2
07E								PRGD Pattern Detector #3
07F								PRGD Pattern Detector #4

Table 63: E1 Mode Register Map - Indirect Register

	Address	Register
RPLC Indirect Registers	20-3FH	Payload control byte for TS0 to TS 31
	40-5FH	Data trunk conditioning code for TS0 to TS31
	61-7FH	Signaling trunk conditioning code for TS1 to TS31
TPLC Indirect Registers	20-3FH	Payload control byte for TS0 to TS 31
	40-5FH	Idle code for TS0 to TS31
	61-7FH	Signaling control byte for TS1 to TS31
RCRB Indirect Registers	01-1FH / 21-3FH	Signaling data for TS1 to TS31
	41-5FH	Signaling control for TS1 to TS31

5.1.2 T1/J1 MODE REGISTER MAP

When the TEMODE (b0, 400H) is logic 1, the T1/J1 mode registers are accessed.

Table 64: T1/J1 Mode Register Map - Direct Register

T1/J1 Address								Register
Framer 1	Framer 2	Framer 3	Framer4	Framer 5	Framer 6	Framer 7	Framer8	
000	080	100	180	200	280	300	380	Receive Line Options
001	081	101	181	201	281	301	381	Receive Side System Interface Options
002	082	102	182	202	282	302	382	Back-plane Parity Configuration/Status
003	083	103	183	203	283	303	383	Receive Interface Configuration
004	084	104	184	204	284	304	384	Transmit Interface Configuration
005	085	105	185	205	285	305	385	Transmit Side System Interface Options
006	086	106	186	206	286	306	386	Transmit Framing and Bypass Options
007	087	107	187	207	287	307	387	Transmit Timing Options
008	088	108	188	208	288	308	388	Interrupt Source #1
009	089	109	189	209	289	309	389	Interrupt Source #2
00A	08A	10A	18A	20A	28A	30A	38A	Diagnostic
00B								Reserved
00C								Chip ID/ Global PMON Update
00D	08D	10D	18D	20D	28D	30D	38D	HDLC Micro Select/Framer Reset
00E								Framer Interrupt ID
00F								PRGD Positioning/control
010	090	110	190	210	29F	310	390	RJAT Interrupt Status

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Table 64: T1/J1 Mode Register Map - Direct Register (Continued)

T1/J1 Address								Register
Framer 1	Framer 2	Framer 3	Framer4	Framer 5	Framer 6	Framer 7	Framer8	
011	091	111	191	211	291	311	391	RJAT Reference Clock Divisor (N1)
012	092	112	192	212	292	312	392	RJAT Reference Clock Divisor (N2)
013	093	113	193	213	293	313	393	RJAT Configuration
014	094	114	194	214	294	314	394	TRSI Time Slot Offset
015	095	115	195	215	295	315	395	TRSI Bit Offset
016 ~ 017	096 ~ 097	116 ~ 117	196 ~ 197	216 ~ 217	296 ~ 297	316 ~ 317	396 ~ 397	Reserved
018	098	118	198	218	298	318	398	TJAT Interrupt Status
019	099	119	199	219	299	319	399	TJAT Reference Clock Divisor (N1)
01A	09A	11A	19A	21A	29A	31A	39A	TJAT Reference Clock Divisor (N2)
01B	09B	11B	19B	21B	29B	31B	39B	TJAT Configuration
01C	09C	11C	19C	21C	29C	31C	39C	Reserved
01D	09D	11D	19D	21D	29D	31D	39D	ELSB Interrupt Enable/Status
01E	09E	11E	19E	21E	29E	31E	39E	ELSB Idle Code
01F	09F	11F	19F	21F	29F	31F	39F	Reserved
020	0A0	120	1A0	220	2A0	320	3A0	T1 FRMP Configuration
021	0A1	121	1A1	221	2A1	321	3A1	T1 FRMP Interrupt Enable
022	0A2	122	1A2	222	2A2	322	3A2	T1 FRMP Interrupt Status
023 ~ 026	0A3 ~ 0A6	123 ~ 126	1A3 ~ 1A6	223 ~ 226	2A3 ~ 2A6	323 ~ 326	3A3 ~ 3A6	Reserved
027	0A7	127	1A7	227	2A7	327	3A7	Clock Monitor
028 ~ 029	0A8 ~ 0A9	128 ~ 129	1A8 ~ 1A9	228 ~ 229	2A8 ~ 2A9	328 ~ 329	3A8 ~ 3A9	Reserved
02A	0AA	12A	1AA	22A	2AA	32A	3AA	RBOM Configuration
02B	0AB	12B	1AB	22B	2AB	32B	3AB	RBOM Code Status
02C	0AC	12C	1AC	22C	2AC	32C	3AC	ALMD Configuration
02D	0AD	12D	1AD	22D	2AD	32D	3AD	ALMD Interrupt Enable
02E	0AE	121	1A1	221	2A1	321	3A1	ALMD Interrupt Status
02F	0AF	12F	1AF	22F	2AF	32F	3AF	ALMD Alarm Detection Status
030	0B0	130	1B0	230	2B0	330	3B0	TPLC Configuration
031	0B1	131	1B1	231	2B1	331	3B1	TPLC µP Access Status
032	0B2	132	1B2	232	2B2	332	3B2	TPLC Channel Indirect Address/Control
033	0B3	133	1B3	233	2B3	333	3B3	TPLC Channel Indirect Data Buffer
034	0B4	134	1B4	234	2B4	334	3B4	THDLC #1, 2, 3 Configuration
035	0B5	135	1B5	235	2B5	335	3B5	THDLC #1, 2, 3 Upper Transmit Threshold
036	0B6	136	1B6	236	2B6	336	3B6	THDLC #1, 2, 3 Lower Transmit Threshold
037	0B7	137	1B7	237	2B7	337	3B7	THDLC #1, 2, 3 Interrupt Enable
038	0B8	138	1B8	238	2B8	338	3B8	THDLC #1, 2, 3 Interrupt Status
039	0B9	139	1B9	239	2B9	339	3B9	THDLC #1, 2, 3 Transmit Data
03A ~ 03B	0BA ~ 0BB	13A ~ 13B	1BA ~ 1BB	23A ~ 23B	2BA ~ 2BB	33A ~ 33B	3BA ~ 3BB	Reserved
03C	0BC	13C	1BC	23C	2BC	33C	3BC	IBCD Configuration
03D	0BD	13D	1BD	23D	2BD	33D	3BD	IBCD Interrupt Enable/Status
03E	0BE	13E	1BE	23E	2BE	33E	3BE	IBCD Active Code
03F	0BF	13F	1BF	23F	2BF	33F	3BF	IBCD Deactivate Code
040	0C0	140	1C0	240	2C0	340	3C0	RCRB Configuration (COSS = 0) / RCRB COSS[30:25] (COSS = 1)
041	0C1	141	1C1	241	2C1	341	3C1	RCRB µP Access Status (COSS = 0) / RCRB COSS[24:17] (COSS = 1)

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Table 64: T1/J1 Mode Register Map - Direct Register (Continued)

T1/J1 Address								Register
Framer 1	Framer 2	Framer 3	Framer4	Framer 5	Framer 6	Framer 7	Framer8	
042	0C2	142	1C2	242	2C2	342	3C2	RCRB CH IND Addr/Control (COSS = 0) / RCRB COSS[16:9] (COSS = 1)
043	0C3	143	1C3	243	2C3	343	3C3	RCRB CH Indirect Data Buffer (COSS = 0) / RCRB COSS[8:1] (COSS = 1)
044	0C4	144	1C4	244	2C4	344	3C4	FRMG Configuration
045	0C5	145	1C5	245	2C5	345	3C5	FRMG Alarm Transmit
046	0C6	146	1C6	246	2C6	346	3C6	IBCG Configuration
047	0C7	147	1C7	247	2C7	347	3C7	IBCG Loop-back Code
048	0C8	148	1C8	248	2C8	348	3C8	Reserved
049	0C9	149	1C9	249	2C9	349	3C9	PMON Interrupt Enable/Status
04A	0CA	14A	1CA	24A	2CA	34A	3CA	PMON BEE Count (LSB)
04B	0CB	14B	1CB	24B	2CB	34B	3CB	PMON BEE Count (MSB)
04C	0CC	14C	1CC	24C	2CC	34C	3CC	PMON FER Count (LSB)
04D	0CD	14D	1CD	24D	2CD	34D	3CD	PMON FER Count (MSB)
04E	0CE	14E	1CE	24E	2CE	34E	3CE	PMON OOF Count
04F	0CF	14F	1CF	24F	2CF	34F	3CF	PMON COFA Count
050	0D0	150	1D0	250	2D0	350	3D0	RPLC Configuration
051	0D1	151	1D1	251	2D1	351	3D1	RPLC µP Access Status
052	0D2	152	1D2	252	2D2	352	3D2	RPLC Channel Indirect Address/Control
053	0D3	153	1D3	253	2D3	353	3D3	RPLC Channel Indirect Data Buffer
054	0D4	154	1D4	254	2D4	354	3D4	RHDLC #1, 2, 3 Configuration
055	0D5	155	1D5	255	2D5	355	3D5	RHDLC #1, 2, 3 Interrupt Control
056	0D6	156	1D6	256	2D6	356	3D6	RHDLC #1, 2, 3 Status
057	0D7	157	1D7	257	2D7	357	3D7	RHDLC #1, 2, 3 Data
058	0D8	158	1D8	258	2D8	358	3D8	RHDLC #1, 2, 3 Primary Address Match
059	0D9	159	1D9	259	2D9	359	3D9	RHDLC #1, 2, 3 Secondary Address Match
05A ~ 05C	0DA ~ 0DC	15A ~ 15C	1DA ~ 1DC	25A ~ 25C	2DA ~ 2DC	35A ~ 35C	3DA ~ 3DC	Reserved
05D	0DD	15D	1DD	25D	2DD	35D	3DD	TBOM Code
05E ~ 05F	0DE ~ 0DF	15E ~ 15F	1DE ~ 1DF	25E ~ 25F	2DE ~ 2DF	35E ~ 35F	3DE ~ 3DF	Reserved
060								PRGD Control
061								PRGD Interrupt Enable/Status
062								PRGD Shift Register Length
063								PRGD Tap
064								PRGD Error Insertion
065 ~ 067								Reserved
068								PRGD Pattern Insertion #1
069								PRGD Pattern Insertion #2
06A								PRGD Pattern Insertion #3
06B								PRGD Pattern Insertion #4
06C								PRGD Pattern Detector #1
06D								PRGD Pattern Detector #2
06E								PRGD Pattern Detector #3
06F								PRGD Pattern Detector #4
070	0F0	170	1F0	270	2F0	370	3F0	RHDLC 2 (TXCISEL = 0) Link Control / THDLC 2 (TXCISEL = 1) Link Control

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Table 64: T1/J1 Mode Register Map - Direct Register (Continued)

T1/J1 Address								Register
Framer 1	Framer 2	Framer 3	Framer4	Framer 5	Framer 6	Framer 7	Framer8	
071	0F1	171	1F1	271	2F1	371	3F1	RHDLC 2 (TXCISEL = 0) bits select / THDLC 2 (TXCISEL = 1) bits select
072 ~ 076	0F2 ~ 0F6	172 ~ 176	1F2 ~ 1F6	272 ~ 276	2F2 ~ 0F6	372 ~ 376	3F2 ~ 3F6	Reserved
077	0F7	177	1F7	277	2F7	377	3F7	RESI Time Slot Offset
078	0F8	178	1F8	278	2F8	378	3F8	RESI Bit Offset

Table 65: T1/J1 Mode Register Map - Indirect Register

	Address	Register
RPLC Indirect Register	01-18H	Payload control byte for CH1 to CH24
	19-30H	Data trunk conditioning code for CH1 to CH24
	31-48H	Signaling trunk conditioning code for CH1 to CH24
TPLC Indirect Register	01-18H	Payload control byte for CH1 to CH24
	19-30H	Idle code for CH1 to CH24
	31-48H	Signaling control byte for CH1 to CH24
RCRB Indirect Register	01-18H / 21-38H	Signaling data for CH1 to CH24
	41-58H	Signaling control for CH1 to CH24

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5.2 REGISTER DESCRIPTION

E1 Or T1 / J1 Mode Selection (400H)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	Reserved							TEMODE
Type								R/W
Default								1

TEMODE:

This bit chooses the operation mode globally for the chip.

= 0: The chip operates in the E1 mode.

= 1: The chip operates in the T1/J1 mode.

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5.2.1 E1 MODE

E1 Receive Path Line Options (000H, 080H, 100H, 180H, 200H, 280H, 300H, 380H)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	FIFOBYP	UNF	WORDERR	CNTNFAS	AUTOYELLOW	AUTORED	AUTOOOF	AUTOUPDATE
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

FIFOBYP:

This bit decides whether the received data should pass through or bypass the Receive Jitter Attenuation FIFO.

= 0: The received data pass through the RJAT FIFO.

= 1: The RJAT FIFO is bypassed. The delay is reduced by typically 24 bits.

UNF:

= 0: The Frame Processor operates normally.

= 1: Frame searching is disabled, the Receive CAS/RBS Buffer holds the signaling frozen, and Auto_OOF function, if enabled, will consider OOF to be declared.

WORDERR, CNTNFAS:

WORDERR	CNTNFAS	Framing Bit Error
0	0	Each bit error in a 7-bit FAS pattern is counted as a single framing bit error.
1	0	One or more than one bit errors in a 7-bit FAS pattern is counted as a single framing bit error.
0	1	Each bit error in a 7-bit FAS pattern is counted as a single framing bit error, and a logic 0 in the second bit of TS0 of NFAS is counted as a single bit error too.
1	1	An 8-bit Error Word is consisted of a 7-bit FAS pattern and the second bit of TS0 in the next NFAS frame. One or more than one bit errors in this 8-bit Error Word is counted as a single framing bit error.

AUTOYELLOW:

This bit decides whether to send Yellow Alarm signal automatically.

= 0: The automatic Yellow Alarm Transmission is disabled. It means that the RAI bit, the 3rd bit of NFAS frame, can only be transmitted when the REMAIS (b3, E1-041H) is set to '1'.

= 1: The automatic Yellow Alarm Transmission is enabled. It means that the RAI bit (the 3rd bit of NFAS frame) in the transmit data stream will be set to '1' automatically during loss of frame alignment or receiving AIS. The G706RAI (b0, E1-00EH) is used to select the conditions, under which the Yellow Alarm signal will be transmitted automatically.

AUTORED:

This bit decides whether to start trunk conditioning (replacing data on RSDn with the data stored in the data trunk conditioning registers in RPLC) automatically when Red Alarm is declared.

= 0: The trunk conditioning is not activated automatically when RED (b3, E1-037 H) becomes '1'.

= 1: The trunk conditioning will be initiated automatically when the RED (b3, E1-037H) becomes '1'.

AUTOOOF:

This bit decides whether to start trunk conditioning (replacing data on RSDn with the data stored in the data trunk conditioning registers in RPLC) automatically in the duration of loss of basic frame.

= 0: The trunk conditioning is not activated automatically when the OOFV (b6, E1-036 H) becomes '1'.

= 1: The trunk conditioning will be activated automatically when the OOFV (b6, E1-036 H) becomes '1'.

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AUTOUPDATE:

This bit decides whether the PMON and PRGD registers are automatically updated once every second.

= 0: The PMON and PRGD registers are not automatically updated. They can only be updated by MCU operation.

= 1: The PMON and PRGD registers will be automatically updated once every second.

E1 Receive Side System Interface Options (001H, 081H, 101H, 181H, 201H, 281H, 301H, 381H)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	LRCKFALL	RSSIG_EN	RSCKSEL	MRBS	MRBC	OOSMFAIS	TRKEN	RXMTKC
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	1	0	0	0	0	0	0

LRCKFALL:

This bit chooses the active edge of LRCKn to sample the data on the corresponding LRDn.

= 0: the rising edge is chosen.

= 1: the falling edge is chosen.

RSSIG_EN:

When the Receive Clock Slave Mode is enabled (RSCKSLV = 1, b5, E1-010H), this bit configures the receive side system interface.

= 0: the Receive Clock Slave RSCK Reference Mode is enabled. The RSCKn/RSSIGn pin will be used as RSCKn to output a 2.048 MHz jitter attenuated version of LRCKn or an 8 KHz clock.

= 1: the Receive Clock Slave External Signaling mode is enabled. The RSCKn/RSSIGn pin is used as RSSIGn to output the extracted signaling data. Each time-slot signaling bits are time slot aligned with RSDn data stream and located in the lower nibble (b5b6b7b8).

RSCKSEL:

When the Receive Clock Slave RSCK Reference Mode is enabled, this bit chooses the frequency of RSCKn.

= 0: RSCKn outputs an 8 KHz timing reference that is generated by dividing the jitter attenuated version of LRCKn.

= 1: RSCKn outputs a jitter attenuated version of the 2.048 MHz Line Receive Clock (LRCKn).

MRBS:

In the Receive Multiplexed mode, this bit decides which bus the corresponding framer will use to output the received data.

= 0: The first multiplexed bus (MRSD[1], MRSFS[1], MRSSIG[1]) is chosen.

= 1: The second multiplexed bus (MRSD[2], MRSFS[2], MRSSIG[2]) is chosen.

MRBC:

This bit turns on or off the transmission of received data from the corresponding framer to the selected multiplexed receive bus. Users should complete the setting in the MRBS (b4, E1-001H) before enabling this bit. This bit of the framers that are output to the same multiplexed bus must be set to the same value.

= 0: The corresponding framer will not output its data stream on the multiplexed bus.

= 1: The corresponding framer will output its data stream on the multiplexed bus.

OOSMFAIS:

This bit decides whether to send Alarm Indication Signals (All Ones Signals) on RSSIGn to the system side in the condition of out of signaling multi-frame. This bit affects the corresponding time slot of the MRSSIGn data stream if the multiplexed bus is enabled.

= 0: The output on the RSSIGn/MRSSIG pin will not be affected by the indication of out of Signaling Multi-Frame.

= 1: The output on the RSSIGn/MRSSIG pin will be set to all ‘One’s in the condition of out of Signaling Multi-Frame.

TRKEN:

This bit decides whether to substitute the data on RSDn with the contents in the ELSB Idle Code Register during out of Basic frame. After substitution. The ELSB Idle Code can still be overwritten by the contents in RPLC Data Trunk Conditioning Registers and Signaling Trunk Conditioning Reg-

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isters on per time slot basis. This bit only has effect in the Receive Clock Slave mode, and it affects the corresponding time slot of multiplexed bus MRSD when multiplexed bus operation is enabled.

= 0: ELSB Idle Code Substitution is disabled.

= 1: Data in all time slots on RSDn will be replaced by the contents in ELSB Idle Code Register during out of Basic frame.

RXMTKC:

This bit decides how to substitute the received data stream on RSDn and RSSIGn with the contents in the RPLC Data Trunk Conditioning Registers and the RPLC Signaling Trunk Conditioning Registers. This bit affects the corresponding time slot of MRSD and MRSSIG if the multiplexed backplane is enabled.

= 0: The data and the signaling are substituted on a per-timeslot basis in accordance with the control bits contained in the per-timeslot Payload Control Byte registers in the RPLC.

= 1: The data on RSDn of all time slots is replaced with the data contained in the Data Trunk Conditioning registers in RPLC, and the signaling on RSSIGn of all time slots is replaced with the data contained in the Signaling Trunk Conditioning registers. To enable this function, the PCCE (b0, E1-05CH) of the RPLC must be set to logic 1.

E1 Transmit Path Configuration (002H, 082H, 102H, 182H, 202H, 282H, 302H, 382H)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	FIFOBYP	TAISEN	Reserved	PATHCRC	Reserved	TSFSRISE	Reserved	LTCKRISE
Type	R/W	R/W		R/W		R/W		R/W
Default	0	0		0		0		0

FIFOBYP:

This bit decides whether the transmit data should pass through or bypass the Transmit Jitter Attenuation FIFO.

= 0: The transmit data pass through the TJAT FIFO.

= 1: The TJAT FIFO is bypassed. The delay is reduced by typically 24 bits.

TAISEN:

This bit enables the line interface to generate an un-framed all-ones Alarm Indication Signal on the LTDn pin.

= 0: normal operation.

= 1: LTDn transmits all ‘One’s.

PATHCRC:

This bit allows upstream bit errors to be transmitted to the downstream transparently. When the data stream on TSDn is already in the CRC Multi-Frame format, and the IDT82V2108 is going to change some bits in the data stream, this bit decides whether to replace the original CRC-4 bits with re-calculated CRC-4 bits or just modify the original CRC-4 bits according to the contribution caused by changing bits in the data stream. This bit only takes effect when the FPTYP (b1, E1-019H) is set to ‘1’ and one of the INDIS (b1, E1-040H) or FDIS (b3, E1-045H) is set to ‘1’.

= 0: A new re-calculated CRC-4 value will overwrite the incoming CRC-4 word. As the new CRC-4 value is transmitted to downstream, the bit errors in upstream can not be detected by the downstream.

= 1: The incoming CRC-4 value is modified to just reflect the bit changes made by the IDT82V2108. If there is any bit error in the upstream, it will be transmitted to the downstream transparently, and the downstream machine can detect it.

TSFSRISE:

This bit chooses the active edge of TSCCKB to update the Transmit Frame Pulse on the TSFSn pin.

= 0: the signal on TSFSn is updated on the falling edge of TSCCKB.

= 1: the signal on TSFSn is updated on the rising edge of TSCCKB.

LTCKRISE:

This bit chooses the active edge of LTCKn to update the data on LTDn.

= 0: the data on LTDn pin is updated on the falling edge of LTCKn.

= 1: the data on LTDn pin is updated on the rising edge of LTCKn.

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E1 Transmit Side System Interface Options (003H, 083H, 103H, 183H, 203H, 283H, 303H, 383H)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	Reserved	TSSIG_EN	Reserved	MTBS	Reserved			
Type		R/W		R/W				
Default		1		0				

TSSIG_EN:

In Transmit Clock Slave mode (TSCKSLV = 1, b5, E1-018H), this bit configures the transmit side system interface.
= 0: Transmit Clock Slave TSFS Enable mode is selected. The TSFSn/TSSIGn pin is used as TSFSn output.
= 1: Transmit Clock Slave External Signaling mode is selected. The TSFSn/TSSIGn pin is used as TSSIGn input.
In Transmit Multiplexed mode, this bit must be set to '1'.

MTBS:

In Transmit Multiplexed mode, this bit determines which multiplexed bus will interface with the corresponding framer.
= 0: The incoming data is taken from the first multiplexed bus (MTSD1, MTSSIG1).
= 1: The incoming data is taken from the second multiplexed bus (MTSD2, MTSSIG2).

E1 Transmit Timing Options (004H, 084H, 104H, 184H, 204H, 284H, 304H, 384H)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	Reserved		TJATREF_SEL[2]	TJATREF_SEL[1]	TJATREF_SEL[0]	LTCK_SEL[2]	LTCK_SEL[1]	LTCK_SEL[0]
Type			R/W	R/W	R/W	R/W	R/W	R/W
Default			1	0	0	1	0	1

TJATREF_SEL[2:0] - Transmit Jitter Attenuation DPLL Input Reference Clock Selection

The TJATREF_SEL[2:0] select the input reference clock for the TJAT DPLL.

TJATREF_SEL[2:0]	Input Reference Clock
000	TSCCKA / 8
001	TSCCKB
010	LRCK
011	TSCCKA
100	XCK / 24
Others	TSCCKB

LTCK_SEL[2:0] - Line Transmit Clock (LTCKn) Selection

The LTCK_SEL[2:0] select the line transmit clock.

LTCK_SEL[2:0]	Line Transmit Clock
000	TSCCKA / 8
001	TSCCKB
010	LRCK
011	TSCCKA
100	XCK / 24
Others	A smoothed clock output from the TJAT DPLL

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E1 Interrupt Source #1 (005H, 085H, 105H, 185H, 205H, 285H, 305H, 385H)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	PMON	FRMG	FRMP	PRGD	ELSB	RHDLC#1	RHDLC#2	RHDLC#3
Type	R	R	R	R	R	R	R	R
Default	X	X	X	X	X	X	X	X

Bits in this register indicate which function block introduced an interrupt signal on the $\overline{INT}$ pin. Reading this register does not remove the interrupt indication. To remove the interrupt indication on the $\overline{INT}$ pin, the corresponding interrupt status register must be read.

E1 Interrupt Source #2 (006H, 086H, 106H, 186H, 206H, 286H, 306H, 386H)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	TRSI	Reserved	TJAT	RJAT	THDLC#1	THDLC#2	THDLC#3	RCRB
Type	R		R	R	R	R	R	R
Default	X		X	X	X	X	X	X

Bits in this register indicate which function block introduced an interrupt signal on the $\overline{INT}$ pin. Reading this register does not remove the interrupt indication. To remove the interrupt indication on the $\overline{INT}$ pin, the corresponding interrupt status register must be read.

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E1 Diagnostics (007H, 087H, 107H, 187H, 207H, 287H, 307H, 387H)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	Reserved			LINELB	V52DIS	DDLB	RAIS	TXDIS
Type				R/W	R/W	R/W	R/W	R/W
Default				0	0	0	0	0

LINELB:

Line Loopback means that the transmit line interface data and clock (LTDn and LTCKn) are internal directly comes from the received line data and clock (LRDn and LRCKn). The loop back data stream can pass through the Receive Jitter Attenuator or bypass the Receive Jitter Attenuator (if the Receive Jitter Attenuator is configured to be bypassed).

= 0: Line loop back is disabled.

= 1: Line loop back is enabled.

V52DIS:

= 0: All HDLC controllers of the corresponding framer are available to use.

= 1: Only the first HDLC controller in receive direction (RHDLC#1) and transmit direction (THDLC#1) is available to use, the remaining HDLC controllers are disabled.

Note that this bit can not be reset by software reset. It can only be reset by hardware reset.

DDLB:

Digital Loopback means that the received line data and clock (LRDn and LRCKn) are internal directly comes from the transmit line data and clock (LTDn and LTCKn) without the Receive Jitter Attenuator.

= 0: Digital loop back is disabled.

= 1: Digital loop back is enabled.

RAIS:

= 0: normal operation.

= 1: Force the data output on RSDn to be all ‘One’s, and freeze the signal on RSSIGn at the current valid signaling in Receive Clock Slave External Signaling mode. In Receive Multiplexed mode, the data of the corresponding framer output on MRSD is forced to be all ‘One’s, and the signal of the corresponding framer output on MRSSIG is frozen at the current valid signaling.

TXDIS:

= 0: normal transmission.

= 1: Force the data to be transmitted on the TLDn pin to be all ‘Zero’s.

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E1 Revision / Chip ID / Global PMON Update (009H)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	TYPE[2]	TYPE[1]	TYPE[0]	ID[4]	ID[3]	ID[2]	ID[1]	ID[0]
Type	R	R	R	R	R	R	R	R
Default	0	0	0	0	0	0	0	1

Writing to this register causes all Performance Monitor and PRGD Generator/Detector counters to be updated simultaneously.

TYPE[2:0]:

TYPE[2:0] are fixed to 000, representing the IDT82V2108 chip.

ID[4:0]:

Chip revision. '00H' is for the first version.

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E1 Data Link Micro Select / Framer Reset (00AH, 08AH, 10AH, 18AH, 20AH, 28AH, 30AH, 38AH)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	RHDLCSEL[1]	RHDLCSEL[0]	THDLCSEL[1]	THDLCSEL[0]	TXCISEL	Reserved		RESET
Type	R/W	R/W	R/W	R/W	R/W			R/W
Default	X	X	X	X	X			0

RHDLCSEL[1:0]:

The RHDLCSEL[1:0] select one of the three HDLC Receivers to be accessed by the microprocessor. At one time, the microprocessor can only access one HDLC controller. These bits must be set before using the HDLC controller.

RHDLCSEL[1:0]	HDLC Receiver
00	RHDLC #1
01	RHDLC #2
10	RHDLC #3
11	Reserved

THDLCSEL[1:0]:

The THDLCSEL[1:0] select one of the three HDLC Transmitters to be accessed by the microprocessor. At one time, the microprocessor can only access one HDLC controller. These bits must be set before using the HDLC controller.

THDLCSEL[1:0]	HDLC Transmitter
00	THDLC #1
01	THDLC #2
10	THDLC #3
11	Reserved

TXCISEL:

The registers addressed from E1-028H to E1-02DH are shared by HDLC Receiver and HDLC Transmitter. They decide the position of the extracted bit in the received data stream and the inserted bit in the transmitting data stream respectively. So this bit is used to decide whether the Read/Write operation on the registers addressed from E1-028H to E1-02DH is for HDLC receiver or for HDLC transmitter.

= 0: The Read/Write operation on registers addressed from 028 H to 02D H is for HDLC receiver.

= 1: The Read/Write operation on registers addressed from 028H to 02D H is for HDLC transmitter.

RESET:

This bit implements a software reset for individual framer.

= 0: normal operation.

= 1: The corresponding framer is held in reset. However, this bit, the bits in this register and the V52DIS (b3, E1-007H) will not be reset. Therefor, a logic 0 must be written to bring the framer out of reset. Holding the framer in a reset state effectively puts it into a low power standby mode. A hardware reset clears the RESET bit, the bits in this register and the V52DIS (b3, E1-007H).

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E1 Interrupt ID (00BH)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	INT[8]	INT[7]	INT[6]	INT[5]	INT[4]	INT[3]	INT[2]	INT[1]
Type	R	R	R	R	R	R	R	R
Default	X	X	X	X	X	0	0	0

This register indicates which one of the eight framers introduced the interrupt $\overline{INT}$ pin to be logic low. When any one of the eight framers introduced the interrupt, the corresponding bit in the INT[8:1] will be '1'.

E1 Pattern Generator / Detector Positioning / Control (00CH)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	PRGDSEL[2]	PRGDSEL[1]	PRGDSEL[0]	Reserved		RXPATGEN	UNF_GEN	UNF_DET
Type	R/W	R/W	R/W			R/W	R/W	R/W
Default	0	0	0			0	0	0

The IDT82V2108 has only one PRBS Generator/Detector (PRGD) shared by all eight framers. At one time, only one framer can use this PRGD. This register selects which framer will use the PRGD and how the PRGD will be used.

PRGDSEL[2:0]:

PRGDSEL[2:0] select one of the eight framers to be tested by the PRGD block.

PRGDSEL[2:0]	Selected Framer
000	Framer 1
001	Framer 2
010	Framer 3
011	Framer 4
100	Framer 5
101	Framer 6
110	Framer 7
111	Framer 8

RXPATGEN:

= 0: The pattern in PRGD is generated in the transmit path and is detected in the receive path.

= 1: The pattern in PRGD is generated in the receive path and is detected in the transmit path.

UNF_GEN:

= 0: Which time slots of the selected path will be replaced by the PRGD pattern is specified in TPLC or RPLC.

= 1: All 32 time slots of the selected path will be replaced by the PRGD pattern.

UNF_DET:

= 0: Which time slots of the selected path will be detected by PRGD pattern is specified in TPLC or RPLC.

= 1: All 32 time slots of the selected path will be detected by PRGD pattern.

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E1 Clock Monitor (00DH, 08DH, 10DH, 18DH, 20DH, 28DH, 30DH, 38DH)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	Reserved			XCK	TSCCKB	TSCCKA	RSCCK	LRCK
Type				R	R	R	R	R
Default				X	X	X	X	X

This register provides activity monitoring on the IDT82V2108 clocks. When a monitored clock signal makes a low to high transition, the corresponding bit in this register is set to '1', and this bit remains to be '1' until this register is read. After a read operation on this register, all the bits in this register will be cleared to '0'. A lack of transitions of the monitored clock will be indicated by '0' in the corresponding bit, which means that the clock fails. This register should be read periodically to detect clock failures.

XCK:
= 0: After the bit is read.
= 1: A low to high transition occurs on XCK.

TSCCKB:
= 0: After the bit is read.
= 1: A low to high transition occurs on TSCCKB.

TSCCKA:
= 0: After the bit is read.
= 1: A low to high transition occurs on TSCCKA.

RSCCK:
= 0: After the bit is read.
= 1: A low to high transition occurs on RSCCK.

LRCK:
= 0: After the bit is read.
= 1: A low to high transition occurs on LRCK.

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E1 Receive Path Frame Pulse Configuration (00EH, 08EH, 10EH, 18EH, 20EH, 28EH, 30EH, 38EH)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	Reserved				PERTS_RSFS	REF_MRSFS	OOCMFE0	G706RAI
Type					R/W	R/W	R/W	R/W
Default					0	0	0	0

PERTS_RSFS, REF_MRSFS:

PERTS_RSFS	REF_MRSFS	Pulse on the RSFSn/MRSFS
0	0	The pulse output on the RSFS/MRSFS pin is forced to be logic 0.
1	0	The signal on the RSFS/MRSFS pin is determined by the ROHM, BRXSMFP, BRCMFP and ALTIFP (b3b2b1b0, E1-011 H).
X	1	RSFSn/MRSFS contains a reference frame pulse identical to the receive system side common frame pulse on the RSCFS/ MRSCFS pin.

In Receive Multiplexed mode, these two bits in the eight framers should be set to the same value.

OOCMFE0:

This bit chooses one of two operation modes concerning the transmission of E-bits when the framer is out of CRC-4 multiframe.

= 0: Transmit 'One's for the E-bits while out of CRC-4 Multi-Frame.

= 1: Transmit 'Zero's for the E-bits while out of CRC-4 Multi-Frame. (This setting is compliant with the CRC-4 to non-CRC-4 interworking procedure in Annex B of G.706).

G706RAI:

When the AUTOYELLOW (b3, E1-00H) is set as '1', which means the RAI bit will be transmitted automatically in certain conditions, this bit chooses one of two criteria to define the conditions. If the AUTOYELLOW (b3, E1-00H) is '0', G706RAI does not have any effect.

= 0: The RAI bit will be transmitted when out of Basic Frame, when AISD is declared, when CRC-4 to non-CRC-4 interworking is declared or when the off-line searching indicates out of Basic frame. This definition follows the ETSI standards.

= 1: The RAI bit will be transmitted when out of Basic frame or when AISD is declared, but not when CRC-4 to non-CRC-4 interworking is declared nor when offline out-of frame is declared. This definition follows the Annex B of G.706.

E1 Receive Backplane Configuration (010H, 090H, 110H, 190H, 210H, 290H, 310H, 390H)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	FRACTN[1]	FRACTN[0]	RSCKSLV	DE	FE	CMS	RATE[1]	RATE[0]
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	1	1	1	0	0	0

FRACTN[1:0]:

When Receive Clock Master mode is enabled (RSCKSLV = 0, b5, E1-010H), these two bits selects one of the operation modes shown in the following table. The two bits will be ignored if the Receive Clock Slave mode is enabled (RSCKSLV = 1, b5, E1-010H).

FRACTN[1:0]	Operation Mode
0 0	Receive Clock Master Full E1 mode
0 1	Reserved
1 0	Receive Clock Master Fractional E1 mode
1 1	Receive Clock Master Fractional E1 with F-bit mode

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'Full E1' mode means that the received entire frame (256 bits) is clocked out from the RSDn pin, and there are no gaps in the RSCKn clock pulse.

'Fractional E1' mode means that RSCKn only clocks out on the selected time slots, and RSCKn does not pulse during those un-selected time slots. The time slots selection is decided by the DTRKC/NxTS (b6, E1-RPLC-Indirect Register-20-3F H).

'Fractional E1 with F-bit' mode is to support ITU recommendation G.802 where 1.544 Mbit/s data is carried within a 2.048 Mbit/s data stream. In this configuration, bits from the second bit of TS 26 to the last bit of the Basic Frame are suppressed, and the remaining bits can be gapped by setting the DTRKC/NxTS (b6, E1-RPLC-Indirect Register-20-3F H).

RSCKSLV:

= 0: Receive Clock Master mode is enabled.

= 1: Received Clock Slave mode is enabled.

This bit must be set to '1' to support multiplexed backplane.

DE:

= 0: The signal on the RSDn and RSSIGn pins is updated on the falling edge of RSCCK or the RSCK.

= 1: The signal on the RSDn and RSSIG pins is updated on the rising edge of RSCCK or the RSCK.

In Receive Multiplexed mode, the DE in all eight framers should be set to the same value.

FE:

If the FE is not equal to the DE, the frame pulse will be sampled or updated one clock edge after the corresponding data pulse.

= 0: The signal on the RSCFS pin is sampled or signal on the RSFSn pin is updated on the falling edge of RSCCK or RSCKn.

= 1: The signal on the RSCFS pin is sampled or signal on the RSFSn pin is updated on the rising edge of RSCCK or the RSCKn.

In Receive Multiplexed mode, the FE in all eight framers should be set to the same value.

CMS:

= 0: The clock frequency of RSCCK/MRSCCK is the same as the bit rate of the backplane.

= 1: The clock frequency of RSCCK/MRSCCK is double the bit rate of the backplane.

The CMS of all eight framers should be set to the same value.

RATE[1:0]:

These bits determine the bit rate of the received data stream on the backplane. Note that to operate in Receive Multiplexed mode, the RATE[1:0] in all eight framers should be configured to select the 8.192 Mbit/s backplane bit rate. When the RATE[1:0] select the 8.192 Mbit/s, the RSCKSLV (b5, E1-010H) must be set to '1'.

RATE[1:0]	Backplane Rate
0 0	Reserved
0 1	2.048M bit/s
1 0	Reserved
1 1	8.192M bit/s

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E1 Receive Backplane Frame Pulse Configuration (011H, 091H, 111H, 191H, 211H, 291H, 311H, 391H)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	Reserved	FPINV	FPMODE	Reserved	ROHM	BRXSMFP	BRXCMFP	ALTIFP
Type		R/W	R/W		R/W	R/W	R/W	R/W
Default		0	1		0	0	0	0

FPINV:

= 0: Framing pulse RSCFS and RSFSn/MRSFS are active high.

= 1: Framing pulse RSCFS and RSFSn/MRSFS are active low.

When this bit is used to indicate the active pulse for RSCFS or MRSFS, then it should be set to the same value for all eight framers.

FPMODE:

This bit decides whether to use RSCFS as the framing pulse or not. In Receive Clock Master mode (RSCKSLV = 0, b5, E1-010H), the FPMODE must be '0'.

= 0: RSCFS/MRSCFS is unused.

= 1: RSCFS/MRSCFS is used.

In Receive Multiplexed mode, the FPMODE in all eight framers should be set to the same value.

ROHM:

When the PERTS_RSFS and the REF_MRSFS (b3~2, E1-00EH) are '1' and '0' respectively, this bit decides whether to use RSFSn to indicate TS0 and TS16. Details are tabulated in the following table.

BRXSMFP, BRXCMFP:

When the PERTS_RSFS and the REF_MRSFS (b3~2, E1-00EH) are '1' and '0' respectively, these two bits, together with the ALTIFP bit, select the output signal seen on the RSFSn pin. Details are tabulated in the following table.

ALTIFP:

When the RSFSn pin is configured to output the framing pulse for Basic Frame, Signaling Multiframe or CRC Multiframe, this bit permits suppression of every other framing pulse. The following table shows the details for the different configurations of RSFSn.

ROHM	BRXSMFP	BRXCMFP	ALTIFP	RSFSn / MRSFS Indication
0	0	0	0	RSFSn asserts for 1 bit cycle on the first bit of each Basic Frame output on RSDn.
0	0	0	1	RSFSn asserts for 1 bit cycle on the first bit of every second Basic Frame output on RSDn.
0	0	1	0	RSFSn asserts for 1 bit cycle on the first bit of the first frame of each CRC Multi-Frame output on RSDn (in case CRC Multi-Frame is disabled, RSFSn asserts every 16 frames).
0	0	1	1	RSFSn asserts for 1 bit cycle on the first bit of the first frame of every second CRC Multi-Frame output on RSDn (in case CRC Multi-Frame is disabled, RSFSn asserts every 32 frames).
0	1	0	0	RSFSn asserts for 1 bit cycle on the first bit of the first frame of each Signaling Multi-Frame output on RSDn (in case Signaling Multi-Frame is disabled, RSFSn asserts every 16 frames).
0	1	0	1	RSFSn asserts for 1 bit cycle on the first bit of the first frame of every second Signaling Multi-Frame output on RSDn (in case Signaling Multi-Frame is disabled, RSFSn asserts every 32 frames).
0	1	1	0	RSFSn goes high/low at the start of the first bit of the first frame of each Signaling Multi-Frame, and goes the opposite at the end of the first bit of the first frame of each CRC Multi-Frame.
0	1	1	1	RSFSn goes high/low at the start of the first bit of the first frame of every second Signaling Multi-Frame, and goes the opposite at the end of the first bit of the first frame of every second CRC Multi-Frame.
1	X	X	X	The RSFSn pin pulses during the entire TS0 period and the entire TS16 period.

In Receive Multiplexed mode, when the PERTS_RSFS and the REF_MRSFS (b3~2, E1-00EH) are '1' and '0' respectively, the MRSFS can only indicate the first bit of a Basic Frame of the selected first framer no matter what is set in the ROHM, BRXSMFP, BRXCMFP and ALTIFP.

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E1 Receive Backplane Parity / F-bit Configuration (012H, 092H, 112H, 192H, 212H, 292H, 312H, 392H)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	RPTYP	RPTYE	FIXF	FIXPOL	PTY_EXTD	Reserved	TRI[1]	TRI[0]
Type	R/W	R/W	R/W	R/W	R/W		R/W	R/W
Default	0	0	0	0	0		0	0

RPTYP:

This bit chooses the parity type for the receive side system data.

= 0: Even parity is employed, which means a logic one should be inserted in the first bit of TS0 of each Basic frame when the number of 'One's in the previous Basic frame is odd.

= 1: Odd parity is employed, which means a logic one should be inserted in the first bit of TS0 of each Basic frame when the number of 'One's in the previous Basic frame is even.

RPTYE:

This bit enables the parity for the receive side system data. The bit is invalid in Receive Clock Master Fractional E1 (with F-bit) mode.

= 0: Disable the parity on the RSDn/MRSD pin.

= 1: Enable the parity on the RSDn/MRSD pin.

FIXF:

This bit controls whether the parity bit position is fixed at the level defined by the FIXPOL. It is invalid in Receive Clock Master Fractional E1 (with F-bit) mode and valid when RPTYE = 0.

= 0: No action.

= 1: The setting in the FIXPOL is valid. The first bit of TS0 of each Basic frame output on the RSDn/MRSD pin is fixed with the value of FIXPOL.

FIXPOL:

This bit is invalid in Receive Clock Master Fractional E1 (with F-bit) mode and valid when the RPTYE = 0 and the FIXF = 1.

= 0: Force the first bit of TS0 of each Basic frame output on the RSDn/MRSD pin to be logic 0.

= 1: Force the first bit of TS0 of each Basic frame output on the RSDn/MRSD pin to be logic 1.

PTY_EXTD:

When the parity is calculated over the previous Basic frame, the first bit of TS0 on the RSDn pin can be included or not. The decision is made by this bit.

= 0: The first bit of TS0 on the RSDn/MRSD pin is not calculated.

= 1: The first bit of TS0 on the RSDn/MRSD pin is calculated.

TRI[1:0]:

TRI[1:0]	Output Status on the RSDn/MRSD and RSSIGn/MRSSIG pins
0 0	in high impedance
1 0	Reserved
0 1	normal output
1 1	Reserved

In the Receive Multiplexed Mode, these bits of the framers that are output to the same multiplexed bus must be set to the same value.

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E1 Receive Backplane Time Slot Offset (013H, 093H, 113H, 193H, 213H, 293H, 313H, 393H)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	Reserved	TSOFF[6]	TSOFF[5]	TSOFF[4]	TSOFF[3]	TSOFF[2]	TSOFF[1]	TSOFF[0]
Type		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0

These bits determine the time slot offset between the signal on the RSCFS pin and the start of the Basic Frame output on the RSDn & RSSIGn pins. If RSCFS does not exist, the time slot offset is between RSFSn and the start of the Basic Frame output on RSDn & RSSIGn. In Receive Multiplexed mode, each framer contributes every fourth time slot on MRSD[1:2] and MRSSIG[1:2].

They define a binary number. The offset can be set from 0 to 127 time slots.

E1 Receive Backplane Bit Offset (014H, 094H, 114H, 194H, 214H, 294H, 314H, 394H)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	Reserved		RSD_RSCFS_EDGE	Reserved	BOFF_EN	BOFF[2]	BOFF[1]	BOFF[0]
Type			R/W		R/W	R/W	R/W	R/W
Default			0		0	0	0	0

RSD_RSCFS_EDGE:

Valid when the CMS (b2, E1-010H) is logic 1 and the DE (b4, E1-010H) is not equal to the FE (b3, E1-010H).

= 0: The second active edge of RSCCK is used to update the signal on the RSDn, RSSIGn and RSFSn pins, or the first active edge of MRSCCK is used to update the signal on the MRSD, MRSSIG and MRSFS pins.

= 1: The first active edge of RSCCK is used to update the signal on the RSDn, RSSIGn and RSFSn pins, or the second active edge of MRSCCK is used to update the signal on the MRSD, MRSSIG and MRSFS pins.

(The signal on the RSCFS/MRSCFS pin is always sampled on the first active edge.)

In Receive Multiplexed mode, the RSD_RSCFS_EDGE in all eight framers should be set to the same value.

When the CMS (b2, E1-010H) is logic 1 and the DE (b4, E1-010H) is equal to FE (b3, E1-010H), the signals on the RSDn/MRSD, RSSIGn/MRSSIG and RSFSn/MRSFS pins are updated on the first active edge of RSCCK/MRSCCK.

BOFF_EN:

Valid when the CMS (b2, E1-010H) is logic 0.

= 0: Disable the bit offset.

= 1: Enable the bit offset.

BOFF[2:0]:

Valid when the CMS (b2, E1-010H) is logic 0 and the BOFF_EN is logic 1.

These bits define a binary number. The content in the BOFF[2:0] determines the bit offset between the signal on the RSCFS pin and the start of the Basic Frame output on the RSDn & RSSIGn pins. If RSCFS does not exist, the time slot offset is between RSFSn and the start of the Basic Frame output on RSDn & RSSIGn. It is also available in Receive Multiplexed mode.

Programming of the Bit Offsets is consistent with the convention established by the Concentration Highway Interface (CHI) specification. Refer to the Functional Description for details.

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E1 Transmit Backplane Configuration (018H, 098H, 118H, 198H, 218H, 298H, 318H, 398H)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	Reserved		TSCKSLV	DE	FE	CMS	RATE[1]	RATE[0]
Type			R/W	R/W	R/W	R/W	R/W	R/W
Default			1	1	1	0	0	0

TSCKSLV:

= 0: Transmit Clock Master mode is enabled.

= 1: Transmit Clock Slave mode or Transmit Multiplexed mode is enabled.

DE:

= 0: The data on the TSDn/MTSD and TSSIGn/MTSSIG pins is sampled on the falling edge of TSCCKB/MTSCCKB or LTCKn.

= 1: The data on the TSDn/MTSD and TSSIGn/MTSSIG pins is sampled on the rising edge of TSCCKB/MTSCCKB or LTCKn.

In Transmit Multiplexed mode, the DE of the eight framers should be set to the same value.

FE:

Valid in Transmit Clock Slave mode and Transmit Multiplexed mode.

= 0: The data on the TSCFS/MTSCFS pin is sampled on the falling edge of TSCCKB/MTSCCKB.

= 1: the data on the TSCFS/MTSCFS pin is sampled on the rising edge of TSCCKB/MTSCCKB.

In Transmit Multiplexed mode, the FE of the eight framers should be set to the same value.

CMS:

= 0: The clock rate of TSCCKB/MTSCCKB is the same as that of the backplane.

= 1: The clock rate of TSCCKB/MTSCCKB is double that of the backplane.

The CMS of the eight framers should be set to the same value.

RATE[1:0]:

These bits determine the bit rate of the transmit data stream on the backplane. Note that if any of the eight framers selects the 8.192 Mbit/s backplane bit rate, the multiplexed bus will be enabled for the chip. When the RATE[1:0] select the 8.192 Mbit/s, the TSCKSLV (b5, E1-018H) must be set to '1'.

RATE[1:0]	Backplane Rate
0 0	Reserved
0 1	2.048M bit/s
1 0	Reserved
1 1	8.192M bit/s (valid to eight frames)

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E1 Transmit Backplane Frame Pulse Configuration (019H, 099H, 119H, 199H, 219H, 299H, 319H, 399H)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	Reserved				FPINV	Reserved	FPTYP	Reserved
Type					R/W		R/W	
Default					0		0	

FPINV:

= 0: The positive pulse on the TSCFS pin is valid.

= 1: The negative pulse on the TSCFS pin is valid.

The FPINV of the eight framers should be the same value.

FPTYP:

= 0: Indicate that the signal on the TSCFS pin pulses during the first bit of each Basic Frame.

= 1: Indicate that the signal on the TSCFS pin asserts on the first bit of each Signaling Multi-Frame and asserts oppositely following the first bit of each CRC Multi-Frame.

The FPTYP of the eight framers should be the same value.

E1 Transmit Backplane Parity Configuration and Status (01AH, 09AH, 11AH, 19AH, 21AH, 29AH, 31AH, 39AH)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	TPTYP	TPTYE	TDI	Reserved	PTY_EXTD	Reserved		
Type	R/W	R/W	R		R/W			
Default	0	0	X		0			

TPTYP:

= 0: Even parity is employed in the first bit of TS0 of each Basic Frame input from the TSDn/MTSD pin, which means a logic one is expected in the position when the number of ‘One’s in the previous Basic Frame is odd.

= 1: Odd parity is employed in the first bit of TS0 of each Basic Frame input from the TSDn/MTSD pin, which means a logic one is expected in the position when the number of ‘One’s in the previous Basic Frame is even.

TPTYE:

This bit decides whether to generate an interrupt when a parity error is detected on the TSDn/MTSD pin.

= 0: No interrupt is generated when a parity error is detected on the TSDn/MTSD pin.

= 1: An interrupt on the $\overline{INT}$ pin is generated when a parity error is detected on the TSDn/MTSD pin.

TDI:

This bit indicates the parity error detected on the TSDn/MTSD pin.

= 0: No parity error is detected on the TSDn/MTSD pin.

= 1: A parity error is detected on the TSDn/MTSD pin.

This bit is cleared to ‘0’ when it is read.

PTY_EXTD:

= 0: The parity checking is calculated over the previous Basic frame, excluding the first bit of TS0 on the TSDn/MTSD pin.

= 1: The parity checking is calculated over the previous Basic frame, including the first bit of TS0 on the TSDn/MTSD pin.

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E1 Transmit Backplane Time Slot Offset (01BH, 09BH, 11BH, 19BH, 21BH, 29BH, 31BH, 39BH)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	Reserved	TSOFF[6]	TSOFF[5]	TSOFF[4]	TSOFF[3]	TSOFF[2]	TSOFF[1]	TSOFF[0]
Type		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0

In Transmit Clock Slave mode, the content in the TSOFF[6:0] determines the time slot offset between TSCFS and the start of the Basic Frame transmitted on TSDn & TSSIGn. In Transmit Multiplexed mode, the content in the TSOFF[6:0] determines the time slot offset between MTSCFS and the start of the Basic Frame transmitted on MTSD & MTSSIG for the corresponding framer.

In Transmit Clock Master mode, the time slot offset is disabled, that is, the TSOFF[6:0] must be logic 0.

The TSOFF[6:0] define a binary number. The offset can be set from 0 to 127 time slots.

E1 Transmit Backplane Bit Offset (01CH, 09CH, 11CH, 19CH, 21CH, 29CH, 31CH, 39CH)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	Reserved			COFF	CHI	BOFF[2]	BOFF[1]	BOFF[0]
Type				R/W	R/W	R/W	R/W	R/W
Default				0	0	0	0	0

COFF:

Valid when the CMS (b2, E1-018H) is logic 1.

= 0: The first active edge of TSCCKB/MTSCCKB is used to sample the data on TSDn/MTSD, TSSIGn/MTSSIG and to update the data on TSFSn.

= 1: The second active edge of TSCCKB/MTSCCKB is used to sample the data on TSDn/MTSD, TSSIGn/MTSSIG and to update the data on TSFSn.

(The signal on the TSCFS/MTSCFS pin is always sampled on the first active edge.)

CHI:

This bit controls if the value in the BOFF[2:0] is the actual value or meets the Concentration Highway Interface (CHI) specification.

= 0: Disable the CHI specification.

= 1: Enable the CHI specification.

BOFF[2:0]:

In Transmit Clock Master mode, the content in the BOFF[2:0] determines the bit offset between the signal on TSFSn and the start of the Basic Frame transmitted on TSDn.

In Transmit Clock Slave mode, the content in the BOFF[2:0] determines the bit offset between TSCFS and the start of the Basic Frame transmitted on TSDn & TSSIGn.

In Transmit Multiplexed mode, the content in the BOFF[2:0] determines the bit offset between MTSCFS and the start of the Basic Frame transmitted on MTSD & MTSSIG.

These bits define a binary number. When the CHI = 0, the setting in the BOFF[2:0] is their actual value (‘0’ stands for 0 bit offset, ‘1’ stands for 1 bit offset, and so on). When the CHI = 1, programming of the BOFF[2:0] is consistent with the convention established by the Concentration Highway Interface (CHI) specification. Refer to the Functional Description for details.

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E1 RJAT Interrupt Status (020H, 0A0H, 120H, 1A0H, 220H, 2A0H, 320H, 3A0H)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	Reserved						OVRI	UNDI
Type							R	R
Default							X	X

OVRI:

If data is still attempted to write into the FIFO when the FIFO is already full, the overwritten event will occur.

= 0: The RJAT FIFO is not overwritten.

= 1: The RJAT FIFO is overwritten.

This bit is cleared to '0' when it is read.

UNDI:

If data is still attempted to read from the FIFO when the FIFO is already empty, the under-run event will occur.

= 0: The RJAT FIFO is not under-run.

= 1: The RJAT FIFO is under-run.

This bit is cleared to '0' when it is read.

E1 RJAT Reference Clock Divisor (N1) Control (021H, 0A1H, 121H, 1A1H, 221H, 2A1H, 321H, 3A1H)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	N1[7]	N1[6]	N1[5]	N1[4]	N1[3]	N1[2]	N1[1]	N1[0]
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	1	0	1	1	1	1

These bits define a binary number. The (N1[7:0] + 1) is the divisor of the input reference clock, which is the ratio between the frequency of the input reference clock and the frequency applied to the phase discriminator input.

Writing to this register will reset the DPLL in the RJAT.

E1 RJAT Output Clock Divisor (N2) Control (022H, 0A2H, 122H, 1A2H, 222H, 2A2H, 322H, 3A2H)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	N2[7]	N2[6]	N2[5]	N2[4]	N2[3]	N2[2]	N2[1]	N2[0]
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	1	0	1	1	1	1

These bits define a binary number. The (N2[7:0] + 1) is the divisor of the output smoothed clock, which is the ratio between the frequency of the output smoothed clock and the frequency applied to the phase discriminator input.

Writing to this register will reset the DPLL in the RJAT.

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E1 RJAT Configuration (023H, 0A3H, 123H, 1A3H, 223H, 2A3H, 323H, 3A3H)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	Reserved			CENT	UNDE	OVRE	Reserved	LIMIT
Type				R/W	R/W	R/W		R/W
Default				0	0	0		1

CENT:

The CENT allows the RJAT FIFO to self-center its read pointer, maintaining the pointer at least 4 UI away from the FIFO being empty or full.

= 0: Disable the self-center. Data is pass through uncorrupted.

= 1: Enable the FIFO to self-center its read pointer when the FIFO is 4 UI away from being empty or full.

A positive transition on this bit will execute a self-center action immediately.

UNDE:

This bit decides whether to generate an interrupt when the RJAT FIFO is under-run.

= 0: No interrupt is generated when the RJAT FIFO is under-run.

= 1: An interrupt on the $\overline{INT}$ pin is generated when the RJAT FIFO is under-run.

OVRE:

This bit decides whether to generate an interrupt when the RJAT FIFO is overwritten.

= 0: No interrupt is generated when the RJAT FIFO is overwritten.

= 1: An interrupt on the INT pin is generated when the RJAT FIFO is overwritten.

LIMIT:

= 0: Disable the limitation of the jitter attenuation.

= 1: Enable the DPLL to limit the jitter attenuation by enabling the FIFO to increase or decrease the frequency of the output smoothed clock when the read pointer is 1 UI away from the FIFO being empty or full. This limitation of jitter attenuation ensures that no data is lost during high phase shift conditions.

E1 TJAT Interrupt Status (024H, 0A4H, 124H, 1A4H, 224H, 2A4H, 324H, 3A4H)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	Reserved						OVRI	UNDI
Type							R	R
Default							X	X

OVRI:

If data is still attempted to write into the FIFO when the FIFO is already full, the overwritten event will occur.

= 0: The TJAT FIFO is not overwritten.

= 1: The TJAT FIFO is overwritten.

This bit is cleared to ‘0’ when it is read.

UNDI:

If data is still attempted to read from the FIFO when the FIFO is already empty, the under-run event will occur.

= 0: The TJAT FIFO is not under-run.

= 1: The TJAT FIFO is under-run.

This bit is cleared to ‘0’ when it is read.

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E1 TJAT Reference Clock Divisor (N1) Control (025H, 0A5H, 125H, 1A5H, 225H, 2A5H, 325H, 3A5H)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	N1[7]	N1[6]	N1[5]	N1[4]	N1[3]	N1[2]	N1[1]	N1[0]
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	1	0	1	1	1	1

These bits define a binary number. The (N1[7:0] + 1) is the divisor of the input reference clock, which is the ratio between the frequency of the input reference clock and the frequency applied to the phase discriminator input.

Writing to this register will reset the DPLL in the TJAT.

E1 TJAT Output Clock Divisor (N2) Control (026H, 0A6H, 126H, 1A6H, 226H, 2A6H, 326H, 3A6H)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	N2[7]	N2[6]	N2[5]	N2[4]	N2[3]	N2[2]	N2[1]	N2[0]
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	1	0	1	1	1	1

These bits define a binary number. The (N2[7:0] + 1) is the divisor of the output smoothed clock, which is the ratio between the frequency of the output smoothed clock and the frequency applied to the phase discriminator input.

Writing to this register will reset the DPLL in the TJAT.

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E1 TJAT Configuration (027H, 0A7H, 127H, 1A7H, 227H, 2A7H, 327H, 3A7H)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	Reserved			CENT	UNDE	OVRE	Reserved	LIMIT
Type				R/W	R/W	R/W		R/W
Default				0	0	0		1

CENT:

The CENT allows the TJAT FIFO to self-center its read pointer, maintaining the pointer at least 4 UI away from the FIFO being empty or full.

= 0: Disable the self-center. Data is pass through uncorrupted.

= 1: Enable the FIFO to self-center its read pointer when the FIFO is 4 UI away from being empty or full.

A positive transition on this bit will execute a self-center action immediately.

UNDE:

This bit decides whether to generate an interrupt when the TJAT FIFO is under-run.

= 0: No interrupt is generated when the TJAT FIFO is under-run.

= 1: An interrupt on the $\overline{INT}$ pin is generated when the TJAT FIFO is under-run.

OVRE:

This bit decides whether to generate an interrupt when the TJAT FIFO is overwritten.

= 0: No interrupt is generated when the TJAT FIFO is overwritten.

= 1: An interrupt on the INT pin is generated when the TJAT FIFO is overwritten.

LIMIT:

= 0: Disable the limitation of the jitter attenuation.

= 1: Enable the DPLL to limit the jitter attenuation by enabling the FIFO to increase or decrease the frequency of the output smoothed clock when the read pointer is 1 UI away from the FIFO being empty or full. This limitation of jitter attenuation ensures that no data is lost during high phase shift conditions.

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E1 RHDLC Receive Data Link 1 Control (TXCISEL = 0) (028H, 0A8H, 128H, 1A8H, 228H, 2A8H, 328H, 3A8H)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	DL1_EVEN	DL1_ODD	TS16_EN	DL1_TS[4]	DL1_TS[3]	DL1_TS[2]	DL1_TS[1]	DL1_TS[0]
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	1	0	0	0	0	0

When the TXCISEL (b3, E1-00AH) is '0', this register is used for the Receive HDLC #1.

DL1_EVEN:
= 0: The data is not extracted from the even frames.
= 1: The data is extracted from the even frames.
The even frames are FAS frames.

DL1_ODD:
= 0: The data is not extracted from the odd frames.
= 1: The data is extracted from the odd frames.
The odd frames are NFAS frames.

TS16_EN:
This bit is valid when the DL1_EVEN and DL1_ODD are both '0'.
= 0: The data is not extracted from TS16.
= 1: The data is extracted from TS16.

DL1_TS[4:0]:
These bits represent the binary value of the time slot to extract the data from. They are invalid when the DL1_EVEN and the DL1_ODD are both '0'.

E1 RHDLC Data Link 1 Bit Select (TXCISEL = 0) (029H, 0A9H, 129H, 1A9H, 229H, 2A9H, 329H, 3A9H)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	DL1_BIT[7]	DL1_BIT[6]	DL1_BIT[5]	DL1_BIT[4]	DL1_BIT[3]	DL1_BIT[2]	DL1_BIT[1]	DL1_BIT[0]
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

When the TXCISEL (b3, E1-00AH) is '0', this register is used for the Receive HDLC #1.

DL1_BITn:
= 0: The data is not extracted from the corresponding bit.
= 1: The data is extracted from the corresponding bit of the assigned time slot.
These bits are invalid when the DL1_EVEN and the DL1_ODD are both '0'.
The DL1_BIT[7] corresponds to the first bit (MSB) of the selected time slot.

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E1 RHDLC Receive Data Link 2 Control (TXCISEL = 0) (02AH, 0AAH, 12AH, 1AAH, 22AH, 2AAH, 32AH, 3AAH)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	DL2_EVEN	DL2_ODD	Reserved	DL2_TS[4]	DL2_TS[3]	DL2_TS[2]	DL2_TS[1]	DL2_TS[0]
Type	R/W	R/W		R/W	R/W	R/W	R/W	R/W
Default	0	0		0	0	0	0	0

When the TXCISEL (b3, E1-00AH) is '0', this register is used for the Receive HDLC #2.

DL2_EVEN:

= 0: The data is not extracted from the even frames.

= 1: The data is extracted from the even frames.

The even frames are FAS frames.

DL2_ODD:

= 0: The data is not extracted from the odd frames.

= 1: The data is extracted from the odd frames.

The odd frames are NFAS frames.

DL2_TS[4:0]:

These bits represent the binary value of the time slot to extract the data from. They are invalid when the DL2_EVEN and the DL2_ODD are both '0'.

E1 RHDLC Data Link 2 Bit Select (TXCISEL = 0) (02BH, 0ABH, 12BH, 1ABH, 22BH, 2ABH, 32BH, 3ABH)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	DL2_BIT[7]	DL2_BIT[6]	DL2_BIT[5]	DL2_BIT[4]	DL2_BIT[3]	DL2_BIT[2]	DL2_BIT[1]	DL2_BIT[0]
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

When the TXCISEL (b3, E1-00AH) is '0', this register is used for the Receive HDLC #2.

DL2_BITn:

= 0: The data is not extracted from the corresponding bit.

= 1: The data is extracted from the corresponding bit of the assigned time slot.

These bits are invalid when the DL2_EVEN and the DL2_ODD are both '0'.

The DL2_BIT[7] corresponds to the first bit (MSB) of the selected time slot.

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E1 RHDLC Receive Data Link 3 Control (TXCISEL = 0) (02CH, 0ACH, 12CH, 1ACH, 22CH, 2ACH, 32CH, 3ACH)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	DL3_EVEN	DL3_ODD	Reserved	DL3_TS[4]	DL3_TS[3]	DL3_TS[2]	DL3_TS[1]	DL3_TS[0]
Type	R/W	R/W		R/W	R/W	R/W	R/W	R/W
Default	0	0		0	0	0	0	0

When the TXCISEL (b3, E1-00AH) is '0', this register is used for the Receive HDLC #3.

DL3_EVEN:

= 0: The data is not extracted from the even frames.

= 1: The data is extracted from the even frames.

The even frames are FAS frames.

DL3_ODD:

= 0: The data is not extracted from the odd frames.

= 1: The data is extracted from the odd frames.

The odd frames are NFAS frames.

DL3_TS[4:0]:

These bits represent the binary value of the time slot to extract the data from. They are invalid when the DL3_EVEN and the DL3_ODD are both '0'.

E1 RHDLC Data Link 3 Bit Select (TXCISEL = 0) (02DH, 0ADH, 12DH, 1ADH, 22DH, 2ADH, 32DH, 3ADH)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	DL3_BIT[7]	DL3_BIT[6]	DL3_BIT[5]	DL3_BIT[4]	DL3_BIT[3]	DL3_BIT[2]	DL3_BIT[1]	DL3_BIT[0]
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

When the TXCISEL (b3, E1-00AH) is '0', this register is used for the Receive HDLC #3.

DL3_BITn:

= 0: The data is not extracted from the corresponding bit.

= 1: The data is extracted from the corresponding bit of the assigned time slot.

These bits are invalid when the DL3_EVEN and the DL3_ODD are both '0'.

The DL3_BIT[7] corresponds to the first bit (MSB) of the selected time slot.

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E1 THDLC Transmit Data Link 1 Control (TXCISEL = 1) (028H, 0A8H, 128H, 1A8H, 228H, 2A8H, 328H, 3A8H)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	DL1_EVEN	DL1_ODD	TS16_EN	DL1_TS[4]	DL1_TS[3]	DL1_TS[2]	DL1_TS[1]	DL1_TS[0]
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	1	0	0	0	0	0

When the TXCISEL (b3, E1-00AH) is '1', this register is used for the Transmit HDLC #1.

DL1_EVEN:
= 0: The data is not inserted to the even frames.
= 1: The data is inserted to the even frames.
The even frames are FAS frames.

DL1_ODD:
= 0: The data is not inserted to the odd frames.
= 1: The data is inserted to the odd frames.
The odd frames are NFAS frames.

TS16_EN:
This bit is valid when the DL1_EVEN and DL1_ODD are both '0' and the CCS is enabled (the SIGEN [b6, E1-040H] and the DLEN [b5, E1-040H] are '1').
= 0: The data is not inserted to TS16.
= 1: The data is inserted to TS16.

DL1_TS[4:0]:
The data is inserted into the time slot defined by the binary number in these bits. They are invalid when the DL1_EVEN and the DL1_ODD are both '0'.

E1 THDLC Data Link 1 Bit Select (TXCISEL = 1) (029H, 0A9H, 129H, 1A9H, 229H, 2A9H, 329H, 3A9H)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	DL1_BIT[7]	DL1_BIT[6]	DL1_BIT[5]	DL1_BIT[4]	DL1_BIT[3]	DL1_BIT[2]	DL1_BIT[1]	DL1_BIT[0]
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

When the TXCISEL (b3, E1-00AH) is '1', this register is used for the Transmit HDLC #1.

DL1_BITn:
= 0: The data is not inserted to the corresponding bit.
= 1: The data is inserted to the corresponding bit of the assigned time slot.
These bits are invalid when the DL1_EVEN and the DL1_ODD are both logic 0.
The DL1_BIT[7] corresponds to the first bit (MSB) of the selected time slot.

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E1 THDLC Transmit Data Link 2 Control (TXCISEL = 1) (02AH, 0AAH, 12AH, 1AAH, 22AH, 2AAH, 32AH, 3AAH)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	DL2_EVEN	DL2_ODD	Reserved	DL2_TS[4]	DL2_TS[3]	DL2_TS[2]	DL2_TS[1]	DL2_TS[0]
Type	R/W	R/W		R/W	R/W	R/W	R/W	R/W
Default	0	0		0	0	0	0	0

When the TXCISEL (b3, E1-00AH) is '1', this register is used for the Transmit HDLC #2.

DL2_EVEN:

= 0: The data is not inserted to the even frames.

= 1: The data is inserted to the even frames.

The even frames are FAS frames.

DL2_ODD:

= 0: The data is not inserted to the odd frames.

= 1: The data is inserted to the odd frames.

The odd frames are NFAS frames.

DL2_TS[4:0]:

The data is inserted into the time slot defined by the binary number in these bits. They are invalid when the DL2_EVEN and the DL2_ODD are both logic 0.

E1 THDLC Data Link 2 Bit Select (TXCISEL = 1) (02BH, 0ABH, 12BH, 1ABH, 22BH, 2ABH, 32BH, 3ABH)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	DL2_BIT[7]	DL2_BIT[6]	DL2_BIT[5]	DL2_BIT[4]	DL2_BIT[3]	DL2_BIT[2]	DL2_BIT[1]	DL2_BIT[0]
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

When the TXCISEL (b3, E1-00AH) is '1', this register is used for the Transmit HDLC #2.

DL2_BITn:

= 0: The data is not inserted to the corresponding bit.

= 1: The data is inserted to the corresponding bit of the assigned time slot.

These bits are invalid when the DL2_EVEN and the DL2_ODD are both logic 0.

The DL2_BIT[7] corresponds to the first bit (MSB) of the selected time slot.

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E1 THDLC Transmit Data Link 3 Control (TXCISEL = 1) (02CH, 0ACH, 12CH, 1ACH, 22CH, 2ACH, 32CH, 3ACH)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	DL3_EVEN	DL3_ODD	Reserved	DL3_TS[4]	DL3_TS[3]	DL3_TS[2]	DL3_TS[1]	DL3_TS[0]
Type	R/W	R/W		R/W	R/W	R/W	R/W	R/W
Default	0	0		0	0	0	0	0

When the TXCISEL (b3, E1-00AH) is '1', this register is used for the Transmit HDLC #3.

DL3_EVEN:

= 0: The data is not inserted to the even frames.

= 1: The data is inserted to the even frames.

The even frames are FAS frames.

DL3_ODD:

= 0: The data is not inserted to the odd frames.

= 1: The data is inserted to the odd frames.

The odd frames are NFAS frames.

DL3_TS[4:0]:

The data is inserted into the time slot defined by the binary number in these bits. They are invalid when the DL3_EVEN and the DL3_ODD are both logic 0.

E1 THDLC Data Link 3 Bit Select (TXCISEL = 1) (02DH, 0ADH, 12DH, 1ADH, 22DH, 2ADH, 32DH, 3ADH)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	DL3_BIT[7]	DL3_BIT[6]	DL3_BIT[5]	DL3_BIT[4]	DL3_BIT[3]	DL3_BIT[2]	DL3_BIT[1]	DL3_BIT[0]
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

When the TXCISEL (b3, E1-00AH) is '1', this register is used for the Transmit HDLC #3.

DL3_BITn:

= 0: The data is not inserted to the corresponding bit.

= 1: The data is inserted to the corresponding bit of the assigned time slot.

These bits are invalid when the DL3_EVEN and the DL3_ODD are both logic 0.

The DL3_BIT[7] corresponds to the first bit (MSB) of the selected time slot.

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E1 FRMP Frame Alignment Options (030H, 0B0H, 130H, 1B0H, 230H, 2B0H, 330H, 3B0H)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	CRCEN	CASDIS	C2NCIWCK	Reserved		REFR	REFCRCE	REFRDIS
Type	R/W	R/W	R/W			R/W	R/W	R/W
Default	1	0	0			0	1	0

CRCEN:

= 0: Disable searching for CRC Multi-Frame.

= 1: Enable searching for CRC Multi-Frame alignment signal and monitor the errors in the CRC Multi-Frame.

CASDIS:

= 0: Enable searching for Channel Associated Signaling (CAS) Multi-Frame alignment signal and monitor the errors in the Signaling Multi-Frame.

= 1: Disable searching for Channel Associated Signaling Multi-Frame.

C2NCIWCK:

= 0: Stop searching for CRC Multi-Frame alignment signal in CRC to non-CRC inter-working mode.

= 1: Continue searching for CRC Multi-Frame alignment signal even if CRC to non-CRC inter-working has been declared.

REFR:

A transition from logic 0 to logic 1 forces to re-search for a new Basic Frame.

REFCRCE:

This bit decides if the Frame Processor re-searches for the Basic Frame when there are excessive CRC errors. The excessive CRC errors are defined as more than 914 CRC errors in one second. One CRC error is counted when the local calculated CRC-4 is not equal to the received CRC-4.

= 0: Disable re-searching for Basic Frame when there are excessive CRC errors.

= 1: Enable re-searching for Basic Frame when there are excessive CRC errors.

REFRDIS:

0 = Enable re-searching for Basic Frame when it is out of Basic frame synchronization or there are excessive CRC errors.

1 = 'Locked in frame' once initial frame alignment has been found. Disable re-searching for Basic Frame under any error conditions once the initial Basic Frame synchronization is acquired.

While the FRMP remains locked in frame due to REFRDIS = 1, a received AIS will not be detected since the Frame Processor must be out-of-frame to detect AIS.

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E1 FRMP Maintenance Mode Options (031H, 0B1H, 131H, 1B1H, 231H, 2B1H, 331H, 3B1H)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	Reserved	BIT2C	SMFASC	TS16C	RAIC	Reserved	AISC	EXCRCERR
Type		R/W	R/W	R/W	R/W		R/W	R
Default		1	0	0	0		X	X

BIT2C:

= 0: Out of Basic frame synchronization is declared on 3 consecutive FAS errors.

= 1: Enable the additional criteria to declare out of Basic frame synchronization. Thus, out of Basic frame synchronization is declared when 3 consecutive logic '0's are received in Bit 2 of TS0 of NFAS or 3 consecutive FAS are in errors.

SMFASC:

= 0: Enable the declaration of out of Signaling Multi-Frame synchronization when 2 consecutive Signaling Multi-Frame alignment patterns have been received in error.

= 1: Enable the declaration of out of Signaling Multi-Frame synchronization when 2 consecutive Signaling Multi-Frame alignment patterns have been received in error or when all the content in TS16 of Frame 0 are logic '0's for one or two consecutive multi-frames which is defined in the TS16C (b4, E1-031H).

TS16C:

Valid when the SMFASC (b5, E1-031H) is logic 1.

= 0: Enable the declaration of out of Signaling Multi-Frame synchronization when all the content in TS16 are logic '0's for one multi-frame.

= 1: Enable the declaration of out of Signaling Multi-Frame synchronization when all the content in TS16 are logic '0's for two consecutive multi-frames.

RAIC:

= 0: Set the RAIV (b7, E1-037H) to be logic 1 on the reception of any 'A' bit being logic one, and set the RAIV (b7, E1-037H) to be logic 0 on the reception of any 'A' bit being logic zero.

= 1: Set the RAIV (b7, E1-037H) to be logic 1 on the reception of the 'A' bit being logic one for 4 or more consecutive occasions, and set the RAIV (b7, E1-037H) to be logic 0 on the reception of any 'A' bit being logic zero.

AISC:

= 0: Set the AISD (b5, E1-037H) to logic 1 when it is out of Basic frame synchronization and less than 3 zeros are detected in a 512-bit stream, and set the AISD (b5, E1-037H) to logic 0 when 3 or more zeros are detected in a 512-bit stream.

= 1: Set the AISD (b5, E1-037H) to logic 1 when it is out of Basic frame synchronization and less than 3 zeros are detected in each of 2 consecutive 512-bit stream, and set the AISD (b5, E1-037H) to logic 0 when 3 or more zeros are detected in each of 2 consecutive 512-bit stream.

EXCRCERR:

The excessive CRC errors are defined as more than 914 CRC errors in one second. One CRC error is counted when the local calculated CRC-4 is not equal to the received CRC-4.

= 0: Normal operation.

= 1: Indicate that there are excessive CRC errors in the received data stream.

This bit is cleared to '0' after it is read.

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E1 FRMP Framing Status Interrupt Enable (032H, 0B2H, 132H, 1B2H, 232H, 2B2H, 332H, 3B2H)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	C2NCIWE	OOFE	OOSMFE	OOCMFE	COFAE	FERE	SMFERE	CMFERE
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	1	0

C2NCIWE:
= 0: Disable the interrupt on the $\overline{INT}$ pin when the C2NCIWI (b7, E1-034H) is logic one.
= 1: Enable the interrupt on the $\overline{INT}$ pin when the C2NCIWI is logic one.

OOFE:
= 0: Disable the interrupt on the $\overline{INT}$ pin when the OOFI (b6, E1-034H) is logic one.
= 1: Enable the interrupt on the $\overline{INT}$ pin when the OOFI is logic one.

OOSMFE:
= 0: Disable the interrupt on the $\overline{INT}$ pin when the OOSMFI (b5, E1-034H) is logic one.
= 1: Enable the interrupt on the $\overline{INT}$ pin when the OOSMFI is logic one.

OOCMFE:
= 0: Disable the interrupt on the $\overline{INT}$ pin when the OOCMFI (b4, E1-034H) is logic one.
= 1: Enable the interrupt on the $\overline{INT}$ pin when the OOCMFI is logic one.

COFAE:
= 0: Disable the interrupt on the $\overline{INT}$ pin when the position of the Basic frame alignment signal changes.
= 1: Enable the interrupt on the $\overline{INT}$ pin when the position of the Basic frame alignment signal changes.

FERE:
= 0: Disable the interrupt on the $\overline{INT}$ pin when there is error in the Basic frame alignment pattern.
= 1: Enable the interrupt on the $\overline{INT}$ pin when there is error in the Basic frame alignment pattern.

SMFERE:
= 0: Disable the interrupt on the $\overline{INT}$ pin when there is an error in the Signaling Multi-Frame alignment pattern.
= 1: Enable the interrupt on the $\overline{INT}$ pin when there is an error in the Signaling Multi-Frame alignment pattern.

CMFERE:
= 0: Disable the interrupt on the $\overline{INT}$ pin when there is error in the CRC Multi-Frame alignment pattern.
= 1: Enable the interrupt on the $\overline{INT}$ pin when there is error in the CRC Multi-Frame alignment pattern.

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E1 FRMP Maintenance / Alarm Status Interrupt Enable (033H, 0B3H, 133H, 1B3H, 233H, 2B3H, 333H, 3B3H)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	RAIE	RMAIE	AISDE	Reserved	REDE	AISE	FEBEE	CRCEE
Type	R/W	R/W	R/W		R/W	R/W	R/W	R/W
Default	0	0	0		0	0	0	0

RAIE:

= 0: Disable the interrupt on the $\overline{INT}$ pin when the RAII (b7, E1-035H) is logic one.

= 1: Enable the interrupt on the $\overline{INT}$ pin when the RAII is logic one.

RMAIE:

= 0: Disable the interrupt on the $\overline{INT}$ pin when the RMAII (b6, E1-035H) is logic one.

= 1: Enable the interrupt on the $\overline{INT}$ pin when the RMAII is logic one.

AISDE:

= 0: Disable the interrupt on the $\overline{INT}$ pin when the AISDI (b5, E1-035H) is logic one.

= 1: Enable the interrupt on the $\overline{INT}$ pin when the AISDI is logic one.

REDE:

= 0: Disable the interrupt on the $\overline{INT}$ pin when the REDI (b3, E1-035H) is logic one.

= 1: Enable the interrupt on the $\overline{INT}$ pin when the REDI is logic one.

AISE:

= 0: Disable the interrupt on the $\overline{INT}$ pin when the AISI (b2, E1-035H) is logic one.

= 1: Enable the interrupt on the $\overline{INT}$ pin when the AISI is logic one.

FEBEE:

= 0: Disable the interrupt on the $\overline{INT}$ pin when a logic 0 is received in the E1 (the first bit in TS0 in the 13th Frame of CRC-4 Multi-Frame) or E2 (the first bit in TS0 in the 15th Frame of CRC-4 Multi-Frame) bit.

= 1: Enable the interrupt on the $\overline{INT}$ pin when a logic 0 is received in the E1 or E2 bit.

CRCEE:

= 0: Disable the interrupt on the $\overline{INT}$ pin when there is difference between the calculated CRC-4 remainder and the received CRC-4.

= 1: Enable the interrupt on the $\overline{INT}$ pin when there is difference between the calculated CRC-4 remainder and the received CRC-4.

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E1 FRMP Framing Status Interrupt Indication (034H, 0B4H, 134H, 1B4H, 234H, 2B4H, 334H, 3B4H)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	C2NCIWI	OOFI	OOSMFI	OOCMFI	COFAI	FERI	SMFERI	CMFERI
Type	R	R	R	R	R	R	R	R
Default	X	X	X	X	X	X	X	X

All the bits in this register are clear to '0' after the register is read.

C2NCIWI:
= 0: No status change on the C2NCIWV (b7, E1-036H).
= 1: There is a transition (from '0' to '1' or from '1' to '0') on the C2NCIWV (b7, E1-036H).

OOFI:
= 0: No status change on the OOFV (b6, E1-036H)
= 1: There is a transition (from '0' to '1' or from '1' to '0') on the OOFV (b6, E1-036H).

OOSMFI:
= 0: No status change on the OOSMFV (b5, E1-036H)
= 1: There is a transition (from '0' to '1' or from '1' to '0') on the OOSMFV (b5, E1-036H).

OOCMFI:
= 0: No status change on the OOCMFV (b4, E1-036H)
= 1: There is a transition (from '0' to '1' or from '1' to '0') on the OOCMFV (b4, E1-036H).

COFAI:
= 0: The position of the Basic frame alignment signal does not change.
= 1: The position of the Basic frame alignment signal changes.

FERI:
= 0: There is no error in the Basic frame alignment pattern.
= 1: There is an error in the Basic frame alignment pattern.

SMFERI:
= 0: There is no error in the Signaling Multi-Frame alignment pattern.
= 1: There is an error in the Signaling Multi-Frame alignment pattern.

CMFERI:
= 0: There is no error in the CRC Multi-Frame alignment pattern.
= 1: There is an error in the CRC Multi-Frame alignment pattern.

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E1 FRMP Maintenance / Alarm Status Interrupt Indication (035H, 0B5H, 135H, 1B5H, 235H, 2B5H, 335H, 3B5H)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	RAII	RMAII	AISDI	Reserved	REDI	AISI	FEBEI	CRCEI
Type	R	R	R		R	R	R	R
Default	X	X	X		X	X	X	X

All the bits in this register are clear to '0' after the register is read.

RAII:
= 0: No status change on the RAIV (b7, E1-037H).
= 1: There is a transition (from '0' to '1' or from '1' to '0') on the RAIV (b7, E1-037H).

RMAII:
= 0: No status change on the RMAIV (b6, E1-037H).
= 1: There is a transition from '0' to '1' or from '1' to '0' on the RMAIV (b6, E1-037H).

AISDI:
= 0: No status change on the AISD (b5, E1-037H).
= 1: There is a transition from '0' to '1' or from '1' to '0' on the AISD (b5, E1-037H).

REDI:
= 0: No status change on the RED (b3, E1-037H).
= 1: There is a transition from '0' to '1' or from '1' to '0' on the RED (b3, E1-037H).

AISI:
= 0: No status change on the AIS (b2, E1-037H).
= 1: There is a transition from '0' to '1' or from '1' to '0' on the AIS (b2, E1-037H).

FEBEI:
= 0: No logic 0 is received in the E1 or E2 bit.
= 1: A logic 0 is received in the E1 or E2 bit.

CRCEI:
= 0: No difference between the calculated CRC-4 remainder and the received CRC-4.
= 1: There is difference between the calculated CRC-4 remainder and the received CRC-4 remainder.

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E1 FRMP Framing Status (036H, 0B6H, 136H, 1B6H, 236H, 2B6H, 336H, 3B6H)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	C2NCIWV	OOFV	OOSMFV	OOCMFV	OOOFV	RAICCRCV	CFEBEV	V52LINKV
Type	R	R	R	R	R	R	R	R
Default	X	X	X	X	X	X	X	X

C2NCIWV:

= 0: The Frame Processor does not operate in CRC to non-CRC inter-working mode.

= 1: The Frame Processor operates in CRC to non-CRC inter-working mode.

OOFV:

= 0: The Basic Frame is in synchronization.

= 1: The Basic Frame is out of synchronization.

OOSMFV:

= 0: The Signaling Multi-Frame is in synchronization.

= 1: The Signaling Multi-Frame is out of synchronization.

OOCMFV:

= 0: The CRC Multi-Frame is in synchronization.

= 1: The CRC Multi-Frame is out of synchronization.

OOOFV:

= 0: The offline frame is in synchronization.

= 1: The offline frame is out of synchronization.

RAICCRCV:

= 0: Normal operation.

= 1: The remote alarm (logic 1 in A bit) and the FEBE (logic 0 in bit E1 or E2) have existed for a period of 10 ms.

CFEBEV:

= 0: Normal operation.

= 1: FEBE (logic 0 in bit E1 and E2) has existed for more than or equal to 990 occasions in each second for 5 consecutive seconds.

V52LINKV:

= 0: V5.2 link ID signal is not received.

= 1: V5.2 link ID signal is received, i.e., 2 out of 3 Sa7 bits are logic zeros

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E1 FRMP Maintenance / Alarm Status (037H, 0B7H, 137H, 1B7H, 237H, 2B7H, 337H, 3B7H)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	RAIV	RMAIV	AISD	Reserved	RED	AIS	Reserved	
Type	R	R	R		R	R		
Default	X	X	X		X	X		

RAIV:

This bit indicates the value of the Remote Alarm Indication (A) bit.

= 0: The 'A' bit is logic 0.

= 1: RAI is detected according to the criterion set in the RAIC (b3, E1-031H). When the RAIC is '0', RAI is detected when the 'A' bit is received as logic 1. When the RAIC is '1', RAI is detected when the 'A' bit is received as logic 1 for 4 or more consecutive occasions.

The RAIV is updated every two frames.

RMAIV:

This bit indicates the value of the Remote Signaling Multi-Frame Alarm Indication (Y) bit.

= 0: The 'Y' bit is logic 0.

= 1: Logic 1 has been received in 'Y' bit for 3 consecutive Signaling Multi-Frames.

The RMAIV is updated every 16 frames.

AISD:

This bit indicates the Alarm Indication Signal (AIS) detect value. The detection of AIS is disabled in unframed mode.

= 0: AIS is clear according to the criterion set in the AISC (b1, E1-031H). When the AISC is '0', AIS is clear when 3 or more zeros are detected in a 512-bit stream. When the AISC is '1', AIS is clear when 3 or more zeros are detected in each of 2 consecutive 512-bit stream.

= 1: AIS is detected according to the criterion set in the AISC (b1, E1-031H). When the AISC is '0', AIS is detected when it is out of Basic frame synchronization and less than 3 zeros are detected in a 512-bit stream. When the AISC is '1', AIS is detected when it is out of Basic frame synchronization and less than 3 zeros are detected in each of 2 consecutive 512-bit stream.

The AISD bit is updated once every 512 bit periods.

RED:

= 0: Out of Basic frame synchronization has been absent for 100 ms.

= 1: Out of Basic frame synchronization has persisted for 100 ms.

AIS:

= 0: The condition of AIS has been absent for 100 ms.

= 1: The condition of AIS has persisted for 100 ms.

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E1 FRMP Time Slot 0 International / National Bits (038H, 0B8H, 138H, 1B8H, 238H, 2B8H, 338H, 3B8H)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	Si[1]	Si[0]	A	Sa[4]	Sa[5]	Sa[6]	Sa[7]	Sa[8]
Type	R	R	R	R	R	R	R	R
Default	X	X	X	X	X	X	X	X

The content in this register reflects the International bits, Remote Alarm Indication bit and National bits. The Si[1:0] bits are the International bits. The 'A' bit is the Remote Alarm Indication bit. The Sa[4:8] bits are the National bits. Their position is shown in the following table:

Frame Type	Eight Bits in TS0							
	0	1	2	3	4	5	6	7
FAS	Si[1]	0	0	1	1	0	1	1
NFAS	Si[0]	1	A	Sa[4]	Sa[5]	Sa[6]	Sa[7]	Sa[8]

Note that the contents of this register are not updated while the received data stream is out of Basic Frame.

Si[1]:

Directly reflect the content in the International bit in the latest received FAS frame and is updated on the generation of the IFPI interrupt on FAS frames.

Si[0]:

Directly reflect the content in the International bit in the latest received NFAS frame and is updated on the generation of the IFPI interrupt on NFAS frames.

A:

Directly reflect the content in the Remote Alarm Indication (A) bit in the latest received NFAS frame and is updated on the generation of the IFPI interrupt on NFAS frames.

Sa[4:8]:

Directly reflect the content in the National bit in the latest received NFAS frame and is updated on the generation of the IFPI interrupt on NFAS frames.

E1 FRMP CRC Error Counter-LSB (039H, 0B9H, 139H, 1B9H, 239H, 2B9H, 339H, 3B9H)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	CRCERR[7]	CRCERR[6]	CRCERR[5]	CRCERR[4]	CRCERR[3]	CRCERR[2]	CRCERR[1]	CRCERR[0]
Type	R	R	R	R	R	R	R	R
Default	X	X	X	X	X	X	X	X

The CRCERR[7:0], together with the CRCERR[9:8], represent the number of the CRC errors and update every second. The CRCERR[0] is the LSB.

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E1 FRMP CRC Error Counter-MSB / Time Slot 16 Extra Bits (03AH, 0BAH, 13AH, 1BAH, 23AH, 2BAH, 33AH, 3BAH)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	OVR	NEWDATA	X[0]	Y	X[1]	X[2]	CRCERR[9]	CRCERR[8]
Type	R	R	R	R	R	R	R	R
Default	0	0	X	X	X	X	X	X

OVR:

Overwritten means that the data is still written into the CRCERR[9:0] (b1~0, E1-03AH & b7~0, E1-039H) without the data being read in the latest one second interval.

= 0: The CRCERR[9:0] (b1~0, E1-03AH & b7~0, E1-039H) are not overwritten.

= 1: The CRCERR[9:0] (b1~0, E1-03AH & b7~0, E1-039H) are overwritten.

This bit is clear to '0' after it is read.

NEWDATA:

= 0: The value in the CRCERR[9:0] (b1~0, E1-03AH & b7~0, E1-039H) has not been updated with new value.

= 1: The value in the CRCERR[9:0] (b1~0, E1-03AH & b7~0, E1-039H) has been updated with new value.

This bit is clear to '0' after it is read. This bit can be polled to determine the 1 second timing boundary used by the Frame Processor.

X[0:2], Y:

Directly reflect the content in the Extra bits (X[0:2]) and the Remote Signaling Multi-Frame Alarm bit (Y) in Frame0 of TS16 of the latest received Signaling Multi-Frame. They are updated on the generation of the IFPI interrupt on NFAS frames. Note that these bits are not updated when the received data stream is out of Basic Frame. The position of the X[2:0] and Y bit is shown in the following table:

Frame 0	Eight Bits in TS16							
	0	1	2	3	4	5	6	7
	0	0	0	0	X[0]	Y	X[1]	X[2]

CRCERR[9:8]:

The CRCERR[9:8], together with the CRCERR[7:0], represent the number of the CRC errors and update every second. The CRCERR[9] is the MSB.

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E1 FRMP National Bit Codeword Interrupt Enables (03BH, 0BBH, 13BH, 1BBH, 23BH, 2BBH, 33BH, 3BBH)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	SaSEL[2]	SaSEL[1]	SaSEL[0]	Sa4E	Sa5E	Sa6E	Sa7E	Sa8E
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

SaSEL[2:0]:

The SaSEL[2:0] select the National Bit Codeword (SaX) to appear in the SaX[1:4] (b3~0, E1-03DH) of the National Bit Codeword register.

SaSEL[2:0]	National Bit Codeword
0 0 1	Reserved
0 1 0	
0 1 1	
1 0 0	Sa4
1 0 1	Sa5
1 1 0	Sa6
1 1 1	Sa7
0 0 0	Sa8

Sa4E, Sa5E, Sa6E, Sa7E, Sa8E:

= 0 (in any of the 5 bits): Disable the interrupt on the $\overline{INT}$ pin when the value is changed in its corresponding SaX[1:4] (b3~0, E1-03DH).

= 1 (in any of the 5 bits): Enable the interrupt on the $\overline{INT}$ pin when the value is changed in its corresponding SaX[1:4] (b3~0, E1-03DH) (X is 4 through 8).

The interrupt enable should be logic 0 for the bit receiving a HDLC data link.

E1 FRMP National Bit Codeword Interrupts (03CH, 0BCH, 13CH, 1BCH, 23CH, 2BCH, 33CH, 3BCH)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	Reserved			Sa4I	Sa5I	Sa6I	Sa7I	Sa8I
Type				R	R	R	R	R
Default				X	X	X	X	X

Sa4I, Sa5I, Sa6I, Sa7I, Sa8I:

= 0 (in any of the 5 bits): The value is not changed in its corresponding SaX[1:4] (b3~0, E1-03DH) bits (X is 4 through 8).

= 1 (in any of the 5 bits): The value is changed in its corresponding SaX[1:4] (b3~0, E1-03DH) bits (X is 4 through 8).

This bit is clear to '0' after the register is read.

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E1 FRMP National Bit Codeword (03DH, 0BDH, 13DH, 1BDH, 23DH, 2BDH, 33DH, 3BDH)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	Reserved				SaX[1]	SaX[2]	SaX[3]	SaX[4]
Type					R	R	R	R
Default					X	X	X	X

These bits directly reflect the content in the SaX nibble codeword of the CRC Sub Multi-Frame. 'X' is determined by the SaSEL[2:0] (b7~5, E1-03BH). SaX[1] is the first SaX bit of the Sub Multi-Frame and analogically. The SaX[1:4] are debounced. They are updated only when two consecutive codewords are the same.

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E1 FRMP Frame Pulse/Alarm/V5.2 Link ID Interrupt Enables (03EH, 0BEH, 13EH, 1BEH, 23EH, 2BEH, 33EH, 3BEH)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	OOOFE	RAICCRCE	CFEBEE	V52LINKE	IFPE	ICSMFPE	ICMFPE	ISMFPE
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

OOOFE:

= 0: Disable the interrupt on the $\overline{INT}$ pin when the OOOFI (b7, E1-03FH) is logic one.

= 1: Enable the interrupt on the $\overline{INT}$ pin when the OOOFI (b7, E1-03FH) is logic one.

RAICCRCE:

= 0: Disable the interrupt on the $\overline{INT}$ pin when the Remote Alarm (logic 1 in A bit) and the FEBE (logic 0 in bit E1 or E2) have existed for 10 ms.

= 1: Enable the interrupt on the $\overline{INT}$ pin when the Remote Alarm (logic 1 in A bit) and the FEBE (logic 0 in bit E1 or E2) have existed for 10 ms.

CFEBEE:

= 0: Disable the interrupt on the $\overline{INT}$ pin when the FEBE (logic 0 in bit E1 or E2) has existed for more than 990 occasions in each second for 5 consecutive seconds.

= 1: Enable the interrupt on the $\overline{INT}$ pin when the FEBE (logic 0 in bit E1 or E2) has existed for more than 990 occasions in each second for 5 consecutive seconds.

V52LINKE:

= 0: Disable the interrupt on the $\overline{INT}$ pin when the V52LINKI is logic one.

= 1: Enable the interrupt on the $\overline{INT}$ pin when the V52LINKI (b4, E1-03FH) is logic one.

IFPE:

= 0: Disable the interrupt on the $\overline{INT}$ pin when the first bit of each Basic frame is received.

= 1: Enable the interrupt on the $\overline{INT}$ pin when the first bit of each Basic frame is received.

ICSMFPE:

= 0: Disable the interrupt on the $\overline{INT}$ pin when the first bit of each CRC Sub Multi-Frame is received.

= 1: Enable the interrupt on the $\overline{INT}$ pin when the first bit of each CRC Sub Multi-Frame is received.

ICMFPE:

= 0: Disable the interrupt on the $\overline{INT}$ pin when the first bit of each CRC Multi-Frame is received.

= 1: Enable the interrupt on the $\overline{INT}$ pin when the first bit of each CRC Multi-Frame is received.

ISMFPE:

= 0: Disable the interrupt on the $\overline{INT}$ pin when the first bit of each Signaling Multi-Frame is received.

= 1: Enable the interrupt on the $\overline{INT}$ pin when the first bit of each Signaling Multi-Frame is received.

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E1 FRMP Frame Pulse / Alarm Interrupts (03FH, 0BFH, 13FH, 1BFH, 23FH, 2BFH, 33FH, 3BFH)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	OOOFI	RAICCRCI	CFEBEI	V52LINKI	IFPI	ICSMFPI	ICMFPI	ISMFPI
Type	R	R	R	R	R	R	R	R
Default	X	X	X	X	X	X	X	X

The bits of this register are clear to '0' after the register is read.

OOOFI:

= 0: There is no transition (from '0' to '1' or from '1' to '0') on the OOOFV (b3, E1-036H).

= 1: There is a transition (from '0' to '1' or from '1' to '0') on the OOOFV (b3, E1-036H).

RAICCRCI:

= 0: There is no transition from normal operation to the Remote Alarm (logic 1 in A bit) or the FEBE (logic 0 in bit E1 or E2) has being absent for a period of 10 ms.

= 1: There is a transition from normal operation to the Remote Alarm (logic 1 in A bit) and the FEBE (logic 0 in bit E1 or E2) has existed for a period of 10 ms.

CFEBEI:

= 0: The existence of no transition from normal operation to FEBE (logic 0 in bit E1 or E2) has occurred for more than 990 occasions in each second for 5 consecutive seconds.

= 1: The existence of a transition from normal operation to FEBE (logic 0 in bit E1 or E2) has occurred for more than 990 occasions in each second for 5 consecutive seconds.

V52LINKI:

= 0: There is no transition (from '0' to '1' or from '1' to '0') on the V52LINKV (b0, E1-036H).

= 1: There is a transition (from '0' to '1' or from '1' to '0') on the V52LINKV (b0, E1-036H).

IFPI:

= 0: The received bit is not the first bit of each Basic Frame.

= 1: The first bit of each Basic Frame is received.

ICSMFPI:

= 0: The received bit is not the first bit of each CRC Sub Multi-Frame.

= 1: The first bit of each CRC Sub Multi-Frame is received.

ICMFPI:

= 0: The received bit is not the first bit of each CRC Multi-Frame.

= 1: The first bit of each CRC Multi-Frame is received.

ISMFPI:

= 0: The received bit is not the first bit of each Signaling Multi-Frame.

= 1: The first bit of each Signaling Multi-Frame is received.

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E1 FRMG Configuration (040H, 0C0H, 140H, 1C0H, 240H, 2C0H, 340H, 3C0H)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	FRESH	SIGEN	DLEN	GENCRC	FDIS	FEBEDIS	INDIS	XDIS
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	1	1	0	0	0	0	0

FRESH:

= 0: Normal operation.

= 1: Initiate the FIFO in the Frame Generator block.

After initialization of the backplane interface, the user should write '1' into this bit and then clear it.

SIGEN, DLEN:

These two bits select the signaling sources for TS16. They are valid when the AIS (b0, E1-041H) is logic 0:

SIGEN, DLEN	Signaling Source
0 0	Signaling insertion disable or CCS enable. TS16 data is taken directly from the input TSDn TS16 or from the THDLC if the THDLC selects this inserted position. The XDIS (b0, E1-040H) must also be set to logic 1 to disable the insertion of the extra bits in TS16 of frame 0.
0 1	Reserved
1 0	Reserved
1 1	CAS enable. TS16 data is taken from either TSSIGn stream or from the TPLC Signaling/PCM Control byte as selected on a per-time slot basis via the SIGSRC (b4, E1-TPLC-indirect registers - 61~7FH). However, the TS16 of Frame0 of Signaling Multi-Frame is overwritten by '0000X[0]YX[1]X[2]'.

GENCRC:

= 0: CRC Multi-Frame generation is disabled. Then the International bits are replaced with the value contained in the Si[1:0] (b7~6, E1-042H) if the INDIS (b1, E1-040H) is enabled (logic 0), or, if the INDIS (b1, E1-040H) is not enabled, the International bits are taken directly from TSDn/MTSD.

= 1: CRC Multi-Frame generation is enabled. When CRC Multi-Frame is generated, the International bits on the TSDn pin are replaced with CRC Multi-Frame alignment pattern and calculated CRC-4 bits. The CRC bits calculated during the transmission of the SMFn are transmitted in the following SMF (SMF n+1). If the FEBEDIS (b2, E1-040H) is enabled (logic 0), the FEBE indication is inserted in the E1 and E2 bit positions. This setting is valid when the FDIS (b3, E1-040H) and the INDIS (b1, E1-040H) are logic 0.

FDIS:

= 0: Replace the data on TS0 of FAS on the TSDn/MTSD pin with Basic Frame alignment sequence (FAS).

= 1: Keep the data on the TSDn/MTSD pin to pass through the Frame Generation transparently. The values in the control bits GENCRC (b4, E1-040H), FEBEDIS (b2, E1-040H) and INDIS (b1, E1-040H) are ignored.

FEBEDIS:

Valid when the FDIS (b3, E1-040H) and the INDIS (b1, E1-040H) are logic 0 and the GENCRC (b4, E1-040H) is logic 1.

= 0: The International bits of frame 13 & 15 are for FEBE indication.

= 1: FEBE indication is disabled.

INDIS:

= 0: Enabled to replace the International bit.

= 1: Disable to replace the International bit. The value of the international bit is directly taken from TSDn/MTSD or from the THDLC if the THDLC selects this inserted position.

XDIS:

Valid when the FDIS (b3, E1-040H) is logic 0, and the SIGEN (b6, E1-040H) and the DLEN (b5, E1-040H) are logic 1.

= 0: Replace the extra bits with the setting in the X[2:0].

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= 1: Ignore the setting in the X[2:0] bits. The value in the extra bits is taken from TSDn/MTSD.

E1 FRMG Transmit Alarm / Diagnostic Control (041H, 0C1H, 141H, 1C1H, 241H, 2C1H, 341H, 3C1H)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	MTRK	FPATINV	SPLRINV	SPATINV	REMAIS	MFAIS	TS16AIS	AIS
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

MTRK:

Valid when the FDIS (b3, E1-040H) is logic 0 and the PCCE (b0, E1-060H) is logic 1.

= 0: Ignore the setting in the IDLE Code Byte register.

= 1: Replace the data on TS1~15 & TS17~31 with the IDLE code. And when the SIGEN (b6, E1-040H) is logic 1, replace the data on TS16 with signaling; when the SIGEN (b6, E1-040H) is logic 0, replace the data on TS16 with IDLE code.

FPATINV:

Valid when the FDIS (b3, E1-040H) is logic 0.

= 0: Disable the inversion of the FAS.

= 1: Enable the inversion of the FAS (from '0011011' to '1100100').

SPLRINV:

Valid when the FDIS (b3, E1-040H) is logic 0.

= 0: Disable the inversion of the 2nd bit of NFAS.

= 1: Enable the inversion of the 2nd bit of NFAS (from '1' to '0').

SPATINV:

Valid when the FDIS (b3, E1-040H) is logic 0 and the SIGEN (b6, E1-040H) & the DLEN (b5, E1-040H) are logic 1.

= 0: Disable the inversion of the Signaling Multi-Frame alignment signal.

= 1: Enable the inversion of the Signaling Multi-Frame alignment signal (from '0000' to '1111').

REMAIS:

Valid when the FDIS (b3, E1-040H) is logic 0.

= 0: Normal operation.

= 1: Force the 3rd bit of NFAS to be logic 1.

MFAIS:

Valid when the FDIS (b3, E1-040H) is logic 0.

= 0: Normal operation.

= 1: Force to transmit the 'Y' bit as logic 1.

TS16AIS:

Valid when the FDIS (b3, E1-040H) is logic 0 and Signaling Multi-Frame generator is enabled.

= 0: Normal transmission.

= 1: Force to transmit all 'One's in TS16 unconditionally.

AIS:

= 0: Normal transmission.

= 1: Force to transmit all 'One's on all time slots unconditionally.

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E1 FRMG International Bits Control (042H, 0C2H, 142H, 1C2H, 242H, 2C2H, 342H, 3C2H)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	Si[1]	Si[0]	Reserved					
Type	R/W	R/W						
Default	1	1						

Si[1:0]:

Valid when the FDIS (b3, E1-040H) and the INDIS (b1, E1-040H) are logic 0.

When CRC Multi-Frame generation is disabled (GENCRC is logic 0), the Si[1] and Si[0] bits can be programmed to any value and will be inserted into the first of each FAS frame and NFAS frame respectively. When CRC Multi-Frame generation is enabled (GENCRC is logic 1) and FEBE indication is disabled (FEBEDIS is logic 1), the values programmed in the Si[1] and Si[0] bit positions are inserted into the E1 & E2 bit positions respectively. When GENCRC is logic 1 and FEBEDIS is logic 0, both Si[1] and Si[0] are ignored.

E1 FRMG Extra Bits Control (043H, 0C3H, 143H, 1C3H, 243H, 2C3H, 343H, 3C3H)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	Reserved				X[0]	Reserved	X[1]	X[2]
Type					R/W		R/W	R/W
Default					1		1	1

X[2:0]:

Valid when the FDIS (b3, E1-040H), the XDIS (b0, E1-040H), the SIGEN (b6, E1-040H) and the DLEN (b5, E1-040H) are all logic 0.

Replace the extra bits located in bits 5, 7 & 8 in TS16 of frame 0 of the Signaling Multi-Frame.

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E1 FRMG Interrupt Enable (044H, 0C4H, 144H, 1C4H, 244H, 2C4H, 344H, 3C4H)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	Reserved			SIGMFE	FASE	MFE	SMFE	Reserved (must be 0)
Type				R/W	R/W	R/W	R/W	
Default				0	0	0	0	

SIGMFE:

= 0: Disable the interrupt on the $\overline{INT}$ pin when the SIGMFI (b4, E1-045H) is logic one.

= 1: Enable the interrupt on the $\overline{INT}$ pin when the SIGMFI (b4, E1-045H) is logic one.

FASE:

= 0: Disable the interrupt on the $\overline{INT}$ pin when the FASI (b3, E1-045H) is logic one.

= 1: Enable the interrupt on the $\overline{INT}$ pin when the FASI (b3, E1-045H) is logic one.

MFE:

= 0: Disable the interrupt on the $\overline{INT}$ pin when the MFI (b2, E1-045H) is logic one.

= 1: Enable the interrupt on the $\overline{INT}$ pin when the MFI (b2, E1-045H) is logic one.

SMFE:

= 0: Disable the interrupt on the $\overline{INT}$ pin when the SMFI (b1, E1-045H) is logic one.

= 1: Enable the interrupt on the $\overline{INT}$ pin when the SMFI (b1, E1-045H) is logic one.

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E1 FRMG Interrupt Status (045H, 0C5H, 145H, 1C5H, 245H, 2C5H, 345H, 3C5H)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	Reserved			SIGMFI	FASI	MFI	SMFI	Reserved
Type				R	R	R	R	
Default				X	X	X	X	

The bits in this register are clear to ‘0 after the register is read.

SIGMFI:

Valid when the Signaling Multi-Frame is generated and coincides with the CRC Multi-Frame.
= 0: Not at the end of the first frame of a Signaling Multi-Frame.
= 1: Indicate the end of the first frame of a Signaling Multi-Frame.

FASI:

Valid when the Basic Frame is generated.
= 0: Not on the boundary of a FAS frame.
= 1: Indicate the boundary of a FAS frame.

MFI:

Valid when the CRC-4 Multi-Frame is generated.
= 0: Not at the end of the first frame of a CRC-4 Multi-Frame.
= 1: Indicate the end of the first frame of a CRC-4 Multi-Frame.

SMFI:

Valid when the CRC-4 Multi-Frame is generated.
= 0: Not at the end of the first frame of a CRC-4 Sub Multi-Frame.
= 1: Indicate the end of the first frame of a CRC-4 Sub Multi-Frame.

E1 FRMG National Bit Codeword Select (046H, 0C6H, 146H, 1C6H, 246H, 2C6H, 346H, 3C6H)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	SaSEL[2]	SaSEL[1]	SaSEL[0]					
Type	R/W	R/W	R/W			Reserved		
Default	0	0	0					

SaSEL[2:0]:

The SaSEL[2:0] select which National Bit Codeword (SaX) will be replaced by the SaX[1:4] (b3~0, E1-047H).

SaSEL[2:0]	National Bit Codeword
0 0 0	Reserved
0 0 1	
0 1 0	
0 1 1	Sa4
1 0 0	Sa5
1 0 1	Sa6
1 1 0	Sa7
1 1 1	Sa8

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E1 FRMG National Bit Codeword (047H, 0C7H, 147H, 1C7H, 247H, 2C7H, 347H, 3C7H)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	SaX_EN[1]	SaX_EN[2]	SaX_EN[3]	SaX_EN[4]	SaX[1]	SaX[2]	SaX[3]	SaX[4]
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	1	1	1	1

SaX_ENn:

Valid when the FDIS (b3, E1-040H) is logic 0, and the INDIS (b1, E1-040H) is logic 0.

= 0: Disable the corresponding bit in the SaX[1:4] to replace the national bit codeword selected by the SaSEL[2:0].

= 1: Enable the corresponding bit in the SaX[1:4] to replace the national bit codeword selected by the SaSEL[2:0].

SaX[1:4]:

These bits are the codeword to be inserted into a CRC-4 Sub Multi-Frame.

The setting in the SaX[1:4] will replace the National bits which are assigned by the SaSEL[2:0].

If the code word is written during SMF I of a CRC-4 Multi-Frame, it will appear in the SaX[1:4] bits of SMF II of the same Multi-Frame. If the code word is written during SMF II of a Multi-Frame, its contents will be latched internally and will appear in SMF I of the next Multi-Frame.

E1 RHDLC #1, #2, #3 Configuration (048H, 0C8H, 148H, 1C8H, 248H, 2C8H, 348H, 3C8H)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	Reserved				MEN	MM	TR	EN
Type					R/W	R/W	R/W	R/W
Default					0	0	0	0

Selection of the RHDLC block (#1, #2, or #3) whose registers are visible on the microprocessor interface is done via the RHDLCSEL[1:0] (b7~6, E1-00AH).

MEN, MM:

The MEN & MM define the address matching mode:

MEN	MM	Address Matching Mode
0	X	No address matching is needed. All the HDLC data is stored in the FIFO.
1	0	The HDLC data is stored in the FIFO when the first byte is all 'One's or the same as the setting in the PA[7:0] (b7~0, E1-04CH) or the SA[7:0] (b7~0, E1-04DH).
1	1	The HDLC data is stored in the FIFO when the most significant 6 bits in the first byte are all 'One's or the same as the setting in the PA[7:2] (b7~2, E1-04CH)or the SA[7:2] (b7~2, E1-04DH).

TR:

= 0: Normal operation.

= 1: Force the RHDLC to immediately terminate the reception of the current data frame, empty the FIFO buffer, clear the interrupts and initiate a new HDLC search.

This bit is clear to '0' after a rising and falling edge occur on the internal clock or after the register is read.

EN:

= 0: Disable the operation of the RHDLC block and all the FIFO buffer and interrupts are cleared.

= 1: Enable the operation of the RHDLC block and the HDLC opening flag will be searched immediately.

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If the EN is set from logic 1 to logic 0 and back to logic 1, the RHDLC will immediately terminate the reception of the current data frame, empty the FIFO buffer, clear the interrupts and initiate a new HDLC search.

E1 RHDLC #1, #2, #3 Interrupt Control (049H, 0C9H, 149H, 1C9H, 249H, 2C9H, 349H, 3C9H)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	INTE	INTC[6]	INTC[5]	INTC[4]	INTC[3]	INTC[2]	INTC[1]	INTC[0]
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Selection of the RHDLC block (#1, #2, or #3) whose registers are visible on the microprocessor interface is done via the RHDLCSEL[1:0] (b7~6, E1-00AH).

INTE:

= 0: Disable the interrupt on the $\overline{INT}$ pin when there is a transition from '0' to '1' on the INTR (b0, E1-04AH).

= 1: Enable the interrupt on the $\overline{INT}$ pin when there is a transition from '0' to '1' on the INTR (b0, E1-04AH).

INTC[6:0]:

These bits set the interrupt threshold point of the FIFO buffer. Exceeding the set point will cause an interrupt, and the interrupt will persist until the FIFO is empty. The set point is decimal 128 when the INTC[6:0] is all zeros.

The contents of this register should only be changed when the EN (b0, E1-048H) is logic 0. This prevents any erroneous interrupt generation.

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E1 RHDLC #1, #2, #3 Status (04AH, 0CAH, 14AH, 1CAH, 24AH, 2CAH, 34AH, 3CAH)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	FE	OVR	COLS	PKIN	PBS[2]	PBS[1]	PBS[0]	INTR
Type	R	R	R	R	R	R	R	R
Default	X	X	X	X	X	X	X	X

Selection of the RHDLC block (#1, #2, or #3) whose registers are visible on the microprocessor interface is done via the RHDLCSEL[1:0] (b7~6, E1-00AH).

FE:

= 0: The FIFO is loaded with data.

= 1: The FIFO is empty.

OVR:

The overwritten condition occurs when data is written over unread data in the FIFO buffer. This bit is cleared to '0' after the register is read.

= 0: No overwriting occurs.

= 1: The FIFO is overwritten, and then the FIFO is reset, which cause the COLS and PKIN to be reset to logic 0.

COLS:

This bit reflects the HDLC link status change.

= 0: Normal operation.

= 1: The first HDLC opening flag sequence (7E) activating the HDLC or the HDLC abort sequence (7F) deactivating the HDLC is detected.

This bit is cleared to '0' after the bit is read, or after the OVR transits to be logic 1, or after the EN is clear.

PKIN:

= 0: A HDLC packet has not been written into the FIFO.

= 1: A HDLC packet has been written into the FIFO.

This bit is cleared to '0' after the bit is read, or after the OVR transits to logic 1.

PBS[2:0]:

The PBS[2:0] indicate the status of the last byte read from the FIFO.

PBS[2:0]	Status of the Data
0 0 0	Normal data
0 0 1	A dummy byte to indicate the first HDLC opening flag sequence (7E) was detected, which means the HDLC link became active.
0 1 0	A dummy byte to indicate the HDLC abort sequence (7F) was detected, which means the HDLC link became inactive.
0 1 1	Reserved.
1 0 0	The last byte of a non-aborted HDLC packet was received. The HDLC packet is in an integer number of bytes and has no FCS error.
1 0 1	The last byte of a non-aborted HDLC packet was received and a non-integer number of bytes are in the packet.
1 1 0	The last byte of a non-aborted HDLC packet was received. The HDLC packet is in an integer number of bytes and has FCS errors.
1 1 1	The last byte of a non-aborted HDLC packet was received. The HDLC packet is in a non-integer number of bytes and has FCS errors.

INTR:

= 0: No interrupt sources in the HDLC Receiver block occur

= 1: Any one of the interrupt sources in the HDLC Receiver block occurs. The interrupt sources in the HDLC Receiver are: 1. Receiving the first 7E opening flag sequence which activates the HDLC link; 2. A packet was received; 3. Change of link status; 4. Exceeding the set point of the FIFO which is defined in the INTC[6:0] (b6~0, E1-049H); 5. Over-writing the FIFO.

This bit is cleared to '0' after the bit is read.

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E1 RHDLC #1, #2, #3 Data (04BH, 0CBH, 14BH, 1CBH, 24BH, 2CBH, 34BH, 3CBH)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	RD[7]	RD[6]	RD[5]	RD[4]	RD[3]	RD[2]	RD[1]	RD[0]
Type	R	R	R	R	R	R	R	R
Default	X	X	X	X	X	X	X	X

Selection of the RHDLC block (#1, #2, or #3) whose registers are visible on the microprocessor interface is done via the RHDLCSEL[1:0] (b7~6, E1-00AH).

RD[7:0]:

This register represents the bytes read from the FIFO. This register should not be accessed at a rate greater than 1/15 of the XCK rate.

The RD[0] corresponds to the first bit of the serial received data from the FIFO.

E1 RHDLC #1, #2, #3 Primary Address Match (04CH, 0CCH, 14CH, 1CCH, 24CH, 2CCH, 34CH, 3CCH)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	PA[7]	PA[6]	PA[5]	PA[4]	PA[3]	PA[2]	PA[1]	PA[0]
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	1	1	1	1	1	1	1	1

Selection of the RHDLC block (#1, #2, or #3) whose registers are visible on the microprocessor interface is done via the RHDLCSEL[1:0] (b7~6, E1-00AH).

PA[7:0]:

These bits stipulate the primary address pattern.

PA[0] stores the first bit of the serial data.

E1 RHDLC #1, #2, #3 Secondary Address Match (04DH, 0CDH, 14DH, 1CDH, 24DH, 2CDH, 34DH, 3CDH)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	SA[7]	SA[6]	SA[5]	SA[4]	SA[3]	SA[2]	SA[1]	SA[0]
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	1	1	1	1	1	1	1	1

Selection of the RHDLC block (#1, #2, or #3) whose registers are visible on the microprocessor interface is done via the RHDLCSEL[1:0] (b7~6, E1-00AH).

SA[7:0]:

These bits stipulate the secondary address pattern.

SA[0] stores the first bit of the serial data.

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E1 THDLC #1, #2, #3 Configuration (050H, 0D0H, 150H, 1D0H, 250H, 2D0H, 350H, 3D0H)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	FLGSHARE	FIFOCLR	Reserved		EOM	ABT	CRC	EN
Type	R/W	R/W			R/W	R/W	R/W	R/W
Default	1	0			0	0	1	0

Selection of the THDLC block (#1, #2, or #3) whose registers are visible on the microprocessor interface is done via the THDLCSEL[1:0] (b5~4, E1-00AH).

FLGSHARE:

= 0: The opening flag of the next HDLC frame and closing flag of the current HDLC frame are separate.

= 1: The opening flag of the next HDLC frame and closing flag of the current HDLC frame are shared

FIFOCLR:

= 0: Normal operation.

= 1: Clear the FIFO.

EOM:

= 0: Normal operation.

= 1: A positive transition of this bit starts a packet transmission. Then if the CRC(b1, E1-050H) is set, the 16-bit FCS word is appended to the last data byte transmitted.

ABT:

= 0: Normal operation.

= 1: Transmit the 7F abort sequence after the current setting in the Transmit Data register is transmitted, so that the FIFO is cleared and all data in the FIFO will be lost.

Aborts are continuously sent and the FIFO is held in reset until this bit is reset to a logic 0. At least one Abort sequence will be sent when the ABT transitions from logic 0 to logic 1.

CRC:

= 0: Do not append the CRC-16 frame check sequences (FCS) to the end of the HDLC data.

= 1: Append the FCS to the end of the HDLC data.

EN:

= 0: Disable the operation of the THDLC block.

= 1: Enable the operation of the THDLC block and flag sequences are sent until data is written into the THDLC Transmit Data register and the EOM is set to logic 1.

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E1 THDLC #1, #2, #3 Upper Transmit Threshold (051H, 0D1H, 151H, 1D1H, 251H, 2D1H, 351H, 3D1H)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	Reserved	UTHR[6]	UTHR[5]	UTHR[4]	UTHR[3]	UTHR[2]	UTHR[1]	UTHR[0]
Type		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		1	0	0	0	0	0	0

Selection of the THDLC block (#1, #2, or #3) whose registers are visible on the microprocessor interface is done via the THDLCSEL[1:0] (b5~4, E1-00AH).

UTHR[6:0]:

These bits define the upper fill level of the FIFO. Once the fill level exceeds the UTHR[6:0] value, the data stored in the FIFO will start to transmit. The transmission will not stop until the complete packet is transmitted and the THDLC FIFO fill level is below 'UTHR[6:0] + 1'.

It should be greater than the value of the LINT[6:0] unless both are equal to 00H.

E1 THDLC #1, #2, #3 Lower Interrupt Threshold (052H, 0D2H, 152H, 1D2H, 252H, 2D2H, 352H, 3D2H)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	Reserved	LINT[6]	LINT[5]	LINT[4]	LINT[3]	LINT[2]	LINT[1]	LINT[0]
Type		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	1	1	1

Selection of the THDLC block (#1, #2, or #3) whose registers are visible on the microprocessor interface is done via the THDLCSEL[1:0] (b5~4, E1-00AH).

LINT[6:0]:

These bits define the fill level of the FIFO that can introduce an interrupt. That is, when the fill level of the FIFO is below the LINT[6:0], an interrupt will be generated. The LINT[6:0] should be less than the value of the UTHR[6:0] unless both are equal to 00H.

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E1 THDLC #1, #2, #3 Interrupt Enable (053H, 0D3H, 153H, 1D3H, 253H, 2D3H, 353H, 3D3H)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	Reserved				FULLE	OVRE	UDRE	LFILLE
Type					R/W	R/W	R/W	R/W
Default					0	0	0	0

Selection of the THDLC block (#1, #2, or #3) whose registers are visible on the microprocessor interface is done via the THDLCSEL[1:0] (b5~4, E1-00AH).

FULLE:
= 0: Disable the interrupt on the $\overline{INT}$ pin when the FULLI (b3, E1-054H) is logic 1.
= 1: Enable the interrupt on the $\overline{INT}$ pin when the FULLI (b3, E1-054H) is logic 1.

OVRE:
= 0: Disable the interrupt on the $\overline{INT}$ pin when the OVRI (b2, E1-054H) is logic 1.
= 1: Enable the interrupt on the $\overline{INT}$ pin when the OVRI (b2, E1-054H) is logic 1.

UDRE:
= 0: Disable the interrupt on the $\overline{INT}$ pin when the UDRI (b1, E1-054H) is logic 1.
= 1: Enable the interrupt on the $\overline{INT}$ pin when the UDRI (b1, E1-054H) is logic 1.

LFILLE:
= 0: Disable the interrupt on the $\overline{INT}$ pin when the LFILLI (b0, E1-054H) is logic 1.
= 1: Enable the interrupt on the $\overline{INT}$ pin when the LFILLI (b0, E1-054H) is logic 1.

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E1 THDLC #1, #2, #3 Interrupt Status / UDR Clear (054H, 0D4H, 154H, 1D4H, 254H, 2D4H, 354H, 3D4H)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	Reserved	FULL	BLFILL	Reserved	FULLI	OVRI	UDRI	LFILLI
Type		R	R		R	R	R	R
Default		X	X		X	X	X	X

Selection of the THDLC block (#1, #2, or #3) whose registers are visible on the microprocessor interface is done via the THDLCSEL[1:0] (b5~4, E1-00AH).

FULL:

= 0: The THDLC FIFO is not full.

= 1: The THDLC FIFO is full (128 bytes).

BLFILL:

= 0: The fill level in the THDLC FIFO is not below the value of the LINT[6:0] (b6~0, E1-052H).

= 1: The fill level in the THDLC FIFO is empty or below the value of the LINT[6:0] (b6~0, E1-052H).

FULLI:

= 0: There is no transition (from '0' to '1') on the FULL.

= 1: There is a transition (from '0' to '1') on the FULL.

This bit is cleared to '0' after the bit is read.

OVRI:

The Over-Written is that the THDLC FIFO was already full when another data byte was written to the THDLC Transmit Data register.

= 0: The THDLC FIFO is not overwritten.

= 1: The THDLC FIFO is overwritten.

This bit is cleared to '0' after the bit is read.

UDRI:

The Under-Run is that the THDLC was in the process of transmitting a packet when it ran out of data to be transmitted.

= 0: The THDLC FIFO is not under-run.

= 1: The THDLC FIFO is under-run.

This bit is cleared to '0' after the bit is read.

LFILLI:

= 0: There is no transition (from '0' to '1') on the BLFILL.

= 1: There is a transition (from '0' to '1') on the BLFILL.

This bit is cleared to '0' after the bit is read.

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E1 THDLC #1, #2, #3 Transmit Data (055H, 0D5H, 155H, 1D5H, 255H, 2D5H, 355H, 3D5H)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	TD[7]	TD[6]	TD[5]	TD[4]	TD[3]	TD[2]	TD[1]	TD[0]
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	X	X	X	X	X	X	X	X

Selection of the THDLC block (#1, #2, or #3) whose registers are visible on the microprocessor interface is done via the THDLCSEL[1:0] (b5~4, E1-00AH).

The content is the data to be transmitted. It is serially transmitted (TD[0] is the first).

E1 ELSB Interrupt Enable / Status (059H, 0D9H, 159H, 1D9H, 259H, 2D9H, 359H, 3D9H)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	Reserved					SLIPE	SLIPD	SLIPI
Type						R/W	R	R
Default						0	X	X

SLIPE:
= 0: Disable the interrupt on the $\overline{INT}$ pin when a slip occurs.
= 1: Enable the interrupt on the $\overline{INT}$ pin when a slip occurs.

SLIPD:
This bit makes sense only when the SLIPI is logic 1.
= 0: The latest slip is due to the Elastic Store Buffer being empty; a frame was duplicated.
= 1: The latest slip is due to the Elastic Store Buffer being full; a frame was deleted.

SLIPI:
= 0: No slip occurs.
= 1: A slip occurs.
This bit is cleared to '0' after the bit is read.

E1 ELSB Idle Code (05AH, 0DAH, 15AH, 1DAH, 25AH, 2DAH, 35AH, 3DAH)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	D7	D6	D5	D4	D3	D2	D1	D0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	1	1	1	1	1	1	1	1

These bits set the idle code that will replace the data on RSDn/MRSD when it is out of Basic Frame and the TRKEN (b1, E1-001H) is logic 1. D7 is the first bit to be inserted.

The writing of the idle code pattern is asynchronous with respect to the output data clock. One time slot of idle code data will be corrupted if the register is written to when the framer is out of frame.

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E1 RPLC Configuration (05CH, 0DCH, 15CH, 1DCH, 25CH, 2DCH, 35CH, 3DCH)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	Reserved							PCCE
Type								R/W
Default								0

PCCE:

= 0: The per-TS functions in RPLC are disabled.

= 1: The per-TS functions in RPLC are enabled.

E1 RPLC µP Access Status (05DH, 0DDH, 15DH, 1DDH, 25DH, 2DDH, 35DH, 3DDH)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	BUSY	Reserved						
Type	R							
Default	0							

BUSY:

= 0: No reading or writing operation on the indirect registers.

= 1: An internal indirect register is being accessed, any new operation on the internal indirect register is not allowed.

This bit goes low timed to an internal high-speed clock rising edge after the operation has been completed. The operation cycle is 490 ns. No operations to the indirect registers are possible until this bit is logic 0.

E1 RPLC Channel Indirect Address / Control (05EH, 0DEH, 15EH, 1DEH, 25EH, 2DEH, 35EH, 3DEH)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	R/WB	A6	A5	A4	A3	A2	A1	A0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Writing to this register with a valid address and Read/Write command initiates an internal operation cycle to the indirect registers.

R/WB:

= 0: Write the data to the specified indirect register.

= 1: Read the data from the specified indirect register.

A[6:0]:

Specify the address of the indirect registers (from 20H to 7FH) for the microprocessor access.

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E1 RPLC Channel Indirect Data Buffer (05FH, 0DFH, 15FH, 1DFH, 25FH, 2DFH, 35FH, 3DFH)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	D7	D6	D5	D4	D3	D2	D1	D0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

This register hold the value which will be read from or write into the indirect registers (from 20H to 7FH). If data is to be written to the indirect registers, the byte to be written must be written into this register before the target indirect register address and R/WB = 0 is written into the Address/Control register, initiating the access. If data is to be read from the indirect registers, only the target indirect register address and R/WB = 1 is written into the Address/Control register, initiating the request. After 490 ns, this register will contain the requested data byte.

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RPLC Indirect Registers Map	
20H ~ 3FH	Per-TS Configuration Byte for TS0 ~ TS31
40H ~ 5FH	Data Trunk Conditioning Code Byte for TS0 ~ TS31
61H ~ 7FH	Signaling Trunk Conditioning Byte for TS1 ~ TS31

E1 RPLC Per-TS Configuration Registers (RPLC Indirect Registers 20H ~ 3FH)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	TEST	DTRKC/NxTS	STRKC	DMW	DMWALAW	SIGNINV	RINV[1]	RINV[0]
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	X	X	X	X	X	X	X	X

TEST:

= 0: Disable the data in the corresponding time slot to be tested by PRGD.

= 1: Enable the data in the corresponding time slot to be extracted to PRGD for test (when the RXPATGEN [b2, E1-00CH] is logic 0), or enable the test pattern from PRGD to replace the data in the corresponding time slot for test (when the RXPATGEN [b2, E1-00CH] is logic 1).

All the time slots that are extracted to the PRGD are concatenated and treated as a continuous stream in which pseudo random is searched for. Similarly, all time slots set to be replaced with PRGD test pattern data are concatenated replaced by the PRBS.

DTRKC/NxTS:

= 0: Disable the data in the corresponding time slot to be replaced by the data set in the DTRK[7:0] (b7~0, E1-RPLC-indirect registers-40~5FH) when output on the RSDn/MRSD pin.

= 1: Enable the data in the corresponding time slot to be replaced by the data set in the DTRK[7:0] (b7~0, E1-RPLC-indirect registers-40~5FH) when output on the RSDn/MRSD pin.

In addition, it controls RSCKn of the corresponding time slot in Receive Clock Slave Fractional E1 mode:

= 0: RSCKn is clocked for the corresponding time slot.

= 1: RSCKn is held in its inactive state.

STRKC:

= 0: Disable the signaling of the corresponding time slot to be replaced by the data set in the A, B, C, D (b3~0, E1-RPLC-indirect registers-61~7FH) when output on the RSSIGn/MRSSIG pin.

= 1: Enable the signaling of the corresponding time slot to be replaced by the data set in the A, B, C, D (b3~0, E1-RPLC-indirect registers-61~7FH) when output on the RSSIGn/MRSSIG pin.

DMW:

= 0: Disallow the data in the corresponding time slot to be replaced by a digital milliwatt pattern when output on the RSDn/MRSD pin.

= 1: Enable the data in the corresponding time slot to be replaced by a digital milliwatt pattern when output on the RSDn/MRSD pin.

DMWALAW:

= 0: The milliwatt pattern is the μ-Law pattern.

= 1: The milliwatt pattern is the A-Law pattern.

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SIGNINV, RINV[1:0]:

The SIGNINV and the RINV[1:0] bits select the bits in the corresponding time slot to be inverted when output on the RSDn/MRSD pin:

SIGNINV	RINV[1:0]	Bits Inverted
0	0 0	No inversion
0	0 1	Invert the even bits (2, 4, 6, 8) of the time slot (bit 1 is the MSB)
0	1 0	Invert the odd bits (1, 3, 5, 7) of the time slot (bit 1 is the MSB)
0	1 1	Invert all the bits of the time slot
1	0 0	Invert the bit 1 (MSB) of the time slot
1	0 1	Invert the bits 1, 2, 4, 6 and 8 of the time slot
1	1 0	Invert the bits 3, 5 and 7 of the time slot
1	1 1	Invert all the bits of the time slot except the MSB (bit1)

The priority of the RPLC operation on the RSDn pin from high to low is:

Extract data to PRGD for test; Replace the data with the value in the DTRK[7:0]; Replace the data with the milliwatt pattern; Replace the data with the pattern generated in the PRGD; Invert the bit.

E1 RPLC Data Trunk Conditioning Code Byte Registers (RPLC Indirect Registers 40H ~ 5FH)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	DTRK7	DTRK6	DTRK5	DTRK4	DTRK3	DTRK2	DTRK1	DTRK0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	X	X	X	X	X	X	X	X

They contain the data that will replace the data output on the RSDn/MRSD pin when the corresponding bit DTRKC/NxTS (b6, E1-RPLC-indirect registers-20~3FH) is logic 1. The DTRK7 is the MSB.

E1 RPLC Signaling Trunk Conditioning Byte Registers (RPLC Indirect Registers 61H ~ 7FH)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	Reserved				A	B	C	D
Type					R/W	R/W	R/W	R/W
Default					X	X	X	X

These bits contain the data that will replace the data output on the RSSIGn/MRSSIG pin when the corresponding STRKC (b5, E1-RPLC-indirect registers-20~3FH) is logic 1. They are in the least significant nibble.

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E1 TPLC Configuration (060H, 0E0H, 160H, 1E0H, 260H, 2E0H, 360H, 3E0H)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	Reserved							PCCE
Type								R/W
Default								0

PCCE:

= 0: The per-TS functions in TPLC are disabled.

= 1: The per-TS functions in TPLC are enabled.

E1 TPLC µP Access Status (061H, 0E1H, 161H, 1E1H, 261H, 2E1H, 361H, 3E1H)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	BUSY	Reserved						
Type	R							
Default	0							

BUSY:

= 0: No reading or writing operation on the indirect registers.

= 1: An internal indirect register is being accessed. Any new operation on the internal indirect register is not allowed.

This bit goes low timed to an internal high-speed clock rising edge after the operation has been completed. The operation cycle is 490 ns. No more operations to the indirect registers could be done until this bit is cleared.

E1 TPLC Channel Indirect Address / Control (062H, 0E2H, 162H, 1E2H, 262H, 2E2H, 362H, 3E2H)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	R/WB	A6	A5	A4	A3	A2	A1	A0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Writing to this register with a valid address and Read/Write command initiates an internal operation cycle to the indirect registers.

R/WB:

= 0: Write the data to the specified indirect register.

= 1: Read the data from the specified indirect register.

A[6:0]:

Specify the address of the indirect registers (from 20H to 7FH) for the microprocessor access.

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E1 TPLC Channel Indirect Data Buffer (063H, 0E3H, 163H, 1E3H, 263H, 2E3H, 363H, 3E3H)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	D7	D6	D5	D4	D3	D2	D1	D0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

This register hold the value which will be read from or write into the indirect registers (from 20H to 7FH). If data is to be written to the indirect registers, the byte to be written must be written into this register before the target indirect register address and R/WB = 0 is written into the Address/Control register, initiating the access. If data is to be read from the indirect registers, only the target indirect register address and R/WB = 1 is written into the Address/Control register, initiating the request. After 490 ns, this register will contain the requested data byte.

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TPLC Indirect Registers Map	
20H ~ 3FH	Per-TS Control Byte for TS0 ~ TS31
40H ~ 5FH	IDLE Code Byte for TS0 ~ TS31
61H ~ 7FH	Signaling /PCM Control Byte for TS1 ~ TS31

E1 TPLC Per-TS Control Registers (TPLC Indirect Registers 20H ~ 3FH)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	SUBS	Reserved	DS1	DS0	TEST	LOOP	Reserved	
Type	R/W		R/W	R/W	R/W	R/W		
Default	X		X	X	X	X		

SUBS, DS1, DS0:

The SUBS, DS[1:0] bits select one of the operations to the corresponding time slot:

SUBS	DS[1]	DS[0]	OPERATION
0	0	0	No change to the time slot
0	1	0	Invert the odd bits (1, 3, 5, 7) of the time slot (bit 1 is the LSB)
0	0	1	Invert the even bits (2, 4, 6, 8) of the time slot (bit 8 is the MSB)
0	1	1	Invert all the bits of the time slot
1	-	0	Replace the time slot with the IDLE code
1	0	1	Replace the time slot with the A-law digital milliwatt pattern (per G.711)
1	1	1	Replace the time slot with the μ-law digital milliwatt pattern (per G.711)

TEST:

= 0: Disable the data in the corresponding time slot to be tested by PRGD.

= 1: Enable the data in the corresponding time slot to be extracted to PRGD for test (when the RXPATGEN [b2, E1-00CH] is logic 1), or enable the test pattern from PRGD to replace the data in the corresponding time slot for test (when the RXPATGEN [b2, E1-00CH] is logic 0).

All the time slots that are extracted to the PRGD are concatenated and treated as a continuous stream in which pseudo random is searched for. Similarly, all time slots set to be replaced with PRGD test pattern data are concatenated replaced by the PRBS.

LOOP:

= 0: Disable the payload loopback.

= 1: Enable the payload loopback. When Receive Clock Master modes are enabled, the Elastic Store is used to align the receive line data to the data to be transmitted. When Receive Clock Slave modes are enabled, the Elastic Store is unavailable to facilitate the payload loopbacks, and loop-back functionality is provided only when the transmit path is also in Transmit Clock Slave mode, and the received clock and the clock to be transmitted and Common Frame Pulse are identical (RSCCK = TSCCKB, RSCFS = TSCFS).

The priority of the TPLC operation on the TSDn pin from high to low is:

Extract data to PRGD for test; Payload loopback; Replace the data with the milliwatt pattern; Replace the data with the pattern generated in the PRGD; Replace the data with the value in the IDLE[7:0]; Invert the even bits or/and odd bits.

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E1 TPLC IDLE Code Byte Registers (TPLC Indirect Registers 40H ~ 5FH)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	IDLE7	IDLE6	IDLE5	IDLE4	IDLE3	IDLE2	IDLE1	IDLE0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	X	X	X	X	X	X	X	X

They contain the data that will replace the data input from the TSDn pin when the corresponding SUBS and DS[1:0] are allowed. IDLE7 is the MSB.

E1 TPLC Signaling / PCM Control Byte Registers (TPLC Indirect Registers 61H ñ 7FH)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	Reserved			SIGSRC	A	B	C	D
Type				R/W	R/W	R/W	R/W	R/W
Default				X	X	X	X	X

SIGSRC:

This bit is valid only if the Channel Associated Signaling (CAS) is selected in the E1 FRMG Configuration Register.

= 0: Use the data on the TSSIGn pin as the signaling.

= 1: Use the data in the A, B, C, D bits as the signaling.

A, B, C, D:

They contain the data that can be used as signaling when the corresponding SIGSRC is logic 1. They are in the least significant nibble.

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E1 RCRB Configuration (COSS = 0) (064H, 0E4H, 164H, 1E4H, 264H, 2E4H, 364H, 3E4H)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	Reserved	COSS	SIGE	Reserved				PCCE
Type		R/W	R/W					R/W
Default		0	0					0

COSS:

= 0: Allow the RCRB registers to access the indirect registers.

= 1: Allow the RCRB registers to reflect the change of the signaling of its corresponding time slot.

SIGE:

= 0: Disable generation of an interrupt on the $\overline{INT}$ pin when there is a signaling change in any one of the 30 time slots.

= 1: Enable generation of an interrupt on the $\overline{INT}$ pin when there is a signaling change in any one of the 30 time slots.

PCCE:

= 0: The per-TS functions in RCRB are disabled.

= 1: The per-TS functions in RCRB are enabled.

E1 RCRB Time Slot Indirect Status (COSS = 0) (065H, 0E5H, 165H, 1E5H, 265H, 2E5H, 365H, 3E5H)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	BUSY	Reserved						
Type	R							
Default	0							

BUSY:

= 0: No reading or writing operation on the indirect registers.

= 1: An internal indirect register is being accessed. Any new operation on the internal indirect register is not allowed.

This bit goes low timed to an internal high-speed clock rising edge after the operation has been completed. The operation cycle is 490 ns. No operations to the indirect registers can be done until this bit is cleared.

E1 RCRB Time Slot Indirect Address / Control (COSS = 0) (066H, 0E6H, 166H, 1E6H, 266H, 2E6H, 366H, 3E6H)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	R/WB	A6	A5	A4	A3	A2	A1	A0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

R/WB:

= 0: Write the data to the specified indirect register.

= 1: Read the data from the specified indirect register.

A[6:0]:

Specified the address of the indirect registers (from 20H to 5FH) for the microprocessor access.

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E1 RCRB Time Slot Indirect Data Buffer (COSS = 0) (067H, 0E7H, 167H, 1E7H, 267H, 2E7H, 367H, 3E7H)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	D7	D6	D5	D4	D3	D2	D1	D0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	X	X	X	X	X	X	X	X

This register holds the value which will be read from or written to the indirect registers (from 20H to 7FH). If data is to be written to the indirect registers, the byte to be written must be written into this register before the target indirect register address and R/WB = 0 is written into the Address/Control register, initiating the access. If data is to be read from the indirect registers, only the target indirect register address and R/WB = 1 is written into the Address/Control register, initiating the request. After 490 ns, this register will contain the requested data byte.

E1 RCRB Change of Signaling State (COSS = 1) (064H, 0E4H, 164H, 1E4H, 264H, 2E4H, 364H, 3E4H)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	Reserved	COSS	COSS[30]	COSS[29]	COSS[28]	COSS[27]	COSS[26]	COSS[25]
Type		R/W	R	R	R	R	R	R
Default		0	X	X	X	X	X	X

COSS:

= 0: Allow the RCRB registers to access the indirect registers.

= 1: Allow the RCRB registers to reflect the change of the signaling of its corresponding time slot.

COSSn:

= 0: The signaling in its corresponding time slot is not changed.

= 1: The signaling in its corresponding time slot is changed.

These bits are cleared to '0' after the register is read. COSS[30:25] correspond to time slots 31 to 26.

E1 RCRB Change of Signaling State (COSS = 1) (065H, 0E5H, 165H, 1E5H, 265H, 2E5H, 365H, 3E5H)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	COSS[24]	COSS[23]	COSS[22]	COSS[21]	COSS[20]	COSS[19]	COSS[18]	COSS[17]
Type	R	R	R	R	R	R	R	R
Default	X	X	X	X	X	X	X	X

COSSn:

= 0: The signaling in its corresponding time slot is not changed.

= 1: The signaling in its corresponding time slot is changed.

These bits are cleared to '0' after the register is read. COSS[24:17] correspond to time slots 25 to 18.

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E1 RCRB Change of Signaling State (COSS = 1) (066H, 0E6H, 166H, 1E6H, 266H, 2E6H, 366H, 3E6H)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	COSS[16]	COSS[15]	COSS[14]	COSS[13]	COSS[12]	COSS[11]	COSS[10]	COSS[9]
Type	R	R	R	R	R	R	R	R
Default	X	X	X	X	X	X	X	X

COSSn:

= 0: The signaling in its corresponding time slot is not changed.

= 1: The signaling in its corresponding time slot is changed.

These bits are cleared to '0' after the register is read. COSS[16] corresponds to time slots 17. COSS[15:9] correspond to time slot 15 to 9.

E1 RCRB Change of Signaling State (COSS = 1) (067H, 0E7H, 167H, 1E7H, 267H, 2E7H, 367H, 3E7H)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	COSS[8]	COSS[7]	COSS[6]	COSS[5]	COSS[4]	COSS[3]	COSS[2]	COSS[1]
Type	R	R	R	R	R	R	R	R
Default	X	X	X	X	X	X	X	X

COSSn:

= 0: The signaling in its corresponding time slot is not changed.

= 1: The signaling in its corresponding time slot is changed.

These bits are cleared to '0' after the register is read. COSS[8:1] correspond to time slots 8 to 1.

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RCRB Indirect Registers Map	
20H	-
01H ~ 0FH / 21H ~ 2FH	Signaling Data Register for TS1 ~ 15
10H, 30H	-
11H ~ 1FH / 31H ~ 3FH	Signaling Data Register for TS17 ~31
40H ~ 5FH	TS0 ~ 31 Configuration Data

E1 RCRB Time Slot / Channel Signaling Data Registers (COSS = 0) (RCRB Indirect Registers 01H ~ 1FH / 21H ~ 3FH)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	Reserved				A	B	C	D
Type					R	R	R	R
Default					X	X	X	X

A, B, C, D:

They contain the signaling of the corresponding time slot. The value for TS0 and TS16 is not valid.

There is a maximum 2 ms delay between the transition of the COSS[n] bit (E1-064H & E1-065H & E1-066H & E1-067H) and the updating of the A, B, C, D code in the corresponding indirect registers 21H ~ 3FH. To avoid this 2 ms delay, users can read the corresponding b3~0 in the indirect registers 01H ~ 1FH first. If the value of these four bits is different from the previous A, B, C, D code, then the content of b3~0 in the 01H ~ 1FH is the updated A, B, C, D code. If the content of the four bits is the same as the previous A, B, C, D code, then users should read the b3~0 in the 21H ~ 3FH to get the updated A, B, C, D code.

E1 RCRB Per-Timeslot Configuration Registers (COSS = 0) (RCRB Indirect Registers 40H ~ 5FH)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	Reserved							DEB
Type								R/W
Default								X

DEB:

= 0: Disable signaling debounce.

= 1: Enable signaling debounce (valid only if the PCCE is logic 1). That is, the signaling is acknowledged only when 2 consecutive signaling bits of a time slot are the same.

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E1 PMON Interrupt Enable / Status (068H, 0E8H, 168H, 1E8H, 268H, 2E8H, 368H, 3E8H)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	Reserved					INTE	XFER	OVR
Type						R/W	R	R
Default						0	0	0

INTE:

= 0: Disable the interrupt on the $\overline{INT}$ pin when the counter data has been transferred into the Error Count registers.

= 1: Enable the interrupt on the $\overline{INT}$ pin when the counter data has been transferred into the Error Count registers.

XFER:

= 0: Indicate that the counter data has not been transferred to the Error Count registers.

= 1: Indicate that the counter data has been transferred to the Error Count registers.

This bit is clear to '0' after the bit is read.

OVR:

= 0: Indicate that no overwritten on the Error Count registers has occurred.

= 1: Indicate that one of the Error Count registers is overwritten.

This bit is clear to '0' after the bit is read.

Registers 069H-06DH, 0E9H-0EDH, 16H-16DH, 1E9H-1EDH, 269H-26DH,2E9H-2EDH,369H-36DH, 3E9H-3EDH:

The PMON Error Count registers for a single framer are updated as a group by writing to any of the PMON count registers or updated every 1 second when the AUTOUPDATE (b0, E1-000H) is set. The PMON Error Count registers for eight framers are updated by writing to the Chip ID/Global PMON Update register (E1-009H).

When the chip is reset, the contents of the PMON Error Count registers are unknown until the first latching of performance data is performed.

E1 PMON Framing Bit Error Count (069H, 0E9H, 169H, 1E9H, 269H, 2E9H, 369H, 3E9H)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	Reserved	FER[6]	FER[5]	FER[4]	FER[3]	FER[2]	FER[1]	FER[0]
Type		R	R	R	R	R	R	R
Default		X	X	X	X	X	X	X

These bits are valid when it is in the Basic Frame Synchronization. They represent the number of the basic frame alignment signal errors and update on the defined intervals. The basic frame alignment signal errors are defined in the WORDERR (b5, E1-000H) and the CNTNFAS (b4, E1-000H).

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E1 PMON Far End Block Error Count LSB (06AH, 0EAH, 16AH, 1EAH, 26AH, 2EAH, 36AH, 3EAH)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	FEBE[7]	FEBE[6]	FEBE[5]	FEBE[4]	FEBE[3]	FEBE[2]	FEBE[1]	FEBE[0]
Type	R	R	R	R	R	R	R	R
Default	X	X	X	X	X	X	X	X

E1 PMON Far End Block Error Count MSB (06BH, 0EBH, 16BH, 1EBH, 26BH, 2EBH, 36BH, 3EBH)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	Reserved						FEBE[9]	FEBE[8]
Type							R	R
Default							X	X

The FEBE[9:0] are valid when it is in CRC Multi-Frame Synchronization. They represent the number of the Far End Block Errors (FEBE) and update on the defined intervals.

E1 PMON CRC Error Count LSB (06CH, 0ECH, 16CH, 1ECH, 26CH, 2ECH, 36CH, 3ECH)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	CRCE[7]	CRCE[6]	CRCE[5]	CRCE[4]	CRCE[3]	CRCE[2]	CRCE[1]	CRCE[0]
Type	R	R	R	R	R	R	R	R
Default	X	X	X	X	X	X	X	X

E1 PMON CRC Error Count MSB (06DH, 0EDH, 16DH, 1EDH, 26DH, 2EDH, 36DH, 3EDH)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	Reserved						CRCE[9]	CRCE[8]
Type							R	R
Default							X	X

The CRCE[9:0] are valid when it is in CRC Multi-Frame Synchronization. They represent the number of the CRC errors and update on the defined intervals.

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E1 PRGD Control (070H)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	PDR[1]	PDR[0]	Reserved	PS	TINV	RINV	AUTOSYNC	MANSYNC
Type	R/W	R/W		R/W	R/W	R/W	R/W	R/W
Default	0	0		0	0	0	1	0

PDR[1:0]:

The PDR[1:0] define the function of the four PRGD Pattern Detector registers:

PDR[1:0]	PRGD Pattern Detector Registers (#1 ~ #4)
0 0, 0 1	Pattern Receive
1 0	Error Count
1 1	Bit Count
(The #1 is the LSB, while the #4 is the MSB.)	

PS:

= 0: A pseudo-random pattern is generated/detected by the PRGD.

= 1: A repetitive pattern is generated/detected by the PRGD.

This bit should be set first of all the PRGD registers.

TINV:

= 0: Disable the inversion of the generated pattern before being transmitted.

= 1: Enable the inversion of the generated pattern before being transmitted.

RINV:

= 0: Disable the inversion of the received pattern before being processed.

= 1: Enable the inversion of the received pattern before being processed.

AUTOSYNC:

= 0: Disable automatically re-searching for the synchronization of the pattern when the PRGD pattern is out of synchronization.

= 1: Enable automatically re-searching for the synchronization of the pattern when the PRGD pattern is out of synchronization.

MANSYNC:

Trigger on the rising edge. A transition from logic 0 to logic 1 on this bit manually initiates a re-search for the synchronization of a pattern.

Every time when the setting of the PRGD registers is changed or the detector data source changes, a manual synchronization operation is recommended to ensure that the detector works correctly.

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E1 PRGD Interrupt Enable / Status (071H)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	SYNCE	BEE	XFERE	SYNCV	SYNCI	BEI	XFERI	OVR
Type	R/W	R/W	R/W	R	R	R	R	R
Default	0	0	0	X	X	X	X	X

SYNCE:

= 0: Disable the interrupt on the $\overline{INT}$ pin when the SYNCI is logic one.

= 1: Enable the interrupt on the $\overline{INT}$ pin when the SYNCI is logic one.

BEE:

= 0: Disable the interrupt on the $\overline{INT}$ pin when bit error has been detected in the received pattern.

= 1: Enable the interrupt on the $\overline{INT}$ pin when each bit error is detected in the received pattern.

XFERE:

= 0: Disable the interrupt on the $\overline{INT}$ pin when the data in the PRGD pattern detector register is updated.

= 1: Enable the interrupt on the $\overline{INT}$ pin when the data in the PRGD pattern detector register is updated.

SYNCV:

= 0: The pattern is out of synchronization (the pattern detector has detected 10 or more bit errors in a hopping 48-bit window).

= 1: The pattern is in synchronization (the pattern detector has observed at least 48 consecutive error-free bit-periods).

SYNCI:

= 0: There is no transition on the SYNCV.

= 1: There is a transition (from '0' to '1' or from '1' to '0') on the SYNCV.

This bit is cleared to '0' after the bit is read.

BEI:

= 0: No bit error is detected in the received pattern.

= 1: At least one bit error has been detected in the received pattern.

This bit is cleared to '0' after the bit is read.

XFERI:

= 0: The data in the PRGD pattern detector register is not updated.

= 1: The data in the PRGD pattern detector register is updated.

This bit is cleared to '0' after the bit is read.

OVR:

= 0: The PRGD pattern detector register is not overwritten.

= 1: The PRGD pattern detector register is overwritten.

This bit is cleared to '0' after the bit is read.

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E1 PRGD Shift Register Length (072H)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	Reserved			PL[4]	PL[3]	PL[2]	PL[1]	PL[0]
Type				R/W	R/W	R/W	R/W	R/W
Default				0	0	0	0	0

These bits determine the length of the valid data in the PRGD pattern insertion register. The length is equal to the value of 'PL[4:0] + 1'.

E1 PRGD Tap Bit Type Function Default (073H)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	Reserved			PT[4]	PT[3]	PT[2]	PT[1]	PT[0]
Type				R/W	R/W	R/W	R/W	R/W
Default				0	0	0	0	0

These bits determine the feedback tap position of the generated pseudo random pattern before it is transmitted. The feedback tap position is equal to the value of 'PT[4:0] + 1'. In application, the PT is always less than the PL.

E1 PRGD Error Insertion (074H)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	Reserved				EVENT	EIR[2]	EIR[1]	EIR[0]
Type					R/W	R/W	R/W	R/W
Default					0	0	0	0

EVENT:

A single bit error is generated when the state of this bit is changed from '0' to '1'. To insert another bit error, this bit must be cleared to '0', and then set from '0' to '1' again.

EIR[2:0]:

The EIR[2:0] bits determine the bit error rate that will be inserted in the PRGD test pattern. If the bit error rate is changed from one non-zero value to another non-zero value, it is recommended to set the EIR[2:0] to '000' first, then set the EIR[2:0] to the desired value.

EIR[2:0]	Bit error rate
0 0 0	No error inserted
0 0 1	No error inserted
0 1 0	10^{-2}
0 1 1	10^{-3}
1 0 0	10^{-4}
1 0 1	10^{-5}
1 1 0	10^{-6}
1 1 1	10^{-7}

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E1 PRGD Pattern Insertion #1 (078H)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	PI[7]	PI[6]	PI[5]	PI[4]	PI[3]	PI[2]	PI[1]	PI[0]
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

E1 PRGD Pattern Insertion #2 (079H)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	PI[15]	PI[14]	PI[13]	PI[12]	PI[11]	PI[10]	PI[9]	PI[8]
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

E1 PRGD Pattern Insertion #3 (07AH)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	PI[23]	PI[22]	PI[21]	PI[20]	PI[19]	PI[18]	PI[17]	PI[16]
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

E1 PRGD Pattern Insertion #4 (07BH)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	PI[31]	PI[30]	PI[29]	PI[28]	PI[27]	PI[26]	PI[25]	PI[24]
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

When a repetitive pattern is selected to transmit, the data in these registers is the repetitive pattern.

When a pseudo random pattern is selected to transmit, the data in these registers should be set to FFFFFFFFH. They are the initial value for the pseudo random pattern.

Writing to the PI[31:24] updates the PRGD configuration.

When a repetitive pattern is transmitted, the PI[31] bit is transmitted first, followed by the remaining bits in sequence down to PI[0]. The length of the valid data in these four registers is determined by the PL[4:0]. When the length is less than 31, the bits in higher PI are not used.

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E1 PRGD Pattern Detector #1 (07CH)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	PD[7]	PD[6]	PD[5]	PD[4]	PD[3]	PD[2]	PD[1]	PD[0]
Type	R	R	R	R	R	R	R	R
Default	X	X	X	X	X	X	X	X

E1 PRGD Pattern Detector #2 (07DH)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	PD[15]	PD[14]	PD[13]	PD[12]	PD[11]	PD[10]	PD[9]	PD[8]
Type	R	R	R	R	R	R	R	R
Default	X	X	X	X	X	X	X	X

E1 PRGD Pattern Detector #3 (07EH)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	PD[23]	PD[22]	PD[21]	PD[20]	PD[19]	PD[18]	PD[17]	PD[16]
Type	R	R	R	R	R	R	R	R
Default	X	X	X	X	X	X	X	X

E1 PRGD Pattern Detector #4 (07FH)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	PD[31]	PD[30]	PD[29]	PD[28]	PD[27]	PD[26]	PD[25]	PD[24]
Type	R	R	R	R	R	R	R	R
Default	X	X	X	X	X	X	X	X

When the PDR[1:0] (b7~6, E1-070H) are set to '00' or '01', the four PRGD pattern detector registers are configured as Pattern Receive registers. They reflect the content of the received pattern.

When the PDR[1:0] (b7~6, E1-070H) are set to '10', the four PRGD pattern detector registers are configured as Error Counter registers. The value in these registers represents the number of the bit errors. The bit errors are not accumulated when the pattern is out of synchronization.

When the PDR[1:0] (b7~6, E1-070H) are set to '11', the four PRGD pattern detector registers are configured as Bit Counter registers. The value in these registers represents the total received bit number.

These registers can be configured to update every second automatically when the AUTOUPDATE (b0, E1-000H) is set to '1', or by writing to any of these four registers, or to the Revision / Chip ID / Global PMON register.

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5.2.2 T1/J1 MODE

T1 / J1 Receive Line Options (000H, 080H, 100H, 180H, 200H, 280H, 300H, 380H)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	FIFOBYP	UNF	IBCD_IDLE	Reserved	AUTOYELLOW	AUTORED	AUTOOOF	AUTOUPDATE
Type	R/W	R/W	R/W		R/W	R/W	R/W	R/W
Default	0	0	0		0	0	0	0

FIFOBYP:

This bit decides whether the received data should pass through or bypass the Receive Jitter Attenuation FIFO.

= 0: The received data passes through the RJAT FIFO.

= 1: The RJAT FIFO is bypassed. The delay is reduced by typically 24 bits.

UNF:

= 0: The Frame Processor operates normally.

= 1: Frame searching is disabled, the RCRB holds its signaling frozen, and Auto_OOF function, if enabled, will consider OOF to be declared.

IBCD_IDLE:

This bit is valid in framed mode.

= 0: Compare the inband loopback activate/deactivate code with all received data stream, including the F-bit. However, the result of F-bit comparison is discarded.

= 1: Compare the inband loopback activate/deactivate code with the received data stream, excluding the F-bit.

AUTOYELLOW:

This bit decides whether to send the Yellow Alarm signal automatically.

= 0: The automatic Yellow Alarm Transmission is disabled. It means that the Yellow Alarm can only be transmitted when the XYEL (b1, T1/J1-045H) is set to '1'.

= 1: The automatic Yellow Alarm Transmission is enabled. It means that the Yellow Alarm will be transmitted automatically when Red alarm is declared in the received data stream.

AUTORED:

This bit decides whether to start trunk conditioning (replacing data on RSDn/MRSD with the data stored in the data trunk conditioning registers in RPLC) automatically when Red Alarm is declared.

= 0: The trunk conditioning is not activated automatically when Red Alarm is declared in the Alarm Detector block.

= 1: The trunk conditioning will be initiated automatically when Red Alarm is declared in the Alarm Detector block.

AUTOOOF:

This bit decides whether to start trunk conditioning (replacing data on RSDn/MRSD with the data stored in the data trunk conditioning registers in RPLC) automatically in the duration of loss of SF/ESF frame.

= 0: The trunk conditioning is not activated automatically when the INFR (b0, T1/J1-022H) is declared in the Frame Processor block.

= 1: The trunk conditioning will be activated automatically when the INFR (b0, T1/J1-022H) is declared in the Frame Processor block.

AUTOUPDATE:

This bit decides whether the PMON and PRGD registers are automatically updated once every second.

= 0: The PMON and PRGD registers are not automatically updated. They can only be updated by MCU operation.

= 1: The PMON and PRGD registers will be automatically updated once every second.

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T1 / J1 Receive Side System Interface Options (001H, 081H, 101H, 181H, 201H, 281H, 301H, 381H)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	IMODE[1]	IMODE[0]	RSCKSEL	RSCCK2M	RSCCK8M	RSFSP	ALTIFP	IMTKC
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	1	1	0	0	0	0	0	0

IMODE[1:0]:

These bits select the operation mode in the receive path.

IMODE[1:0]	Operation Mode In Receive Path
0 0	Receive Clock Master Fractional T1/J1 mode
0 1	Receive Clock Master Full T1/J1 mode
1 0	Receive Clock Slave RSCK Reference mode
1 1	Receive Clock Slave External Signaling mode

'Receive Clock Master Full T1/J1' mode means that the received entire frame (193 bits) is clocked out from the RSDn pin, and there are no gaps in the RSCKn clock pulse.

'Receive Clock Master Fractional T1/J1' mode means that RSCKn only clocks out on the selected channels, and RSCKn does not pulse during those un-selected channels. The selection of the channel is decided by the EXTRACT (b2, T1/J1-RPLC-Indirect Register-01-18 H).

When Receive Clock Slave RSCK Reference Mode is enabled, the RSCKn/RSSIGn pin will be used as RSCKn to output a 1.544 MHz jitter attenuated version of LRCKn or an 8KHz clock.

When Receive Clock Slave External Signaling mode is enabled, the RSCKn/RSSIGn pin is used as RSSIGn to output the extracted signaling data. Each channel signaling data is channel aligned with the RSDn data stream and located in lower nibble (b5b6b7b8) of the time slot.

RSCKSEL:

When Receive Clock Slave RSCK Reference Mode is enabled, this bit selects the frequency of RSCKn.

= 0: RSCKn outputs an 8 KHz timing reference that is generated by dividing the jitter attenuated version of LRCKn.

= 1: RSCKn outputs a jitter attenuated version of the 1.544MHz receive line clock (LRCK).

RSCCK2M, RSCCK8M:

These bits determine the bit rate of the received data stream on the backplane. The 2.048 Mbit/s rate can only be supported when the backplane is configured in Receive Clock Slave mode. If the Receive Multiplexed mode is desired, all the RSCCK2M & RSCCK8M in eight framers must be set the same to select the 8.192 Mbit/s backplane bit rate. When the RSCCK2M, RSCCK8M selects the 8.192 Mbit/s, the IMODE[1:0] (b7~6, T1/J1-001H) must be set to '11'.

RSCCK2M, RSCCK8M	Backplane Rate
0 0	1.544M bit/s
1 0	2.048M bit/s
0 1	8.192M bit/s
1 1	Reserved

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RSFSP, ALTIFP:

RSFSP	ALTIFP	RSFSn Indication
0	0	RSFSn asserts on each F-bit.
0	1	RSFSn asserts on every second F-bit (i.e., the F-bit of even frame if there is no channel offset).
1	0	RSFSn asserts on the first F-bit of every 12 frames (in SF format) or every 24 frames (in ESF format).
1	1	-

In Receive Multiplexed mode, regardless of the setting in the RSFSP and the ALTRSFS, MRSFS can only indicate each F-bit of SF/ESF of the selected first framer.

IMTKC:

This bit decides how to substitute the received data stream on RSDn and RSSIGn with contents in RPLC Data Trunk Conditioning Registers and RPLC Signaling Trunk Conditioning Registers. This bit affects the corresponding time slot of MRSD and MRSSIG even if the multiplexed backplane is enabled.

= 0: The data and signaling signals are substituted on a per-timeslot basis in accordance with the control bits contained in the per-timeslot Payload Control Byte registers in the RPLC.

= 1: The data on RSDn of all time slots is replaced with the data contained in the Data Trunk Conditioning registers in RPLC, and the data on RSSIGn of all time slots is replaced with the data contained in the Signaling Trunk Conditioning registers. To enable this function, the PCCE (b0, T1/J1-050H) of the RPLC must be set to logic 1.

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T1 / J1 Backplane Parity Configuration / Status (002H, 082H, 102H, 182H, 202H, 282H, 302H, 382H)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	TPTYP	TPRTYE	TSDI	TSSIGI	PTY_EXTD	Reserved	RPTYP	RPRTYE
Type	R/W	R/W	R	R	R/W		R/W	R/W
Default	0	0	X	X	0		0	0

TPTYP:

= 0: Even parity check is employed in the F-bit input from the TSDn/MTSD and TSSIGn/MTSSIG pins, which means a logic one is expected in the F-bit position when the number of ones in the previous SF/ESF is odd.

= 1: Odd parity check is employed in the F-bit input from the TSDn/MTSD and TSSIGn/MTSSIG pins, which means a logic one is expected in the F-bit position when the number of ones in the previous SF/ESF is even.

TPRTYE:

This bit is invalid in Receive Clock Master Fractional T1/J1 mode.

= 0: Disable the interrupt on the $\overline{INT}$ pin when a parity error is detected on the TSDn/MTSD pin or a parity error is detected on the TSSIGn/MTSSIG pin.

= 1: Enable the interrupt on the $\overline{INT}$ pin when a parity error is detected on the TSDn/MTSD pin or a parity error is detected on the TSSIGn/MTSSIG pin.

TSDI:

= 0: Indicate that no parity error is detected on the TSDn/MTSD pin.

= 1: Indicate that a parity error is detected on the TSDn/MTSD pin.

This bit is cleared to '0' after the bit is read.

TSSIGI:

= 0: Indicate that no parity error is detected on the TSSIGn/MTSSIG pin.

= 1: Indicate that a parity error is detected on the TSSIGn/MTSSIG pin.

This bit is cleared to '0' after the bit is read.

PTY_EXTD:

= 0: The parity is calculated over the previous SF/ESF, excluding the F-bit on the TSDn/MTSD, TSSIGn/MTSSIG, RSDn/MRSD and RSSIGn/MRSSIG pins.

= 1: The parity is calculated over the previous SF/ESF, including the F-bit on the TSDn/MTSD, TSSIGn/MTSSIG, RSDn/MRSD and RSSIGn/MRSSIG pins.

RPTYP:

This bit is invalid in Receive Clock Master Fractional T1/J1 mode and valid when the RPRTYE is '1'.

= 0: Even parity check is employed in the F-bit output on the RSDn/MRSD and RSSIGn/MRSSIG pins, which means a logic one should be replaced in the F-bit when the number of ones in the previous SF/ESF is odd.

= 1: Odd parity check is employed in the F-bit output on the RSDn/MRSD and RSSIGn/MRSSIG pins, which means a logic one should be replaced in the F-bit when the number of ones in the previous SF/ESF is even.

RPRTYE:

This bit is invalid in Receive Clock Master Fractional T1/J1 mode.

= 0: Disable the parity on the RSDn/MRSD and RSSIGn/MRSSIG pins.

= 1: Enable the parity on the RSDn/MRSD and RSSIGn/MRSSIG pins.

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T1 / J1 Receive Interface Configuration (003H, 083H, 103H, 183H, 203H, 283H, 303H, 383H)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	MRBS	MRBC	TRI[1]	TRI[0]	RSCKRISE	LRCKFALL	RSCFSFALL	RSCCKRISE
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

MRBS:

In Receive Multiplexed mode, this bit decides which bus the corresponding framer will use to output the received data.

= 0: The first multiplexed bus (MRSD[1], MRSFS[1], MRSSIG[1]) is selected.

= 1: The second multiplexed bus (MRSD[2], MRSFS[2], MRSSIG[2]) is selected.

MRBC:

This bit turns on or turn off the transmission of received data from the corresponding framer to the selected multiplexed receive bus. Users should complete the setting in the MRBS (b7, T1/J1-003H) before turn on this bit. This bit of the framers that are output to the same multiplexed bus must be set to the same value.

= 0: The corresponding framer will not output its data stream on the multiplexed bus.

= 1: The corresponding framer will output its data stream on the multiplexed bus.

TRI[1:0]:

These bits decide the output status of the RSDn/MRSD and RSSIGn/MRSSIG pins.

TRI[1:0]	Output Status on RSDn/MRSD and RSSIGn/MRSSIG
0 0	In high impedance
1 0	Reserved
0 1	Normal operation
1 1	Reserved

In the Receive Multiplexed Mode, these bits of the framers that are output to the same multiplexed bus must be set to the same value.

RSCKRISE:

This bit selects the active edge of RSCKn to update the data on the corresponding RSDn and RSFSn.This bit is valid in Receive Clock Master mode.

= 0: The falling edge is selected.

= 1: The rising edge is selected.

LRCKFALL:

This bit selects the active edge of LRCKn to sample the data on the corresponding LRDn.

= 0: The rising edge is selected.

= 1: The falling edge is selected.

RSCFSFALL:

This bit selects the active edge of RSCCK/MRSCCK to sample the data on the corresponding RSCFS/MRSCFS. This bit is valid in Receive Clock Slave mode and Receive Multiplexed mode.

= 0: The rising edge is selected.

= 1: The falling edge is selected.

This bit in all eight framers must be set to the same value.

RSCCKRISE:

This bit selects the active edge of RSCCK/MRSCCK to update the data on the corresponding RSDn/MRSD, RSSIGn/MRSSIG and RSFSn/MRSFS. This bit is valid in Receive Clock Slave mode and Receive Multiplexed mode.

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= 0: The falling edge is selected.
= 1: The rising edge is selected.
In Receive Multiplexed mode, the RSCCKRISE of the eight framers must be set to the same value.

T1 / J1 Transmit Interface Configuration (004H, 084H, 104H, 184H, 204H, 284H, 304H, 384H)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	FIFOBYP	TAISEN	Reserved		TSCCKBFALL	TSFSRISE	TSDFALL	LTCKRISE
Type	R/W	R/W			R/W	R/W	R/W	R/W
Default	0	0			0	0	0	

FIFOBYP:
This bit decides whether the transmit data should pass through or bypass the Transmit Jitter Attenuation FIFO. The bit is valid in Clock Slave mode.
= 0: The data to be transmitted passes through the TJAT FIFO.
= 1: The TJAT FIFO is bypassed. The delay is reduced by typically 24 bits.

TAISEN:
This bit enables the line interface to generate an un-framed all-'One's Alarm Indication Signal on the TLDn pin or the corresponding framer on MTLD.
= 0: Normal operation.
= 1: TLDn or the corresponding framer on MTLD transmits all 'One's.

TSCCKBFALL:
This bit selects the active edge of TSCCKB/MTSCCKB to sample the data on the corresponding TSDn/MTSD, TSSIGn/MTSSIG and TSCFS/MTSCFS. This bit is valid in Transmit Clock Slave mode and Transmit Multiplexed mode.
= 0: The rising edge is selected.
= 1: The falling edge is selected.
The TSCCKBFALL of the eight framers should be set to the same value.

TSFSRISE:
This bit is valid in Transmit Clock Slave TSFS Enabled mode and Transmit Clock Master mode.
= 0: In Transmit Clock Slave TSFS Enabled mode, the signal on the TSFSn pin is updated on the falling edge of TSCCKB. In Transmit Clock Master mode, the signal on the TSFSn pin is updated on the falling edge of LTCKn.
= 1: In Transmit Clock Slave TSFS Enabled mode, the signal on the TSFSn pin is updated on the rising edge of TSCCKB. In Transmit Clock Master mode, the signal on the TSFSn pin is updated on the rising edge of LTCKn.

TSDFALL:
This bit selects the active edge of LTCKn to sample the data on the corresponding TSDn in Transmit Clock Master mode.
= 0: The TSDn is sampled on the rising edge of LTCKn.
= 1: The TSDn is sampled on the falling edge of LTCKn.

LTCKRISE:
This bit selects the active edge of LTCKn to update the data on the corresponding LTDn.
= 0: The falling edge is selected.
= 1: The rising edge is selected.

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T1 / J1 Transmit Side System Interface Options (005H, 085H, 105H, 185H, 205H, 285H, 305H, 385H)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	EMODE[1]	EMODE[0]	FPINV	ABXXEN	RATE[1]	RATE[0]	TSCFSP	Reserved
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Default	1	1	0	0	0	0	0	

EMODE[1:0]:

EMODE[1:0]	Operation Mode In Transmitter Path
0 0	Reserved
0 1	Transmit Clock Master mode
1 0	Transmit Clock Slave TSFS Enable mode
1 1	Transmit Clock Slave External Signaling mode

In Transmit Multiplexed mode, these bits must be set to '11'.

FPINV:

= 0: The positive pulse on the TSCFS/MTSCFS pin is valid.

= 1: The negative pulse on the TSCFS/MTSCFS pin is valid.

This bit of the eight framers should be set to the same value.

ABXXEN:

This bit is valid only in T1 ESF mode.

= 0: The valid signaling on the TSSIGn/MTSSIG pin is in the lower four nibble of each channel (i.e. XXXXABCD).

= 1: The valid signaling on the TSSIGn/MTSSIG pin is in the upper two-bit positions of the lower nibble of each channel (i.e. XXXXABXX). Thus, the 'A' bit will be inserted to the signaling bit of Frame 6 and 18, and the 'B' bit will be inserted to the signaling bit of Frame 12 and 24.

RATE[1:0]:

These bits determine the bit rate of the transmit data stream on the backplane. Note that if any of the eight framers selects the 8.192 Mbit/s backplane bit rate, the multiplexed bus will be enabled for the chip. When the RATE[1:0] selects the 2.048 Mbit/s or 8.192 Mbit/s, the EMODE[1] (b7, T1/J1-005H) must be set to '1' (i.e., in Transmit Clock Slave mode).

RATE[1:0]	Backplane Rate
0 0	1.544M bit/s
0 1	2.048M bit/s
1 0	Reserved
1 1	8.192M bit/s

TSCFSP:

= 0: Indicate that the signal on the TSCFS pin asserts on each F-bit.

= 1: Indicate that the signal on the TSCFS pin asserts on the first F-bit of every 12 SFs or every 24 ESFs.

This bit of the eight framers should be set to the same value.

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T1 / J1 Transmit Framing and Bypass Options (006H, 086H, 106H, 186H, 206H, 286H, 306H, 386H)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	FRESH	Reserved	SIGAEN	Reserved	FDIS	FBITBYP	CRCBYP	FDLBYP
Type	R/W		R/W		R/W	R/W	R/W	R/W
Default	0		0		0	0	0	0

FRESH:

= 0: Normal operation.

= 1: Initiate the FIFO in the Frame Generator block.

After initialization of the backplane interface, the user should write '1' into this bit and then clear it.

SIGAEN:

= 0: Track the signaling input from the TSSIGn/MTSSIG pin as the signaling bit.

= 1: Take a snapshot of the 1st frame input from the TSSIGn/MTSSIG pin and lock it for the signaling bit of the whole SF/ESF.

FDIS:

This bit is valid when the UF (b6, T1/J1-046H) is logic 0.

= 0: The Frame Generator is enabled to generate and insert the framing bits into the transmit data.

= 1: The Frame Generator is bypassed. Data on the TSDn/MTSD pin is transmitted transparently.

FBITBYP:

This bit is valid when the UF (b6, T1/J1-046H) and the FDIS (b3, T1/J1-006H) are logic 0.

= 0: The frame synchronization bits in the output data stream are generated by the Frame Generator.

= 1: The frame synchronization bits in the input data stream on the TSDn/MTSD pin will be output transparently.

CRCBYP:

This bit is valid when the UF (b6, T1/J1-046H) and the FDIS (b3, T1/J1-006H) are logic 0.

= 0: The framing bit corresponding to the CRC-6 bit position in the output data stream is generated by the Frame Generator.

= 1: The framing bit corresponding to the CRC-6 bit position in the input data stream on the TSDn/MTSD pin will be output transparently.

FDLBYP:

This bit is valid when the UF (b6, T1/J1-046H) and the FDIS (b3, T1/J1-006H) are logic 0.

= 0: The framing bit corresponding to the data link bit position in the output data stream is generated by the Frame Generator.

= 1: The framing bit corresponding to the data link bit position in the input data stream on the TSDn/MTSD pin will be output transparently.

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T1 / J1 Transmit Timing Options (007H, 087H, 107H, 187H, 207H, 287H, 307H, 387H)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	Reserved		TJATREF_SEL[2]	TJATREF_SEL[1]	TJATREF_SEL[0]	LTCK_SEL[2]	LTCK_SEL[1]	LTCK_SEL[0]
Type			R/W	R/W	R/W	R/W	R/W	R/W
Default			1	0	0	1	0	1

TJATREF_SEL[2:0]:

The TJATREF_SEL[2:0] select the input reference clock for the TJAT DPLL.

TJATREF_SEL[2:0]	Input Reference Clock
0 0 0	TSCCKA / 8
0 0 1	TSCCKB
0 1 0	LRCK
0 1 1	TSCCKA
1 0 0	XCK / 24
others	TSCCKB

LTCK_SEL[2:0]:

LTCK_SEL[2:0]	Line Transmit Clock
0 0 0	TSCCKA / 8
0 0 1	TSCCKB
0 1 0	LRCK
0 1 1	TSCCKA
1 0 0	XCK / 24
others	A smoothed clock output from the TJAT DPLL

T1 / J1 Interrupt Source #1 (008H, 088H, 108H, 188H, 208H, 288H, 308H, 388H)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	PMON	IBCD	FRMP	PRGD	ELSB	RHDLC#1	RBOM	ALMD
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Bits in this register indicate which function block introduced an interrupt signal on the $\overline{INT}$ pin. Reading this register does not clear the interrupt indication. To clear the interrupt indication on the $\overline{INT}$ pin, the corresponding interrupt status register must be read.

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T1 / J1 Interrupt Source #2 (009H, 089H, 109H, 189H, 209H, 289H, 309H, 389H)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	RHDLC#2	PRTY	TJAT	RJAT	THDLC#1	THDLC#2	Reserved	RCRB
Type	R/W	R/W	R/W	R/W	R/W	R/W		R/W
Default	0	0	0	0	0	0		0

Bits in this register indicate which function block introduced an interrupt signal on the $\overline{INT}$ pin.

The PRTY bit indicates a pending parity error indication needs serving in the Backplane Parity Configuration and Status registers.

Reading this register does not clear the interrupt indication. To clear the interrupt indication on the $\overline{INT}$ pin, the corresponding interrupt status register must be read.

T1 / J1 Diagnostics (00AH, 08AH, 10AH, 18AH, 20AH, 28AH, 30AH, 38AH)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	Reserved			LINELB	Reserved	DDLB	TXMFP	TXDIS
Type				R/W		R/W	R/W	R/W
Default				0		0	0	0

LINELB:

Line Loop back means that the transmit line interface data and clock (LTDn and LTCKn) are internal directly comes from the received line data and clock (LRDn and LRCKn). The loop back data stream can pass through the Receive Jitter Attenuator or bypass the Receive Jitter Attenuator (if the Receive Jitter Attenuator is configured to be bypassed)

= 0: Line loop back is disabled.

= 1: Line loop back is enabled.

DDLB:

Digital Loop back means that the received line data and clock (LRDn and LRCKn) are internal directly comes from the transmit line data and clock (LTDn and LTCKn) without the Receive Jitter Attenuator.

= 0: Digital loop back is disabled.

= 1: Digital loop back is enabled.

TXMFP:

This bit controls whether mimic pattern is generated. The mimic pattern is a copy of the F-bit. The mimic pattern is generated in the 1st bit of each channel.

= 0: Mimic pattern is not generated.

= 1: Mimic pattern is generated.

TXDIS:

= 0: Normal transmission.

= 1: Force the data to be transmitted on the TLDn pin to be all ‘Zero’s.

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T1 / J1 Revision / Chip ID / Global PMON Update (00CH)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	TYPE[2]	TYPE[1]	TYPE[0]	ID[4]	ID[3]	ID[2]	ID[1]	ID[0]
Type	R	R	R	R	R	R	R	R
Default	0	0	0	0	0	0	0	1

Writing to this register causes all Performance Monitor and PRGD Generator/Detector counters to be updated simultaneously.

TYPE[2:0]:

The TYPE[2:0] are fixed to '000', representing the IDT82V2108 chip.

ID[4:0]:

Chip revision. '00H' is for the first version.

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T1 / J1 Data Link Micro Select / Framer Reset (00DH, 08DH, 10DH, 18DH, 20DH, 28DH, 30DH, 38DH)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	RHDLCSEL[1]	RHDLCSEL[0]	THDLCSEL[1]	THDLCSEL[0]	TXCISEL	Reserved		RESET
Type	R/W	R/W	R/W	R/W	R/W			R/W
Default	X	X	X	X	X			0

RHDLCSEL[1:0]:

The RHDLCSEL[1:0] select one of the two HDLC Receivers to be accessed by the microprocessor in ESF format. When RHDLC #1 is selected, the HDLC link position is fixed in the DL of F-bit. When RHDLC #2 is selected, the microprocessor will access the HDLC #2 controller to assign the link to any one of 24 channels. These bits must be set before using the HDLC controller.

RHDLCSEL[1:0]	HDLC Receiver
0 0	RHDLC #1
0 1	RHDLC #2
1 0	Reserved
1 1	

THDLCSEL[1:0]:

The THDLCSEL[1:0] select which one of the two HDLC Transmitters to be accessed by the microprocessor in ESF format. When THDLC #1 is selected, the HDLC link position is fixed in the DL of F-bit. When THDLC #2 is selected, the microprocessor will access the HDLC #2 controller to assign the link to any one of 24 channels. These bits must be set before using the HDLC controller.

THDLCSEL[1:0]	HDLC Transmitter
0 0	THDLC #1
0 1	THDLC #2
1 0	Reserved
1 1	

TXCISEL:

The registers addressed from T1/J1-070H to T1/J1-071H are shared by the HDLC Receiver and HDLC Transmitter to decide the position of the extracted bit in the received data stream and the inserted bit in the transmitting data stream respectively. This bit is used to decide whether the Read/Write operation on the registers addressed from T1/J1-070H to T1/J1-071H is for the HDLC receiver or for the HDLC transmitter.

= 0: The Read/Write operation on registers addressed from T1/J1-070H to T1/J1-071H is for HDLC receiver.

= 1: The Read/Write operation on registers addressed from T1/J1-070H to T1/J1-071H is for the HDLC transmitter.

RESET:

This bit implements a software reset for individual framer.

= 0: Normal operation.

= 1: The corresponding framer is held in reset. However, this bit and the bits in this register can not be reset. Therefore, a logic 0 must be written to bring the framer out of reset. Holding the framer in a reset state effectively puts it into a low power standby mode. A hardware reset clears the RESET bit and the bits in this register.

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T1 / J1 Interrupt ID (00EH)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	INT[8]	INT[7]	INT[6]	INT[5]	INT[4]	INT[3]	INT[2]	INT[1]
Type	R	R	R	R	R	R	R	R
Default	0	0	0	0	0	0	0	0

This register indicates which one of the eight framers introduced the interrupt $\overline{INT}$ pin to logic low. When any one of the eight framers introduced the interrupt, the corresponding bit in the INT[8:1] will be high.

T1 / J1 Pattern Generator / Detector Positioning / Control (00FH)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	PRGDSEL[2]	PRGDSEL[1]	PRGDSEL[0]	Nx56k_GEN	Nx56k_DET	RXPATGEN	UNF_GEN	UNF_DET
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

The IDT82V2108 has only one Pattern Generator/Detector (PRGD) shared by all eight framers. At one time, only one framer can use this PRGD. This register selects which framer will use the PRGD and how the PRGD will be used.

PRGDSEL[2:0]:

The PRGDSEL[2:0] select one of the eight framers to be tested by the PRGD block.

PRGDSEL[2:0]	Tested Framer
0 0 0	Framer 1
0 0 1	Framer 2
0 1 0	Framer 3
0 1 1	Framer 4
1 0 0	Framer 5
1 0 1	Framer 6
1 1 0	Framer 7
1 1 1	Framer 8

Nx56k_GEN:

This bit is invalid when the UNF_GEN (b1, T1/J1-00FH) is logic 1.

= 0: Eight bits are all replaced with the PRGD pattern when one channel is selected by the TPLC or RPLC.

= 1: The 7 most significant bits are replaced with the PRGD pattern when one channel is selected by the TPLC or RPLC.

Nx56k_DET:

This bit is invalid when the UNF_DEL (b0, T1/J1-00FH) is logic 1.

= 0: Eight bits are all detected by the PRGD when one channel is selected by the TPLC or RPLC.

= 1: The 7 most significant bits are detected by the PRGD when one channel is selected by the TPLC or RPLC.

RXPATGEN:

= 0: The pattern in PRGD is generated in the transmit path and is detected in the receive path.

= 1: The pattern in PRGD is generated in the receive path and is detected in the transmit path.

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UNF_GEN:

= 0: Which channels of the selected path will be replaced by the PRGD pattern is specified by TPLC or RPLC.

= 1: All 24 channels and the F-bit of the selected path will be replaced by the PRGD pattern.

UNF_DET:

= 0: Which channels of the selected path will be detected by PRGD pattern is specified by TPLC or RPLC.

= 1: All 24 channels and the F-bit of the selected path will be detected by PRGD pattern.

T1 / J1 RJAT Interrupt Status (010H, 090H, 110H, 190H, 210H, 290H, 310H, 390H)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	Reserved						OVRI	UNDI
Type							R	R
Default							X	X

OVRI:

If data is still attempted to write into the FIFO when the FIFO is already full, the overwritten event will occur.

= 0: The RJAT FIFO is not overwritten.

= 1: The RJAT FIFO is overwritten.

This bit is cleared to ‘0’ when it is read.

UNDI:

If data is still attempted to read from the FIFO when the FIFO is already empty, the under-run event will occur.

= 0: The RJAT FIFO is not under-run.

= 1: The RJAT FIFO is under-run.

This bit is cleared to ‘0’ when it is read.

T1 / J1 RJAT Reference Clock Divisor (N1) Control (011H, 091H, 111H, 191H, 211H, 291H, 311H, 391H)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	N1[7]	N1[6]	N1[5]	N1[4]	N1[3]	N1[2]	N1[1]	N1[0]
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	1	0	1	1	1	1

These bits define a binary number. The (N1[7:0] + 1) is the divisor of the input reference clock, which is the ratio between the frequency of the input reference clock and the frequency applied to the phase discriminator input.

Writing to this register will reset the DPLL in the RJAT.

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T1 / J1 RJAT Output Clock Divisor (N2) Control (012H, 092H, 112H, 192H, 212H, 292H, 312H, 392H)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	N2[7]	N2[6]	N2[5]	N2[4]	N2[3]	N2[2]	N2[1]	N2[0]
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	1	0	1	1	1	1

These bits define a binary number. The (N2[7:0] + 1) is the divisor of the output smoothed clock, which is the ratio between the frequency of the output smoothed clock and the frequency applied to the phase discriminator input.

Writing to this register will reset the DPLL in the RJAT.

T1 / J1 RJAT Configuration (013H, 093H, 113H, 193H, 213H, 293H, 313H, 393H)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	Reserved			CENT	UNDE	OVRE	Reserved	LIMIT
Type				R/W	R/W	R/W		R/W
Default				0	0	0		1

CENT:

The CENT allows the RJAT FIFO to self-center its read pointer, maintaining the pointer at least 4 UI away from the FIFO being empty or full.

= 0: Disable the self-center. Data passes through uncorrupted when the FIFO is empty or full.

= 1: Enable the FIFO to self-center its read pointer when the FIFO is 4 UI away from being empty or full.

A positive transition in this bit will execute a self-center action immediately.

UNDE:

This bit decides whether to generate an interrupt when the RJAT FIFO is under-run.

= 0: No interrupt is generated when the RJAT FIFO is under-run.

= 1: An interrupt on the $\overline{INT}$ pin is generated when the RJAT FIFO is under-run.

OVRE:

This bit decides whether to generate an interrupt when the RJAT FIFO is overwritten.

= 0: No interrupt is generated when the RJAT FIFO is overwritten.

= 1: An interrupt on the INT pin is generated when the RJAT FIFO is overwritten.

LIMIT:

= 0: Disable the limitation of the jitter attenuation.

= 1: Enable the DPLL to limit the jitter attenuation by enabling the FIFO to increase or decrease the frequency of the output smoothed clock when the read pointer is 1 UI away from the FIFO being empty or full. This limitation of jitter attenuation ensures that no data is lost during high phase shift conditions.

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T1 / J1 TRSI Time Slot Offset (014H, 094H, 114H, 194H, 214H, 294H, 314H, 394H)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	Reserved	TSOFF[6]	TSOFF[5]	TSOFF[4]	TSOFF[3]	TSOFF[2]	TSOFF[1]	TSOFF[0]
Type		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0

In T1/J1 Transmit Clock Slave External Signaling mode E1 rate, the content in the TSOFF[6:0] determines the channel offset between the signal on the TSCFS pin and the start of the corresponding frame transmitted on TSDn & TSSIGn.

In T1/J1 Transmit Clock Slave TSFS Enabled mode E1 rate, the content in the TSOFF[6:0] determine the channel offset between the signal on the TSCFS pin and the start of the corresponding frame transmitted on TSDn.

In Transmit Multiplexed mode, the content in the TSOFF[6:0] determine the channel offset between the signal on the MTSCFS pin and the start of the corresponding frame transmitted on MTSD.

Except for the above three modes, the channel offset is disabled. Thus, the TSOFF[6:0] must be logic 0.

These bits define a binary number. The offset can be set from 0 to 127 channels.

T1 / J1 TRSI Bit Offset (015H, 095H, 115H, 195H, 215H, 295H, 315H, 395H)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	Reserved	MTBS	CMS	COFF	Reserved	BOFF[2]	BOFF[1]	BOFF[0]
Type		R/W	R/W	R/W		R/W	R/W	R/W
Default		0	0	0		0	0	0

MTBS:

Valid in Transmit Multiplexed mode.

= 0: Data of the current channel is taken from the first multiplexed bus (MTSD[1], MTSSIG[1]).

= 1: Data of the current channel is taken from the second multiplexed bus (MTSD[2], MTSSIG[2]).

CMS:

= 0: The clock rate of TSCCKB/MTSCCKB is the same as that of the backplane.

= 1: The clock rate of TSCCKB/MTSCCKB is double that of the backplane.

The CMS of the eight framers should be set to the same value.

COFF:

Valid when the CMS (b5, T1/J1-015H) is logic 1.

= 0: The first active edge of TSCCKB/MTSCCKB is used to sample / update the data.

= 1: The second active edge of TSCCKB/MTSCCKB is used to sample / update the data.

In Transmit Clock Multiplexed mode, the COFF of the eight framers should be set to the same value.

BOFF[2:0]:

In T1/J1 Transmit Clock Slave External Signaling mode E1 rate, the content in the BOFF[2:0] determines the bit offset between the signal on the TSCFS pin and the start of the SF/ESF transmitted on TSDn & TSSIGn.

In T1/J1 Transmit Clock Slave TSFS Enabled mode E1 rate, the content in the BOFF[2:0] determines the bit offset between the signal on the TSCFS pin and the start of the SF/ESF transmitted on TSDn.

In Transmit Multiplexed mode, the content in the BOFF[2:0] determines the bit offset between the signal on the MTSCFS pin and the start of the SF/ESF transmitted on MTSD & MTSSIG.

Except for the above three modes, the bit offset is disabled. Thus, the BOFF[2:0] must be logic 0.

These bits define a binary number. Refer to the Functional Description for details.

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T1 / J1 TJAT Interrupt Status (018H, 098H, 118H, 198H, 218H, 298H, 318H, 398H)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	Reserved						OVRI	UNDI
Type							R	R
Default							X	X

OVRI:

If data is still attempted to write into the FIFO when the FIFO is already full, the overwritten event will occur.

= 0: The TJAT FIFO is not overwritten.

= 1: The TJAT FIFO is overwritten.

This bit is cleared to '0' when it is read.

UNDI:

If data is still attempted to read from the FIFO when the FIFO is already empty, the under-run event will occur.

= 0: The TJAT FIFO is not under-run.

= 1: The TJAT FIFO is under-run.

This bit is cleared to '0' when it is read.

T1 / J1 TJAT Reference Clock Divisor (N1) Control (019H, 099H, 119H, 199H, 219H, 299H, 319H, 399H)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	N1[7]	N1[6]	N1[5]	N1[4]	N1[3]	N1[2]	N1[1]	N1[0]
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	1	0	1	1	1	1

These bits define a binary number. The (N1[7:0] + 1) is the divisor of the input reference clock, which is the ratio between the frequency of the input reference clock and the frequency applied to the phase discriminator input.

Writing to this register will reset the DPLL in the TJAT.

T1 / J1 TJAT Output Clock Divisor (N2) Control (01AH, 09AH, 11AH, 19AH, 21AH, 29AH, 31AH, 39AH)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	N2[7]	N2[6]	N2[5]	N2[4]	N2[3]	N2[2]	N2[1]	N2[0]
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	1	0	1	1	1	1

These bits define a binary number. The (N2[7:0] + 1) is the divisor of the output smoothed clock, which is the ratio between the frequency of the output smoothed clock and the frequency applied to the phase discriminator input.

Writing to this register will reset the DPLL in the TJAT.

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T1 / J1 TJAT Configuration (01BH, 09BH, 11BH, 19BH, 21BH, 29BH, 31BH, 39BH)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	Reserved			CENT	UNDE	OVRE	Reserved	LIMIT
Type				R/W	R/W	R/W		R/W
Default				0	0	0		1

CENT:

The CENT allows the TJAT FIFO to self-center its read pointer, maintaining the pointer at least 4 UI away from the FIFO being empty or full.

= 0: Disable the self-center. Data passes through uncorrupted when the FIFO is empty or full.

= 1: Enable the FIFO to self-center its read pointer when the FIFO is 4 UI away from being empty or full.

A positive transition in this bit will execute a self-center action immediately.

UNDE:

This bit decides whether to generate an interrupt when the TJAT FIFO is under-run.

= 0: No interrupt is generated when the TJAT FIFO is under-run.

= 1: An interrupt on the $\overline{INT}$ pin is generated when the TJAT FIFO is under-run.

OVRE:

This bit decides whether to generate an interrupt when the TJAT FIFO is overwritten.

= 0: No interrupt is generated when the TJAT FIFO is overwritten.

= 1: An interrupt on the INT pin is generated when the TJAT FIFO is overwritten.

LIMIT:

= 0: Disable the limitation of the jitter attenuation.

= 1: Enable the DPLL to limit the jitter attenuation by enabling the FIFO to increase or decrease the frequency of the output smoothed clock when the read pointer is 1 UI away from the FIFO being empty or full. This limitation of jitter attenuation ensures that no data is lost during high phase shift conditions.

T1 / J1 ELSB Interrupt Enable / Status (01DH, 09DH, 11DH, 19DH, 21DH, 29DH, 31DH, 39DH)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	Reserved					SLIPE	SLIPD	SLIPI
Type						R/W	R	R
Default						0	X	X

SLIPE:

= 0: Disable the interrupt on the $\overline{INT}$ pin when a slip occurs.

= 1: Enable the interrupt on the $\overline{INT}$ pin when a slip occurs.

SLIPD:

This bit is valid when the SLIPI is logic 1.

= 0: The latest slip is due to the Elastic Store Buffer being empty; a frame was duplicated.

= 1: The latest slip is due to the Elastic Store Buffer being full; a frame was deleted.

SLIPI:

= 0: No slip occurs.

= 1: A slip occurs.

This bit is cleared to '0' after the bit is read.

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T1 / J1 ELSB Idle Code (01EH, 09EH, 11EH, 19EH, 21EH, 29EH, 31EH, 39EH)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	D7	D6	D5	D4	D3	D2	D1	D0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	1	1	1	1	1	1	1	1

These bits set the idle code that will replace the data on RSDn/MRSD automatically when it is out of SF/ESF synchronization. D7 is the first bit to be inserted.

The writing of the idle code pattern is asynchronous with respect to the output data clock. One channel of idle code data will be corrupted if the register is written to when the framer is out of frame.

T1 / J1 FRMP Configuration (020H, 0A0H, 120H, 1A0H, 220H, 2A0H, 320H, 3A0H)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	M2O[1]	M20[0]	ESFFA	ESF	JYEL	Reserved		
Type	R/W	R/W	R/W	R/W	R/W			
Default	0	0	0	0	0			

M20[1:0]:

These bits select the SF/ESF frame loss criteria.

= 00: 2 of 4 frame alignment bits in error.

= 01: 2 of 5 frame alignment bits in error.

= 10: 2 of 6 frame alignment bits in error.

= 11: Reserved

ESFFA:

This bit selects the framing algorithm for ESF format.

= 0: If four consecutive Frame Alignment Patterns are detected in the F-Bit in the received data stream without the mimic framing pattern, the ESF synchronization is acquired. However, if there are mimic framing patterns in the received data stream, the ESF In-frame is not declared.

= 1: When 6 consecutive Frame Alignment Patterns are received error free and the CRC-6 checksum is also error free, the synchronization is acquired. In this condition, the existence of the mimic framing patterns is not considered.

ESF:

This bit selects the SF or ESF format in the Frame Processor block.

= 0: SF format is selected.

= 1: ESF format is selected.

JYEL:

This bit selects the T1 or J1 mode in the Frame Processor block.

= 0: T1 mode is selected.

= 1: J1 mode is selected.

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T1 / J1 FRMP Interrupt Enable (021H, 0A1H, 121H, 1A1H, 221H, 2A1H, 321H, 3A1H)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	Reserved		COFAE	FERE	BEEE	SFEE	MFPE	INFRE
Type			R/W	R/W	R/W	R/W	R/W	R/W
Default			0	0	0	0	0	0

COFAE:

When the frame alignment pattern has been achieved and the position of the new frame alignment pattern differs from the previous one, this bit decides whether to generate an interrupt or not.

= 0: Disable the interrupt when there is a shift on the framing signal position.

= 1: Enable the interrupt on the $\overline{INT}$ pin when there is a shift on the framing signal position.

FERE:

= 0: No interrupt is generated when there is a framing bit error.

= 1: An interrupt on the $\overline{INT}$ pin is generated when a framing bit error is detected.

BEEE:

= 0: No interrupt is generated when there is a bit error event.

= 1: An interrupt on the $\overline{INT}$ pin is generated when a bit error event occurs. Here, the bit error event is defined as a framing bit error for SF formatted data and a CRC-6 error (the local calculated CRC-6 result is not the same as the received CRC-6 bits) for ESF formatted data.

(In SF mode, this bit has the same function as the FERE.)

SFEE:

The Severe Framing Error is defined as 2 or more framing bit errors during the current super-frame of SF or ESF data.

= 0: No interrupt is generated when there is a Severe Framing Error.

= 1: An interrupt on the $\overline{INT}$ pin is generated when Severe Framing Error event occurs.

MFPE:

Mimic Framing Pattern is defined as more than one framing alignment pattern existing simultaneously in the receiving data stream. This bit decides whether to generate an interrupt when Mimic Framing Pattern appears or disappears.

= 0: No interrupt is generated when there is a transition of the status of Mimic Framing Pattern.

= 1: An interrupt on the $\overline{INT}$ pin is generated when there is a transition (exist to non-exist, or non-exist to exist) of the status of Mimic Framing Pattern.

INFRE:

This bit decides whether to generate an interrupt when the status of incoming data stream changes from in-frame to out-of-frame or from out-of-frame to in-frame.

= 0: No interrupt is generated when there is a transition of Frame Synchronization Status.

= 1: An interrupt on the $\overline{INT}$ pin is generated when there is a transition of Framing Synchronization Status.

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T1 / J1 FRMP Interrupt Status (022H, 0A2H, 122H, 1A2H, 222H, 2A2H, 322H, 3A2H)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	COFAI	FERI	BEEI	SFEI	MFPI	INFRI	MFP	INFR
Type	R	R	R	R	R	R	R	R
Default	0	0	0	0	0	0	0	0

COFAI:

= 0: Indicates the framing signal position shift has not occurred.

= 1: Indicates the occurrence of framing signal position shift, which means when the frame alignment pattern has been achieved, the position of the new alignment pattern differs from the previous one.

This bit is cleared to '0' after it is read.

FERI:

= 0: Indicates that there is no framing bit error.

= 1: Indicates the occurrence of a framing bit error.

This bit is cleared to '0' after it is read.

BEEI:

This bit indicates the occurrence of a bit error event. The bit error event is defined as a framing bit error for SF format or a CRC-6 error (the local calculated CRC-6 result is not the same as the received CRC-6 bits) for ESF format.

= 0: Indicates there is no bit error.

= 1: Indicates the occurrence of a bit error.

(For SF formatted data, this bit has the same function as FERI bit.)

This bit is cleared to '0' after it is read.

SFEI:

The Severe Framing Error is defined as 2 or more framing bit errors during the current super-frame of SF or ESF data.

= 0: Indicates there is no severe framing error.

= 1: Indicates the occurrence of severe framing error.

This bit is cleared to '0' after it is read.

MFPI:

This bit indicates the transition of the status of the current mimic framing pattern.

= 0: When the status of current mimic framing pattern is not changed.

= 1: When there is a transition (exist to non-exist, or non-exist to exist) of the status of mimic framing pattern.

This bit is cleared to '0' after it is read.

INFRI:

This bit indicates the transition of frame synchronization status.

= 0: When the frame synchronization status is not changed.

= 1: When the frame synchronization status of the receiving data stream changes from in-frame to out-of-frame or from out-of-frame to in-frame.

MFP:

This bit reflects the current status of mimic framing pattern.

= 0: Indicates that the mimic framing pattern does not exist.

= 1: Indicates the presence of more than one framing alignment patterns in the receiving data stream.

Read operation will not change the status of this bit.

INFR:

This bit reflects the current status of frame synchronization.

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= 0: The received data stream is out-of-frame.
= 1: The received data stream is in-frame.
Read operation will not change the status of this bit.

T1 / J1 Clock Monitor (027H, 0A7H, 127H, 1A7H, 227H, 2A7H, 327H, 3A7H)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	Reserved			XCK	TSCCKB	TSCCKA	RSCCK	LRCK
Type				R	R	R	R	R
Default				X	X	X	X	X

This register provides monitoring on the IDT82V2108 clocks. When a monitored clock signal makes a low to high transition, the corresponding bit in this register is set to '1', and this bit remains to be '1' until this register is read. After a read operation on this register, all the bits in this register will be cleared to '0'. A lack of transitions of the monitored clock will be indicated by '0' in the corresponding bit, which means that the clock fails. This register should be read periodically to detect clock failures.

XCK:
= 0: After the bit is read.
= 1: A low to high transition occurs on XCK.

TSCCKB:
= 0: After the bit is read.
= 1: A low to high transition occurs on TSCCKB.

TSCCKA:
= 0: After the bit is read.
= 1: A low to high transition occurs on TSCCKA.

RSCCK:
= 0: After the bit is read.
= 1: A low to high transition occurs on RSCCK.

LRCK:
= 0: After the bit is read.
= 1: A low to high transition occurs on LRCK.

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T1 / J1 RBOM Enable (02AH, 0AAH, 12AH, 1AAH, 22AH, 2AAH, 32AH, 3AAH)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	Reserved					IDLE	AVC	BOCE
Type						R/W	R/W	R/W
Default						0	0	0

IDLE:

= 0: Disable the interrupt on the $\overline{INT}$ pin when there is a transition from BOM to non-BOM in the received data stream.

= 1: Enable the interrupt on the $\overline{INT}$ pin when there is a transition from BOM to non-BOM in the received data stream.

AVC:

This bit selects the validation criteria used to acknowledge the Bit Oriented Message (BOM) in the received data stream, or to acknowledge the Yellow signal in T1/J1 ESF format.

= 0: The BOM or the Yellow signal is acknowledged when the pattern is matched and the received code is identical 8 out of 10 times.

= 1: The BOM or the Yellow signal is acknowledged when the pattern is matched and the received code is identical 4 out of 5 times.

BOCE:

= 0: Disable the interrupt on the $\overline{INT}$ pin when a valid BOM code is detected in the received data stream.

= 1: Enable the interrupt on the $\overline{INT}$ pin when a valid BOM code is detected in the received data stream.

T1 / J1 RBOM Code Status (02BH, 0ABH, 12BH, 1ABH, 22BH, 2ABH, 32BH, 3ABH)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	IDLEI	BOCI	BOC[5]	BOC[4]	BOC[3]	BOC[2]	BOC[1]	BOC[0]
Type	R	R	R	R	R	R	R	R
Default	0	0	1	1	1	1	1	1

IDLEI:

= 0: No transition from Bit Oriented Message (BOM) to non-BOM in the received data stream.

= 1: A transition from BOM to non-BOM in the received data stream.

This bit is cleared to '0' after the register is read.

BOCI:

= 0: No Bit Oriented Message (BOM) is detected.

= 1: BOM is detected in the received data stream.

This bit is cleared to '0' after the register is read.

BOC[5:0]:

These bits directly reflect the content of the Bit Oriented Message (BOM) in the received data stream.

All 'One's in the BOC[5:0] mean there is no BOM received.

The BOC[5] corresponds to the MSB of the code while the BOC[0] corresponds to the LSB.

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T1 / J1 ALMD Configuration (02CH, 0ACH, 12CH, 1ACH, 22CH, 2ACH, 32CH, 3ACH)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	Reserved		J1_YEL	ESF	Reserved			
Type			R/W	R/W				
Default			0	0				

J1_YEL:

This bit selects the T1 or J1 mode in the Alarm Detector block.

= 0: T1 mode is selected in the ALMD block.

= 1: J1 mode is selected in the ALMD block.

ESF:

This bit selects the SF or ESF format in the Alarm Detector block.

= 0: SF format is selected.

= 1: ESF format is selected.

T1 / J1 ALMD Interrupt Enable (02DH, 0ADH, 12DH, 1ADH, 22DH, 2ADH, 32DH, 3ADH)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	Reserved			FASTD	Reserved	YELE	REDE	AISE
Type				R/W		R/W	R/W	R/W
Default				0		0	0	0

FASTD:

= 0: RED Alarm is cleared when the out of SF/ESF synchronization event has been absent for 16.6 sec (±500 ms); AIS Alarm is cleared when the AIS signal has been absent for 16.8 sec (±500 ms).

= 1: RED Alarm is cleared when the out of SF/ESF synchronization event has been absent for 120 ms; AIS Alarm is cleared when the AIS signal has been absent for 180 ms.

YELE:

= 0: Disable the interrupt on the $\overline{INT}$ pin when the YELI (b5, T1/J1-02EH) is logic one.

= 1: Enable the interrupt on the $\overline{INT}$ pin when the YELI (b5, T1/J1-02EH) is logic one.

REDE:

= 0: Disable the interrupt on the $\overline{INT}$ pin when the REDI (b4, T1/J1-02EH) is logic one.

= 1: Enable the interrupt on the $\overline{INT}$ pin when the REDI (b4, T1/J1-02EH) is logic one.

AISE:

= 0: Disable the interrupt on the $\overline{INT}$ pin when the AISI (b3, T1/J1-02EH) is logic one.

= 1: Enable the interrupt on the $\overline{INT}$ pin when the AISI (b3, T1/J1-02EH) is logic one.

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T1 / J1 ALMD Interrupt Status (02EH, 0AEH, 12EH, 1AEH, 22EH, 2AEH, 32EH, 3AEH)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	Reserved		YELI	REDI	AISI	YEL	RED	AIS
Type			R	R	R	R	R	R
Default			0	0	0	0	0	0

YELI:

= 0: There is no transition (from '1' to '0' or from '0' to '1') on the YEL (b2, T1/J1-02EH).
= 1: There is a transition (from '1' to '0' or from '0' to '1') on the YEL (b2, T1/J1-02EH).
This bit is clear to '0' after the register is read.

REDI:

= 0: There is no transition (from '1' to '0' or from '0' to '1') on the RED (b1, T1/J1-02EH).
= 1: There is a transition (from '1' to '0' or from '0' to '1') on the RED (b1, T1/J1-02EH).
This bit is clear to '0' after the register is read.

AISI:

= 0: There is no transition (from '1' to '0' or from '0' to '1') on the AIS (b0, T1/J1-02EH).
= 1: There is a transition (from '1' to '0' or from '0' to '1') on the AIS (b0, T1/J1-02EH).
This bit is clear to '0' after the register is read.

YEL:

= 0: Yellow signal has been absent for 425 ms (±50 ms).
= 1: Yellow signal has been present for 425 ms (±50 ms).

RED:

= 0: The REDD (b2, T1/J1-02FH) has been logic 0 for 16.6 sec (±500 ms), or for 120 ms if the FASTD (b4, T1/J1-02DH) is set.
= 1: The REDD (b2, T1/J1-02FH) has been logic 1 for 2.55 sec (±40 ms).

AIS:

= 0: AIS signal has been absent for 16.8 sec (±500 ms), or for 180 ms if the FASTD (b4, T1/J1-02DH) is set.
= 1: AIS signal has been present for 1.5 sec (±100 ms).

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T1 / J1 ALMD Alarm Detection Status (02FH, 0AFH, 12FH, 1AFH, 22FH, 2AFH, 32FH, 3AFH)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	Reserved					REDD	YELD	AISD
Type						R	R	R
Default						X	X	X

REDD:

= 0: No out of SF/ESF synchronization event has occurred in the latest 40 ms period.

= 1: One or more out of SF/ESF synchronization events have occurred in the latest 40 ms period.

YELD:

= 0: In SF format, the Yellow signal is absent during the latest 40 ms period; in ESF format, the Yellow signal is absent during the latest 4 ms period.

= 1: In SF format, the Yellow signal is present during the latest 40 ms period; in ESF format, when the AVC (b1, T1/J1-02AH) is '0', the Yellow signal is present during the latest 40 ms period, when the AVC (b1, T1/J1-02AH) is '1', the Yellow signal is present during the latest 20 ms period.

The Yellow signal is acknowledged differently in each format:

- In T1 SF format: The Yellow signal occupies the 2nd bit of each channel. When the bit is logic 1 for 16 or fewer times during the 40 ms period, the Yellow signal is present.

- In J1 SF format: The Yellow signal occupies the F-bit of the 12th frame. However, when the bit is logic 0 for 2 or fewer times during the 40 ms period, the Yellow signal is present.

- In T1/J1 ESF format: The Yellow signal occupies the DL of the F-bit (refer to Table-4). The pattern is ëFF00í in T1 mode and 'FFFF' in J1 mode. When the AVC (b1, T1/J1-02AH) is logic 0, the Yellow signal is acknowledged if the pattern is matched in 8 out of 10 successive DL. When the AVC (b1, T1/J1-02AH) is logic 1, the Yellow signal is acknowledged if the pattern is matched in 4 out of 5 successive DL.

AISD:

= 0: AIS signal is absent during the latest 60 ms period.

= 1: AIS signal is present during the latest 60 ms period.

The AIS signal is acknowledged when the received data is out of SF/ESF synchronization for 60 ms and the received logic 0 is less than 127 times in the same period.

T1 / J1 TPLC Configuration (030H, 0B0H, 130H, 1B0H, 230H, 2B0H, 330H, 3B0H)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	Reserved							PCCE
Type								R/W
Default								0

PCCE:

= 0: The per-channel functions in TPLC are disabled.

= 1: The per-channel functions in TPLC are enabled.

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T1 / J1 TPLC µP Access Status (031H, 0B1H, 131H, 1B1H, 231H, 2B1H, 331H, 3B1H)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	BUSY	Reserved						
Type	R							
Default	0							

BUSY:

= 0: No reading or writing operation on the indirect registers.

= 1: An internal indirect register is being accessed, any new operation on the internal indirect register is not allowed.

This bit goes low timed to an internal high-speed clock rising edge after the operation has been completed. The operation cycle is 650 ns. No more operations to the indirect registers could be done until this bit is cleared.

T1 / J1 TPLC Channel Indirect Address / Control (032H, 0B2H, 132H, 1B2H, 232H, 2B2H, 332H, 3B2H)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	R/WB	A6	A5	A4	A3	A2	A1	A0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Writing to this register with a valid address and Read/Write command initiates an internal operation cycle to the indirect registers.

R/WB:

= 0: Write the data to the specified indirect register.

= 1: Read the data from the specified indirect register.

A[6:0]:

Specify the address of the indirect registers (from 01H to 48H) for the microprocessor access.

T1 / J1 TPLC Channel Indirect Data Buffer (033H, 0B3H, 133H, 1B3H, 233H, 2B3H, 333H, 3B3H)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	D7	D6	D5	D4	D3	D2	D1	D0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

This register holds the value which will be read from or write into the indirect registers (from 01H to 48H). If data is to be written to the indirect registers, the byte to be written must be written into this register before the target indirect register address and R/WB = 0 is written into the Address/Control register, initiating the access. If data is to be read from the indirect registers, only the target indirect register address and R/WB = 1 is written into the Address/Control register, initiating the request. After 490 ns, this register will contain the requested data byte.

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TPLC Indirect Registers Map	
01H ~ 18H	Per-Channel Control for Channel 1 ~ 24
19H ~ 30H	IDLE Code Byte for Channel 1 ~ 24
31H ~ 48H	Signaling Control Byte for Channel 1 ~ 24

T1 / J1 TPLC Per-Channel Control Registers (TPLC Indirect Registers 01H ~ 18H)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	INVERT	IDLE_DS0	DMW	SIGNINV	TEST	LOOP	ZCS[1]	ZCS[0]
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	X	X	X	X	X	X	X	X

INVERT:

This bit, together with the SIGNINV (b4, T1/J1-TPLC-indirect register - 01~18H), determines the bit inversion of the corresponding channel when input from the TSDn/MTSD pin.

INVERT	SIGNINV	Bit Inversion
0	0	No bit inversion
0	1	Invert the MSB of the corresponding channel
1	0	Invert all the bits of the corresponding channel
1	1	Invert all the bits except the MSB of the corresponding channel

IDLE_DS0:

= 0: Disable the data in the corresponding channel to be replaced by the data set in the IDLE[7:0] when input from the TSDn/MTSD pin.

= 1: Enable the data in the corresponding channel to be replaced by the data set in the IDLE[7:0] when input from the TSDn/MTSD pin.

DMW:

= 0: Disable the data in the corresponding channel to be replaced with a digital milliwatt pattern when input from the TSDn/MTSD pin.

= 1: Enable the data in the corresponding channel to be replaced with a digital milliwatt pattern when input from the TSDn/MTSD pin.

SIGNINV:

Refer to the INVERT (b7, T1/J1-TPLC-indirect register - 01~18H).

TEST:

= 0: Disable the data in the corresponding channel to be tested by PRGD.

= 1: Enable the data in the corresponding channel to be extracted to PRGD for test (when the RXPATGEN [b2, T1/J1-00FH] is logic 1), or enable the test pattern from PRGD to replace the data in the corresponding channel for test (when the RXPATGEN [b2, T1/J1-00FH] is logic 0).

All the time slots that are extracted to the PRGD are concatenated and treated as a continuous stream in which pseudo random is searched for. Similarly, all time slots set to be replaced with PRGD test pattern data are concatenated replaced by the PRBS.

LOOP:

= 0: Disable the payload loopback.

= 1: Enable the payload loopback. When Receive Clock Master modes are enabled, the Elastic Store is used to align the receive line data to the data to be transmitted. When Receive Clock Slave modes are enabled, the Elastic Store is unavailable to facilitate the payload loopbacks, and loop-back functionality is provided only when the transmit path is also in Transmit Clock Slave mode, and the received clock and the clock to be transmitted and Common Frame Pulse are identical (RSCCK = TSCCKB, RSCFS = TSCFS).

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ZCS[1:0]:

ZCS[1:0]	Per-Channel Zero Code Suppression
0 0	No zero code suppression.
0 1	Every bit 8 in the corresponding channel is forced to be logic one.
1 0	GTE Zero Code Suppression - Every bit 8 (or bit 7 in signaling frames) is forced to be logic one when the bits in the corresponding channel are all 'Zero's.
1 1	Bell Zero Code Suppression - Every bit 7 is forced to be logic one when the bits in the corresponding channel are all 'Zero's.

The priority of the TPLC operation on the TSDn/MTSD pin from high to low is:

Extract data to PRGD for test; Zero Code Suppression; Payload loopback; Replace the data with the milliwatt pattern; Replace the data with the pattern generated in the PRGD; Replace the data with the value in the IDLE[7:0]; Invert the bit.

T1 / J1 TPLC IDLE Code Byte Registers (TPLC Indirect Registers 19H ~ 30H)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	IDLE7	IDLE6	IDLE5	IDLE4	IDLE3	IDLE2	IDLE1	IDLE0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	X	X	X	X	X	X	X	X

They contain the data that will replace the data input from the TSDn/MTSD pin when the corresponding IDLE_DS0 is logic 1. IDLE7 is the MSB.

T1 / J1 TPLC Signaling Control Byte Registers (TPLC Indirect Registers 31H ~ 48H)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	SIGC0	SIGC1	Reserved		A	B	C	D
Type	R/W	R/W			R/W	R/W	R/W	R/W
Default	X	X			X	X	X	X

SIGC0:

This bit is valid when the corresponding SIGC1 is logic 1.

= 0: Use the data input from the TSSIGn/MTSSIG pin as the signaling.

= 1: Use the data in the A, B, C, D as the signaling.

SIGC1:

= 0: Disable replacing the signaling bit with the data input from the TSSIGn/MTSSIG pin or the data in the A, B, C, D.

= 1: Enable replacing the signaling bit with the data input from the TSSIGn/MTSSIG pin or the data in the A, B, C, D.

A, B, C, D:

They contain the data that can be used as signaling when the corresponding SIGC0 is logic 1. They are in the least significant nibble.

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T1 / J1 THDLC #1, #2 Configuration (034H, 0B4H, 134H, 1B4H, 234H, 2B4H, 334H, 3B4H)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	FLGSHARE	FIFOCLR	Reserved		EOM	ABT	CRC	EN
Type	R/W	R/W			R/W	R/W	R/W	R/W
Default	1	0			0	0	1	0

Selection of the THDLC block (#1 or #2) whose registers are visible on the microprocessor interface is done via the THDLCSEL[1:0] (b5~4, T1/J1-00DH).

FLGSHARE:

= 0: The closing flag of the current HDLC and the opening flag of the next HDLC are separate.

= 1: The closing flag of the current HDLC and the opening flag of the next HDLC are shared.

FIFOCLR:

= 0: Normal operation.

= 1: Clear the FIFO.

EOM:

= 0: Normal operation.

= 1: A positive transition of this bit starts a packet transmission. Then if the CRC(b1, E1-050H) is set, the 16-bit FCS word is appended to the last data byte transmitted.

ABT:

= 0: Normal operation.

= 1: Transmit the 7F abort sequence after the current setting in the Transmit Data register is transmitted, so that the FIFO is cleared and all data in the FIFO will be lost.

Aborts are continuously sent and the FIFO is held in reset until this bit is reset to a logic 0. At least one abort sequence will be sent when the ABT transitions from logic 0 to logic 1.

CRC:

= 0: Do not append the CRC-16 frame check sequences (FCS) to the end of the HDLC data.

= 1: Append the FCS to the end of the HDLC data.

EN:

= 0: Disable the operation of the THDLC block and transmit all ‘One’s on the assigned data link.

= 1: Enable the operation of the THDLC block and flag sequences are sent until data is written into the THDLC Transmit Data register and the EOM is set to logic 1.

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T1 / J1 THDLC #1, #2 Upper Transmit Threshold (035H, 0B5H, 135H, 1B5H, 235H, 2B5H, 335H, 3B5H)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	Reserved	UTHR[6]	UTHR[5]	UTHR[4]	UTHR[3]	UTHR[2]	UTHR[1]	UTHR[0]
Type		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		1	0	0	0	0	0	0

Selection of the THDLC block (#1 or #2) whose registers are visible on the microprocessor interface is done via the THDLCSEL[1:0] (b5~4, T1/J1-00DH).

UTHR[6:0]:

These bits define the upper fill level of the FIFO. Once the fill level exceeds the UTHR[6:0] value, the data stored in the FIFO will start to transmit. The transmission will not stop until the last complete packet is transmitted and the THDLC FIFO fill level is below 'UTHR[6:0] + 1'.

It should be greater than the value of the LINT[6:0] unless both are equal to 00H.

T1 / J1 THDLC #1, #2 Lower Interrupt Threshold (036H, 0B6H, 136H, 1B6H, 236H, 2B6H, 336H, 3B6H)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	Reserved	LINT[6]	LINT[5]	LINT[4]	LINT[3]	LINT[2]	LINT[1]	LINT[0]
Type		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	1	1	1

Selection of the THDLC block (#1 or #2) whose registers are visible on the microprocessor interface is done via the THDLCSEL[1:0] (b5~4, T1/J1-00DH).

LINT[6:0]:

These bits define the fill level of the FIFO that can introduce an interrupt. That is, when the fill level of the FIFO is below the LINT[6:0], an interrupt will be generated. It should be less than the value of the UTHR[6:0] unless both are equal to 00H.

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T1 / J1 THDLC #1, #2 Interrupt Enable (037H, 0B7H, 137H, 1B7H, 237H, 2B7H, 337H, 3B7H)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	Reserved				FULLE	OVRE	UDRE	LFILLE
Type					R/W	R/W	R/W	R/W
Default					0	0	0	0

Selection of the THDLC block (#1 or #2) whose registers are visible on the microprocessor interface is done via the THDLCSEL[1:0] (b5~4, T1/J1-00DH).

FULLE:
= 0: Disable the interrupt on the $\overline{INT}$ pin when the FULLI (b3, T1/J1-038H) is logic 1.
= 1: Enable the interrupt on the $\overline{INT}$ pin when the FULLI (b3, T1/J1-038H) is logic 1.

OVRE:
= 0: Disable the interrupt on the $\overline{INT}$ pin when the OVRI (b2, T1/J1-038H) is logic 1.
= 1: Enable the interrupt on the $\overline{INT}$ pin when the OVRI (b2, T1/J1-038H) is logic 1.

UDRE:
= 0: Disable the interrupt on the $\overline{INT}$ pin when the UDRI (b1, T1/J1-038H) is logic 1.
= 1: Enable the interrupt on the $\overline{INT}$ pin when the UDRI (b1, T1/J1-038H) is logic 1.

LFILLE:
= 0: Disable the interrupt on the $\overline{INT}$ pin when the LFILLI (b0, T1/J1-038H) is logic 1.
= 1: Enable the interrupt on the $\overline{INT}$ pin when the LFILLI (b0, T1/J1-038H) is logic 1.

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T1 / J1 THDLC #1, #2 Interrupt Status / UDR Clear (038H, 0B8H, 138H, 1B8H, 238H, 2B8H, 338H, 3B8H)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	Reserved	FULL	BLFILL	Reserved	FULLI	OVRI	UDRI	LFILLI
Type		R	R		R	R	R	R
Default		X	X		X	X	X	X

Selection of the THDLC block (#1 or #2) whose registers are visible on the microprocessor interface is done via the THDLCSEL[1:0] (b5~4, T1/J1-00DH).

FULL:
= 0: The THDLC FIFO is not full.
= 1: The THDLC FIFO is full (128 bits).

BLFILL:
= 0: The data in the THDLC FIFO is not below the value of the LINT[6:0] (b6~0, T1/J1-036H).
= 1: The data in the THDLC FIFO is empty or below the value of the LINT[6:0] (b6~0, T1/J1-036H).

FULLI:
= 0: There is no transition (from '0' to '1') on the FULL.
= 1: There is a transition (from '0' to '1') on the FULL.
This bit is clear to '0' after the bit is read.

OVRI:
The Over-Written is that the THDLC FIFO was already full when another data byte was written to the THDLC Transmit Data register.
= 0: The THDLC FIFO is not overwritten.
= 1: The THDLC FIFO is overwritten (more than 128 bits).
This bit is clear to '0' after the bit is read.

UDRI:
The Under-Run is that the THDLC was in the process of transmitting a packet when it ran out of data to be transmitted.
= 0: The THDLC FIFO is not under-run.
= 1: The THDLC FIFO is under-run.
This bit is clear to '0' after the bit is read.

LFILLI:
= 0: There is no transition (from '0' to '1') on the BLFILL.
= 1: There is a transition (from '0' to '1') on the BLFILL.
This bit is clear to '0' after the bit is read.

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T1 / J1 THDLC #1, #2 Transmit Data (039H, 0B9H, 139H, 1B9H, 239H, 2B9H, 339H, 3B9H)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	TD[7]	TD[6]	TD[5]	TD[4]	TD[3]	TD[2]	TD[1]	TD[0]
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	X	X	X	X	X	X	X	X

Selection of the THDLC block (#1 or #2) whose registers are visible on the microprocessor interface is done via the THDLCSEL[1:0] (b5~4, T1/J1-00DH).

The content is the data to be transmitted. It is serially transmitted (TD[0] is the first).

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T1 / J1 IBCD Configuration (03CH, 0BCH, 13CH, 1BCH, 23CH, 2BCH, 33CH, 3BCH)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	Reserved		IBCD_ERR[1]	IBCD_ERR[0]	DSEL1	DSEL0	ASEL1	ASEL0
Type			R/W	R/W	R/W	R/W	R/W	R/W
Default			0	0	0	0	0	0

IBCD_ERR[1:0]:

The IBCD_ERR[1:0] set the error tolerance in the received activate/deactivate code within 39.8 ms:

IBCD_ERR[1:0]	Error Tolerance
0 0	0 bit
0 1	200 bits
1 0	20 bits
1 1	2 bits

DSEL[1:0]:

The DSEL[1:0] define the length of the received loopback deactivate code, meanwhile, it define the valid code in the DACT[7:0] (b7~0, T1/J1-03FH):

DSEL[1:0]	Deactivate Code Length & Valid Code In the DACT[7:0]
0 0	5-bit length & the code in the DACT[7:3] is valid
0 1	6-bit or 3-bit length & the code in the DACT[7:2] is valid
1 0	7-bit length & the code in the DACT[7:1] is valid
1 1	8-bit or 4-bit length & the code in the DACT[7:0] is valid

ASEL[1:0]:

The ASEL[1:0] define the length of the received loopback activate code, meanwhile, it define the valid code in the ACT[7:0] (b7~0, T1/J1-03EH):

ASEL[1:0]	Activate Code Length & Valid Code In the ACT[7:0]
0 0	5-bit length & the code in the ACT[7:3] is valid
0 1	6-bit or 3-bit length & the code in the ACT[7:2] is valid
1 0	7-bit length & the code in the ACT[7:1] is valid
1 1	8-bit or 4-bit length & the code in the ACT[7:0] is valid

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T1 / J1 IBCD Interrupt Enable / Status (03DH, 0BDH, 13DH, 1BDH, 23DH, 2BDH, 33DH, 3BDH)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	LBACP	LBDCP	LBAE	LBDE	LBAI	LBDI	LBA	LBD
Type	R	R	R/W	R/W	R	R	R	R
Default	0	0	0	0	0	0	0	0

LBACP:
= 0: No loopback activate code is present for 39.8 ms.
= 1: The loopback activate code is present for 39.8 ms.

LBDCP:
= 0: No loopback deactivate code is present for 39.8 ms.
= 1: The loopback deactivate code is present for 39.8 ms.

LBAE:
= 0: Disable the interrupt on the $\overline{INT}$ pin when the loopback activate code status changes (i.e., the LBAI is logic one).
= 1: Enable the interrupt on the $\overline{INT}$ pin when the loopback activate code status changes (i.e., the LBAI is logic one).

LBDE:
= 0: Disable the interrupt on the $\overline{INT}$ pin when the loopback deactivate code status changes (i.e., the LBDI is logic one).
= 1: Enable the interrupt on the $\overline{INT}$ pin when the loopback deactivate code status changes (i.e., the LBDI is logic one).

LBAI:
= 0: The loopback activate code status does not change.
= 1: The loopback activate code status changes (i.e., there is a transition from ‘0’ to ‘1’ or from ‘1’ to ‘0’ on the LBA).
This bit is cleared to ‘0’ after the register is read.

LBDI:
= 0: The loopback deactivate code status does not change.
= 1: The loopback deactivate code status changes (i.e., there is a transition from ‘0’ to ‘1’ or from ‘1’ to ‘0’ on the LBD).
This bit is cleared to ‘0’ after the register is read.

LBA:
= 0: No loopback activate code is present for 5.1 s.
= 1: The loopback activate code is present for 5.1 s.

LBD:
= 0: No loopback deactivate code is present for 5.1 s.
= 1: The loopback deactivate code is present for 5.1 s.

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T1 / J1 IBCD Activate Code (03EH, 0BEH, 13EH, 1BEH, 23EH, 2BEH, 33EH, 3BEH)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	ACT7	ACT6	ACT5	ACT4	ACT3	ACT2	ACT1	ACT0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

The ACT[7:X] define the content of the activate code. 'X' is 3, 2, 1 or 0 and depends on the length defined by the ASEL[1:0] (b1~0, T1/J1-03CH). The unused bits should be ignored. The ACT[7] is the MSB and compares with the first received code bit.

T1 / J1 IBCD Deactivate Code (03FH, 0BFH, 13FH, 1BFH, 23FH, 2BFH, 33FH, 3BFH)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	DACT7	DACT6	ADCT5	DACT4	DACT3	DACT2	DACT1	DACT0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

The DACT[7:X] define the content of the deactivate code. 'X' is 3, 2, 1 or 0 and depends on the length defined by the DSEL[1:0] (b3~2, T1/J1-03CH). The unused bits should be ignored. The DACT[7] is the MSB and compares with the first received code bit.

T1 / J1 RCRB Configuration (COSS = 0) (040H, 0C0H, 140H, 1C0H, 240H, 2C0H, 340H, 3C0H)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	Reserved	COSS	SIGE	Reserved		ESF	Reserved	PCCE
Type		R/W	R/W			R/W		R/W
Default		0	0			0		0

COSS:

= 0: Allow the RCRB registers to access the indirect registers.

= 1: Allow the RCRB registers to reflect the change of the signaling of its corresponding channel.

SIGE:

= 0: Disable generation of an interrupt on the $\overline{INT}$ pin when there is signaling change in any one of the 24 channels.

= 1: Enable generation of an interrupt on the $\overline{INT}$ pin when there is signaling change in any one of the 24 channels.

ESF:

This bit selects the SF or ESF format in the Receive CAS/RBS Buffer block.

= 0: SF format is selected.

= 1: ESF format is selected.

PCCE:

= 0: The per-channel functions in RCRB are disabled.

= 1: The per-channel functions in RCRB are enabled.

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T1 / J1 RCRB Channel Indirect Status (COSS = 0) (041H, 0C1H, 141H, 1C1H, 241H, 2C1H, 341H, 3C1H)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	BUSY	Reserved						
Type	R							
Default	0							

BUSY:

= 0: No reading or writing operation on the indirect registers is occurring.

= 1: An internal indirect register is being accessed. Any new operation on the internal indirect register is not allowed.

This bit goes low timed to an internal high-speed clock rising edge after the operation has been completed. The operation cycle is 650 ns. No more operations to the indirect registers could be done until this bit is cleared.

T1 / J1 RCRB Channel Indirect Address / Control (COSS = 0) (042H, 0C2H, 142H, 1C2H, 242H, 2C2H, 342H, 3C2H)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	R/WB	A6	A5	A4	A3	A2	A1	A0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

R/WB:

= 0: Write the data to the specified indirect register.

= 1: Read the data from the specified indirect register.

A[6:0]:

Specifies the address of the indirect registers (from 20H to 57H) for the microprocessor access.

T1 / J1 RCRB Channel Indirect Data Buffer (COSS = 0) (043H, 0C3H, 143H, 1C3H, 243H, 2C3H, 343H, 3C3H)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	D7	D6	D5	D4	D3	D2	D1	D0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	X	X	X	X	X	X	X	X

This register holds the value which will be read from or written to the indirect registers (from 20H to 57H). If data is to be written to the indirect registers, the byte to be written must be written into this register before the target indirect register address and R/WB = 0 is written into the Address/Control register, initiating the access. If data is to be read from the indirect registers, only the target indirect register address and R/WB = 1 is written into the Address/Control register, initiating the request. After 640 ns, this register will contain the requested data byte.

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T1 / J1 RCRB Configuration (COSS = 1) (040H, 0C0H, 140H, 1C0H, 240H, 2C0H, 340H, 3C0H)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	Reserved	COSS	Reserved					
Type		R/W						
Default		0						

COSS:

= 0: Allow the RCRB registers to access the indirect registers.

= 1: Allow the RCRB registers to reflect the change of the signaling of its corresponding channel.

T1 / J1 RCRB Signaling State Change Channels 17-24 (COSS = 1) (041H, 0C1H, 141H, 1C1H, 241H, 2C1H, 341H, 3C1H)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	COSS[24]	COSS[23]	COSS[22]	COSS[21]	COSS[20]	COSS[19]	COSS[18]	COSS[17]
Type	R	R	R	R	R	R	R	R
Default	X	X	X	X	X	X	X	X

COSSn:

= 0: The signaling in its corresponding channel is not changed.

= 1: The signaling in its corresponding channel is changed.

These bits are cleared to '0' after the register is read. COSS[24:17] correspond to channels 24 to 17.

T1 / J1 RCRB Signaling State Change Channels 9-16 (COSS = 1) (042H, 0C2H, 142H, 1C2H, 242H, 2C2H, 342H, 3C2H)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	COSS[16]	COSS[15]	COSS[14]	COSS[13]	COSS[12]	COSS[11]	COSS[10]	COSS[9]
Type	R	R	R	R	R	R	R	R
Default	X	X	X	X	X	X	X	X

COSSn:

= 0: The signaling in its corresponding channel is not changed.

= 1: The signaling in its corresponding channel is changed.

These bits are cleared to '0' after the register is read. COSS[16:9] correspond to channels 16 to 9.

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T1 / J1 RCRB Signaling State Change Channels 1-8 (COSS = 1) (043H, 0C3H, 143H, 1C3H, 243H, 2C3H, 343H, 3C3H)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	COSS[8]	COSS[7]	COSS[6]	COSS[5]	COSS[4]	COSS[3]	COSS[2]	COSS[1]
Type	R	R	R	R	R	R	R	R
Default	X	X	X	X	X	X	X	X

COSSn:

= 0: The signaling in its corresponding channel is not changed.

= 1: The signaling in its corresponding channel is changed.

These bits are cleared to '0' after the register is read. COSS[8:1] correspond to channels 8 to 1.

RCRB Indirect Registers Map	
01H ~ 18H / 21H ~ 38H	Channel Signaling Data Register for Channel 1 ~ 24
19H ~ 20H, 39H ~ 40H	-
41H ~ 58H	Per-Channel Configuration Register for Channel 1 ~ 24

T1 / J1 RCRB Channel Signaling Data Registers (COSS = 0) (RCRB Indirect Registers 01H ~ 18H / 21H ~ 38H)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	Reserved				A	B	C	D
Type					R	R	R	R
Default					X	X	X	X

A, B, C, D:

They contain the signaling of the corresponding channel.

There is a maximum 2 ms delay between the transition of the COSS[n] bit (T1/J1-041H & T1/J1-042H & T1/J1-043H) and the updating of the A, B, C, D code in the corresponding indirect registers 21H ~ 38H. To avoid this 2 ms delay, users can read the corresponding b3~0 in the indirect registers 01H ~ 18H first. If the value of these four bits are different from the previous A, B, C, D code, then the content of b3~0 in the 01H ~ 18H is the updated A, B, C, D code. If the content of the four bits is the same as the previous A, B, C, D code, then users should read the b3~0 in the 21H ~ 38H to get the updated A, B, C, D code.

In SF format, the C and D are the repetition of the A and B respectively.

T1 / J1 RCRB Per-Channel Configuration Registers (COSS = 0) (RCRB Indirect Registers 41H ~ 58H)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	Reserved							DEB
Type								R/W
Default								X

DEB:

= 0: Disable signaling debounce.

= 1: Enable signaling debounce (valid only if the PCCE is logic 1). That is, the signaling is acknowledged only when 2 consecutive signaling bits of a channel are the same.

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T1 / J1 FRMG Configuration (044H, 0C4H, 144H, 1C4H, 244H, 2C4H, 344H, 3C4H)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	MTRK	J1_CRC	J1_YEL	ESF	Reserved		GZCS[1]	GZCS[0]
Type	R/W	R/W	R/W	R/W			R/W	R/W
Default	0	0	0	0			0	0

MTRK:

Valid when the PCCE (b0, T1/J1-030H) is logic 1.

= 0: Normal operation.

= 1: Replace the data on all channels with the data set in the IDLE[7:0] (b7~0, T1/J1-TPLC-indirect registers-19~30H); replace the signaling on all channels with the data on the TSSIGn/MTSSIG pin or the data in the A, B, C, D (b3~0, T1/J1-TPLC-indirect registers-31~48H) according to the setting in the SIGC[1:0] (b7~6, T1/J1-TPLC-indirect registers-31~48H).

J1_CRC:

This bit selects the T1 or J1 CRC-6 algorithm when the ESF (b4, T1/J1-044H) is '1'.

= 0: The CRC-6 algorithm meets T1 standard.

= 1: The CRC-6 algorithm meets J1 standard.

J1_YEL:

This bit selects the T1 or J1 Yellow alarm pattern to be transmitted.

= 0: The Yellow alarm transition meets T1 standard.

= 1: The Yellow alarm transition meets J1 standard.

The Yellow alarm pattern is:

- In T1 SF format: Transmit logic 0 on the 2nd bit of each channel.
- In T1 ESF format: Transmit 'FF00' on each FDL link.
- In J1 SF format: Transmit logic 1 on the 12th F-bit.
- In J1 ESF format: Transmit 'FFFF' on each FDL link.

The SF or ESF format is selected by the ESF (b4, T1/J1-044H).

ESF:

This bit selects the SF or ESF format in the Frame Generator block.

= 0: The SF format is selected.

= 1: The ESF format is selected.

GZCS[1:0]:

These bits select the Zero Code Suppression format to be used. They are logically ORed with the ZCS[1:0] (b1~0, T1/J1-TPLC-indirect registers-01~18H).

GZCS[1:0]	Zero Code Suppression
0 0	No zero code suppression.
0 1	GTE Zero Code Suppression - Every bit 8 (or bit 7 in signaling frames) is forced to be logic one when the bits in a channel are all 'Zero's.
1 0	Reserved.
1 1	Bell Zero Code Suppression - Every bit 7 is forced to be logic one when the bits in a channel are all 'Zero's.

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T1 / J1 FRMG Alarm Transmit (045H, 0C5H, 145H, 1C5H, 245H, 2C5H, 345H, 3C5H)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	Reserved						XYEL	Reserved
Type							R/W	
Default							0	

XYEL:

= 0: Disable generating Yellow alarm manually.

= 1: Enable generating Yellow alarm manually.

T1 / J1 IBCG Control (046H, 0C6H, 146H, 1C6H, 246H, 2C6H, 346H, 3C6H)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	EN	UF	Reserved				CL1	CL0
Type	R/W	R/W					R/W	R/W
Default	0	0					0	0

EN:

= 0: Disable transmitting the inband loopback code.

= 1: Enable transmitting the inband loopback code.

UF:

= 0: The Frame Generator block operates normally. It transmits the inband loopback code in framed mode, that is, only the 192 bits are replaced with the inband loopback while the F-bit is occupied by Frame Alignment Pattern, DL or CRC-6.

= 1: Disable the Frame Generator block, that is, disable to form the SF/ESF frame. It transmits the inband loopback code in un-framed mode, that is, all 193 bits are replaced with the inband loopback code.

CL[1:0]:

The CL[1:0] define the length of the loopback code to be transmitted, meanwhile, they define the valid code in the IBC[7:0] (b7~0, T1/J1-047H):

CL[1:0]	Loopback Code Length & valid code in the IBC[7:0]
0 0	5-bit length & the code in the IBC[7:3] is valid
0 1	6-bit or 3-bit length & the code in the IBC[7:2] is valid
1 0	7-bit length & the code in the IBC[7:1] is valid
1 1	8-bit or 4-bit length & the code in the IBC[7:0] is valid

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T1 / J1 IBCG Loopback Code (047H, 0C7H, 147H, 1C7H, 247H, 2C7H, 347H, 3C7H)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	IBC7	IBC6	IBC5	IBC4	IBC3	IBC2	IBC1	IBC0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	X	X	X	X	X	X	X	X

The IBC[7:X] define the content of the inband loopback code. 'X' is one of 3 to 0 which is depending on the length defined by the CL[1:0] (b1~0, T1/J1-046H). The IBC[7] is the MSB.

T1 / J1 PMON Interrupt Enable / Status (049H, 0C9H, 149H, 1C9H, 249H, 2C9H, 349H, 3C9H)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	Reserved					INTE	XFER	OVR
Type						R/W	R	R
Default						0	0	0

INTE:

= 0: Disabled the interrupt on the $\overline{INT}$ pin when the counter data has been transferred into the Error Count registers.

= 1: Enabled the interrupt on the $\overline{INT}$ pin when the counter data has been transferred into the Error Count registers.

XFER:

= 0: Indicate that the counter data has not been transferred to the Error Count registers.

= 1: Indicate that the counter data has been transferred to the Error Count registers.

This bit is clear to '0' after the bit is read.

OVR:

= 0: Indicate that no overwritten on the Error Count registers has occurred.

= 1: Indicate that one of the Error Count registers is overwritten.

This bit is clear to '0' after the bit is read.

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Registers 04A-04FH, 0CA-0CFH, 14A-14FH, 1CA-1CFH, 24A-24FH, 2CA-2CFH, 34A-34FH, 3CA-3CFH:

The PMON Error Count registers for a single framer are updated as a group by writing to any of the PMON count registers or updated every 1 second when the AUTOUPDATE (b0, T1/J1-000H) is set. The PMON Error Count registers for eight framers are updated by writing to the Chip ID/ Global PMON Update register (T1/J1-00CH).

When the chip is reset, the contents of the PMON Error Count registers are unknown until the first latching of performance data is performed.

T1 / J1 PMON BEE Count (LSB) (04AH, 0CAH, 14AH, 1CAH, 24AH, 2CAH, 34AH, 3CAH)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	BEE7	BEE6	BEE5	BEE4	BEE3	BEE2	BEE1	BEE0
Type	R	R	R	R	R	R	R	R
Default	X	X	X	X	X	X	X	X

T1 / J1 PMON BEE Count (MSB) (04BH, 0CBH, 14BH, 1CBH, 24BH, 2CBH, 34BH, 3CBH)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	Reserved				BEE11	BEE10	BEE9	BEE8
Type					R	R	R	R
Default					X	X	X	X

In the ESF format, the BEE[11:0] represent the number of the CRC-6 errors, that is, the differences between the received CRC-6 and the local calculated CRC-6

In the SF format, the BEE[11:0] represent the number of the bit errors in the Frame Alignment Pattern.

This register is updated on the defined intervals.

T1 / J1 PMON FER Count (LSB) (04CH, 0CCH, 14CH, 1CCH, 24CH, 2CCH, 34CH, 3CCH)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	FER7	FER6	FER5	FER4	FER3	FER2	FER1	FER0
Type	R	R	R	R	R	R	R	R
Default	X	X	X	X	X	X	X	X

T1 / J1 PMON FER Count (MSB) (04DH, 0CDH, 14DH, 1CDH, 24DH, 2CDH, 34DH, 3CDH)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	Reserved							FER8
Type								R
Default								X

The FER[8:0] represent the number of the bit errors in the Frame Alignment Pattern.

This register is updated on the defined intervals.

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T1 / J1 PMON OOF Count (04EH, 0CEH, 14EH, 1CEH, 24EH, 2CEH, 34EH, 3CEH)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	Reserved			OOF4	OOF3	OOF2	OOF1	OOF0
Type				R	R	R	R	R
Default				X	X	X	X	X

The OOF[4:0] represent the number of the out of SF/ESF synchronization events and update on the defined intervals.

T1 / J1 PMON COFA Count (04FH, 0CFH, 14FH, 1CFH, 24FH, 2CFH, 34FH, 3CFH)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	Reserved					COFA2	COFA1	COFA0
Type						R	R	R
Default						X	X	X

The COFA[2:0] represent the number of the changes of the Frame Alignment Pattern position and update on the defined intervals.

T1 / J1 RPLC Configuration (050H, 0D0H, 150H, 1D0H, 250H, 2D0H, 350H, 3D0H)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	Reserved							PCCE
Type								R/W
Default								0

PCCE:

= 0: The per-channel functions in RPLC are disabled.

= 1: The per-channel functions in RPLC are enabled.

T1 / J1 RPLC µP Access Status (051H, 0D1H, 151H, 1D1H, 251H, 2D1H, 351H, 3D1H)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	BUSY	Reserved						
Type	R							
Default	0							

BUSY:

= 0: No reading or writing operation on the indirect registers.

= 1: An internal indirect register is being accessed. Any new operation on the internal indirect register is not allowed.

This bit goes low timed to an internal high-speed clock rising edge after the operation has been completed. The operation cycle is 640 ns. No more operations to the indirect registers could be done until this bit is cleared.

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T1 / J1 RPLC Channel Indirect Address / Control (052H, 0D2H, 152H, 1D2H, 252H, 2D2H, 352H, 3D2H)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	R/WB	A6	A5	A4	A3	A2	A1	A0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Writing to this register with a valid address and Read/Write command initiates an internal operation cycle to the indirect registers.

R/WB:

= 0: Write the data to the specified indirect register.

= 1: Read the data from the specified indirect register.

A[6:0]:

Specify the address of the indirect registers (from 01H to 48H) for the microprocessor access.

T1 / J1 RPLC Channel Indirect Data Buffer (053H, 0D3H, 153H, 1D3H, 253H, 2D3H, 353H, 3D3H)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	D7	D6	D5	D4	D3	D2	D1	D0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

This register holds the value which will be read from or written to the indirect registers (from 01H to 48H). If data is to be written to the indirect registers, the byte to be written must be written into this register before the target indirect register address and R/WB = 0 is written into the Address/Control register, initiating the access. If data is to be read from the indirect registers, only the target indirect register address and R/WB = 1 is written into the Address/Control register, initiating the request. After 640 ns, this register will contain the requested data byte.

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RPLC Indirect Registers Map	
01H ~ 18H	Per-Channel Configuration for Channel 1 ~ 24
19H ~ 30H	Data Trunk Conditioning Code for Channel 1 ~ 24
31H ~ 48H	Signaling Trunk Conditioning for Channel 1 ~ 24

T1 / J1 RPLC Per-Channel Configuration Registers (RPLC Indirect Registers 01H ñ 18H)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	INVERT	DTRKC	DMW	SIGNINV	TEST	EXTRACT	FIX	POL
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	X	X	X	X	X	X	X	X

INVERT:

This bit, together with the SIGNINV (b4, T1/J1-RPLC-indirect register - 01~18H), determines the bit inversion of the corresponding channel when output from the RSDn/MRSD pin.

INVERT	SIGNINV	Bit Inversion
0	0	No bit inversion
0	1	Invert the MSB of the corresponding channel
1	0	Invert all the bits of the corresponding channel
1	1	Invert all the bits except the MSB of the corresponding channel

DTRKC:

= 0: Disable the data in the corresponding channel to be replaced by the data set in the DTRK[7:0] (b7~0, T1/J1-19~30H) when output on the RSDn/MRSD pin.

= 1: Enable the data in the corresponding channel to be replaced by the data set in the DTRK[7:0] (b7~0, T1/J1-19~30H) when output on the RSDn/MRSD pin.

DMW:

= 0: Disable the data in the corresponding channel to be replaced with a digital milliwatt pattern when output on the RSDn/MRSD pin.

= 1: Enable the data in the corresponding channel to be replaced with a digital milliwatt pattern when output on the RSDn/MRSD pin.

SIGNINV:

Refer to the INVERT (b7, T1/J1-RPLC-indirect register - 01~18H)

TEST:

= 0: Disable the data in the corresponding channel to be tested by PRGD.

= 1: Enable the data in the corresponding channel to be extracted to PRGD for test (when the RXPATGEN [b2, T1/J1-00FH] is logic 0), or enable the test pattern from PRGD to replace the data in the corresponding channel for test (when the RXPATGEN [b2, T1/J1-00FH] is logic 1).

All the channels that are extracted to the PRGD are concatenated and treated as a continuous stream in which pseudo random is searched for. Similarly, all channels set to be replaced with PRGD test pattern data are concatenated replaced by the PRBS.

EXTRACT:

This bit is valid in Receive Clock Slave Fractional T1/J1 mode:

= 0: RSCKn is held in its inactivated state.

= 1: RSCKn is clocked for the corresponding channel.

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FIX:

= 0: Disable the signaling bit of the corresponding channel to be fixed with the value set by the POL when output on the RSDn/MRSD pin.

= 1: Enable the signaling bit of the corresponding channel to be fixed with the value set by the POL when output on the RSDn/MRSD pin.

POL:

Valid when the FIX is logic 1:

= 0: Fix the signaling bit of the corresponding channel to be logic 0.

= 1: Fix the signaling bit of the corresponding channel to be logic 1.

The priority of the RPLC operation of the corresponding channel on the RSDn/MRSD pin from high to low is:

Extract data to PRGD for test; Replace the data with the value in the DTRK[7:0]; Replace the data with the milliwatt pattern; Replace the data with the pattern generated in the PRGD; Invert the bits in the channel; Fix the signaling bit.

T1 / J1 RPLC Data Trunk Conditioning Code Byte Registers (RPLC Indirect Registers 19H ~ 30H)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	DTRK7	DTRK6	DTRK5	DTRK4	DTRK3	DTRK2	DTRK1	DTRK0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	X	X	X	X	X	X	X	X

These indirect registers contain the data that will replace the data output on the RSDn/MRSD pin when the corresponding DTRKC (b6, T1/J1-RPLC-indirect registers-01~18H) is logic 1. DTRK7 is the MSB.

T1 / J1 RPLC Signaling Trunk Conditioning Byte Registers (RPLC Indirect Registers 31H ~ 48H)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	STRKC	Reserved			A	B	C	D
Type	R/W				R/W	R/W	R/W	R/W
Default	X				X	X	X	X

STRKC:

= 0: Disable the signaling of the corresponding channel to be replaced by the data set in the A, B, C, D (b3~0, T1/J1-RPLC-indirect registers-31~48H) when output on the RSSIGn/MRSSIG pin.

= 1: Enable the signaling of the corresponding channel to be replaced by the data set in the A, B, C, D (b3~0, T1/J1-RPLC-indirect registers-31~48H) when output on the RSSIGn/MRSSIG pin.

A, B, C, D:

These bits contain the data that will replace the data output on the RSSIGn/MRSSIG pin when the corresponding STRKC (b7, T1/J1-RPLC-indirect registers-31~48H) is logic 1. They are in the least significant nibble.

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T1 / J1 RHDLC #1, #2 Configuration (054H, 0D4H, 154H, 1D4H, 254H, 2D4H, 354H, 3D4H)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	Reserved				MEN	MM	TR	EN
Type					R/W	R/W	R/W	R/W
Default					0	0	0	0

Selection of the RHDLC block (#1 or #2) whose registers are visible on the microprocessor interface is done via the RHDLCSEL[1:0] (b7~6, T1/J1-00DH).

MEN, MM:

The MEN & MM define the address matching mode:

MEN	MM	Address Matching Mode
0	X	No address matching is needed. All the HDLC data is stored in the FIFO.
1	0	The HDLC data is stored in the FIFO when the first byte is all 'One's or the same as the setting in the PA[7:0] (b7~0, T1/J1- 058H) or the SA[7:0] (b7~0, T1/J1-059H).
1	1	The HDLC data is stored in the FIFO when the most significant 6 bits in the first byte are all 'One's or the same as the setting in the PA[7:2] (b7~2, T1/J1-058H) or the SA[7:2] (b7~2, T1/J1-059H).

TR:

= 0: Normal operation.

= 1: Force the RHDLC to immediately terminate the reception of the current data frame, empty the FIFO buffer, clear the interrupts and initiate a new HDLC searching.

This bit is clear to '0' after a rising and falling edge occur on the internal clock or after the register is read.

EN:

= 0: Disabled the operation of the RHDLC block and all the FIFO buffer and interrupts are cleared.

= 1: Enabled the operation of the RHDLC block and the HDLC opening flag will be searched immediately.

If the EN is set from logic 1 to logic 0 and back to logic 1, the RHDLC will immediately terminate the reception of the current data frame, empty the FIFO buffer, clear the interrupts and initiate a new HDLC searching.

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T1 / J1 RHDLC #1, #2 Interrupt Control (055H, 0D5H, 155H, 1D5H, 255H, 2D5H, 355H, 3D5H)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	INTE	INTC[6]	INTC[5]	INTC[4]	INTC[3]	INTC[2]	INTC[1]	INTC[0]
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Selection of the RHDLC block (#1 or #2) whose registers are visible on the microprocessor interface is done via the RHDLCSEL[1:0] (b7~6, T1/J1-00DH).

INTE:

= 0: Disable the interrupt on the $\overline{INT}$ pin when there is a transition from '0' to '1' on the INTR (b0, T1/J1-056H).

= 1: Enable the interrupt on the $\overline{INT}$ pin when there is a transition from '0' to '1' on the INTR (b0, T1/J1-056H).

INTC[6:0]:

These bits set the interrupt set point of the FIFO buffer. Exceeding the set point will introduce an interrupt, and the interrupt will persist until the FIFO is empty. The set point is decimal 128 when the INTC[6:0] is all 'Zero's.

The contents of this register should only be changed when the EN (b0, T1/J1-054H) is logic 0. This prevents any erroneous interrupt generation.

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T1 / J1 RHDLC #1, #2 Status (056H, 0D6H, 156H, 1D6H, 256H, 2D6H, 356H, 3D6H)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	FE	OVR	COLS	PKIN	PBS[2]	PBS[1]	PBS[0]	INTR
Type	R	R	R	R	R	R	R	R
Default	X	X	X	X	X	X	X	X

Selection of the RHDLC block (#1 or #2) whose registers are visible on the microprocessor interface is done via the RHDLCSEL[1:0] (b7~6, T1/J1-00DH).

FE:

= 0: The FIFO is loaded with data.

= 1: The FIFO is empty.

OVR:

The overwritten condition occurs when data is written over unread data in the FIFO buffer. This bit is cleared to '0' after the register is read.

= 0: No overwritten occurs.

= 1: The FIFO is overwritten, and then the FIFO is reset, which introduce the COLS and PKIN to be reset to logic 0.

COLS:

This bit reflects the HDLC link status change.

= 0: Normal operation.

= 1: The first HDLC opening flag sequence (7E) activated the HDLC or the HDLC abort sequence (7F) deactivated the HDLC is detected.

This bit is cleared to '0' after the bit is read, or after the OVR transitions to logic 1, or after the EN is cleared.

PKIN:

= 0: The last byte of a non-aborted packet is not written into the FIFO.

= 1: The last byte of a non-aborted packet is written into the FIFO.

This bit is cleared to '0' after the bit is read, or after the OVR transitions to logic 1.

PBS[2:0]:

The PBS[2:0] indicate the status of the last byte read from the FIFO.

PBS[2:0]	Status of the Data
0 0 0	Normal data
0 0 1	A dummy byte to indicate the first HDLC opening flag sequence (7E) was detected, which means the HDLC link became active.
0 1 0	A dummy byte to indicate the HDLC abort sequence (7F) was detected, which means the HDLC link became inactive.
0 1 1	Reserved
1 0 0	The last byte of a non-aborted HDLC packet was received. The HDLC packet is in an integer number of bytes and has no FCS error
1 0 1	The last byte of a non-aborted HDLC packet was received and a non-integer number of bytes is in the packet.
1 1 0	The last byte of a non-aborted HDLC packet was received. The HDLC packet is in an integer number of bytes and has FCS error.
1 1 1	The last byte of a non-aborted HDLC packet was received. The HDLC packet is in a non-integer number of bytes and has FCS error.

INTR:

= 0: No interrupt sources in the HDLC Receiver block occurred.

= 1: Any one of the interrupt sources in the HDLC Receiver block occurred. The interrupt sources in the HDLC Receiver are: 1. Receiving the first 7E opening flag sequence which activates the HDLC link; 2. A packet was received; 3. Change of link status; 4. Exceeding the set point of the FIFO which is defined in the INTC[6:0] (b6~0, T1/J1-055H); 5. Over-writing the FIFO.

This bit is cleared to '0' after the bit is read.

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T1 / J1 RHDLC #1, #2 Data (057H, 0D7H, 157H, 1D7H, 257H, 2D7H, 357H, 3D7H)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	RD[7]	RD[6]	RD[5]	RD[4]	RD[3]	RD[2]	RD[1]	RD[0]
Type	R	R	R	R	R	R	R	R
Default	X	X	X	X	X	X	X	X

Selection of the RHDLC block (#1 or #2) whose registers are visible on the microprocessor interface is done via the RHDLCSEL[1:0] (b7~6, T1/J1-00DH).

RD[7:0]:

These bits represent the bytes read from the FIFO. These bits should not be accessed at a rate greater than 1/15 of the XCK rate.

The RD[0] corresponds to the first bit of the serial received data from the FIFO.

T1 / J1 RHDLC #1, #2 Primary Address Match (058H, 0D8H, 158H, 1D8H, 258H, 2D8H, 358H, 3D8H)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	PA[7]	PA[6]	PA[5]	PA[4]	PA[3]	PA[2]	PA[1]	PA[0]
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	1	1	1	1	1	1	1	1

Selection of the RHDLC block (#1 or #2) whose registers are visible on the microprocessor interface is done via the RHDLCSEL[1:0] (b7~6, T1/J1-00DH).

PA[7:0]:

These bits stipulate the primary address pattern.

The PA[0] compares to the first bit of the serial data.

T1 / J1 RHDLC #1, #2 Second Address Match (059H, 0D9H, 159H, 1D9H, 259H, 2D9H, 359H, 3D9H)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	SA[7]	SA[6]	SA[5]	SA[4]	SA[3]	SA[2]	SA[1]	SA[0]
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	1	1	1	1	1	1	1	1

Selection of the RHDLC block (#1 or #2) whose registers are visible on the microprocessor interface is done via the RHDLCSEL[1:0] (b7~6, T1/J1-00DH).

SA[7:0]:

These bits stipulate the secondary address pattern.

The SA[0] compares to the first bit of the serial data.

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T1 / J1 TBOM Code (05DH, 0DDH, 15DH, 1DDH, 25DH, 2DDH, 35DH, 3DDH)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	Reserved		BOC[5]	BOC[4]	BOC[3]	BOC[2]	BOC[1]	BOC[0]
Type			R/W	R/W	R/W	R/W	R/W	R/W
Default			1	1	1	1	1	1

When the BOC[5:0] are written with any 6-bit code other than the '111111', the code will be transmitted as the Bit Oriented Message (BOM), over-writing any HDLC packets currently being transmitted. The BOM pattern is '111111110BOC[0]BOC[1]BOC[2]BOC[3]BOC[4]BOC[5]0', that is, the BOC[0] is transmitted first.

T1 / J1 PRGD Control (060H)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	PDR[1]	PDR[0]	Reserved	PS	TINV	RINV	AUTOSYNC	MANSYNC
Type	R/W	R/W		R/W	R/W	R/W	R/W	R/W
Default	0	0		0	0	0	1	0

PDR[1:0]:

The PDR[1:0] define the function of the four PRGD Pattern Detector registers:

PDR[1:0]	PRGD Pattern Detector Registers (#1 ~ #4)
0 0, 0 1	Pattern Receive
1 0	Error Count
1 1	Bit Count
(The #1 is the LSB, while the #4 is the MSB.)	

PS:

= 0: A pseudo-random pattern is generated/detected by the PRGD.

= 1: A repetitive pattern is generated/detected by the PRGD.

This bit should be set first of all the PRGD registers.

TINV:

= 0: Disable inverting the generated pattern before being transmitted.

= 1: Enable inverting the generated pattern before being transmitted.

RINV:

= 0: Disable inverting the received pattern before being processed.

= 1: Enable inverting the received pattern before being processed.

AUTOSYNC:

= 0: Disable automatic re-search for the synchronization of the pattern after the pattern is out of synchronization.

= 1: Enable automatic re-search for the synchronization of the pattern after the pattern is out of synchronization.

MANSYNC:

Trigger on the rising edge. A transition from logic 0 to logic 1 on this bit manually initiates a re-search for the synchronization of a pattern.

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Each time the value of the PRGD registers is changed or the detector data source changes, a manual sync operation is recommended to ensure that the detector works correctly.

T1 / J1 PRGD Interrupt Enable / Status (061H)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	SYNCE	BEE	XFERE	SYNCV	SYNCI	BEI	XFERI	OVR
Type	R/W	R/W	R/W	R	R	R	R	R
Default	0	0	0	X	X	X	X	X

SYNCE:
= 0: Disable the interrupt on the $\overline{INT}$ pin when the SYNCI is logic one.
= 1: Enable the interrupt on the $\overline{INT}$ pin when the SYNCI is logic one.

BEE:
= 0: Disable the interrupt on the $\overline{INT}$ pin when at least one bit error has been detected in the received pattern.
= 1: Enable the interrupt on the $\overline{INT}$ pin when at least one bit error has been detected in the received pattern.

XFERE:
= 0: Disable the interrupt on the $\overline{INT}$ pin when the data in the PRGD pattern detector register is updated.
= 1: Enable the interrupt on the $\overline{INT}$ pin when the data in the PRGD pattern detector register is updated.

SYNCV:
= 0: The pattern is out of synchronization (the pattern detector has detected 10 or more bit errors in a fixed 48-bit window).
= 1: The pattern is in synchronization (the pattern detector has observed at least 48 consecutive error-free bit periods).

SYNCI:
= 0: There is no transition on the SYNCV.
= 1: There is a transition (from '0' to '1' or from '1' to '0') on the SYNCV.
This bit is cleared to '0' after the bit is read.

BEI:
= 0: No bit error is detected in the received pattern.
= 1: At least one bit error has been detected in the received pattern.
This bit is cleared to '0' after the bit is read.

XFERI:
= 0: The data in the PRGD pattern detector register is not updated.
= 1: The data in the PRGD pattern detector register is updated.
This bit is cleared to '0' after the bit is read.

OVR:
= 0: The PRGD pattern detector register is not overwritten.
= 1: The PRGD pattern detector register is overwritten.
This bit is cleared to '0' after the bit is read.

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T1 / J1 PRGD Shift Register Length (062H)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	Reserved			PL[4]	PL[3]	PL[2]	PL[1]	PL[0]
Type				R/W	R/W	R/W	R/W	R/W
Default				0	0	0	0	0

These bits determine the length of the valid data in the PRGD pattern insertion register. The length is equal to the value of 'PL[4:0] + 1'.

T1 / J1 PRGD Tap (063H)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	Reserved			PT[4]	PT[3]	PT[2]	PT[1]	PT[0]
Type				R/W	R/W	R/W	R/W	R/W
Default				0	0	0	0	0

These bits determine the feedback tap position of the generated pseudo random pattern before it is transmitted. The feedback tap position is equal to the value of 'PT[4:0] + 1'. In application, the PT is always less than the PL.

T1 / J1 PRGD Error Insertion (064H)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	Reserved				EVENT	EIR[2]	EIR[1]	EIR[0]
Type					R/W	R/W	R/W	R/W
Default					0	0	0	0

EVENT:

A single bit error is generated when the state of this bit is changed from '0' to '1'. To insert another bit error, this bit must be cleared to '0', and then set from '0' to '1' again.

EIR[2:0]:

The EIR[2:0] bits determine the bit error rate that will be inserted in the PRGD test pattern. If the bit error rate is changed from one non- zero value to another non-zero value, it is recommended to set the EIR[2:0] to '000' first, then set the EIR[2:0] to the desired value.

EIR[2:0]	Bit error rate
0 0 0	No error inserted
0 0 1	No error inserted
0 1 0	10^{-2}
0 1 1	10^{-3}
1 0 0	10^{-4}
1 0 1	10^{-5}
1 1 0	10^{-6}
1 1 1	10^{-7}

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T1 / J1 PRGD Pattern Insertion #1 (068H)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	PI[7]	PI[6]	PI[5]	PI[4]	PI[3]	PI[2]	PI[1]	PI[0]
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

T1 / J1 PRGD Pattern Insertion #2 (069H)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	PI[15]	PI[14]	PI[13]	PI[12]	PI[11]	PI[10]	PI[9]	PI[8]
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

T1 / J1 PRGD Pattern Insertion #3 (06AH)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	PI[23]	PI[22]	PI[21]	PI[20]	PI[19]	PI[18]	PI[17]	PI[16]
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

T1 / J1 PRGD Pattern Insertion #4 (06BH)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	PI[31]	PI[30]	PI[29]	PI[28]	PI[27]	PI[26]	PI[25]	PI[24]
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

When a repetitive pattern is selected to transmit, the data in these registers is the repetitive pattern.

When a pseudo random pattern is selected to transmit, the data in these registers should be set to FFFFFFFFH. They are the initial value for the pseudo random pattern.

Writing to the PI[31:24] updates the PRGD configuration.

When a repetitive pattern is transmitted, the PI[31] is transmitted first, followed by the remaining bits in sequence down to the PI[0]. The length of the valid data in these four registers is determined by the PL[4:0]. When the length is less than 31, the bits in higher PI are not used.

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T1 / J1 PRGD Pattern Detector #1 (06CH)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	PD[7]	PD[6]	PD[5]	PD[4]	PD[3]	PD[2]	PD[1]	PD[0]
Type	R	R	R	R	R	R	R	R
Default	X	X	X	X	X	X	X	X

T1 / J1 PRGD Pattern Detector #2 (06DH)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	PD[15]	PD[14]	PD[13]	PD[12]	PD[11]	PD[10]	PD[9]	PD[8]
Type	R	R	R	R	R	R	R	R
Default	X	X	X	X	X	X	X	X

T1 / J1 PRGD Pattern Detector #3 (06EH)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	PD[23]	PD[22]	PD[21]	PD[20]	PD[19]	PD[18]	PD[17]	PD[16]
Type	R	R	R	R	R	R	R	R
Default	X	X	X	X	X	X	X	X

T1 / J1 PRGD Pattern Detector #4 (06FH)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	PD[31]	PD[30]	PD[29]	PD[28]	PD[27]	PD[26]	PD[25]	PD[24]
Type	R	R	R	R	R	R	R	R
Default	X	X	X	X	X	X	X	X

When the PDR[1:0] (b7~6, T1/J1-060H) are set to '00' or '01', the four PRGD pattern detector registers are configured as Pattern Receive registers. They reflect the content of the received pattern.

When the PDR[1:0] (b7~6, T1/J1-060H) are set to '10', the four PRGD pattern detector registers are configured as Error Counter registers. The value in these registers represents the number of bit errors. The bit errors are not accumulated when the pattern is out of synchronization.

When the PDR[1:0] (b7~6, T1/J1-060H) are set to '11', the four PRGD pattern detector registers are configured as Bit Counter registers. The value in these registers represents the total received bit number.

These registers are updated each second automatically, or by writing to any of these four registers, or to the Revision / Chip ID / Global PMON register.

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T1 / J1 RHDLC Receive Data Link 2 Control (TXCISEL = 0) (070H, 0F0H, 170H, 1F0H, 270H, 2F0H, 370H, 3F0H)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	DL2_EVEN	DL2_ODD	Reserved	DL2_TS[4]	DL2_TS[3]	DL2_TS[2]	DL2_TS[1]	DL2_TS[0]
Type	R/W	R/W		R/W	R/W	R/W	R/W	R/W
Default	0	0		0	0	0	0	0

When the TXCISEL (b3, T1/J1-00DH) is '0', this register is used for the Receive HDLC #2.

DL2_EVEN:
= 0: The data is not extracted from the even frames.
= 1: The data is extracted from the even frames.

DL2_ODD:
= 0: The data is not extracted from the odd frames.
= 1: The data is extracted from the odd frames.

DL2_TS[4:0]:
These bits binary define one channel of even and/or odd frames to extract the data from. They are invalid when the DL2_EVEN and the DL2_ODD are both logic 0.

T1 / J1 RHDLC Data Link 2 Bit Select (TXCISEL = 0) (071H, 0F1H, 171H, 1F1H, 271H, 2F1H, 371H, 3F1H)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	DL2_BIT[7]	DL2_BIT[6]	DL2_BIT[5]	DL2_BIT[4]	DL2_BIT[3]	DL2_BIT[2]	DL2_BIT[1]	DL2_BIT[0]
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

When the TXCISEL (b3, T1/J1-00DH) is '0', this register is used for the Receive HDLC #2.

DL2_BITn:
= 0: The data is not extracted from the corresponding bit.
= 1: The data is extracted from the corresponding bit of the assigned channel.
These bits are invalid when the DL2_EVEN and the DL2_ODD are both logic 0.
The DL1_BIT[7] corresponds to the first bit (MSB) of the selected channel.

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T1 / J1 THDLC Transmit Data Link 2 Control (TXCISEL = 1) (070H, 0F0H, 170H, 1F0H, 270H, 2F0H, 370H, 3F0H)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	DL2_EVEN	DL2_ODD	Reserved	DL2_TS[4]	DL2_TS[3]	DL2_TS[2]	DL2_TS[1]	DL2_TS[0]
Type	R/W	R/W		R/W	R/W	R/W	R/W	R/W
Default	0	0		0	0	0	0	0

When the TXCISEL (b3, T1/J1-00DH) is '1', this register is used for the Transmit HDLC #2.

DL2_EVEN:
= 0: The data is not inserted to the even frames.
= 1: The data is inserted to the even frames.

DL2_ODD:
= 0: The data is not inserted to the odd frames.
= 1: The data is inserted to the odd frames.

DL2_TS[4:0]:
These bits binary define one channel of even and/or odd frames to insert the data to. They are invalid when the DL2_EVEN and the DL2_ODD are both logic 0.

T1 / J1 THDLC Data Link 2 Bit Select (TXCISEL = 1) (071H, 0F1H, 171H, 1F1H, 271H, 2F1H, 371H, 3F1H)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	DL2_BIT[7]	DL2_BIT[6]	DL2_BIT[5]	DL2_BIT[4]	DL2_BIT[3]	DL2_BIT[2]	DL2_BIT[1]	DL2_BIT[0]
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

When the TXCISEL (b3, T1/J1-00DH) is '1', this register is used for the Transmit HDLC #2.

DL2_BITn:
= 0: The data is not inserted to the corresponding bit.
= 1: The data is inserted to the corresponding bit of the assigned channel.
These bits are invalid when the DL2_EVEN and the DL2_ODD are both logic 0.
The DL1_BIT[0] corresponds to the first bit (MSB) of the selected channel.

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T1 / J1 RESI Time Slot Offset (077H, 0F7H, 177H, 1F7H, 277H, 2F7H, 377H, 3F7H)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	Reserved	TSOFF[6]	TSOFF[5]	TSOFF[4]	TSOFF[3]	TSOFF[2]	TSOFF[1]	TSOFF[0]
Type		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0

In Receive Clock Slave mode, when the data rate on the system side is 2.048 Mbit/s (the RSCCK2M [b4, T1/J1-001H] and RSCCK8M [b3, T1/J1-001H] are set to '10'), these bits determine the channel offset between RSCFS and the start of the corresponding frame on RSDn (and RSSIGn).

In Receive Multiplexed mode, these bits determine the channel offset between MRSCFS and the start of the corresponding frame on MRSD and MRSSIG.

In Receive Clock Slave mode, when the data rate on the system side is 1.544 Mbit/s, and in Receive Clock Master mode, the channel offset is disabled. Thus, the TSOFF must be set to '0'.

They define a binary number. The offset can be set from 0 to 127 channels.

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T1 / J1 RESI Time Slot Offset (078H, 0F8H, 178H, 1F8H, 278H, 2F8H, 378H, 3F8H)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	Reserved	FPINV	RSD_RSCFS_EDGE	CMS	BOFF_EN	BOFF[2]	BOFF[1]	BOFF[0]
Type		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0

FPINV:

= 0: The receive framing pulse RSCFS and RSFSn/MRSFS are active high.

= 1: The receive framing pulse RSCFS and RSFSn/MRSFS are active low.

When the bit indicates RSCFS and MRSFS polarity, the bits of all eight framers must have the same value.

RSD_RSCFS_EDGE:

Valid when the CMS (b4, T1/J1-078H) is logic 1 and the setting in the RSCFSFALL (b1, T1/J1-003H) and that in the RSCCKRISE (b0, T1/J1-003H) are equal.

= 0: The second active edge of RSCCK is used to update the signal on the RSDn, RSSIGn and RSFSn pins, or the first active edge of MRSCCK is used to update the signal on the MRSD, MRSSIG and MRSFS pins.

= 1: The first active edge of RSCCK is used to update the signal on the RSDn, RSSIGn and RSFSn pins, or the second active edge of MRSCCK is used to update the signal on the MRSD, MRSSIG and MRSFS pins.

(The signal on the RSCFS/MRSCFS pin is always sampled on the first active edge.)

In Receive Multiplexed mode, the RSD_RSCFS_EDGE in all eight framers should be set to the same value.

CMS:

= 0: The bit rate of RSCCK/MRSCCK is the same as the bit rate of the backplane.

= 1: The bit rate of RSCCK/MRSCCK is double the bit rate of the backplane.

The CMS in all eight framers should be set to the same value.

BOFF_EN:

Valid when the CMS (b4, T1/J1-078H) is 0.

= 0: Disable the bit offset.

= 1: Enable the bit offset.

BOFF[2:0]:

Valid when the CMS (b4, T1/J1-078H)is ‘0’ and the BOFF_EN is ‘1’.

In Receive Clock Slave mode, when the data rate in the system side is 2.048 Mbit/s (the RSCCK2M [b4, T1/J1-001H] and RSCCK8M [b3, T1/J1-001H] are set to ‘10’), these bits determine the bit offset between RSCFS and the start of the corresponding frame on RSDn (and RSSIGn).

In Receive Multiplexed mode, these bits determine the bit offset between MRSCFS and the start of the corresponding frame on MRSD and MRSSIG.

In Receive Clock Slave mode, when the data rate in the system side is 1.544 Mbit/s, and in Receive Clock Master mode, the bit offset is disabled.

These bits define a binary number. Programming of the Bit Offsets is consistent with the convention established by the Concentration Highway Interface (CHI) specification. Refer to the Function Description for details.

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6 IEEE STD 1149.1 JTAG TEST ACCESS PORT

The IDT82V2108 supports the digital Boundary Scan Specification as described in the IEEE 1149.1 standards.

The boundary scan architecture consists of data and instruction registers plus a Test Access Port (TAP) controller. Control of the TAP is achieved through signals applied to the Test Mode Select (TMS) and Test Clock (TCK) input pins. Data is shifted into the registers via the Test Data Input (TDI) pin, and shifted out of the registers via the Test Data Output (TDO) pin. Both TDI and TDO are clocked at a rate determined by TCK.

The JTAG boundary scan registers includes BSR (Boundary Scan Register), IDR (Device Identification Register), BR (Bypass Register) and IR (Instruction Register). These will be described in the following pages. Refer to Figure 85 for architecture.

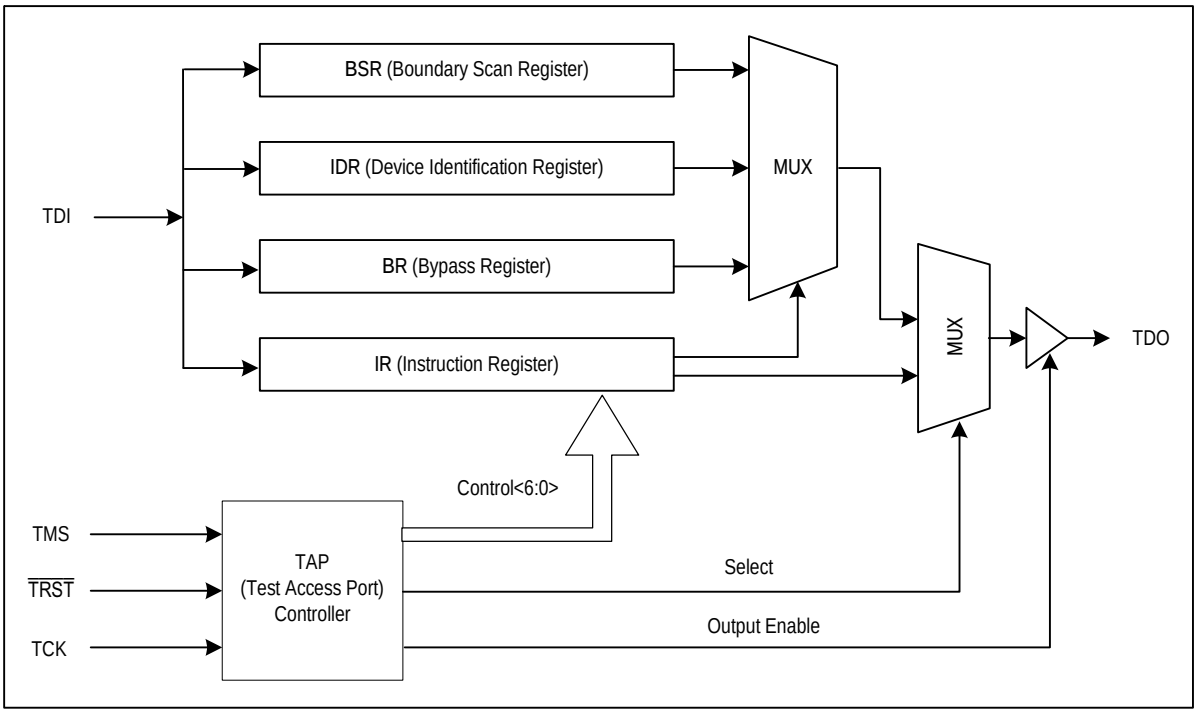


Figure 85. JTAG Architecture

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6.1 JTAG INSTRUCTIONS AND INSTRUCTION REGISTER (IR)

The IR (Instruction Register) with instruction decode block is used to select the test to be executed or the data register to be accessed or both.

The instructions are shifted in LSB first to this 3-bit register. See Table 66 for details of the codes and the instructions related.

Table 66: IR Code

IR CODE	INSTRUCTION	COMMENTS
0 0 0	EXTEST	The external test instruction allows testing of the interconnection to other devices. When the current instruction is the EXTEST instruction, the boundary scan register is placed between TDI and TDO. The signal on the input pins can be sampled by loading the boundary scan register using the Capture-DR state. The sampled values can then be viewed by shifting the boundary scan register using the Shift-DR state. The signal on the output pins can be controlled by loading patterns shifted in through input TDI into the boundary scan register using the Update-DR state.
0 1 0	SAMPLE / PRELOAD	The SAMPLE/PRELOAD instruction is used to allow scanning of the boundary-scan register without causing interference to the normal operation of the on-chip system logic. Data received at system input pins is supplied without modification to the on-chip system logic; data from the on-chip system logic is driven without modification through the system output pins. SAMPLE allows a snapshot to be taken of the data flowing from the system pins to the on-chip system logic or vice versa, without interfering with the normal operation of the assembled board. PRELOAD allows an initial data pattern to be placed at the latched parallel outputs of boundary-scan register cells prior to selection of another boundary-scan test operation.
0 0 1	IDCODE	The identification instruction is used to connect the identification register between TDI and TDO. The device's identification code can then be shifted out using the Shift-DR state.
1 1 1	BYPASS	The BYPASS instruction shifts data from input TDI to output TDO with one TCK clock period delay. The instruction is used to bypass the device.
1 0 0	CLAMP	This instruction allows the state of the signals driven from device pins to be determined from the boundary-scan register while the bypass register is selected as the serial path between TDI and TDO. The signals driven from the device pins will not change while the CLAMP instruction is selected.
1 0 1	HIGHZ	Use of the HIGHZ instruction places the device in a state in which all of its system logic outputs are placed in an inactive drive state (e.g., high impedance). In this state, and in-circuit test system may drive signals onto the connections normally driven by a device output without incurring the risk of damage to the device.
0 1 1		(for manufactory test)

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6.2 JTAG DATA REGISTER

6.2.1 DEVICE IDENTIFICATION REGISTER (IDR)

The IDR can be set to define the Vision, the Part Number, the Manufacturer Identity and a fixed bit. The IDR is 32 bits long and is partitioned as in Table 67. Data from the IDR is shifted out to the TDO LSB first.

Table 67: IDR

BIT No.	COMMENTS
0	Set to '1'
1 ~ 11	Manufacturer Identity (033H)
12 ~ 27	Part Number (04D0H)
28 ~ 31	Version (2H)

6.2.2 BYPASS REGISTER (BYR)

The BYR consists of a single bit. It can provide a serial path between the TDI input and TDO output, bypassing the BYR to reduce test access times.

6.2.3 BOUNDARY SCAN REGISTER (BSR)

The scan chain uses 3 types of cells:

- Input / Output cells: When used as input, the cells are able to sample and control the state of an external signal during BS tests. When used as output, the cells are able to control the state of an external signal during BS tests.

- In/Out or Tri-state output cells: When configured as input, the cells are able to sample and control the state of an external signal. When configured as output, the cells are able to control the state of an external signal.

- Control cell: This cell provides a signal for direction control of bi-directional or tri-state output pins during BS tests.

The Boundary Scan sequence and the I/O Pad Cell type are illustrated in Table 68:

Table 68: Boundary Scan Sequence & I/O Pad Cell Type

Pin_name	Cell Type	BS *
LRD[1]	Input	128
LRCK[1]	Input	127
LRD[2]	Input	126
LRCK[2]	Input	125
LRD[3]	Input	124
LRCK[3]	Input	123
LRD[4]	Input	122
LRCK[4]	Input	121
LTD[1]	Output	120
LTCK[1]	Output	119
LTD[2]	Output	118
LTCK[2]	Output	117
LTD[3]	Output	116
LTCK[3]	Output	115
LTD[4]	Output	114
LTCK[4]	Output	113
LTD[5]	Output	112
LTCK[5]	Output	111
LTD[6]	Output	110
LTCK[6]	Output	109
LTD[7]	Output	108
LTCK[7]	Output	107
LTD[8]	Output	106
LTCK[8]	Output	105
LRD[5]	Input	104
LRCK[5]	Input	103
LRD[6]	Input	102
LRCK[6]	Input	101
LRD[7]	Input	100
LRCK[7]	Input	99
LRD[8]	Input	98
LRCK[8]	Input	97
$\overline{RST}$	Input	96
$\overline{INT}$	Output	95
D[7:0]_EN	Control	94
D[0]	In/Out	93
D[1]	In/Out	92
D[2]	In/Out	91
D[3]	In/Out	90
D[4]	In/Out	89
D[5]	In/Out	88
D[6]	In/Out	87
D[7]	In/Out	86
ALE	Input	85
A[0]	Input	84
A[1]	Input	83
A[2]	Input	82
A[3]	Input	81
A[4]	Input	80
A[5]	Input	79
A[6]	Input	78
A[7]	Input	77
A[8]	Input	76
A[9]	Input	75

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Table 68: Boundary Scan Sequence & I/O Pad Cell Type

Pin_name	Cell Type	BS *
A[10]	Input	74
$\overline{CS}$	Input	73
$\overline{WR}$	Input	72
$\overline{RD}$	Input	71
RSFS[8]	Output	70
RSCK[8]/RSSIG[8]	Tri-state Output	69
RSCK[8]/RSSIG[8]_EN	Control	68
RSD[8]	Tri-state Output	67
RSD[8]_EN	Control	66
RSFS[7]	Output	65
RSCK[7]/RSSIG[7]	Tri-state Output	64
RSCK[7]/RSSIG[7]_EN	Control	63
RSD[7]	Tri-state Output	62
RSD[7]_EN	Control	61
RSFS[6]	Output	60
RSCK[6]/RSSIG[6]	Tri-state Output	59
RSCK[6]/RSSIG[6]_EN	Control	58
RSD[6]	Tri-state Output	57
RSD[6]_EN	Control	56
RSFS[5]	Output	55
RSCK[5]/RSSIG[5]	Tri-state Output	54
RSCK[5]/RSSIG[5]_EN	Control	53
RSD[5]	Tri-state Output	52
RSD[5]_EN	Control	51
RSFS[4]	Output	50
RSCK[4]/RSSIG[4]	Tri-state Output	49
RSCK[4]/RSSIG[4]_EN	Control	48
RSD[4]	Tri-state Output	47
RSD[4]_EN	Control	46
RSFS[3]	Output	45
RSCK[3]/RSSIG[3]	Tri-state Output	44
RSCK[3]/RSSIG[3]_EN	Control	43
RSD[3]	Tri-state Output	42
RSD[3]_EN	Control	41
RSFS[2]/MRSFS[2]	Output	40
RSCK[2]/RSSIG[2]/MRSSIG[2]	Tri-state Output	39
RSCK[2]/RSSIG[2]/MRSSIG[2]_EN	Control	38
RSD[2]/MRSD[2]	Tri-state Output	37
RSD[2]/MRSD[2]_EN	Control	36
RSFS[1]/MRSFS[1]	Output	35
RSCK[1]/RSSIG[1]/MRSSIG[1]	Tri-state Output	34
RSCK[1]/RSSIG[1]/MRSSIG[1]_EN	Control	33
RSD[1]/MRSD[1]	Tri-state Output	32

Table 68: Boundary Scan Sequence & I/O Pad Cell Type

Pin_name	Cell Type	BS *
RSD[1]/MRSD[1]_EN	Control	31
TSSIG[8]/TSFS[8]	In/Out	30
TSSIG[8]/TSFS[8]_EN	Control	29
TSD[8]	Input	28
TSSIG[7]/TSFS[7]	In/Out	27
TSSIG[7]/TSFS[7]_EN	Control	26
TSD[7]	Input	25
TSSIG[6]/TSFS[6]	In/Out	24
TSSIG[6]/TSFS[6]_EN	Control	23
TSD[6]	Input	22
TSSIG[5]/TSFS[5]	In/Out	21
TSSIG[5]/TSFS[5]_EN	Control	20
TSD[5]	Input	19
TSSIG[4]/TSFS[4]	In/Out	18
TSSIG[4]/TSFS[4]_EN	Control	17
TSD[4]	Input	16
TSSIG[3]/TSFS[3]	In/Out	15
TSSIG[3]/TSFS[3]_EN	Control	14
TSD[3]	Input	13
TSFS[2]/TSSIG[2]/MTSSIG[2]	In/Out	12
TSFS[2]/TSSIG[2]/MTSSIG[2]_EN	Control	11
TSD[2]/MTSD[2]	Input	10
TSFS[1]/TSSIG[1]/MTSSIG[1]	In/Out	9
TSFS[1]/TSSIG[1]/MTSSIG[1]_EN	Control	8
TSD[1]/MTSD[1]	Input	7
XCK	Input	6
RSCFS/MRSCFS	Input	5
RSCCK/MRSCCK	Input	4
TSCFS/MTSCFS	Input	3
TSCCKB/MTSCCKB	Input	2
TSCCKA	Input	1

Note: * BS means Boundary Scan Sequence

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6.3 TEST ACCESS PORT CONTROLLER

The TAP controller is a 16-state synchronous state machine. Figure 86 shows its state diagram. A description of each state follows. Note that the figure contains two main branches to access either the data or instruction registers. The value shown next to each state transition in this figure states the value present at TMS at each rising edge of TCK. Please refer to Table 69 for details of the state description.

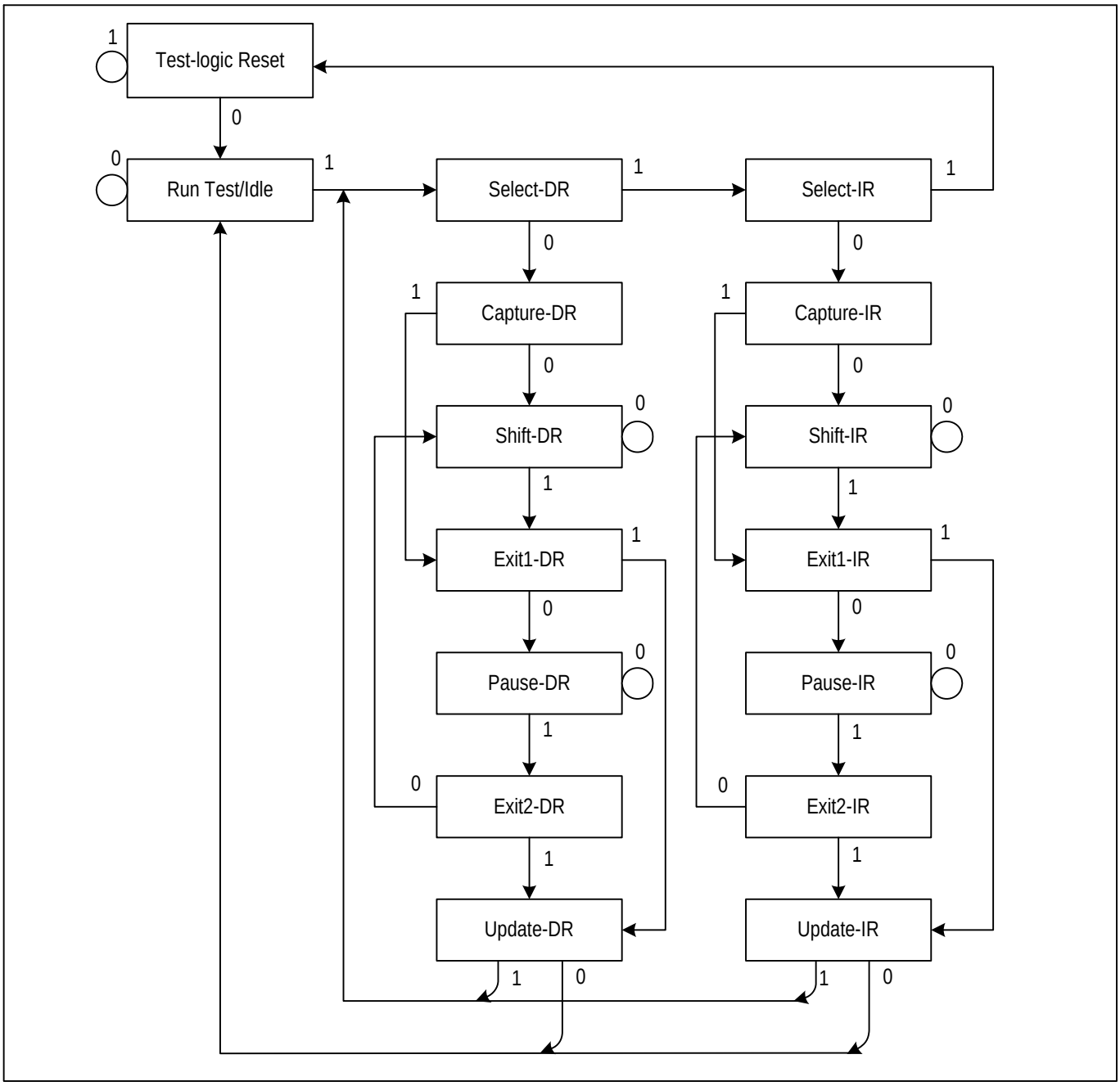


Figure 86. JTAG State Diagram

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Table 69: TAP Controller State Description

STATE	DESCRIPTION
Test Logic Reset	In this state, the test logic is disabled to continue normal operation of the device. During initialization, the device initializes the instruction register with the IDCODE instruction. Regardless of the original state of the controller, the controller enters the Test-Logic-Reset state when the TMS input is held high for at least 5 rising edges of TCK. The controller remains in this state while TMS is high.
Run-Test/Idle	This is a controller state between scan operations. Once in this state, the controller remains in the state as long as TMS is held low. The instruction register and all test data registers retain their previous state. When TMS is high and a rising edge is applied to TCK, the controller moves to the Select-DR state.
Select-DR-Scan	This is a temporary controller state and the instruction does not change in this state. The test data register selected by the current instruction retains its previous state. If TMS is held low and a rising edge is applied to TCK when in this state, the controller moves into the Capture-DR state and a scan sequence for the selected test data register is initiated. If TMS is held high and a rising edge applied to TCK, the controller moves to the Select-IR-Scan state.
Capture-DR	In this state, the Boundary Scan Register captures input pin data if the current instruction is EXTEST or SAMPLE/PRELOAD. The instruction does not change in this state. The other test data registers, which do not have parallel input, are not changed. When the TAP controller is in this state and a rising edge is applied to TCK, the controller enters the Exit1-DR state if TMS is high or the Shift-DR state if TMS is low.
Shift-DR	In this controller state, the test data register connected between TDI and TDO as a result of the current instruction shifts data on stage toward its serial output on each rising edge of TCK. The instruction does not change in this state. When the TAP controller is in this state and a rising edge is applied to TCK, the controller enters the Exit1-DR state if TMS is high or remains in the Shift-DR state if TMS is low.
Exit1-DR	This is a temporary state. While in this state, if TMS is held high, a rising edge applied to TCK causes the controller to enter the Update-DR state, which terminates the scanning process. If TMS is held low and a rising edge is applied to TCK, the controller enters the Pause-DR state. The test data register selected by the current instruction retains its previous value and the instruction does not change during this state.
Pause-DR	The pause state allows the test controller to temporarily halt the shifting of data through the test data register in the serial path between TDI and TDO. For example, this state could be used to allow the tester to reload its pin memory from disk during application of a long test sequence. The test data register selected by the current instruction retains its previous value and the instruction does not change during this state. The controller remains in this state as long as TMS is low. When TMS goes high and a rising edge is applied to TCK, the controller moves to the Exit2-DR state.
Exit2-DR	This is a temporary state. While in this state, if TMS is held high, a rising edge applied to TCK causes the controller to enter the Update-DR state, which terminates the scanning process. If TMS is held low and a rising edge is applied to TCK, the controller enters the Shift-DR state. The test data register selected by the current instruction retains its previous value and the instruction does not change during this state.
Update-DR	The Boundary Scan Register is provided with a latched parallel output to prevent changes while data is shifted in response to the EXTEST and SAMPLE/PRELOAD instructions. When the TAP controller is in this state and the Boundary Scan Register is selected, data is latched into the parallel output of this register from the shift-register path on the falling edge of TCK. The data held at the latched parallel output changes only in this state. All shift-register stages in the test data register selected by the current instruction retain their previous value and the instruction does not change during this state.
Select-IR-Scan	This is a temporary controller state. The test data register selected by the current instruction retains its previous state. If TMS is held low and a rising edge is applied to TCK when in this state, the controller moves into the Capture-IR state, and a scan sequence for the instruction register is initiated. If TMS is held high and a rising edge is applied to TCK, the controller moves to the Test-Logic-Reset state. The instruction does not change during this state.
Capture-IR	In this controller state, the shift register contained in the instruction register loads a fixed value of '100' on the rising edge of TCK. This supports fault-isolation of the board-level serial test data path. Data registers selected by the current instruction retain their value and the instruction does not change during this state. When the controller is in this state and a rising edge is applied to TCK, the controller enters the Exit1-IR state if TMS is held high, or the Shift-IR state if TMS is held low.
Shift-IR	In this state, the shift register contained in the instruction register is connected between TDI and TDO and shifts data one stage towards its serial output on each rising edge of TCK. The test data register selected by the current instruction retains its previous value and the instruction does not change during this state. When the controller is in this state and a rising edge is applied to TCK, the controller enters the Exit1-IR state if TMS is held high, or remains in the Shift-IR state if TMS is held low.
Exit1-IR	This is a temporary state. While in this state, if TMS is held high, a rising edge applied to TCK causes the controller to enter the Update-IR state, which terminates the scanning process. If TMS is held low and a rising edge is applied to TCK, the controller enters the Pause-IR state. The test data register selected by the current instruction retains its previous value and the instruction does not change during this state.
Pause-IR	The pause state allows the test controller to temporarily halt the shifting of data through the instruction register. The test data register selected by the current instruction retains its previous value and the instruction does not change during this state. The controller remains in this state as long as TMS is low. When TMS goes high and a rising edge is applied to TCK, the controller moves to the Exit2-IR state.

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Table 69: TAP Controller State Description

STATE	DESCRIPTION
Exit2-IR	This is a temporary state. While in this state, if TMS is held high, a rising edge applied to TCK causes the controller to enter the Update-IR state, which terminates the scanning process. If TMS is held low and a rising edge is applied to TCK, the controller enters the Shift-IR state. The test data register selected by the current instruction retains its previous value and the instruction does not change during this state.
Update-IR	The instruction shifted into the instruction register is latched into the parallel output from the shift-register path on the falling edge of TCK. When the new instruction has been latched, it becomes the current instruction. The test data registers selected by the current instruction retain their previous value.

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7 PHYSICAL AND ELECTRICAL SPECIFICATIONS

7.1 ABSOLUTE MAXIMUM RATINGS

	Min	Max	
Storage temperature	-65 °C	+150 °C	
Voltage on VDD w.r.t. GND	-0.3 V	4.6 V	
Voltage on BIAS w.r.t. GND	VDD - 0.3 V	5.5 V	
Voltage on any pin	-0.3 V	BIAS + 0.3 V	
Maximum lead temperature		230 °C	during TBC seconds
ESD Performance (HBM)	2000 V		
ESD Performance (CDM)	1000 V		
Latch-up current on any pin	100 ma		
Maximum DC current on any pin			
Maximum lead temperature			
Maximum junction temperature			

7.2 OPERATING CONDITIONS

@ TA = -40 to +85 °C, VDD = 3.3V ± 10%, VDD ≤ BIAS ≤ 5.5 V

7.3 D.C. CHARACTERISTICS

Parameter	Description	Min	Typ	Max	Unit	Test Conditions
VDDC, VDDIO	Core Power Supply	2.97	3.3	3.63	V	
BIAS	5V Tolerant Bias	VDD	5.0	5.5	V	
IBIAS	Current into 5V Bias	0	1	3	mA	VBIAS = 5.5 V
VIL	Input Low Voltage			0.8	V	
VIH	Input High Voltage	2.0		BIAS	V	
VOL	Output Low Voltage			0.4	V	VDD = min, IOL = 2 mA, 3 mA
VOH	Output High Voltage	2.4			V	VDD = min, IOL = 3 mA, 3 mA
VT+	Reset Input High Voltage	1.50	1.75	2.0	V	
VT-	Reset Input Low Voltage	0.83	1.10	1.33	V	
VTH	Reset Input Hysteresis Voltage	0.17	0.65	1.17	V	
IILPU	Input Low Current	-70	-330	-450	uA	VIL = GND
IIL	Input Low Current	-1	0	+1	uA	VIL = GND
IIH	Input High Current	-10	0	+10	uA	VIH = VBIAS
I_{DDOP1}	Operating current		160		mA	E1 mode, XCK = 49.152 MHz, TSCCKB = 2.048 MHz, output unloaded, Vdd = 3.63 V.
I_{DDOP2}	Operating current		170		mA	E1 mode, XCK = 49.152 MHz, TSCCKB = 8.192 MHz, output unloaded, Vdd = 3.63 V.
I_{DDOP3}	Operating current		120		mA	T1 mode, XCK = 37.056 MHz, TSCCKB = 1.544 MHz, output unloaded, Vdd = 3.63 V.

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7.4 CLOCK AND RESET TIMING

The $\overline{RST}$ must be asserted for a minimum of 100 ns after XCLK is stable to ensure that the chip is completely reset.

7.4.1 CLOCK PARAMETERS E1 CONFIGURATION

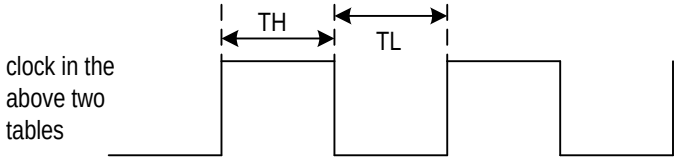
	Min. Frequency (MHz)	Max. Frequency (MHz)	ppm	$T_{L\ min\ (ns)}$ *	$T_{H\ min\ (ns)}$ *
XCK	49.152		±50		
LRCK	2.0	2.1		100	100
MRSCCK	8.0	8.4		40	40
TSCCKA	2.0	2.1		100	100
RSCCK	2.0	2.1		140	140
TSCCKB	2.0	2.1		140	140

7.4.2 CLOCK PARAMETERS T1/J1 CONFIGURATION

	Min. Frequency (MHz)	Max. Frequency (MHz)	ppm	$T_{L\ min}$ [1]	$T_{H\ min}$ [1]
XCK [3]	37.056		±32 [2]		
LRCK	1.534	1.545		100	100
MRSCCK	8.00	8.40		40	40
TSCCKA	1.534	1.545		100	100
RSCCK	1.50	2.058 [4]		140	140
TSCCKB	1.50	2.10 [4]		140	140

NOTE:

1. The T_L and T_H are defined in the figure.



2. An XCK input accuracy of ±100 ppm is only acceptable if an accurate line rate reference is provided. If TJAT is left to free-run without a reference, or referenced to a derivative of XCK, then XCK accuracy must be ±32 ppm. The accuracy of XCK affect the performance of TJAT/RJAT.
3. An XCK input accuracy of ±100 ppm is only acceptable if an accurate line rate reference is provided. If TJAT is left to free-run without a reference, or referenced to a derivative of XCLK, then XCLK accuracy must be ±32 ppm. The accuracy of XCLK affect the performance of TJAT/DJAT.
4. For T1 mode with 2.048Mb/s back-plane data rate only.

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7.5 MICROPROCESSOR READ ACCESS TIMING

Symbol	Parameter		Min	Max	Units
tS_{AR}	Address to Valid Read Set-up Time		0		ns
tH_{AR}	Address to Valid Read Hold Time		0		ns
tS_{ALR}	Address to Latch Set-up Time		5		ns
tH_{ALR}	Address to Latch Hold Time		5		ns
tV_{L}	Valid Latch Pulse Width		10		ns
tS_{LR}	Latch to Read Set-up Time		0		ns
tH_{LR}	Latch to Read Hold		0		ns
tZ_{RD}	Valid Read Negated to Output Tri-state			20	ns
tP_{RD}	Valid Read to Valid Data Propagation Delay	E1		130	ns
		T1		160	ns
tZ_{INTH}	Valid Read Negated to INT Inactive	E1		145	ns
		T1		185	ns
tV_{RD}	Valid Read Width	E1	120		ns
		T1	150		ns
t_{W2R}	Valid interval from last write to next read	E1	120		ns
		T1	150		ns

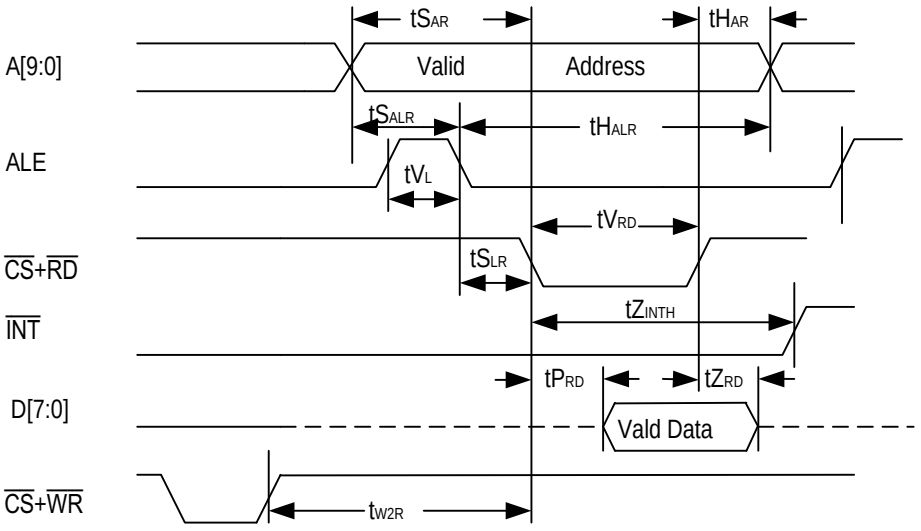


Figure 87. Read Access Timing

Notes:

1. Output propagation delay time is the time from the V_{DD} / 2 point of the reference signal to the 1.4 V point of the output.
2. Maximum output propagation delays are measured with a 100 pF load on the MPIF data bus D[7:0].
3. All the set-up time or hold time are defined as the time between the V_{DD} / 2 point of the reference signal.
4. In non-multiplexed mode, ALE can be held high, tSA_{LR}, tH_{ALR}, tV_{L}, tS_{LR} and tH_{LR} are not applicable.
5. Parameter tH_{AR} is not applicable when address latching is used. The interval of read accesses should > = 180 ns.

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7.6 MICROPROCESSOR WRITE ACCESS TIMING

Symbol	Parameter		Min	MAX	Units
tS_{AW}	Address to Valid Write Set-up Time		5		ns
tS_{DW}	Data to Valid Write Set-up Time		0		ns
tS_{ALW}	Address to Latch Set-up Time		5		ns
tH_{ALW}	Address to Latch Hold Time		5		ns
tV_L	Valid Latch Pulse Width		5		ns
tH_{LW}	Latch to Write Hold		5		ns
tH_{DW}	Data to Valid Write Hold Time		5		ns
tH_{AW}	Address to Valid Write Hold Time		5		ns
t_{W2W}	Write to write interval	E1	80		ns
		T1	100		ns

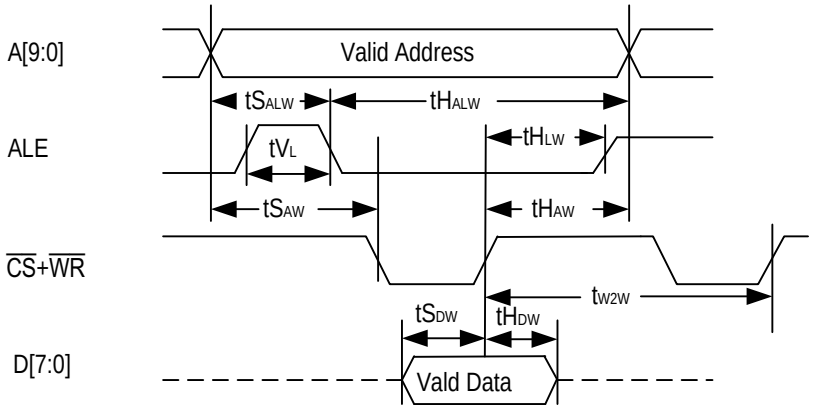


Figure 88. Write Access Timing

Notes:

1. Output propagation delay time is the time from the V_{DD} / 2 point of the reference signal to the V_{DD} / 2 point of the output.
2. All the set-up time or hold time are defined as the time between the V_{DD} / 2 point of the reference signal.
3. In non-multiplexed mode, ALE can be held high, tSA_{LW}, tH_{ALW}, tV_L, tS_{LW} and tH_{LW} are not applicable.
4. Parameter tH_{AW} and tS_{AW} are not applicable when address latching is used.

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7.7 I/O TIMING CHARACTERISTICS

7.7.1 TRANSMIT SYSTEM INTERFACE TIMING

Note that timing information can refer to the positive or negative edge of the reference clock. The active clock edge is selected by configuration flags.

Symbol	Parameter	Min	Typ	Max	Unit
Tprop	Propagation delay	0		20	ns
Ts	Set up time	15			ns
Thold	Hold time	10			ns

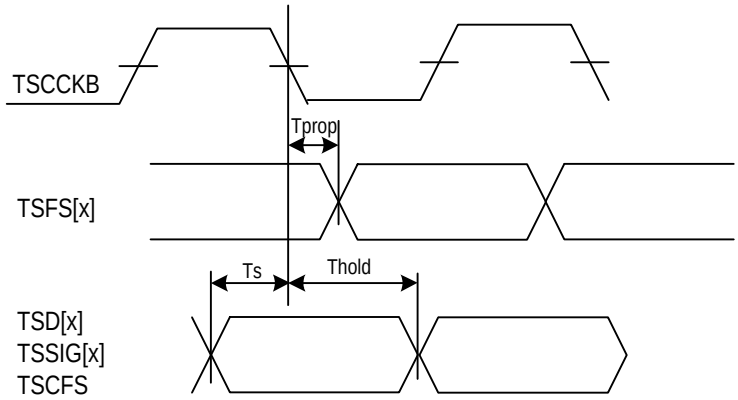


Figure 89. Transmit Interface Timing (Transmit System Common Clock #B)

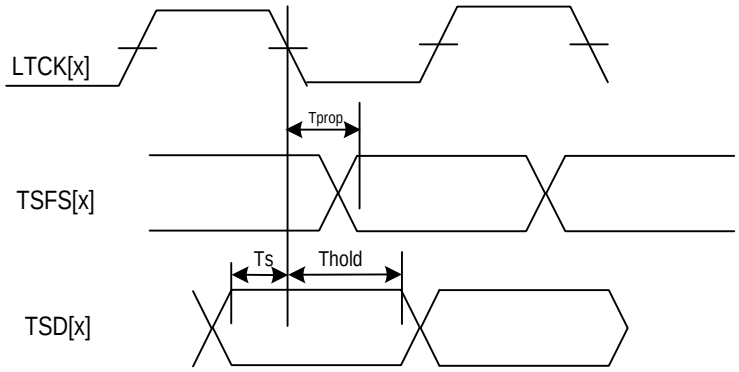


Figure 90. Transmit Interface Timing (Line Transmit Clock)

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7.7.2 RECEIVE SYSTEM INTERFACE TIMING

Note that timing information can refer to the positive or negative edge of the reference clock. The active clock edge is selected by configuration flags.

Symbol	Parameter	Min	Typ	Max	Unit
Tprop	Propagation delay	0		20	ns
Ts	Set up time	10			ns
Thold	Hold time	10			ns

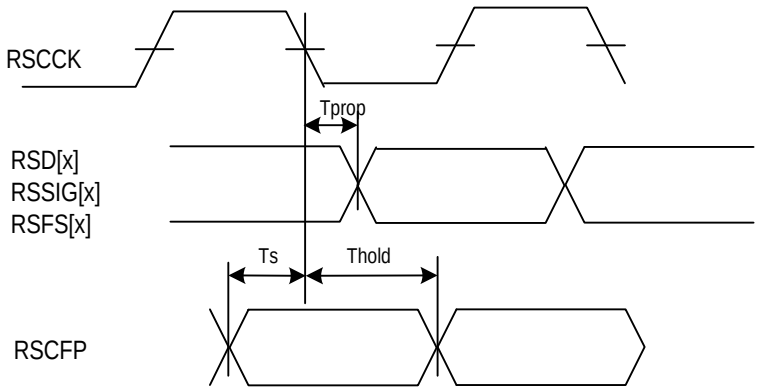


Figure 91. Receive Interface Timing (Receive System Common Clock)

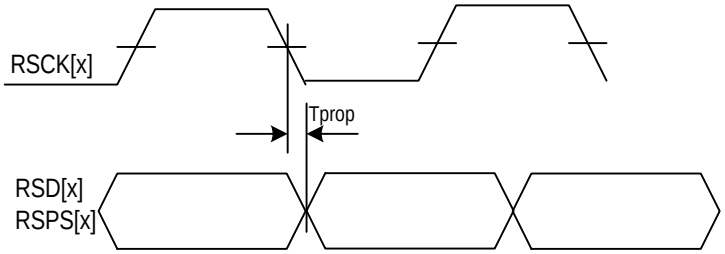


Figure 92. Receive Interface Timing (Receive System Clock)

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7.7.3 RECEIVE & TRANSMIT LINE TIMING

Note that timing information can refer to the positive or negative edge of the reference clock. The active clock edge is selected by configuration flags.

7.7.3.1 Receive Line Interface Timing

Symbol	Parameter	Min	Typ	Max	Unit
Ts	Setup Time	10			ns
Th	Hold Time	10			ns

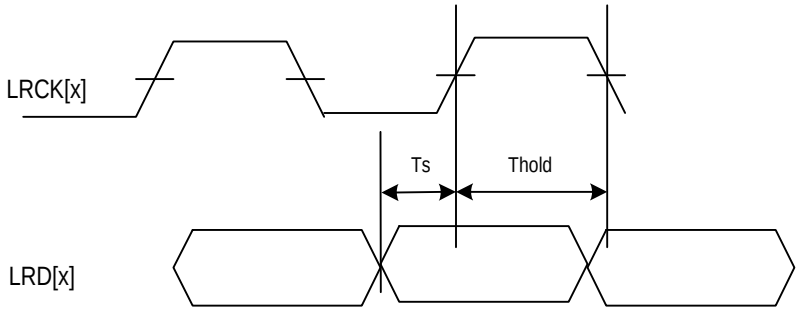


Figure 93. Receive Line Interface Timing

7.7.3.2 Transmit Line Interface Timing

Symbol	Parameter	Min	Typ	Max	Unit
Tprop	Propagation delay	-10		10	ns

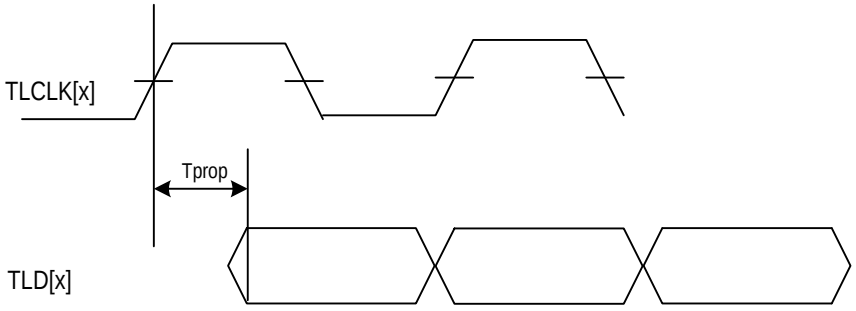
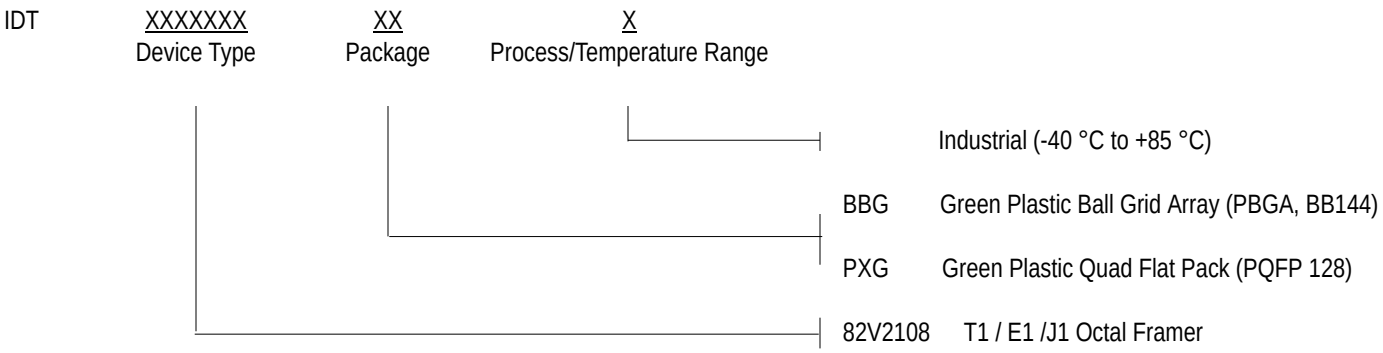


Figure 94. Transmit Line Interface Timing

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ORDERING INFORMATION



Data Sheet Document History

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