INVERSE MULTIPLEXING FOR ATM
IDT82V2604

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FEATURES

- Highlights
  - *Provides API command set for convenient configuration and operation. An embedded controller and a downloaded software are used to interpret the commands. Functions can be added by software upgrading.*
  - *Supports IMA group auto detect.*
  - *Supports link backup so that a backup link can be automatically added when a previously configured link fails.*
  - *All the state machines are implemented in hardware.*
  - *Advanced cell buffer management algorithm to support ATM QoS requirements.*
- Other Features
  - *Accommodates up to 4 IMA logical groups.*
  - *Supports 4 T1/E1 channelized or unchannelized links.*
  - *Supports T1 ISDN links.*
  - *Supports MIXED mode: links not assigned to an IMA group can be used in UNI mode.*
  - *Supports symmetrical and asymmetrical operation.*
  - *Supports Common Transmit Clock (CTC) and Independent Transmit Clock (ITC) timing modes.*
  - *Provides 4 Utopia Level 2 8 bit cell level handshake MPHY interface to ATM device.*
  - *Supports maximum link delay tolerance of up to 212 ms for E1 or 281 ms for T1 (when 512 KB external memory is used).*
  - *Provides parameters for MIB (Management Information Base).*
  - *Supports dynamic addition/deletion of links to/from a working IMA group.*
  - *Supports non-multiplexed Intel or Motorola microprocessor interface.*
  - *Loopback capability at both TDM and Utopia ports.*
  - *Supports MVIP.*
  - *JTAG boundary scan meets IEEE 1149.1.*
  - *Package: 208 pin PBGA.*
  - *3.3V operation / 5V tolerant input.*

APPLICATIONS

- *DSLAM concentrator*
- *3G Wireless base station controller (NodeB) and Radio Network Controller (RNC)*
- *Integrated Access Devices (IAD)*

STANDARDS COMPLIANT

- ATM-Forum
  - *Utopia Level 2 Version 1.0, af-phy-0039.000, June 1995.*
  - *Inverse Multiplexing for ATM Specification version 1.1, af-phy-0086.001, March 1999.*
  - *Backward compatible with Inverse Multiplexing for ATM Specification version 1.0, af-phy-0086.000, September 1994.*
  - *DS1 Physical Layer Specification, af-phy-0016.000, September 1994.*
  - *E1 Physical Interface Specification, af-phy-0064.000, September 1996.*
- ITU-T
  - *I.432 B-ISDN User Network Interface PHY specification.*
  - *G.804 ATM Cell Mapping into Plesiochronous Digital Hierarchy (PDH).*
  - *G.802 Inter-working between networks based on different digital hierarchies and speech encoding laws.*
  - *I.610 B-ISDN operation and maintenance principles and functions.*
- ANSI
  - *ANSI T1.646-1995, Broadband-ISDN-Physical Layer Specification for User-Network Interface Including DS1/ATM, 1995.*
- MVIP

DESCRIPTION

The 4-port IDT82V2604 is a feature-rich device that provides the solution to implement IMA and UNI logical channels over T1 or E1 links in all public or private UNI, NNI and B-ICI applications. The chip is compliant with the ATM Forum IMA specification v1.1 and backward compatible with IMA specification v1.0.

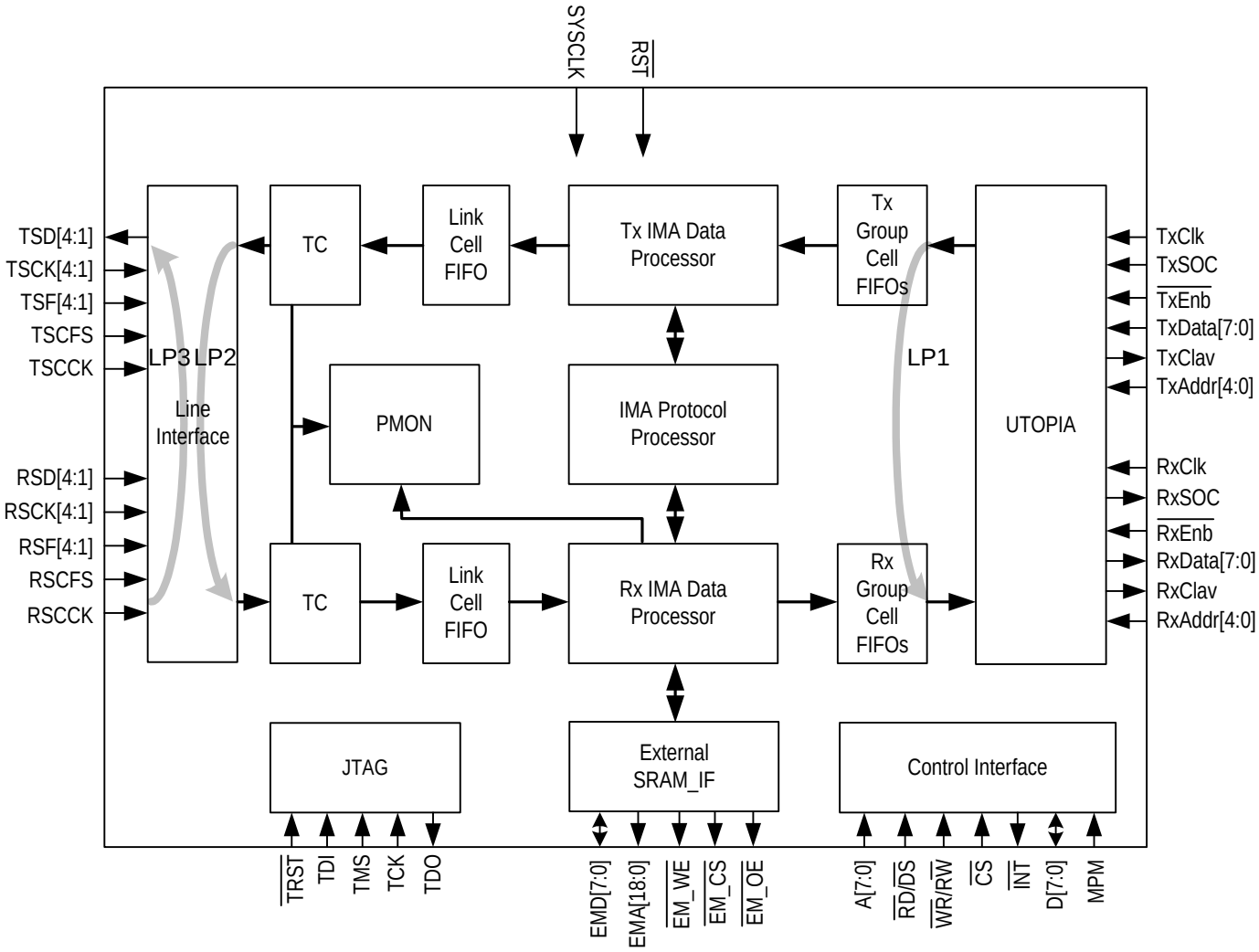
In the chip architecture, up to 4 physically independent T1/E1 streams can be terminated through the utilization of most T1/E1 framers and LIUs in the market, and up to 4 logical IMA groups (i.e., 4 data channels) can be supported at the same time. To interface with most popular ATM layer chips in the market, IDT82V2604 supports Utopia Level 2 MPHY cell level handshake 8-bit bus interface.

Through a well-defined API command set, IMA function can be easily designed into various IMA systems and there is little necessity to access a large amount of registers. A downloaded software is used to interpret the command set and can be easily upgraded to meet specific requirement.

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FUNCTIONAL BLOCK DIAGRAM



LP1: Utopia loopback
LP2: Line interface internal loopback
LP3: Line interface external loopback

Figure-1 Functional Diagram

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1 PIN ASSIGNMENT

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
A	GND	IC	IC	EMD4	EMD0	EMA18	EMA15	EMA12	EMA11	EMA8	EMA5	EMA1	RxData2	RxData5	RxData7	GND	A
B	TMS	TDI	IC	EMD5	EMD1	$\overline{EM_OE}$	EMA16	EMA13	EMA10	EMA7	EMA4	EMA0	RxData3	RxData6	RxSOC	RxClav	B
C	$\overline{TRST}$	TCK	IC	EMD6	EMD2	$\overline{EM_CS}$	EMA17	EMA14	EMA9	EMA6	EMA3	RxData0	RxData4	RxAddr4	RxAddr3	RxAddr2	C
D	NC	TDO	IC	EMD7	EMD3	$\overline{EM_WE}$	VDD	GND	GND	VDD	EMA2	RxData1	RxAddr1	RxAddr0	$\overline{RxENB}$	RxCLK	D
E	RSCK1	RSD1	VDD	SYSCLK									TxClav	TxCLK	TxAddr0	TxAddr1	E
F	RSCK2	RSD2	RSF1	VDD									TxAddr2	TxAddr3	TxAddr4	TxSOC	F
G	RSCK3	RSD3	RSF2	VDD			GND	GND	GND	GND			VDD	$\overline{TxENB}$	TxData7	TxData6	G
H	RSCK4	RSD4	RSF3	GND			GND	GND	GND	GND			GND	TxData5	TxData4	TxData3	H
J	RSF4	IC	IC	GND			GND	GND	GND	GND			GND	TxData0	TxData1	TxData2	J
K	IC	IC	IC	VDD			GND	GND	GND	GND			VDD	IC	IC	IC	K
L	IC	IC	IC	VDD									$\overline{CS}$	IC	IC	IC	L
M	IC	IC	IC	VDD									A6	A7	$\overline{RD}/\overline{DS}$	$\overline{WR}/\overline{RW}$	M
N	IC	RSCFS	RSCCK	VDD	VDD	VDD	VDD	GND	GND	VDD	VDD	A1	A2	A3	A4	A5	N
P	TSCCK	TSCFS	VDD	IC	IC	IC	IC	TSF4	TSCK2	TSCK1	IC	VDD	D6	D7	MPM	A0	P
R	VDD	NC	IC	IC	IC	IC	TSD4	TSD3	TSD2	TSD1	$\overline{RST}$	$\overline{INT}$	D2	D3	D4	D5	R
T	GND	VDD	IC	IC	IC	IC	TSCK4	TSCK3	TSF3	TSF2	TSF1	IC	NC	D0	D1	GND	T
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	

Figure-2 IDT82V2604 PBGA208 Package Pin Assignment (Top View)

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2 PIN DESCRIPTION

Table-1 Pin Description

Name	Pin Number	Input/Output	Description
			Global Signals
SYSCLK	E4	I	SYSCLK: System Clock System clock for the IDT82V2604. Default is 20 MHz.
$\overline{\text{RST}}$	R11	I	**$\overline{\text{RST}}$**: System Reset System reset signal, low active. After reset, all registers are reset to default values, and both the contents in SRAM and the downloaded software are cleared.
			ATM Utopia Interface
TxClk	E14	I	TxClk: Utopia Transmit Clock Utopia transmit clock used to transfer data from the ATM layer to the IDT82V2604. The frequency of the TxClk should be less than or equal to that of the system clock. Data is sampled on the rising edge of this signal.
$\overline{\text{TxEnb}}$	G14	I	**$\overline{\text{TxEnb}}$**: Utopia Transmit Enable Utopia low active signal asserted by the ATM layer device during cycles when TxData contains valid cell data. The $\overline{\text{TxEnb}}$ input is sampled on the rising edge of TxClk.
TxAddr4 TxAddr3 TxAddr2 TxAddr1 TxAddr0	F15 F14 F13 E16 E15	I	TxAddr[4:0]: Utopia Transmit Address Utopia transmit port address driven from the ATM layer to poll and select an appropriate port. The TxAddr[4:0] input bus are sampled on the rising edge of TxClk.
TxData7 TxData6 TxData5 TxData4 TxData3 TxData2 TxData1 TxData0	G15 G16 H14 H15 H16 J16 J15 J14	I	TxData[7:0]: Utopia Transmit Data Utopia 8-bit data bus driven from the ATM layer to the IDT82V2604. The TxData[7:0] input bus are sampled on the rising edge of TxClk.
TxClav	E13	High-Z O	TxClav: Utopia Transmit Cell Available Utopia transmit cell available signal from the IDT82V2604 to the ATM layer. A polled port drives TxClav only during each cycle following one with its address on the TxAddr lines. The polled port asserts TxClav high to indicate its corresponding FIFO can accept the transfer of a complete cell, otherwise it deasserts the signal. The TxClav output is updated on the rising edge of TxClk. Note: This pin requires a pull-down resistor.
TxSOC	F16	I	TxSOC: Utopia Transmit Start of Cell Utopia start of cell signal. It will be driven high by the ATM layer when TxData[7:0] contain the first valid byte of a cell. The TxSOC input is sampled on the rising edge of TxClk.
RxClk	D16	I	RxClk: Utopia Receive Clock Utopia receive clock. The frequency of RxClk should be less than or equal to the frequency of the system clock. Data is sampled on the rising edge of this signal.
$\overline{\text{RxEnb}}$	D15	I	**$\overline{\text{RxEnb}}$**: Utopia Receive Enable When this pin is low, the received data will be transferred on RxData[7:0] in the following cycles. The $\overline{\text{RxEnb}}$ input is sampled on the rising edge of RxClk.

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Table-1 Pin Description (Continued)

Name	Pin Number	Input/Output	Description
RxAddr4 RxAddr3 RxAddr2 RxAddr1 RxAddr0	C14 C15 C16 D13 D14	I	RxAddr[4:0]: Utopia Receive Address Utopia receive port address driven from the ATM layer to poll and select an appropriate port. The RxAddr[4:0] input bus are sampled on the rising edge of RxClk.
RxData7 RxData6 RxData5 RxData4 RxData3 RxData2 RxData1 RxData0	A15 B14 A14 C13 B13 A13 D12 C12	High-Z O	RxData[7:0]: Utopia Receive Data Utopia 8-bit data bus driven from the IDT82V2604 to the ATM layer. The RxData[7:0] output bus are updated on the rising edge of RxClk.
RxClav	B16	High-Z O	RxClav: Utopia Receive Cell Available Utopia cell available signal. A polled port drives RxClav only during each cycle following one with its address on the RxAddr lines. The polled port asserts RxClav high to indicate its corresponding FIFO has a complete cell available for transfer to the ATM layer, otherwise it deasserts the signal. The RxClav output is updated on the rising edge of RxClk. Note: This pin requires a pull-down resistor.
RxSOC	B15	High-Z O	RxSOC: Utopia Receive Start of Cell Utopia start of cell pulse. It will be driven high when RxData[7:0] contain the first valid byte of a cell. The RxSOC input is updated on the rising edge of RxClk.
T1/E1 Line Interface			
TSD4 TSD3 TSD2 TSD1	R7 R8 R9 R10	O	TSDn: Transmit Side Data Output TSDn contains the transmit data for the n-th link. The TSDn output is updated on the rising edge of TSCKn or TSCCK if common clock is used.
TSCK4 TSCK3 TSCK2 TSCK1	T7 T8 P9 P10	I	TSCKn: Transmit Side Clock TSCKn contains the transmit clock for the n-th link. Note: If unused, TSCKn should be connected to ground.
TSF4 TSF3 TSF2 TSF1	P8 T9 T10 T11	I	TSFn: Transmit Side Frame pulse TSFn is used to delineate each frame for the n-th link. The TSFn input is sampled on the falling edge of TSCKn or TSCCK if common clock is used. Note: If unused, TSFn should be connected to ground.
TSCCK	P1	I	TSCCK: Transmit Side Common Clock TSCCK is the transmit clock for links that are configured in Common Clock Mode. Note: If unused, TSCCK should be connected to ground.
TSCFS	P2	I	TSCFS: Transmit Side Common Frame Pulse This signal is used to delineate each frame for links that are configured in Common Clock Mode. The TSCFS input is sampled on the falling edge of TSCCK. Note: If unused, TSCFS should be connected to ground.

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Table-1 Pin Description (Continued)

Name	Pin Number	Input/Output	Description
RSD4 RSD3 RSD2 RSD1	H2 G2 F2 E2	I	RSDn: Receive Side Data Input RSDn contains the receive data for the n-th link. The RSDn input is sampled on the falling edge of RSCKn or RSCCK if common clock is used. Note: If unused, RSDn should be connected to ground.
RSCK4 RSCK3 RSCK2 RSCK1	H1 G1 F1 E1	I	RSCKn: Receive Side Clock RSCKn contains the recovered line clock for the n-th link. Note: If unused, RSCKn should be connected to ground.
RSF4 RSF3 RSF2 RSF1	J1 H3 G3 F3	I	RSFn: Receive Side Frame Pulse RSFn is used to delineate each frame for the n-th link. The RSFn input is sampled on the falling edge of RSCKn or RSCCK if common clock is used. Note: If unused, RSFn should be connected to ground.
RSCCK	N3	I	RSCCK: Receive Side Common Clock RSCCK is the receive clock for links that are configured in Common Clock Mode. Note: If unused, RSCCK should be connected to ground.
RSCFS	N2	I	RSCFS: Receive Side Common Frame Pulse RSCFS is used to delineate each frame for links that are configured in Common Clock Mode. The RSCFS input is sampled on the falling edge of RSCCK. Note: if unused, RSCFS should be connected to ground.
Microprocessor Interface			
MPM	P15	I	MPM: Microprocessor Interface Mode Connected to VDD for Intel; connected to GND for Motorola.
$\overline{RD}$/$\overline{DS}$	M15	I	$\overline{RD}$: Read Operation In parallel Intel microprocessor interface mode, this pin is asserted low by the microprocessor to initiate a read cycle. Data is output to D[7:0] from the device. $\overline{DS}$: Data Strobe In parallel Motorola microprocessor interface mode, this pin is the data strobe of the parallel interface. During a write operation (R$\overline{W}$=0), data on D[7:0] is sampled into the device. During a read operation (R$\overline{W}$=1), data is output to D[7:0] from the device.
$\overline{WR}$/R$\overline{W}$	M16	I	$\overline{WR}$: Write Operation In parallel Intel microprocessor interface mode, this pin is asserted low by the microprocessor to initiate a write cycle. Data on D[7:0] is sampled into the device during a write operation. R$\overline{W}$: Read/Write Select In parallel Motorola microprocessor interface mode, this pin is asserted low for write operation and high for read operation.
D7 D6 D5 D4 D3 D2 D1 D0	P14 P13 R16 R15 R14 R13 T15 T14	I/O	D[7:0]: Data Bus These pins function as a bi-directional data bus of the microprocessor interface.

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Table-1 Pin Description (Continued)

Name	Pin Number	Input/Output	Description
A7 A6 A5 A4 A3 A2 A1 A0	M14 M13 N16 N15 N14 N13 N12 P16	I	A[7:0]: Address Bus These pins function as an address bus of the microprocessor interface.
$\overline{\text{CS}}$	L13	I	**$\overline{\text{CS}}$**: Chip Select For each read or write operation, this pin must be changed from high to low, and remains low until the operation is over.
$\overline{\text{INT}}$	R12	Open_drain	**$\overline{\text{INT}}$**: Interrupt Request A low level on this pin indicates that an interrupt is pending inside the chip.
SRAM Interface			
EMD7 EMD6 EMD5 EMD4 EMD3 EMD2 EMD1 EMD0	D4 C4 B4 A4 D5 C5 B5 A5	I/O	EMD[7:0]: Data Bus Data Input/Output pins for the external SRAM. Used for data exchange between the IDT82V2604 and the external SRAM.
EMA18 EMA17 EMA16 EMA15 EMA14 EMA13 EMA12 EMA11 EMA10 EMA9 EMA8 EMA7 EMA6 EMA5 EMA4 EMA3 EMA2 EMA1 EMA0	A6 C7 B7 A7 C8 B8 A8 A9 B9 C9 A10 B10 C10 A11 B11 C11 D11 A12 B12	O	EMA[18:0]: Address Bus Address of the external SRAM. Used to select a data entry in the external SRAM.
$\overline{\text{EM_WE}}$	D6	O	**$\overline{\text{EM_WE}}$**: Write Enable Write enable signal for the external SRAM. When $\overline{\text{EM_WE}}$ pin and $\overline{\text{EM_CS}}$ pin are both low, data can be written to the external SRAM.
$\overline{\text{EM_OE}}$	B6	O	**$\overline{\text{EM_OE}}$**: Output Enable Output enable signal for the external SRAM. When $\overline{\text{EM_OE}}$ pin and $\overline{\text{EM_CS}}$ pin are both low, data can be read from the external SRAM.
$\overline{\text{EM_CS}}$	C6	O	**$\overline{\text{EM_CS}}$**: Chip Select Chip enable signal for the external SRAM.

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Table-1 Pin Description (Continued)

Name	Pin Number	Input/Output	Description
JTAG & Scan Interface			
TCK	C2	I	TCK: JTAG Test Clock This pin is the input clock for JTAG.
TMS	B1	I	TMS: JTAG Test Mode Select This pin has an internal pull-up resistor.
TDI	B2	I	TDI: JTAG Test Data Input This pin is used to load instructions and data into the test logic and has an internal pull-up resistor.
TDO	D2	High-Z	TDO: JTAG Test Data Output This is normally high impedance and is used to read all the serial configuration and test data from the test logic.
$\overline{\text{TRST}}$	C1	I	$\overline{\text{TRST}}$: JTAG Test Port Reset This pin has an internal pull-up resistor.
Power Supplies and Grounds			
VDD	D7,D10,E3,F4,G4,G13, K4,K13,L4,M4,N4,N5, N6,N7,N10,N11,P3, P12,R1,T2	-	3.3V Power Supply
GND	A1,A16,D8,D9,G7,G8, G9,G10,H4,H7,H8,H9, H10,H13,J4,J7,J8,J9, J10,J13,K7,K8,K9, K10,N8,N9,T1,T16	-	Ground
Others			
IC	L16	-	IC: Internal Connected Internal use. For normal operation, these pins should be connected to VDD.
IC	A2,A3,B3,C3,D3,J2, J3,K1,K2,K3,L1,L2,L3, L15,M1,M2,M3,N1,P4, P5,P6,P7,P11,T3,T4, T5,T6,T12	-	IC: Internal Connected Internal use. For normal operation, these pins should be connected to ground.
IC	K14,K15,K16,L14,R3, R4,R5,R6	-	IC: Internal Connected Internal use. For normal operation, these pins should be left open.
NC	D1,R2,T13	-	NC: No Connection

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3 INTERFACE

3.1 UTOPIA INTERFACE

The Utopia interface operates in Level 2 mode. The IDT82V2604 supports up to 4 Utopia Level 2 ports. Each port is assigned an address ranging from 0 to 30. The address value of 31 is reserved and should not be used. All the 31 ports can be individually enabled or disabled by ConfigUtopiaIF command.

Each IMA group or UNI link corresponds to a port. For each IMA group, the port address can be assigned by ConfigGroupInterface command. For each UNI link, the port address can be assigned by ConfigUNILink command. Inside the device, each port corresponds to a GCF (Group Cell FIFO) which is 2 cells deep.

The IDT82V2604 uses cell level handshake for cell transfer. One entire cell is transferred before another port can be selected. The start of a cell is marked by TxSOC and RxSOC signals in the transmit and the receive directions respectively. These two signals are active during the first byte of a cell.

3.1.1 UTOPIA LOOPBACK FUNCTION

For diagnostic purpose, the capability to loop back all Utopia traffic to Utopia bus is provided. This loopback is called Utopia loopback and can be enabled by ConfigLoopMode command. In this mode, cells are taken from TGCFs (Transmit Group Cell FIFO) and sent to the respective RGCFs (Receive Group Cell FIFO). When in Utopia loopback mode, cells will not be transmitted to the line interface. Refer to Figure-3.

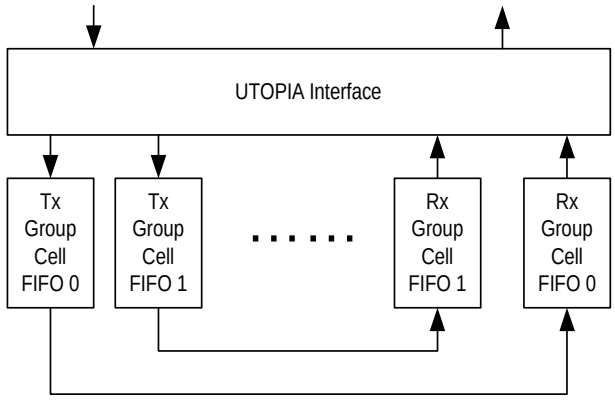


Figure-3 Utopia Loopback

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3.2 LINE INTERFACE

3.2.1 LINE INTERFACE WORK MODES

For different framers, the line interface can be configured to different Work Mode to adapt to different data format. Figure-4 shows all the 16 Work Modes and Table-2 lists IMA layer data rate for each mode.

In channelized mode, all the framing bits and signalling bits are set to zero in transmit direction. And all the received signalling bits and framing bits are discarded in receive direction. In unchannelized mode, all bits are utilized for data transfer.

Work Mode is selected by AddTxLink or AddRxLink command when a link is in an IMA group. The Work Mode is selected by ConfigUNILink command when a link is used as a UNI link.

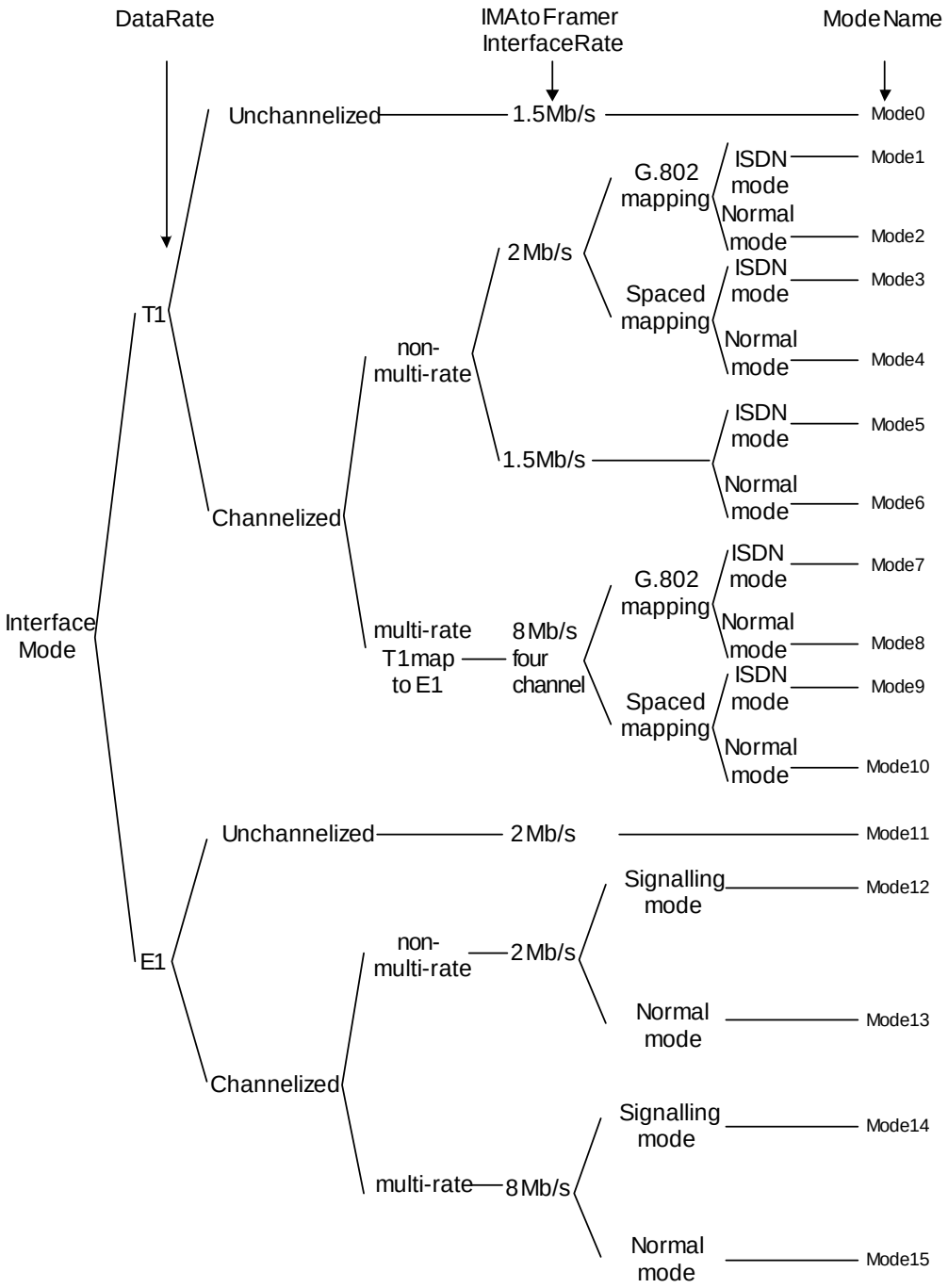


Figure-4 Line Interface Work Modes

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Table-2 Data Rates of Different Modes

Mode	IMA Data Rate Per Channel (Maximum)	Interface Clock (Maximum)
Mode0	1.544 Mb/s	1.544 MHz
Mode1	1.472 Mb/s	2.048 MHz
Mode2	1.536 Mb/s	2.048 MHz
Mode3	1.472 Mb/s	2.048 MHz
Mode4	1.536 Mb/s	2.048 MHz
Mode5	1.472 Mb/s	1.544 MHz
Mode6	1.536 Mb/s	1.544 MHz
Mode7	1.472 Mb/s	8.192 MHz
Mode8	1.536 Mb/s	8.192 MHz
Mode9	1.472 Mb/s	8.192 MHz
Mode10	1.536 Mb/s	8.192 MHz
Mode11	2.048 Mb/s	2.048 MHz
Mode12	1.920 Mb/s	2.048 MHz
Mode13	1.984 Mb/s	2.048 MHz
Mode14	1.920 Mb/s	8.192 MHz
Mode15	1.984 Mb/s	8.192 MHz

3.2.1.1 Mode0

In this mode, the transmit and receive data are viewed as a continuous 1.544 Mb/s serial stream. There is no concept of time slot in an unchannelized link. Each eight bits are grouped into an octet with arbitrary alignment. The first bit received/transmitted is the most significant bit of an octet while the last bit is the least significant bit. The 1.544 MHz data stream clock is provided by the system.

The 1.544 MHz clock in Tx and Rx directions can be either common clock or independent clock. If common clock is used, TSCCK and RSCCK are used as Tx clock and Rx clock respectively, and TSCFS and RSCFS are used as common frame pulse in Tx and Rx directions respectively. If independent clock is used, TSCK[i] and RSCK[i] are used as Tx clock and Rx clock respectively, and TSF[i] and RSF[i] are used as the frame pulse in Tx and Rx directions respectively.

3.2.1.2 Mode1~Mode4

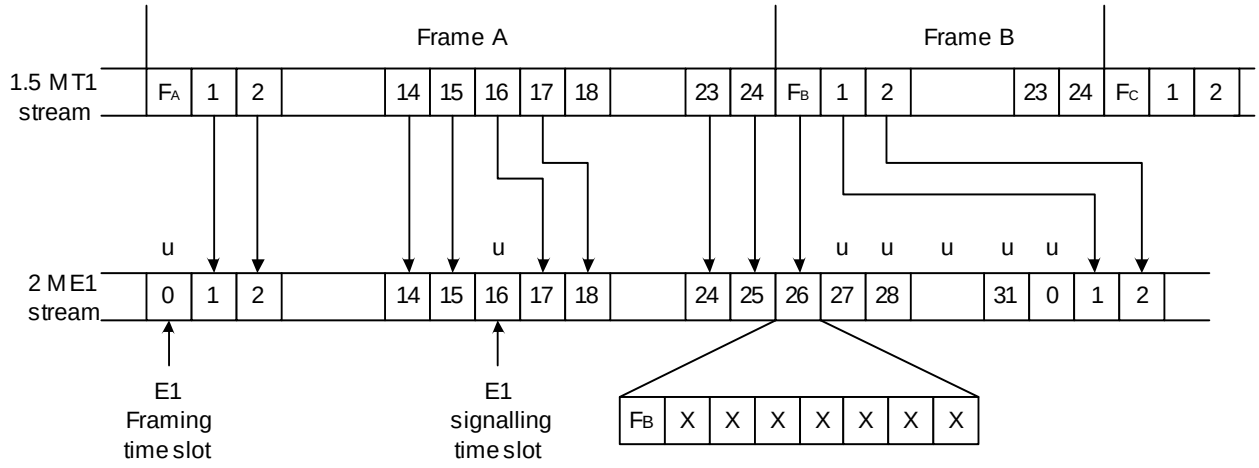
In these four modes, the transmit/receive data rate is T1 channelized while the line interface timing clock is 2.048 MHz (E1 clock). Thus the mapping between T1 frame and E1 frame is needed. Two mapping modes can be used: G.802 mapping mode and spaced mapping mode. Each mapping mode can be further divided into two data modes: T1 ISDN mode and T1 normal mode. The mapping is done in a frame-by-frame fashion and the unassigned time slots are set to zero.

In these modes, the clock for Tx and Rx can be either common clock or independent clock. If common clock is used, TSCCK and RSCCK are used as Tx clock and Rx clock respectively, and TSCFS and RSCFS are used as common frame pulse in Tx and Rx directions respectively. If independent clock is used, TSCK[i] and RSCK[i] are used as Tx clock and Rx clock respectively, and TSF[i] and RSF[i] are used as the frame pulse in Tx and Rx directions respectively.

G.802 Mapping

This mode supports ITU-T Recommendation G.802, which describes how 24 (or 23, in signalling mode) T1 time slots and one framing bit (totally 193/185 bits per T1/T1-ISDN frame) are mapped to 32 E1 time slots (256 bits). This mapping is done by mapping the 24 (or 23 in T1-ISDN mode) T1 time slots to TS1~TS15 and TS17~TS25 (or TS17~TS24), and mapping the framing bit to bit 1 of TS26/TS25. TS0, TS16, TS27/TS26 through TS31 are all unassigned and set to zero (refer to Figure-5).

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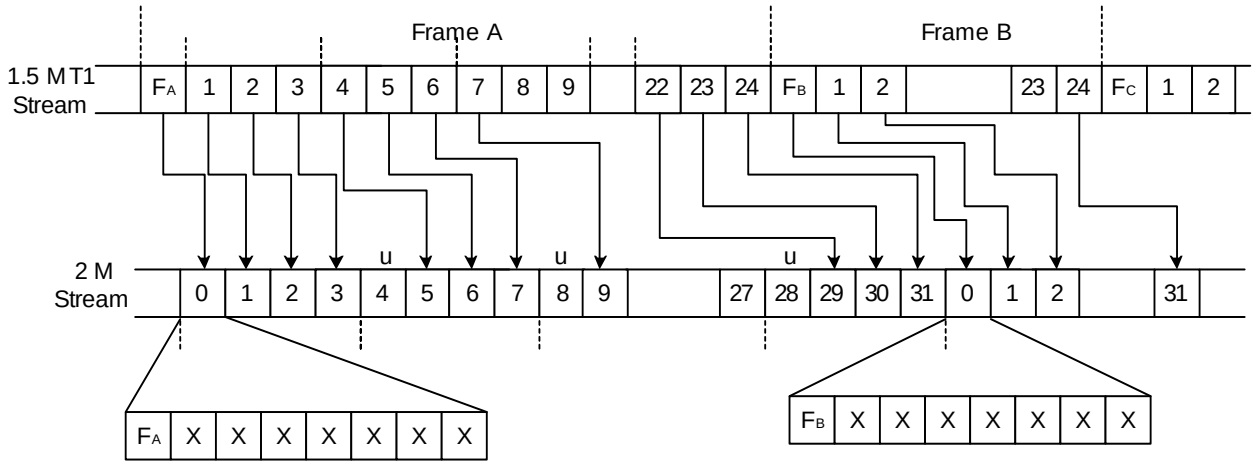


1. X=unused bit
2. u=unassigned time slot
3. F_A, F_B and F_C are T1 framing bits for frame A, B and C respectively.

Figure-5 G.802 Mapping Mode

Spaced Mapping

In this mode, T1 to E1 mapping makes every fourth time slot unassigned (i.e., 4, 8, 12, 16, 20, 24 and 28). Refer to Figure-6. Suppose T1 time slot x is mapped to E1 time slot y. We have y=x+int((x-1)/3), where int(n) is the largest integer no greater than n. The framing bit is assigned to the first bit of TS0. This distribution of unassigned time slots averages out the idle time slots and optimizes the framer's slip buffer's usage.



1. X=unused bits
2. u=unassigned time slot
3. F_A, F_B and F_C are T1 framing bits for frame A, B and C respectively.
4. Mapping rule: If T1 time slot x is mapped to E1 time slot y, y = x+int(x/3). Here int(n) is the largest integer no greater than n.

Figure-6 Spaced Mapping Mode

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T1 ISDN Mode

The T1 ISDN mode corresponds to the use of 23 time slots to transmit data, that is, T1 data is not transmitted during the framing bit and time slot 24. Therefore, only 23 time slots are considered useful and are mapped while time slot 24 and the framing bit are meaningless and are not mapped.

T1 Normal Mode

In this mode, data is not transmitted during the framing bit. The other 24 time slots are useful.

3.2.1.3 Mode5~Mode6

In these modes, the transmit/receive data rate is T1 channelized, and the line interface timing clock is 1.544 MHz (T1 clock). The ISDN mode and normal mode are defined in T1 ISDN Mode and T1 Normal Mode on page 21.

In these modes, the clock for Tx and Rx can be either common clock or independent clock. If common clock is used, TSCCK and RSCCK are used as Tx clock and Rx clock respectively, and TSCFS and RSCFS are used as common frame pulse in Tx and Rx directions respectively. If independent clock is used, TSCK[i] and RSCK[i] are used as Tx clock and Rx clock respectively, and TSF[i] and RSF[i] are used as the frame pulse in Tx and Rx directions respectively.

3.2.1.4 Mode7~Mode10

In these modes, only TSCCK and RSCCK are used to input the 8.192 MHz clock in Tx and Rx directions respectively, and TSCFS and RSCFS are used as common frame pulse in Tx and Rx directions respectively. All the TSCK[i], TSF[i], RSCK[i] and RSF[i] pins are not used and should be connected to ground. The unused RSD pins should also be connected to ground.

The data pins used for multiplexing are shown in the table below:

Table-3 Pins Used in Multi-Rate Multiplex Mode

Tx Pin Name	Rx Pin Name	Multiplexed Channel
TSD[1]	RSD[1]	channel 1~channel 4

Multi-rate

Multi-rate is used for multiplexing four E1 streams into one high-speed stream. Figure-7 shows four 2.048 MHz E1 streams multiplexed into a single 8.192 MHz stream through one data pin. The multiplexing uses the round-robin technology. The system provides 8.192 MHz common clock and 8 kHz common frame pulse.

For T1 channel, before multiplexing, a mapping from each T1 frame to E1 frame is first done. Then the mapped 4 E1 channels are multiplexed into one 8.192 MHz stream as shown in Figure-7.

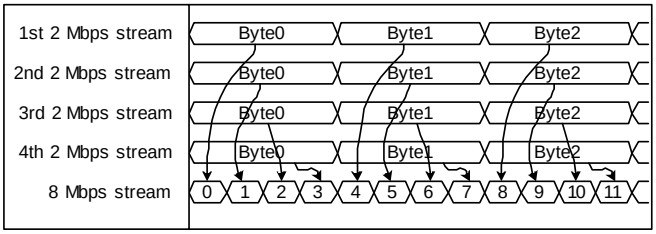


Figure-7 Multiplexing Four 2 MHz Streams into One 8 MHz Stream

T1 Multi-Rate Mode

Since there are two T1 to E1 mapping methods that can be used as described in G.802 Mapping and Spaced Mapping on page 19, two new modes can be derived when multiplexing is further used. Again, T1 ISDN data mode and T1 normal mode can be applied, thus we have 4 more modes: mode7~mode10.

3.2.1.5 Mode11

In this mode, the transmit and receive data are viewed as a continuous 2.048 Mb/s serial stream. There is no concept of time slot in an unchannelized link. Each eight bits are grouped into an octet. TSF or TSCFS signal determine whether the data stream is in byte alignment or not. The first bit received/transmitted is the most significant bit of an octet while the last bit is the least significant bit. The 2.048 MHz data stream clock is provided by the system.

In this mode, the clock for Tx and Rx can be either common clock or independent clock. If common clock is used, TSCCK and RSCCK are used as Tx clock and Rx clock respectively. If independent clock is used, the clock for the i-th link comes from TSCK[i] and RSCK[i] in Tx and Rx directions respectively.

In Common Clock Mode, the TSCFS signal is used for byte alignment pulse for the transmitted bit stream while in Independent Clock Mode, the TSF[i] signal is used for byte alignment pulse for the i-th transmit link.

The frequency for TSF[i] (or TSCSF) is the result of TSCK[i] (or TSCCK) divided by 256 and the pulse width of this signal is one cycle of TSCK[i] or TSCCK signal.

3.2.1.6 Mode12~Mode13

These two modes are E1 non-multi-rate combined with different signalling modes. The non-multi-rate is the channelized generic E1 interface, i.e., a 2.048 MHz channel is divided into 32 sub-channels (also called time slots), and these sub-channels are used to exchange data.

In these modes, the clock for Tx and Rx can be either common clock or independent clock. If common clock is used, TSCCK and RSCCK are used as Tx clock and Rx clock respectively, and TSCFS and RSCFS are used as common frame pulse in Tx and Rx directions respectively. If independent clock is used, TSCK[i] and RSCK[i] are used as Tx clock and Rx clock respectively, and TSF[i] and RSF[i] are used as the frame pulse in Tx and Rx directions respectively.

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Channelized Non-Multi-Rate E1

In this mode, the system provides 2.048 MHz clock and 8 kHz frame pulse for E1 bit stream exchange between the IDT82V2604 and the line interface. The E1 time slot 0 is not used for data exchange while time slot 16 may or may not be used for data exchange, depending on Signalling or Non-Signalling mode.

Signalling and Non-Signalling

In signalling mode, time slot 0 and time slot 16 are not used for data exchange between the IDT82V2604 and the line interface. In non-signalling mode, only time slot 0 is not used for data exchange.

3.2.1.7 Mode14~Mode15

The multi-rate concept is defined in Multi-rate on page 21, and the signalling and non-signalling concepts are defined in Signalling and Non-Signalling on page 22. The system provides 8.192 MHz common clock and 8 kHz common frame pulse.

In these modes, only the TSCCK and RSCCK pins are used to input the 8.192 MHz clock in Tx and Rx directions respectively, and TSCFS and RSCFS are used as common frame pulse in Tx and Rx directions respectively. The TSCK[i], TSF[i], RSCK[i] and RSF[i] pins are not used and should be connected to ground. The unused RSD pins should also be connected to ground.

The data pins used for multiplexing are shown in Table-3.

3.2.2 LINE INTERFACE TIMING CLOCK MODES

Two timing clock modes can be selected. One is Common Clock Mode, the other is Independent Clock Mode. The timing clock mode can be individually configured for each link. In IMA mode, AddTxLink command and AddRxLink command can be used to configure the clock mode in the transmit and receive directions respectively. In UNI mode, ConfigUNILink command can be used to configure the clock mode.

If a link is configured in Common Clock Mode, TSCCK and RSCCK are used as Tx clock and Rx clock respectively, and TSCFS and RSCFS are used as common frame pulse in Tx and Rx directions respectively.

If a link is configured in Independent Clock Mode, TSCK[i] and RSCK[i] are used as Tx clock and Rx clock respectively, and TSF[i] and RSF[i] are used as the frame pulse in Tx and Rx directions respectively.

These two timing clock modes can be configured at the same time, i.e., some links can work in Common Clock Mode while other links can work in Independent Clock Mode.

The line interface mode7~mode10 and mode14~mode15 cannot be used in Independent Clock Mode.

3.2.3 LINE INTERFACE LOOPBACK FUNCTION

The line interface supports two line loopback functions, one is external loopback mode and the other is internal loopback mode. The two loopback modes can be selected by ConfigLoopMode command.

In external loopback mode, all the data received at the line side is looped back to the transmit side and is transmitted out. When this function is enabled, all the links will be in external loopback mode. Data will not be transmitted to the Utopia interface.

In internal loopback mode, the data transmitted are also sent to the receive side. When this function is enabled, all the links will be in internal loopback mode. Data will not be transmitted to the FE Utopia interface.

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3.3 EXTERNAL MICROPROCESSOR INTERFACE

The IDT82V2604 uses an embedded controller and a downloaded software (IMAOS04 or IMAOS04_Slave[1]) to communicate with the external microprocessor. The external microprocessor sends commands to configure the device and read feedbacks. The downloaded software interprets these commands and the embedded controller executes these commands. This relieves programmers from accessing vast registers. Just by accessing a few registers, programmers can use a set of well-defined commands to communicate with IDT82V2604.

3.3.1 EXTERNAL MICROPROCESSOR INTERFACE SELECTION

The IDT82V2604 supports both non-multiplexed Intel and non-multiplexed Motorola microprocessor interfaces. For Intel microprocessor interface, the MPM pin should be connected to VDD; for Motorola microprocessor interface, the MPM pin should be connected to ground.

1. IMAOS04 is used when the device is in normal communication while IMAOS04_Slave is used when the device operates in Slave Mode. Refer to 8.1 Group Auto Detect.

3.3.2 COMMAND FIFOS

The embedded controller uses two FIFOs to communicate with the external microprocessor. One is Input FIFO, which is used to receive commands and data from the external microprocessor; the other is Output FIFO, which is used to send data to the external microprocessor. The lengths of these two FIFOs are both 16 bytes. These two FIFOs can only be accessed through registers.

3.3.3 REGISTERS

The IDT82V2604 provides 9 registers for the external microprocessor to load software to the device, send commands and read feedbacks.

3.3.4 REGISTER MAP

Table-4 Register Map

Address (Hex)	Register	R/W	Map							
			b7	b6	b5	b4	b3	b2	b1	b0
00	INPUT_FIFO_LENGTH_REG	R/W	-	-	-	Input_Message_Length[4:0]				
01	OUTPUT_FIFO_LENGTH_REG	R	-	-	-	Output_Message_Length[4:0]				
02	OUTPUT_FIFO_DATA_REG	R	Output_Data[7:0]							
03	INPUT_FIFO_DATA_REG	R/W	Input_Data[7:0]							
04	FIFO_INT_ENABLE_REG	R/W	-	-	-	-	-	Input_FIFO_empty_int_en	Input_FIFO_overflow_int_en	Output_FIFO_msg_available_int_en
05	FIFO_STATE_REG	R	HW_version					Input_FIFO_empty_state	Input_FIFO_overflow_state	Output_FIFO_msg_available_state
06	FIFO_INT_RESET_REG	W	-	-	-	-	-	-	Input_FIFO_overflow&empty_int_rst	Output_FIFO_msg_available_int_rst
07	OUTPUT_FIFO_INTERNAL_STATE_REG	R	-	-	-	Output_remain_msg_length[4:0]				
08	INPUT_FIFO_INTERNAL_STATE_REG	R	-	-	-	Input_remain_msg_length[4:0]				

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3.3.5 REGISTER DESCRIPTION

Table-5 Input FIFO Data Length Register (INPUT_FIFO_LENGTH_REG)
(R/W, Address=00H)

Symbol	Position	Default	Description
-	7-5	0	Reserved.
Input_Message_Length[4:0]	4-0	0	These 5 bits contain the message length in the Input FIFO which should be written after the message is sent to the Input FIFO. The valid length is from 0 to 16 bytes.

Table-6 Output FIFO Data Length Register (OUTPUT_FIFO_LENGTH_REG)
(R, Address=01H)

Symbol	Position	Default	Description
-	7-5	0	Reserved.
Output_Message_Length[4:0]	4-0	0	These 5 bits contain the length of the message in the Output FIFO. Valid length is from 0 to 16 bytes.

Table-7 Output FIFO Data Register (OUTPUT_FIFO_DATA_REG)
(R, Address=02H)

Symbol	Position	Default	Description
Output_Data[7:0]	7-0	0	These bits contain the data from the message Output FIFO. The complete message can be retrieved by continuously reading this register.

Table-8 Input FIFO Data Register (INPUT_FIFO_DATA_REG)
(R/W, Address=03H)

Symbol	Position	Default	Description
Input_Data[7:0]	7-0	0	These bits contain data to be sent to the Input FIFO. By continuously writing to this register, a complete message can be sent. Before the message is sent, the Input_FIFO_empty_state bit in the EP_interrupt status register should be polled to see whether the Input FIFO is available for writing. After the message is sent, the message length should be written to the EP_Tx_length register.

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Table-9 FIFO Interrupt Enable Register (FIFO_INT_ENABLE_REG)
(R/W, Address=04H)

Symbol	Position	Default	Description
-	7-3	0	Reserved.
Input_FIFO_empty_int_en	2	0	Input FIFO empty interrupt enable 0: Interrupt disabled 1: Interrupt enabled
Input_FIFO_overflow_int_en	1	0	Input FIFO overflow interrupt enable 0: Interrupt disabled 1: Interrupt enabled
Output_FIFO_msg_available_int_en	0	0	Output FIFO message available interrupt enable 0: Interrupt disabled 1: Interrupt enabled

Table-10 FIFO Interrupt Status Register (FIFO_STATE_REG)
(R, Address=05H)

Symbol	Position	Default	Description
HW_version	7-3	1	Current device version. For revision A and B, these bits are '0000'. For revision C, these bits are '0001'.
Input_FIFO_empty_state	2	1	Input FIFO availability status 0: Input FIFO is not available for writing. 1: Input FIFO is available for writing.
Input_FIFO_overflow_state	1	0	Input FIFO overflow status 0: Input FIFO is not full. 1: Input FIFO is full.
Output_FIFO_msg_available_state	0	0	Output FIFO message availability status 0: No message is in the Output FIFO. 1: A message is in the Output FIFO.

Table-11 FIFO Interrupt Reset Register (FIFO_INT_RESET_REG)
(W, Address=06H)

Symbol	Position	Default	Description
-	7-2	0	Reserved.
Input_FIFO_overflow&empty_int_rst	1	0	Write '1' to clear the Input_FIFO_overflow_state status and Input_FIFO_empty_state status.
Output_FIFO_msg_available_int_rst	0	0	Write '1' to clear the Output_FIFO_msg_available_state status.

Table-12 Output FIFO Internal State Register (OUTPUT_FIFO_INTERNAL_STATE_REG)
(R, Address=07H)

Symbol	Position	Default	Description
-	7-5	0	Reserved.
Output_remain_msg_length[4:0]	4-0	0	The length of the message remaining in the Output FIFO to be read by the external microprocessor.

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Table-13 Input FIFO Internal State Register (INPUT_FIFO_INTERNAL_STATE_REG)
(R, Address=08H)

Symbol	Position	Default	Description
-	7-5	0	Reserved.
Input_remain_msg_length[4:0]	4-0	0	The length of the message remaining in the Input FIFO to be processed by the IDT82V2604.

3.3.6 PROCEDURE OF LOADING SOFTWARE AND SENDING COMMANDS

After chip reset, the IMAOS04 or IMAOS04_Slave (a binary file shipped with the chip) should be loaded to the IDT82V2604 to interpret commands. The procedure of loading the IMAOS04 or IMAOS04_Slave is the same with that of sending the commands. Figure-8 shows the Input-FIFO write process and Figure-9 shows the Output-FIFO read process.

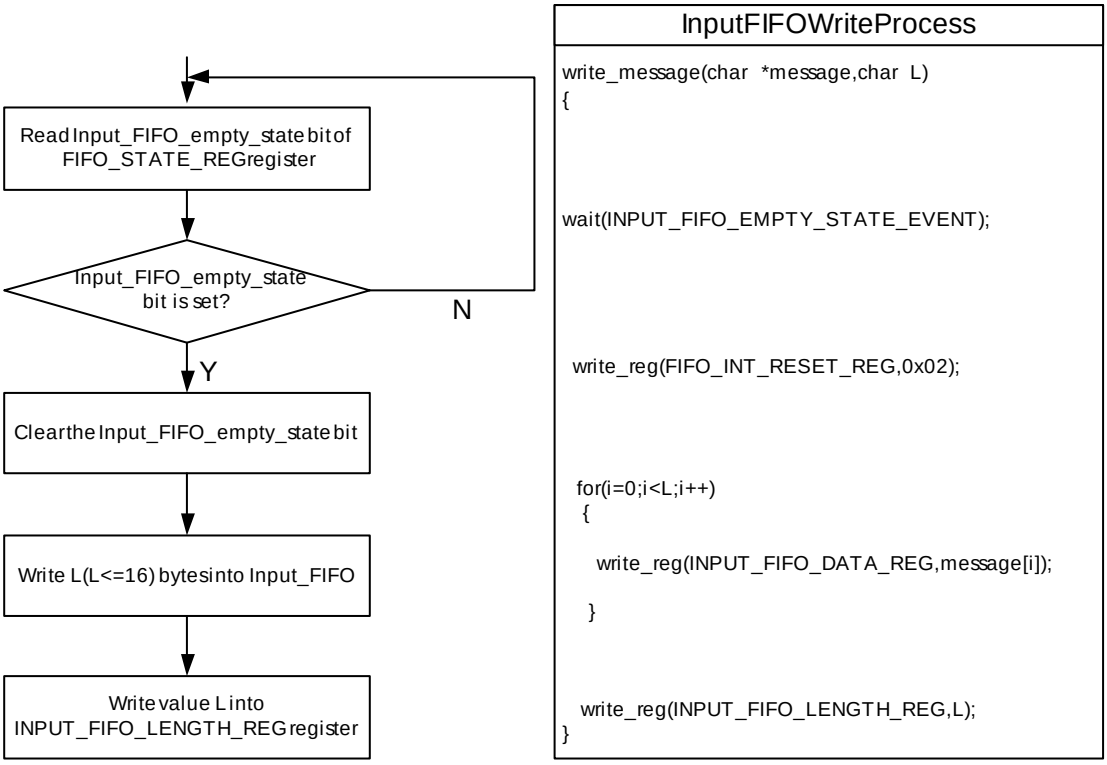


Figure-8 Input FIFO Write Process

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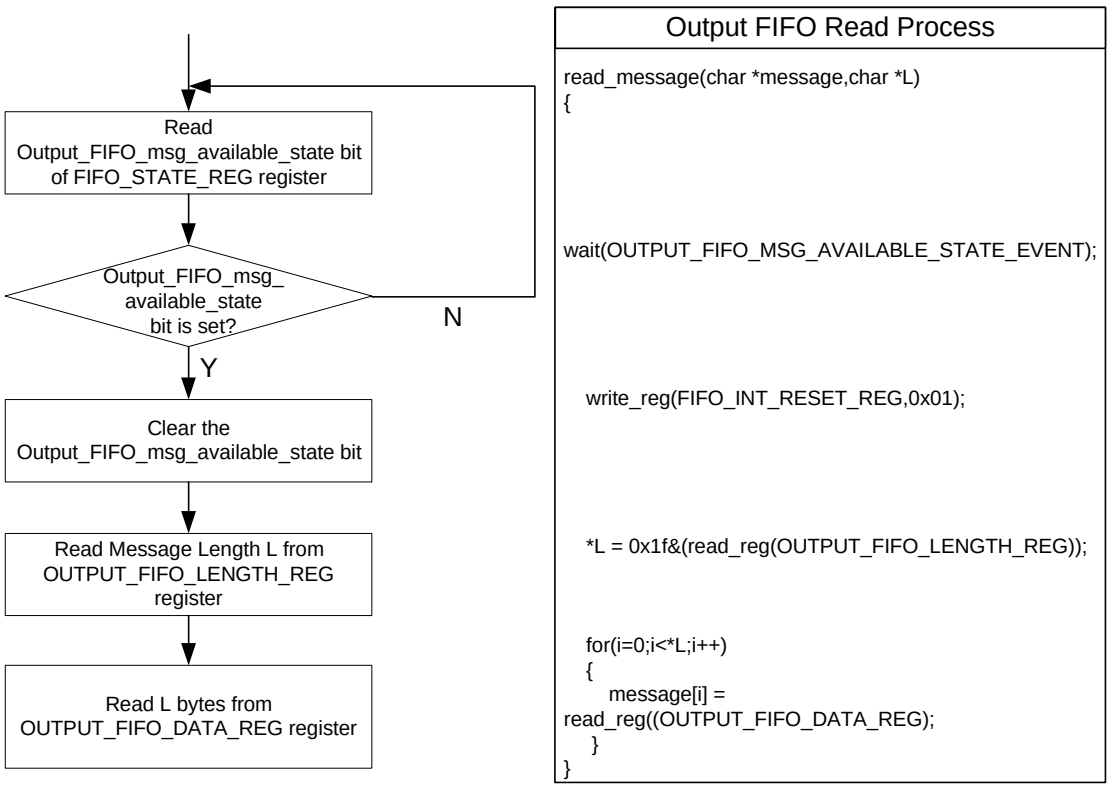


Figure-9 Output FIFO Read Process

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3.4 SRAM INTERFACE

The SRAM interface has an 8-bit wide data bus, EMD[7:0], and a 19-bit wide address bus, EMA[18:0]. The minimum throughput is 4 Mbyte/s and the minimum access time is 40ns.

When both $\overline{\text{EM_WE}}$ pin and $\overline{\text{EM_CS}}$ pin are low, data can be written to the external SRAM. When both $\overline{\text{EM_OE}}$ pin and $\overline{\text{EM_CS}}$ pin are low, data can be read from the external SRAM.

The size of the SRAM can be selected from 2K byte to 512 Kbyte. When the minimum 2K byte memory is selected, only 11 address pins will be used. Different memory size will affect different delay compensation capability. Table-14 and Table-15 show memory size vs. maximum delay tolerance in T1 and E1 unchannelized modes respectively.

Table-14 Maximum Delay Tolerance Value for Different SRAM Size in T1 Unchannelized Mode

SRAM Used (Kbyte)	Maximum Delay Tolerance (ms)	Address Bus Used
512	281	EMA[18:0]
256	141	EMA[17:0]
128	70	EMA[16:0]
64	35	EMA[15:0]
32	17.58	EMA[14:0]
16	8.79	EMA[13:0]
8	4.39	EMA[12:0]
4	2.20	EMA[11:0]
2	1.10	EMA[10:0]

Table-15 Maximum Delay Tolerance Value for Different SRAM Size in E1 Unchannelized Mode

SRAM Used (Kbyte)	Maximum Delay Tolerance (ms)	Address Bus Used
512	212	EMA[18:0]
256	106	EMA[17:0]
128	53	EMA[16:0]
64	26.5	EMA[15:0]
32	13.25	EMA[14:0]
16	6.625	EMA[13:0]
8	3.31	EMA[12:0]
4	1.66	EMA[11:0]
2	0.83	EMA[10:0]

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4 IMA AND UNI FUNCTIONS[1]

The IDT82V2604 is capable of combining the transport bandwidth of multiple links into one single logical link. The logical link is called a group. The IDT82V2604 supports up to 4 independent groups with each group capable of supporting from 1 to 4 links. Links that are assigned to an IMA group are called in IMA mode while links that are not assigned to any IMA group can be used in UNI mode.

4.1 IMA MODE

4.1.1 IMA FRAME

An IMA frame is defined as M consecutive cells, numbered from 0 to M-1 on each link, across all the links in an IMA group. It is generated by inserting an ICP cell after every M-1 cells per link. Values of M supported are 32, 64, 128 and 256, which can be programmed for all the links in a group by ConfigGroupPara command. The ICP cell occurs within the frame at the ICP cell offset position and should be at the same position throughout the frame. The ICP offset is programmable on a per-link basis by AddTxLink command.

4.1.2 TRL (TIMING REFERENCE LINK)

Within an IMA group, a TRL should be selected to pass synchronization from the transmit to the receive end. The TRL can be selected by ConfigTRLLink command.

4.1.3 STUFFING MODE

The insertion of stuff cells is to compensate for timing differences between links within an IMA group.

There are two kinds of stuffing method: CTC (Common Transmit Clock) mode and ITC (Independent Transmit Clock) mode. The stuffing method is selected by ConfigGroupWorkMode command.

In CTC mode, a stuff cell is added after every 2048 ICP, filler and ATM layer cells. The stuff cell is generated by repeating the ICP cell. Both the ICP cell and the stuff cell are identified as ICP cells via the Link Stuff Indication (LSI) field of the ICP cell. The stuff cell event will occur on the same frame on all the links. However, the pre-defined ICP offset will determine at which cell in the frame the stuff event will occur.

In ITC mode, a stuff cell is added to the TRL the same way as in CTC mode, that is, it is added after every 2048 ICP, filler and ATM layer cells. On all other links in the group, stuff cells are added as necessary to compensate for timing differences between the TRL and other links of the group.

In an IMA group, if at least one of the links uses independent clock pin as its clock input, stuff mode can only be set as ITC. If all the links within the group use common clock pin (i.e., TSCCK and RSCCK) as their clock input, stuff mode can be set as either CTC or ITC. For details about the two clock modes, please refer to 3.2.2 Line Interface Timing Clock Modes.

4.1.4 LINK BACKUP

The group link backup function is used to add a link to the group for backup in case of link failure. This function is only enabled when the device is working in symmetry mode.

The link to be added to the group is specified as backup link or non-backup link in 'AddLink' command (i.e., AddTxLink and AddRxLink commands). Note that only one backup link is supported in each group. If several links are specified as backup links, only the last added backup link is regarded as a backup link.

When a link failure event occurred, the IDT82V2604 will automatically pick up a backup link and activate it.

4.2 UNI MODE

ConfigDev command and ConfigUNILink command are used to configure a UNI link. ConfigDev command can be used to configure TC Work Mode, TC Alpha and Delta value and LCD threshold. ConfigUNILink command can be used to configure link physical ID, Tx and Rx Utopia port, line interface Work Mode and clock mode.

When a link is configured in UNI mode, IMA functions are bypassed. ATM cells are simply transmitted from the Utopia interface to the line interface.

1. Chapter 4, 5, 6 and 7 are specific to IMAOS04. Details about IMAOS04_Slave are provided in Chapter 8.

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5 PROGRAMMING INFORMATION FOR IMAOS04

5.1 COMMAND TYPES

There are three types of messages:

1.Command message (external MPU⇒embedded controller)
2.Reply message (embedded controller⇒external MPU)
3.Notification message (embedded controller⇒external MPU)

The formats of the three types of messages are different.

5.1.1 COMMAND MESSAGE

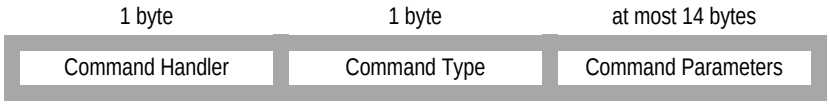


Figure-10 Command Message Format

Command Handler

From 0~126 defined by user's driver. It is the sequence number of the sent message.

Command Type

The encoding of the command. Refer to 5.2 Command Encoding.

Command Parameters

The Parameters of the command.

5.1.2 COMMAND REPLY MESSAGE

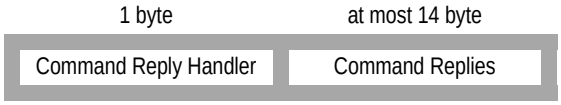


Figure-11 Command Reply Message Format

Command Reply Handler

The original Command Handler plus 128.

Command Replies

The replies of the original command.

5.1.3 ALARM MESSAGE

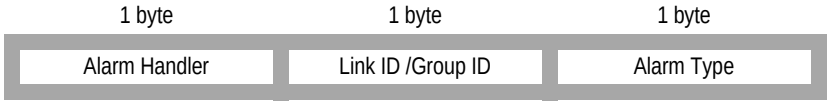


Figure-12 Alarm Message Format

Alarm Handler

FFH.

Link ID /Group ID

The link ID or group ID.

Alarm Type

The sequence in Table-53 Failure/Alarm Signals on page 71.

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5.2 COMMAND ENCODING

Table-16 Command Encoding[1]

Command Encoding	Command Name
01H	ConfigDev
03H	ConfigUtopiaIF
04H	ConfigLoopMode
05H	ConfigGroupPara
06H	ConfigGroupInterFace
07H	ConfigGroupWorkMode
08H	ConfigGSMTimers
09H	ConfigTRLLink
0AH	ConfigIFSMPara
0BH	AddTxLink
0CH	AddRxLink
0DH	ConfigUNILink
0EH	StartGroup
0FH	StartLASR
10H	InhibitGrp
11H	NotInhibitGrp
12H	RestartGrp
13H	DeleteGrp
14H	RecoverLink
15H	DeleteLink
16H	DeactLink
17H	GetGroupState
18H	GetGroupDelayInfo
19H	GetLinkState
1AH	GetGrpPerf
1BH	GetLinkPerf
1CH	GetConfigPara
1DH	GetGrpWorkingPara
1EH	GetLinkWorkingPara
1FH	StartTestPattern
20H	GetLoopedTestPattern
21H	StopTestPattern
22H	GetVersionInfo

1. IMAOS will be in unknown state if the user sends a value not listed in this table.

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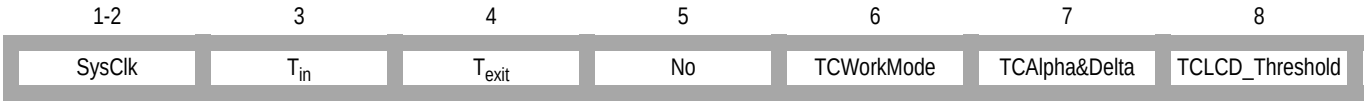
5.3 COMMAND DESCRIPTION

Each command description contains two parts: Command Parameters and Command Reply. In the Command Parameters part, a figure is used to illustrate the byte sequence of the parameters. All the parameter descriptions are listed below the figure. In the Command Reply part, another figure is used to illustrate the reply sequence in the reply message. The reply description is listed below the figure. For detailed information about the packet of command message and reply message, refer to page 30.

Table-17 ConfigDev Command (Encoding: 01H)

This is the first command to be issued. If this command is not issued, the default value will be used.

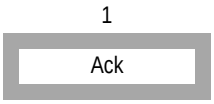
Command Parameters



Byte Sequence	Parameter Name	Default	Description
1-2	SysClk	4E20H	SysClk=Frequency of System Clock (Hz)/1000. For example, if the system clock is 20 MHz, this value would be 20000. Unit: sys-ticks in 1 ms (MSB first) Note: Wrong configuration will make IMAOS's timer work improperly.
3	T_{in}	2H	Timer of entering failure alarm state. When a defect persists for a period set by this timer, the IDT82V2604will enter failure alarm state. Unit: 1 s
4	T_{exit}	0AH	Timer of exiting failure alarm state. If a defect no longer exists for a period set by this timer, the IDT82V2604 will exit failure alarm state. Unit: 1 s
5	No	0H	Reserved. Write 0 to this field.
6	TCWorkMode	7H	<table><tr><th>Bit Position</th><th>Description</th></tr><tr><td>7~3</td><td>Don't Care</td></tr><tr><td>2</td><td>1: Enable Tx TC scrambling (default); 0: Disable Tx TC scrambling</td></tr><tr><td>1</td><td>1: Enable Rx TC HEC error correct control (default); 0: Disable Rx TC HEC error correct control</td></tr><tr><td>0</td><td>1: Enable Rx TC de-scrambling (default); 0: Disable Rx TC de-scrambling</td></tr></table>
7	TCAlpha&Delta	67H	<table><tr><th>Bit Position</th><th>Description</th></tr><tr><td>7-4</td><td>Delta value. Valid is 0~15.</td></tr><tr><td>3-0</td><td>Alpha value. Valid is 0~15.</td></tr></table> Alpha value is the number of consecutive incorrect HEC fields for the Rx cell synchronization state machine to exit sync state. Delta value is the number of consecutive correct HEC fields for the Rx cell synchronization state machine to enter sync state.

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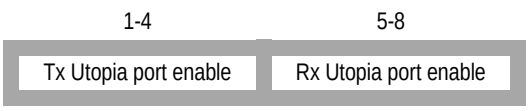
Table-17 ConfigDev Command (Encoding: 01H) (Continued)

8	TCLCD_Threshold	68H	0~255 LCD threshold. If the OCD anomaly persists for the time set by this parameter, LCD defect will be reported. Unit: one cell's transmission time
Command Reply			
			
Byte Sequence	Reply Name	Description	
1	Ack	0: OK; 1: Invalid parameter (length of the command is incorrect); Others: Internal error. The chip should be reset.	

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Table-18 ConfigUtopiaIF Command (Encoding: 03H)

Command Parameters



Byte Sequence	Parameter Name	Default	Description
1-4	Tx Utopia port enable	00000000H	Every bit of the 4 bytes enables a Utopia Tx port (MSB byte first, LSB byte last). 0: Disable the port; 1: Enable the port This 4 bytes parameter enables or disables each of the 31 Utopia port (port 31 is reserved and should not be used). The 4 bytes can be regarded as a sequence of 32 bits. The most significant bit in byte 1 (the first byte sent to embedded controller) is bit 31. The least significant bit of byte 4 (the last byte sent) is bit 0.
5-8	Rx Utopia port enable	00000000H	Every bit of the 4 bytes enables a Utopia Rx port (MSB byte first, LSB byte last). 0: Disable the port; 1: Enable the port The meaning of this parameter is similar to the Utopia Tx port enable field. See above.

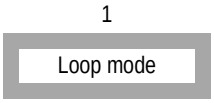
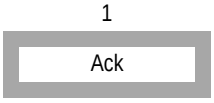
Command Reply



Byte Sequence	Reply Name	Description
1	Ack	0: OK; 1: Invalid parameter (length of the command is incorrect); Others: Internal error. The chip should be reset.

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Table-19 ConfigLoopMode Command (Encoding: 04H)

Command Parameters			
			
Byte Sequence	Parameter Name	Default	Description
1	Loop mode	0H	0: Disable all the loopback functions; 1: Enable line interface internal loopback mode; 2: Enable line interface external loopback mode; 3: Enable Utopia loopback mode; Others: The same as 0.
Command Reply			
			
Byte Sequence	Reply Name	Description	
1	Ack	0: OK; 1: Invalid parameter (length of the command is incorrect); Others: Internal error. The chip should be reset.	

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Table-20 ConfigGroupPara Command (Encoding: 05H)

This is the first command to configure a physical group. Other configuration commands prior to this command would make the group work improperly.

Command Parameters

1	2	3	4	5-6	7	8	9
Group ID	NE IMA ID	M for Tx (M_{tx})	Acceptable M for Rx (M_{rx})	Max delay compensation value	Version Backward Compatibility	P_{tx}	P_{rx}

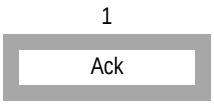
Byte Sequence	Parameter Name	Default	Description
1	Group ID	NA (Not Available)	The physical group ID (0~3) This is the physical identification of an IMA group. Each Group ID is unique in the IDT82V2604 and should not be equal to any Channel ID that has been assigned to a UNI link. There are altogether 4 physical groups. This group ID can be any value from 0~3. Note that this Group ID is not the same as IMA ID which is used to identify a logical IMA group and can be any value from 0~255.
2	NE IMA ID	0H	0~255 This is the logical ID of a physical IMA group, which is packaged in ICP cells and is sent to the FE to indicate which group a link belongs to.
3	M for Tx (M_{tx})	0H	0: 32 (default); 1: 64; 2: 128; 3: 256 This is the IMA frame length that this group will use at the transmit end. There are altogether 4 frame lengths that can be selected: 32, 64, 128 and 256. Note: M_{tx} must be right, otherwise IMAOS will work improperly.
4	Acceptable M for Rx (M_{rx})	NA	<table><tr><th>Bit</th><th>Meaning</th></tr><tr><td>3</td><td>1: Accept M=256 0: Do not accept M=256</td></tr><tr><td>2</td><td>1: Accept M=128 0: Do not accept M=128</td></tr><tr><td>1</td><td>1: Accept M=64 0: Do not accept M=64</td></tr><tr><td>0</td><td>1: Accept M=32 0: Do not accept M=32</td></tr></table>This is the acceptable IMA frame length of the receive end. Note: M_{rx} must be right, otherwise IMAOS will work improperly.
5-6	Max delay compensation value	NA	0~1024 cells This is the maximum cells delay that can be tolerated. This value is constrained by the size of the external SRAM and it shall be no more than 1024 cells. Refer to 3.4 SRAM Interface. Note: If the value exceeds 1024, IMAOS will work improperly.
7	Version Backward Compatibility	NA	0: No; 1: Yes Version backward compatibility indicates whether version 1.0 is supported when the FE's group is using IMA 1.0. By default, the chip works in version 1.1 and does not support backward compatibility.

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Table-20 ConfigGroupPara Command (Encoding: 05H) (Continued)

8	P_{tx}	NA	1~4 The minimum number of active Tx links for the GSM to move to operational state. This implies that the Tx links to be configured should be no less than this number. Note: If this value is larger than the link numbers that will be added later, this IMA group's state machine will stop at Insufficient-Link state.
9	P_{rx}	NA	1~4 The minimum number of active Rx links for the GSM to move to operational state. This implies that the Rx links to be configured should be no less than this number. In SCSO mode, if P_{rx} is not equal to P_{tx}, P_{tx} is used as P_{rx}. Note: If this value is larger than the link numbers that will be added later, this IMA group's state machine will stop at Insufficient-Link state.

Command Reply



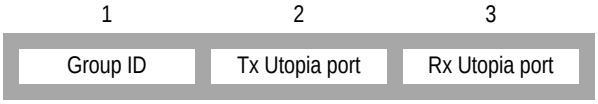
Byte Sequence	Reply Name	Description
1	Ack	0: OK; 1: Invalid parameter; Others: Internal error. The chip should be reset.

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Table-21 ConfigGroupInterFace Command (Encoding: 06H)

This command should follow the ConfigGroupPara command.

Command Parameters



Byte Sequence	Parameter Name	Default	Description
1	Group ID	NA	The physical group ID (0~3). This is the same Group ID in ConfigGroupPara command.
2	Tx Utopia port	1FH	0~30 The Utopia port address for data transmit. Port 31 is reserved and should not be used. Note: The upper 3 bits are Don't Care.
3	Rx Utopia port	1FH	0~30 The Utopia port address for data receive. Port 31 is reserved and should not be used. Note: The upper 3 bits are Don't Care.

Command Reply



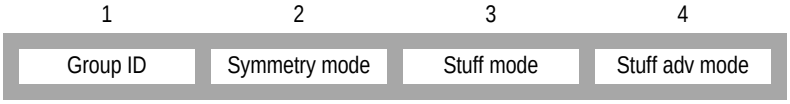
Byte Sequence	Reply Name	Description
1	Ack	0: OK; 1: Invalid parameter; 2: The physical group is not configurable (should issue ConfigGroupPara command first); Others: Internal error. The chip should be reset.

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Table-22 ConfigGroupWorkMode Command (Encoding: 07H)

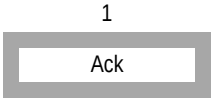
This should be the third command issued to configure a group, i.e., this command should follow ConfigGroupInterface command.

Command Parameters



Byte Sequence	Parameter Name	Default	Description
1	Group ID	NA	The physical group ID (0~3). This is the same Group ID in ConfigGroupPara command.
2	Symmetry mode	NA	0: SCSO (Symmetrical Configuration and Symmetrical Operation); 1: SCAO (Symmetrical Configuration and Asymmetrical Operation); 2: ACAO (Asymmetrical Configuration and Asymmetrical Operation) Note: Value exceeding 2 will be regarded as 0.
3	Stuff mode	1H	0: ITC (Independent Transmit Clock stuff insertion); 1: CTC (Common Transmit Clock stuff insertion) If at least one of the links uses independent clock pin as its clock input, stuff mode can only be set as ITC. If all the links within the group use common clock pin (i.e., TSCCK and RSCCK) as their clock input, stuff mode can be set as either CTC or ITC. Note: Wrong configuration will lead to wrong ICP cells.
4	Stuff adv mode	1H	0: Pre-notify the stuff event 1 frame ahead; 1: Pre-notify the stuff event 4 frames ahead. ICP stuff cell indication. It tells the FE the distance (unit is IMA frame) between the current ICP cell and the forthcoming stuff ICP cell. Note: The upper 7 bits are Don't Care.

Command Reply



Byte Sequence	Reply Name	Description
1	Ack	0: OK; 1: Invalid parameter; 2: The physical group is not configurable; Others: Internal error. The chip should be reset.

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Table-23 ConfigGSMTimers Command (Encoding: 08H)

Command Parameters

1	2	3	4	5
Group ID	Timer for GSM start-up Ack	Timer for GSM Con-figure Abort	Timer for GSM to report Rx=Active	Timer for GSM to report Tx=Active

Byte Sequence	Parameter Name	Default	Description
1	Group ID	NA	Any value is OK. All the groups in the device share the same Timer values.
2	Timer for GSM start-up Ack	4H	1~255 Unit: 250 ms This timer will start when the GSM enters start-up Ack state. If there is no response from the FE after a period set by this timer, the GSM will return from start-up Ack to start-up state. If 0 is sent, it will be interpreted as 1*250 ms by the embedded controller.
3	Timer for GSM Configure Abort	4H	1~255 Unit: 250 ms This timer will start when the GSM enters start-up Abort state. After a period set by this timer, the GSM will return to start-up state. If 0 is sent, it will be interpreted as 1*250 ms by the embedded controller.
4	Timer for GSM to report Rx=Active	4H	1~255 Unit: 250 ms This timer will start when all the Rx links are reported Usable. If either all the configured links are being reported Tx=Usable by the FE or the timer expires, all the Rx links will be brought to Active state. If 0 is sent, it will be interpreted as 1*250 ms by the embedded controller.
5	Timer for GSM to report Tx=Active	4H	1~255 Unit: 250 ms This timer will start when all the Tx links are reported Usable. If either all the configured links are being reported Rx=Active by the FE or the timer expires, all the Tx links will be brought to Active state. If 0 is sent, it will be interpreted as 1*250 ms by the embedded controller.

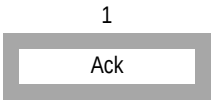
Command Reply

1
Ack

Byte Sequence	Reply Name	Description
1	Ack	0: OK; 1: Invalid parameter; 2: The physical group is not configurable; Others: Internal error. The chip should be reset.

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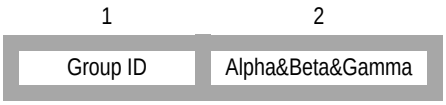
Table-24 ConfigTRLLink Command (Encoding: 09H)

Command Parameters			
			
Byte Sequence	Parameter Name	Default	Description
1	Group ID	NA	The physical group ID (0~3). This is the same Group ID in ConfigGroupPara command.
2	TxTRL	0H	0~3 The TRL link selected for this group. Data on TSD1 pin is deemed data on Tx link 0; Data on TSD2 pin is deemed data on Tx link 1 and so on. This link should have been added to the group, otherwise the group will fail to start up. If the TRL link has been configured previously, this command is used to change the TRL link.
Command Reply			
			
Byte Sequence	Reply Name	Description	
	Ack	0: OK; 1: Invalid parameter; 2: The physical group is not configurable; Others: Internal error. The chip should be reset.	

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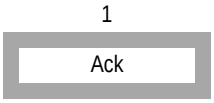
Table-25 ConfigIFSMPara Command (Encoding: 0AH)

Command Parameters



Byte Sequence	Parameter Name	Default	Description
1	Group ID	NA	The physical group ID (0~3). This is the same Group ID in ConfigGroupPara command.
2	Alpha&Beta&Gamma	91H	Bit 7-6: Alpha value. Default is 2. Bit 5-3: Beta value. Default is 2. Bit 2-0: Gamma value. Default is 1. Alpha value is the number of consecutive invalid ICP cells for the IFSM state machine to exit SYNC state. Beta is the number of consecutive errored ICP cells for the IFSM state machine to exit SYNC state. Gamma is the number of consecutive valid ICP cells for the IFSM state machine to enter SYNC state.

Command Reply

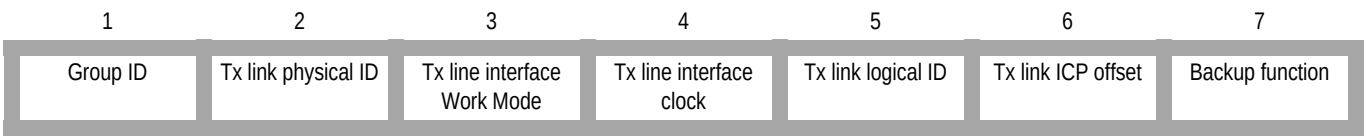


Byte Sequence	Reply Name	Description
1	Ack	0: OK; 1: Invalid parameter; 2: The physical group is not configurable; Others: Internal error. The chip should be reset.

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Table-26 AddTxLink Command (Encoding: 0BH)

Command Parameters



Byte Sequence	Parameter Name	Default	Description
1	Group ID	NA	The physical group ID (0~3). This is the same Group ID in ConfigGroupPara command.
2	Tx link physical ID	NA	0~3 The Tx link that will be configured to this group. Data on TSD1 pin is deemed data on Tx link 0; Data on TSD2 pin is deemed data on Tx link 1 and so on. Note: If the value exceeds 3, IMAOS will work improperly.
3	Tx line interface Work Mode	0FH	Mode0~Mode15 Line interface Work Mode for this link. Note: If the value exceeds 15, IMAOS will work improperly.
4	Tx line interface clock	0H	0: Common Clock Mode; 1: Independent Clock Mode Line interface clock input mode. The line interface mode7~mode10 and mode14~mode15 cannot be used in Independent Clock Mode. Note: IMAOS does not check this value. Value exceeding 1 will cause wrong configuration.
5	Tx link logical ID	0H	0~31 The logical Tx link # designated to that physical link. It is used for Tx ICP cell. Note: IMAOS does not check this value. If this value is wrong, IMAOS will work improperly.
6	Tx link ICP offset	0H	The ICP offset over that Tx link The ICP cell offset of the IMA frame on that link. This value should be smaller than the Tx frame length. Note: If this value is wrong, IMAOS will work improperly.
7	Backup function	NA	0: No; 1: Yes Whether this is a backup link or not. When other links failed, this link will be automatically added to the group. Note1: Only one backup link is supported in each group. If several links are specified as backup links, only the last added backup link is regarded as a backup link. Note2: If a backup link is added after the StartGroup or StartLASR command, a StartLASR command should be issued to make this backup link take effect.

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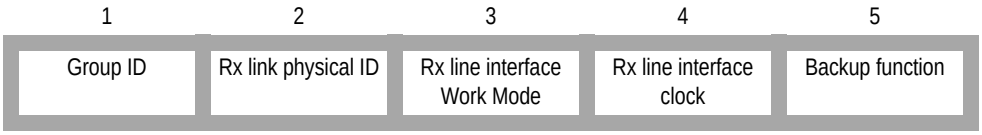
Table-26 AddTxLink Command (Encoding: 0BH) (Continued)

Command Reply		
		
Byte Sequence	Reply Name	Description
	Ack	0: OK; 1: Invalid parameter; 2: The physical group is not configurable; 3: Tx physical link is used by other groups; 4: Tx ICP offset is larger than M; 5: Link logical ID is used by other links in this group; Others: Internal error. The chip should be reset.

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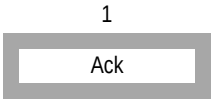
Table-27 AddRxLink Command (Encoding: 0CH)

Command Parameters



Byte Sequence	Parameter Name	Default	Description
1	Group ID	NA	The physical group ID (0~3). This is the same Group ID in ConfigGroupPara command.
2	Rx link physical ID	NA	0~3 The Rx link that will be configured to this group. Data on RSD1 pin is deemed data on Rx link 0; Data on RSD2 pin is deemed data on Rx link 1 and so on. Note: If the value exceeds 3, IMAOS will work improperly.
3	Rx line interface Work Mode	0FH	Mode0~mode15 Line interface Work Mode for this link. Note: If the value exceeds 15, IMAOS will work improperly.
4	Rx line interface clock	0H	0: Common Clock Mode; 1: Independent Clock Mode Line interface clock input mode. The line interface mode7~mode10 and mode14~mode15 cannot be used in Independent Clock Mode. Note: IMAOS does not check this value. Value exceeding 1 will cause wrong configuration.
5	Backup function	NA	0: No; 1: Yes Whether this is a backup link or not. When other links fail, this link will be automatically added to the group. Note: Only one backup link is supported in each group. If several links are specified as backup links, only the last added backup link is regarded as a backup link.

Command Reply

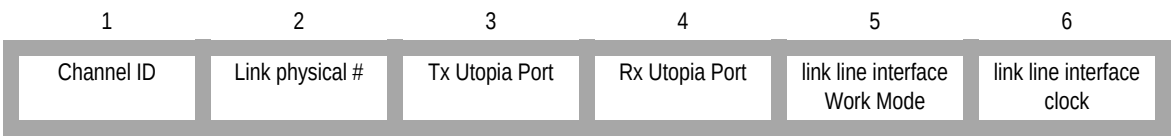


Byte Sequence	Reply Name	Description
1	Ack	0: OK; 1: Invalid parameter; 2: The physical group is not configurable; 3: The Rx physical link is used by other groups; Others: Internal error. The chip should be reset.

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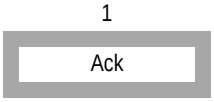
Table-28 ConfigUNILink Command (Encoding: 0DH)

Command Parameters



Byte Sequence	Parameter Name	Default	Description
1	Channel ID	NA	0~3 The internally used channel for this UNI link. Each Channel ID is unique and should not be equal to any Group ID that has been assigned.
2	Link physical #	NA	0~3 The physical link to be used in UNI mode. Note: If the value exceeds 3, the performance cannot be guaranteed.
3	Tx Utopia Port	1FH	0~30 The Utopia port address for data transmit. Port 31 is reserved and should not be used. Note: The upper 3 bits are Don't Care.
4	Rx Utopia Port	1FH	0~30 The Utopia port address for data receive. Port 31 is reserved and should not be used. Note: The upper 3 bits are Don't Care.
5	link line interface Work Mode	0FH	Mode0~mode15 Line interface Work Mode for this link. Note: If the value exceeds 15, IMAOS will work improperly.
6	link line interface clock	0H	0: Common Clock Mode; 1: Independent Clock Mode Line interface clock input mode. The line interface mode7~mode10 and mode14~mode15 cannot be used in Independent Clock Mode. Note: IMAOS does not check this value. Value exceeding 1 will cause wrong configuration.

Command Reply

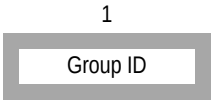
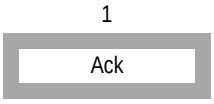


Byte Sequence	Reply Name	Description
1	Ack	0: OK; 1: The link is busy or Channel ID is over 15; Others: Internal error. The chip should be reset.

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Table-29 StartGroup Command (Encoding: 0EH)

This command is used to start a configured group.

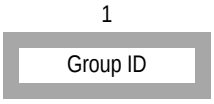
Command Parameters			
			
Byte Sequence	Parameter Name	Default	Description
1	Group ID	NA	The valid physical group that has been configured. This is the same Group ID in ConfigGroupPara command.
Command Reply			
			
Byte Sequence	Reply Name	Description	
1	Ack	0: Acknowledge; 1: Invalid parameter; 2: The group is not configured; Others: Internal error. The chip should be reset.	

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Table-30 StartLASR Command (Encoding: 0FH)

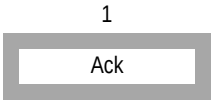
This command is used to start LASR procedure on one or more links. The links here may be new links or links with failure/fault/inhibiting condition. This command may combine with AddTxLink and AddRxLink commands.

Command Parameters



Byte Sequence	Parameter Name	Default	Description
1	Group ID	NA	The physical group ID (0~3). Valid physical group that has been configured and is in OPERATIONAL state.

Command Reply



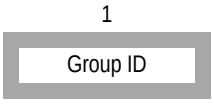
Byte Sequence	Reply Name	Description
1	Ack	0: Acknowledge; 1: Invalid parameter; 2: The group is not configured; 3: The Previous LASR is not finished; Others: Internal error. The chip should be reset.

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Table-31 InhibitGrp Command (Encoding: 10H)

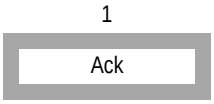
This command is used to inhibit a group. Once a group is inhibited by this command, it will go to BLOCKED state instead of the OPERATIONAL state when sufficient links exist in the group. If the group is already in OPERATIONAL state, the GSM will transition to BLOCKED state.

Command Parameters



Byte Sequence	Parameter Name	Default	Description
1	Group ID	NA	The physical group ID (0~3). The physical group to be inhibited.

Command Reply



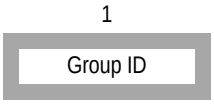
Byte Sequence	Reply Name	Description
1	Ack	0: Acknowledge; 1: Invalid parameter; Others: Internal error. The chip should be reset.

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Table-32 NotInhibitGrp Command (Encoding: 11H)

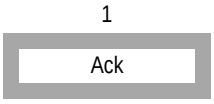
This command is used to clear the inhibiting status. If a group is in BLOCKED state, the GSM will go to OPERATIONAL state.

Command Parameters



Byte Sequence	Parameter Name	Default	Description
1	Group ID	NA	The physical group ID (0~3). The physical group to be uninhibited.

Command Reply



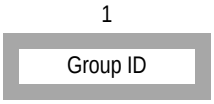
Byte Sequence	Reply Name	Description
1	Ack	0: Acknowledge; 1: Invalid parameter; Others: Internal error. The chip should be reset.

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Table-33 RestartGrp Command (Encoding: 12H)

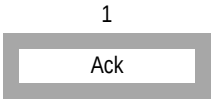
This command is used to restart the specified group. The GSM will go back to Start-up state and all the Tx and Rx links will go back to Unusable state.

Command Parameters



Byte Sequence	Parameter Name	Default	Description
1	Group ID	NA	The physical group ID (0~3). The physical group to be restarted.

Command Reply



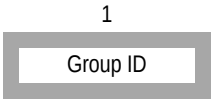
Byte Sequence	Reply Name	Description
1	Ack	0: Acknowledge; 1: Invalid parameter; 2: The group is not configured; Others: Internal error. The chip should be reset.

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Table-34 DeleteGrp Command (Encoding: 13H)

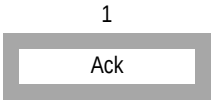
This command is used to delete the specified group and all its links at once. Upon the issue of this command, the GSM will go back to Not Configured state and all the links will transition to Not In Group state.

Command Parameters



Byte Sequence	Parameter Name	Default	Description
1	Group ID	NA	The physical group ID (0~3). The physical group to be deleted.

Command Reply



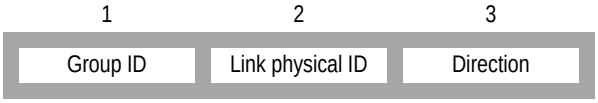
Byte Sequence	Reply Name	Description
1	Ack	0: Acknowledge; 1: Invalid parameter (length of the command is incorrect or Group ID is over 3); Others: Internal error. The chip should be reset.

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Table-35 RecoverLink Command (Encoding: 14H)

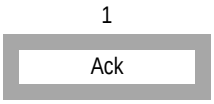
This command is used to tell the IDT82V2604 that a link is no longer in fault state or cancel the inhibition made by “DeactLink” command. This command should combine with a “StartLASR” command in order to recover the link physically.

Command Parameters



Byte Sequence	Parameter Name	Default	Description
1	Group ID	NA	The physical group ID (0~3). The physical group that contains the link to be recovered by this command.
2	Link physical ID	NA	0~3 The physical link to be recovered. The link should belong to the group, and was previously deactivated.
3	Direction	NA	0: Rx; 1: Tx; 2: Both Note1: If the group is in symmetry mode, both links should be recovered; Note2: If the value exceeds 2, IMAOS will work improperly.

Command Reply



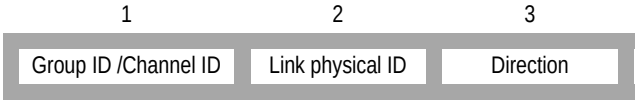
Byte Sequence	Reply Name	Description
1	Ack	0: OK; 1: Invalid parameter; 2: The link does not belong to that group; Others: Internal error. The chip should be reset.

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Table-36 DeleteLink Command (Encoding: 15H)

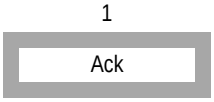
This command is used to delete a link from a group.

Command Parameters



Byte Sequence	Parameter Name	Default	Description
1	Group ID /Channel ID	NA	The physical group ID (0~3) or Channel ID (0~3). The physical group that contains the link to be deleted or Channel ID of the UNI link to be deleted.
2	Link physical ID	NA	0~3 Physical link to be deleted. The link should belong to the group.
3	Direction	NA	0: Rx; 1: Tx; 2: Both Note1: If the group is in symmetry mode, both directions are deleted and the direction value is ignored. If it is a UNI link, this parameter is ignored. Note2: If the value exceeds 2, IMAOS will work improperly.

Command Reply



Byte Sequence	Reply Name	Description
1	Ack	0: Acknowledge; 1: Invalid parameter; 2: The link does not belong to that group; Others: Internal error. The chip should be reset. After the link has both ends deleted, the link is in UNI mode, which is the default Work Mode of a link. The “GetLink-State” command can be used to poll the link state.

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Table-37 DeactLink Command (Encoding: 16H)

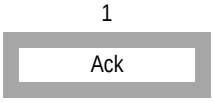
This command is to make a link go to Unusable state due to user defined fault condition or that user just wants to inhibit it.

Command Parameters



Byte Sequence	Parameter Name	Default	Description
1	Group ID	NA	The physical group ID (0~3) The physical group that contains the link to be deactivated by this command.
2	Link physical ID	NA	0~3 Physical link to be deactivated. The link should belong to the group. Note: If the value exceeds 3, the performance cannot be guaranteed.
3	Reason	NA	0: Inhibition; 1: Fault
4	Direction	NA	0: Rx; 1: Tx; 2: Both Note1: If the group is in symmetry mode, both directions are deactivated and the direction value is ignored. Note2: If the value exceeds 2, IMAOS will work improperly.

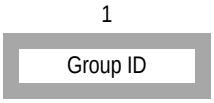
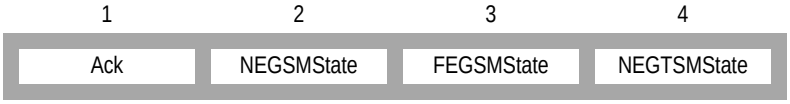
Command Reply



Byte Sequence	Reply Name	Description
1	Ack	0: Acknowledge; 1: Invalid parameter; 2: The link does not belong to that group; Others: Internal error. The chip should be reset.

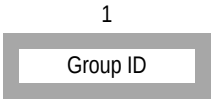
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Table-38 GetGroupState Command (Encoding: 17H)

Command Parameters		
		
Byte Sequence	Parameter Name	Description
1	Group ID	The physical group ID (0~3).
Command Reply		
		
Byte Sequence	Reply Name	Description
1	Ack	0: Acknowledge; 1: Invalid parameter; 2: Information not available; Others: Internal error. The chip should be reset. Note: If Ack is not equal to 0, values for the following fields will not be returned.
2	NEGSMState	Bits 3:0: NE Group State 0000: Start-up; 0001: Start-up-Ack; 0010: Config-Aborted - Unsupported M; 0011: Config-Aborted - Incompatible Group Symmetry; 0100: Config-Aborted - Unsupported IMA Version; 0101, 0110: Reserved for other Config-Aborted reasons in a future version of the IMA specification; 0111: Config-Aborted - Other reasons; 1000: Insufficient-Links; 1001: Blocked; 1010: Operational; Others: Reserved for later use in a future version of the IMA specification.
3	FEGSMState	Bits 3:0: FE Group State 0000: Start-up; 0001: Start-up-Ack; 0010: Config-Aborted - Unsupported M; 0011: Config-Aborted - Incompatible Group Symmetry; 0100: Config-Aborted - Unsupported IMA Version; 0101, 0110: Reserved for other Config-Aborted reasons in a future version of the IMA specification; 0111: Config-Aborted - Other reasons; 1000: Insufficient-Links; 1001: Blocked; 1010: Operational; Others: Reserved for later use in a future version of the IMA specification.
4	NEGTSMState	0: GTSM is down; 1: GTSM is up. NE GTSM state.

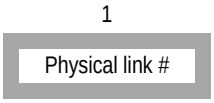
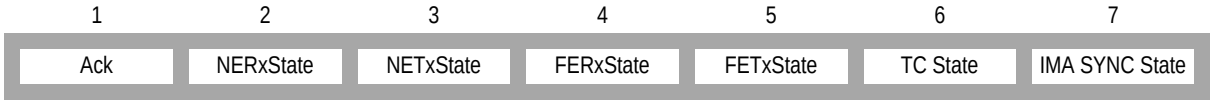
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Table-39 GetGroupDelayInfo Command (Encoding: 18H)

Command Parameters		
		
Byte Sequence	Parameter Name	Description
1	Group ID	The physical group ID (0~3).
Command Reply		
		
Byte Sequence	Reply Name	Description
1	Ack	0: Acknowledge; 1: Invalid parameter; 2: The info is not available; Others: Internal error. The chip should be reset. Note: If Ack is not equal to 0, the value for the following field will not be returned.
2-3	MaxDiffDelayOf-GroupLinks (cells)	The maximum delay value between any two links in that group. (MSB byte first)

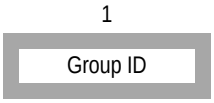
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Table-40 GetLinkState Command (Encoding: 19H)

Command Parameters		
		
Byte Sequence	Parameter Name	Description
1	Physical link #	0~3 The # of the physical link.
Command Reply		
		
Byte Sequence	Reply Name	Description
1	Ack	0: Acknowledge; 1: Invalid parameter; Others: Internal error. The chip should be reset. Note1: For a UNI link, only the TC State value is meaningful. Other values are all meaningless. Note2: If Ack is not equal to 0, values for the following fields will not be returned.
2	NERxState	0x00: not in any group; 0x01: Unusable-No-reason; 0x02: Unusable-Fault; 0x03: Unusable-Misconnected; 0x04: Unusable-Inhibited; 0x05: Unusable-Failed; 0x06: Usable; 0x07: Active. The NE Rx LSM State.
3	NETxState	The same as above. The NE Tx LSM State.
4	FERxState	The same as above. The FE Rx LSM State.
5	FETxState	The same as above. The FE Tx LSM State.
6	TC State	Bit2: 0: Not TC sync; 1: TC sync. Other bits: Don't Care
7	IMA Sync State	Bit5: 0: Not IMA sync state; 1: IMA sync state. Other bits: Don't Care

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Table-41 GetGrpPerf Command (Encoding: 1AH)

Command Parameters		
		
Byte Sequence	Parameter Name	Description
1	Group ID	The physical group ID (0~3).
Command Reply		
		
Byte Sequence	Reply Name	Description
1	Ack	0: Acknowledge; 1: Invalid parameter; 2: Info not available; Others: Internal error. The chip should be reset. Note: If Ack is not equal to 0, the value for the following field will not be returned.
2-3	Value	value of GR-UAS-IMA (For detailed definition, refer to Table-51) (MSB byte first) If Ack is equal to 0, the value of IMAGrpUnavaiSec will be returned. If the performance parameter is not retrieved after a long period, it might reach the maximum value. In this case, the value is held. If Ack is not 0, the value will be 0.

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Table-42 GetLinkPerf Command (Encoding: 1BH)

Command Parameters



Byte Sequence	Parameter Name	Description
1	Physical link #	0~3 The # of the physical link.
2	Type	The performance types (For detailed description of these performance types, please refer to Table-51):

Performance Type	Parameters
0	SES-IMA
	SES-IMA-FE
	UAS-IMA
	UAS-IMA-FE
1	Tx-UUS-IMA
	Rx-UUS-IMA
	Tx-UUS-IMA-FE
	Rx-UUS-IMA-FE
2	OCD_TC
	HCS_ERR_TC
	IV-IMA
3	Rx-Stuff-IMA
	Tx-Stuff-IMA
	OIF-IMA

Command Reply



Byte Sequence	Reply Name	Description
1	Ack	0: Acknowledge; 1: Invalid parameter; 2: Info not available; Others: Internal error. The chip should be reset. Note: If Ack is not equal to 0, the value for the following field will not be returned.

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Table-42 GetLinkPerf Command (Encoding: 1BH) (Continued)

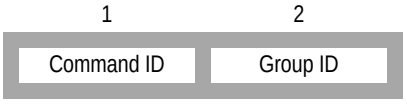
<table>
<tr>
<td>2-10</td>
<td>Value</td>
<td>The counter value of the performance parameter according to Type (MSB first).
The returned value occupies 9 bytes. Different parameters take different number of bytes.
<table>
<tr><th>Performance Type</th><th>Parameters</th><th>Bytes</th></tr>
<tr><td rowspan="5">0</td><td>SES-IMA</td><td>2</td></tr>
<tr><td>SES-IMA-FE</td><td>2</td></tr>
<tr><td>UAS-IMA</td><td>2</td></tr>
<tr><td>UAS-IMA-FE</td><td>2</td></tr>
<tr><td>0</td><td>1</td></tr>
<tr><td rowspan="5">1</td><td>Tx-UUS-IMA</td><td>2</td></tr>
<tr><td>Rx-UUS-IMA</td><td>2</td></tr>
<tr><td>Tx-UUS-IMA-FE</td><td>2</td></tr>
<tr><td>Rx-UUS-IMA-FE</td><td>2</td></tr>
<tr><td>0</td><td>1</td></tr>
<tr><td rowspan="3">2</td><td>OCD_TC</td><td>3</td></tr>
<tr><td>HCS_ERR_TC</td><td>3</td></tr>
<tr><td>IV-IMA</td><td>3</td></tr>
<tr><td rowspan="3">3</td><td>Rx-Stuff-IMA</td><td>3</td></tr>
<tr><td>Tx-Stuff-IMA</td><td>3</td></tr>
<tr><td>OIF-IMA</td><td>3</td></tr>
</table>
Note: If the performance parameters are not retrieved after a long period, they might reach the maximum value. In this case, the values are held.</td>
</tr>
</table>

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Table-43 GetConfigPara Command (Encoding: 1CH)

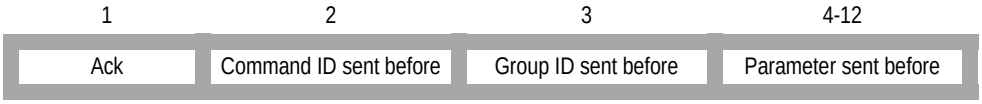
This command is used to get the parameters as shown in the parameter list of a command (designated by Command ID), i.e., get the configured information or default information as a command's parameter list designated.

Command Parameters



Byte Sequence	Parameter Name	Description
1	Command ID	The command encoding of the commands below: • ConfigDev • ConfigUTOPIAIF • ConfigLoopMode • ConfigGroupPara • ConfigGroupInterface • ConfigGroupWorkMode • ConfigGSMTimers • ConfigTRL • ConfigIFSMpara Note: If the value is not one from above, IMAOS will work improperly.
2	Group ID	The Group ID (If command ID is 'ConfigDev', do not care this parameter, that is, any value will do.) If the command (such as ConfigDev command) has no Group ID parameter, this field should be set to 0 and will be ignored by the embedded controller.

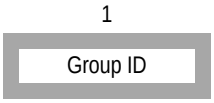
Command Reply



Byte Sequence	Reply Name	Description
1	Ack	0: Acknowledge; 1: Invalid parameter; 2: Info not available; Others: Internal error. The chip should be reset. Note1: If Ack is not equal to 0, values for the following fields will not be returned. Note2: If Ack for this command is equal to 0 but the Ack for the command sent before is not equal to 0, values for the following fields are undetermined.
2	Command ID sent before	The command ID sent before.
3	Group ID sent before	The Group ID sent before. For ConfigDev command, this byte has no meaning.
4-12	Parameter sent before	This field contains all the parameters that were sent previously excluding the Group ID, as it is returned in byte 3. The length of this field depends on the Command ID and the sequence is the same as the input.

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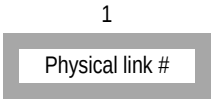
Table-44 GetGrpWorkingPara Command (Encoding: 1DH)

Command Parameters		
		
Byte Sequence	Parameter Name	Description
1	Group ID	The physical group ID (0~3).
Command Reply		
		
Byte Sequence	Reply Name	Description
1	Ack	0: Acknowledge; 1: Invalid parameter; 2: Info not available; Others: Internal error. The chip should be reset. Note: If Ack is not equal to 0, values for the following fields will not be returned.
2	NE IMA ID	The IMA ID in the ICP cell transmitted to the FE from the NE.
3	FE IMA ID	The IMA ID in the ICP cell that the NE received from the FE.
4	M_{tx}	The IMA frame length the NE is using.
5	M_{rx}	The IMA frame length the FE is using.
6	Version now used	0: Both ends are 1.1; 1: The FE is 1.0 and the NE is 1.0 compatible.
7	Tx TRL	The physical link # used for Tx TRL.
8	Rx TRL	The physical link # the FE used for TRL.

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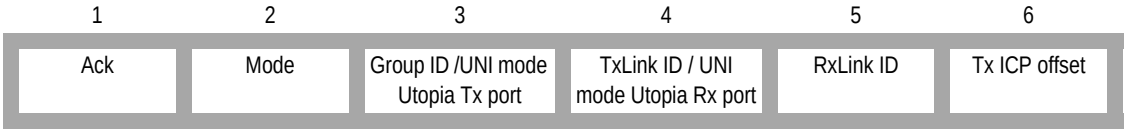
Table-45 GetLinkWorkingPara Command (Encoding: 1EH)

Command Parameters



Byte Sequence	Parameter Name	Description
1	Physical link #	0~3. The # of the physical link.

Command Reply

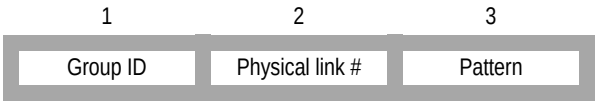


Byte Sequence	Reply Name	Description
1	Ack	0: Acknowledge; 1: Invalid parameter; 2: Info not available; Others: Internal error. The chip should be reset. Note: If Ack is not equal to 0, values for the following fields will not be returned.
2	Mode	0: UNI; 1: IMA mode – Only Rx used; 2: IMA mode – Only Tx used; 3: IMA mode – Both Tx and Rx are used.
3	Group ID /UNI mode Utopia Tx port	If Mode is IMA, this value means which physical group at the NE the link belongs to; If mode is UNI, this value is the Utopia Tx port address.
4	TxLink ID / UNI mode Utopia Rx port	If Mode is IMA, this value means the logical link # assigned (0~31), If mode is UNI, this value is the Utopia Rx port address.
5	RxLink ID	The logical link ID the FE is using.
6	Tx ICP offset	0~255 (in IMA mode; not used in UNI mode).

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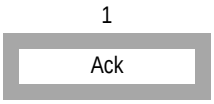
Table-46 StartTestPattern Command (Encoding: 1FH)

Command Parameters



Byte Sequence	Parameter Name	Description
1	Group ID	The physical group ID (0~3)
2	Physical link #	0~3 The # of the physical link.
3	Pattern	0~FFH, and FFH is not recommended. This byte is used to define the pattern for testing purpose.

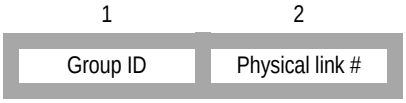
Command Reply



Byte Sequence	Reply Name	Description
	Ack	0: Acknowledge; 1: Invalid parameter; 2: The link does not belong to the group; Others: Internal error. The chip should be reset.

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Table-47 GetLoopedTestPattern Command (Encoding: 20H)

Command Parameters		
		
Byte Sequence	Parameter Name	Description
1	Group ID	The physical group ID (0~3)
2	Physical link #	0~3 The # of the physical link.
Command Reply		
		
Byte Sequence	Reply Name	Description
Ack	1	0: Acknowledge; 1: Invalid parameter; 2: The link does not belong to the group; Others: Internal error. The chip should be reset. Note: If Ack is not equal to 0, the value for the following field will not be returned.
Pattern	1	The FE looped test pattern over that link

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Table-48 StopTestPattern Command (Encoding: 21H)

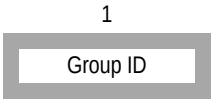
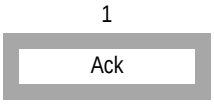
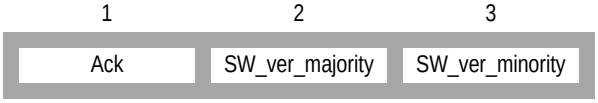
Command Parameters		
		
Byte Sequence	Parameter Name	Description
1	Group ID	The physical group ID (0~3)
Command Reply		
		
Byte Sequence	Reply Name	Description
1	Ack	0: OK; 1: Invalid parameter; Others: Internal error. The chip should be reset.

Table-49 GetVersionInfo Command (Encoding: 22H)

Command Parameters		
No.		
Command Reply		
		
Byte Sequence	Reply Name	Description
1	Ack	0: OK; Others: Internal error. The chip should be reset. Note: If Ack is not equal to 0, values for the following fields will not be returned.
2	SW_ver_majority	The integer part of the IMAOS version. For example, if the current version is 1.12, the returned value will be 1.
3	SW_ver_minority	The fractional part of the IMAOS version. For example, if the current version is 1.12, the returned value will be 12.

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6 IMA OPERATION

This chapter is a brief introduction of how a group and links are configured, started, inhibited, deleted and so on.

6.1 IMA INITIALIZATION

ConfigDev command is the first command to be issued to initialize the device. If this command is not issued, the default value will be used.

6.2 CONFIGURE A GROUP

After a group is configured, an ID (IMA ID) is allocated to a physical group, links are assigned to that group and other parameters needed for the group's proper operation are set. The IMA ID should not be changed during the whole life cycle of the group except that the group is restarted. Table-50 is the list of group parameters that should be configured.

Table-50 Parameters for IMA Group Configuration

Parameter Name	Description
Group ID	The physical group ID used for this IMA group.
NE IMA ID	The IMA group logical ID#.
M for Tx (M_{tx})	The frame length that the NE Tx would like to use.
Acceptable M for Rx (M_{rx})	The frame length proposed by the FE Tx that the NE Rx can accept.
Max delay compensation value (cells)	The maximum different link delay value a group is expected to have.
Version Backward Compatibility	Whether IMA 1.0 is supported
TxUtopia port	The Utopia address where ATM traffic comes from
RxUtopia port	The Utopia address where ATM traffic goes
Symmetry mode	The group link's configuration and operation mode.
Timing clock mode	The transmission timing clock mode.
Stuff mode	The SICP insertion method.
Stuff adv mode	The stuff pre-notify mode. Valid value is 1 or 4.
Timer for GSM start up Ack	This is the timer for GSM to return from start-up Ack to start-up state when there is no response from the FE.
Timer for GSM Configure Abort	This is the timer for GSM to return from start-up Abort state to start-up state.
Timer for GSM to report Rx=active	This is the timer for Group wide start-up procedure to report Rx=Active state.
Timer for GSM to report Tx=active	This is the timer for Group wide start-up procedure to report Tx=Active state.
Tx TRL	The transmit timing reference link. (Physical ID)
Alpha	The number of consecutive invalid ICP cells for the IFSM state machine to exit SYNC state. Default value is 2.
Beta	The number of consecutive errored ICP cells for the IFSM state machine to exit SYNC state. Default value is 2.
Gamma	The number of consecutive valid ICP cells for the IFSM state machine to enter SYNC state. Default value is 1.
P_{tx}	The minimum number of active Tx links for the group to enter operational state
P_{rx}	The minimum number of active Rx links for the group to enter operational state
All the Tx links' physical IDs	The physical links' ID used for transmission.
All the Tx links' logical IDs	The logical link ID for each Tx link.
All the Rx links' physical IDs	The physical links' ID used for receiving.
All Tx links' line interface Work Mode	The line interface Work Mode for each Tx link.
All Rx links' line interface Work Mode	The line interface Work Mode for each Rx link.
All Tx links' line interface clock mode	The line interface clock mode for each Tx link.
All Rx links' line interface Work Mode	The line interface clock mode for each Rx link.

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Table-50 Parameters for IMA Group Configuration (Continued)

Tx links' ICP offsets	The ICP cell location within the IMA frame transmitted over each Tx link.
All Tx links' backup property	The Tx link added to the group is a backup link or not.
All Rx links' backup property	The Rx link added to the group is a backup link or not.

6.3 START UP A GROUP

A group can be started by StartGroup command. At IMA group start-up, the NE and the FE exchange their configuration parameters. When both ends accept the parameters proposed by the other end, they enter an intermediate state to wait for P_{tx} and P_{rx} links to enter active state. The group can then enter operational state.

6.4 INHIBIT A GROUP/NOT INHIBIT A GROUP

The inhibition of a group is the shut down of the group for a reason other than insufficient links.

A group can be inhibited by InhibitGrp command.

A group inhibition state can be cancelled by NotInhibitGrp command.

6.5 ADD LINKS TO A GROUP THAT IS IN OPERATIONAL STATE

The LASR (Link Addition and Slow Recovery) procedure is to be started when new links are to be inserted or links are to be recovered from a group.

The LASR procedure can be started by StartLASR command.

6.6 DELETE LINKS

A link can be removed by DeleteLink command. The deletion procedure can be initiated from both the Tx and Rx side.

6.7 DEACTIVATE AND RECOVER LINKS

Links are deactivated because of link fault, failure (Rx failed) or inhibition while links are recovered because defect no longer exists or inhibition is cancelled.

The deactivation-recovering of a link is done by the IDT82V2604 automatically according to the FE notification (Remote Failure Indicator in ICP cell) or by the embedded controller (issue commands like DeactLink and RecoverLink commands) due to link fault or inhibition or no longer link fault or inhibition.

6.8 RESTART A GROUP

After a group is started, the parameters of the group can be reconfigured at any time, which will cause the group to be restarted automatically. However, a group can also be restarted by RestartGrp command. When a group is restarted, the GSM transits to Start-up state from any other states except Not Configured state. If the GSM is in Operational state, the group may be blocked and all the links be inhibited before restart.

6.9 DELETE A GROUP

When a group is deleted from any other state by DeleteGrp command, the GSM enters Not Configured state and all the links belonging to that group will also be deleted and unassigned.

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7 PMON (PERFORMANCE MONITORING)

The PMON module uses counters for performance monitoring and failure/alarms integration. Table-51 shows the performance parameters that the IDT82V2604 implements. Table-53 lists the failure/alarm signals sent by alarm messages.

Table-51 The PMON Parameters

Parameter	Link/Group	Definition	Retrieve
SES-IMA	Link	Count of NE Severely Errored Seconds.	GetLinkPerf command
SES-IMA-FE	Link	Count of FE Severely Errored Seconds.	
UAS-IMA	Link	Count of NE UnAvailable Seconds.	
UAS-IMA-FE	Link	Count of FE UnAvailable Seconds.	
Tx-UUS-IMA	Link	Count of NE Tx Unusable seconds.	
Rx-UUS-IMA	Link	Count of NE Rx Unusable seconds.	
Tx-UUS-IMA-FE	Link	Count of FE Tx UnUsable Seconds.	
Rx-UUS-IMA-FE	Link	Count of FE Rx UnUsable Seconds.	
OCD_TC	Link	Count of link out of cell delineation entrances.	
HCS_ERR_TC	Link	Count of Cell header sequence error.	
IV-IMA	Link	Count of ICP Violations. Three types of ICP invalid signals will cause the IV-IMA. They are: Errored ICP, invalid ICP and missing ICP. (See Table-52 for definitions). The IV-IMA is counted only during Non-SES-IMA or Non-UAS-IMA period.	
Rx-Stuff-IMA	Link	Count of received Stuff ICP cells over one link.	
Tx-Stuff-IMA	Link	Count of transmitted Stuff ICP cells over one link.	
OIF-IMA	Link	Count of Out of IMA Frame anomalies except during SES-IMA or UAS-IMA conditions.	
GR-UAS-IMA	Group	Count of Seconds when GTSM is down.	GetGrpPerf command

Table-52 Definitions of Different ICP Cells

ICP Cell Type	Definition
Errored ICP	Cell with a HEC or CRC-10 error at expected ICP frame position and is not a Missing ICP cell.
Invalid ICP	Cell with good HEC and CRC-10 and CID=ICP at expected frame position but with one of the following unexpected errors: • Unexpected IMA label • Unexpected LID • Unexpected IMA ID • Received M≠expected M • Unexpected IMA frame sequence number • Unexpected ICP cell offset
Missing ICP	Cell located at ICP cell location with: • No HEC error but without IMA OAM cell header or • No HEC error and with IMA OAM cell header but the CID≠ ICP.

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Table-53 Failure/Alarm Signals

Sequence	Name	Link /Group	Implement	Definition
01H	LCD	Link	SW	Loss of Cell Delineation.
02H	LIF	Link	SW	Loss of IMA Frame.
03H	LODS	Link	SW	Link Out of Delay Synchronization.
04H	RFI-IMA	Link	SW	Persistence of an RDI-IMA defect at the NE.
05H	Tx-Unusable-FE	Link	SW	When the FE reports Tx-Unusable.
06H	Rx-Unusable-FE	Link	SW	When the FE reports Rx-Unusable.
07H	Start-up-FE	Group	SW	When the FE is starting-up (the declaration of this failure alarm may be delayed to ensure the FE remains in Start-up).
08H	Config-Aborted	Group	SW	When the FE tries to use unacceptable configuration parameters.
09H	Config-Aborted-FE	Group	SW	When the FE reports unacceptable configuration parameters.
0AH	Insufficient-Links	Group	SW	When less than P_{tx} transmit or P_{rx} receive links are Active.
0BH	Insufficient-Links-FE	Group	SW	When the FE reports that less than P_{tx} transmit or P_{rx} receive links are Active.
0CH	Blocked-FE	Group	SW	When the FE reports that it is blocked.
0DH	GR-Timing-Mismatch	Group	SW	When the FE transmit clock mode is different from the NE transmit clock mode.

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8 IMAOS04_SLAVE

The previous chapters 4, 5, 6 and 7 are specific to IMAOS04. Details about IMAOS04_Slave are provided in this chapter.

When IMAOS04_Slave is downloaded, the device supports the Group Auto Detect function and operates in Slave Mode.

8.1 GROUP AUTO DETECT

The group auto detect function can be used to configure and start a group from one end while forcing the other end's group to follow this end's group configuration and start-up procedure, that is, the other end's group can be brought into operational state automatically. The two ends are called Master Side and Slave Side separately.

8.1.1 MASTER SIDE

The Master Side should download IMAOS04 and work in symmetry mode. Up to 4 groups can be started at the Master side.

The configuration of the Master Side is the same as that in normal Work Mode.

8.1.2 SLAVE SIDE

The Slave Side should download IMAOS04_Slave.

After power-on or reset, the Slave Side should be initialized by issuing the DeviceInitial, ConfigSlaveFrame, ConfigUtopiaIF and GroupInitial commands. Only after the Slave Side has been initialized will the Slave Side start to detect the far end's start-up procedure.

After the far end has started up, the Slave Side will be brought into operational state automatically without any need of local group configuration and management.

8.2 PROGRAMMING INFORMATION FOR IMAOS04_SLAVE

8.2.1 COMMAND TYPES

Refer to 5.1 Command Types.

8.2.2 COMMAND ENCODING

Table-54 Command Encoding

Command Encoding	Command Name
01H	DeviceInitial
02H	ConfigSlaveFrame
03H	ConfigUtopiaIF
22H	GetVersionInfo
23H	GroupInitial

8.2.3 COMMAND DESCRIPTION

Each command description contains two parts: the Command Parameters and the Command Reply. In the Command Parameters part, a figure is used to illustrate the byte sequence of the parameters. All the parameters description are listed below the figure. In the Command Reply part, a figure is used to illustrate the reply sequence in the reply message. The reply description is listed below the figure. For detailed information about the packet of command message and reply message, refer to page 30.

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Table-55 DeviceInitial Command (Encoding: 01H)

This is the first command to be issued. If this command is not issued, the default value will be used.

Command Parameters

1-2	3	4	5	6	7	8
SysClk	T_{in}	T_{exit}	No	TCWorkMode	TCAlpha&Delta	TCLCD_Threshold

Byte Sequence	Parameter Name	Default	Description
1-2	SysClk	4E20H	SysClk=Frequency of System Clock (Hz)/1000. For example, if the system clock is 20 MHz, this value would be 20000. Unit: sys-ticks in 1 ms (MSB first) Note: Wrong configuration will make IMAOS_Slave's timer work improperly.
3	T_{in}	2H	Timer of entering failure alarm state. When a defect persists for a period set by this timer, the IDT82V2604will enter failure alarm state. Unit: 250 ms
4	T_{exit}	0AH	Timer of exiting failure alarm state. If a defect no longer exists for a period set by this timer, the IDT82V2604 will exit failure alarm state. Unit: 250 ms
5	No	0H	Reserved. Write 0 to this field.
6	TCWorkMode	7H	Bit Position / Description 7~3: Don't Care 2: 1: Enable Tx TC scrambling (default); 0: Disable Tx TC scrambling 1: 1: Enable Rx TC HEC error correct control (default); 0: Disable Rx TC HEC error correct control 0: 1: Enable Rx TC de-scrambling (default); 0: Disable Rx TC de-scrambling
7	TCAlpha&Delta	67H	Bit Position / Description 7-4: Delta value. Valid is 0~15. 3-0: Alpha value. Valid is 0~15. Alpha value is the number of consecutive incorrect HEC fields for the Rx cell synchronization state machine to exit sync state. Delta value is the number of consecutive correct HEC fields for the Rx cell synchronization state machine to enter sync state.
8	TCLCD_Threshold	68H	0~255 LCD threshold. If the OCD anomaly persists for the time set by this parameter, LCD defect will be reported. Unit: one cell's transmission time

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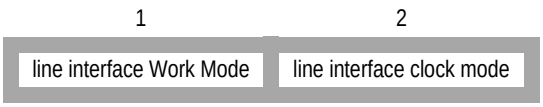
Table-55 DeviceInitial Command (Encoding: 01H) (Continued)

Command Reply		
		
Byte Sequence	Reply Name	Description
1	Ack	0: OK; 1: Invalid parameter (length of the command is incorrect); Others: Internal error. The chip should be reset.

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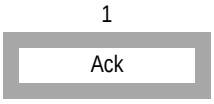
Table-56 ConfigSlaveFrame Command (Encoding: 02H)

Command Parameters



Byte Sequence	Parameter Name	Default	Description
1	line interface Work Mode	0FH	Mode0~mode15 Line interface Work Mode for all the links.
2	line interface clock mode	0H	0: Common Clock Mode; 1: Independent Clock Mode Line interface clock input mode for all the links. Line interface mode7~mode10 and mode14~mode15 cannot be used in Independent Clock Mode.

Command Reply

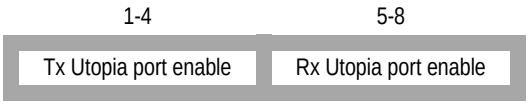


Byte Sequence	Reply Name	Description
1	Ack	0: OK; 1: Invalid parameter (length of the command is incorrect). Others: Internal error. The chip should be reset.

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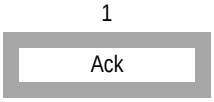
Table-57 ConfigUtopiaIF Command (Encoding: 03H)

Command Parameters



Byte Sequence	Parameter Name	Default	Description
1-4	Tx Utopia port enable	00000000H	Every bit of the 4 bytes enables a Utopia Tx port (MSB byte first, LSB byte last). 0: Disable the port; 1: Enable the port This 4 bytes parameter enables or disables each of the 31 Utopia port (port 31 is reserved and should not be used). The 4 bytes can be regarded as a sequence of 32 bits. The most significant bit in byte 1 (the first byte sent to embedded controller) is bit 31. The least significant bit of byte 4 (the last byte sent) is bit 0.
5-8	Rx Utopia port enable	00000000H	Every bit of the 4 bytes enables a Utopia Rx port (MSB byte first, LSB byte last). 0: Disable the port; 1: Enable the port The meaning of this parameter is similar to the Utopia Tx port enable field. See above.

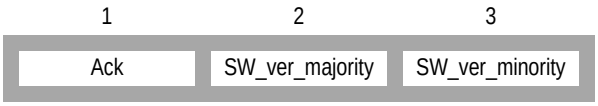
Command Reply



Byte Sequence	Reply Name	Description
1	Ack	0: OK; 1: Invalid parameter (length of the command is incorrect); Others: Internal error. The chip should be reset.

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Table-58 GetVersionInfo Command (Encoding: 22H)

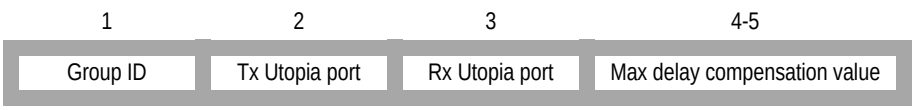
Command Parameters		
No.		
Command Reply		
		
Byte Sequence	Reply Name	Description
1	Ack	0: OK; Others: Internal error. The chip should be reset. Note: If Ack is not equal to 0, values for the following fields will not be returned.
2	SW_ver_majority(1)	The integer part of the version. For example, if the current version is 2.12, the returned value will be 2.
3	SW_ver_minority	The fractional part of the version. For example, if the current version is 2.12, the returned value will be 12.

1. For IMAOS04, the returned value is an odd number. For IMAOS04_Slave, the returned value is an even number.

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Table-59 GroupInitial Command (Encoding: 23H)

Command Parameters



Byte Sequence	Parameter Name	Default	Description
1	Group ID	NA	The physical group ID (0~3). The Group ID follows the IMA ID of the Master Side. Note that the IMA ID of the Master Side should not exceed 3.
2	Tx Utopia port	1FH	0~30 The Utopia port address for data transmit. Port 31 is reserved and should not be used. Note: The upper 3 bits are Don't Care.
3	Rx Utopia port	1FH	0~30 The Utopia port address for data receive. Port 31 is reserved and should not be used. Note: The upper 3 bits are Don't Care.
4-5	Max delay compen-sation value	NA	0~1024 cells This is the maximum cells delay that can be tolerated. This value is constrained by the size of the external SRAM and it shall be no more than 1024 cells. Refer to 3.4 SRAM Interface. Note: If the value exceeds 1024, IMAOS_Slave will work improperly.

Command Reply



Byte Sequence	Reply Name	Description
1	Ack	0: OK; 1: Invalid parameter; Others: Internal error. The chip should be reset.

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9 JTAG TEST ACCESS PORT

9.1 TAP BUS SIGNALS

The interface from the board to the on-chip Test Access Port is the TAP bus, which consists of five signals:

- The standard bus: TDI, TDO, TCK, TMS.
- $\overline{\text{TRST}}$: Test reset. Reset the TAP controller. The signal is specified as optional in the IEEE spec. $\overline{\text{TRST}}$ is an active low signal that resets all flip-flops of TAP asynchronously.

9.2 INSTRUCTIONS

Meet the IEEE standard [13] which requires at least EXTEST, BYPASS, IDCODE and SAMPLE instructions are implemented. The IDT82V2604 identification code is 104B8067 hexadecimal.

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10 PHYSICAL AND ELECTRICAL CHARACTERISTICS

10.1 ABSOLUTE MAXIMUM RATINGS

Table-60 Absolute Maximum Ratings

Parameter	Min	Max
Storage temperature	-65 °C	+150 °C
Voltage on VDD with reference to GND	-0.3 V	4.6 V
Voltage on input pin	-0.3 V	5.25 V
Voltage on output pin	-0.3 V	VDD+0.3 V
Maximum lead temperature for soldering during 10 s		230 °C
ESD Performance (HBM)	2000 V	
Latch-up current on any pin	100 mA	
Maximum junction temperature		150 °C

10.2 D.C. CHARACTERISTICS

@ TA= -40 to +85°C.

Table-61 D.C. Characteristics

Parameter	Description	Min	Typ	Max	Unit	Test Conditions
VDD	Core Power Supply	2.97	3.3	3.63	V	
V_{OL}	Output Low Voltage			0.40	V	VDD=min, I_{OL}=4 mA or 6 mA(1)
V_{OH}	Output High Voltage	2.4			V	VDD=min, I_{OH}= 4 mA or 6 mA
V_{T+}	Input High Voltage(2)			2.0	V	
V_{T-}	Input Low Voltage	0.83			V	
V_{TH}	Input Hysteresis Voltage	0.17	0.65	1.17	V	
I_{ILPU}	Input Low Current	-20	-55	-200	uA	V_{IL}=GND
I_{IL}	Input Low Current	-1	0	+1	uA	V_{IL}=GND
I_{IH}	Input High Current	-2	0	+2	uA	V_{IH}=+5 V
I_{DDOP1}	Operating current		160		mA	VDD=3.63 V, SYSClk=25 MHz

1. The output driving capacity of all the embedded memory output pins are 4mA while the output driving capacity of all the other output pins are 6mA.

2. All the input pins are schmitt-trigger pins.

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10.3 A.C. CHARACTERISTICS

@ TA=-40 to +85 °C, VDD=3.3 V±10%

10.3.1 OUTPUT LOADING

Default load capacitance on output is 50 pF.

Microprocessor interface and Utopia interface outputs are loaded by 100 pF.

10.3.2 SYSTEM CLOCK AND $\overline{\text{RST}}$ SIGNAL TIMING

Table-62 System Clock and Reset Timing Parameters

Parameter	Description	Min	Max	Unit
tSYSCLK	The system clock cycle time	40	54	ns
D_{SYSCLK}	The system clock duty cycle	40	60	%
$t\overline{RST}$	The $\overline{RST}$ pulse width	1		ms

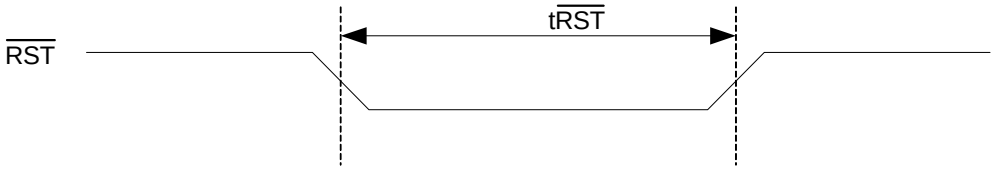


Figure-13 Reset Signal Timing Diagram

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10.3.3 UTOPIA INTERFACE TIMING

Table-63 Utopia Interface Timing Parameters

Parameter	Description	Min	Max	Unit
f_{txCLK}	Utopia Tx interface clock frequency		f_{SYSCLK}(1)	MHz
f_{rxCLK}	Utopia Rx interface clock frequency		f_{SYSCLK}	MHz
tCLAV	TxClav and RxClav valid from rising edge of TxClk and RxClk respectively		20	
tUTS	$\overline{TxEnb}$, TxSOC, TxData and TxAddr to TxClk setup time	6		ns
tUTH	$\overline{TxEnb}$, TxSOC, TxData and TxAddr to TxClk hold time	1		ns
tURCO	RxClav, RxSOC, RxData valid from rising edge of RxClk		20	ns
tURS	RxAddr, $\overline{RxEnb}$ to RxClk setup time	6		ns
tURH	RxAddr, $\overline{RxEnb}$ to RxClk hold time	1		ns
tP	Width of pull-down pulse after TxClav or RxClav is deasserted.	2		ns

1. f_{SYSCLK} is the frequency of the system clock the chip uses.

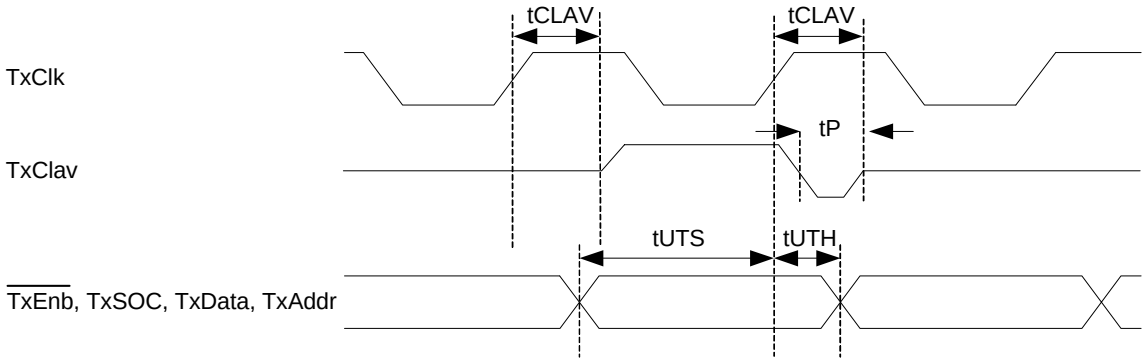


Figure-14 Tx Utopia Interface Timing Diagram

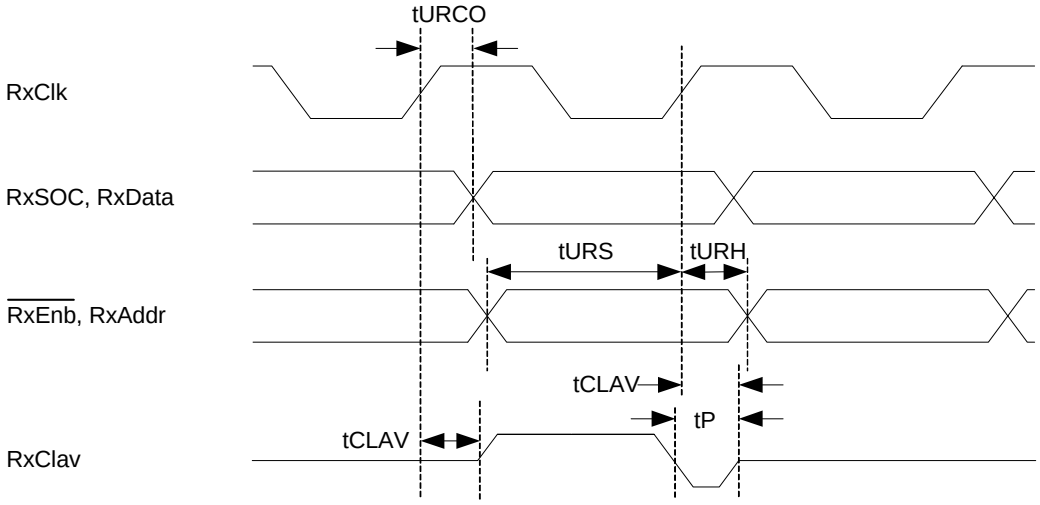


Figure-15 Rx Utopia Interface Timing Diagram

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10.3.4 LINE INTERFACE TIMING

Table-64 Line Interface Timing Parameters

Parameter	Description	Min	Max	Unit
D_{CK}	The TSCK, TSCCK, RSCK and RSCCK clock duty cycle	40	60	%
f_{TSCKE1}	E1 mode transmit direction clock frequency		8.192	MHz
f_{RSCKE1}	E1 mode receive direction clock frequency		8.192	MHz
f_{TSCKT1}	T1 mode transmit direction clock frequency		8.192	MHz
f_{RSCKT1}	T1 mode receive direction clock frequency		8.192	MHz
tFDCO	TSD valid from TSCK		20	ns
tFS	TSF, TSCFS to TSCK set up time; RSD, RSF, RSCFS to RSCK set up time	10		ns
tFH	TSF, TSCFS to TSCK hold time; RSD, RSF, RSCFS to RSCK hold time	5		ns

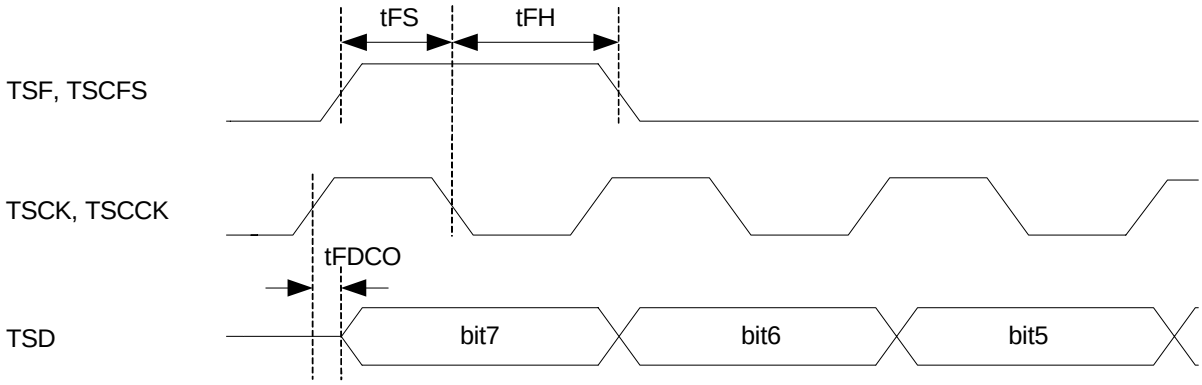


Figure-16 Line Interface Transmit Timing Diagram

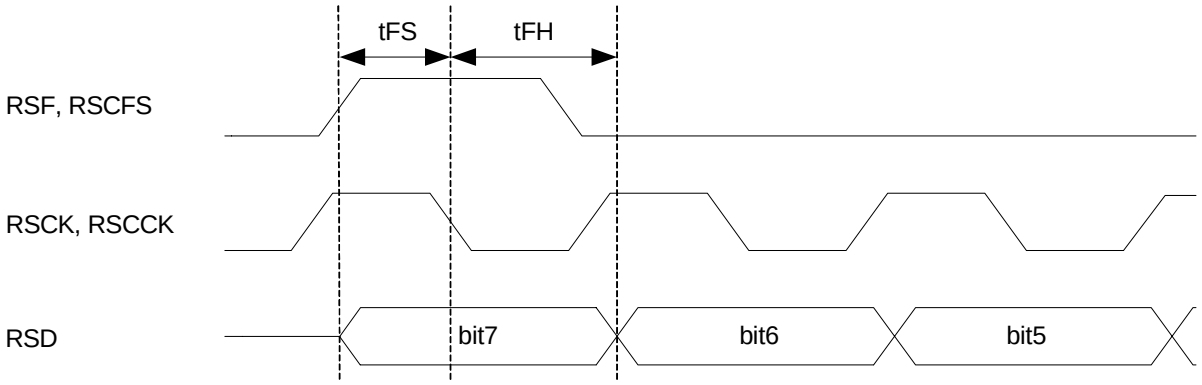


Figure-17 Line Interface Receive Timing Diagram

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10.3.5 MICROPROCESSOR INTERFACE TIMING

10.3.5.1 Interface with Motorola CPU (MPM =0)

Read Cycle Specification

Table-65 Microprocessor Interface Timing Parameter for Motorola CPU Read Cycle

Symbol	Parameter	Min	Max	Unit
tRC	Read cycle time	240		ns
tDW	Valid read signal width	235		ns
tRWV	R/$\overline{W}$ available time after valid read signal falling edge		10	ns
tRWH	R/$\overline{W}$ hold time after valid read signal falling edge	135		ns
tAV	Address available time after valid read signal falling edge		10	ns
tADH	Address hold time after valid read signal falling edge	135		ns
tPRD	Data propagation delay after valid read signal falling edge		205	ns
tDH	Read out data hold time after valid read signal rising edge	5	20	ns
tRecovery	Recovery time from read cycle	5		ns

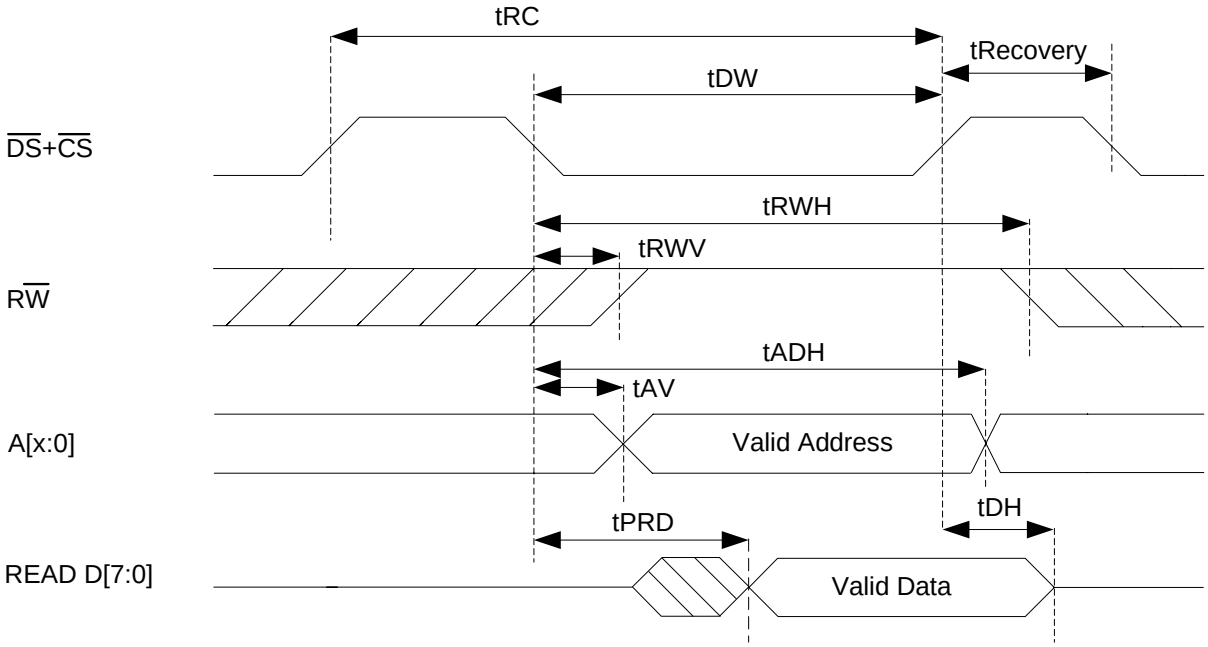


Figure-18 Microprocessor Interface Timing Diagram for Motorola CPU Read Cycle

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Write Cycle Specification

Table-66 Microprocessor Interface Timing Parameters for Motorola CPU Write Cycle

Symbol	Parameter	Min	Max	Unit
tWC	Write cycle time	240		ns
tDW	Valid write signal width	235		ns
tRWV	R/$\overline{W}$ available time after valid write signal falling edge		10	ns
tRWH	R/$\overline{W}$ hold time after valid write signal falling edge	165		ns
tAV	Address available time after valid write signal falling edge		10	ns
tAH	Address hold time after valid write signal falling edge	165		ns
tDV	Data propagation delay after valid write signal falling edge		50	ns
tDHW	Data hold time after valid write signal rising edge	165		ns
tRecovery	Recovery time from write cycle	5		ns

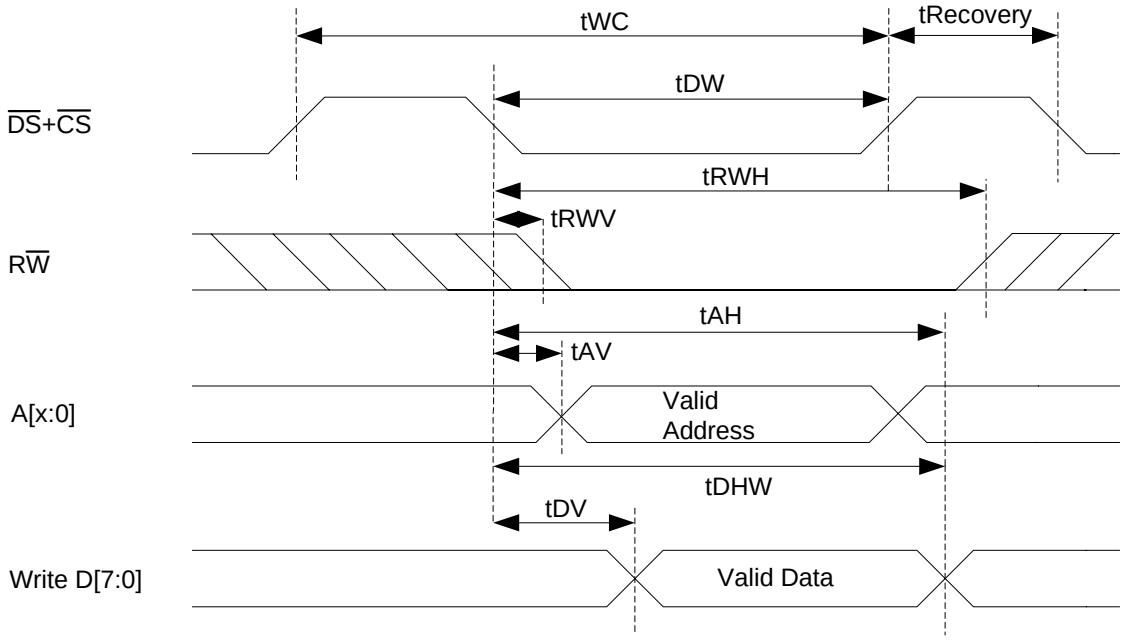


Figure-19 Microprocessor Interface Timing Diagram for Motorola CPU Write Cycle

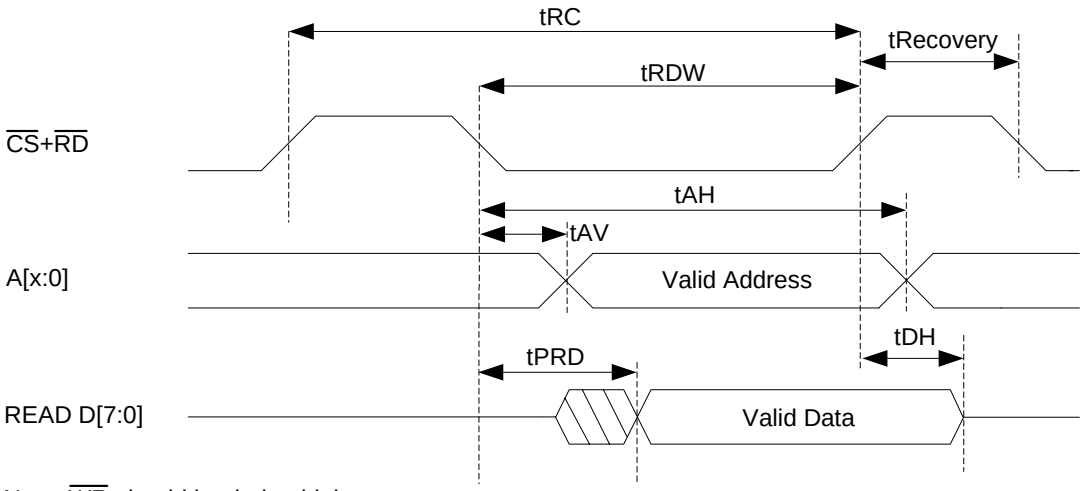
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10.3.5.2Interface with Intel CPU (MPM =1)

Read Cycle Specification

Table-67 Microprocessor Interface Timing Parameter for Intel CPU Read Cycle

Symbol	Parameter	Min	Max	Unit
tRC	Read cycle time	240		ns
tRDW	Valid read signal width	235		ns
tAV	Address available time after valid read signal falling edge		10	ns
tAH	Address hold time after valid read signal falling edge	135		ns
tPRD	Data propagation delay after valid read signal falling edge		205	ns
tDH	Read out data hold time after valid read signal rising edge	5	20	ns
tRecovery	Recovery time from read cycle	5		ns



Note: $\overline{WR}$ should be tied to high

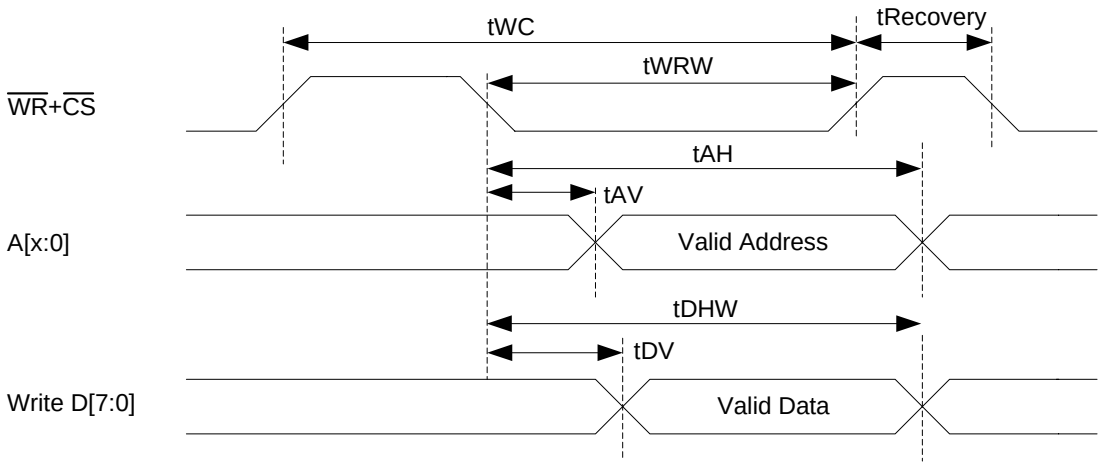
Figure-20 Microprocessor Interface Timing Diagram for Intel CPU Read Cycle

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Write Cycle Specification

Table-68 Microprocessor Interface Timing Parameters for Intel CPU Write Cycle

Symbol	Parameter	Min	Max	Unit
tWC	Write cycle time	240		ns
tWRW	Valid write signal width	235		ns
tAV	Address available time after valid write signal falling edge		10	ns
tAH	Address hold time after valid write signal falling edge	165		ns
tDV	Data available time after valid write signal falling edge		50	ns
tDHW	Data hold time after valid write signal falling edge	165		ns
tRecovery	Recovery time from write cycle	5		ns



Note: RD should be tied to high

Figure-21 Microprocessor Interface Timing Diagram for Intel CPU Write Cycle

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10.3.6 SRAM INTERFACE TIMING

10.3.6.1 Write Cycle Specification

Table-69 SRAM Interface Write Cycle Parameters

Symbol	Description	Min	Max	Unit
tWC	Write cycle time	40		ns
tAS	Address set up time	3	20	ns
tAH	Address hold time	1		ns
tWP	Write pulse width	20		ns
tDW	Data valid to end of write	7		ns
tDH	Data hold time	0		ns

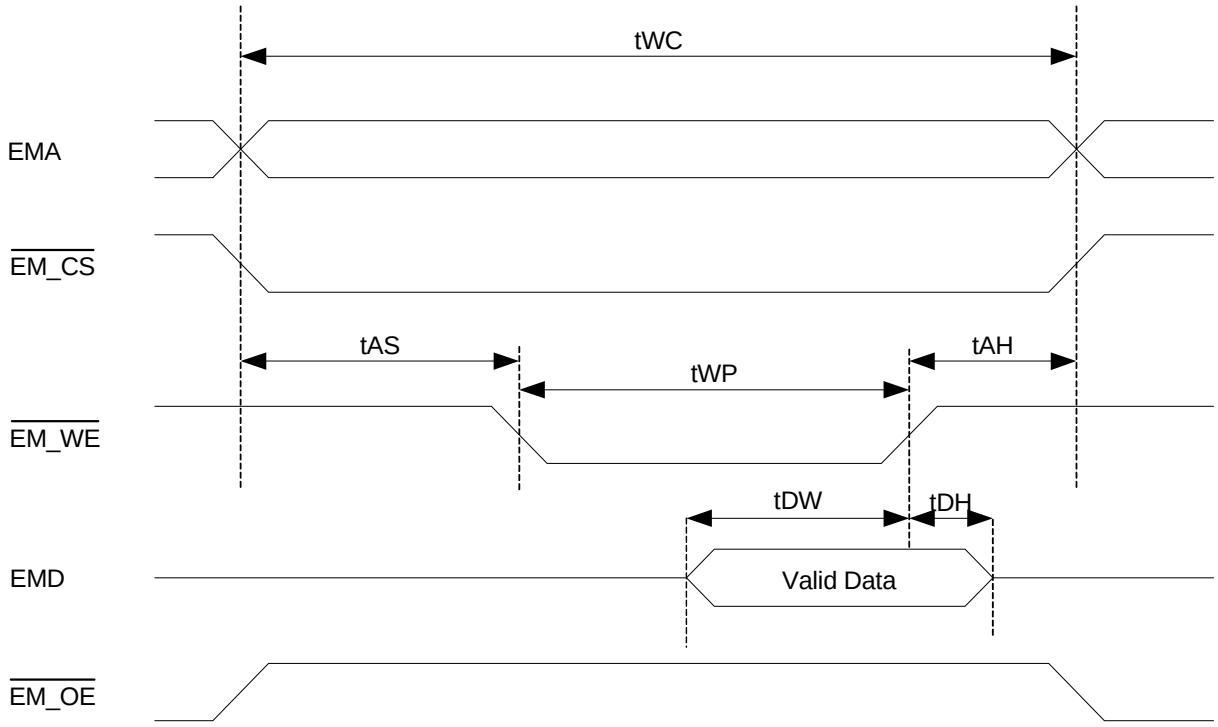


Figure-22 SRAM Interface Timing Diagram for Write Cycle

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10.3.6.2Read Cycle Specification

Table-70 SRAM Interface Read Cycle Parameters

Symbol	Description	Min	Max	Unit
tRC	Read cycle time	40		ns
tAA	Address Access time		20	ns
tCA	$\overline{EM_CS}$ Access time		20	ns
tOA	$\overline{EM_OE}$ Access time		20	
tCHZ	Delay from disabled $\overline{EM_CS}$ to data bus high impedance		7	ns
tOHZ	Delay from disabled $\overline{EM_OE}$ to data bus high impedance		7	ns

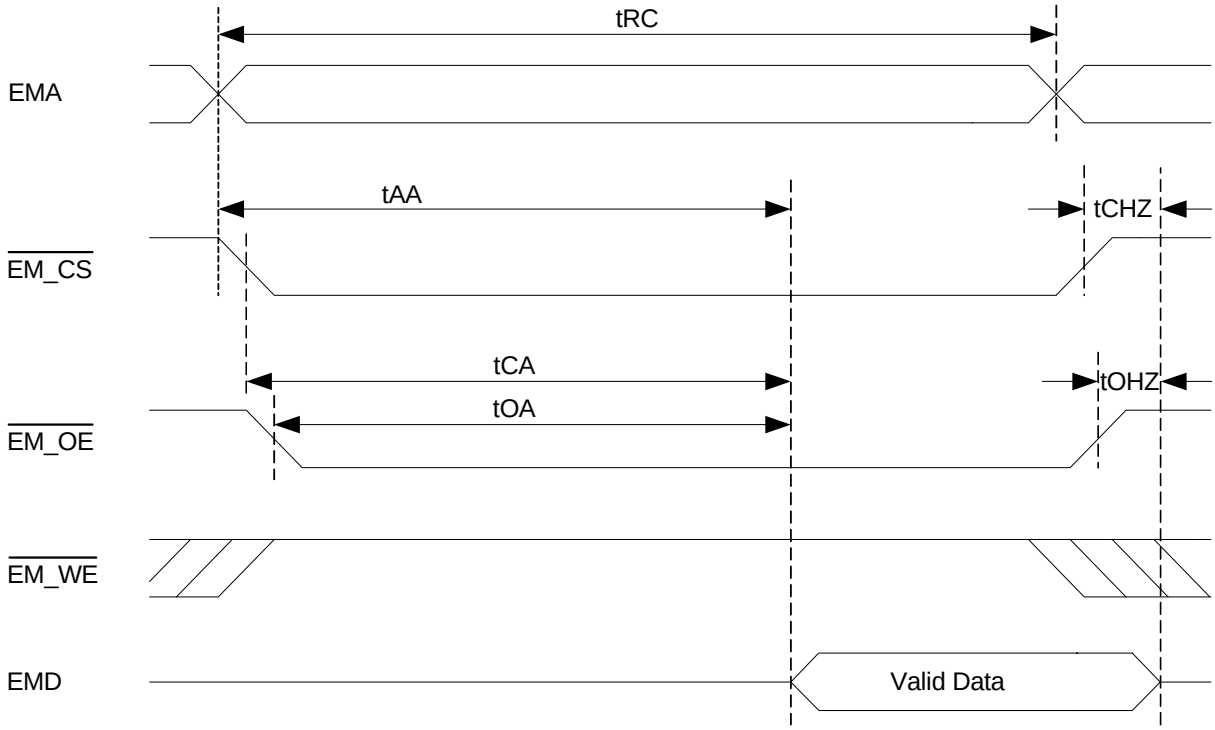


Figure-23 SRAM Interface Timing Diagram for Read Cycle

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Glossary

Active State	—	A link state indicating that the link is ready for transmitting or receiving ATM cells in the specified direction, either Tx or Rx. Each direction may enter active state asynchronously.
Anomaly	—	Discrepancy between the actual and desired characteristic of an item. An anomaly may or may not affect an item to perform a required function.
API	—	Application Programming Interface
Asymmetrical Configuration	—	This is an IMA configuration scheme. In this configuration mode, the physical links that are assigned to an IMA group are not required to be configured in both Tx and Rx directions. That is, some of the physical links may be configured to use both directions while others may only use one direction (Tx or Rx).
Asymmetrical Operation	—	This is an ATM traffic transfer mode of an IMA group. In this mode, the physical link can be used to transfer data in one direction and does not care the other direction's Tx and Rx state. That is, when the Tx state of end A and Rx state of end B have both entered active state, end A starts to transfer data to end B and end B starts to receive. In this case, end A does not care whether end A's Rx state is active or not and end B does not care whether end B's Tx state is active or not.
ATM	—	Asynchronous Transfer Mode
ATM Layer Cells	—	Cells (ATM formatted) that are exchanged between ATM layer and IMA sublayer. It is also called application data.
Blocked State	—	This is a group state indicating that the group has been inhibited from transiting into OPERATIONAL state for some administrative purposes.
Config-Aborted	—	This is a group state indicating that the group has rejected the group parameters proposed by the FE IMA group.
Common Transmit Clock (CTC)	—	This is a configuration where the transmit clocks of all the physical links within an IMA group are derived from the same clock source.
Data Round-Robin	—	This is the data transfer method IMA used to deliver cells from ATM layer to multiple transmit links within an IMA group, or the data play-out method that the IMA used to form a consecutive cell stream from multiple receive links within an IMA group.
Defect	—	A defect may be caused by successive anomaly of an item to perform a required function. The defect may or may not lead to maintenance action depending on the results of additional analysis.
ES	—	Errored Seconds
Far End (FE)	—	Two communication entities are considered to be two communication ends. Mostly, one is called Near-End (NE) and the other is called Far-End (FE).
Filler Cell	—	This is a kind of OAM cell used by IMA layer. It is used to fill in the IMA frame when no cells are available at the ATM layer. Thus filler cell is used for cell rate decoupling at IMA sublayer (like idle cell used in TC layer).
Group State Machine (GSM)	—	This is the state machine that determines the behavior of the IMA group.
Group Traffic State Machine (GTSM)	—	This state machine controls when to exchange ATM layer cell between the ATM layer and the IMA layer
Group Wide Procedure (GWP)	—	This refers to the Group Start-up and LASR procedures performed by the IMA unit to synchronize the activation of IMA links within the IMA group.
Header Error Check (HEC)	—	This is used for checking the correctness of the ATM cell header.

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ICP Offset	—	The ICP cell is used for IMA frame synchronization. The ICP offset is used to tell the receive side the ICP cell's position in an IMA frame and the receive side can make use of this information to figure out the first cell of the frame.
ICP Cell	—	The ICP cell is a kind of OAM cell. It can be used by the IMA sublayer to delineate the IMA frame. Also, it conveys information about the status or configuration parameters of each end.
ICP Stuff	—	The ICP stuff is two consecutive ICP cells at the ICP offset position. The ICP stuff is inserted by repeating the ICP cell. The purpose of the ICP stuff is to decrease the IMA data cell rate of fast links at the transmit side. When an ICP stuff is inserted into an IMA frame, the frame length will become M+1, with M being the frame length without ICP stuff.
IMA Frame Synchronization Mechanism (IFSM)	—	This is a state machine used for receiving IMA frame synchronization. It is an analogy to the cell delineation mechanism defined in ITU-T recommendation I.432.
IMA	—	Inverse Multiplexing for ATM
IMA Frame	—	The IMA frame is a cell stream transmitted over IMA links within an IMA group. There are altogether M cells in one IMA frame without ICP stuff. M could be 32, 64, 128 or 256. In each IMA frame, there are one ICP cell, ATM layer cells and IMA Filler cells. The ICP cells occur at the offset position specified in the ICP cell (the offset may be different for different links).
IMA Group	—	The IMA group is a number of links at one end that are used to establish an IMA virtual link to the other end.
IMA Link	—	An IMA link is a unidirectional logical link of a physical link's Tx or Rx direction. The IMA link is identified by the value of LID field of the ICP cells carried over that IMA link. Thus a physical link that connects two ends (A and B) may consist of two IMA links, one from A to B and the other from B to A.
IMA Sublayer	—	The IMA is a sublayer part of the Physical layer and located between the interface specific Transmission Convergence (TC) sublayer and the ATM layer.
IMA Virtual Link	—	This is a data communication channel between two communication ends (two IMA units) over a number of physical links; These links are also called an IMA group.
IMAOS04	—	A downloaded software used when the device is in normal communication.
IMAOS04_Slave	—	A downloaded software used when the device operates in Slave Mode. It supports the Group Auto Detect function.
Independent Transmit Clock (ITC)	—	This is a configuration where there is at least one IMA link within an IMA group that has its transmit clock derived from a clock source that is different from that of other IMA links. The IMA transmitter may indicate that it is in the ITC mode even if all of the transmit clocks of the links are derived from the same source.
In Group	—	This is an event indicating that a link has been configured into an IMA group.
Inhibiting	—	This represents the action to voluntarily disable the capacity of the group or the link to carry ATM layer cells for reasons other than reported problems.
Insufficient-Links	—	Group state indicating that the group does not have sufficient links in the Active state to be in the Operational state.
LASR	—	This stands for Link Addition and Slow Recovery procedure.
LCD	—	Loss of Cell Delineation defect. The LCD defect is reported when the OCD anomaly persists for the time specified in ITU-T Recommendation I.432 [30]. The LCD defect is cleared when the OCD anomaly has not been detected for the period of time specified in ITU-T Recommendation I.432.
LID	—	Link Identifier. The LID field in the ICP cell is used to identify an IMA link on which the ICP cells are transmitted. The LID is been used to determine the round-robin order to retrieve cells from the incoming IMA links at the IMA receiver.
LIF	—	Loss of IMA Frame defect. The LIF defect is the occurrence of persistent OIF anomalies for at least 2 IMA frames.
Link	—	The term "link" refers to an IMA link in this data sheet, unless the context clearly refers to a physical link.
Link Defect	—	A link defect is the occurrence of the persistent detection of an anomaly at the Interface Specific Transmission Convergence sublayer. LOS, LOF/OOF, AIS, LOC and LCD defects are examples of link defects reported at the Interface Specific Transmission Convergence sublayer.

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LODS	—	Link Out Of Delay Synchronization defect. The LODS is a link event indicating that the link is not synchronized with the other links within the IMA group.
LOF	—	Loss Of Frame
LOS	—	Loss Of Signal
LSB	—	Least Significant Bit
LSI	—	Link Stuff Indication
LSM	—	Link State Machine
M	—	IMA frame size
MIB	—	Management Information Base
MPU	—	MicroProcessor Unit
MSB	—	Most Significant Bit
NE	—	Near-End (local end)
Not Configured	—	This is a group state indicating that the group does not exist yet.
Not in Group	—	This is used as an event or a state indicating that a link is no longer configured within an IMA group.
OAM	—	Operations And Maintenance
OCD	—	Out of Cell Delineation anomaly. As specified in ITU-T Recommendation I.432 [30], an OCD anomaly is reported upon the occurrence of Alpha (α) consecutive cells with incorrect HEC, and it is no longer reported after detecting Delta (δ) consecutive cells with correct HEC.
OIF	—	Out of IMA Frame anomaly
OOF	—	Out Of Frame
Operational	—	Group state indicating that the group has sufficient links in both Tx and Rx directions to carry ATM layer cells.
Physical Link	—	This is the link being used by the IMA unit to transmit and receive ATM cells. The IMA unit may use physical links in one or both directions.
P_{rx}	—	Minimum number of links required to be active in the receive direction for the IMA group to move into the Operational state.
P_{tx}	—	Minimum number of links required to be active in the transmit direction for the IMA group to move into the Operational state.
RDI	—	Remote Defect Indicator
RFI	—	Remote Failure Indicator
Rx	—	Receive (side)
SES	—	Severely Errored Seconds
SICP Cell	—	Stuff ICP cell. One of the 2 ICP cells comprising a stuff event.
Stuff Event	—	This is a repetition of an ICP cell over one IMA link to compensate for timing difference with other links within the IMA group.
Start-up	—	This is a group state indicating that the group is waiting to see the FE in Start-up.
Start-up-Ack	—	This is a group transitional state, when both groups are in start-up and the FE group parameters have been accepted.
Symmetrical Configuration	—	This is an IMA group configuration scheme. In this configuration mode, physical links that are assigned to an IMA group are required to be configured in both Tx and Rx directions.
Symmetrical Operation	—	This is an ATM traffic mode of an IMA group. In this mode, the physical link can be used to transfer data only when the link's NE's Tx and Rx and FE's Tx and Rx are all in active state.

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TAP bus	—	Test Access Port bus
TC	—	Transmission Convergence
TRL	—	Timing Reference Link.
Tx	—	Transmit (side)
UAS	—	UnAvailable Seconds
UAS-IMA	—	UnAvailable Seconds for IMA. Interval during which the IMA receiver is declared unavailable. The period of unavailability begins at the onset of 10 continuous SES-IMA, including the first 10 seconds to enter the UAS-IMA condition. The period of unavailability ends at the onset of 10 continuous seconds with no SES-IMA, excluding the last 10 seconds to exit the UAS-IMA condition.
Unusable	—	This is a link state indicating the link is not in use due to fault, inhibition, etc.
Usable	—	This is a link state indicating the link is ready to operate in the specified direction, but it is waiting to move to Active.
UUS	—	UnUsable Seconds. Number of seconds during which the link state is Unusable.

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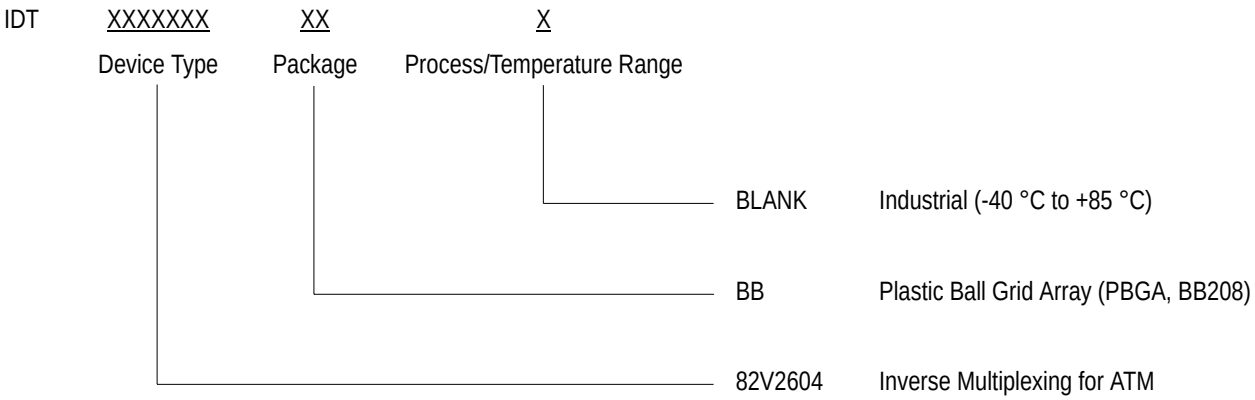
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