Dual Synchronous Ethernet Line Card PLL

Product Brief
IDT82V3395

FEATURES

HIGHLIGHTS

- Dual PLL chip:
  - Provides clocks for ITU-T G.8261/G.8262 Synchronous Ethernet (SyncE)
  - Exceeds GR-253-CORE (OC-12) and ITU-T G.813 (STM-4) jitter generation requirements
  - Provides clocks for Cellular and WLL base-station (GSM and 3G networks)
  - Provides clocks for 1 Gigabit and 10 Gigabit Ethernet applications

MAIN FEATURES

- Employs PLL architecture to feature excellent jitter performance and minimize the number of external components
- Integrates 2 DPLLs; one can be used on the transmit path and the other on the receive path
- Supports programmable DPLL bandwidth: 18 Hz, 35 Hz, 70 Hz and 560 Hz
- Provides OUT1~OUT4 output clock frequencies up to 644.53125 MHz
  - Includes 25MHz, 125 MHz and 156.25 MHz for CMOS outputs
  - Includes 25.78125MHz, 128.90625 MHz and 161.1328125 MHz for CMOS outputs
  - Includes 25MHz, 125 MHz, 156.25 MHz, 312.5 MHz and 625 MHz for differential outputs
  - Includes 25.78125 MHz, 128.90625 MHz, 161.1328125 MHz, 322.265625 MHz and 644.53125 MHz for differential outputs
- Provides IN1~IN4 input clock frequencies cover from 2 kHz to 155.52MHz MHz
- Supports Forced or Automatic operating mode switch controlled by an internal state machine. It supports Free- Run, Locked and Hold-over modes
- Supports manual and automatic selected input clock switch
- Supports automatic hitless selected input clock switch on clock failure
- Provides a 2 kHz, 4 kHz, or 8 kHz frame sync input signal, and a 2 kHz or 8 kHz frame sync output signals
- Provides a 1PPS sync input signal and a 1PPS sync output signal
- Provides output clocks for BITS, GPS, 3G, GSM, etc.
- Supports PECL/LVDS and CMOS input/output technologies
- Supports master clock calibration
- Supports Telcordia GR-1244-CORE, Telcordia GR-253-CORE, ITU-T G.812, ITU-T G.8262. ITU-T G.813 and ITU-T G.783 Recommendations

OTHER FEATURES

- I2C and Serial microprocessor interface modes
- IEEE 1149.1 JTAG Boundary Scan
- Single 3.3 V operation with 5 V tolerant CMOS I/Os
- 72-pin QFN package, green package options available

APPLICATIONS

- 1 Gigabit Ethernet and 10 Gigabit Ethernet
- BITS / SSU
- SMC / SEC (SONET / SDH)
- DWDM cross-connect and transmission equipment
- Synchronous Ethernet equipment
- Central Office Timing Source and Distribution
- Core and access IP switches / routers
- Gigabit and Terabit IP switches / routers
- IP and ATM core switches and access equipment
- Cellular and WLL base-station node clocks
- Broadband and multi-service access equipment

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DESCRIPTION

The IDT82V3395 is an integrated, single-chip solution for the Synchronous Equipment Timing applications in SONET / SDH / Synchronous Ethernet equipment, DWDM and Wireless base station.

The device supports several types of input clock sources: recovered clock from Synchronous Ethernet, STM-N or OC-n, PDH network synchronization timing.

The device consists of 2 DPLL+APLL paths. The two path lock independently from each other.

An input clock is automatically or manually selected for both path. Both paths support three primary operating modes: Free-Run, Locked and Holdover. In Free-Run mode, the DPLL refers to the master clock. In Locked mode, the DPLL locks to the selected input clock. In Holdover mode, the DPLL resorts to the frequency data acquired in Locked mode. Whatever the operating mode is, the DPLL gives a stable performance without being affected by operating conditions or silicon process variations.

There are 2 high performance APLLs that can be used for low jitter SONET and Ethernet Clocks

The device provides programmable DPLL bandwidths: 18 Hz, 35 Hz, 70 Hz and 560 Hz.

A stable input is required for the master clock in different applications. The master clock is used as a reference clock for all the internal circuits in the device.

All the read/write registers are accessed through a microprocessor interface. The device supports I2C and serial microprocessor interface modes.

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FUNCTIONAL BLOCK DIAGRAM

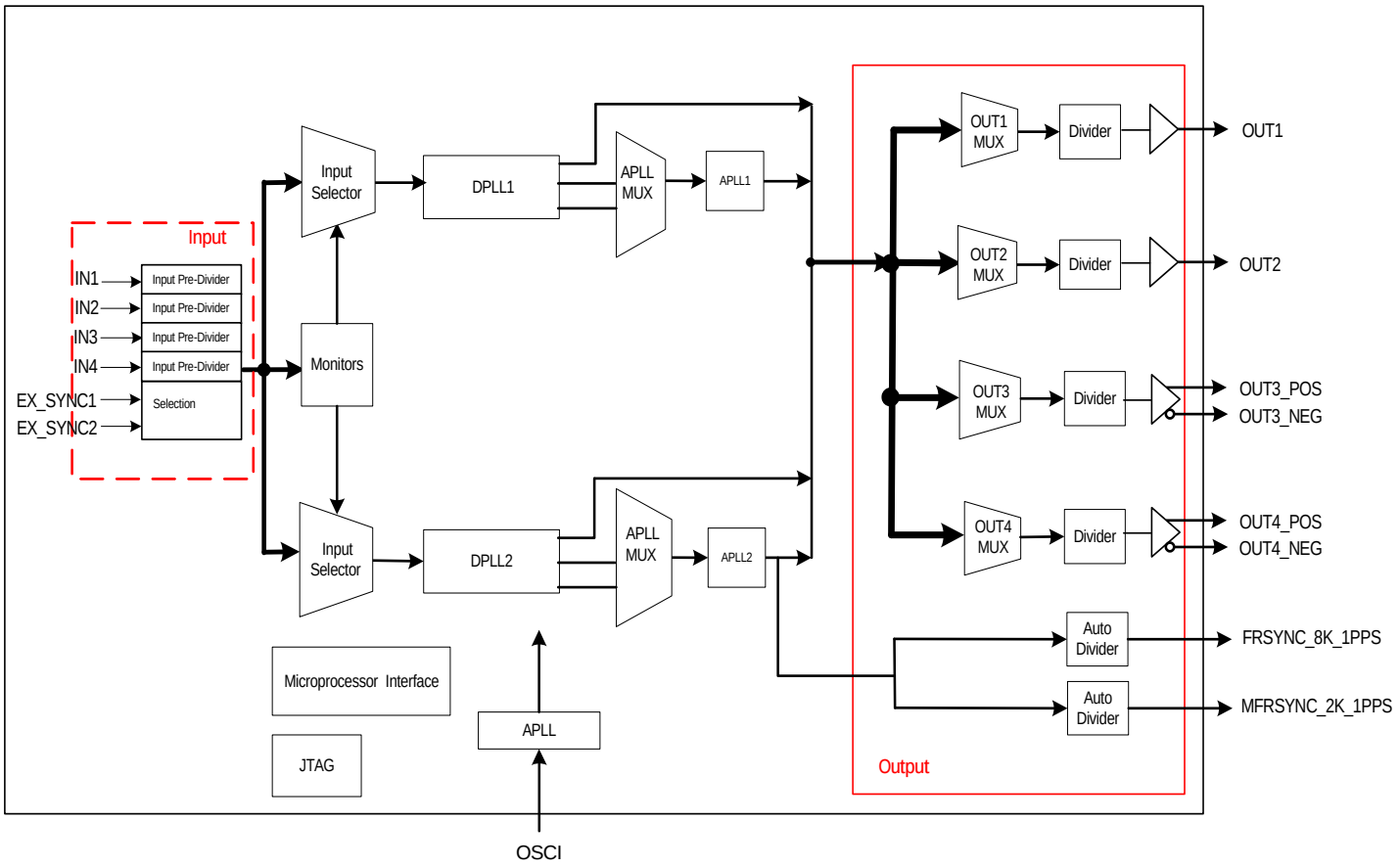
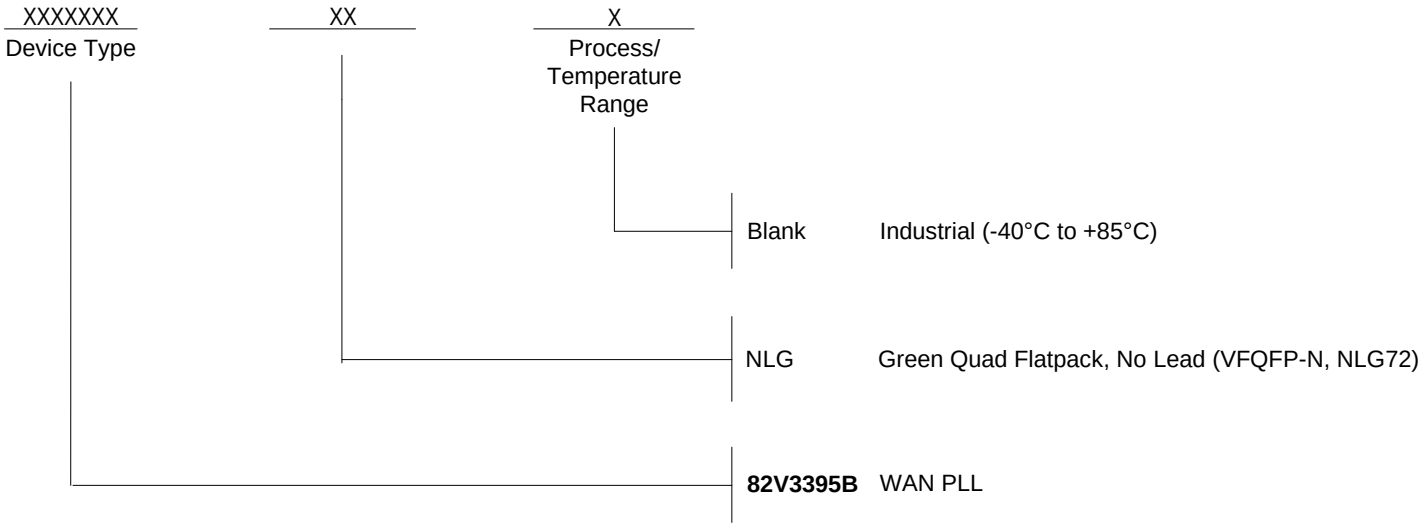


Figure 1. Functional Block Diagram

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ORDERING INFORMATION



REVISION HISTORY

March 5, 2012 Initial Version

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