# Synchronous Ethernet SETS for 10GbE and 40GbE

**IDT82V3910**
***Short Form Datasheet***

## FEATURES

### HIGHLIGHTS

- Jitter generation <0.3 ps RMS (10 kHz to 20 MHz), meets jitter generation requirements of leading PHYs supporting 10GBASE-R, 10GBASE-W, 40GBASE-R, OC-192 and STM-64
- Features 0.5 mHz to 35 Hz bandwidth
- Provides node clock for ITU-T G.8261/G.8262 Synchronous Ethernet (SyncE)
- Provides node clocks for Cellular and WLL base-station (GSM and 3G networks)
- Provides clocks for DSL access concentrators (DSLAM), especially for Japan TCM-ISDN network timing based ADSL equipments
- Provides clocks for 1 Gigabit, 10 Gigabit, and 40 Gigabit Ethernet
- Supports clock generation for IEEE-1588 applications

### MAIN FEATURES

- Provides an integrated solution for Synchronous Equipment Timing Source, including Stratum 3, SMC, EEC-Option 1 and EEC-Option 2 Clocks
- Integrates T4 DPLL and T0 DPLL; T4 DPLL locks independently or locks to T0 DPLL
- Supports programmable DPLL bandwidth (0.5 mHz to 35 Hz) and damping factor (1.2 to 20 in 5 steps)
- Supports $1.1X10^{-5}$ ppm absolute holdover accuracy and $4.4X10^{-8}$ ppm instantaneous holdover accuracy
- Supports hitless reference switching to minimize phase transients on T0 DPLL output to be no more than 0.61 ns
- Integrates 2 jitter attenuating APLLs to generate ultra-low jitter clocks
  - Supports 3 clock modes: SONET, Ethernet, and Ethernet LAN-PHY
  - Supports up to two crystal connections, allowing each APLL to support up to two modes of operation
- Supports input and output clocks whose frequencies range from 1PPS to 644.53125 MHz
  - Includes 1PPS clock input and output
  - Provides IN1 and IN2 for 64 kHz + 8 kHz or 64 kHz + 8 kHz + 0.4 kHz composite clocks
  - Provides IN3, IN4, IN7~IN14 input CMOS clocks whose frequencies range from 1PPS to 156.25 MHz
  - Provides IN5 and IN6 input differential clocks whose frequencies range from 1PPS to 625 MHz
  - Provides OUT1 to OUT5 output CMOS clocks whose frequency cover from 1PPS to 125 MHz
  - Provides OUT6,OUT7,OUT10 and OUT11 output differential clocks whose frequency cover from 25 MHz to 644.53125 MHz
  - Provides OUT8 for composite clocks and OUT9 for 1.544 MHz/2.048 MHz (BITS/SSU)
- Provides output clocks for BITS, GPS, 3G, GSM, etc.
- Provides a 1PPS, 2 kHz, 4 kHz, or 8 kHz frame sync input signal, and a 1PPS, 2 kHz or 8 kHz frame sync output signal
- Internal DCO can be controlled by an external processor to be used for IEEE-1588 clock generation
- Supports programmable input-to-output phase offset adjustment
- Limits the phase and frequency offset of the outputs
- Supports Forced or Automatic operating mode switch controlled by an internal state machine. Automatic mode switch supports Free-Run, Locked and Holdover modes
- Supports manual and automatic selected input clock switch
- Supports automatic hitless selected input clock switch on clock failure
- Supports three types of input clock sources: recovered clock from STM-N or OC-n, PDH network synchronization timing and external synchronization reference timing
- Supports AMI, LVPECL/LVDS and CMOS input/output technologies
- Supports Master/Slave application (two chips used together) to enable system protection against single chip failure
- Supports Telcordia GR-1244-CORE, Telcordia GR-253-CORE, ITU-T G.812, ITU-T G.8262, ITU-T G.813 and ITU-T G.783 Recommendations

### OTHER FEATURES

- I2C Microprocessor interface
- IEEE 1149.1 JTAG Boundary Scan
- Single 3.3 V operation with 5 V tolerant CMOS I/Os
- 1mm ball pitch CABGA green package

## APPLICATIONS

- SMC / SEC (SONET / SDH equipment)
- EEC (Synchronous Ethernet equipment)
- Core and access IP switches / routers
- Gigabit and Terabit IP switches / routers
- Cellular and WLL base-station node clocks
- Broadband and multi-service access equipment

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# DESCRIPTION

The 82V3910 Synchronous Ethernet (SyncE) SETS meets the requirements of ITU-T G.8262/G.813 for EEC/SEC options 1 and 2; and it meets the requirements of Telcordia GR-253-CORE Stratum 3 (S3) and SONET Minimum Clock (SMC). The 82V3910 ultra-low jitter output clocks can be used to directly synchronize 10GBASE-R/10GBASE-W and OC-192/STM-64 PHYs and 40GBASE-R PHYs in Synchronous Ethernet and SONET/SDH equipment.

The Synchronous Equipment Timing Source (SETS) functions are provided by two independent digital PLLs (DPLLs), T0 and T4, each with embedded clock synthesizers. The T0 DPLL meets the network synchronization requirements for frequency accuracy, pull-in, hold-in, pull-out, noise generation, noise tolerance, transient response and holdover performance. The T4 DPLL provides rate conversion functions that can be used, for example, to convert a recovered line clock to a 1.544 MHz, 2.048MHz or 64 kHz synchronization reference for external equipment.

The 82V3910 provides ten single ended reference inputs and two differential reference inputs that can operate at common Ethernet, SONET/SDH and PDH frequencies and other frequencies. The device also provides two Alternate Mark Inversion (AMI) inputs for Composite Clock (CC) signals bearing 64 kHz, 8 kHz and 0.4 kHz synchronization information. The references are continually monitored for loss of signal and for frequency offset per user programmed thresholds. All of the references are available to both digital PLLs (DPLLs). The active reference for each DPLL is determined by forced selection or by automatic selection based on user programmed priorities and locking allowances and based on the reference monitors.

The 82V3910 can accept a clock reference and a phase locked external sync signal as a pair. The T0 DPLL can lock to the reference clock input and align its frame sync and multi-frame sync outputs with the paired external sync input. The device provides to two external sync inputs that can be associated with any of the twelve reference inputs to create up to two pairs. The external sync signals can have a frequency of 1 Hz, 2 kHz or 8 kHz. This feature enables the T0 DPLL to phase align its frame sync and multi-frame sync outputs with an external sync input without the need use a low bandwidth setting to lock directly to an external sync input.

Both DPLLs support four primary operating modes: Free-Run, Locked, Holdover and Digitally Controlled Oscillator (DCO) Control. In Free-Run mode the DPLLs generate clocks based on the master clock alone. In Locked mode the DPLLs filter reference clock jitter with the selected bandwidth. In Locked mode the long-term DPLL frequency accuracy is the same as the long term frequency accuracy of the selected input reference. In Holdover mode the DPLL uses frequency data acquired while in Locked mode to generate accurate frequencies when input references are not available. In DCO Control Mode the DPLL control loop is opened and the DCO can be used by an algorithm (e.g. IEEE 1588 clock servo) running on an external processor to synthesize clock signals.

The 82V3910 requires a 12.8 MHz master clock for its reference monitors and other digital circuitry. The frequency accuracy of the master clock determines the frequency accuracy of the DPLLs in Free-Run mode. The frequency stability of the master clock determines the frequency stability of the DPLLs in Free-Run mode and in Holdover mode.

The T0 DPLL can be configured with a range of selectable filtering bandwidths from 0.5 mHz to 35 Hz. The 15 mHz and lower bandwidths can be used to lock the T0 DPLL directly to a 1 pulse per second (PPS) reference. The 0.1 Hz bandwidth can be used for G.8262/G.813 Option 2 or Telcordia GR-253-CORE S3 or SMC applications. The bandwidths in the range 1.2 Hz to 8 Hz can be used for G.8262/G.813 Option 1 applications. The bandwidths 18 Hz and 35 Hz can be used in jitter attenuation and rate conversion applications.

The T4 DPLL can be configured with filtering bandwidths of 18Hz or 35 Hz.

The clocks synthesized by the 82V3910 DPLLs can be passed through either of the two independent voltage controlled crystal oscillator (VCXO) based jitter attenuating analog PLLs (APLLs). Both APLLs drive two independent dividers that have differential outputs. The APLLs use external crystal resonators with resonant frequencies equal to the APLL base frequency divided by 25. Both APLLs can be provisioned with one or two selectable crystal resonators to support up to two base frequencies per APLL. The output clocks generated by the APLLs exhibit jitter below 0.30ps RMS over the integration range 10 kHz to 20 MHz for most output frequencies.

Any of the 82V3910 DPLL clocks can be routed through a mux to any of five single ended outputs via independent output dividers. The output of the T0 DPLL can be routed through the two auto-dividers to the single ended frame sync output that operates at 8 kHz or 1 PPS,


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# FUNCTIONAL BLOCK DIAGRAM

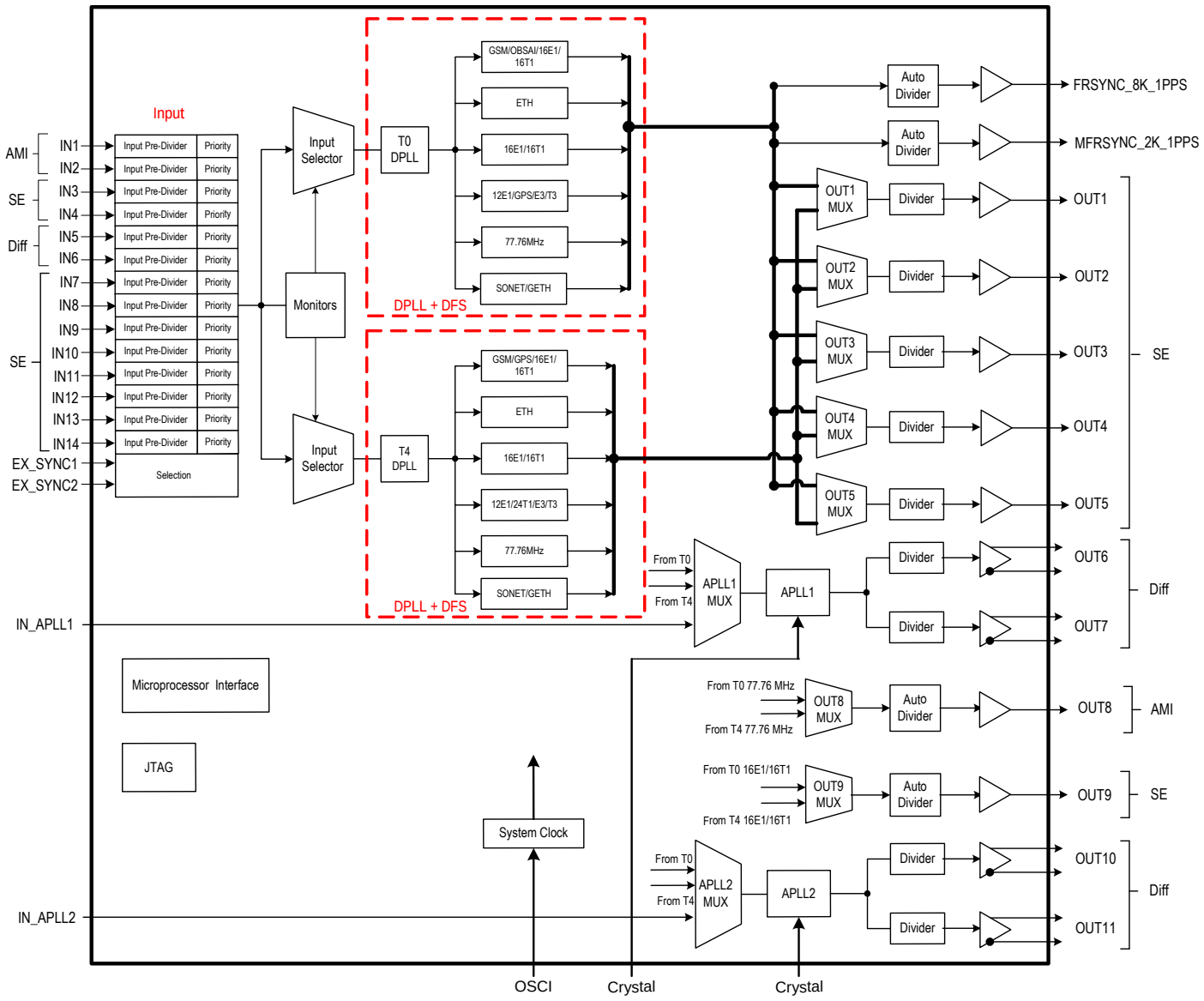



***Figure 1. Functional Block Diagram***



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# 1 PIN ASSIGNMENT

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A | IC10 | VDDA | XTAL1_IN | CAP1 | IN_APLL1_NEG | OUT8_NEG | IN1 | TDI | IC7 | FF_SRCSW | OSCI | TMS | IC6 | TRST | A |
| B | IC11 | VSSA | XTAL1_OUT | VSSAO | IN_APLL1_POS | OUT8_POS | IN2 | TDO/ T0_LOS_INT | VSSAO | TCK | VSSA | VSSA | VSSDO | VDDDO | B |
| C | IC4 | VDDA | NC | CAP2 | MFRSYNC_2K_1PPS | FRSYNC_8K_1PPS | VDDDO | VSSDO | VDDA | VSSA | VDDA | VDDA | INT_REQ | OUT9 | C |
| D | VSSA | VSSAO | CAP3 | VSSA | VDDA | MS/SL | VSSD | VDDD | IC2 | VDDA | VSSA | VDDA | OUT4 | OUT5 | D |
| E | XTAL3_IN | XTAL3_OUT | VSSA | VSSAO | VSSA | SONET/SDH | VSSD | VDDD | IC1 | VSSA | VDDA | VSSA | OUT2 | OUT3 | E |
| F | VDDD | VSSD | VSSAO | VSSA | VDDA | VSSAO | VSSD | VDDD | VSSD | VDDD | EX_SYNC1 | VDDDO | OUT1 | VSSDO | F |
| G | VSSD | VDDD | VSSAO | VSSAO | VSSAO | VSSD | VDDD | IC3 | VDDD | VSSD | EX_SYNC2 | IN12 | IN11 | IN13 | G |
| H | VDDAO | VSSAO | VDDAO | VSSAO | VSSAO | VSSAO | VSSD | VDDD | VSSD | VDDD | IN10 | IN14 | RST | IN3 | H |
| J | OUT6_NEG | OUT6_POS | VDDAO | VSSAO | VDDAO | VSSAO | VDDAO | VSSAO | VSSA | VDDA | T0_LOCK | IN9 | IN4 | IN7 | J |
| K | VSSAO | VSSAO | VSSAO | VDDAO | VSSAO | VDDAO | VSSAO | VSSD | VDDD | VSSAO | T4_LOCK | IN8 | I2C_SCL | I2C_SDA | K |
| L | OUT7_NEG | OUT7_POS | VDDAO | VSSAO | VSSAO | VSSAO | VSSAO | I2C_AD1 | I2C_AD2 | CAP4 | VSSA | CAP5 | VSSA | CAP6 | L |
| M | VDDAO | VSSAO | VSSAO | VSSAO | VDDAO | VSSAO | VDDAO | VSSAO | VSSAO | VSSAO | VSSAO | NC | XTAL4_OUT | XTAL4_IN | M |
| N | VSSAO | OUT10_POS | VSSAO | OUT11_POS | VSSAO | IN_APLL2_POS | IN5_POS | IN6_POS | VSSA | XTAL2_OUT | VSSA | IC9 | VSSAO | VSSA | N |
| P | VDDAO | OUT10_NEG | VSSAO | OUT11_NEG | VDDAO | IN_APLL2_NEG | IN5_NEG | IN6_NEG | VDDA | XTAL2_IN | VDDA | IC8 | IC5 | VDDA | P |
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | |

Key:

| Diff Outputs | Outputs | Inputs | Power | Ground |
|---|---|---|---|---|

*Figure 2. Pin Assignment (Top View)*



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# 2 PIN DESCRIPTION

Table 1: Pin Description

| Name | Pin No. | I/O | Type | Description [1] |
|---|---|---|---|---|
| Global Control Signal | | | | |
| OSCI | A11 | I | CMOS | OSCI: Crystal Oscillator Master Clock<br>A nominal 12.8000 MHz clock provided by a crystal oscillator is input on this pin. It is the master clock for the device. |
| FF_SRCSW | A10 | I pull-down | CMOS | FF_SRCSW: External Fast Selection Enable<br>During reset, this pin determines the default value of the EXT_SW bit (b4, MON_SW_HS_CNFG). The EXT_SW bit determines whether the External Fast Selection is enabled.<br>High: The default value of the EXT_SW bit (b4, MON_SW_HS_CNFG) is '1' (External Fast selection is enabled);<br>Low: The default value of the EXT_SW bit (b4, MON_SW_HS_CNFG) is '0' (External Fast selection is disabled).<br>After reset, this pin selects an input clock pair for the T0 DPLL if the External Fast selection is enabled:<br>High: Pair IN3 / IN5 is selected.<br>Low: Pair IN4 / IN6 is selected.<br>After reset, the input on this pin takes no effect if the External Fast selection is disabled. |
| MS/SL | D6 | I pull-up | CMOS | MS/SL: Master / Slave Selection<br>This pin, together with the MS_SL_CTRL bit (b0, MS_SL_CTRL_CNFG), controls whether the device is configured as the Master or as the Slave. Refer to Chapter 3.14 Master / Slave Configuration for details.<br>The signal level on this pin is reflected by the MASTER_SLAVE bit (b1, INPUT_-MODE_CNFG).<br>High: The value of the MASTER_SLAVE bit is '1'<br>Low: The value of the MASTER_SLAVE bit is '0' |
| SONET/SDH | E6 | I pull-down | CMOS | SONET/SDH: SONET / SDH Frequency Selection<br>During reset, this pin determines the default value of the IN_SONET_SDH bit (b2, INPUT_-MODE_CNFG):<br>High: The default value of the IN_SONET_SDH bit is '1' (SONET);<br>Low: The default value of the IN_SONET_SDH bit is '0' (SDH).<br>After reset, the value on this pin takes no effect. |
| RST | H13 | I pull-up | CMOS | RST: Reset<br>A low pulse of at least 50 µs on this pin resets the device. After this pin is high, the device will still be held in reset state for 500 ms (typical). |
| Frame Synchronization Input Signal | | | | |
| EX_SYNC1 | F11 | I pull-down | CMOS | EX_SYNC1: External Sync Input 1<br>A 2 kHz, 4 kHz, 8 kHz, or 1PPS signal is input on this pin. |
| EX_SYNC2 | G11 | I pull-down | CMOS | EX_SYNC2: External Sync Input 1<br>A 2 kHz, 4 kHz, 8 kHz, or 1PPS signal is input on this pin. |
| Input Clock | | | | |
| IN1 | A7 | I | AMI | IN1: Input Clock 1<br>A 64 kHz + 8 kHz or 64 kHz + 8 kHz + 0.4 kHz composite clock is input on this pin. |
| IN2 | B7 | I | AMI | IN2: Input Clock 2<br>A 64 kHz + 8 kHz or 64 kHz + 8 kHz + 0.4 kHz composite clock is input on this pin. |
| IN3 | H14 | I pull-down | CMOS | IN3: Input Clock 3<br>A 1 PPS, 2 kHz, 4 kHz, N x 8 kHz [3], 1.544 MHz (SONET) / 2.048 MHz (SDH), 6.25 MHz, 6.48 MHz, 10MHz, 19.44 MHz, 25MHz, 25.92 MHz, 38.88 MHz, 51.84 MHz, 77.76 MHz, 125MHz, 155.52 MHz or 156.25 MHz clock is input on this pin. |


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Table 1: Pin Description (Continued)

| Name | Pin No. | I/O | Type | Description [1] |
|---|---|---|---|---|
| IN4 | J13 | I pull-down | CMOS | IN4: Input Clock 4<br>A 1 PPS, 2 kHz, 4 kHz, N x 8 kHz [3], 1.544 MHz (SONET) / 2.048 MHz (SDH), 6.25 MHz, 6.48 MHz, 10MHz, 19.44 MHz, 25MHz, 25.92 MHz, 38.88 MHz, 51.84 MHz, 77.76 MHz, 125MHz, 155.52 MHz or 156.25 MHz clock is input on this pin. |
| IN5_POS<br>IN5_NEG | N7<br>P7 | I | LVPECL/LVDS | IN5_POS / IN5_NEG: Positive / Negative Input Clock 5<br>A 1 PPS, 2 kHz, 4 kHz, N x 8 kHz [3], 1.544 MHz (SONET) / 2.048 MHz (SDH), 6.25 MHz, 6.48 MHz, 10MHz, 19.44 MHz, 25MHz, 25.92 MHz, 38.88 MHz, 51.84 MHz, 77.76 MHz, 155.52 MHz, 156.25 MHz, 311.04 MHz, 312.5 MHz, 622.08 MHz or 625 MHz clock is differentially input on this pair of pins. Whether the clock signal is LVPECL or LVDS is automatically detected.<br>Single-ended input for differential input is also supported. Refer to Chapter 7.3.3.5 Single-Ended Input for Differential Input. |
| IN6_POS<br>IN6_NEG | N8<br>P8 | I | LVPECL/LVDS | IN6_POS / IN6_NEG: Positive / Negative Input Clock 6<br>A 1 PPS, 2 kHz, 4 kHz, N x 8 kHz [3], 1.544 MHz (SONET) / 2.048 MHz (SDH), 6.25 MHz, 6.48 MHz, 10MHz, 19.44 MHz, 25MHz, 25.92 MHz, 38.88 MHz, 51.84 MHz, 77.76 MHz, 155.52 MHz, 156.25 MHz, 311.04 MHz or 312.5 MHz, 622.08 MHz or 625 MHz clock is differentially input on this pair of pins. Whether the clock signal is LVPECL or LVDS is automatically detected.<br>Single-ended input for differential input is also supported. Refer to Chapter 7.3.3.5 Single-Ended Input for Differential Input. |
| IN7 | J14 | I pull-down | CMOS | IN7: Input Clock 7<br>A 1 PPS, 2 kHz, 4 kHz, N x 8 kHz [3], 1.544 MHz (SONET) / 2.048 MHz (SDH), 6.25 MHz, 6.48 MHz, 10MHz, 19.44 MHz, 25MHz, 25.92 MHz, 38.88 MHz, 51.84 MHz, 77.76 MHz, 125MHz, 155.52 MHz or 156.25 MHz clock is input on this pin. |
| IN8 | K12 | I pull-down | CMOS | IN8: Input Clock 8<br>A 1 PPS, 2 kHz, 4 kHz, N x 8 kHz [3], 1.544 MHz (SONET) / 2.048 MHz (SDH), 6.25 MHz, 6.48 MHz, 10MHz, 19.44 MHz, 25MHz, 25.92 MHz, 38.88 MHz, 51.84 MHz, 77.76 MHz, 125MHz, 155.52 MHz or 156.25 MHz clock is input on this pin. |
| IN9 | J12 | I pull-down | CMOS | IN9: Input Clock 9<br>A 1 PPS, 2 kHz, 4 kHz, N x 8 kHz [3], 1.544 MHz (SONET) / 2.048 MHz (SDH), 6.25 MHz, 6.48 MHz, 10MHz, 19.44 MHz, 25MHz, 25.92 MHz, 38.88 MHz, 51.84 MHz, 77.76 MHz, 155.52 MHz or 156.25 MHz clock is input on this pin. |
| IN10 | H11 | I pull-down | CMOS | IN10: Input Clock 10<br>A 1 PPS, 2 kHz, 4 kHz, N x 8 kHz [3], 1.544 MHz (SONET) / 2.048 MHz (SDH), 6.25 MHz, 6.48 MHz, 10MHz, 19.44 MHz, 25MHz, 25.92 MHz, 38.88 MHz, 51.84 MHz, 77.76 MHz, 155.52 MHz or 156.25 MHz clock is input on this pin. |
| IN11 | G13 | I pull-down | CMOS | IN11: Input Clock 11<br>A 1 PPS, 2 kHz, 4 kHz, N x 8 kHz [3], 1.544 MHz (SONET) / 2.048 MHz (SDH), 6.25 MHz, 6.48 MHz, 10MHz, 19.44 MHz, 25MHz, 25.92 MHz, 38.88 MHz, 51.84 MHz, 77.76 MHz, 155.52 MHz or 156.25 MHz clock is input on this pin.<br>In Slave operation, the frequency of the T0 selected input clock IN11 is recommended to be 6.48 MHz. |
| IN12 | G12 | I pull-down | CMOS | IN12: Input Clock 12<br>A 1 PPS, 2 kHz, 4 kHz, N x 8 kHz [3], 1.544 MHz (SONET) / 2.048 MHz (SDH), 6.25 MHz, 6.48 MHz, 10MHz, 19.44 MHz, 25MHz, 25.92 MHz, 38.88 MHz, 51.84 MHz, 77.76 MHz, 155.52 MHz or 156.25 MHz clock is input on this pin. |
| IN13 | G14 | I pull-down | CMOS | IN13: Input Clock 13<br>A 1 PPS, 2 kHz, 4 kHz, N x 8 kHz [3], 1.544 MHz (SONET) / 2.048 MHz (SDH), 6.25 MHz, 6.48 MHz, 10MHz, 19.44 MHz, 25MHz, 25.92 MHz, 38.88 MHz, 51.84 MHz, 77.76 MHz, 155.52 MHz or 156.25 MHz clock is input on this pin. |


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Table 1: Pin Description (Continued)

| Name | Pin No. | I/O | Type | Description [1] |
|---|---|---|---|---|
| IN14 | H12 | I pull-down | CMOS | IN14: Input Clock 14<br>A 1 PPS, 2 kHz, 4 kHz, N x 8 kHz [3], 1.544 MHz (SONET) / 2.048 MHz (SDH), 6.25 MHz, 6.48 MHz, 10MHz, 19.44 MHz, 25MHz, 25.92 MHz, 38.88 MHz, 51.84 MHz, 77.76 MHz, 155.52 MHz or 156.25 MHz clock is input on this pin. |
| IN_APLL1_POS<br>IN_APLL1_NEG | B5<br>A5 | I pull-down<br>I pull-up/ pull-down | LVPECL/LVDS/ LVHSTL/SSTL/ HCSL | IN_APLL1_POS / IN_APLL1_NEG: Input Clock to APLL1<br>Direct input clock to APLL1. This pin is used for test. It can be left floating or a 1kΩ resistor can be tied from IN_APLL1_POS to ground. |
| IN_APLL2_POS<br>IN_APLL2_NEG | N6<br>P6 | I pull-down<br>I pull-up/ pull-down | LVPECL/LVDS/ LVHSTL/SSTL/ HCSL | IN_APLL2_POS / IN_APLL2_NEG: Input Clock APLL2<br>Direct input clock to APLL2. This pin is used for test. It can be left floating or a 1kΩ resistor can be tied from IN_APLL2_POS to ground. |
| Output Frame Synchronization Signal | | | | |
| FRSYN-C_8K_1PPS | C6 | O | CMOS | FRSYNC_8K_1PPS: 8 kHz Frame Sync Output<br>An 8 kHz signal or a 1PPS Frame Pulse is output on this pin. |
| MFRSYN-C_2K_1PPS | C5 | O | CMOS | MFRSYNC_2K_1PPS: 2 kHz Multiframe Sync Output<br>A 2 kHz signal or a 1PPS Frame Pulse is output on this pin. |
| Output Clock | | | | |
| OUT1<br>OUT2<br>OUT3<br>OUT4<br>OUT5 | F13<br>E13<br>E14<br>D13<br>D14 | O | CMOS | OUT1 ~ OUT5: Output Clock 1 ~ 5<br>A 1 pps, 400 Hz, 2 kHz, 8 kHz, 64 kHz, N x E1 [4], N x T1 [5], N x 13.0 MHz [6], N x 3.84 MHz [7], 5 MHz, 10 MHz, 20 MHz, E3, T3, 6.48 MHz, 19.44 MHz, 25.92 MHz, 38.88 MHz, 51.84 MHz, 77.76 MHz, 25MHz, or 125 MHz clock is output on these pins. |
| OUT6_POS<br>OUT6_NEG | J2<br>J1 | O | LVPECL/LVDS | OUT6_POS / OUT6_NEG: Positive / Negative Output Clock 6<br>A SONET based (77.76 MHz, 155.52 MHz, 311.04 MHz, 622.08 MHz), Ethernet based (25 MHz, 125 MHz, 156.25 MHz, 312.5 MHz, 625 MHz), or Ethernet LAN based (161.1328125 MHz, 322.265625 MHz, 644.53125 MHz) clock is differentially output on this pair of pins from APLL1. |
| OUT7_POS<br>OUT7_NEG | L2<br>L1 | O | LVPECL/LVDS | OUT7_POS / OUT7_NEG: Positive / Negative Output Clock 7<br>A SONET based (77.76 MHz, 155.52 MHz, 311.04 MHz, 622.08 MHz), Ethernet based (25 MHz, 125 MHz, 156.25 MHz, 312.5 MHz, 625 MHz), or Ethernet LAN based (161.1328125 MHz, 322.265625 MHz, 644.53125 MHz) clock is differentially output on this pair of pins from APLL1. |
| OUT8_POS<br>OUT8_NEG | B6<br>A6 | O | AMI | OUT8_POS / OUT8_NEG: Positive / Negative Output Clock 8<br>A 64 kHz + 8 kHz or 64 kHz + 8 kHz + 0.4 kHz composite clock is differentially output on this pair of pins. |
| OUT9 | C14 | O | CMOS | OUT9: Output Clock 9<br>A 1.544 MHz (SONET) / 2.048 MHz (SDH) BITS/SSU clock is output on this pin. |
| OUT10_POS<br>OUT10_NEG | N2<br>P2 | O | LVPECL/LVDS | OUT10_POS / OUT10_NEG: Positive / Negative Output Clock 10<br>A SONET based (77.76 MHz, 155.52 MHz, 311.04 MHz, 622.08 MHz), Ethernet based (25 MHz, 125 MHz, 156.25 MHz, 312.5 MHz, 625 MHz), or Ethernet LAN based (161.1328125 MHz, 322.265625 MHz, 644.53125 MHz) clock is differentially output on this pair of pins from APLL2. |
| OUT11_POS<br>OUT11_NEG | N4<br>P4 | O | LVPECL/LVDS | OUT11_POS / OUT11_NEG: Positive / Negative Output Clock 11<br>A SONET based (77.76 MHz, 155.52 MHz, 311.04 MHz, 622.08 MHz), Ethernet based (25 MHz, 125 MHz, 156.25 MHz, 312.5 MHz, 625 MHz), or Ethernet LAN based (161.1328125 MHz, 322.265625 MHz, 644.53125 MHz) clock is differentially output on this pair of pins from APLL2. |
| Miscellaneous | | | | |
| CAP1, CAP2, CAP3 | A4, C4, D3 | O | Analog | CAP1, CAP2 and CAP3: Analog Power Filter Capacitor connection 1 to 3<br>Connect a 10uF capacitor in parallel with a low ESR 100nF capacitor between these pins and VSS1 |



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Table 1: Pin Description (Continued)

| Name | Pin No. | I/O | Type | Description [1] |
|---|---|---|---|---|
| CAP4, CAP5, CAP6 | L10, L12, L14 | O | Analog | CAP4, CAP5 and CAP6: Analog Power Filter Capacitor connection 4 to 6<br>Connect a 10uF capacitor in parallel with a low ESR 100nF capacitor between these pins and VSS2 |
| XTAL1_IN | A3 | I | Analog | Crystal oscillator 1 input.<br>Determines first of two frequency families (Sonet/SDH, Ethernet or Ethernet*66/64) available for APLL1. Connect to ground if XTAL1 is not used. |
| XTAL1_OUT | B3 | O | Analog | Crystal oscillator 1 output.<br>Leave open if XTAL1 is not used. |
| XTAL2_IN | P10 | I | Analog | Crystal oscillator 2 input.<br>Determines first of two frequency families (chosen from Sonet/SDH, Ethernet or Ethernet*66/64) available for APLL2. Connect to ground if XTAL2 is not used |
| XTAL2_OUT | N10 | O | Analog | Crystal oscillator 2 output.<br>Leave open if XTAL2 is not used. |
| XTAL3_IN | E1 | I | Analog | Crystal oscillator 3 input.<br>Determines second of two frequency families (chosen from Sonet/SDH, Ethernet or Ethernet*66/64) available for APLL1. Connect to ground if XTAL3 is not used. |
| XTAL3_OUT | E2 | O | Analog | Crystal oscillator 3 output.<br>Leave open if XTAL3 is not used. |
| XTAL4_IN | M14 | I | Analog | Crystal oscillator 4 input. Connect to ground if XTAL4 is not used.<br>Determines second of two frequency families (chosen from Sonet/SDH, Ethernet or Ethernet*66/64) available for APLL2. |
| XTAL4_OUT | M13 | O | Analog | Crystal oscillator 4 output.<br>Leave open if XTAL4 is not used. |
| Lock Indication Signals | | | | |
| T4_LOCK | K11 | O | CMOS | T4 lock indicator.<br>This pin goes high when T4 is locked. |
| T0_LOCK | J11 | O | CMOS | T0 lock indicator.<br>This pin goes high when T0 is locked. |
| Microprocessor Interface | | | | |
| INT_REQ | C13 | O | CMOS | INT_REQ: Interrupt Request<br>This pin is used as an interrupt request. The output characteristics are determined by the HZ_EN bit (b1, INTERRUPT_CNFG) and the INT_POL bit (b0, INTERRUPT_CNFG). |
| I2C_SDA | K14 | I/O<br>pull-down | CMOS | I2C_SDA: Serial Data Input/Output<br>This pin is used as the input/output for the I2C serial data. |
| I2C_AD1 | L8 | I<br>pull-up | CMOS | I2C_AD1: Device Address Bit 1<br>I2C_AD2 and I2C_AD1 pins are the address bus of the microprocessor interface. |
| I2C_AD2 | L9 | I<br>pull-up | CMOS | I2C_AD2: Device Address Bit 2<br>I2C_AD2 and I2C_AD1 pins are the address bus of the microprocessor interface. |
| I2C_SCL | K13 | I<br>pull-down | CMOS | I2C_SCL: Serial Clock Line<br>The I2C serial clock is input on this pin. |
| JTAG (per IEEE 1149.1) | | | | |
| TRST | A14 | I<br>pull-down | CMOS | TRST: JTAG Test Reset (Active Low)<br>A low signal on this pin resets the JTAG test port.<br>This pin should be connected to ground when JTAG is not used. |
| TMS | A12 | I<br>pull-up | CMOS | TMS: JTAG Test Mode Select<br>The signal on this pin controls the JTAG test performance and is sampled on the rising edge of TCK. |


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Table 1: Pin Description (Continued)

| Name | Pin No. | I/O | Type | Description [1] |
|---|---|---|---|---|
| TCK | B10 | I<br>pull-down | CMOS | TCK: JTAG Test Clock<br>The clock for the JTAG test is input on this pin. TDI and TMS are sampled on the rising edge of TCK and TDO is updated on the falling edge of TCK.<br>If TCK is idle at a low level, all stored-state devices contained in the test logic will indefinitely retain their state. |
| TDI | A8 | I<br>pull-up | CMOS | TDI: JTAG Test Data Input<br>The test data is input on this pin. It is clocked into the device on the rising edge of TCK. |
| TDO/<br>T0_LOS_INT | B8 | O | CMOS | TDO: JTAG Test Data Output<br>The test data is output on this pin. It is clocked out of the device on the falling edge of TCK. TDO pin outputs a high impedance signal except during the process of data scanning.<br>T0_LOS_INT: T0 LOS Interrupt<br>This pin can indicate the interrupt of T0 selected input clock fail, as determined by the LOS_FLAG_ON_TDO bit (b6, MON_SW_HS_CNFG). Refer to Chapter 3.8.1 Input Clock Validity for details. |
| Power & Ground | | | | |
| VDDD | D8, E8, F1, F8, F10, G2, G7, G9, H8, H10, K9 | Power | - | Digital Core Power - +3.3V DC nominal |
| VDDDO | B14, C7, F12 | Power | | Digital Output Power - +3.3V DC nominal |
| VDDA | A2, C2, C9, C11, C12, D5, D10, D12, E11, F5, J10, P9, P11, P14 | Power | | Analog Core Power - +3.3V DC nominal |
| VDDAO | H1, H3, J3, J5, J7, K4, K6, L3, M1, M5, M7, P1, P5 | Power | | Analog Output Power - +3.3V DC nominal |
| VSSD | D7, E7, F2, F7, F9, G1, G6, G10, H7, H9, K8 | Ground | - | Ground |
| VSSDO | B13, C8, F14 | Ground | - | Ground |
| VSSA | B2, B11, B12, C10, D1, D4, D11, E3, E5, E10, E12, F4, J9, L11, L13, N9, N11, N14 | Ground | - | Analog Ground |
| VSSAO | B4, B9, D2, E4, F3, F6,G3, G4, G5, H2, H4, H5, H6, J4, J6, J8, K1, K2, K3, K5,K7, K10, L4, L5, L6, L7, M2, M3, M4, M6, M8, M9, M10, M11, N1, N3, N5, N13, P3 | Ground | - | Analog Output Ground |


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Table 1: Pin Description (Continued)

| Name | Pin No. | I/O | Type | Description [1] |
|---|---|---|---|---|
| Others | | | | |
| IC1<br>IC2<br>IC3<br>IC4<br>IC5<br>IC6<br>IC7<br>IC8<br>IC9<br>IC10<br>IC11 | E9<br>D9<br>G8<br>C1<br>P13<br>A13<br>A9<br>P12<br>N12<br>A1<br>B1 | - | - | IC: Internal Connected<br>Internal Use. These pins should be left open for normal operation. |
| NC | C3, M12 | | | NC: Not Connected<br>Not connected: There is no internal connection to these pins |

Note:
1. All the unused input pins should be connected to ground; the output of all the unused output pins are don't-care.
2. The contents in the brackets indicate the position of the register bit/bits.
3. N x 8 kHz: $1 \leq N \leq 19440$.
4. N x E1: N = 1, 2, 3, 4, 6, 8, 12, 16
5. N x T1: N = 1, 2, 3, 4, 6, 8, 12, 16, 24
6. N x 13.0 MHz: N = 1, 2
7. N x 3.84 MHz: N = 1, 2, 4, 8


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# 2.1 RECOMMENDATIONS FOR UNUSED INPUT AND OUTPUT PINS

## 2.1.1 INPUTS

### Control Pins

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

### Single-Ended Clock Inputs

For protection, unused single-ended clock inputs should be tied to ground.

### Differential Clock Inputs

For applications not requiring the use of a differential input, both *_POS and *_NEG can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from _POS to ground.

### XTAL Inputs

For applications not requiring the use of a crystal oscillator input, both _IN and _OUT can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from _IN to ground.

## 2.1.2 OUTPUTS

### Status Pins

For applications not requiring the use of a status pin, we recommend bringing out to a test point for debugging purposes.

### Single-Ended Clock Outputs

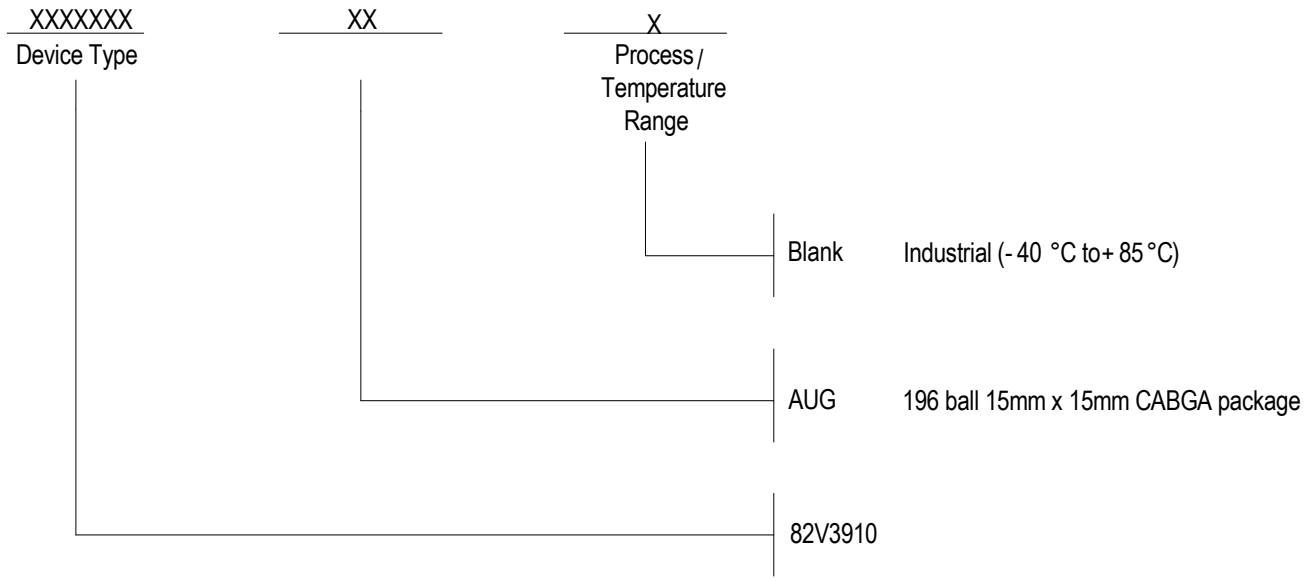
All unused single-ended clock outputs can be left floating, or can be brought out to a test point for debugging purposes.

### Differential Clock Outputs

All unused differential outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.


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# ORDERING INFORMATION





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