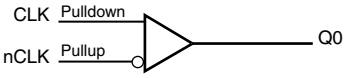
General Description

The 83021I is a 1-to-1 Differential-to-LVCMOS/ LVTTL Translator and a member of the family of High Performance Clock Solutions from IDT. The differential input is highly flexible and can accept the following input types: LVPECL, LVDS, LVHSTL, SSTL, and HCSL. The small 8-lead SOIC footprint makes this device ideal for use in applications with limited board space.

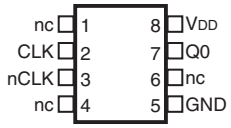
Features

- One LVCMOS/LVTTL output
- Differential CLK/nCLK input pair
- CLK/nCLK pair can accept the following differential input levels: LVPECL, LVDS, LVHSTL, SSTL, HCSL
- Output frequency: 350MHz (typical)
- Part-to-part skew: 500ps (maximum)
- Additive phase jitter, RMS: 0.21ps (typical), 3.3V output
- Full 3.3V and 2.5V operating supply
- -40°C to 85°C ambient operating temperature

Block Diagram



Pin Assignment



83021I

8-Lead SOIC, 150Mil
3.9mm x 4.9mm x 1.375mm package body
M Package
Top View

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Table 1. Pin Descriptions

Number	Name	Type		Description
1, 4, 6	nc	Unused		No connect.
2	CLK	Input	Pulldown	Non-inverting differential clock input.
3	nCLK	Input	Pullup	Inverting differential clock input.
5	GND	Power		Power supply ground.
7	Q0	Output		Single-ended clock output. LVCMOS/LVTTL interface levels.
8	V_{DD}	Power		Positive supply pin.

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ
C_{PD}	Power Dissipation Capacitance	V_{DD} = 3.6V		23		pF
R_{OUT}	Output Impedance		5	7	12	Ω

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Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5V
Outputs, V_O	-0.5V to V_{DD} + 0.5V
Package Thermal Impedance, θ_{JA}	103°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 3A. Power Supply DC Characteristics, V_{DD} = 3.3V ± 0.3V or 2.5V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Positive Supply Voltage		3.0	3.3	3.6	V
			2.375	2.5	2.625	V
I_{DD}	Power Supply Current				20	mA

Table 3B. LVCMOS/LVTTL DC Characteristics, V_{DD} = 3.3V ± 0.3V or 2.5V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1	V_{DD} = 3.6V	2.6			V
		V_{DD} = 2.625V	1.8			V
V_{OL}	Output Low Voltage; NOTE 1	V_{DD} = 3.6V or 2.625V			0.5	V

NOTE 1: Outputs terminated with 50Ω to V_{DD}/2. See Parameter Measurement Information, *Output Load Test Circuit Diagrams.*

Table 3C. Differential DC Characteristics, V_{DD} = 3.3V ± 0.3V or 2.5V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	nCLK	V_{IN} = V_{DD} = 3.6V or 2.625V			5	µA
		CLK	V_{IN} = V_{DD} = 3.6V or 2.625V			150	µA
I_{IL}	Input Low Cureent	nCLK	V_{IN} = 0V, V_{DD} = 3.6V or 2.625V	-150			µA
		CLK	V_{IN} = 0V, V_{DD} = 3.6V or 2.625V	-5			µA
V_{PP}	Peak-to-Peak Input Voltage			0.15		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			GND + 0.5		V_{DD} – 0.85	V

NOTE 1: For single ended applications, the maximum input voltage for CLK, nCLK is V_{DD} + 0.3V.
NOTE 2: Common mode voltage is defined as V_{IH}.

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AC Electrical Characteristics

Table 4A. AC Characteristics, V_{DD} = 3.3V ± 0.3V, T_A = -40°C to 85°C

Parameter	Symbol	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency			350		MHz
t_{PD}	Propagation Delay, NOTE 1	$f \leq$ 350MHz	1.7	2.0	2.3	ns
*t*sk(pp)	Part-to-Part Skew; NOTE 2, 3				500	ps
*t*jit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section	100MHz, Integration Range (637kHz – 10MHz)		0.21		ps
t_R / t_F	Output Rise/Fall Time	0.8V to 2V	100	250	400	ps
odc	Output Duty Cycle	$f \leq$ 166MHz	45	50	55	%
		166MHz < $f \leq$ 350MHz	40	50	60	%

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
All parameters measured at f_{MAX} unless noted otherwise.
NOTE 1: Measured from the differential input crossing point to the output at $V_{DD}/2$.
NOTE 2: Defined as skew between outputs on different devices operating at the same supply voltage and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at $V_{DD}/2$.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

Table 4B. AC Characteristics, V_{DD} = 2.5V ± 5%, T_A = -40°C to 85°C

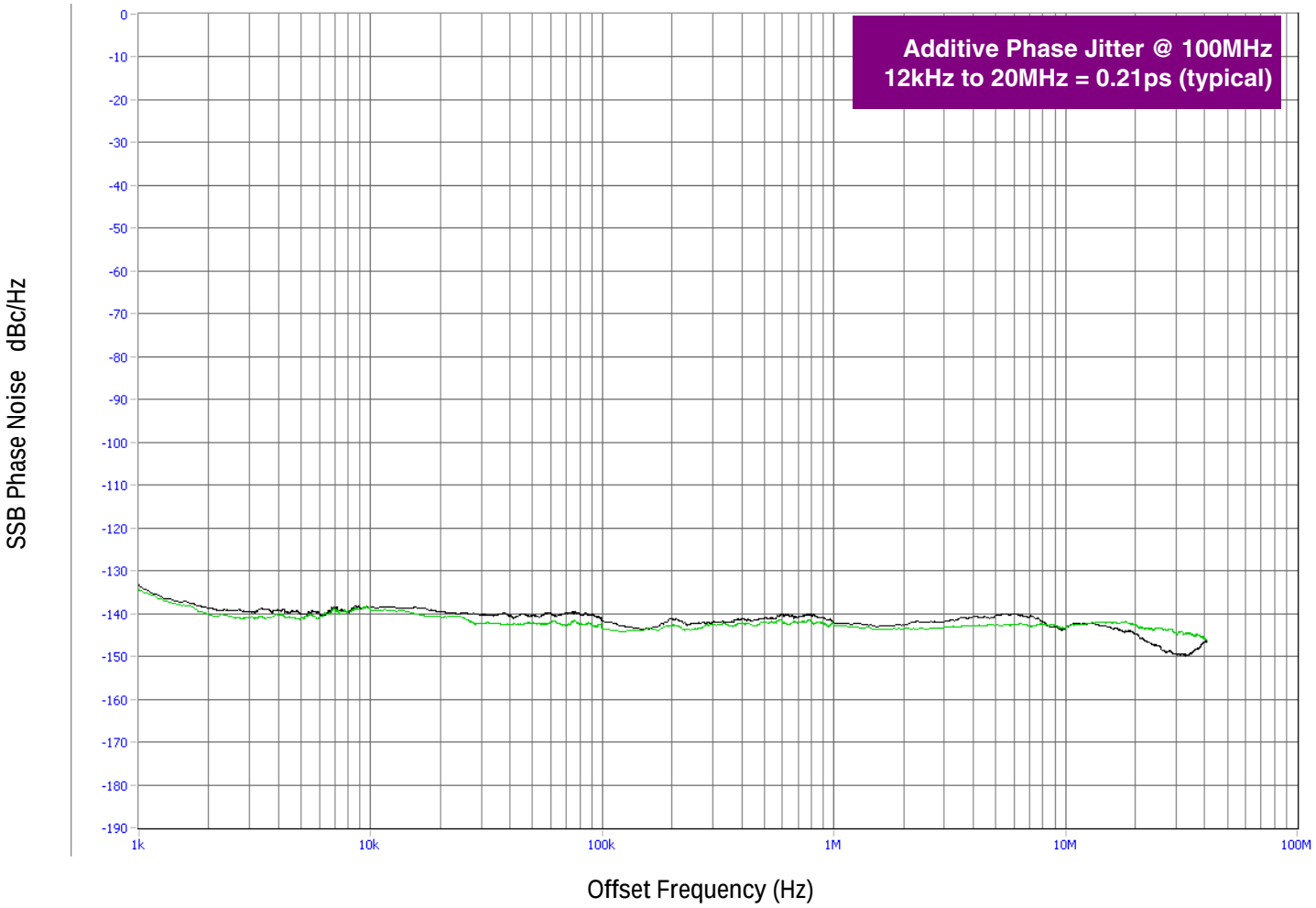
Parameter	Symbol	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency			350		MHz
t_{PD}	Propagation Delay, NOTE 1	$f \leq$ 350MHz	1.9	2.2	2.5	ns
*t*sk(pp)	Part-to-Part Skew; NOTE 2, 3				500	ps
*t*jit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section	100MHz, Integration Range (637kHz – 10MHz)		0.21		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	250		550	ps
odc	Output Duty Cycle	$f \leq$ 250MHz	45	50	55	%
		250MHz < $f \leq$ 350MHz	40	50	60	%

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
All parameters measured at f_{MAX} unless noted otherwise.
NOTE 1: Measured from the differential input crossing point to the output at $V_{DD}/2$.
NOTE 2: Defined as skew between outputs on different devices operating at the same supply voltage and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at $V_{DD}/2$.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

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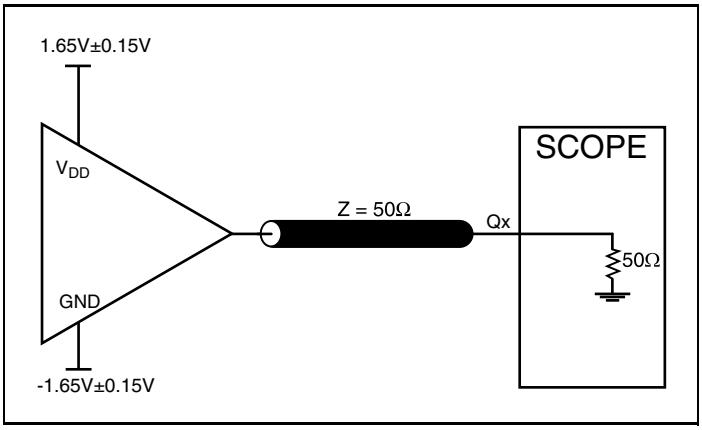
Additive Phase Jitter

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the ***dBc Phase Noise.*** This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a ***dBc*** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.

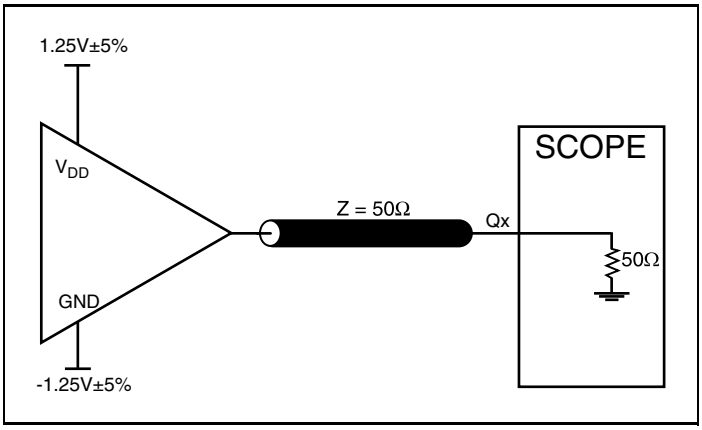


As with most timing specifications, phase noise measurements has issues relating to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This is illustrated above. The device meets the noise floor of what is shown, but can actually be lower. The phase noise is dependent on the input source and measurement equipment.

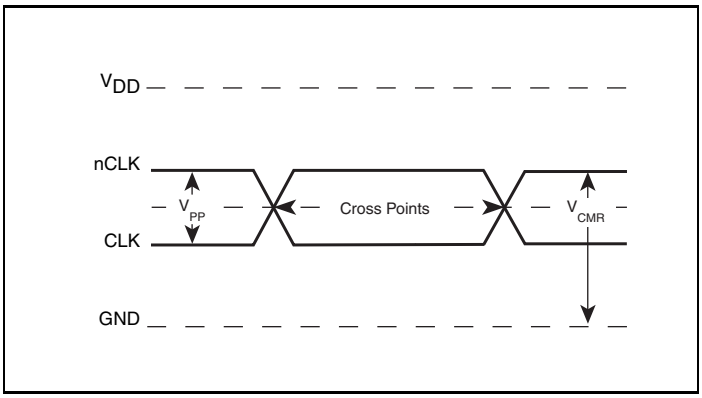
Parameter Measurement Information



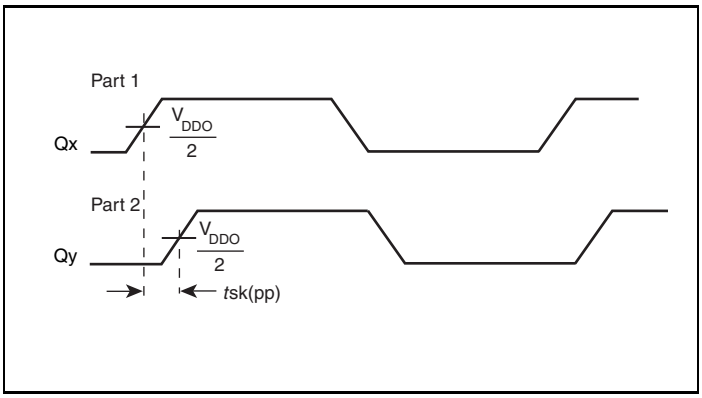
3.3V Core/3.3V LVCMOS Output Load AC Test Circuit



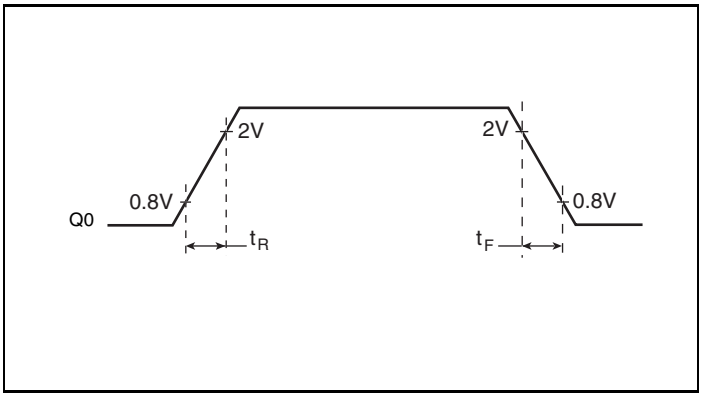
2.5V Core/2.5V LVCMOS Output Load AC Test Circuit



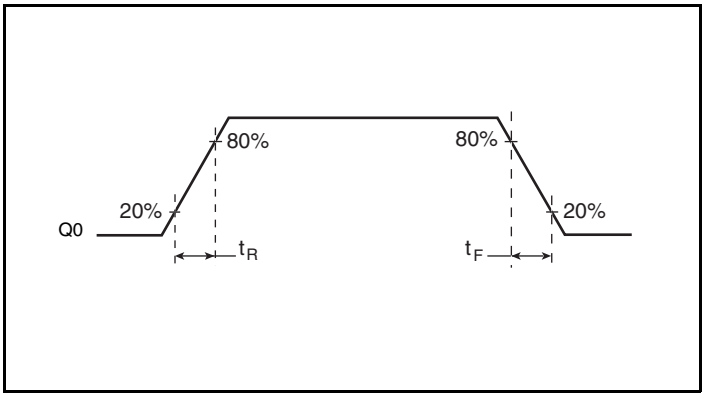
Differential Input Level



Part-to-Part Skew

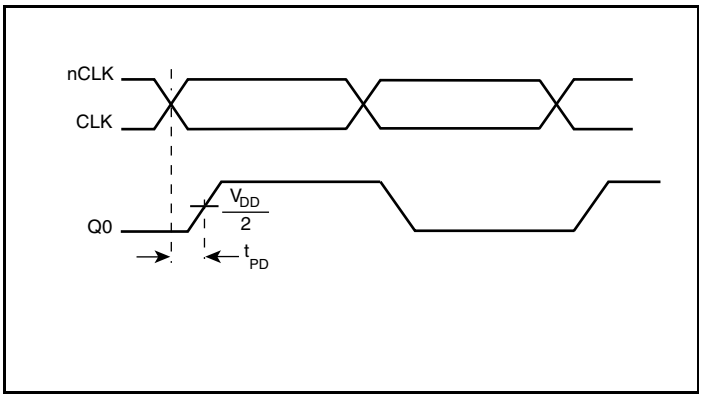


3.3V Output Rise/Fall Time

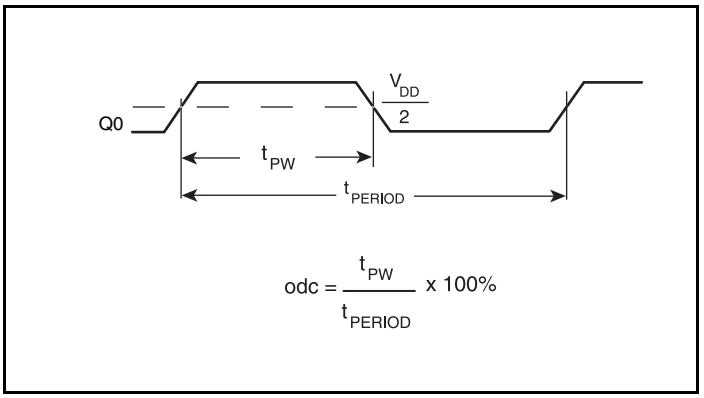


2.5V Output Rise/Fall Time

Parameter Measurement Information, continued



Propagation Delay



Output Duty Cycle/Pulse Width/Period

Application Information

Wiring the Differential Input to Accept Single Ended Levels

Figure 1 shows how the differential input can be wired to accept single ended levels. The reference voltage V_REF = V_{DD}/2 is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and V_{DD} = 3.3V, V_REF should be 1.25V and R2/R1 = 0.609.

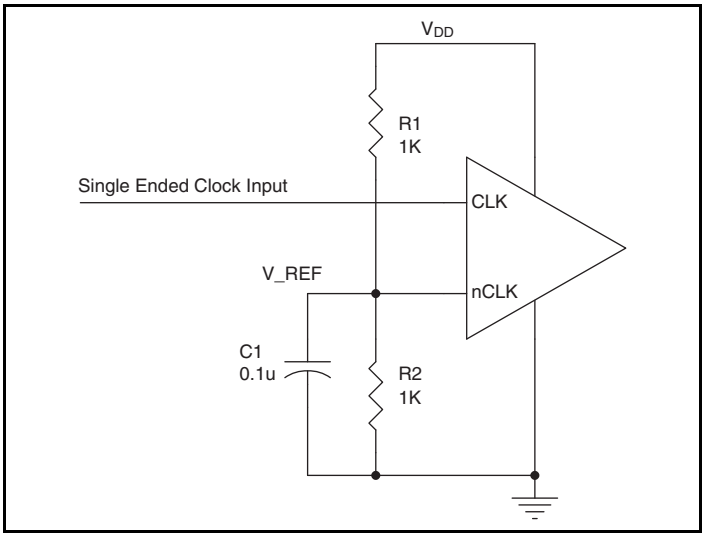


Figure 1. Single-Ended Signal Driving Differential Input

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Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, SSTL, HCSL and other differential signals. Both signals must meet the V_{PP} and V_{CMR} input requirements. *Figures 2A to 2F* show interface examples for the HiPerClockS CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example, in Figure 2A, the input termination applies for IDT HiPerClockS open emitter LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

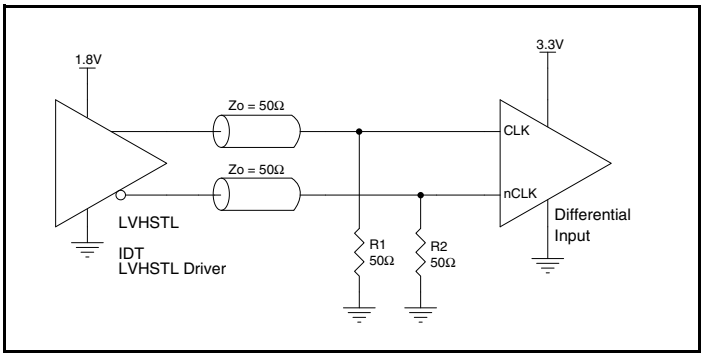


Figure 2A. HiPerClockS CLK/nCLK Input Driven by an IDT Open Emitter HiPerClockS LVHSTL Driver

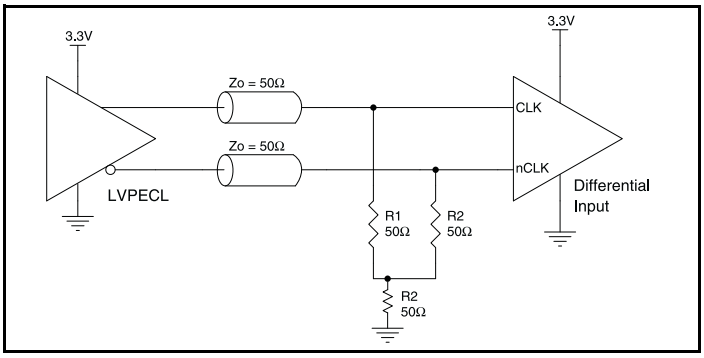


Figure 2B. HiPerClockS CLK/nCLK Input Driven by a 3.3V LVPECL Driver

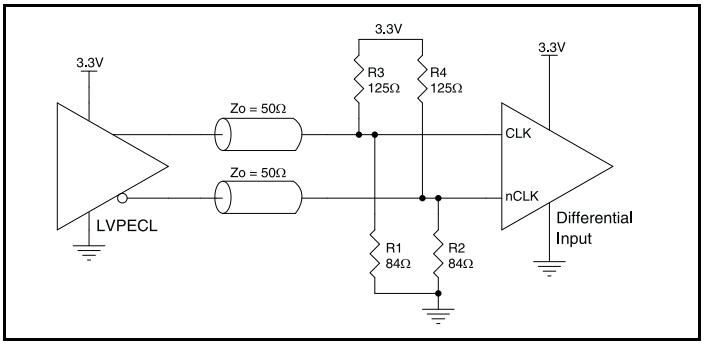


Figure 2C. HiPerClockS CLK/nCLK Input Driven by a 3.3V LVPECL Driver

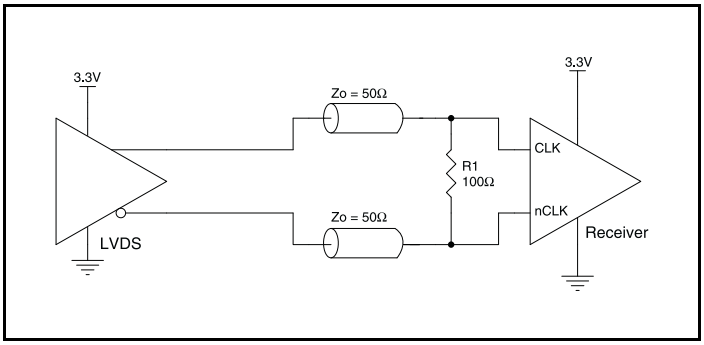


Figure 2D. HiPerClockS CLK/nCLK Input Driven by a 3.3V LVDS Driver

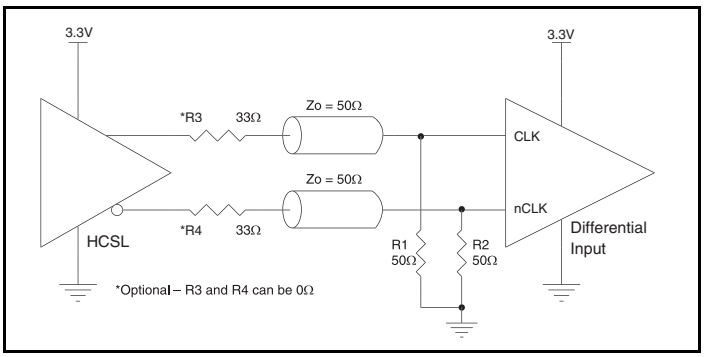


Figure 2E. HiPerClockS CLK/nCLK Input Driven by a 3.3V HCSL Driver

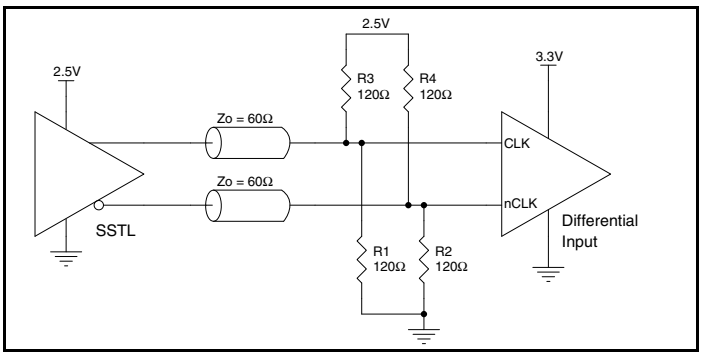


Figure 2F. HiPerClockS CLK/nCLK Input Driven by a 2.5V SSTL Driver

Reliability Information

Table 5. θ_{JA} vs. Air Flow Table for an 8 Lead SOIC

θ_{JA} by Velocity			
Linear Feet per Minute	**0**	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	123°C/W	110°C/W	99°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	103°C/W	94°C/W	89°C/W

Transistor Count

The transistor count for 83021I is: 416
Pin-to-pin compatible with the MC100EPT21

Package Outline and Package Dimensions

Package Outline - M Suffix for 8 Lead SOIC

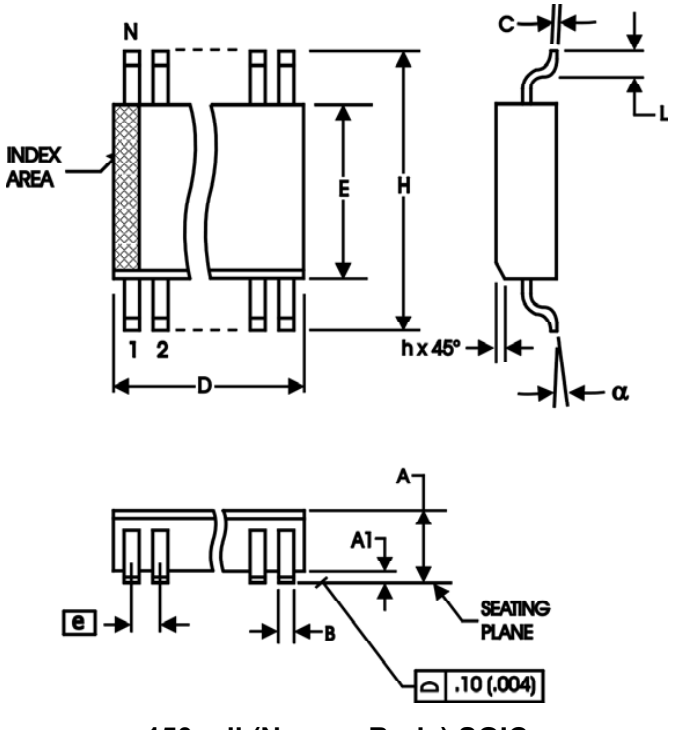


Table 6. Package Dimensions

All Dimensions in Millimeters		
Symbol	**Minimum**	**Maximum**
N	8	
A	1.35	1.75
A1	0.10	0.25
B	0.33	0.51
C	0.19	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 Basic	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.27
α	0°	8°

Reference Document: JEDEC Publication 95, MS-012

Ordering Information

Table 7. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
83021AMILF	83021AIL	“Lead-Free” 8 Lead SOIC	Tube	-40°C to 85°C
83021AMILFT	83021AIL	“Lead-Free” 8 Lead SOIC	Tape & Reel	-40°C to 85°C

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Revision History Sheet

Rev	Table	Page	Description of Change	Date
B	T2 T3B T3C T3D T4B	2 3 3 3 4 5 6 7	Pin Characteristics table - added 2.5V C_{PD}. Added 2.5V Power Supply table. LVCMOS table - added 2.5V V_{OH}. Differential table - added 2.5V. Added 2.5V AC Characteristics table. Added 2.5V Output Load AC Test Circuit Diagram, and 2.5V Output Rise/Fall Time Diagrams. Updated Figure 1. Added Differential Clock Input Interface section.	6/3/04
B	T4A	2 4	Pin Characteristics Table - changed C_{IN} 4pF max. to 4pF typical. 3.3V AC Characteristics Table - changed odc Test Conditions.	6/30/04
B	T7	1 10	Features Section - added Lead-Free bullet. Ordering Information Table - Added Lead-Free part number.	3/21/05
C	T4A, T4B T7	1 4 5 11	Features Section - added Additive Phase Jitter bullet. AC Characteristics Tables - added Additive Phase Jitter row. Added Additive Phase Jitter Plot. Added Lead-Free Note.	12/12/05
C		1 8 9	Pin Assignment - corrected package body measurements. Updated *Differential Clock Input Interface.* Updated *Reliability Information*. Updated datasheet format .	6/18/08
C	T4A, T4B	1 4	Corrected typo in Header from 1-to-2... to 1-to-1.... AC Tables - added Temperature NOTE.	10/31/08
D	T7	10	Remove leaded orderable parts from Ordering Information table	11/14/12
D		1	Features section - removed leaded part note. Description - removed chip	4/23/14
D	T7	1 10	Removed HiPerClockS from General Description. Ordering Information - removed 2500 from Tape and Reel. Updated Datasheet header and footer.	12/14/15

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