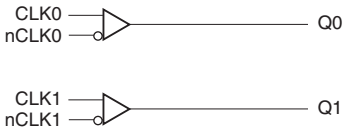
General Description

The 83023I is a dual, 1-to-1 Differential-to-LVCMOS Translator/Fanout Buffer. The differential inputs can accept most differential signal types (LVDS, LVHSTL, LVPECL, SSTL, and HCSL) and translate into two single-ended LVCMOS outputs. The small 8-lead SOIC footprint makes this device ideal for use in applications with limited board space.

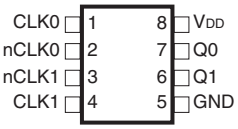
Features

- Two LVCMOS / LVTTL outputs
- Two differential CLKx, nCLKx input pairs
- CLK, nCLK pairs can accept the following differential input levels: LVDS, LVPECL, LVHSTL, SSTL, HCSL
- Maximum output frequency: 350MHz (typical)
- Output skew: 60ps (maximum)
- Part-to-part skew: 500ps (maximum)
- Additive phase jitter, RMS: 0.14ps (typical)
- Small 8 lead SOIC package saves board space
- 3.3V operating supply
- -40°C to 85°C ambient operating temperature

Block Diagram



Pin Assignment



83023I
8-Lead SOIC
3.8mm x 4.8mm x 1.47mm package body
M Package
Top View

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Table 1. Pin Descriptions

Number	Name	Type		Description
1	CLK0	Input	Pulldown	Non-inverting differential clock input.
2	nCLK0	Input	Pullup	Inverting differential clock input.
3	nCLK1	Input	Pullup	Inverting differential clock input.
4	CLK1	Input	Pulldown	Non-inverting differential clock input.
5	GND	Power		Power supply ground.
6	Q1	Output		Single clock output. LVCMOS / LVTTL interface levels.
7	Q0	Output		Single clock output. LVCMOS / LVTTL interface levels.
8	V_{DD}	Power		Positive supply pin.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
C_{PD}	Power Dissipation Capacitance (per output)	V_{DD} = 3.6V		23		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ
R_{OUT}	Output Impedance			7		Ω

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Absolute Maximum Ratings

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5 V
Outputs, V_O	-0.5V to V_{DD} + 0.5V
Package Thermal Impedance, θ_{JA}	112.7°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Table 3A. Power Supply DC Characteristics, V_{DD} = 3.3V±0.3V, TA = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Positive Supply Voltage		3.0	3.3	3.6	V
I_{DD}	Positive Supply Current				20	mA

Table 3B. LVCMOS / LVTTL DC Characteristics, V_{DD} = 3.3V±0.3V, TA = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		2.6			V
V_{OL}	Output Low Voltage; NOTE 1				0.5	V

NOTE 1: Outputs terminated with 50Ω to V_{DD}/2. See Parameter Measurement Section, 3.3V Output Load Test Circuit.

Table 3C. Differential DC Characteristics, V_{DD} = 3.3V±0.3V, TA = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	nCLK0, nCLK1	$V_{IN} = V_{DD}$ = 3.6V			5	µA
		CLK0, CLK1	$V_{IN} = V_{DD}$ = 3.6V			150	µA
I_{IL}	Input Low Current	nCLK0, nCLK1	V_{IN} = 0V, V_{DD} = 3.6V	-150			µA
		CLK0, CLK1	V_{IN} = 0V, V_{DD} = 3.6V	-5			µA
V_{PP}	Peak-to-Peak Input Voltage			0.15		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			GND + 0.5		V_{DD} - 0.85	V

NOTE 1: For single-ended applications, the maximum input voltage for CLKx, nCLKx is V_{DD} + 0.3V.
NOTE 2: Common mode voltage is defined as V_{IH}.

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TABLE 4. AC CHARACTERISTICS, V_{DD} = 3.3V±0.3V, T_A = -40°C TO 85°C

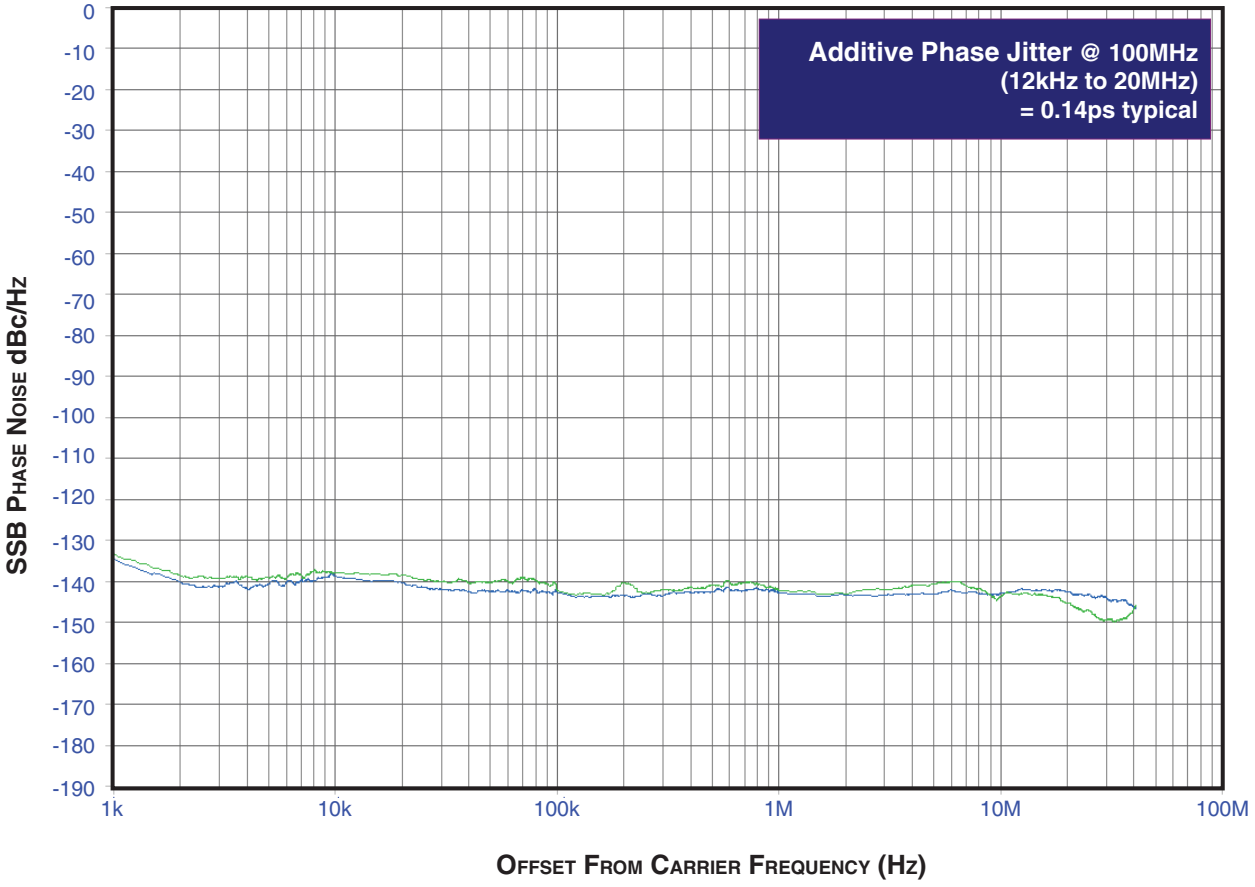
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Maximum Output Frequency			350		MHz
t_{PD}	Propagation Delay; NOTE 1		1.8	2.1	2.4	ns
*t*sk(o)	Output Skew; NOTE 2, 4				60	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 3, 4				500	ps
tjit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section	100MHz, Integration Range (637kHz-10MHz)		0.14		ps
t_R	Output Rise Time	0.8V to 2V	100	250	400	ps
t_F	Output Fall Time	0.8V to 2V	100	250	400	ps
odc	Output Duty Cycle	f ≤ 166MHz	45	50	55	%
		f > 166MHz	43	50	57	%

All parameters measured at f_{MAX} unless noted otherwise. See Parameter Measurement Information.
NOTE 1: Measured from the differential input crossing point to $V_{DD}/2$ of the output.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DD}/2$. Input clocks are phase aligned.
NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at $V_{DD}/2$.
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

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Additive Phase Jitter

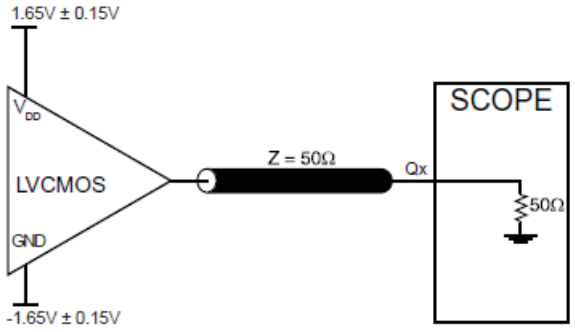
The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the ***dBc Phase Noise.*** This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a ***dBc*** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.



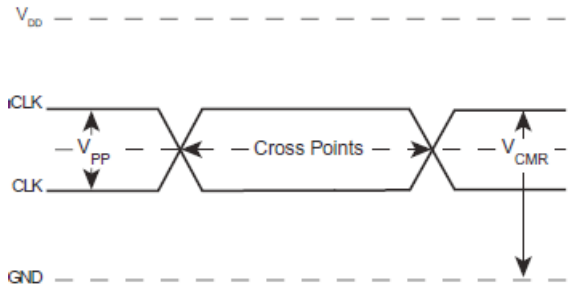
As with most timing specifications, phase noise measurements have issues. The primary issue relates to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This is illustrated above. The device meets the noise floor of what is shown, but can actually be lower. The phase noise is dependant on the input source and measurement equipment.

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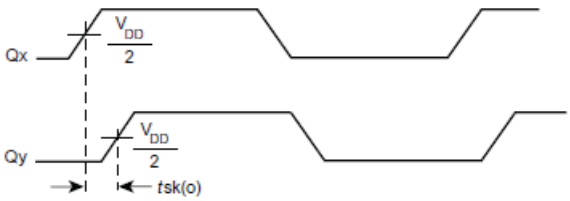
Parameter Measurement Information



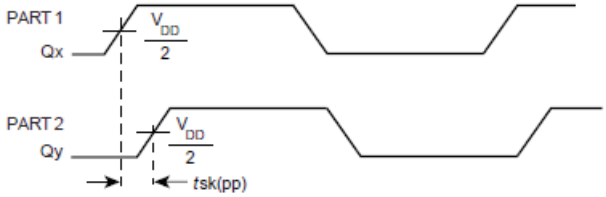
3.3V Output Load AC Test Circuit



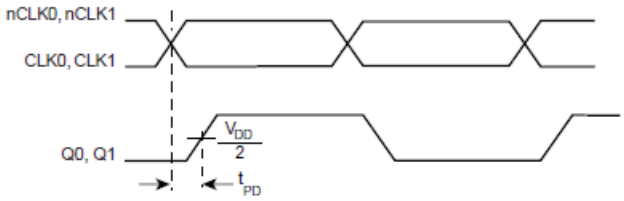
Differential Input Level



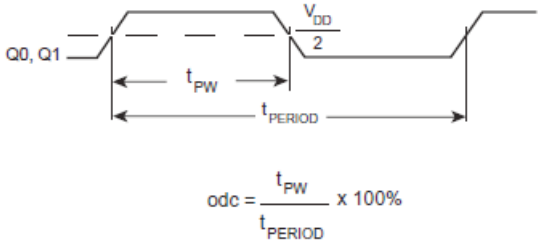
Output Skew



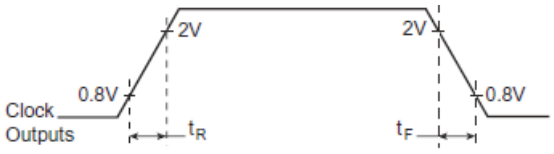
Part-to-Part Skew



Propagation Delay



Output Duty Cycle/Pulse Width/Period



Output Rise/Fall Time

Application Information

Wiring the Differential Input to Accept Single Ended Levels

Figure 1 shows how the differential input can be wired to accept single ended levels. The reference voltage V_REF = V_{DD}/2 is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and V_{DD} = 3.3V, V_REF should be 1.25V and R2/R1 = 0.609.

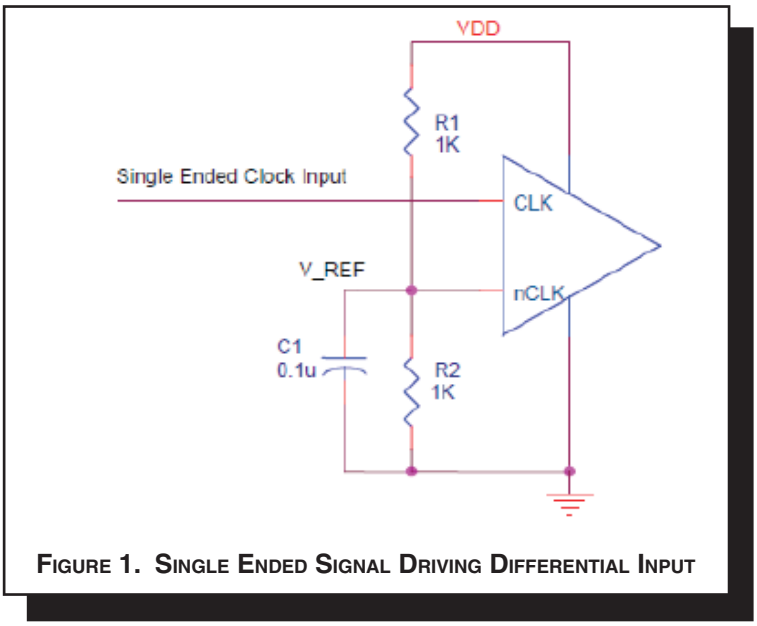


Figure 1. Single Ended Signal Driving Differential Input

Recommendations for Unused Input and Output Pins

Inputs:

CLK/nCLK Input:
For applications not requiring the use of the differential input, both CLK and nCLK can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from CLK to ground.

Outputs:

LVCMOS Output:
All unused LVCMOS output can be left floating. We recommend that there is no trace attached.

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Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, SSTL, HCSL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. Figures 2A to 2E show interface examples for the CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example in *Figure 2A,* the input termination applies for LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

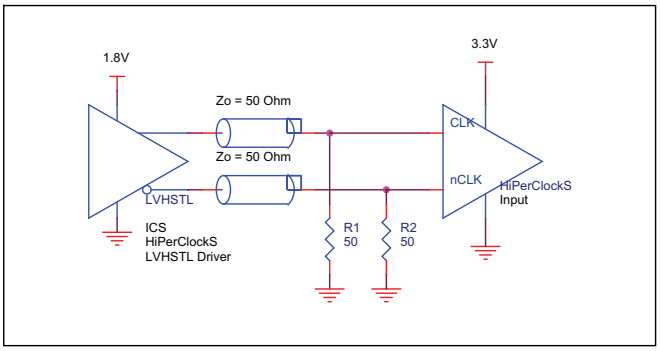


Figure 2A. CLK/nCLK Input Driven by LVHSTL Driver

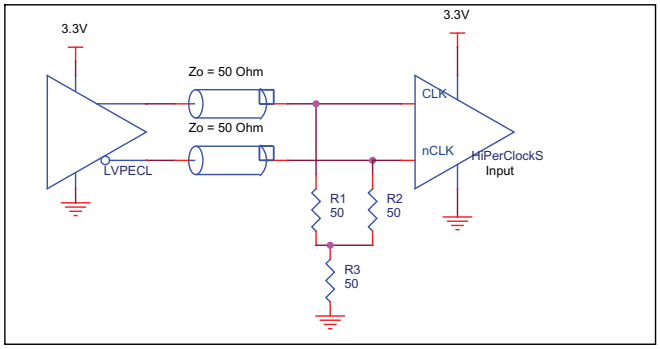


Figure 2B. CLK/nCLK Input Driven by 3.3V LVPECL Driver

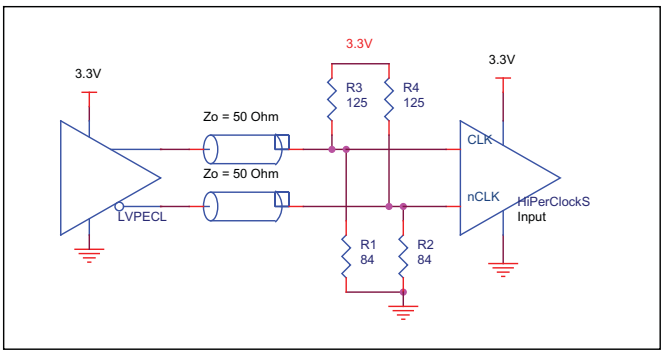


Figure 2C. CLK/nCLK Input Driven by 3.3V LVPECL Driver

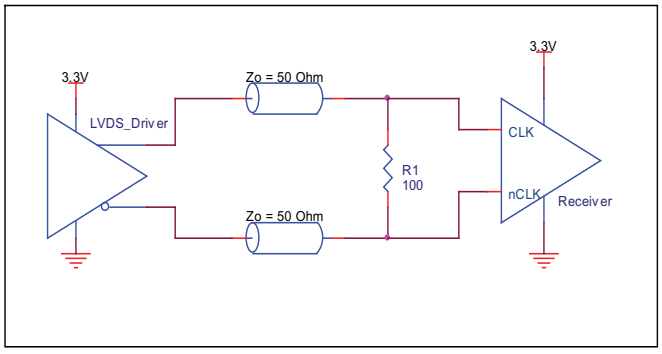


Figure 2D. CLK/nCLK Input Driven by 3.3V LVDS Driver

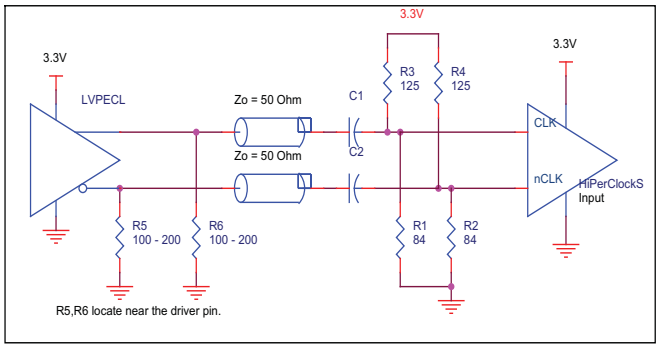


Figure 2E. CLK/nCLK Input Driven by 3.3V LVPECL Driver with AC Couple

RELIABILITY INFORMATION

TABLE 5. θ_{JA} VS. AIR FLOW TABLE FOR 8 LEAD SOIC

θ_{JA} by Velocity (Linear Feet per Minute)			
0	**200**	**500**	
Single-Layer PCB, JEDEC Standard Test Boards	153.3°C/W	128.5°C/W	115.5°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	112.7°C/W	103.3°C/W	97.1°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TRANSISTOR COUNT

The transistor count for 83023I is: 416

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Package Outline - Suffix M for 8 Lead SOIC

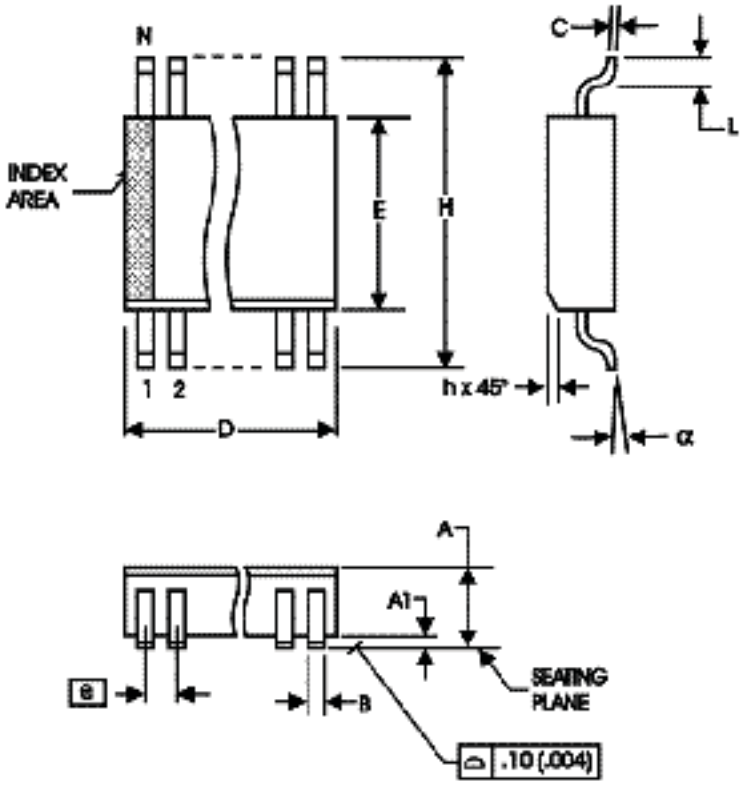


Table 6. Package Dimensions

SYMBOL	Millimeters	
	MINIMUN	MAXIMUM
N	8	
A	1.35	1.75
A1	0.10	0.25
B	0.33	0.51
C	0.19	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BASIC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.27
α	0°	8°

Reference Document: JEDEC Publication 95, MS-012

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TABLE 7. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
83023AMILF	83023AIL	8 lead “Lead Free” SOIC	Tube	-40°C to +85°C
83023AMILFT	83023AIL	8 lead “Lead Free” SOIC	Tape and Reel	-40°C to +85°C

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REVISION HISTORY SHEET				
Rev	**Table**	**Page**	**Description of Change**	**Date**
A	7	11	Ordering Information Table - corrected Part/Order Number for Tape & Reel to read ICS83023AMIT from ICS83023AMI.	09/09/02
B	T2 T4 T7	1 2 4 5 7 8 11	Features Section - added Additive Phase Jitter and Lead-Free bullets. Pin Characteristics Table - changed C_{IN} from 4pF max. to 4pF typical. AC Characteristics Table - added Additive Phase Jitter row. Added Additive Phase Jitter Plot. Added Recommendations for Unused Input and Output Pins. Added Differential Clock Input Interface. Ordering Information Table - added Lead-Free Part Number and Note. Update datasheet format.	12/12/05
B	T7	11	Ordering information Table - added Lead-Free marking.	1/18/08
B	T7	11 13	Updated datasheet's header/footer with IDT from ICS. Removed ICS prefix from Part/Order Number column. Added Contact Page.	7/29/10
B		1	Features Section - removed leaded note	4/23/14
B			Removed ICS from part numbers. Updated datasheet header and footer.	12/14/15

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

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