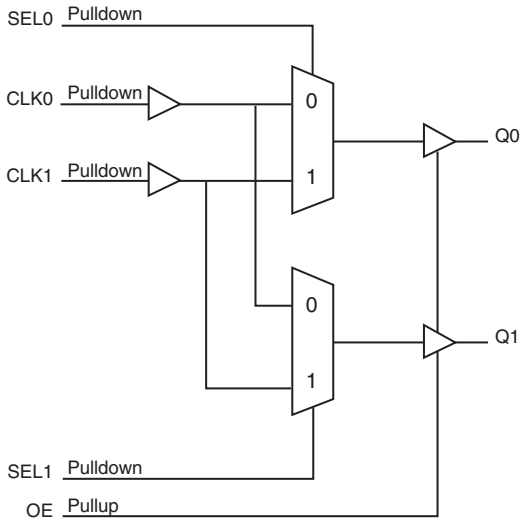
General Description

The 83052I-01 is a 2-bit, 2:1, Single-ended Multiplexer and a member of the family of High Performance Clock Solutions from IDT. The 83052I-01 has two selectable single-ended clock inputs and two single-ended clock outputs. The output has a V_{DDO} pin which may be set at 3.3V, 2.5V, or 1.8V, making the device ideal for use in voltage translation applications. An output enable pin places the output in a high impedance state which may be useful for testing or debug. Possible applications include systems with up to two transceivers which need to be independently set for different rates. For example, a board may have two transceivers, each of which need to be independently configured for 1 Gigabit Ethernet or 1 Gigabit Fibre Channel rates. Another possible application may require the ports to be independently set for FEC (Forward Error Correction) or non-FEC rates. The device operates up to 250MHz and is packaged in a 16 TSSOP.

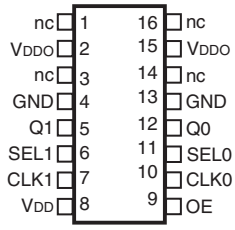
Features

- 2-bit, 2:1 single-ended multiplexer
- Nominal output impedance: 15Ω (V_{DDO} = 3.3V)
- Maximum output frequency: 250MHz
- Propagation delay: 3ns (maximum), V_{DD} = V_{DDO} = 3.3V
- Input skew: 85ps (maximum), V_{DD} = V_{DDO} = 3.3V
- Part-to-part skew: 500ps (maximum), V_{DD} = V_{DDO} = 3.3V
- Output skew: 65ps (maximum), V_{DD} = V_{DDO} = 3.3V
- Additive phase jitter, RMS (12KHz - 20MHz): 0.15ps (typical)
- Operating supply modes:
  V_{DD}/V_{DDO}
  3.3V/3.3V
  3.3V/2.5V
  3.3V/1.8V
  2.5V/2.5V
  2.5V/1.8V
- -40°C to 85°C ambient operating temperature
- Available in lead-free (RoHS 6) package

Block Diagram



Pin Assignment



83052I-01

16-Lead TSSOP
4.4mm x 5.0mm x 0.925mm
package body
G Package

Table 1. Pin Descriptions

Number	Name	Type		Description
1, 3, 14, 16	nc	Unused		No connect.
2, 15	V_{DDO}	Power		Output supply pins.
4, 13	GND	Power		Power supply ground
5, 12	Q1, Q0	Output		Single-ended clock outputs. LVCMOS/LVTTL interface levels.
6, 11	SEL1, SEL0	Input	Pulldown	Clock select inputs. See Table 3, Control Input Function Table. LVCMOS / LVTTL interface levels.
7, 10	CLK1, CLK0	Input	Pulldown	Single-ended clock input. LVCMOS/LVTTL interface levels.
8	V_{DD}	Power		Power supply pin.
9	OE	Input	Pullup	Output enable. When LOW, outputs are in HIGH impedance state. When HIGH, outputs are active. LVCMOS / LVTTL interface levels.

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ
C_{PD}	Power Dissipation Capacitance (per output); NOTE 1	V_{DDO} = 3.465V		18		pF
		V_{DDO} = 2.625V		19		pF
		V_{DDO} = 2.0V		19		pF
R_{OUT}	Output Impedance	V_{DDO} = 3.465V		15		Ω
		V_{DDO} = 2.625V		17		Ω
		V_{DDO} = 2.0V		25		Ω

Function Tables

Table 3. Control Input Function Table

Control Inputs		Outputs	
SEL1	SEL0	Q0	Q1
0	0	CLK0 (default)	CLK0
0	1	CLK1	CLK0
1	0	CLK0	CLK1
1	1	CLK1	CLK1

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Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{CC}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5V
Outputs, V_O	-0.5V to V_{DDO}+ 0.5V
Package Thermal Impedance, θ_{JA}	100.3°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, V_{DD} = 3.3V ± 5%, V_{DDO} = 3.3V ± 5% or 2.5V ± 5% or 1.8V ± 0.2V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Positive Supply Voltage		3.135	3.3	3.465	V
V_{DDO}	Output Supply Voltage		3.135	3.3	3.465	V
			2.375	2.5	2.625	V
			1.6	1.8	2.0	V
I_{DD}	Power Supply Current				40	mA
I_{DDO}	Output Supply Current	No Load			5	mA

Table 4B. Power Supply DC Characteristics, V_{DD} = 2.5V ± 5%, V_{DDO} = 2.5V ± 5% or 1.8V ± 0.2V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Positive Supply Voltage		2.375	2.5	2.625	V
V_{DDO}	Output Supply Voltage		2.375	2.5	2.625	V
			1.6	1.8	2.0	V
I_{DD}	Power Supply Current				40	mA
I_{DDO}	Output Supply Current	No Load			5	mA

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Table 4C. LVCMOS/LVTTL DC Characteristics, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		V_{DD} = 3.465V	2		V_{DD} + 0.3	V
			V_{DD} = 2.625V	1.7		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage		V_{DD} = 3.465V	-0.3		1.3	V
			V_{DD} = 2.625V	-0.3		0.7	V
I_{IH}	Input High Current	CLK0, CLK1, SEL0, SEL1	V_{DD} = V_{IN} = 3.465V or 2.625V			150	µA
		OE	V_{DD} = V_{IN} = 3.465V or 2.625V			5	µA
I_{IL}	Input Low Current	CLK0, CLK1, SEL0, SEL1	V_{DD} = 3.465V or 2.625V, V_{IN} = 0V	-5			µA
		OE	V_{DD} = 3.465V or 2.625V, V_{IN} = 0V	-150			µA
V_{OH}	Output High Voltage; NOTE 1		V_{DDO} = 3.3V ± 5%	2.6			V
			V_{DDO} = 2.5V ± 5%	1.8			V
			V_{DDO} = 1.8V ± 0.2V	V_{DDO} - 0.3			V
V_{OL}	Output Low Voltage; NOTE 1		V_{DDO} = 3.3V ± 5%			0.5	V
			V_{DDO} = 2.5V ± 5%			0.45	V
			V_{DDO} = 1.8V ± 0.2V	-5		0.35	V

NOTE 1: Outputs terminated with 50Ω to V_{DDO}/2. See Parameter Measurement Information, *Output Load Test Circuit diagrams.*

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AC Electrical Characteristics

Table 5A. AC Characteristics, V_{DD} = V_{DDO} = 3.3V ± 5%, T_A =-40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				250	MHz
tp_{LH}	Propagation Delay, Low to High; NOTE 1		2.0	2.45	3.0	ns
tp_{HL}	Propagation Delay, High to Low; NOTE 1		2.0	2.45	3.0	ns
*t*sk(i)	Input Skew; NOTE 2			20	85	ps
*t*sk(o)	Output Skew; NOTE 2, 3			15	65	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 2, 4				500	ps
*t*jit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter section, NOTE 5	Integration Range: 12kHz - 20MHz		0.15		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	200		600	ps
odc	Output Duty Cycle		40		60	%
MUX_{ISOL}	MUX Isolation	Unselected CLK input @100MHz		45		dB

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions
NOTE 1: Measured from the V_{DD}/2 of the input to V_{DDO}/2 of the output.
NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at V_{DDO}/2.
NOTE 4: Defined as skew between outputs on different devices operating at the same supply voltage and with equal load conditions. Using the same input on each device, the output is measured at V_{DDO}/2.
NOTE 5: Driving only one input clock.

Table 5B. AC Characteristics, V_{DD} = 3.3V ± 5%, V_{DDO} = 2.5V ± 5%, T_A =-40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				250	MHz
tp_{LH}	Propagation Delay, Low to High; NOTE 1		2.2	2.55	3.0	ns
tp_{HL}	Propagation Delay, High to Low; NOTE 1		2.2	2.55	3.0	ns
*t*sk(i)	Input Skew; NOTE 2			10	50	ps
*t*sk(o)	Output Skew; NOTE 2, 3			20	70	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 2, 4				500	ps
*t*jit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter section, NOTE 5	Integration Range: 12kHz - 20MHz		0.12		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	200		600	ps
odc	Output Duty Cycle		40		60	%
MUX_{ISOL}	MUX Isolation	Unselected CLK input @100MHz		45		dB

NOTE: See Notes above.

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Table 5C. AC Characteristics, V_{DD} = 3.3V ± 5%, V_{DDO} = 1.8V ± 0.2V, T_A =-40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				250	MHz
tp_{LH}	Propagation Delay, Low to High; NOTE 1		2.2	3.1	4.0	ns
tp_{HL}	Propagation Delay, High to Low; NOTE 1		2.2	3.1	4.0	ns
*t*sk(i)	Input Skew; NOTE 2			15	60	ps
*t*sk(o)	Output Skew; NOTE 2, 3			30	100	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 2, 4				500	ps
*t*jit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter section, NOTE 5	Integration Range: 12kHz - 20MHz		0.14		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	150		1000	ps
odc	Output Duty Cycle	f_{OUT} < 200MHz	40		60	%
MUX_{ISOL}	MUX Isolation	Unselected CLK input @100MHz		45		dB

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions
NOTE 1: Measured from the V_{DD}/2 of the input to V_{DDO}/2 of the output.
NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at V_{DDO}/2.
NOTE 4: Defined as skew between outputs on different devices operating at the same supply voltage and with equal load conditions. Using the same input on each device, the output is measured at V_{DDO}/2.
NOTE 5: Driving only one input clock.

Table 5D. AC Characteristics, V_{DD} = V_{DDO} = 2.5V ± 5%, T_A =-40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				250	MHz
tp_{LH}	Propagation Delay, Low to High; NOTE 1		2.0	2.7	3.4	ns
tp_{HL}	Propagation Delay, High to Low; NOTE 1		2.0	2.7	3.4	ns
*t*sk(i)	Input Skew; NOTE 2			15	55	ps
*t*sk(o)	Output Skew; NOTE 2, 3			20	75	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 2, 4				500	ps
*t*jit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter section, NOTE 5	Integration Range: 12kHz - 20MHz		0.19		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	200		600	ps
odc	Output Duty Cycle		40		60	%
MUX_{ISOL}	MUX Isolation	Unselected CLK input @100MHz		45		dB

NOTE: See Notes above.

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Table 5E. AC Characteristics, V_{DD} = 2.5V ± 5%, V_{DDO} = 1.8V ± 0.2V, T_A =-40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				250	MHz
tp_{LH}	Propagation Delay, Low to High; NOTE 1		2.0	3.1	4.2	ns
tp_{HL}	Propagation Delay, High to Low; NOTE 1		2.0	3.1	4.2	ns
*t*sk(i)	Input Skew; NOTE 2			30	135	ps
*t*sk(o)	Output Skew; NOTE 2, 3			30	95	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 2, 4				500	ps
*t*jit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter section, NOTE 5	Integration Range: 12kHz - 20MHz		0.17		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	150		1000	ps
odc	Output Duty Cycle		40		60	%
MUX_{ISOL}	MUX Isolation	Unselected CLK input @100MHz		45		dB

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions

NOTE 1: Measured from the V_{DD}/2 of the input to V_{DDO}/2 of the output.

NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at V_{DDO}/2.

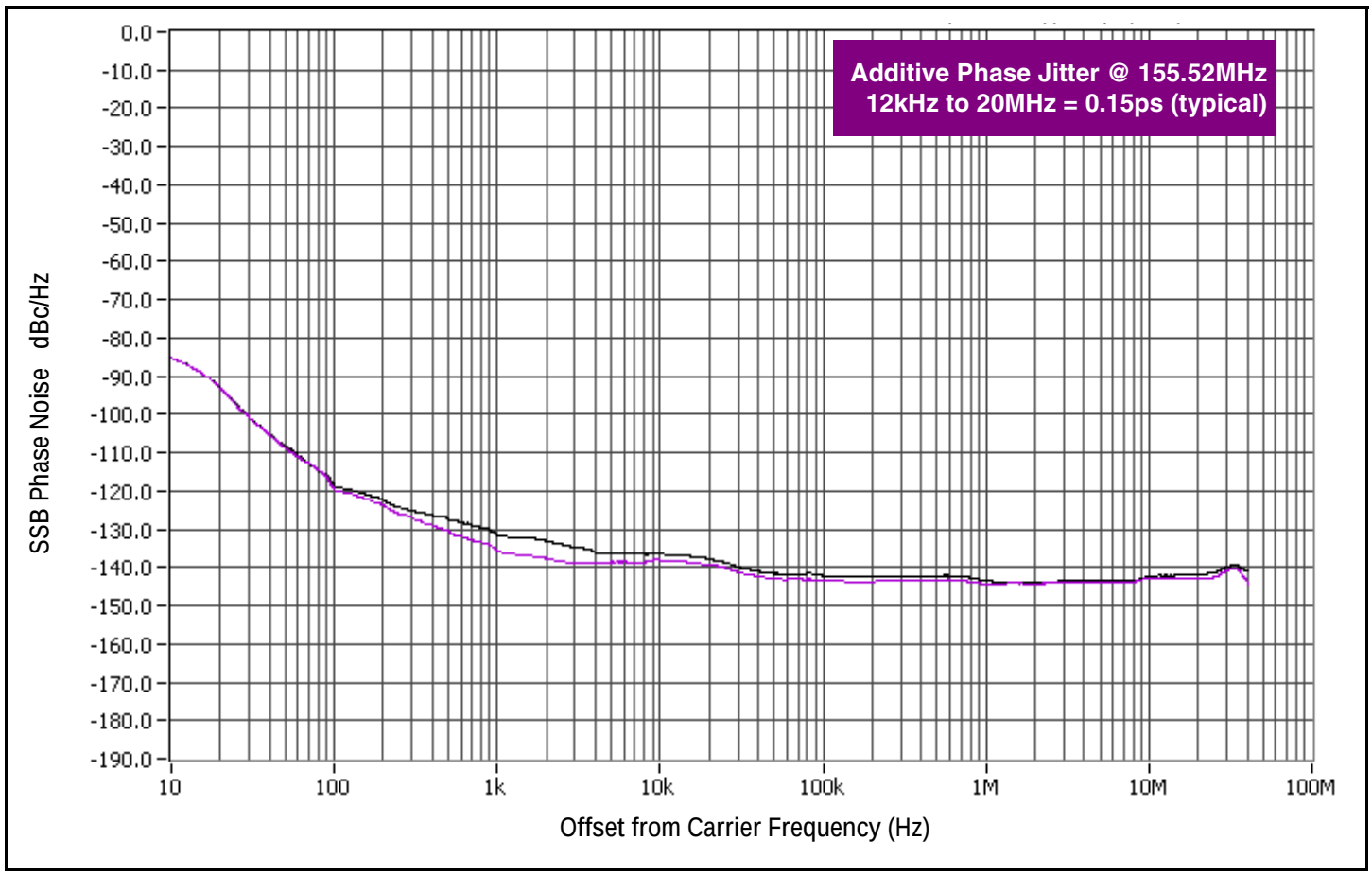
NOTE 4: Defined as skew between outputs on different devices operating at the same supply voltage and with equal load conditions. Using the same input on each device, the output is measured at V_{DDO}/2.

NOTE 5: Driving only one input clock.

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Additive Phase Jitter

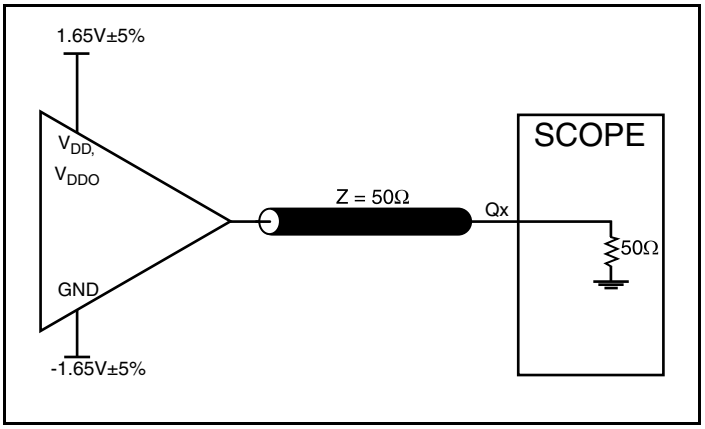
The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the ***dBc Phase Noise.*** This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a ***dBc*** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.



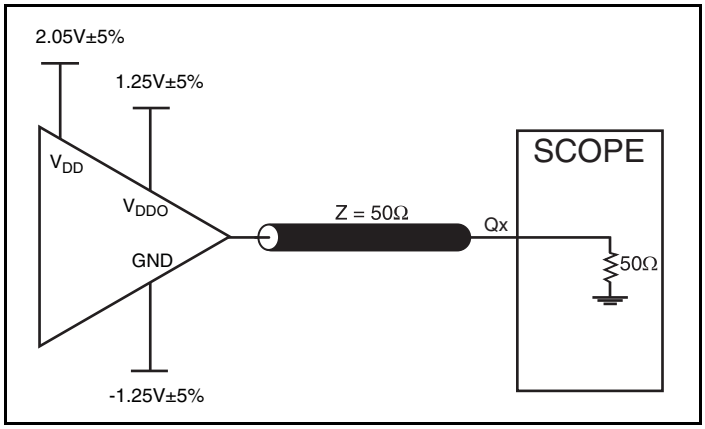
As with most timing specifications, phase noise measurements has issues relating to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This is illustrated above. The device meets the noise floor of what is shown, but can actually be lower. The phase noise is dependent on the input source and measurement equipment.

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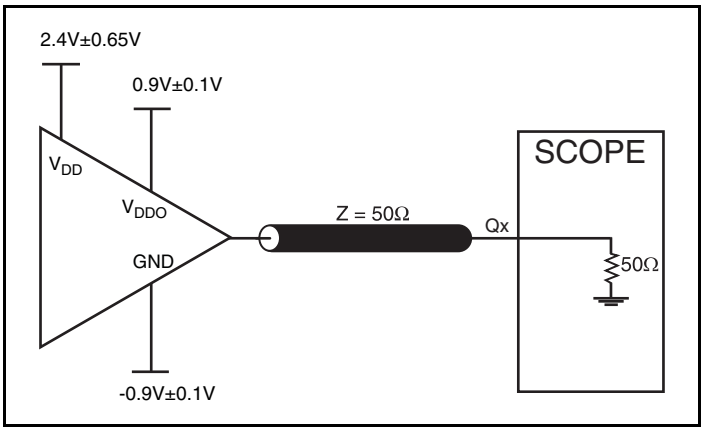
Parameter Measurement Information



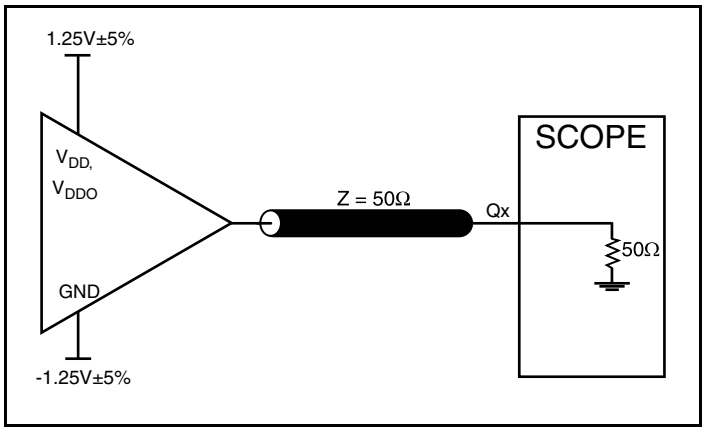
3.3V Core/3.3V LVCMOS Output Load AC Test Circuit



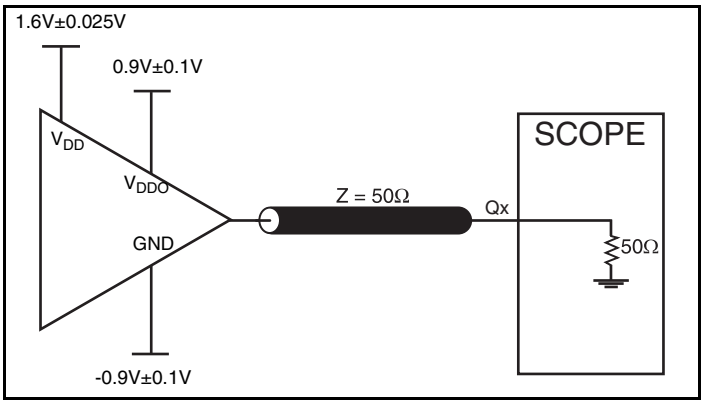
3.3V Core/2.5V LVCMOS Output Load AC Test Circuit



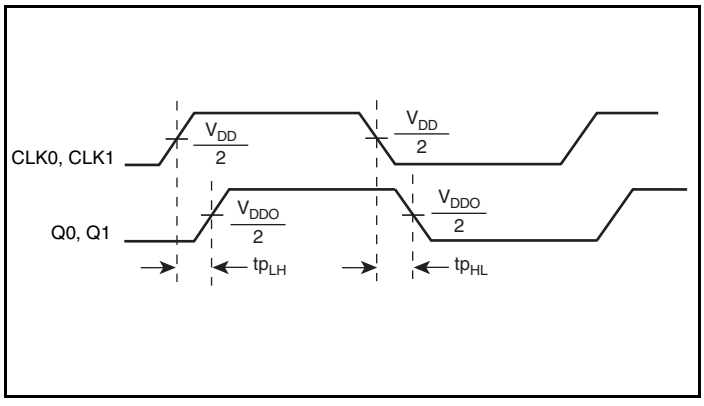
3.3V Core/ 1.8V LVCMOS Output Load AC Test Circuit



2.5V Core/ 2.5V LVCMOS Output Load AC Test Circuit

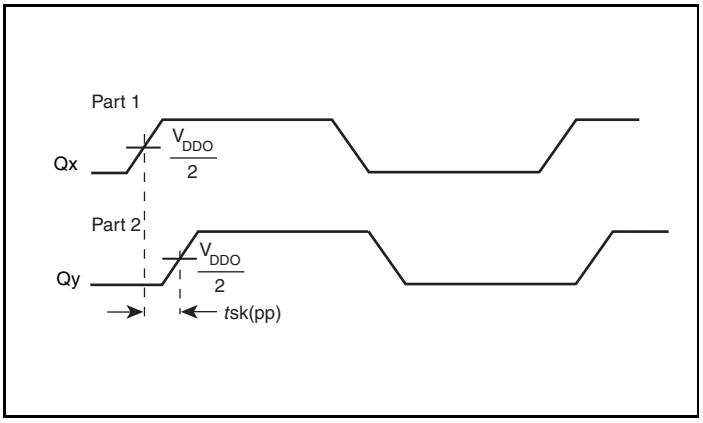


2.5V Core/ 1.8V LVCMOS Output Load AC Test Circuit

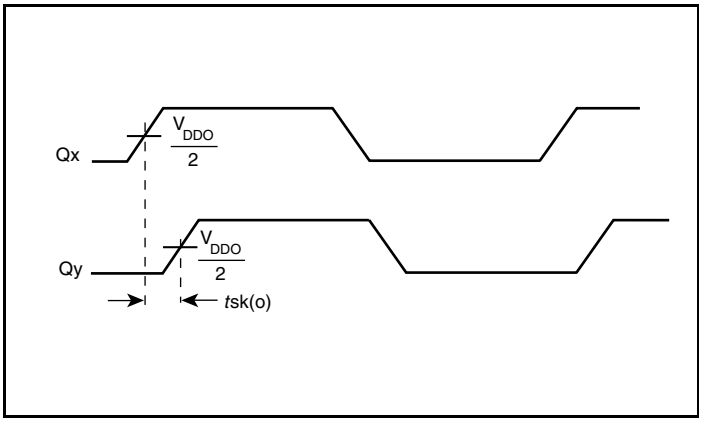


Propagation Delay

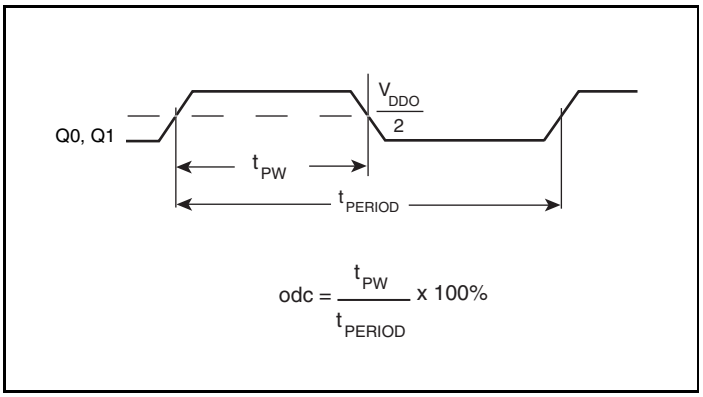
Parameter Measurement Information, continued



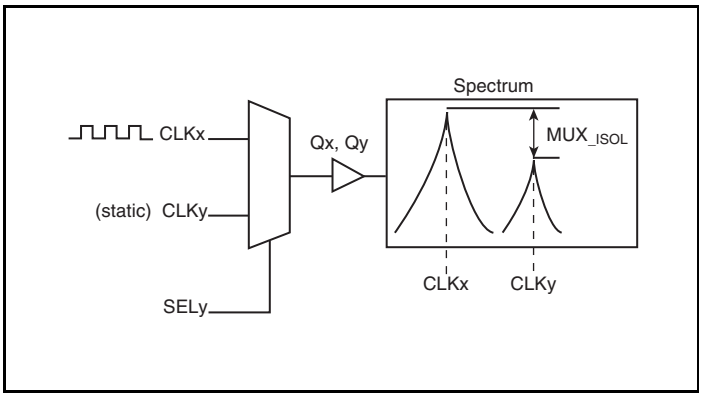
Part-to-Part Skew



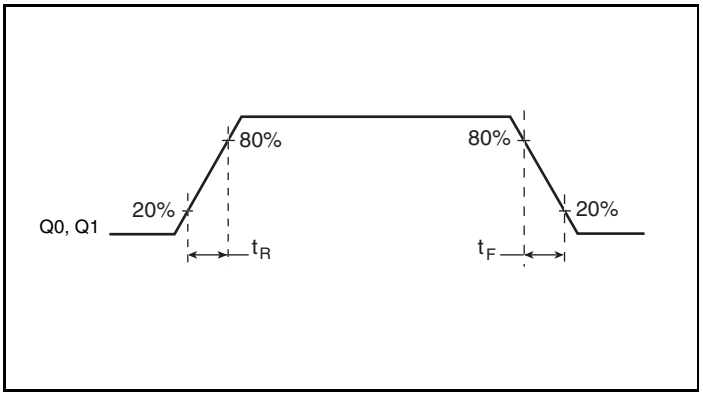
Output Skew



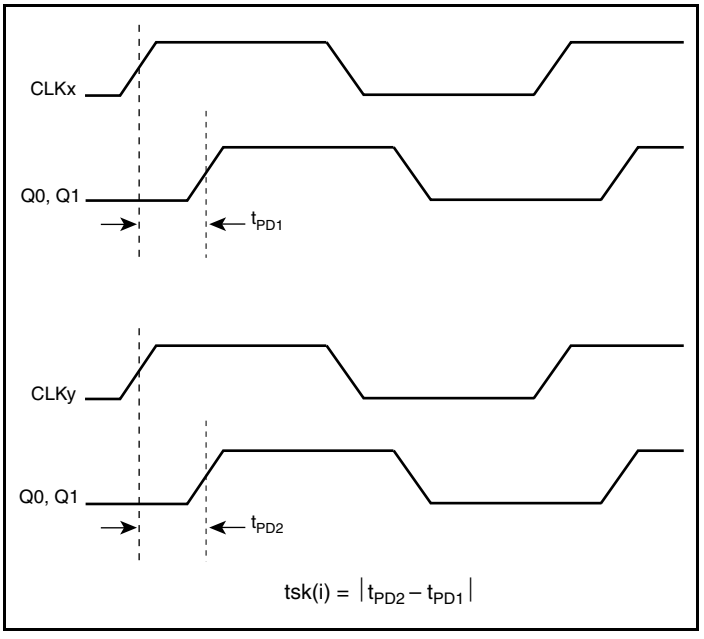
Output Duty Cycle/Pulse Width/Period



MUX Isolation



Output Rise/Fall Time



Input Skew

Application Information

Recommendations for Unused Input and Output Pins

Inputs:

LVCMOS Control Pins

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

CLK Inputs

For applications not requiring the use of a clock input, it can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from the CLK input to ground.

Outputs:

LVCMOS Outputs

All unused LVCMOS output can be left floating. There should be no trace attached.

Reliability Information

Table 6. θ_{JA} vs. Air Flow Table for a 16 Lead TSSOP

θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	100.3°C/W	96.0°C/W	93.9°C/W

NOTE: Most modern PCB design use multi-layered boards. The data in the second row pertains to most designs.

Transistor Count

The transistor count for 83052I-01is: 967

Package Outline and Package Dimensions

Package Outline - G Suffix for 16 Lead TSSOP

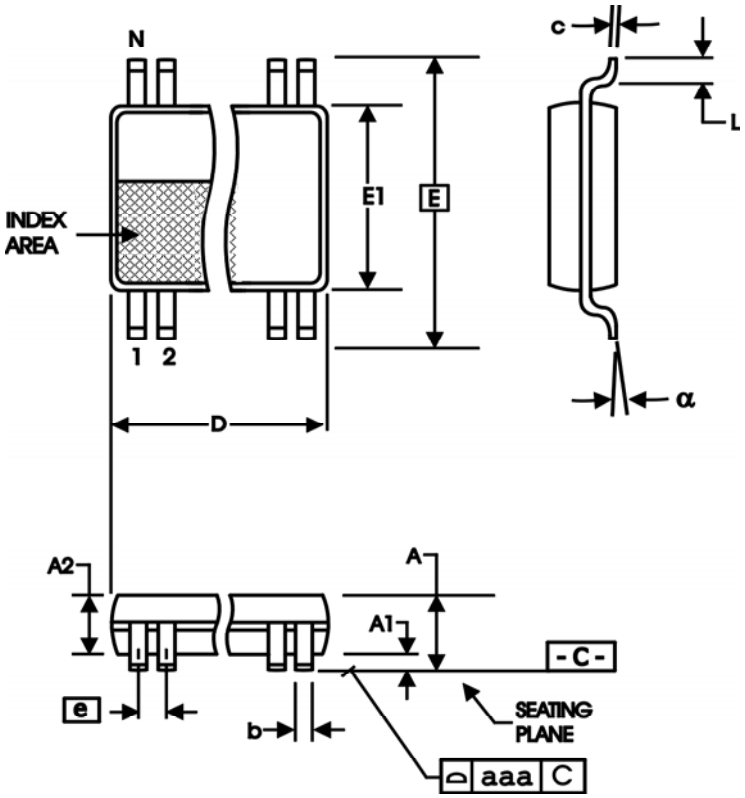


Table 7. Package Dimensions for 16 Lead TSSOP

All Dimensions in Millimeters		
Symbol	**Minimum**	**Maximum**
N	16	
A		1.20
A1	0.5	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	4.90	5.10
E	6.40 Basic	
E1	4.30	4.50
e	0.65 Basic	
L	0.45	0.75
α	0°	8°
aaa		0.10

Reference Document: JEDEC Publication 95, MO-153

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Ordering Information

Table 8. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
83052AGI-01LF	052AI01L	“Lead-Free” 16 Lead TSSOP	Tube	-40°C to 85°C
83052AGI-01LFT	052AI01L	“Lead-Free” 16 Lead TSSOP	Tape & Reel	-40°C to 85°C

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Revision History Sheet

Rev	Table	Page	Description of Change	Date
A	T3	2	Corrected *Control Input Function Table.*	7/25/08
A	T8	13	Ordering Information Table - deleted “ICS” prefix from Part/Order Number column.	3/9/09
A	T8	13	Removed leaded orderable parts from Ordering Information table	11/14/12
A	 T8	1 1 13	Features Section - removed reference to leaded packages. General Description - removed ICS Chip and HiPerClockS. Remove prefix of ICS on the part number. Removed LF note below the table. Updated header and footer.	12/16/15

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