# 6-BIT, 2:1, SINGLE-ENDED LVCMOS MULTIPLEXER

# ICS83056I-01

## General Description

The ICS83056I-01 is a 6-bit, 2:1, Single-ended LVCMOS Multiplexer and a member of the HiPerClockS™ family of High Performance Clock Solutions from IDT. The ICS83056I-01 has two selectable single-ended LVCMOS clock inputs and six single-ended LVCMOS clock outputs. The outputs have a $V_{DDO}$ which may be set at 3.3V, 2.5V, or 1.8V, making the device ideal for use in voltage translation applications. An output enable pin places the output in a high impedance state which may be useful for testing or debug. Possible applications include systems with up to 6 transceivers which need to be independently set for different rates. For example, a board may have six transceivers, each of which need to be independently configured for 1 Gigabit Ethernet or 1 Gigabit Fibre Channel rates. Another possible application may require the ports to be independently set for FEC (Forward Error Correction) or non-FEC rates. The device operates up to 250MHz and is packaged in a 20 TSSOP.

## Features

- 6-Bit, 2:1 single-ended LVCMOS multiplexer
- Maximum output frequency: 250MHz
- Additive phase jitter, RMS at 155.52MHz (12kHz - 20MHz): 0.18ps (typical)
- Operating supply modes:

  Core/Output

  $V_{DD}/V_{DDO}$

  3.3V/3.3V

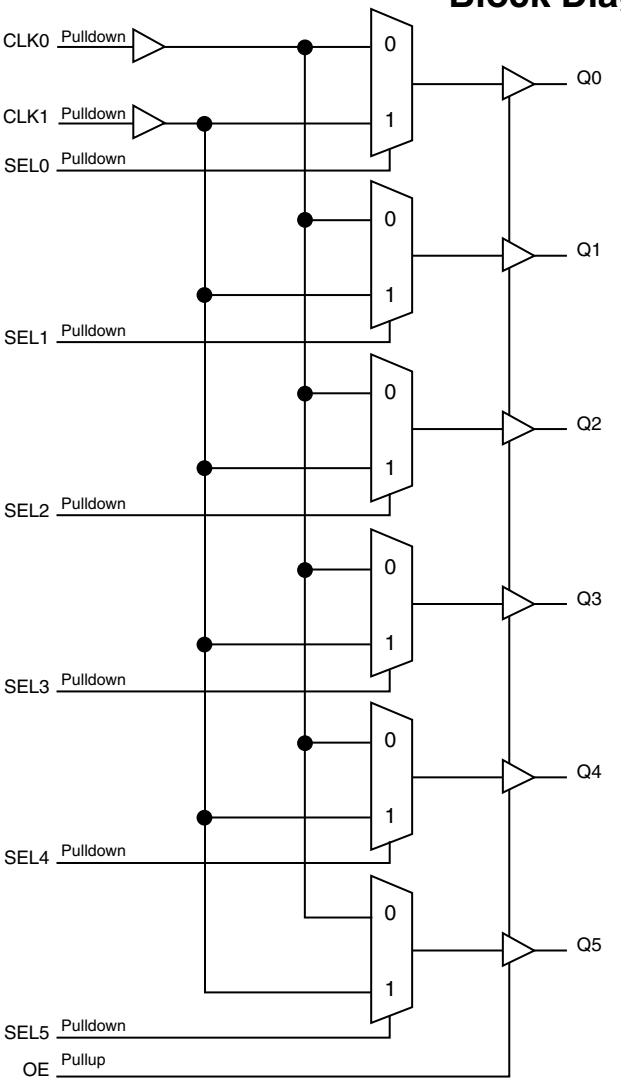
  3.3V/2.5V

  3.3V/1.8V

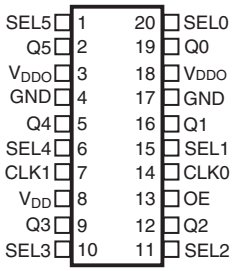
  2.5V/2.5V

  2.5V/1.8V
- -40°C to 85°C ambient operating temperature
- Available in both standard (RoHS 5) and lead-free (RoHS 6) packages

## Block Diagram




## Pin Assignment




**ICS83056I-01**

**20-Lead TSSOP**
**6.50mm x 4.40mm x 0.925mm**
**package body**
**G Package**
**Top View**



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## Table 1. Pin Descriptions

| Number | Name | Type | | Description |
|---|---|---|---|---|
| 1, 6<br>10, 11<br>15, 20 | SEL5, SEL4,<br>SEL3, SEL2,<br>SEL1, SEL0 | Input | Pulldown | Clock select inputs. See Table 3. LVCMOS / LVTTL interface levels. |
| 2, 5, 9<br>12, 16, 19 | Q5, Q4, Q3,<br>Q2, Q1, Q0 | Output | | Single-ended clock output. LVCMOS/LVTTL interface levels. |
| 3, 18 | $V_{DDO}$ | Power | | Output supply pins. |
| 4, 17 | GND | Power | | Power supply ground. |
| 7, 14 | CLK1, CLK0 | Input | Pulldown | Single-ended clock inputs. LVCMOS/LVTTL interface levels. |
| 8 | $V_{DD}$ | Power | | Power supply pin. |
| 13 | OE | Input | Pullup | Output enable. When LOW, outputs are in a High impedance state.<br>When HIGH, outputs are active. LVCMOS / LVTTL interface levels. |

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

## Table 2. Pin Characteristics

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | | | 4 | | pF |
| $C_{PD}$ | Power Dissipation Capacitance (per output) | $V_{DD} = V_{DDO} = 3.465V$ | | 18 | | pF |
| | | $V_{DD} = V_{DDO} = 2.625V$ | | 19 | | pF |
| | | $V_{DD} = V_{DDO} = 2V$ | | 19 | | pF |
| $R_{PULLUP}$ | Input Pullup Resistor | | | 51 | | kΩ |
| $R_{PULLDOWN}$ | Input Pulldown Resistor | | | 51 | | kΩ |
| $R_{OUT}$ | Output Impedance | $V_{DDO} = 3.465V$ | | 15 | | Ω |
| | | $V_{DDO} = 2.625V$ | | 17 | | Ω |
| | | $V_{DDO} = 2V$ | | 25 | | Ω |

## Function Tables

### Table 3. Control Input Function Table

| Control Inputs | Outputs |
|---|---|
| **SELx** | **Qx** |
| 0 | CLK0 |
| 1 | CLK1 |



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## Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

| Item | Rating |
|---|---|
| Supply Voltage, $V_{DD}$ | 4.6V |
| Inputs, $V_I$ | -0.5V to $V_{DD}$ + 0.5V |
| Outputs, $V_O$ | -0.5V to $V_{DDO}$ + 0.5V |
| Package Thermal Impedance, $\theta_{JA}$ | 91.1°C/W (0 mps) |
| Storage Temperature, $T_{STG}$ | -65°C to 150°C |

## DC Electrical Characteristics

**Table 4A. Power Supply DC Characteristics,** $V_{DD}$ = 3.3V±5%, $V_{DDO}$ = 3.3V ± 5% or 2.5V±5%, or 1.8V±0.2V, $T_A$ = -40°C to 85°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Positive Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| $V_{DDO}$ | Output Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| | | | 2.375 | 2.5 | 2.625 | V |
| | | | 1.6 | 1.8 | 2.0 | V |
| $I_{DD}$ | Power Supply Current | | | | 45 | mA |
| $I_{DDO}$ | Output Supply Current | No Load | | | 5 | mA |

**Table 4B. Power Supply DC Characteristics,** $V_{DD}$ = 2.5V±5%, $V_{DDO}$ = 2.5V±5% or 1.8V±0.2V, $T_A$ = -40°C to 85°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Positive Supply Voltage | | 2.375 | 2.5 | 2.625 | V |
| $V_{DDO}$ | Output Supply Voltage | | 2.375 | 2.5 | 2.625 | V |
| | | | 1.6 | 1.8 | 2.0 | V |
| $I_{DD}$ | Power Supply Current | | | | 40 | mA |
| $I_{DDO}$ | Output Supply Current | No Load | | | 5 | mA |



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**Table 4C. LVCMOS/LVTTL DC Characteristics,** $T_A$ = -40°C to 85°C

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Input High Voltage | | $V_{DD}$ = 3.465V | 2 | | $V_{DD}$ + 0.3 | V |
| | | | $V_{DD}$ = 2.625V | 1.7 | | $V_{DD}$ + 0.3 | V |
| $V_{IL}$ | Input Low Voltage | | $V_{DD}$ = 3.465V | -0.3 | | 1.3 | V |
| | | | $V_{DD}$ = 2.625V | -0.3 | | 0.7 | V |
| $I_{IH}$ | Input High Current | CLK0, CLK1, SEL[0:5] | $V_{DD}$ = $V_{IN}$ = 3.465V or 2.625V | | | 150 | µA |
| | | OE | $V_{DD}$ = $V_{IN}$ = 3.465V or 2.625V | | | 5 | µA |
| $I_{IL}$ | Input Low Current | CLK0, CLK1, SEL[0:5] | $V_{DD}$ = 3.465V or 2.625V, $V_{IN}$ = 0V | -5 | | | µA |
| | | OE | $V_{DD}$ = 3.465V or 2.625V, $V_{IN}$ = 0V | -150 | | | µA |
| $V_{OH}$ | Output High Voltage; | | $V_{DDO}$ = 3.3V ± 5%, $I_{OH}$ = -24mA | 2.6 | | | V |
| | | | $V_{DDO}$ = 2.5V ± 5%, $I_{OH}$ = -12mA | 1.8 | | | V |
| | | | $V_{DDO}$ = 1.8V ± 0.2V, $I_{OH}$ = -4mA | $V_{DDO}$ - 0.3 | | | V |
| $V_{OL}$ | Output Low Voltage | | $V_{DDO}$ = 3.3V ± 5%, $I_{OL}$ = 24mA | | | 0.5 | V |
| | | | $V_{DDO}$ = 2.5V ± 5%, $I_{OL}$ = 12mA | | | 0.45 | V |
| | | | $V_{DDO}$ = 1.8V ± 0.2V, $I_{OL}$ = 4mA | | | 0.35 | V |



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# AC Electrical Characteristics

**Table 5A. AC Characteristics,** $V_{DD} = V_{DDO} = 3.3V \pm 5\%$, $T_A$ = -40°C to 85°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $f_{MAX}$ | Output Frequency | | | | 250 | MHz |
| $tp_{LH}$ | Propagation Delay, Low-to-High; NOTE 1 | | 1.8 | 2.5 | 3.2 | ns |
| $tp_{HL}$ | Propagation Delay, High-to-Low; NOTE 1 | | 2.0 | 2.6 | 3.2 | ns |
| *t*jit | Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section; NOTE 2 | 155.52MHz, Integration Range: 12kHz – 20MHz | | 0.18 | | ps |
| *t*sk(i) | Input Skew; NOTE 3 | | | | 145 | ps |
| *t*sk(o) | Output Skew: NOTE 4 | | | | 130 | ps |
| *t*sk(pp) | Part-to-Part Skew; NOTE 3, 5 | | | | 800 | ps |
| $t_R$ / $t_F$ | Output Rise/Fall Time | 20% to 80% | 300 | | 800 | ps |
| odc | Output Duty Cycle | $f_{OUT} \leq 175MHz$ | 40 | | 60 | % |
| $MUX_{ISOLATION}$ | MUX Isolation | 100MHz | | 45 | | dB |

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. Device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE 1: Measured from $V_{DD}/2$ of the input to $V_{DDO}/2$ of the output.
NOTE 2: Driving only one input clock.
NOTE 3: This parameter is defined according with JEDEC Standard 65.
NOTE 4: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DDO}/2$.
NOTE 5: Defined as skew between outputs on different devices operating at the same supply voltage and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.

**Table 5B. AC Characteristics,** $V_{DD} = 3.3V \pm 5\%$, $V_{DDO} = 2.5V \pm 5\%$, $T_A$ = -40°C to 85°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $f_{MAX}$ | Output Frequency | | | | 250 | MHz |
| $tp_{LH}$ | Propagation Delay, Low-to-High; NOTE 1 | | 2.1 | 2.6 | 3.1 | ns |
| $tp_{HL}$ | Propagation Delay, High-to-Low; NOTE 1 | | 2.3 | 2.7 | 3.1 | ns |
| *t*jit | Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section; NOTE 2 | 155.52MHz, Integration Range: 12kHz – 20MHz | | 0.14 | | ps |
| *t*sk(i) | Input Skew; NOTE 3 | | | | 100 | ps |
| *t*sk(o) | Output Skew: NOTE 4 | | | | 130 | ps |
| *t*sk(pp) | Part-to-Part Skew; NOTE 3, 5 | | | | 800 | ps |
| $t_R$ / $t_F$ | Output Rise/Fall Time | 20% to 80% | 300 | | 800 | ps |
| odc | Output Duty Cycle | | 40 | | 60 | % |
| $MUX_{ISOLATION}$ | MUX Isolation | 100MHz | | 45 | | dB |

See notes in Table 5A above.



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**Table 5C. AC Characteristics,** $V_{DD}$ = 3.3V ± 5%, $V_{DDO}$ = 1.8V ± 0.2V, $T_A$ = -40°C to 85°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $f_{MAX}$ | Output Frequency | | | | 250 | MHz |
| $tp_{LH}$ | Propagation Delay, Low-to-High; NOTE 1 | | 2.6 | 3.1 | 3.6 | ns |
| $tp_{HL}$ | Propagation Delay, High-to-Low; NOTE 1 | | 2.7 | 3.2 | 3.7 | ns |
| *t*jit | Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section; NOTE 2 | 155.52MHz, Integration Range: 12kHz – 20MHz | | 0.16 | | ps |
| *t*sk(i) | Input Skew; NOTE 3 | | | | 110 | ps |
| *t*sk(o) | Output Skew: NOTE 4 | | | | 130 | ps |
| *t*sk(pp) | Part-to-Part Skew; NOTE 3, 5 | | | | 800 | ps |
| $t_R$ / $t_F$ | Output Rise/Fall Time | 20% to 80% | 450 | | 850 | ps |
| odc | Output Duty Cycle | | 40 | | 60 | % |
| $MUX_{ISOLATION}$ | MUX Isolation | 100MHz | | 45 | | dB |

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. Device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE 1: Measured from $V_{DD}$/2 of the input to $V_{DDO}$/2 of the output.
NOTE 2: Driving only one input clock.
NOTE 3: This parameter is defined according with JEDEC Standard 65.
NOTE 4: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DDO}$/2.
NOTE 5: Defined as skew between outputs on different devices operating at the same supply voltage and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.

**Table 5D. AC Characteristics,** $V_{DD}$ = $V_{DDO}$ = 2.5V ± 5%, $T_A$ = -40°C to 85°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $f_{MAX}$ | Output Frequency | | | | 250 | MHz |
| $tp_{LH}$ | Propagation Delay, Low-to-High; NOTE 1 | | 1.5 | 3.0 | 4.5 | ns |
| $tp_{HL}$ | Propagation Delay, High-to-Low; NOTE 1 | | 2.2 | 2.8 | 3.4 | ns |
| *t*jit | Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section; NOTE 2 | 155.52MHz, Integration Range: 12kHz – 20MHz | | 0.22 | | ps |
| *t*sk(i) | Input Skew; NOTE 3 | | | | 140 | ps |
| *t*sk(o) | Output Skew: NOTE 4 | | | | 125 | ps |
| *t*sk(pp) | Part-to-Part Skew; NOTE 3, 5 | | | | 800 | ps |
| $t_R$ / $t_F$ | Output Rise/Fall Time | 20% to 80% | 300 | | 700 | ps |
| odc | Output Duty Cycle | $f_{OUT} \leq$ 175MHz | 40 | | 60 | % |
| $MUX_{ISOLATION}$ | MUX Isolation | 100MHz | | 45 | | dB |

See notes in Table 5C above.



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**Table 5E. AC Characteristics,** $V_{DD}$ = 2.5V ± 5%, $V_{DDO}$ = 1.8V ± 0.2V, $T_A$ = -40°C to 85°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $f_{MAX}$ | Output Frequency | | | | 250 | MHz |
| $tp_{LH}$ | Propagation Delay, Low-to-High; NOTE 1 | | 2.2 | 3.2 | 4.2 | ns |
| $tp_{HL}$ | Propagation Delay, High-to-Low; NOTE 1 | | 2.2 | 3.2 | 4.0 | ns |
| *t*jit | Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section; NOTE 2 | 155.52MHz, Integration Range: 12kHz – 20MHz | | 0.19 | | ps |
| *t*sk(i) | Input Skew; NOTE 3 | | | | 110 | ps |
| *t*sk(o) | Output Skew: NOTE 4 | | | | 125 | ps |
| *t*sk(pp) | Part-to-Part Skew; NOTE 3, 5 | | | | 800 | ps |
| $t_R$ / $t_F$ | Output Rise/Fall Time | 20% to 80% | 450 | | 850 | ps |
| odc | Output Duty Cycle | $f_{OUT} \leq$ 200MHz | 40 | | 60 | % |
| $MUX_{ISOLATION}$ | MUX Isolation | 100MHz | | 45 | | dB |

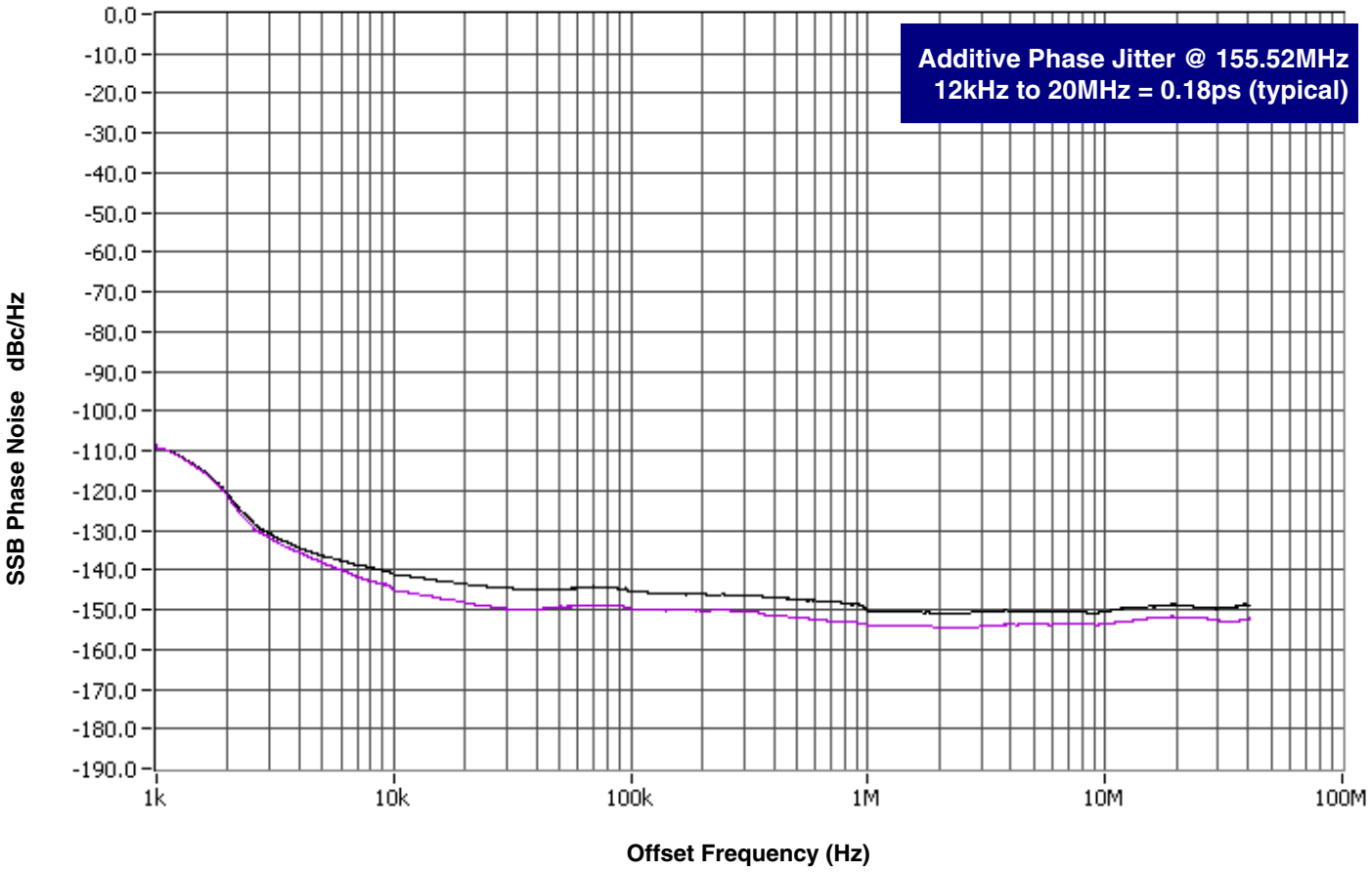
NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. Device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE 1: Measured from $V_{DD}$/2 of the input to $V_{DDO}$/2 of the output.
NOTE 2: Driving only one input clock.
NOTE 3: This parameter is defined according with JEDEC Standard 65.
NOTE 4: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DDO}$/2.
NOTE 5: Defined as skew between outputs on different devices operating at the same supply voltage and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.



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## Additive Phase Jitter

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the ***dBc Phase Noise.*** This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a ***dBc*** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.

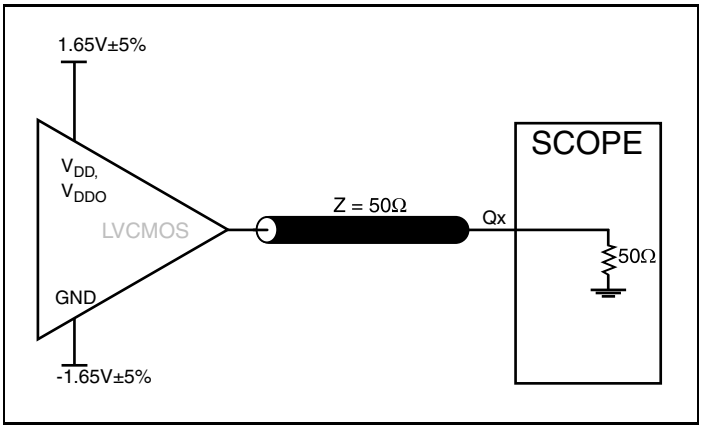



As with most timing specifications, phase noise measurements has issues relating to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This is illustrated above. The device meets the noise floor of what is shown, but can actually be lower. The phase noise is dependent on the input source and measurement equipment.

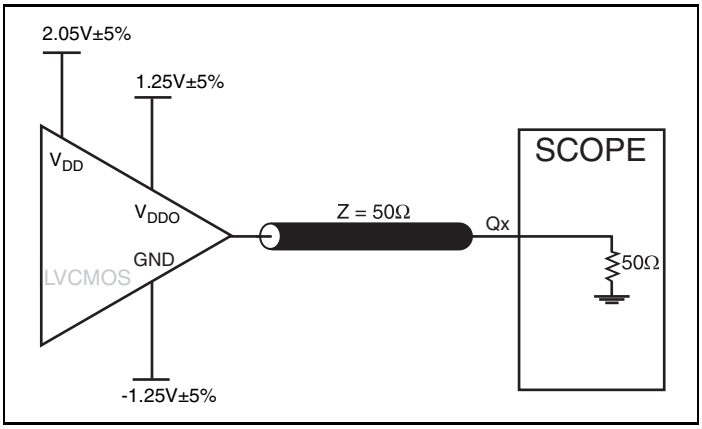


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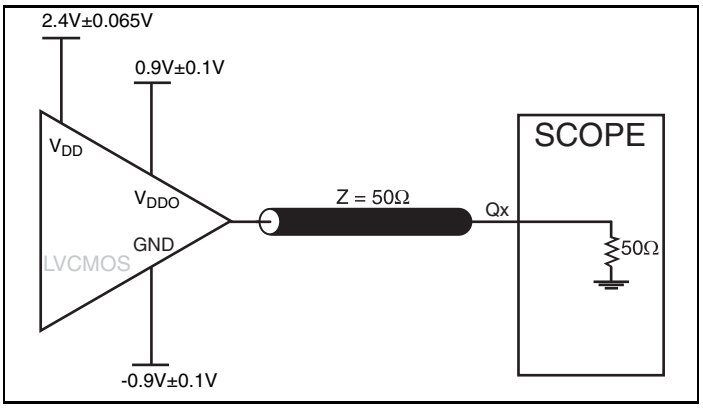
## Parameter Measurement Information



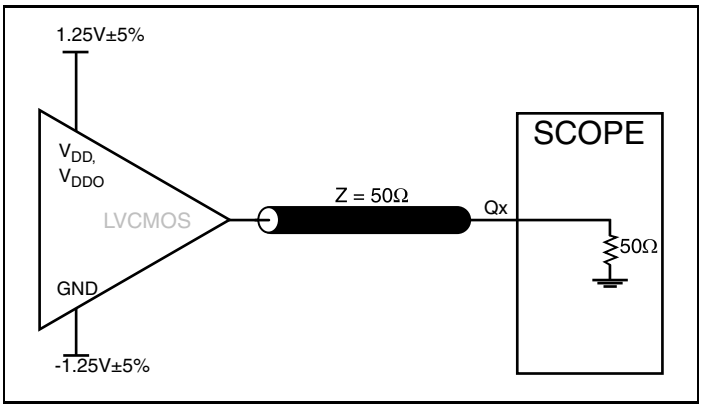

**3.3V Output Load AC Test Circuit**



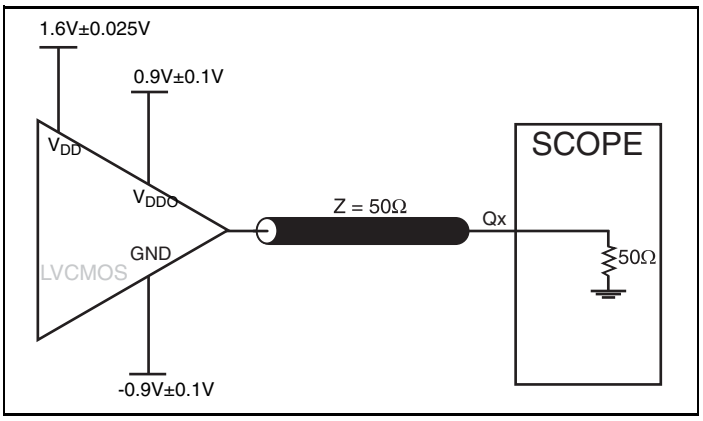

**3.3V Core/2.5V Output Load AC Test Circuit**



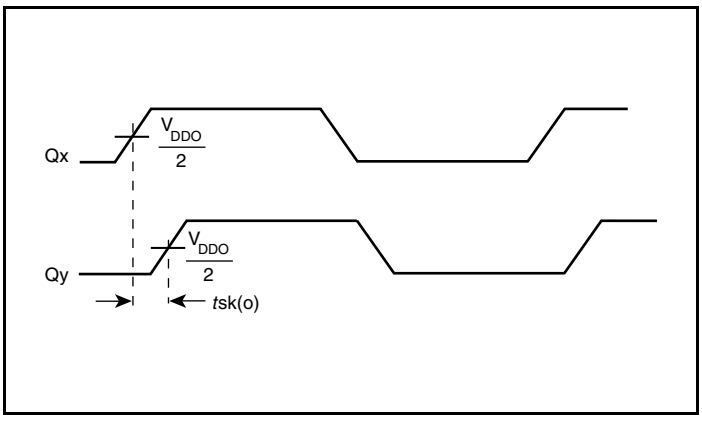

**3.3V Core/1.8V Output Load AC Test Circuit**




**2.5V Core/2.5V Output Load AC Test Circuit**




**2.5V Core/1.8V Output Load AC Test Circuit**

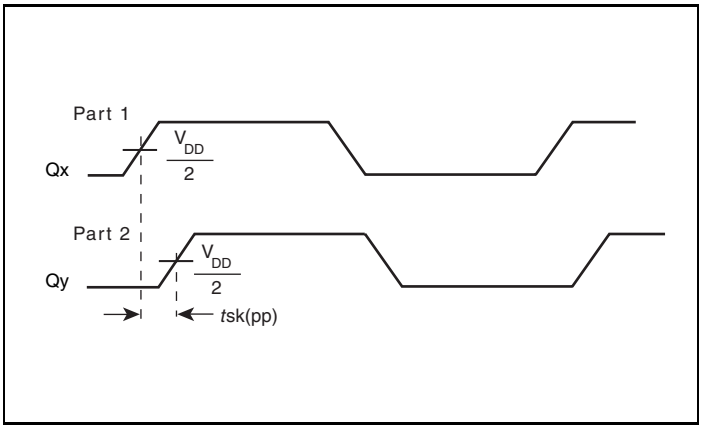



**Output Skew**

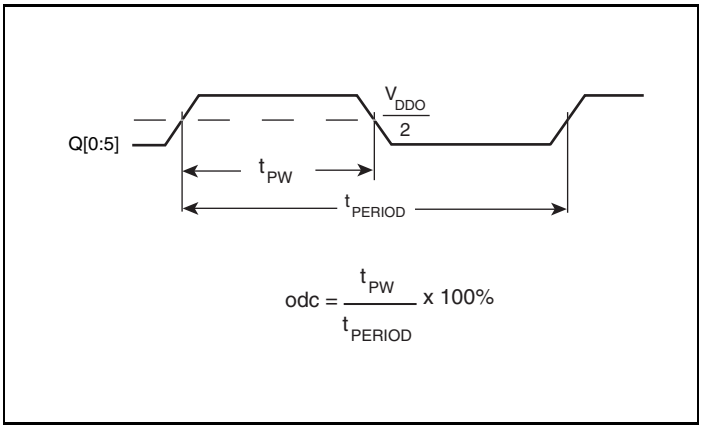


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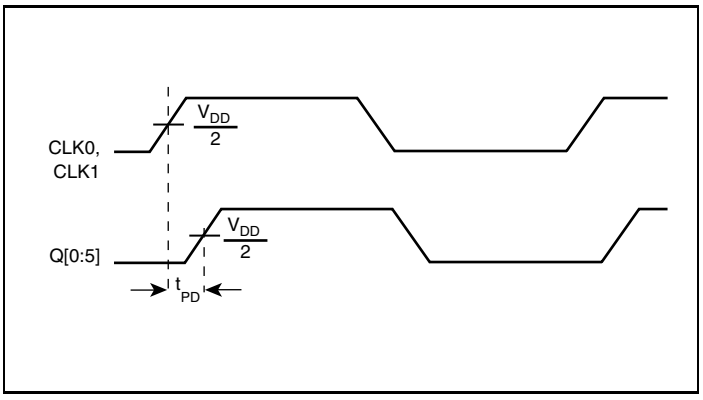
## Parameter Measurement Information, continued



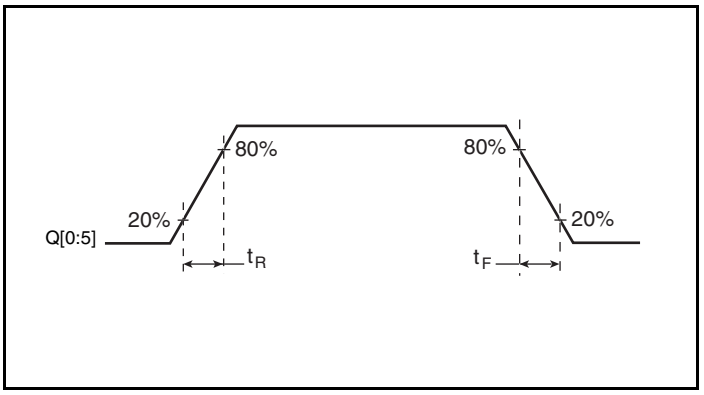

**Part-to-Part Skew**



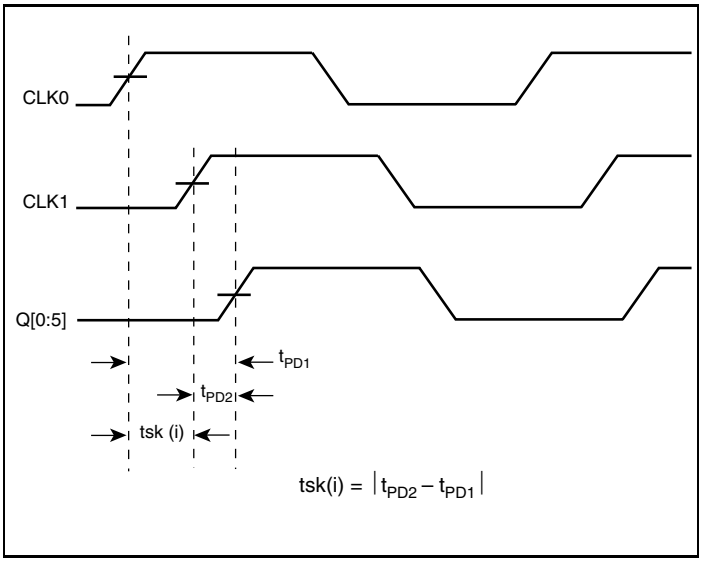

**Output Duty Cycle/Pulse Width/Period**




**Propagation Delay**




**Output Rise/Fall Time**

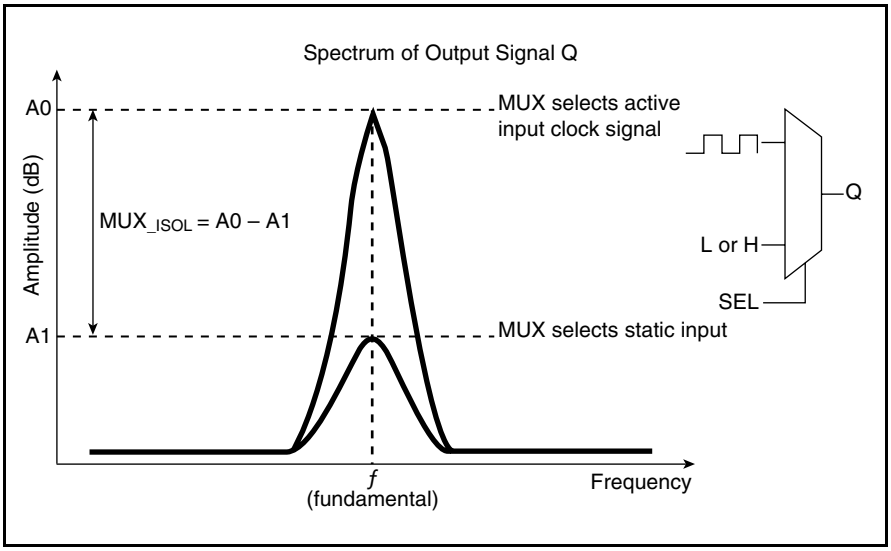



**Input Skew**



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## Parameter Measurement Information, continued




**MUX Isolation**

## Application Information

### Recommendations for Unused Input and Output Pins

### Inputs:

#### CLK Inputs

For applications not requiring the use of a clock input, it can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from the CLK input to ground.

#### LVCMOS Control Pins

All control pins have internal pullups or pulldowns; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

### Outputs:

#### LVCMOS Outputs

All unused LVCMOS output can be left floating. There should be no trace attached.



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# Reliability Information

**Table 6. $\theta_{JA}$ vs. Air Flow Table for a 20 Lead TSSOP**

| $\theta_{JA}$ vs. Air Flow | | | |
|---|---|---|---|
| Meters per Second | **0** | **1** | **2.5** |
| Multi-Layer PCB, JEDEC Standard Test Boards | 91.1°C/W | 86.7°C/W | 84.6°C/W |

## Transistor Count

The transistor count for ICS83056I-01 is: 967

# Package Outline and Package Dimensions

**Package Outline - G Suffix for 20 Lead TSSOP**

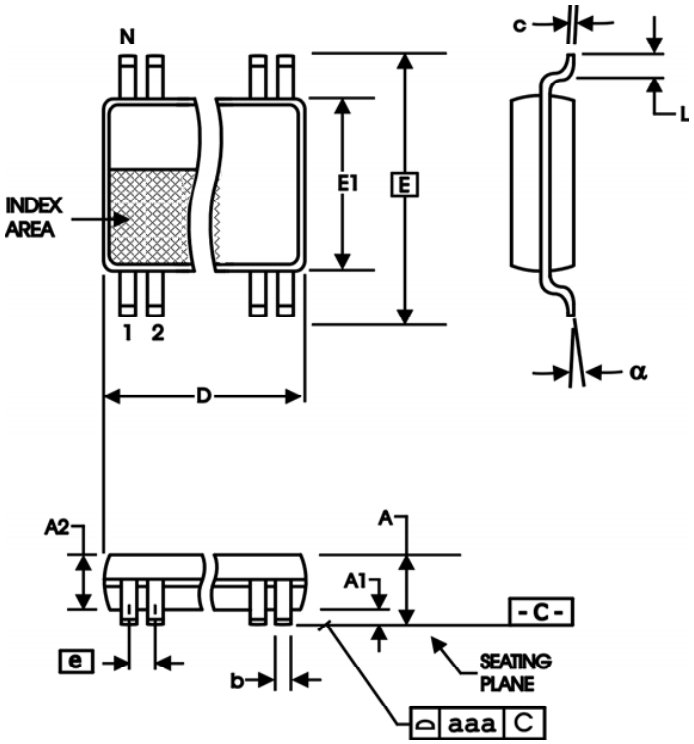



**Table 7. Package Dimensions**

| All Dimensions in Millimeters | | |
|---|---|---|
| **Symbol** | **Minimum** | **Maximum** |
| **N** | 20 | |
| **A** | | 1.20 |
| **A1** | 0.05 | 0.15 |
| **A2** | 0.80 | 1.05 |
| **b** | 0.19 | 0.30 |
| **c** | 0.09 | 0.20 |
| **D** | 6.40 | 6.60 |
| **E** | 6.40 Basic | |
| **E1** | 4.30 | 4.50 |
| **e** | 0.65 Basic | |
| **L** | 0.45 | 0.75 |
| α | 0° | 8° |
| **aaa** | | 0.10 |

Reference Document: JEDEC Publication 95, MO-153



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# Ordering Information

**Table 9. Ordering Information**

| Part/Order Number | Marking | Package | Shipping Packaging | Temperature |
|---|---|---|---|---|
| 83056AGI-01 | ICS83056AI01 | 20 Lead TSSOP | Tube | -40°C to 85°C |
| 83056AGI-01T | ICS83056AI01 | 20 Lead TSSOP | 2500 Tape & Reel | -40°C to 85°C |
| 83056AGI-01LF | ICS3056AI01L | “Lead-Free” 20 Lead TSSOP | Tube | -40°C to 85°C |
| 83056AGI-01LFT | ICS3056AI01L | “Lead-Free” 20 Lead TSSOP | 2500 Tape & Reel | -40°C to 85°C |

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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