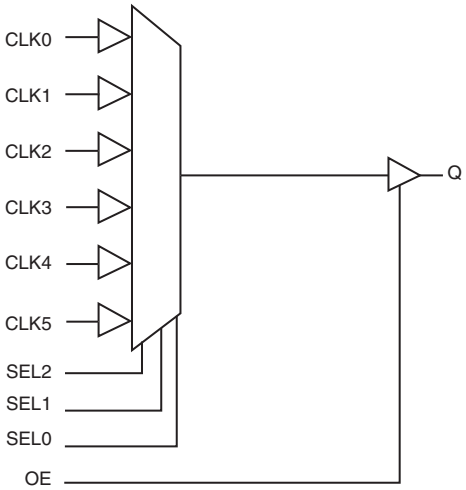
General Description

The 83056 is a low skew, 6:1, Single-ended Multiplexer from IDT. The 83056 has six selectable single-ended clock inputs and one single-ended clock output. The output has a V_{DDO} pin which may be set at 3.3V, 2.5V, or 1.8V, making the device ideal for use in voltage translation applications. An output enable pin places the output in a high impedance state which may be useful for testing or debug purposes. The device operates up to 250MHz and is packaged in a 16 TSSOP package.

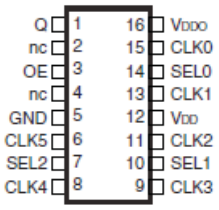
Features

- 6:1 single-ended multiplexer
- Q nominal output impedance: 7Ω (V_{DDO} = 3.3V)
- Maximum output frequency: 250MHz
- Propagation delay: 3ns (maximum), V_{DD} = V_{DDO} = 3.3V
- Input skew: 225ps (maximum), V_{DD} = V_{DDO} = 3.3V
- Part-to-part skew: 475ps (maximum), V_{DD} = V_{DDO} = 3.3V
- Additive phase jitter, RMS: 0.19ps (typical), 3.3V/3.3V
- Operating supply modes:
  V_{DD}/V_{DDO}
  3.3V/3.3V
  3.3V/2.5V
  3.3V/1.8V
  2.5V/2.5V
  2.5V/1.8V
- -40°C to 85°C ambient operating temperature
- Available in lead-free (RoHS 6) package

Block Diagram



Pin Assignment



83056
16-Lead TSSOP
4.4mm x 5.0mm x 0.92mm package body
G Package
Top View

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Table 1. Pin Descriptions

Number	Name	Type		Description
1	Q	Output		Single-ended clock output. LVCMOS/LVTTL interface levels.
2, 4	nc	Unused		No connect.
6, 8, 9, 11, 13, 15	CLK5, CLK4, CLK3, CLK2, CLK1, CLK0	Input	Pulldown	Single-ended clock inputs. LVCMOS/LVTTL interface levels.
3	OE	Input	Pullup	Output enable. When LOW, outputs are in HIGH impedance state. When HIGH, outputs are active. LVCMOS / LVTTL interface levels.
5	GND	Power		Power supply ground.
7, 10, 14	SEL2, SEL1, SEL0	Input	Pulldown	Clock select input. See Control Input Function Table. LVCMOS / LVTTL interface levels.
12	V_{DD}	Power		Core and input supply pin.
16	V_{DDO}	Power		Output supply pin.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ
C_{PD}	Power Dissipation Capacitance (per output)	V = 3.465V		18		pF
		V = 2.625V		20		pF
		V = 1.89V		30		pF
R_{OUT}	Output Impedance	V = 3.465V		7		Ω
		V = 2.625V		7		Ω
		V = 1.89V		10		Ω

Table 3. Control Input Function Table

Control Inputs			Input Selected to Q
SEL2	SEL1	SEL0	
0	0	0	CLK0
0	0	1	CLK1
0	1	0	CLK2
0	1	1	CLK3
1	0	0	CLK4
1	0	1	CLK5
1	1	0	LOW
1	1	1	LOW

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Absolute Maximum Ratings

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5 V
Outputs, V_O	-0.5V to V_{DDO} + 0.5V
Package Thermal Impedance, θ_{JA}	89°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Table 4A. Power Supply DC Characteristics, $V_{DD} = V_{DDO} = 3.3V \pm 5\%$, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Power Supply Voltage		3.135	3.3	3.465	V
V_{DDO}	Output Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current				40	mA
I_{DDO}	Output Supply Current				5	mA

Table 4B. Power Supply DC Characteristics, $V_{DD} = 3.3V \pm 5\%$, $V_{DDO} = 2.5V \pm 5\%$, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Power Supply Voltage		3.135	3.3	3.465	V
V_{DDO}	Output Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Power Supply Current				40	mA
I_{DDO}	Output Supply Current				5	mA

Table 4C. Power Supply DC Characteristics, $V_{DD} = 3.3V \pm 5\%$, $V_{DDO} = 1.8V \pm 0.2V$, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Power Supply Voltage		3.135	3.3	3.465	V
V_{DDO}	Output Supply Voltage		1.71	1.8	1.89	V
I_{DD}	Power Supply Current				40	mA
I_{DDO}	Output Supply Current				5	mA

Table 4D. Power Supply DC Characteristics, $V_{DD} = V_{DDO} = 2.5V \pm 5\%$, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Power Supply Voltage		2.375	2.5	2.625	V
V_{DDO}	Output Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Power Supply Current				35	mA
I_{DDO}	Output Supply Current				5	mA

Table 4E. Power Supply DC Characteristics, $V_{DD} = 2.5V \pm 5\%$, $V_{DDO} = 1.8V \pm 0.2V$, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Power Supply Voltage		2.375	2.5	2.625	V
V_{DDO}	Output Supply Voltage		1.71	1.8	1.89	V
I_{DD}	Power Supply Current				35	mA
I_{DDO}	Output Supply Current				5	mA

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TABLE 4F. LVCMOS/LVTTL DC CHARACTERISTICS, T_A = -40°C TO 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		V_{DD} = 3.3V ± 5%	2		V_{DD} + 0.3	V
			V_{DD} = 2.5V ± 5%	1.7		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage		V_{DD} = 3.3V ± 5%	-0.3		0.8	V
			V_{DD} = 2.5V ± 5%	-0.3		0.7	V
I_{IH}	Input High Current	CLK0:CLK5, SEL0:SEL2	V_{DD} = 3.3V or 2.5V ± 5%			150	µA
		OE	V_{DD} = 3.3V or 2.5V ± 5%			5	µA
I_{IL}	Input Low Current	CLK0:CLK5, SEL0:SEL2	V_{DD} = 3.3V or 2.5V ± 5%	-5			µA
		OE	V_{DD} = 3.3V or 2.5V ± 5%	-150			µA
V_{OH}	Output HighVoltage		V_{DDO} = 3.3V ± 5%; NOTE 1	2.6			V
			V_{DDO} = 2.5V ± 5%; NOTE 1	1.8			V
			V_{DDO} = 1.8V ± 5%; NOTE 1	V_{DD} - 0.3			V
V_{OL}	Output Low Voltage		V_{DDO} = 3.3V ± 5%; NOTE 1			0.5	V
			V_{DDO} = 2.5V ± 5%; NOTE 1			0.45	V
			V_{DDO} = 1.8V ± 5%; NOTE 1			0.35	V

NOTE 1: Outputs terminated with 50W to V_{DDO}/2. See Parameter Measurement section, “Load Test Circuit” diagrams.

TABLE 5A. AC CHARACTERISTICS, V_{DD} = V_{DDO} = 3.3V ± 5%, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				250	MHz
tp_{LH}	Propagation Delay, Low to High; NOTE 1		2.4	2.7	3.0	ns
tp_{HL}	Propagation Delay, High to Low; NOTE 1		2.5	2.7	2.9	ns
*t*sk(i)	Input Skew; NOTE 2			55	225	ps
*t*jit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section; NOTE 3	155.52MHz, (12kHz to 20MHz)		0.19		ps
*t*sk(pp)	Part-to-Part Skew; NOTE 2, 4				475	ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	50		500	ps
odc	Output Duty Cycle		45		55	%
MUX_{ISOL}	MUX Isolation	@ 100MHz		45		dB

NOTE 1: Measured from V_{DD}/2 of the input to V_{DDO}/2 of the output.
NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 3: Driving only one input clock.
NOTE 4: Defined as skew between outputs on different devices operating a the same supply voltages and with equal load conditions. Using the same type of input on each device, the output is measured at V_{DDO}/2.

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TABLE 5B. AC CHARACTERISTICS, V_{DD} = 3.3V ± 5%, V_{DDO} = 2.5V ± 5%, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				250	MHz
tp_{LH}	Propagation Delay, Low to High; NOTE 1		2.5	2.8	3.1	ns
tp_{HL}	Propagation Delay, High to Low; NOTE 1		2.6	2.8	3.0	ns
*t*sk(i)	Input Skew; NOTE 2			45	150	ps
*t*jit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section; NOTE 3	155.52MHz, (12kHz to 20MHz)		0.14		ps
*t*sk(pp)	Part-to-Part Skew; NOTE 2, 4				400	ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	50		500	ps
odc	Output Duty Cycle		45		55	%
MUX_{ISOL}	MUX Isolation	@ 100MHz		45		dB

NOTE 1: Measured from V_{DD}/2 of the input to V_{DDO}/2 of the output.
NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 3: Driving only one input clock.
NOTE 4: Defined as skew between outputs on different devices operating a the same supply voltages and with equal load conditions. Using the same type of input on each device, the output is measured at V_{DDO}/2.

TABLE 5C. AC CHARACTERISTICS, V_{DD} = 3.3V ± 5%, V_{DDO} = 1.8V ± 5%, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				250	MHz
tp_{LH}	Propagation Delay, Low to High; NOTE 1		2.7	3.2	3.8	ns
tp_{HL}	Propagation Delay, High to Low; NOTE 1		2.8	3.3	3.8	ns
*t*sk(i)	Input Skew; NOTE 2			50	150	ps
*t*jit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section; NOTE 3	155.52MHz, (12kHz to 20MHz)		0.16		ps
*t*sk(pp)	Part-to-Part Skew; NOTE 2, 4				475	ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	100		700	ps
odc	Output Duty Cycle		45		55	%
MUX_{ISOL}	MUX Isolation	@ 100MHz		45		dB

NOTE 1: Measured from V_{DD}/2 of the input to V_{DDO}/2 of the output.
NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 3: Driving only one input clock.
NOTE 4: Defined as skew between outputs on different devices operating a the same supply voltages and with equal load conditions. Using the same type of input on each device, the output is measured at V_{DDO}/2.

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TABLE 5D. AC CHARACTERISTICS, $V_{DD} = V_{DDO} = 2.5V \pm 5\%$, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				250	MHz
tp_{LH}	Propagation Delay, Low to High; NOTE 1		2.5	3.0	3.5	ns
tp_{HL}	Propagation Delay, High to Low; NOTE 1		2.5	2.9	3.4	ns
*t*sk(i)	Input Skew; NOTE 2			60	175	ps
tjit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section; NOTE 3	155.52MHz, (12kHz to 20MHz)		0.21		ps
*t*sk(pp)	Part-to-Part Skew; NOTE 2, 4				300	ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	100		500	ps
odc	Output Duty Cycle		40		60	%
MUX_{ISOL}	MUX Isolation	@ 100MHz		45		dB

NOTE 1: Measured from $V_{DD}/2$ of the input to $V_{DDO}/2$ of the output.
NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 3: Driving only one input clock.
NOTE 4: Defined as skew between outputs on different devices operating a the same supply voltages and with equal load conditions. Using the same type of input on each device, the output is measured at $V_{DDO}/2$.

TABLE 5E. AC CHARACTERISTICS, $V_{DD} = 2.5V \pm 5\%$, $V_{DDO} = 1.8V \pm -5\%$, T_A = -40°C TO 85°C

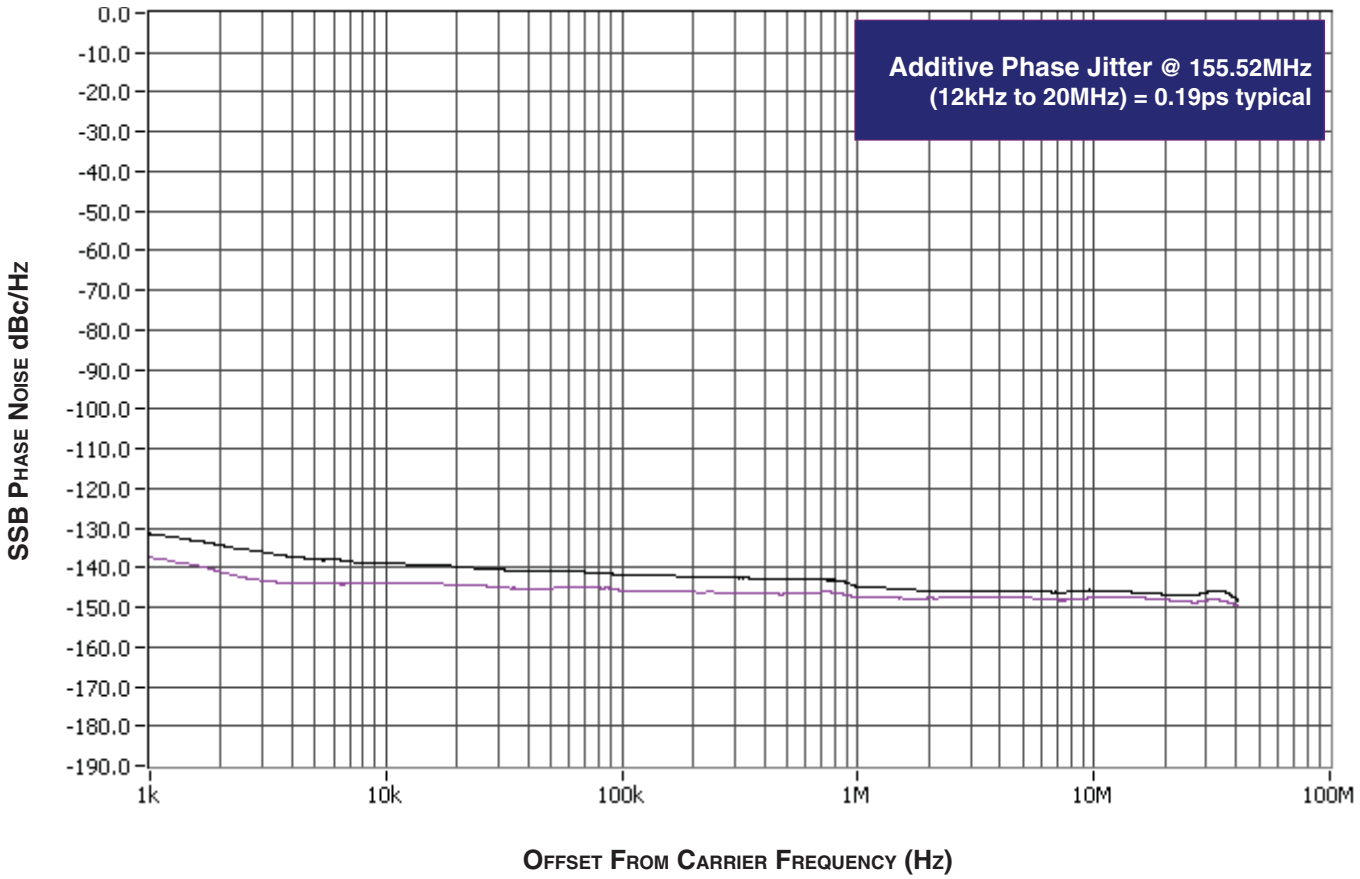
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				250	MHz
tp_{LH}	Propagation Delay, Low to High; NOTE 1		2.6	3.3	4.0	ns
tp_{HL}	Propagation Delay, High to Low; NOTE 1		2.7	3.3	4.0	ns
*t*sk(i)	Input Skew; NOTE 2			50	150	ps
tjit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section; NOTE 3	155.52MHz, (12kHz to 20MHz)		0.17		ps
*t*sk(pp)	Part-to-Part Skew; NOTE 2, 4				325	ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	100		700	ps
odc	Output Duty Cycle		40		60	%
MUX_{ISOL}	MUX Isolation	@ 100MHz		45		dB

NOTE 1: Measured from $V_{DD}/2$ of the input to $V_{DDO}/2$ of the output.
NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 3: Driving only one input clock.
NOTE 4: Defined as skew between outputs on different devices operating a the same supply voltages and with equal load conditions. Using the same type of input on each device, the output is measured at $V_{DDO}/2$.

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Additive Phase Jitter

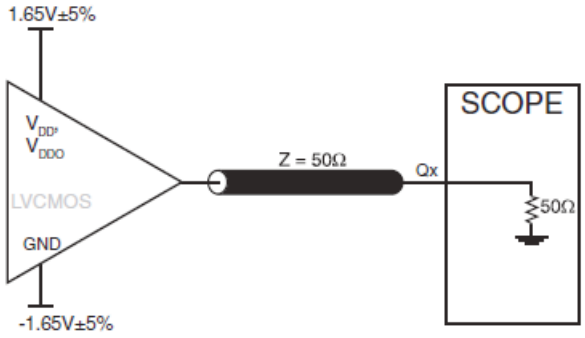
The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the ***dBc Phase Noise.*** This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a ***dBc*** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.



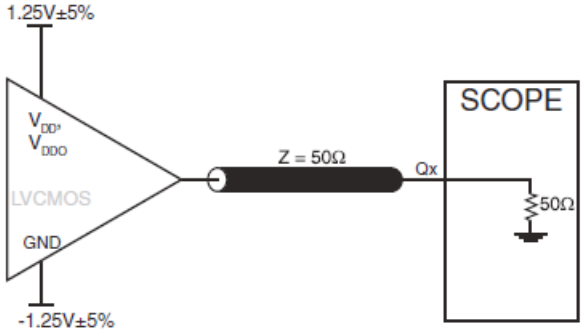
As with most timing specifications, phase noise measurements have issues. The primary issue relates to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This is illustrated above. The device meets the noise floor of what is shown, but can actually be lower. The phase noise is dependant on the input source and measurement equipment.

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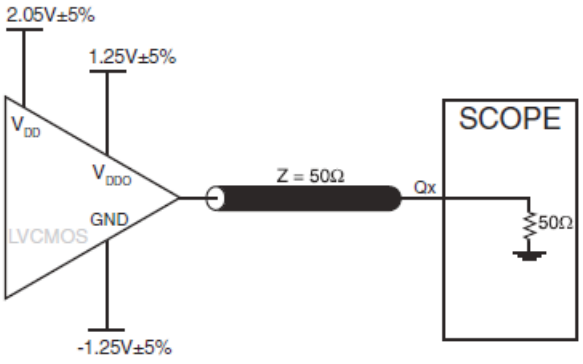
Parameter Measurement Information



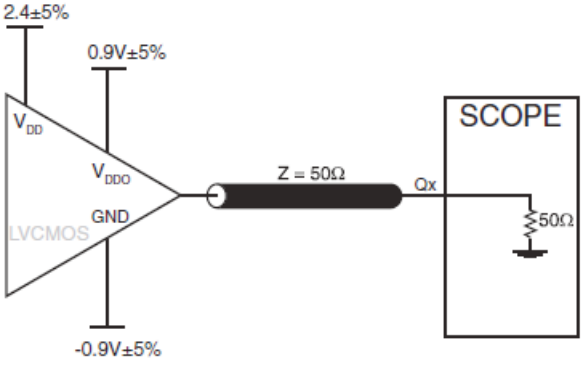
3.3V Core/3.3V Output Load AC Test Circuit



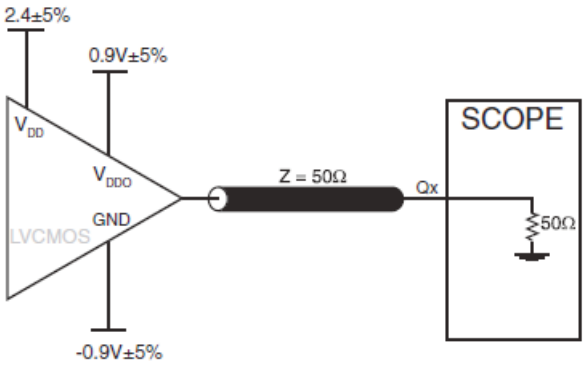
2.5V Core/2.5V Output Load AC Test Circuit



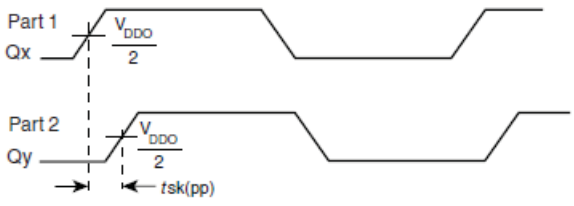
3.3V Core/2.5V Output Load AC Test Circuit



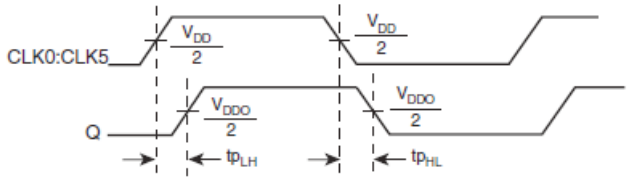
3.3V Core/1.8V Output Load AC Test Circuit



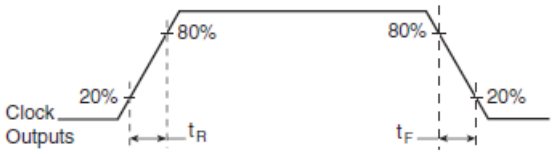
2.5 Core/1.8V Output Load AC Test Circuit



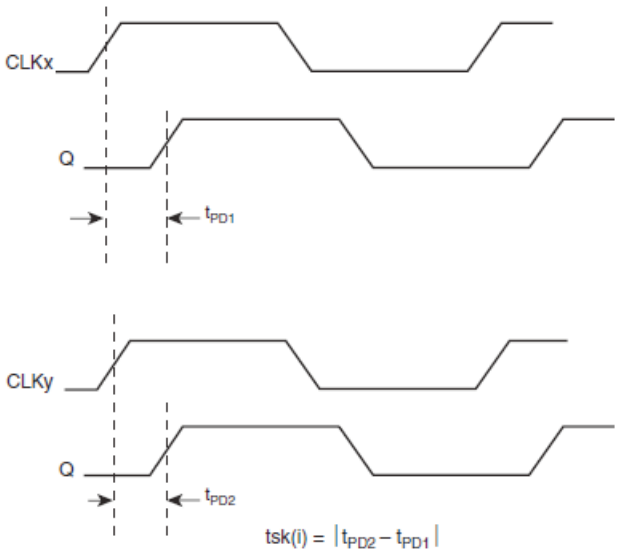
Part-to-Part Skew



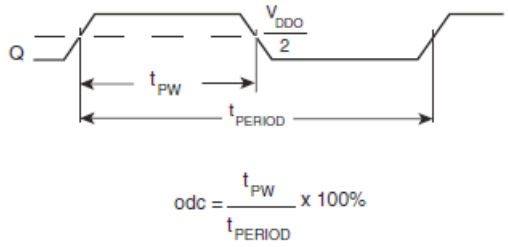
PROPAGATION DELAY



OUTPUT RISE/FALL TIME



INPUT SKEW



OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD

Application Information

Recommendations for Unused Input Pins

Inputs:

CLK Input:
For applications not requiring the use of a clock input, it can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from the CLK input to ground.

LVCMOS Control Pins:
All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

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Reliability Information

Table 6. θ_{JA} vs. Air Flow Table for 16 Lead TSSOP

θ_{JA} by Velocity (Linear Feet per Minute)	0	200	500
Single-Layer PCB, JEDEC Standard Test Boards	137.1°C/W	118.2°C/W	106.8°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	89.0°C/W	81.8°C/W	78.1°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

Transistor Count

The transistor count for 83056 is: 874

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Package Outline - G Suffix for 16 Lead TSSOP

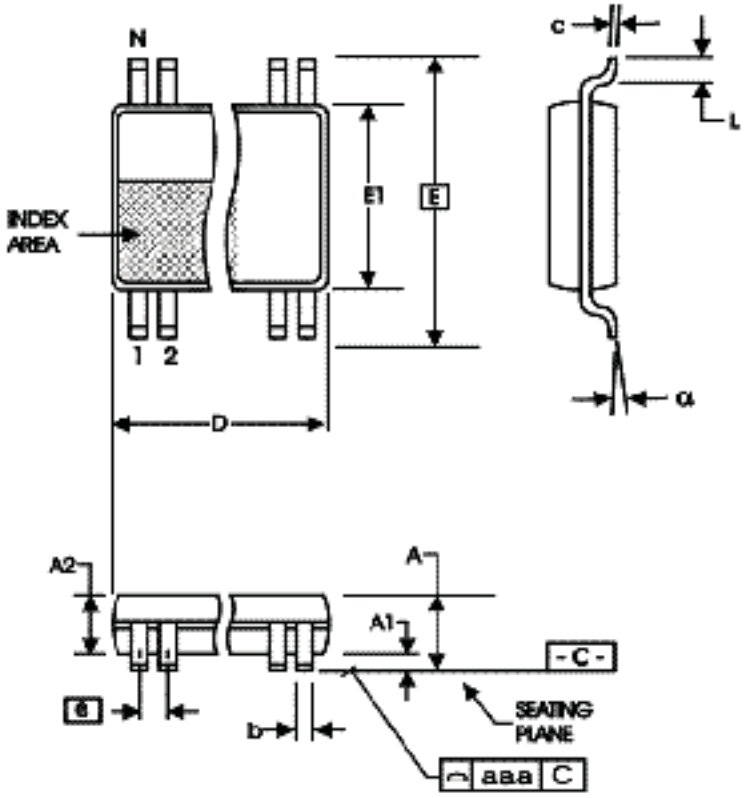


Table 7. Package Dimensions

SYMBOL	Millimeters	
	Minimum	Maximum
N	16	
A	--	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	4.90	5.10
E	6.40 BASIC	
E1	4.30	4.50
e	0.65 BASIC	
L	0.45	0.75
α	0°	8°
aaa	--	0.10

Reference Document: JEDEC Publication 95, MO-153

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TABLE 8. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
83056AGILF	83056AIL	16 Lead “Lead-Free” TSSOP	tube	-40°C to 85°C
83056AGILFT	83056AIL	16 Lead “Lead-Free” TSSOP	tape & reel	-40°C to 85°C

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REVISION HISTORY SHEET				
Rev	**Table**	**Page**	**Description of Change**	**Date**
A	T8	12	Ordering Information Table - added Lead-Free marking.	1/18/06
B	T5A - T5E	1 4 - 6 7	Features Section - added Additive Phase Jitter bullet. AC Characteristics Tables - added tjit row and spec. Added Additive Phase Jitter section.	01/04/07
B	T8	13	Ordering Information - removed leaded devices. Updated data sheet format.	3/20/15
B	T8	13	Ordering Information - Removed ICS from the Part/Order Number. Deleted LF note below table. Updated header and footer.	3/10/16

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