PRODUCT DISCONTINUATION NOTICE - LAST TIME BUY EXPIRES MAY 6, 2017

General Description

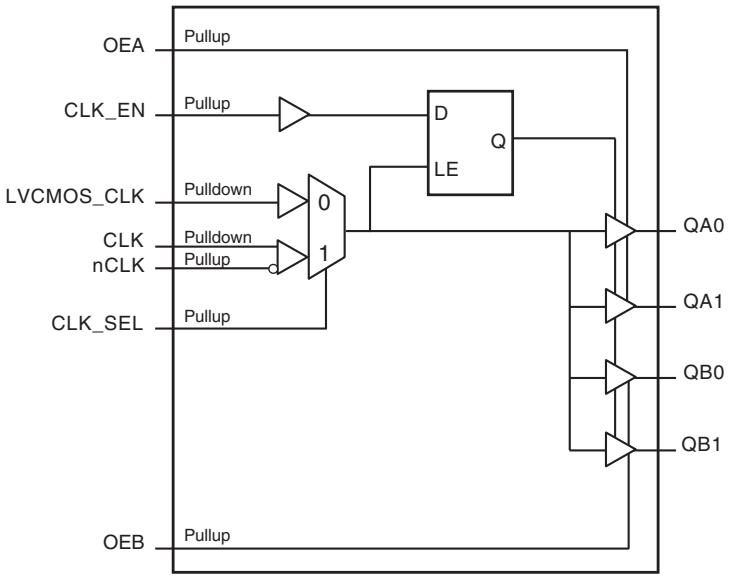
The 8305-02 is a low skew, 1-to-4, Differential/ LVCMOS-to-LVCMOS/LVTTL Fanout Buffer. The 8305-02 has selectable clock inputs that accept either differential or single-ended input levels. The clock enable is internally synchronized to eliminate runt pulses on the outputs during asynchronous assertion/ deassertion of the clock enable pin. Outputs are forced LOW when the clock is disabled. A separate output enable pin controls whether the outputs are in the active or high impedance state.

Guaranteed output and part-to-part skew characteristics make the 8305-02 ideal for those applications demanding well defined performance and repeatability.

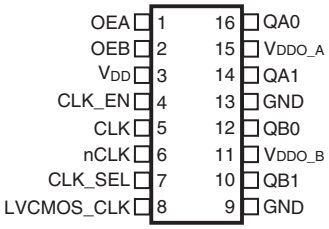
Features

- Four LVCMOS/LVTTL outputs, (two banks of two LVCMOS outputs)
- Selectable differential CLK, nCLK pair or LVCMOS_CLK input
- CLK, nCLK pair can accept the following differential input levels: LVPECL, LVDS, LVHSTL, HCSL
- LVCMOS_CLK supports the following input types: LVCMOS, LVTTL
- Maximum output frequency: 250MHz
- Output skew: 100ps (maximum)
- Power supply modes:
  Core/Output
  3.3V/3.3V
  3.3V/2.5V
  3.3V/1.8V
  3.3V/1.5V
- 0°C to 70°C ambient operating temperature
- Lead-free (RoHS 6) packaging
- For functional replacement part use 8305

Block Diagram



Pin Assignment



8305-02

16-Lead TSSOP
4.4mm x 5.0mm x 0.92mm package body
G Package
Top View

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Table 1. Pin Descriptions

Number	Name	Type		Description
1	OEA	Input	Pullup	Output enable for Bank A outputs. When LOW, QAx outputs are in HIGH impedance state. When HIGH, QAx outputs are active. LVCMOS / LVTTL interface levels.
2	OEB	Input	Pullup	Output enable for Bank B outputs. When LOW, QBx outputs are in HIGH impedance state. When HIGH, QBx outputs are active. LVCMOS / LVTTL interface levels.
3	V_{DD}	Power		Positive supply pins.
4	CLK_EN	Input	Pullup	Synchronizing clock enable. When LOW, the output clocks are disabled. When HIGH, output clocks are enabled. LVCMOS / LVTTL interface levels.
5	CLK	Input	Pulldown	Non-inverting differential clock input.
6	nCLK	Input	Pullup	Inverting differential clock input.
7	CLK_SEL	Input	Pullup	Clock select input. When HIGH, selects CLK, nCLK inputs. When LOW, selects LVCMOS_CLK input. LVCMOS / LVTTL interface levels.
8	LVCMOS_CLK	Input	Pulldown	Single-ended clock input. LVCMOS/LVTTL interface levels.
9, 13	GND	Power		Power supply ground.
10, 12	QB1, QB0	Output		Single-ended Bank B clock outputs. LVCMOS/LVTTL interface levels.
11	V_{DDO_B}	Power		Output supply pin for Bank B outputs.
14, 16	QA1, QA0	Output		Single-ended Bank A clock outputs. LVCMOS/LVTTL interface levels.
15	V_{DDO_A}	Power		Output supply pin for Bank A outputs.

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ
C_{PD}	Power Dissipation Capacitance (per output)			13		pF
R_{OUT}	Output Impedance	$V_{DDO_A} = V_{DDO_B} = 3.3V$		9		Ω
		$V_{DDO_A} = V_{DDO_B} = 2.5V$		11		Ω
		$V_{DDO_A} = V_{DDO_B} = 1.8V$		15		Ω
		$V_{DDO_A} = V_{DDO_B} = 1.5V$		20		Ω

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Function Tables

Table 3. Clock Input Function Table

Inputs				Outputs
OEA, OEB	**CLK_EN**	**CLK_SEL**	**Selected Source**	**QAx, QBx**
1	0	0	LVCMOS_CLK	Disabled; LOW
1	0	1	CLK, nCLK	Disabled; LOW
1	1	0	LVCMOS_CLK	Enabled
1 (default)	1 (default)	1 (default)	CLK, nCLK	Enabled
0	X	X		High-Impedance

NOTE: After CLK_EN switches, the clock outputs are disabled or enabled following a rising and falling input clock edge as shown in Figure 1.

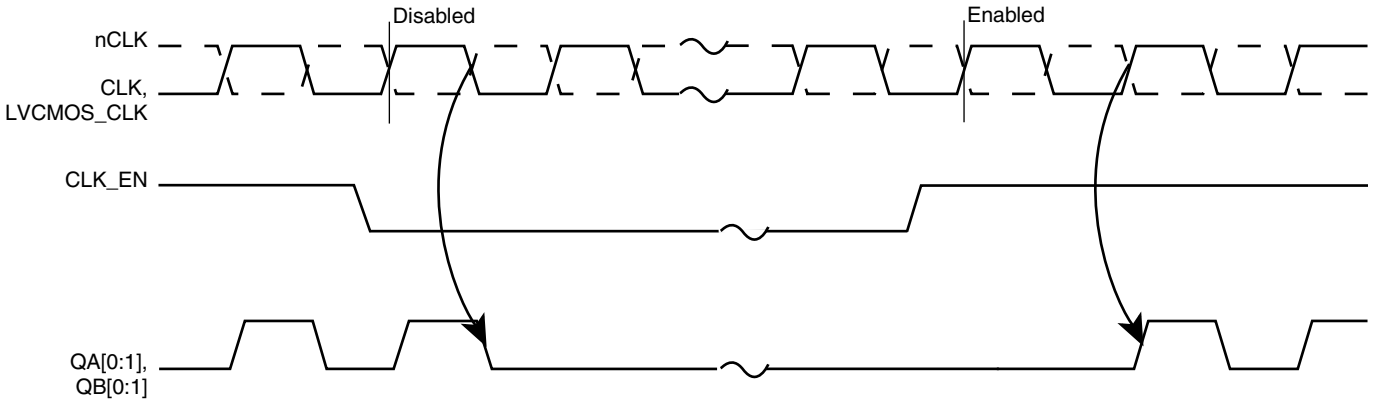


Figure 1. CLK_EN Timing Diagram

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5V
Outputs, V_O	-0.5V to V_{DDO} + 0.5V
Package Thermal Impedance, θ_{JA}	100.3°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, V_{DD} = 3.3V±5%, V_{DDO_A} = V_{DDO_B} = 3.3V±5% or 2.5V±5% or 1.8V±0.15V or 1.5V±5%, T_A = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Positive Supply Voltage		3.135	3.3	3.465	V
V_{DDO_A}, V_{DDO_B}	Output Supply Voltage		3.135	3.3	3.465	V
			2.375	2.5	2.625	V
			1.65	1.8	1.95	V
			1.425	1.5	1.575	V
I_{DD}	Power Supply Current				21	mA
I_{DDO_A} + I_{DDO_B}	Output Supply Current	No Load			5	mA

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Table 4B. LVCMOS DC Characteristics, V_{DD} = 3.3V±5%, V_{DDO_A} = V_{DDO_B} = 3.3V±5% or 2.5V±5% or 1.8V±0.15V or 1.5V±5%, T_A = 0°C to 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage			-0.3		0.8	V
I_{IH}	Input High Current	OEA, OEB, CLK_SEL, CLK_EN	V_{DD} = V_{IN} = 3.465V			5	µA
		LVCMOS_CLK	V_{DD} = V_{IN} = 3.465V			150	µA
I_{IL}	Input Low Current	OEA, OEB, CLK_SEL, CLK_EN	V_{DD} = 3.465V, V_{IN} = 0V	-150			µA
		LVCMOS_CLK	V_{DD} = 3.465V, V_{IN} = 0V	-5			µA
V_{OH}	Output High Voltage; NOTE 1		V_{DDO_X} = 3.3V ± 5%	2.6			V
			V_{DDO_X} = 2.5V ± 5%	1.8			V
			V_{DDO_X} = 1.8V ± 0.15V	1.5			V
			V_{DDO_X} = 1.5V ± 5%	V_{DDO_X} – 0.3			V
V_{OL}	Output Low Voltage; NOTE 1		V_{DDO_X} = 3.3V ± 5%			0.5	V
			V_{DDO_X} = 2.5V ± 5%			0.4	V
			V_{DDO_X} = 1.8V ± 0.15V			0.35	V
			V_{DDO_X} = 1.5V ± 5%			0.30	V
I_{OZL}	Output High-Impedance Low			-5			µA
I_{OZH}	Output High-Impedance High					5	µA

NOTE: V_{DDO_X} denotes V_{DDO_A} and V_{DDO_B}.
NOTE 1: Outputs terminated with 50Ω to V_{DDO_X}/2. See Parameter Measurement Information section, *Output Load Test Circuit diagrams.*

Table 4C. DC Characteristics, V_{DD} = 3.3V±5%, V_{DDO_A} = V_{DDO_B} = 3.3V±5% or 2.5V±5% or 1.8V±0.15V or 1.5V±5%, T_A = 0°C to 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	CLK,	V_{DD} = V_{IN} = 3.465V			150	µA
		nCLK	V_{DD} = V_{IN} = 3.465V			5	µA
I_{IL}	Input Low Current	CLK	V_{DD} = 3.465V, V_{IN} = 0V	-5			µA
		nCLK	V_{DD} = 3.465V, V_{IN} = 0V	-150			µA
V_{PP}	Peak-to-Peak Input Voltage; NOTE 1			0.15		1.3	V
V_{CMR}	Input Common Mode Voltage; NOTE 1, 2			GND + 0.5		V_{DD} – 0.85	V

NOTE 1: V_{IL} should not be less than -0.3V.
NOTE 2: Common mode voltage is defined as V_{IH}.

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AC Electrical Characteristics

Table 5A. AC Characteristics, $V_{DD} = V_{DDO_A} = V_{DDO_B} = 3.3V \pm 5\%$, $T_A = 0°C$ to $70°C$

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency					250	MHz
t_{PD}	Propagation Delay; NOTE 1			1.9		3.2	ns
*t*sk(o)	Output Skew; NOTE 2, 4		Measured on the Rising Edge			100	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 3, 4					900	ps
*t*sk(b)	Bank Skew; NOTE 4, 5					35	ps
*t*jit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section, NOTE 6	CLK, nCLK	156.25MHz, Integration Range: 12kHz - 20MHz		0.25		ps
t_R / t_F	Output Rise/Fall Time; NOTE 7		20% to 80%	100		700	ps
odc	Output Duty Cycle; NOTE 8	CLK, nCLK	$f_{OUT} \leq 156.25$MHz	45		55	%
		LVCMOS_CLK	$f_{OUT} \leq 156.25$MHz	40		60	%
t_{EN}	Output Enable Time: NOTE 7					5	ns
t_{DIS}	Output Disable Time: NOTE 7					5	ns

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE: All parameters measured at $f \leq 250$MHz unless noted otherwise.
NOTE 1: Measured from $V_{DD}/2$ of the input (LVCMOS_CLK) or from the differential input crossing point (CLK, nCLK) to $V_{DDO_X}/2$ of the output.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DDO_X}/2$.
NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages, with equal load conditions. Using the same type of inputs on each device, the outputs are measured at $V_{DDO_X}/2$.
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 5: Defined as skew within a bank of outputs at the same voltages and with equal load conditions.
NOTE 6: Driving only one input clock.
NOTE 7: These parameters are guaranteed by characterization. Not tested in production.
NOTE 8: Input duty cycle must be 50%.

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Table 5B. AC Characteristics, V_{DD} = 3.3V±5%, V_{DDO_A} = V_{DDO_B} = 2.5V±5%, T_A = 0°C to 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency					250	MHz
t_{PD}	Propagation Delay; NOTE 1			1.9		3.2	ns
*t*sk(o)	Output Skew; NOTE 2, 4		Measured on the Rising Edge			100	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 3, 4					900	ps
*t*sk(b)	Bank Skew; NOTE 4, 5					35	ps
*t*jit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section, NOTE 6	CLK, nCLK	156.25MHz, Integration Range: 12kHz - 20MHz		0.25		ps
t_R / t_F	Output Rise/Fall Time; NOTE 7		20% to 80%	100		700	ps
odc	Output Duty Cycle; NOTE 8	CLK, nCLK	f_{OUT} ≤ 156.25MHz	45		55	%
		LVCMOS_CLK	f_{OUT} ≤ 156.25MHz	40		60	%
t_{EN}	Output Enable Time: NOTE 7					5	ns
t_{DIS}	Output Disable Time: NOTE 7					5	ns

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE: All parameters measured at $f \leq$ 250MHz unless noted otherwise.
NOTE 1: Measured from V_{DD}/2 of the input (LVCMOS_CLK) or from the differential input crossing point (CLK, nCLK) to V_{DDO_X}/2 of the output.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at V_{DDO_X}/2.
NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages, with equal load conditions. Using the same type of inputs on each device, the outputs are measured at V_{DDO_X}/2.
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 5: Defined as skew within a bank of outputs at the same voltages and with equal load conditions.
NOTE 6: Driving only one input clock.
NOTE 7: These parameters are guaranteed by characterization. Not tested in production.
NOTE 8: Input duty cycle must be 50%.

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Table 5C. AC Characteristics, V_{DD} = 3.3V±5%, V_{DDO_A} = V_{DDO_B} = 1.8V±0.15V, T_A = 0°C to 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency					250	MHz
t_{PD}	Propagation Delay; NOTE 1			2.2		3.9	ns
*t*sk(o)	Output Skew; NOTE 2, 4		Measured on the Rising Edge			100	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 3, 4					1.2	ns
*t*sk(b)	Bank Skew; NOTE 4, 5					50	ps
*t*jit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section, NOTE 6	CLK, nCLK	156.25MHz, Integration Range: 12kHz - 20MHz		0.28		ps
t_R / t_F	Output Rise/Fall Time; NOTE 7		20% to 80%	100		800	ps
odc	Output Duty Cycle; NOTE 8	CLK, nCLK	f_{OUT} ≤ 156.25MHz	45		55	%
		LVCMOS_CLK	f_{OUT} ≤ 156.25MHz	40		60	%
t_{EN}	Output Enable Time: NOTE 7					5	ns
t_{DIS}	Output Disable Time: NOTE 7					5	ns

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE: All parameters measured at $f \leq$ 250MHz unless noted otherwise.
NOTE 1: Measured from V_{DD}/2 of the input (LVCMOS_CLK) or from the differential input crossing point (CLK, nCLK) to V_{DDO_X}/2 of the output.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at V_{DDO_X}/2.
NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages, with equal load conditions. Using the same type of inputs on each device, the outputs are measured at V_{DDO_X}/2.
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 5: Defined as skew within a bank of outputs at the same voltages and with equal load conditions.
NOTE 6: Driving only one input clock.
NOTE 7: These parameters are guaranteed by characterization. Not tested in production.
NOTE 8: Input duty cycle must be 50%.

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Table 5D. AC Characteristics, V_{DD} = 3.3V±5%, V_{DDO_A} = V_{DDO_B} = 1.5V±5%, T_A = 0°C to 70°C

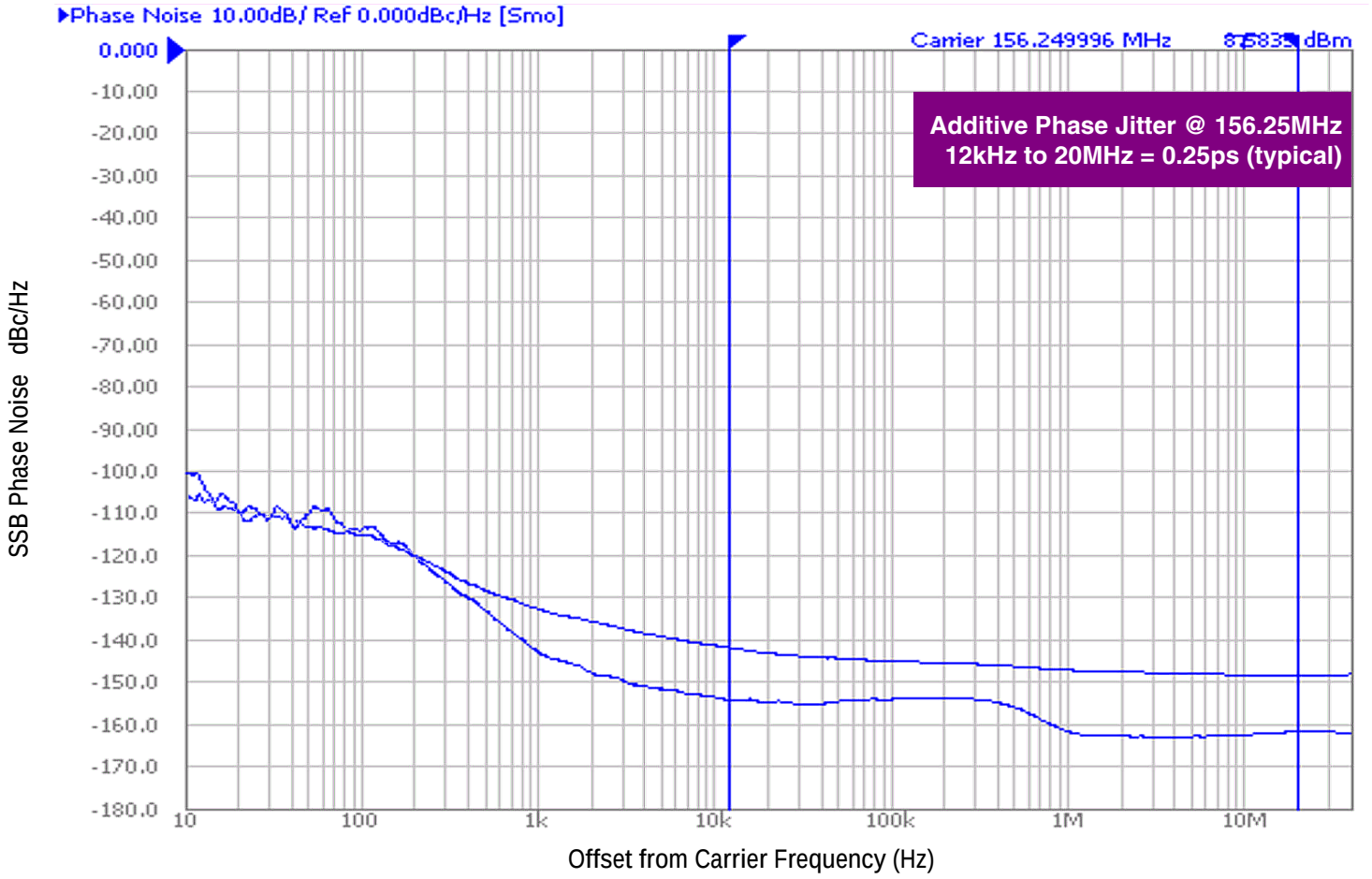
Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency					250	MHz
t_{PD}	Propagation Delay; NOTE 1			2.5		4.3	ns
*t*sk(o)	Output Skew; NOTE 2, 4		Measured on the Rising Edge			100	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 3, 4					1.6	ns
*t*sk(b)	Bank Skew; NOTE 4, 5					50	ps
*t*jit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section, NOTE 6	CLK, nCLK	156.25MHz, Integration Range: 12kHz - 20MHz		0.35		ps
t_R / t_F	Output Rise/Fall Time; NOTE 7		20% to 80%	100		800	ps
odc	Output Duty Cycle; NOTE 8	CLK, nCLK	f_{OUT} ≤ 156.25MHz	45		55	%
		LVCMOS_CLK	f_{OUT} ≤ 156.25MHz	40		60	%
t_{EN}	Output Enable Time: NOTE 7					5	ns
t_{DIS}	Output Disable Time: NOTE 7					5	ns

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE: All parameters measured at $f \leq$ 250MHz unless noted otherwise.
NOTE 1: Measured from V_{DD}/2 of the input (LVCMOS_CLK) or from the differential input crossing point (CLK, nCLK) to V_{DDO_X}/2 of the output.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at V_{DDO_X}/2.
NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages, with equal load conditions. Using the same type of inputs on each device, the outputs are measured at V_{DDO_X}/2.
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 5: Defined as skew within a bank of outputs at the same voltages and with equal load conditions.
NOTE 6: Driving only one input clock.
NOTE 7: These parameters are guaranteed by characterization. Not tested in production.
NOTE 8: Input duty cycle must be 50%.

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Additive Phase Jitter

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the *dBc Phase Noise.* This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a *dBc* value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.

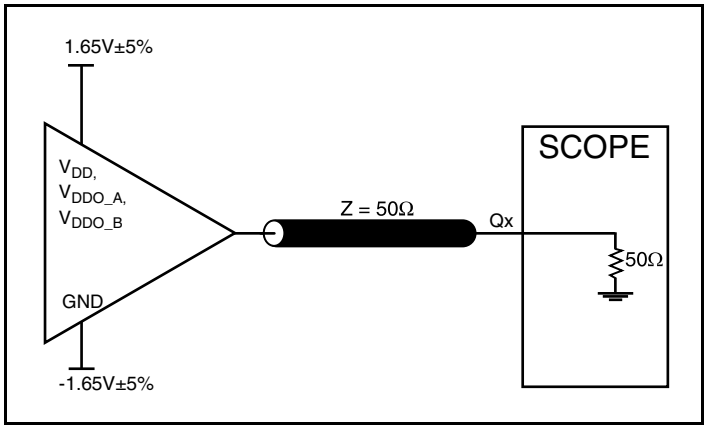


As with most timing specifications, phase noise measurements have issues relating to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This is illustrated above. The device meets the noise floor of what is shown, but can actually be lower. The phase noise is dependent on the input source and measurement equipment.

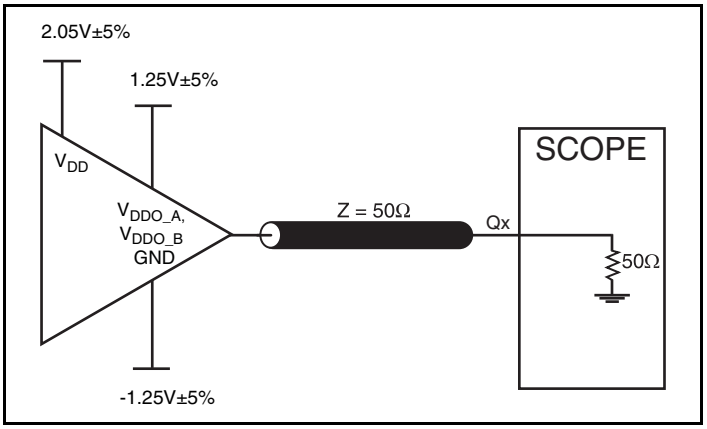
Measured using a Rohde & Schwarz SMA100 as the input source.

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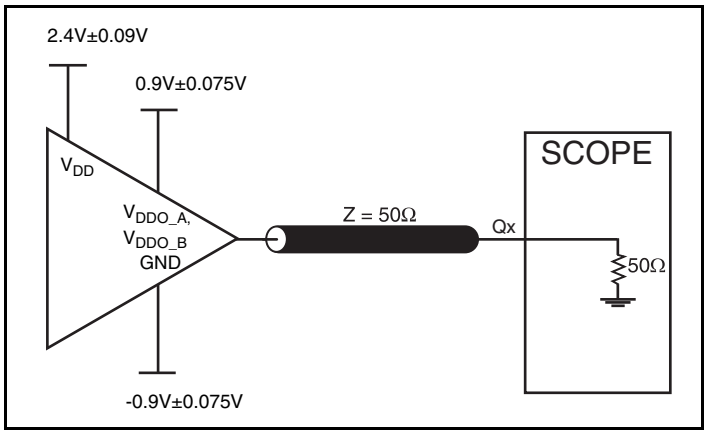
Parameter Measurement Information



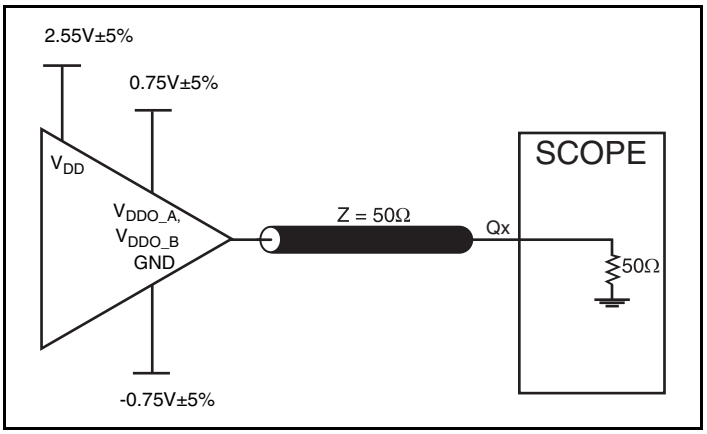
3.3V Core/3.3V LVCMOS Output Load Test Circuit



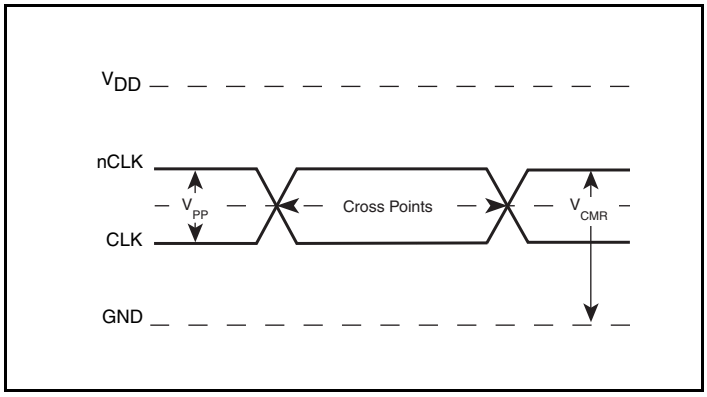
3.3V Core/2.5V LVCMOS Output Load Test Circuit



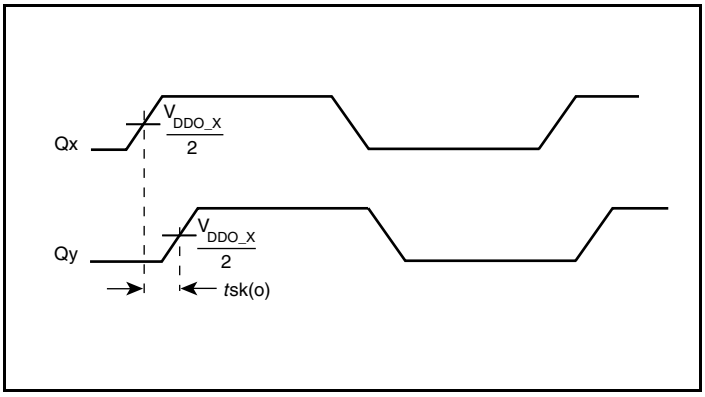
3.3V Core/1.8V LVCMOS Output Load Test Circuit



3.3V Core/1.5V LVCMOS Output Load Test Circuit

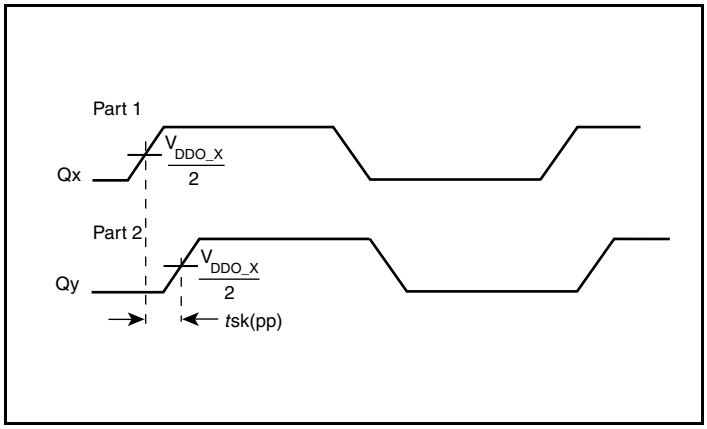


Differential Input Level

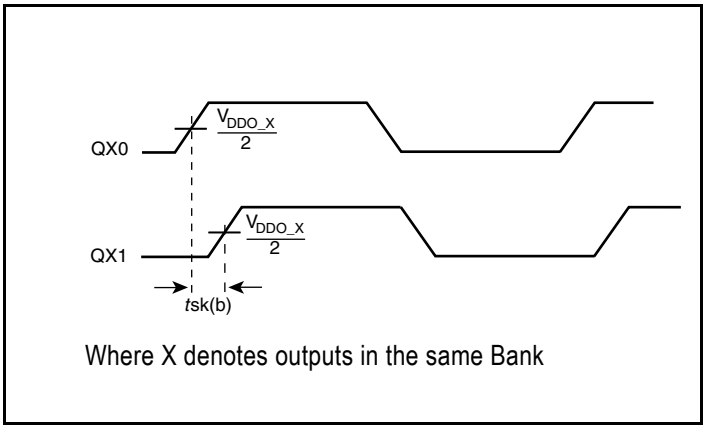


Output Skew

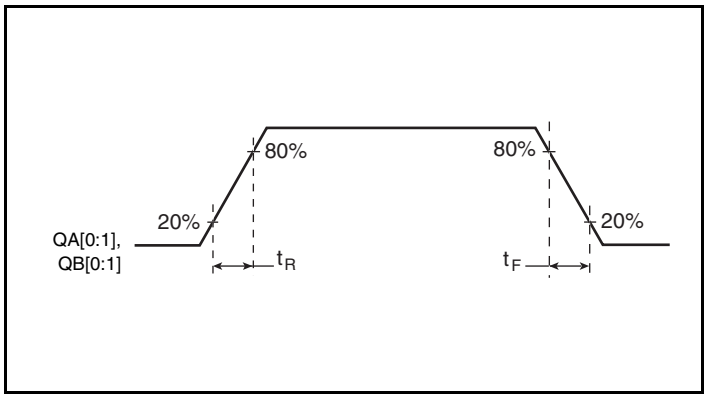
Parameter Measurement Information, continued



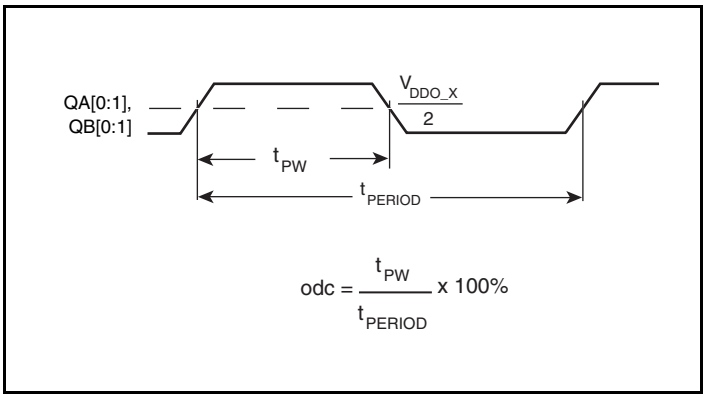
Part-to-Part Skew



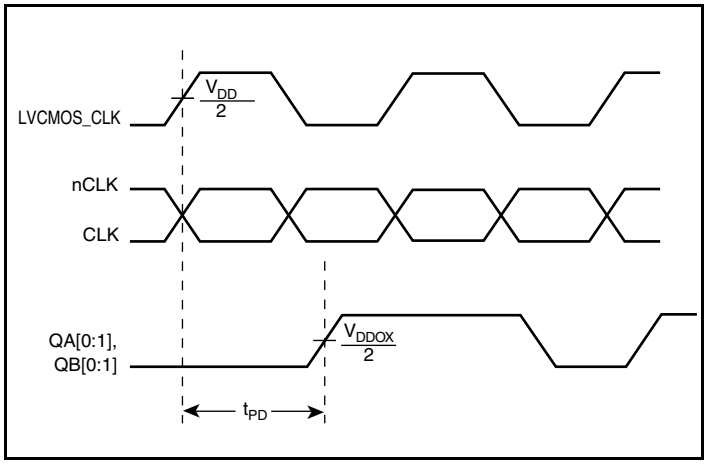
Bank Skew



Output Rise/Fall Time



Output Duty Cycle/Pulse Width/Period



Propagation Delay

Applications Information

Wiring the Differential Input to Accept Single-Ended Levels

Figure 2 shows how a differential input can be wired to accept single ended levels. The reference voltage $V_1 = V_{DD}/2$ is generated by the bias resistors R1 and R2. The bypass capacitor (C1) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of R1 and R2 might need to be adjusted to position the V_1 in the center of the input voltage swing. For example, if the input clock swing is 2.5V and V_{DD} = 3.3V, R1 and R2 value should be adjusted to set V_1 at 1.25V. The values below are for when both the single ended swing and V_{DD} are at the same voltage. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways. First, R3 and R4 in parallel should equal the transmission line impedance. For most 50Ω applications, R3 and R4 can be 100Ω. The values of the resistors can be increased to reduce the loading for slower and weaker LVCMOS driver. When using single-ended signaling, the noise rejection benefits of differential signaling are reduced. Even though the differential input can handle full rail LVCMOS signaling, it is recommended that the amplitude be reduced. The datasheet specifies a lower differential amplitude, however this only applies to differential signals. For single-ended applications, the swing can be larger, however V_{IL} cannot be less than -0.3V and V_{IH} cannot be more than V_{DD} + 0.3V. Though some of the recommended components might not be used, the pads should be placed in the layout. They can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a differential signal.

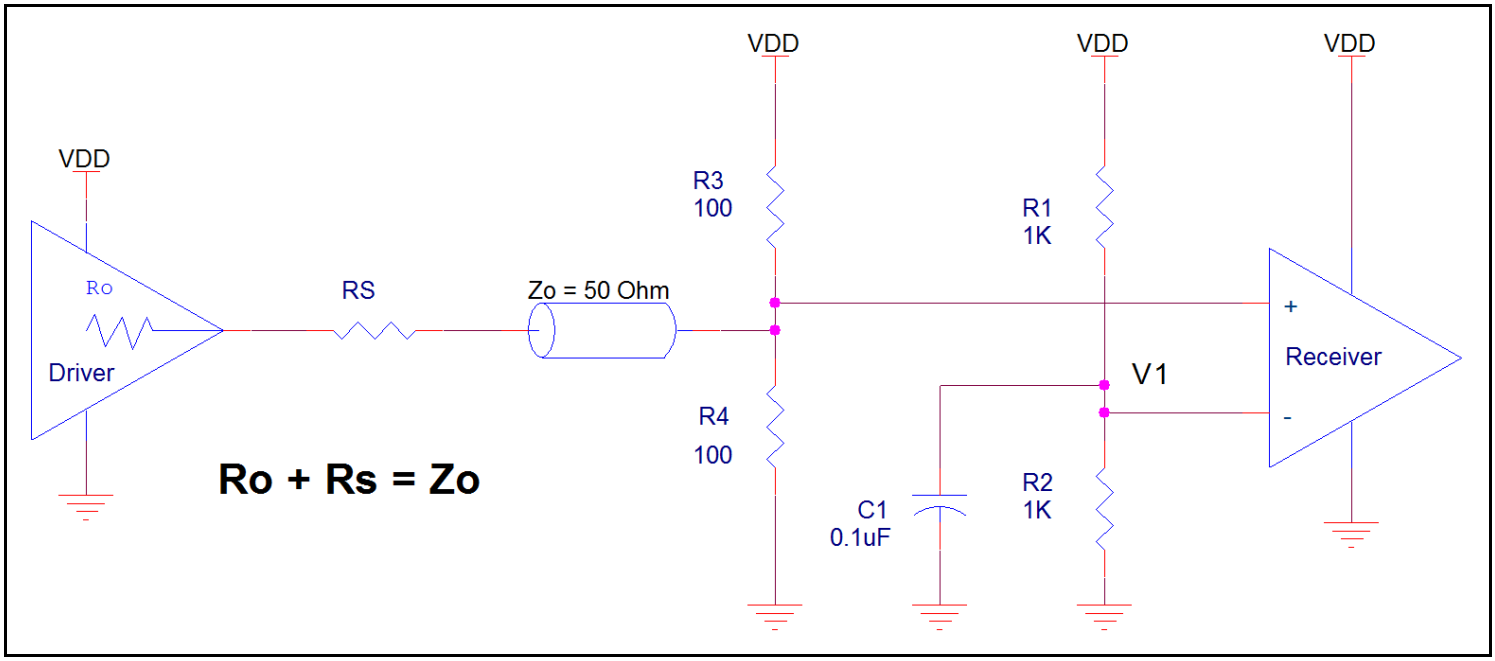


Figure 2. Recommended Schematic for Wiring a Differential Input to Accept Single-ended Levels

Recommendations for Unused Input and Output Pins

Inputs:

CLK/nCLK Inputs

For applications not requiring the use of the differential input, both CLK and nCLK can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from CLK to ground.

LVCMOS_CLK Input

For applications not requiring the use of the single-ended clock input, it can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from the LVCMOS_CLK input to ground.

LVCMOS Control Pins

All control pins have internal pullups or pulldowns; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs:

LVCMOS Outputs

All unused LVCMOS output can be left floating. There should be no trace attached.

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Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, HCSL and other differential signals. The differential signals must meet the V_{PP} and V_{CMR} input requirements. *Figures 3A to 3E* show interface examples for the CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example, in Figure 3A, the input termination applies for IDT open emitter LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

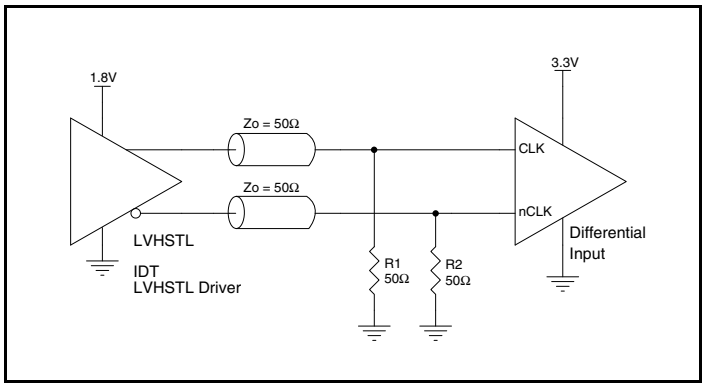


Figure 3A. CLK/nCLK Input Driven by an IDT Open Emitter LVHSTL Driver

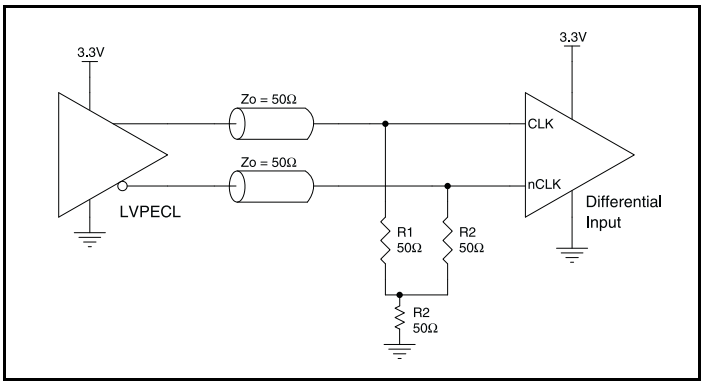


Figure 3B. CLK/nCLK Input Driven by a 3.3V LVPECL Driver

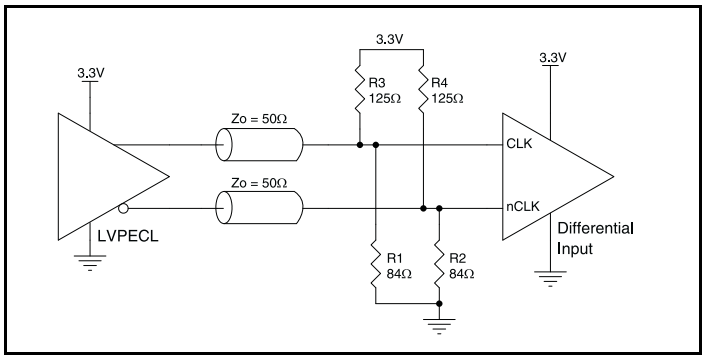


Figure 3C. CLK/nCLK Input Driven by a 3.3V LVPECL Driver

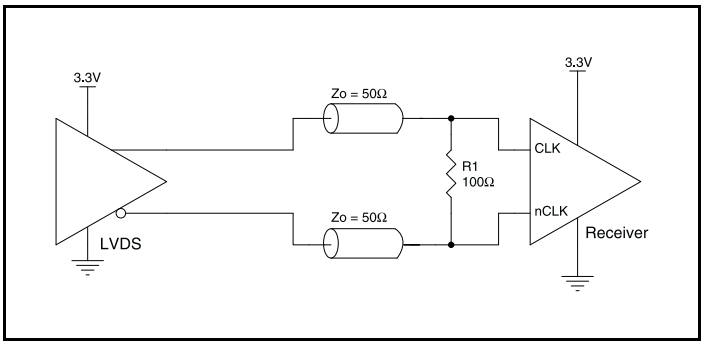


Figure 3D. CLK/nCLK Input Driven by a 3.3V LVDS Driver

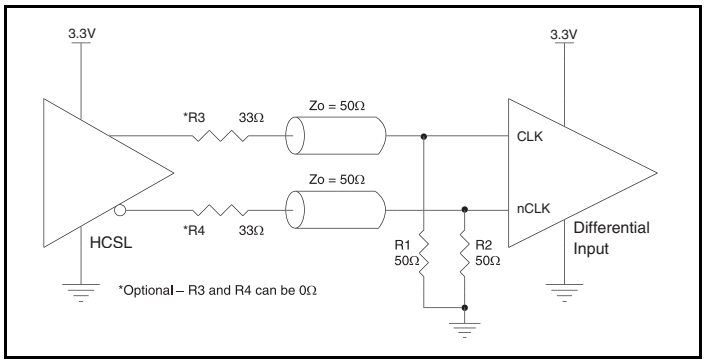


Figure 3E. CLK/nCLK Input Driven by a 3.3V HCSL Driver

Power Considerations

This section provides information on power dissipation and junction temperature for the 8305-02.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the 8305-02 is the sum of the core power plus the power dissipation due to loading.
The following is the power dissipation for V_{DD} = 3.3V + 5% = 3.465V, which gives worst case results.

- Power $(core)_{MAX} = V_{DD_MAX} * I_{DD_MAX}$= 3.465V *21mA = **72.765mW**

LVCMOS Driver Power Dissipation

- Output Impedance R_{OUT} Power Dissipation due to Loading 50Ω to $V_{DD}/2$
  Output Current $I_{OUT} = V_{DD_MAX} / [2 * (50Ω + R_{OUT})]$ = 3.465V / [2 * (50Ω + 9Ω)] = **35.36mA**
- Power Dissipation on the R_{OUT} per LVCMOS output
  Power (LVCMOS) = $R_{OUT} * (I_{OUT})^2$ = 9Ω * (35.36mA)^2 = **11.25mW per output**

Total Power Dissipation on the R_{OUT}
Total Power (R_{OUT}) = 11.25mW * 4 = **45mW**

Dynamic Power Dissipation at 250MHz
Power (250MHz) = C_{PD} * Frequency * $(V_{DD})^2$ * Number of outputs = 13pF * 250MHz * (3.465V)^2 * 4 = **156.53mW**

Total Power
= $(core)_{MAX}$ + Total Power **(R_{OUT})** + Power (250MHz)
= 72.765mW + 45mW + 156.53mW
= 274.3mW

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad, and directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 100.3°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 70°C with all outputs switching is:

70°C + 0.274W *100.3°C/W = 97.5°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 6. Thermal Resistance θ_{JA} for 16 Lead TSSOP, Forced Convection

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	100.3°C/W	96.0°C/W	93.9°C/W

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Reliability Information

Table 7. θ_{JA} vs. Air Flow Table for a 16 Lead TSSOP

θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	100.3°C/W	96.0°C/W	93.9°C/W

Transistor Count

The transistor count for 8305-02: 538

Package Outline and Package Dimensions

Package Outline - G Suffix for 16 Lead TSSOP

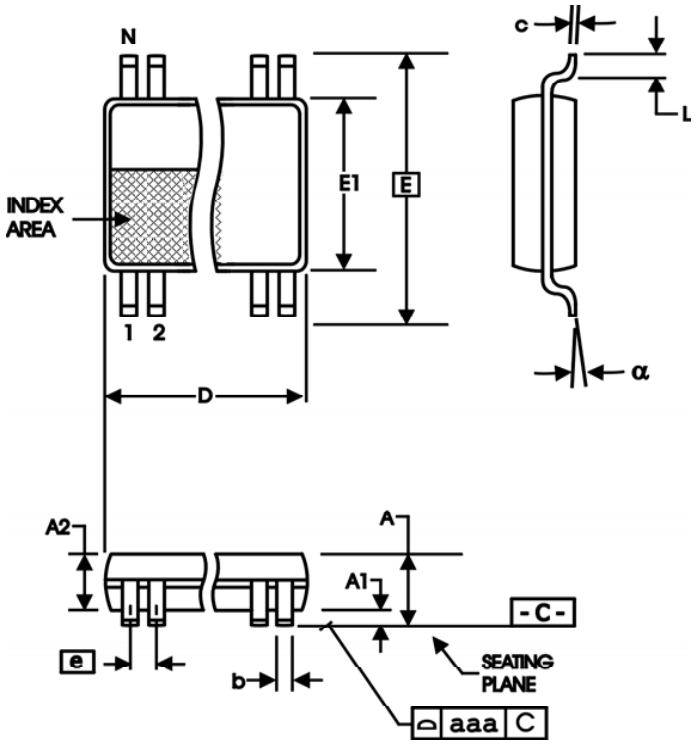


Table 8. Package Dimensions for 16 Lead TSSOP

All Dimensions in Millimeters		
Symbol	**Minimum**	**Maximum**
N	16	
A		1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	4.90	5.10
E	6.40 Basic	
E1	4.30	4.50
e	0.65 Basic	
L	0.45	0.75
α	0°	8°
aaa		0.10

Reference Document: JEDEC Publication 95, MO-153

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Ordering Information

Table 9. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
8305AG-02LF	8305A02L	“Lead-Free” 16 Lead TSSOP	Tube	0°C to 70°C
8305AG-02LFT	8305A02L	“Lead-Free” 16 Lead TSSOP	Tape & Reel	0°C to 70°C

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Revision History

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Revision Date	Description of Change
May 19, 2016	▪ Removed ICS in the part number where needed. Updated header and footer. ▪ Product Discontinuation Notice - Last time buy expires May 6, 2017 ▪ PDN CQ-16-01

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