General Description

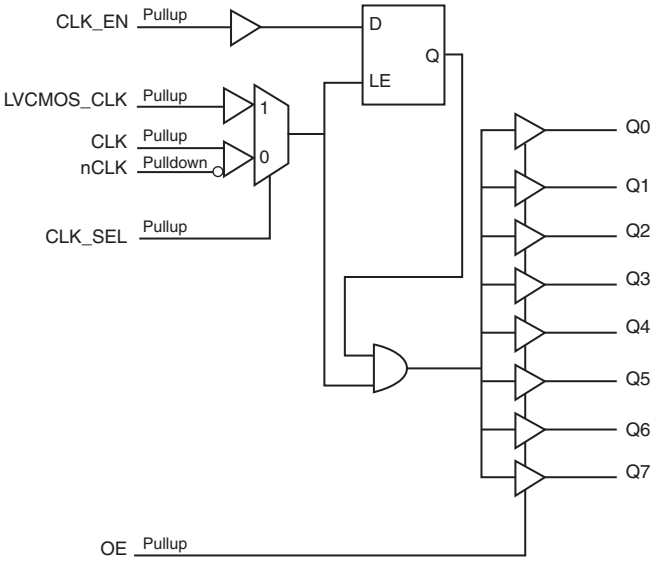
The 8308I is a low-skew, 1-to-8 Fanout Buffer. The 8308I has two selectable clock inputs. The CLK, nCLK pair can accept most differential input levels. The LVCMOS_CLK can accept LVCMOS or LVTTL input levels. The low impedance LVCMOS/LVTTL outputs are designed to drive 50Ω series or parallel terminated transmission lines. The effective fanout can be increased from 8 to 16 by utilizing the ability of the outputs to drive two series terminated transmission lines.

The 8308I is characterized for 3.3V core/3.3V output, 3.3V core/2.5V output or 2.5V core/2.5V output operation. Guaranteed output and part-part skew characteristics make the 8308I ideal for those clock distribution applications requiring well defined performance and repeatability.

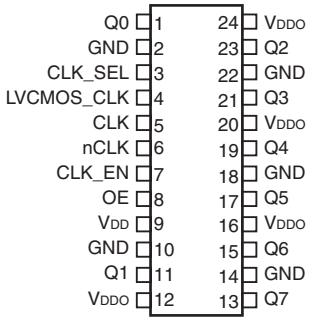
Features

- Eight LVCMOS/LVTTL outputs, (7Ω typical output impedance)
- Selectable LVCMOS_CLK or differential CLK, nCLK inputs
- CLK, nCLK pair can accept the following differential input levels: LVPECL, LVDS, LVHSTL, SSTL, HCSL
- Maximum Output Frequency: 350MHz
- Output Skew: (3.3V± 5%): 100ps (maximum)
- Part to Part Skew: (3.3V± 5%): 1ns (maximum)
- Supply Voltage Modes:
  (Core/Output)
  3.3V/3.3V
  3.3V/2.5V
  2.5V/2.5V
- -40°C to 85°C ambient operating temperature
- Available in lead-free (RoHS 6) package

Block Diagram



Pin Assignment



8308I
24-Lead, 173-MIL TSSOP
4.4mm x 7.8mm x 0.925mm body package
G Package
Top View

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TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1, 11, 13, 15, 17, 19, 21, 23	Q0, Q1, Q7, Q6, Q5, Q4,Q3, Q2	Output		Clock outputs. LVCMOS / LVTTL interface levels.
2, 10, 14, 18, 22	GND	Power		Power supply ground.
3	CLK_SEL	Input	Pullup	Clock select input. Selects LVCMOS clock input when HIGH. Selects CLK, nCLK inputs when LOW. See Table 3A. LVCMOS / LVTTL interface levels.
4	LVCMOS_CLK	Input	Pullup	Clock input. LVCMOS / LVTTL interface levels.
5	CLK	Input	Pullup	Non-inverting differential clock input.
6	nCLK	Input	Pulldown	Inverting differential clock input.
7	CLK_EN	Input	Pullup	Clock enable. LVCMOS / LVTTL interface levels.
8	OE	Input	Pullup	Output enable. LVCMOS / LVTTL interface levels. See Table 3B.
9	V_{DD}	Power		Power supply pin.
12, 16, 20, 24	V_{DDO}	Power		Output supply pins.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
C_{PD}	Power Dissipation Capacitance (per output)			12		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ
R_{OUT}	Output Impedance		5	7	12	Ω

TABLE 3A. CLOCK SELECT FUNCTION TABLE

Control Input	Clock Input
CLK_SEL	
0	CLK, nCLK is selected
1	LVCMOS_CLK is selected

TABLE 3B. OE SELECT FUNCTION TABLE

Control Input	Output Operation
OE	
0	Outputs Q0:Q7 are in Hi-Z (disabled)
1	Outputs Q0:Q7 are active (enabled)

TABLE 3C. CLOCK INPUT FUNCTION TABLE

Inputs				Outputs	Input to Output Mode	Polarity
CLK_SEL	LVCMOS_CLK	CLK	nCLK	Q0:Q7		
0	—	0	1	LOW	Differential to Single Ended	Non Inverting
0	—	1	0	HIGH	Differential to Single Ended	Non Inverting
0	—	0	Biased; NOTE 1	LOW	Single Ended to Single Ended	Non Inverting
0	—	1	Biased; NOTE 1	HIGH	Single Ended to Single Ended	Non Inverting
0	—	Biased; NOTE 1	0	HIGH	Single Ended to Single Ended	Inverting
0	—	Biased; NOTE 1	1	LOW	Single Ended to Single Ended	Inverting
1	0	—	—	LOW	Single Ended to Single Ended	Non Inverting
1	1	—	—	HIGH	Single Ended to Single Ended	Non Inverting

NOTE 1: Please refer to the Application Information section, “Wiring the Differential Input to Accept Single Ended Levels”.

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Absolute Maximum Ratings

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5 V
Outputs, V_O	-0.5V to V_{DDO} + 0.5V
Package Thermal Impedance, θ_{JA}	70°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Table 4A. Power Supply DC Characteristics, $V_{DD} = V_{DDO} = 3.3V\pm5\%$, T_A = -40° to 85°

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Power Supply Voltage		3.135	3.3	3.465	V
V_{DDO}	Output Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current				46	mA
I_{DDO}	Output Supply Current				11	mA

Table 4B. Power Supply DC Characteristics, $V_{DD} = 3.3V\pm5\%$, $V_{DDO} = 2.5V\pm5\%$, T_A = -40° to 85°

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Power Supply Voltage		3.135	3.3	3.465	V
V_{DDO}	Output Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Power Supply Current				46	mA
I_{DDO}	Output Supply Current				10	mA

Table 4C. Power Supply DC Characteristics, V_{DD}, $V_{DDO} = 2.5V\pm5\%$, T_A = -40° to 85°

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Power Supply Voltage		2.375	2.5	2.625	V
V_{DDO}	Output Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Power Supply Current				43	mA
I_{DDO}	Output Supply Current				10	mA

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TABLE 4D. DC CHARACTERISTICS, $V_{DD} = V_{DDO} = 3.3V \pm 5\%$, $T_A = -40°$ TO $85°$

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	LVCMOS		2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage	LVCMOS_CLK		-0.3		1.3	V
		CLK_EN, OE				0.8	V
I_{IN}	Input Current		$V_{IN} = V_{DD}$ or V_{IN} = GND			300	µA
V_{OH}	Output High Voltage; NOTE 1		I_{OH} = -24mA	2.4			V
V_{OL}	Output Low Voltage; NOTE 1		I_{OL} = 24mA			0.55	V
			I_{OL} = 12mA			0.30	V
V_{PP}	Peak-to-Peak Input Voltage	CLK, nCLK		0.15		1.3	V
V_{CMR}	Input Common Mode Voltage; NOTE 2, 3	CLK, nCLK		GND + 0.5		V_{DD} - 0.85	V

NOTE 1: Outputs capable of driving 50Ω transmission lines terminated with 50Ω to $V_{DDO}/2$.
See Parameter Measurement section, “3.3V Output Load AC Test Circuit”.
NOTE 2: For single ended applications, the maximum input voltage for CLK, nCLK is V_{DD} + 0.3V.
NOTE 3: Common mode voltage is defined as V_{IH}.

TABLE 4E. DC CHARACTERISTICS, $V_{DD} = 3.3V \pm 5\%$, $V_{DDO} = 2.5V \pm 5\%$, $T_A = -40°$ TO $85°$

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	LVCMOS		2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage	LVCMOS_CLK		-0.3		1.3	V
		CLK_EN, OE				0.8	V
I_{IN}	Input Current		$V_{IN} = V_{DD}$ or V_{IN} = GND			300	µA
V_{OH}	Output High Voltage; NOTE 1		I_{OH} = -15mA	1.8			V
V_{OL}	Output Low Voltage; NOTE 1		I_{OL} = 15mA			0.6	V
V_{PP}	Peak-to-Peak Input Voltage	CLK, nCLK		0.15		1.3	V
V_{CMR}	Input Common Mode Voltage; NOTE 2, 3	CLK, nCLK		GND + 0.5		V_{DD} - 0.85	V

NOTE 1: Outputs capable of driving 50Ω transmission lines terminated with 50Ω to $V_{DDO}/2$.
See Parameter Measurement section, “3.3V Output Load AC Test Circuit”.
NOTE 2: For single ended applications, the maximum input voltage for CLK, nCLK is V_{DD} + 0.3V.
NOTE 3: Common mode voltage is defined as V_{IH}.

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TABLE 4F. DC CHARACTERISTICS, V_{DD}, V_{DDO} = 2.5V±5%, T_A = -40° TO 85°

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	LVCMOS		1.7		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage	LVCMOS_CLK		-0.3		0.7	V
		CLK_EN, OE				0.7	V
I_{IN}	Input Current		V_{IN} = V_{DD} or V_{IN} = GND			300	µA
V_{OH}	Output High Voltage; NOTE 1		I_{OH} = -15mA	1.8			V
V_{OL}	Output Low Voltage; NOTE 1		I_{OL} = 15mA			0.6	V
V_{PP}	Peak-to-Peak Input Voltage	CLK, nCLK		0.15		1.3	V
V_{CMR}	Input Common Mode Voltage; NOTE 2, 3	CLK, nCLK		GND + 0.5		V_{DD} - 0.85	V

NOTE 1: Outputs capable of driving 50Ω transmission lines terminated with 50Ω to V_{DDO}/2. See Parameter Measurement section, “3.3V Output Load AC Test Circuit”.
NOTE 2: For single ended applications, the maximum input voltage for CLK, nCLK is V_{DD} + 0.3V.
NOTE 3: Common mode voltage is defined as V_{IH}.

TABLE 5A. AC CHARACTERISTICS, V_{DD} = V_{DDO} = 3.3V±5%, T_A = -40° TO 85°

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency					350	MHz
t_{PD}	Propagation Delay;	CLK, nCLK; NOTE 1	$f \leq$ 350MHz	2		4	ns
		LVCMOS_CLK; NOTE 2	$f \leq$ 350MHz	2		4	ns
tsk(o)	Output Skew; NOTE 3, 7		Measured on rising edge @V_{DDO}/2			100	ps
tsk(pp)	Part-to-Part Skew; NOTE 4, 7		Measured on rising edge @V_{DDO}/2			1	ns
t_R / t_F	Output Rise/Fall Time		0.8V to 2V	0.2		1	ns
odc	Output Duty Cycle		$f \leq$ 150MHz, Ref = CLK, nCLK	45		55	%
t_{PZL}, t_{PZH}	Output Enable Time; NOTE 5					5	ns
t_{PLZ}, t_{PHZ}	Output Disable Time; NOTE 5					5	ns
t_S	Clock Enable Setup Time; NOTE 6	CLK_EN to CLK, nCLK		1			ns
		CLK_EN to LVCMOS_CLK		0			ns
t_H	Clock Enable Hold Time; NOTE 6	CLK, nCLK to CLK_EN		0			ns
		LVCMOS_CLK to CLK_EN		1			ns

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE 1: Measured from the differential input crossing point to V_{DDO}/2 of the output.
NOTE 2: Measured from V_{DD}/2 of the input to V_{DDO}/2 of the output.
NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at V_{DDO}/2.
NOTE 4: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at V_{DDO}/2.
NOTE 5: These parameters are guaranteed by characterization. Not tested in production.
NOTE 6: Setup and Hold times are relative to the rising edge of the input clock.
NOTE 7: This parameter is defined in accordance with JEDEC Standard 65.

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TABLE 5B. AC CHARACTERISTICS, V_{DD} = 3.3V±5%, V_{DDO} = 2.5V±5%, T_A = -40° TO 85°

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency					350	MHz
t_{PD}	Propagation Delay;	CLK, nCLK; NOTE 1	$f \leq$ 350MHz	2		4	ns
		LVCMOS_CLK; NOTE 2	$f \leq$ 350MHz	2		4	ns
*t*sk(o)	Output Skew; NOTE 3, 7		Measured on rising edge @V_{DDO}/2			100	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 4, 7		Measured on rising edge @V_{DDO}/2			1	ns
t_R / t_F	Output Rise/Fall Time		0.6V to 1.8V	0.2		1.0	ns
odc	Output Duty Cycle		$f \leq$ 150MHz, Ref = CLK, nCLK	45		55	%
t_{PZL}, t_{PZH}	Output Enable Time; NOTE 5					5	ns
t_{PLZ}, t_{PHZ}	Output Disable Time; NOTE 5					5	ns
t_S	Clock Enable Setup Time; NOTE 6	CLK_EN to CLK, nCLK		1			ns
		CLK_EN to LVCMOS_CLK		0			ns
t_H	Clock Enable Hold Time; NOTE 6	CLK, nCLK to CLK_EN		0			ns
		LVCMOS_CLK to CLK_EN		1			ns

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE 1: Measured from the differential input crossing point to V_{DDO}/2 of the output.
NOTE 2: Measured from V_{DD}/2 of the input to V_{DDO}/2 of the output.
NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at V_{DDO}/2.
NOTE 4: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at V_{DDO}/2.
NOTE 5: These parameters are guaranteed by characterization. Not tested in production.
NOTE 6: Setup and Hold times are relative to the rising edge of the input clock.
NOTE 7: This parameter is defined in accordance with JEDEC Standard 65.

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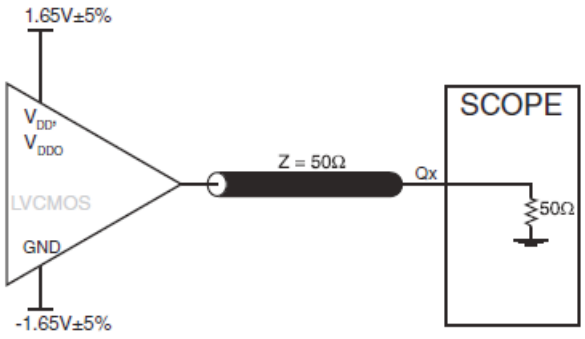
TABLE 5C. AC CHARACTERISTICS, $V_{DD} = V_{DDO} = 2.5V \pm 5\%$, $T_A = -40°$ TO $85°$

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency					350	MHz
t_{PD}	Propagation Delay;	CLK, nCLK; NOTE 1	$f \leq 350MHz$	1.5		4.2	ns
		LVCMOS_CLK; NOTE 2	$f \leq 350MHz$	1.7		4.4	ns
*t*sk(o)	Output Skew; NOTE 3, 7		Measured on rising edge @$V_{DDO}/2$			160	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 4, 7		Measured on rising edge @$V_{DDO}/2$			2	ns
t_R / t_F	Output Rise/Fall Time		0.6V to 1.8V	0.2		1.0	ns
odc	Output Duty Cycle		$f \leq 150MHz$, Ref = CLK, nCLK	40		60	%
t_{PZL}, t_{PZH}	Output Enable Time; NOTE 5					5	ns
t_{PLZ}, t_{PHZ}	Output Disable Time; NOTE 5					5	ns
t_S	Clock Enable Setup Time; NOTE 6	CLK_EN to CLK, nCLK		1			ns
		CLK_EN to LVCMOS_CLK		0			ns
t_H	Clock Enable Hold Time; NOTE 6	CLK, nCLK to CLK_EN		0			ns
		LVCMOS_CLK to CLK_EN		1			ns

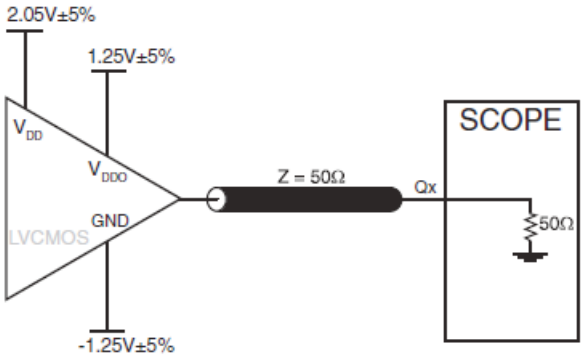
NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE 1: Measured from the differential input crossing point to $V_{DDO}/2$ of the output.
NOTE 2: Measured from $V_{DD}/2$ of the input to $V_{DDO}/2$ of the output.
NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DDO}/2$.
NOTE 4: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at $V_{DDO}/2$.
NOTE 5: These parameters are guaranteed by characterization. Not tested in production.
NOTE 6: Setup and Hold times are relative to the rising edge of the input clock.
NOTE 7: This parameter is defined in accordance with JEDEC Standard 65.

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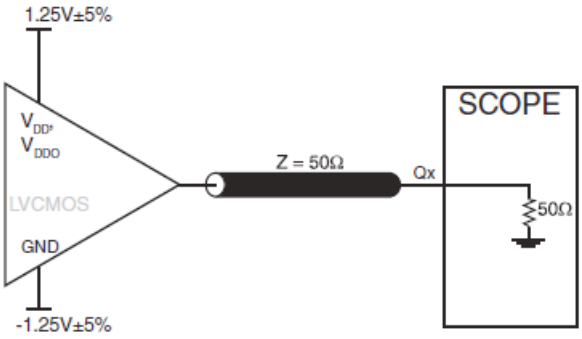
PARAMETER MEASUREMENT INFORMATION



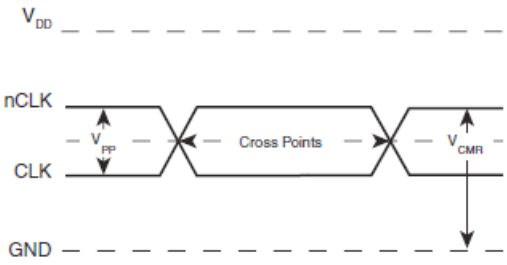
3.3V CORE/3.3V OUTPUT LOAD AC TEST CIRCUIT



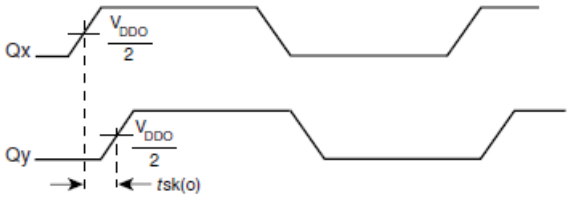
3.3V CORE/2.5V OUTPUT LOAD AC TEST CIRCUIT



2.5V CORE/2.5V OUTPUT LOAD AC TEST CIRCUIT



DIFFERENTIAL INPUT LEVEL

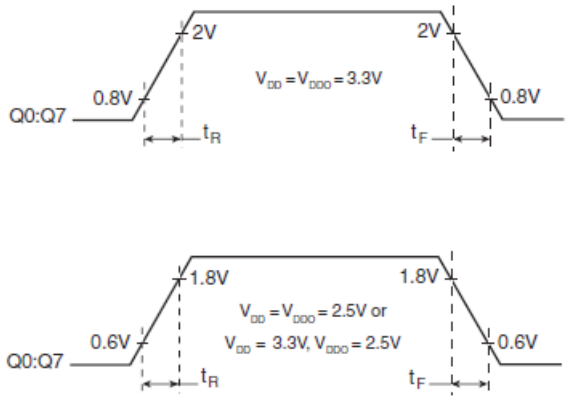


OUTPUT SKEW

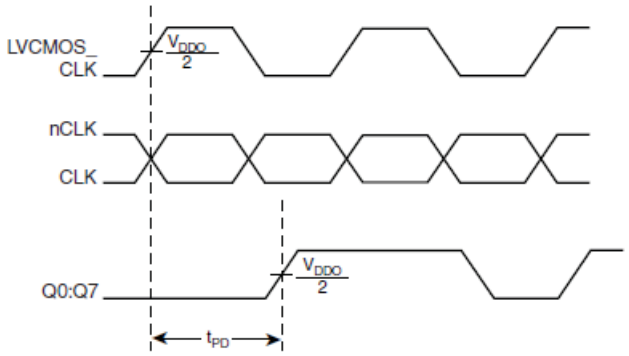


PART-TO-PART SKEW

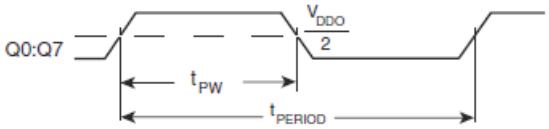
PARAMETER MEASUREMENT INFORMATION, CONTINUED



OUTPUT RISE/FALL TIME



PROPAGATION DELAY



$$odc = \frac{t_{PW}}{t_{PERIOD}} \times 100\%$$

OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD

APPLICATION INFORMATION

WIRING THE DIFFERENTIAL INPUT TO ACCEPT SINGLE ENDED LEVELS

Figure 1 shows how a differential input can be wired to accept single ended levels. The reference voltage V_{REF} = V_{DD}/2 is generated by the bias resistors R1 and R2. The bypass capacitor (C1) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of R1 and R2 might need to be adjusted to position the V_{REF} in the center of the input voltage swing. For example, if the input clock swing is 2.5V and V_{DD} = 3.3V, R1 and R2 value should be adjusted to set V_{REF} at 1.25V. The values below are for when both the single-ended swing and V_{DD} are at the same voltage. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways. First, R3 and R4 in parallel should equal the transmission line impedance. For most 50 applications, R3 and R4 can be 100Ω. The values of the resistors can be increased to reduce the loading for slower and weaker LVCMOS driver. When using single ended signaling, the noise rejection benefits of differential signaling are reduced. Even though the differential input can handle full rail LVCMOS signaling, it is recommended that the amplitude be reduced. The datasheet specifies a lower differential amplitude, however this only applies to differential signals. For single-ended applications, the swing can be larger, however V_{IL} cannot be less than -0.3V and V_{IH} cannot be more than V_{DD} + 0.3V. Though some of the recommended components might not be used, the pads should be placed in the layout. They can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a differential signal.

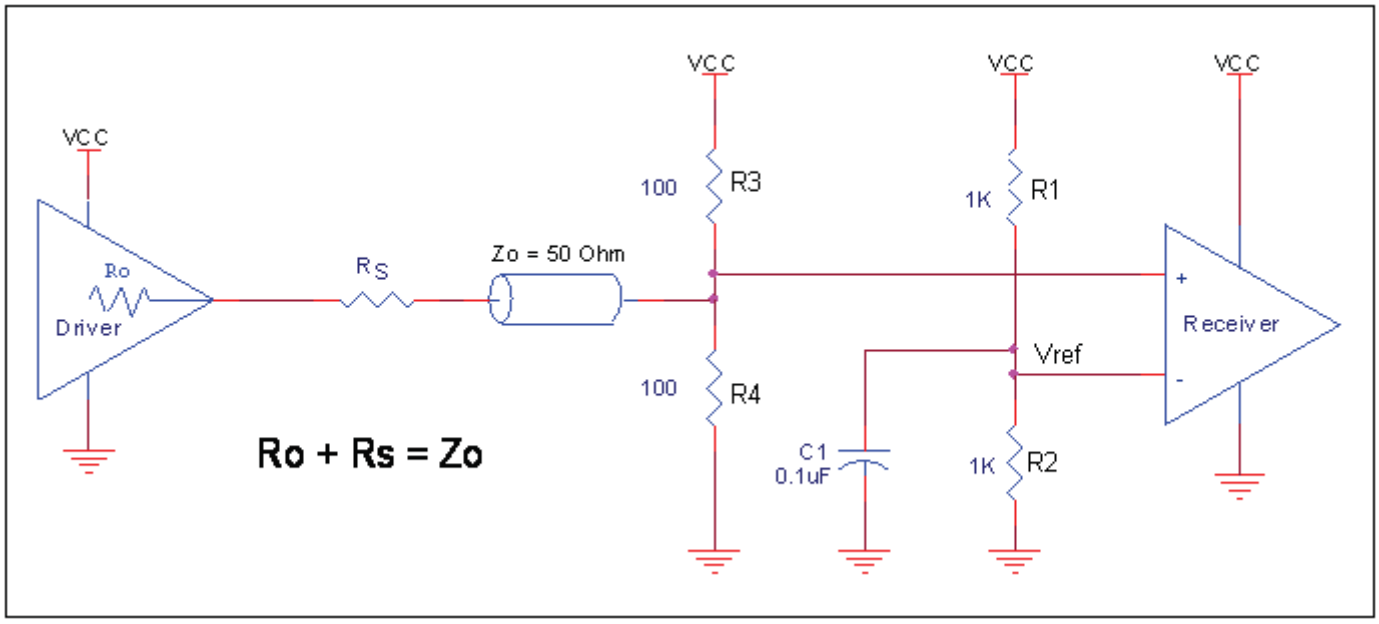


FIGURE 1. RECOMMENDED SCHEMATIC FOR WIRING A DIFFERENTIAL INPUT TO ACCEPT SINGLE-ENDED LEVELS

Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, SSTL, HCSL and other differential signals. Both differential signals must meet the V_{PP} and V_{CMR} input requirements. Figures 2A to 2E show interface examples for the CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example in *Figure 2A,* the input termination applies for IDT LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

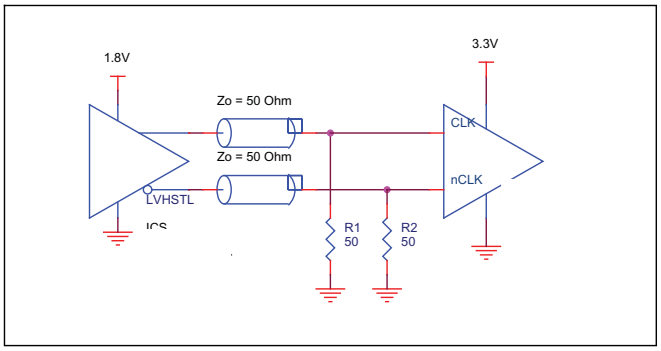


Figure 2A. CLK/nCLK Input Driven by IDT's LVHSTL Driver

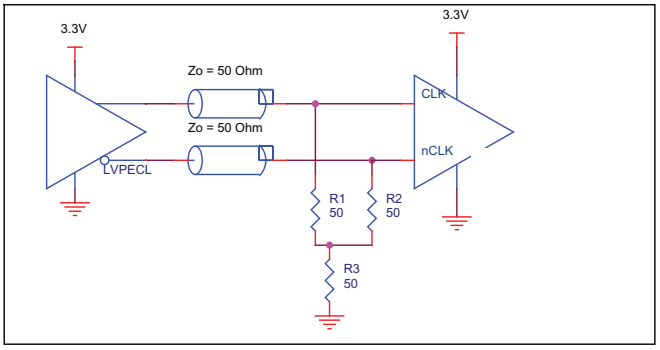


Figure 2B. CLK/nCLK Input Driven by 3.3V LVPECL Driver

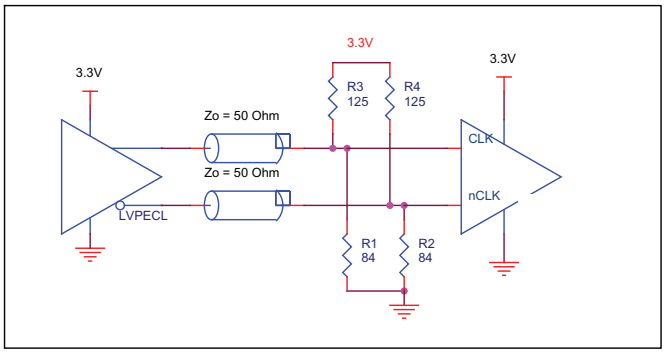


Figure 2C. CLK/nCLK Input Driven by 3.3V LVPECL Driver

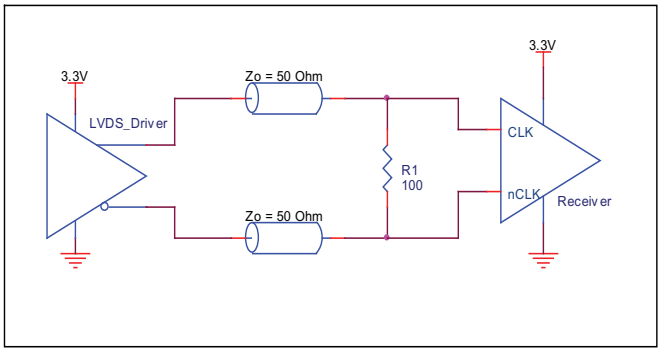


Figure 2D. CLK/nCLK Input Driven by 3.3V LVDS Driver

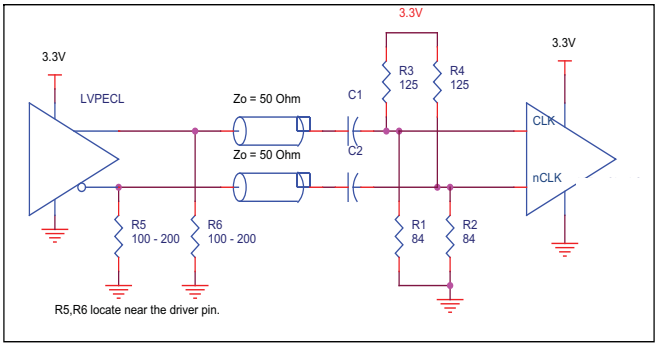


Figure 2E. CLK/nCLK Input Driven by 3.3V LVPECL Driver with AC Couple

Schematic Example

Figure 3 shows a schematic example of the 8308I. In this example, the LVCMOS_CLK input is selected. The decoupling capacitors should be physically located near the power pin.

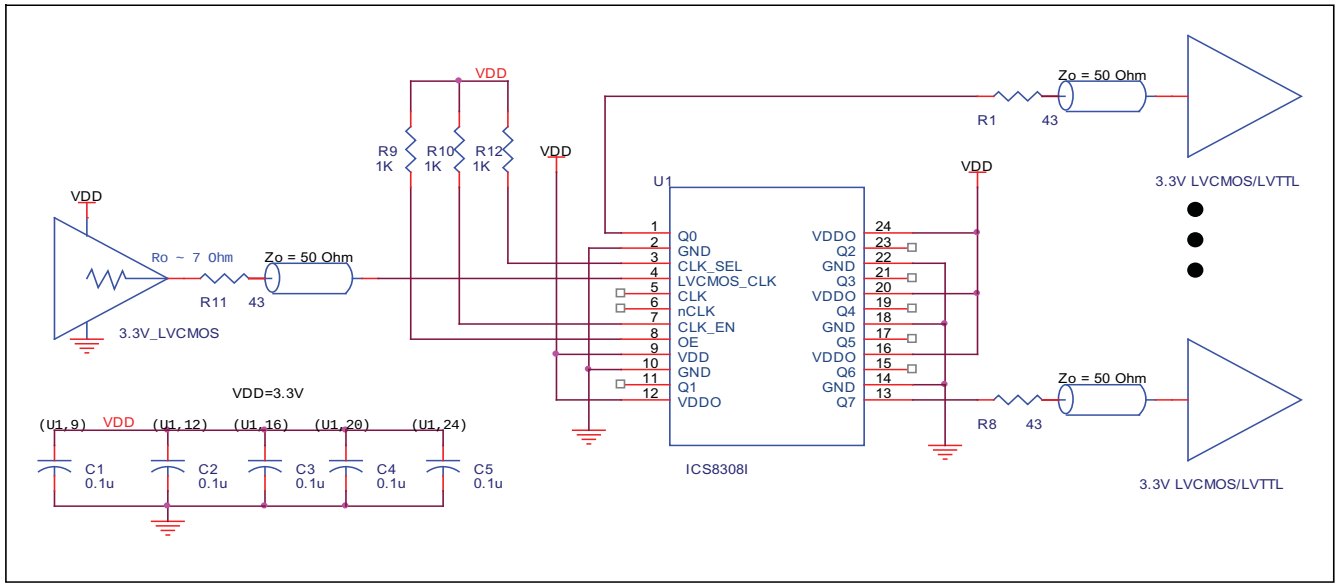


Figure 3. 8308I LVPECL Buffer Schematic Example

Recommendations for Unused Input and Output Pins

Inputs:

LVCMOS_CLK Input

For applications not requiring the use of an LVCMOS_CLK, it can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from the LVCMOS_CLK input to ground.

CLK/nCLK Inputs

For applications not requiring the use of the differential input, both CLK and nCLK can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from CLK to ground.

LVCMOS Control Pins

All control pins have internal pullups or pulldowns; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs:

LVCMOS Outputs

All unused LVCMOS outputs can be left floating. There should be no trace attached.

Power On Sequence

There is no power on sequence requirement for the V_{DD} and V_{DDO}. If the V_{DDO} is turned on before the V_{DD}, there will be unknown state at the outputs during initial condition when the V_{DDO} is on and V_{DD} is off.

Reliability Information

Table 6. θ_{JA} vs. Air Flow Table for 24 Lead TSSOP

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	**200**	**500**
Multi-Layer PCB, JEDEC Standard Test Boards	70°C/W	63°C/W	60°C/W

Transistor Count

The transistor count for 8308I is: 1040

Package Outline and Dimensions

Package Outline - G Suffix for 24 Lead TSSOP

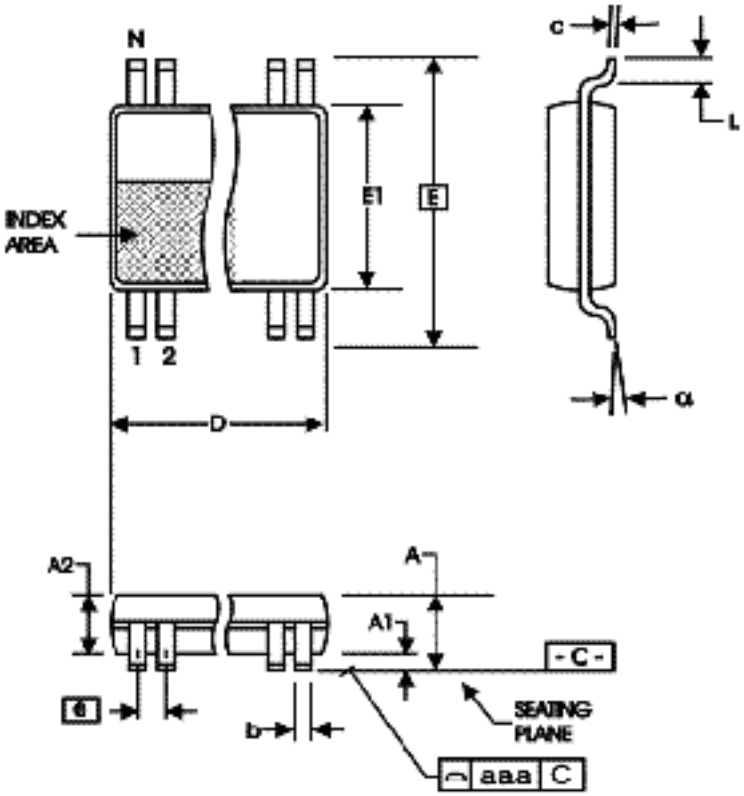


Table 7. Package Dimensions

SYMBOL	Millimeters	
	Minimum	Maximum
N	24	
A	--	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	7.70	7.90
E	6.40 BASIC	
E1	4.30	4.50
e	0.65 BASIC	
L	0.45	0.75
α	0°	8°
aaa	--	0.10

Reference Document: JEDEC Publication 95, MO-153

TABLE 8. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
8308AGILF	ICS8308AGILF	24 Lead “Lead-Free” TSSOP	tube	-40°C to 85°C
8308AGILFT	ICS8308AGILF	24 Lead “Lead-Free” TSSOP	tape & reel	-40°C to 85°C

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REVISION HISTORY SHEET				
Rev	**Table**	**Page**	**Description of Change**	**Date**
A		11	Added Schematic Layout	4/16/04
B	T4B T4E T5B	1 3 4 6 8	Features section - added mix supply voltage bullet. Added Mix Power Supply Table. Added Mix DC Characteristics Table. Added Mix AC Characteristics Table. Added Mix Output Load AC Test Circuit Diagram.	10/20/04
B	T8	14	Ordering Information Table - added “Lead-Free” part number.	1/12/05
B	T8	1 10 14	Corrected Block Diagram, added CLK_SEL. Added “Recommendations for Unused Input and Output Pins”. Ordering Information Table - added Lead-Free note.	7/25/05
B		1	Pin Assignment - corrected package information from 300-MIL to 173-MIL.	8/4/06
B	T3B	2	Added OE Select Function Table.	10/16/07
C	T4F T5A - T5C T8	5 5 -7 14	DC Characteristics - corrected V_{IH} min. from 2V to 1.7V; V_{IL} max. from 1.3V to 0.7V. AC Characteristics - added thermal note. Ordering Information Table - deleted ICS prefix from Part/Order Number column.	7/16/09
C	10 12		Updated Wiring the Differential Input to Accept Single-ended Levels application note. Added Power On Sequence application note.	3/23/11
C	T8	12 14	Recommended for Unusted I/O Pins - changed CLK Input: to LVCMOS_CLK. deleted lead-free note.	4/4/13
C		1	Removed ICS from the part numbers thoughout the datasheet. Removed reference to leaded devices in features section. Updated header and footer.	12/10/15

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