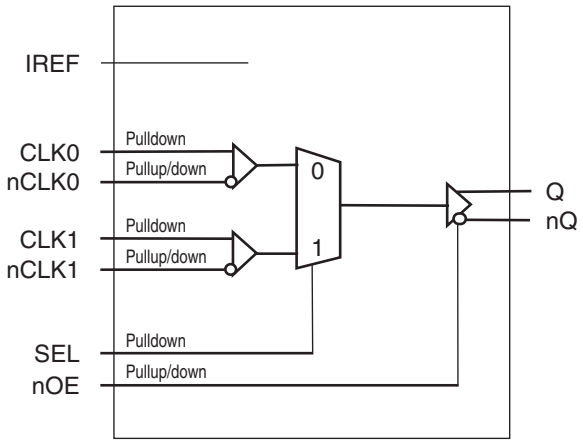
General Description

The ICS831721I is a high-performance, differential HCSL clock/data multiplexer and fanout buffer. The device is designed for the multiplexing of high-frequency clock and data signals. The device has two differential, selectable clock/data inputs. The selected input signal is output at one differential HCSL output. Each input pair accepts HCSL, LVDS, and LVPECL levels. The ICS831721I is characterized to operate from a 3.3V power supply. Guaranteed input, output-to-output and part-to-part skew characteristics make the ICS831721I ideal for those clock and data distribution applications demanding well-defined performance and repeatability. The ICS831721I supports the clock multiplexing and distribution of PCI Express Generation 1, 2 and 3 clock signals.

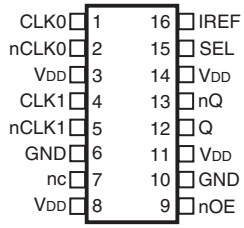
Features

- 2:1 differential clock/data multiplexer with fanout
- Two selectable, differential inputs
- Each differential input pair can accept the following levels: HCSL, LVHSTL, LVDS and LVPECL
- One differential HCSL output
- Maximum input/output clock frequency: 700MHz (maximum)
- Maximum input/output data rate: 1400Mb/s (NRZ)LVCMOS interface levels for all control inputs
- Input skew: 55ps (maximum)
- Part-to-part skew: 400ps (maximum)
- Full 3.3V supply voltage
- Available in lead-free (RoHS 6) 16 TSSOP package
- -40°C to 85°C ambient operating temperature

Block Diagram



Pin Assignment



ICS831721I
16-Lead TSSOP
4.4mm x 5.0mm x 0.925mm package body
G Package
Top View

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Pin Descriptions and Characteristics

Table 1. Pin Descriptions

Number	Name	Type		Description
1	CLK0	Input	Pulldown	Non-inverting clock/data input 0.
2	nCLK0	Input	Pullup/Pulldown	Inverting differential clock input 0. $V_{DD}/2$ default when left floating.
3, 8, 11, 14	V_{DD}	Power		Positive power supply.
4	CLK1	Input	Pulldown	Non-inverting clock/data input 1.
5	nCLK1	Input	Pullup/Pulldown	Inverting differential clock input 1. $V_{DD}/2$ default when left floating.
6, 10	GND	Power		Power supply ground.
7	nc	Unused		No connect.
9	nOE	Input	Pullup	Output enable. See Table 3A for function. LVCMOS/LVTTL interface levels.
12, 13	Q, nQ	Output		Differential output pair. HCSL interface levels.
15	SEL	Input	Pulldown	Input select. See Table 3B for function. LVCMOS/LVTTL interface levels.
16	IREF	Input		An external fixed precision resistor (475Ω) from this pin to ground provides a reference current used for the differential current-mode Q, nQ outputs.

NOTE: *Pullup* and *pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ
R_{PULLUP}	Input Pullup Resistor			51		kΩ

Function Tables

Table 3A. nOE Configuration Table

Input	
nOE	Operation
0	Output Q, nQ is enabled.
1 (default)	Output Q, nQ is in a high-impedance state.

NOTE: nOE is an asynchronous control.

Table 3B. SEL Configuration Table

Input	
SEL	Selected Input
0 (default)	CLK0, nCLK0
1	CLK1, nCLK1

NOTE: SEL is an asynchronous control.

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Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of the product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5V
Outputs, V_O	-0.5V to V_{DD} + 0.5V
Package Thermal Impedance, θ_{JA}	100.3°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, V_{DD} = 3.3V ± 0.3V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Positive Supply Voltage		3.0	3.3	3.6	V
I_{DD}	Power Supply Current				26	mA

Table 4B. LVCMOS/LVTTL Input DC Characteristics, V_{DD} = 3.3V ± 0.3V, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage			-0.3		0.8	V
I_{IH}	Input High Current	nOE	$V_{DD} = V_{IN}$ = 3.6V			5	µA
		SEL	$V_{DD} = V_{IN}$ = 3.6V			150	µA
I_{IL}	Input Low Current	nOE	V_{DD} = 3.6V, V_{IN} = 0V	-150			µA
		SEL	V_{DD} = 3.6V, V_{IN} = 0V	-5			µA

Table 4C. Differential DC Characteristics, V_{DD} = 3.3V ± 0.3V, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	CLK0, nCLK0, CLK1, nCLK1	$V_{DD} = V_{IN}$ = 3.6V			150	µA
I_{IL}	Input Low Current	CLK0, CLK1	V_{DD} = 3.6V, V_{IN} = 0V	-5			µA
		nCLK0, nCLK1	V_{DD} = 3.6V, V_{IN} = 0V	-150			µA
V_{PP}	Peak-to-Peak Voltage; NOTE 1			0.15		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			0.5		V_{DD} – 0.85	V

NOTE 1: V_{IL} should not be less than -0.3V.
NOTE 2: Common mode input voltage is defined as V_{IH}.

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Table 5. PCI Express Jitter Specifications, V_{DD} = 3.3V ± 0.3V, TA= -40°C to 85°C

Parameter	Symbol	Test Conditions	Minimum	Typical	Maximum	PCIe Industry Specification	Units
t_J (PCIe Gen 1)	Phase Jitter Peak-to-Peak NOTE 1, 4	f = 100MHz, Evaluation Band: 0Hz - Nyquist (clock frequency/2)		6.77	11.2	86	ps
$t_{REFCLK_HF_RMS}$ (PCIe Gen 2)	Phase Jitter RMS; NOTE 2, 4	f = 100MHz, High Band:1.5Hz - Nyquist (clock frequency/2)		0.59	1.01	3.1	ps
$t_{REFCLK_LF_RMS}$ (PCIe Gen 2)	Phase Jitter RMS; NOTE 2, 4	f = 100MHz, Low Band: 10kHz - 1.5Hz		0.03	0.07	3.0	ps
t_{REFCLK_RMS} (PCIe Gen 3)	Phase Jitter RMS; NOTE 3, 4	f = 100MHz, Evaluation Band: 0Hz - Nyquist (clock frequency/2)		0.112	0.185	0.8	ps

NOTE: The source generator used in the PCI Express Jitter measurements is Stanford Research Systems CG635 2.0GHz Synthesized Clock Generator.
NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions. For additional information, refer to the *PCI Express Application Note section* in the datasheet.
NOTE 1: Peak-to-Peak jitter after applying system transfer function for the Common Clock Architecture. Maximum limit for PCI Express Gen 1 is 86ps peak-to-peak for a sample size of 10^6 clock periods.
NOTE 2: RMS jitter after applying the two evaluation bands to the two transfer functions defined in the Common Clock Architecture and reporting the worst case results for each evaluation band. Maximum limit for PCI Express Generation 2 is 3.1ps RMS for $t_{REFCLK_HF_RMS}$ (High Band) and 3.0ps RMS for $t_{REFCLK_LF_RMS}$ (Low Band).
NOTE 3: RMS jitter after applying system transfer function for the common clock architecture. This specification is based on the *PCI Express Base Specification Revision 0.7, October 2009* and is subject to change pending the final release version of the specification.
NOTE 4: This parameter is guaranteed by characterization. Not tested in production.

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AC Electrical Characteristics

Table 6. HCSL AC Characteristics, V_{DD} = 3.3V ± 0.3V, T_A = -40°C to 85°C

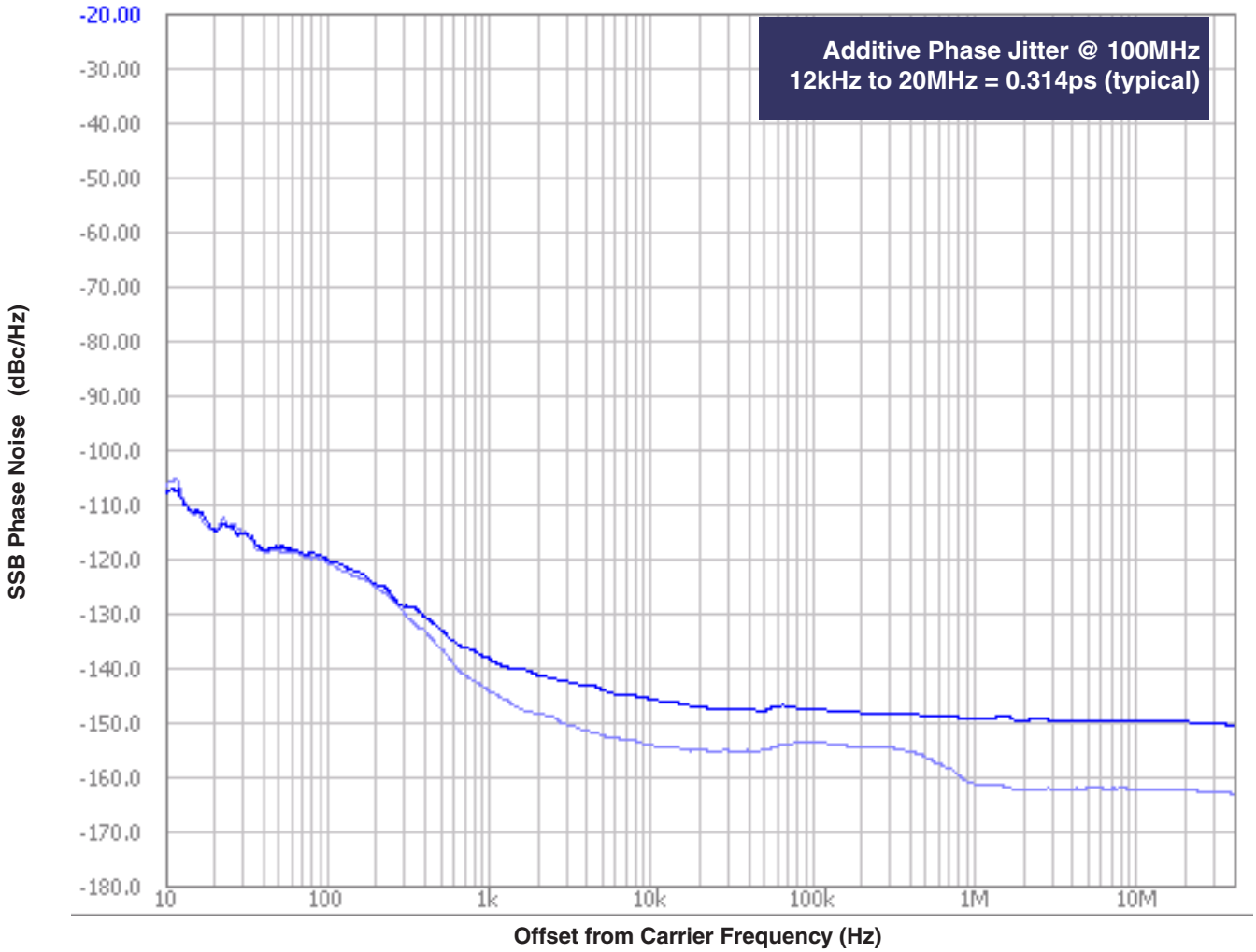
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency				700	MHz
t_{jit}	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Plot	100MHz, Integration Range: 12kHz – 20MHz		0.314	0.337	ps
t_{PD}	Propagation Delay, NOTE 1	Any CLKx, nCLKx to Q, nQ	2		2.4	ns
tsk(i)	Input Skew; NOTE 2				55	ps
tsk(pp)	Part-to-Part Skew; NOTE 3, 4				400	ps
Edge Rate	Rise/Fall Edge Rate; NOTE 5, 6		0.6		4.0	V/ns
V_{RB}	Ringback Voltage; NOTE 5, 7		-100		100	V
V_{MAX}	Absolute Max Output Voltage; NOTE 8, 9				1150	mV
V_{MIN}	Absolute Min Output Voltage; NOTE 8, 10		-300			mV
V_{CROSS}	Absolute Crossing Voltage; NOTE 8, 11, 12		250		550	mV
ΔV_{CROSS}	Total Variation of V_{CROSS} over all edges; NOTE 8, 11, 13				140	mV
odc	Output Duty Cycle; NOTE 14	$f_{OUT} \leq$ 312.5MHz	46		54	%
		$f_{OUT} >$ 312.5MHz	43		57	%
MUX_{ISOL}	Mux Isolation; NOTE 15	f = 100MHz		80		dB

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE 1: Measured from the differential input cross point to the differential output crossing point.
NOTE 2: Defined as skew between input paths on the same device, using the same input signal levels, measured at one specific output at the differential cross points.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 4: Defined as skew between outputs on different devices operating at the same supply voltage and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.
NOTE 5: Measurement taken from differential waveform.
NOTE 6: Measurement from -150mV to +150mV on the differential waveform (derived from Q minus nQ). The signal must be monotonic through the measurement region for rise and fall time. The 300mV measurement window is centered on the differential zero crossing.
NOTE 7: T_{STABLE} is the time the differential clock must maintain a minimum ±150mV differential voltage after rising/falling edges before it is allowed to drop back into the V_{RB} ±100 differential range. See Parameter Measurement Information Section.
NOTE 8: Measurement taken from single-ended waveform.
NOTE 9: Defined as the maximum instantaneous voltage including overshoot. See Parameter Measurement Information Section.
NOTE 10: Defined as the minimum instantaneous voltage including undershoot. See Parameter Measurement Information Section.
NOTE 11: Measured at crossing point where the instantaneous voltage value of the rising edge of Qx equals the falling edge of nQx. See Parameter Measurement Information Section
NOTE 12: Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement. See Parameter Measurement Information Section.
NOTE 13: Defined as the total variation of all crossing voltage of rising Q and falling nQ. This is the maximum allowed variance in the V_{CROSS} for any particular system. See Parameter Measurement Information Section.
NOTE 14: Input duty cycle must be 50%.
NOTE 15: Q, nQ output measured differentially. See MUX Isolation Diagram in Parameter Measurement Information Section.

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Additive Phase Jitter

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the ***dBc Phase Noise.*** This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a ***dBc*** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.

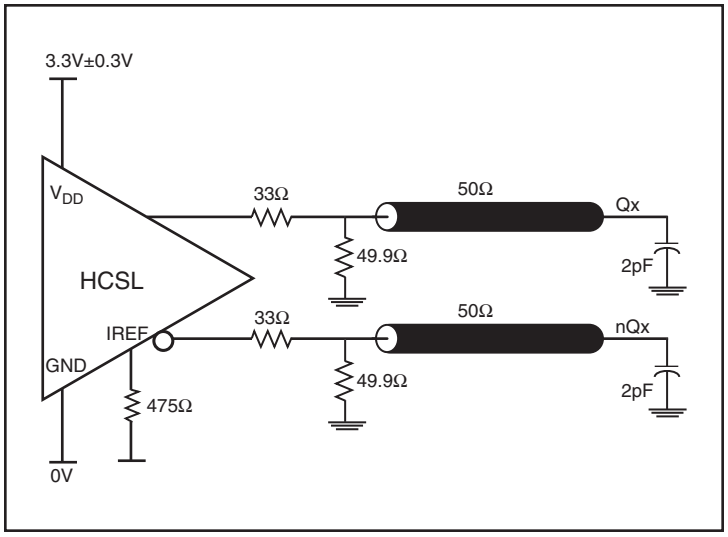


As with most timing specifications, phase noise measurements has issues relating to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This is illustrated above. The device meets the noise floor of what is shown, but can actually be lower. The phase noise is dependent on the input source and measurement equipment.

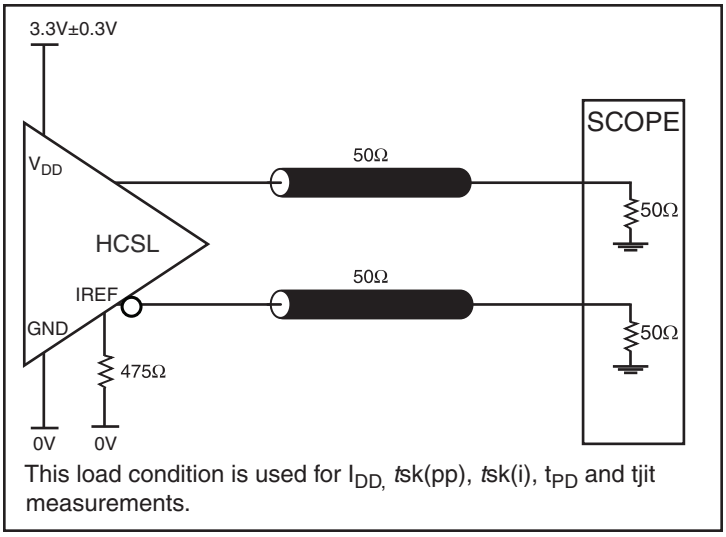
The source generator is the Rhode & Schwarz SMA 100A Signal Generator 9kHz – 6GHz. Phase noise is measured with the Agilent E5052A Signal source Analyzer.

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Parameter Measurement Information

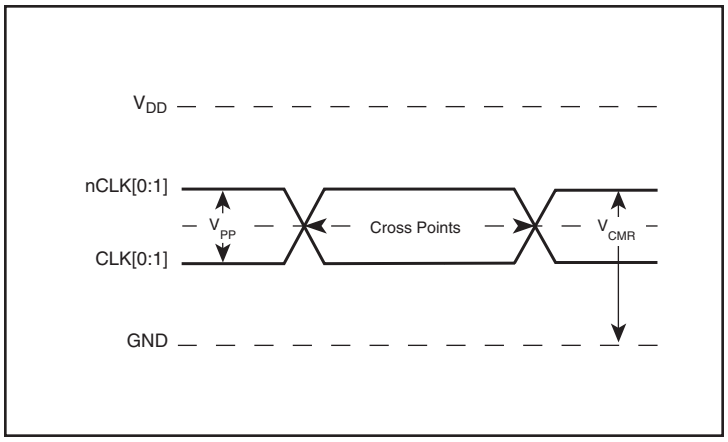


3.3V HCSL Output Load AC Test Circuit

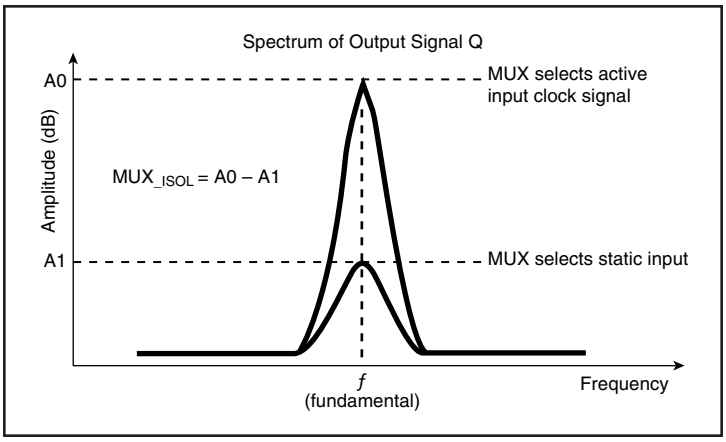


This load condition is used for I_{DD}, *t*sk(pp), *t*sk(i), t_{PD} and tjit measurements.

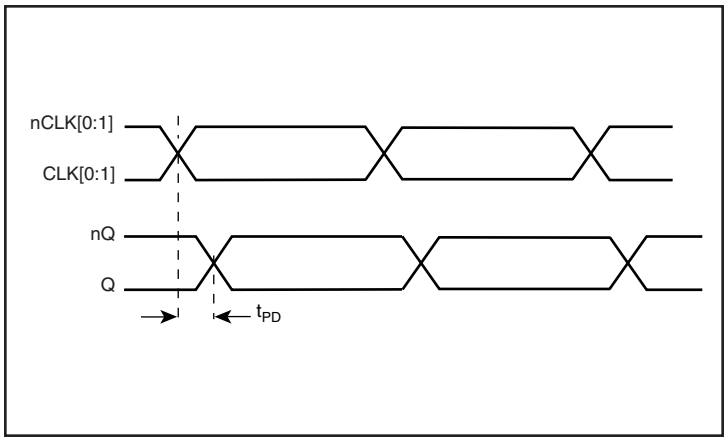
3.3V HCSL Output Load AC Test Circuit



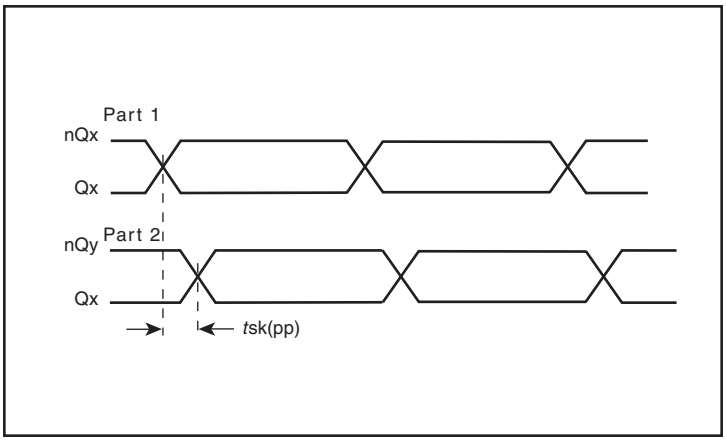
Differential Input Level



MUX_ISOLATION



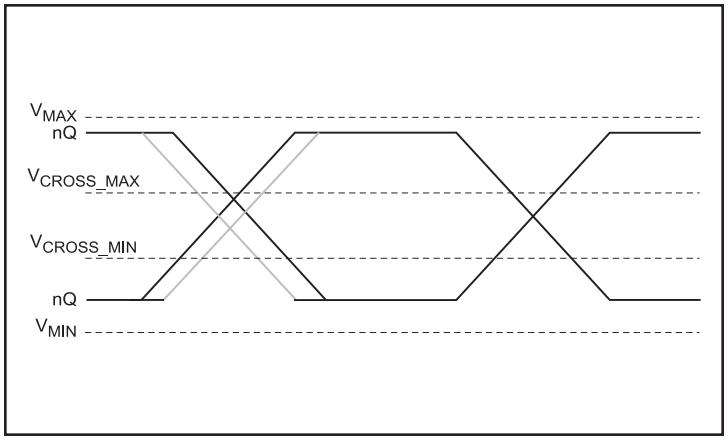
Propagation Delay



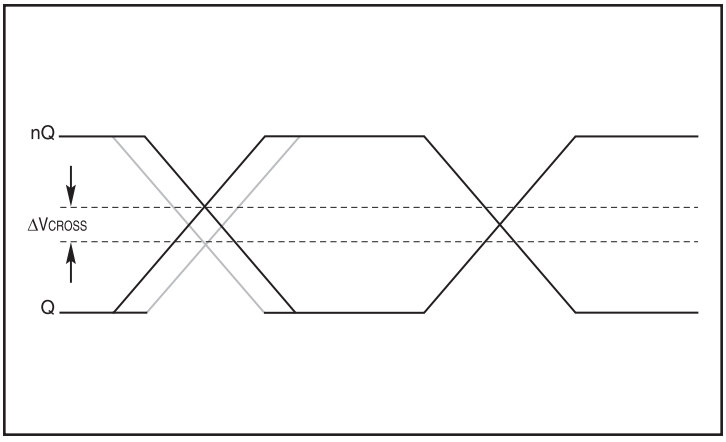
Part-to-Part Skew

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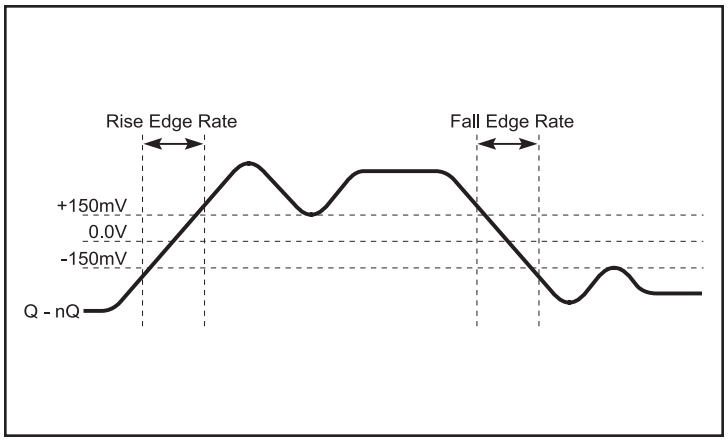
Parameter Measurement Information, continued



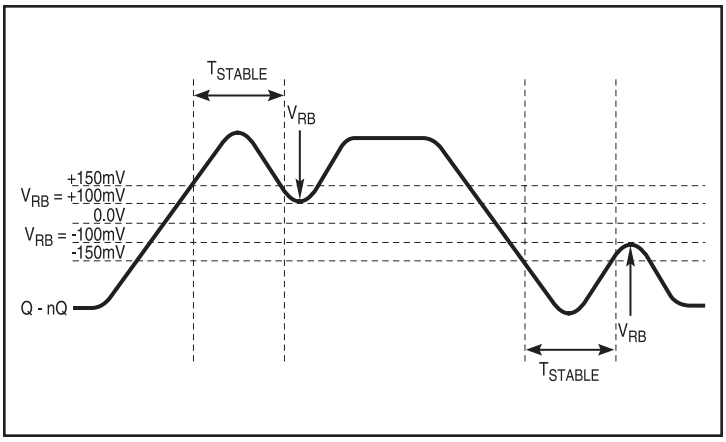
Single-ended Measurement Points for Absolute Cross Point/Swing



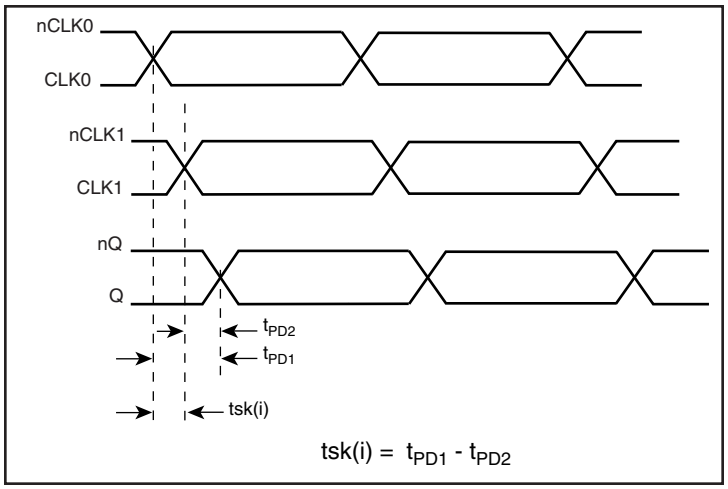
Single-ended Measurement Points for Delta Cross Point



Differential Measurement Points for Rise/Fall Edge Rate



Differential Measurement Points for Ringback



Input Skew

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Applications Information

Recommendations for Unused Input Pins

Inputs:

LVCMOS Control Pins

All control pins have internal pullups and pulldowns; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

CLK/nCLK Inputs

For applications not requiring the use of the differential input, both CLK and nCLK can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from CLK to ground.

Wiring the Differential Input to Accept Single-Ended Levels

Figure 1 shows how a differential input can be wired to accept single ended levels. The reference voltage $V_1 = V_{DD}/2$ is generated by the bias resistors R1 and R2. The bypass capacitor (C1) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of R1 and R2 might need to be adjusted to position the V_1 in the center of the input voltage swing. For example, if the input clock swing is 2.5V and V_{DD} = 3.3V, R1 and R2 value should be adjusted to set V_1 at 1.25V. The values below are for when both the single ended swing and V_{DD} are at the same voltage. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways. First, R3 and R4 in parallel should equal the transmission line impedance. For most 50Ω applications, R3 and R4 can be 100Ω. The values of the resistors can be increased to reduce the loading for slower and weaker LVCMOS driver. When using single-ended signaling, the noise rejection benefits of differential signaling are reduced. Even though the differential input can handle full rail LVCMOS signaling, it is recommended that the amplitude be reduced. The datasheet specifies a lower differential amplitude, however this only applies to differential signals. For single-ended applications, the swing can be larger, however V_{IL} cannot be less than -0.3V and V_{IH} cannot be more than V_{DD} + 0.3V. Though some of the recommended components might not be used, the pads should be placed in the layout. They can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a differential signal.

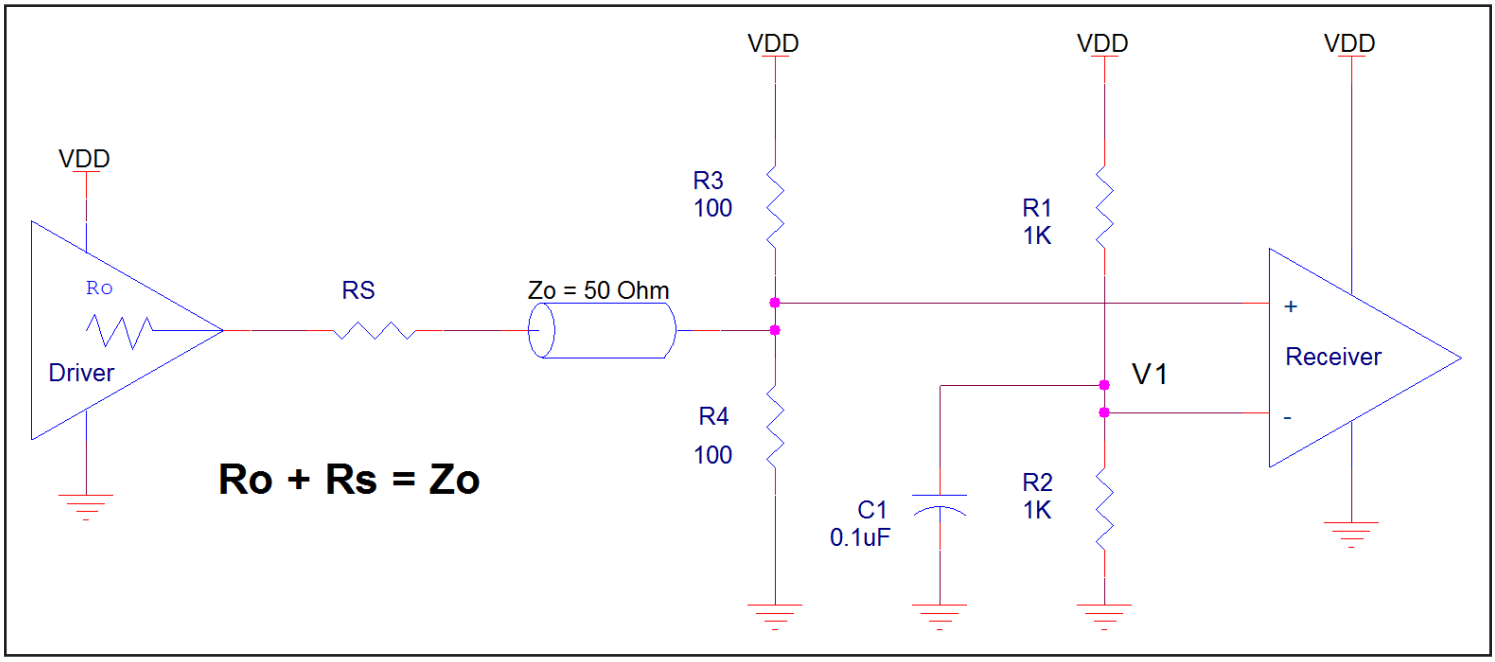


Figure 1. Recommended Schematic for Wiring a Differential Input to Accept Single-ended Levels

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PCI Express Application Note

PCI Express jitter analysis methodology models the system response to reference clock jitter. The block diagram below shows the most frequently used *Common Clock Architecture* in which a copy of the reference clock is provided to both ends of the PCI Express Link.

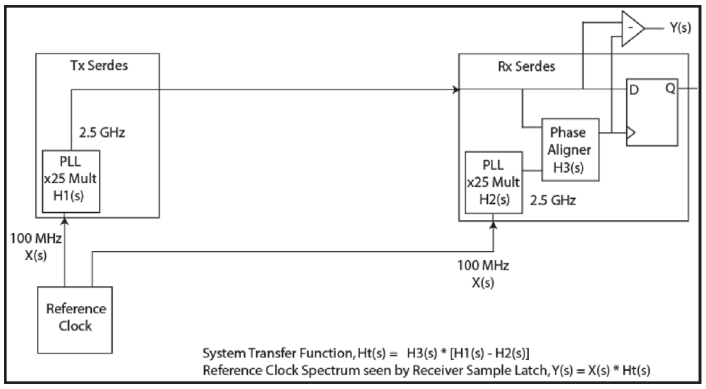
In the jitter analysis, the transmit (Tx) and receive (Rx) serdes PLLs are modeled as well as the phase interpolator in the receiver. These transfer functions are called H1, H2, and H3 respectively. The overall system transfer function at the receiver is:

$$Ht(s) = H3(s) \times [H1(s) - H2(s)]$$

The jitter spectrum seen by the receiver is the result of applying this system transfer function to the clock spectrum X(s) and is:

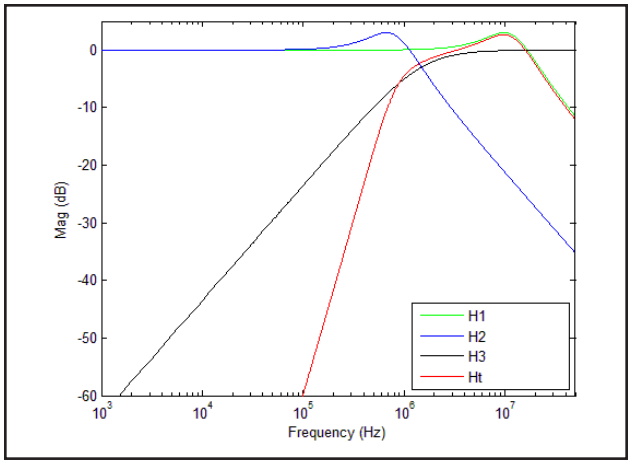
$$Y(s) = X(s) \times H3(s) \times [H1(s) - H2(s)]$$

In order to generate time domain jitter numbers, an inverse Fourier Transform is performed on X(s)*H3(s) * [H1(s) - H2(s)].



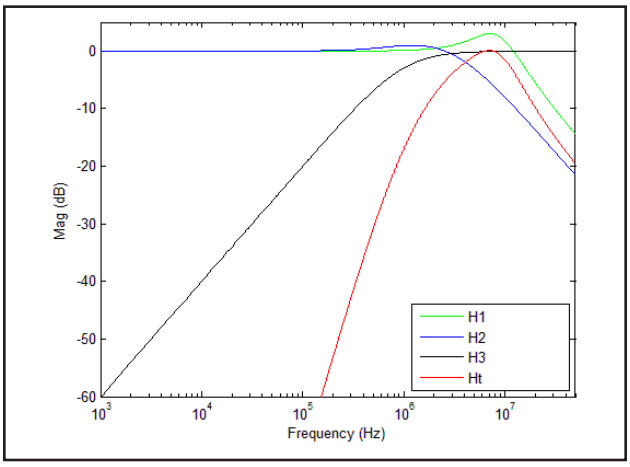
PCI Express Common Clock Architecture

For **PCI Express Gen 1**, one transfer function is defined and the evaluation is performed over the entire spectrum: DC to Nyquist (e.g for a 100MHz reference clock: 0Hz – 50MHz) and the jitter result is reported in peak-peak.

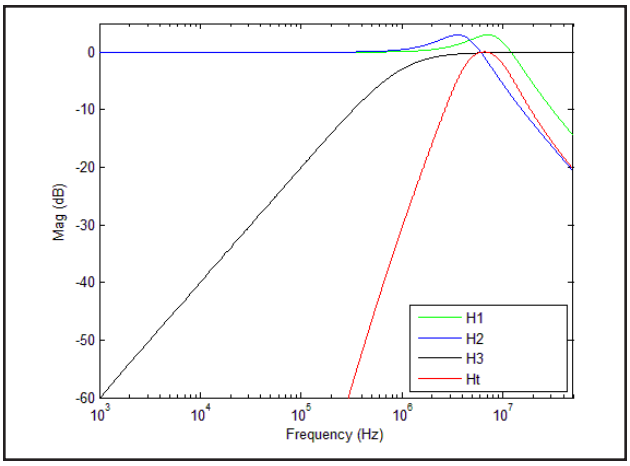


PCIe Gen 1 Magnitude of Transfer Function

For **PCI Express Gen 2**, two transfer functions are defined with 2 evaluation ranges and the final jitter number is reported in rms. The two evaluation ranges for PCI Express Gen 2 are 10kHz – 1.5MHz (Low Band) and 1.5MHz – Nyquist (High Band). The plots show the individual transfer functions as well as the overall transfer function Ht.

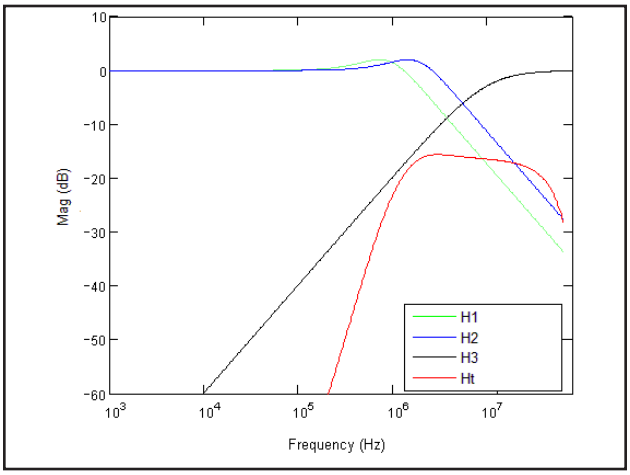


PCIe Gen 2A Magnitude of Transfer Function



PCIe Gen 2B Magnitude of Transfer Function

For **PCI Express Gen 3**, one transfer function is defined and the evaluation is performed over the entire spectrum. The transfer function parameters are different from Gen 1 and the jitter result is reported in RMS.



PCIe Gen 3 Magnitude of Transfer Function

For a more thorough overview of PCI Express jitter analysis methodology, please refer to IDT Application Note *PCI Express Reference Clock Requirements.*

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Recommended Termination

Figure 2A is the recommended source termination for applications where the driver and receiver will be on a separate PCBs. This termination is the standard for PCI Express™ and HCSL output types. All traces should be 50Ω impedance single-ended or 100Ω differential.

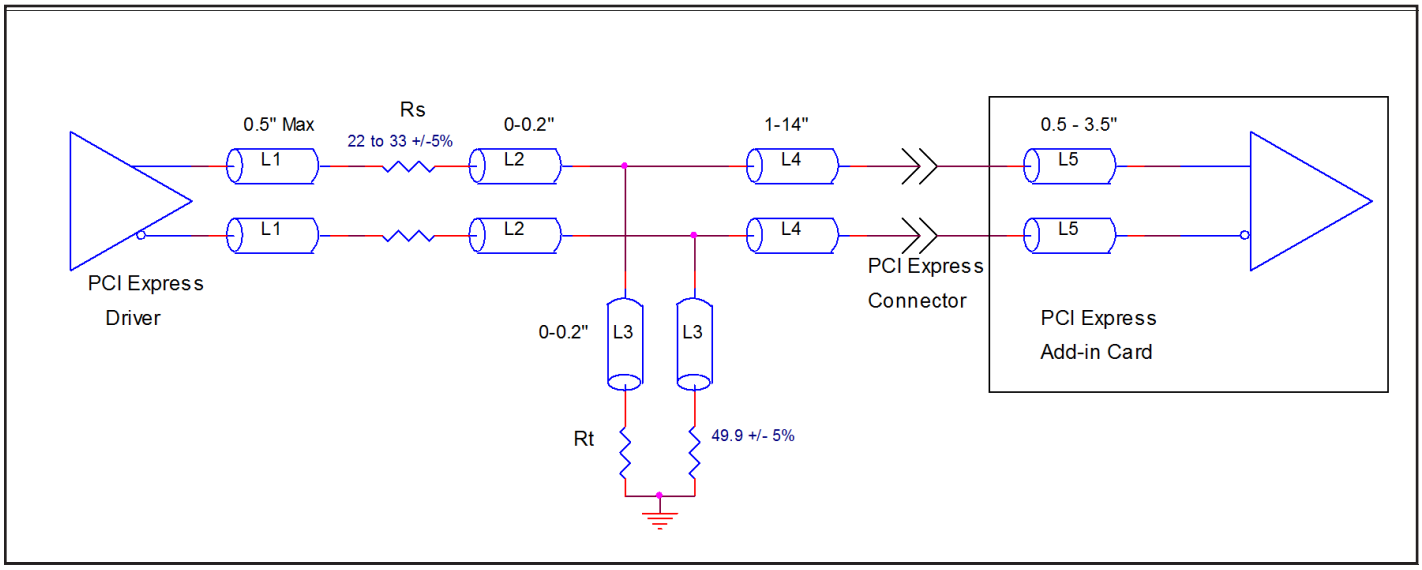


Figure 2A. Recommended Source Termination (where the driver and receiver will be on separate PCBs)

Figure 2B is the recommended termination for applications where a point-to-point connection can be used. A point-to-point connection contains both the driver and the receiver on the same PCB. With a matched termination at the receiver, transmission-line reflections will be minimized. In addition, a series resistor (Rs) at the driver offers flexibility and can help dampen unwanted reflections. The optional resistor can range from 0Ω to 33Ω. All traces should be 50Ω impedance single-ended or 100Ω differential.

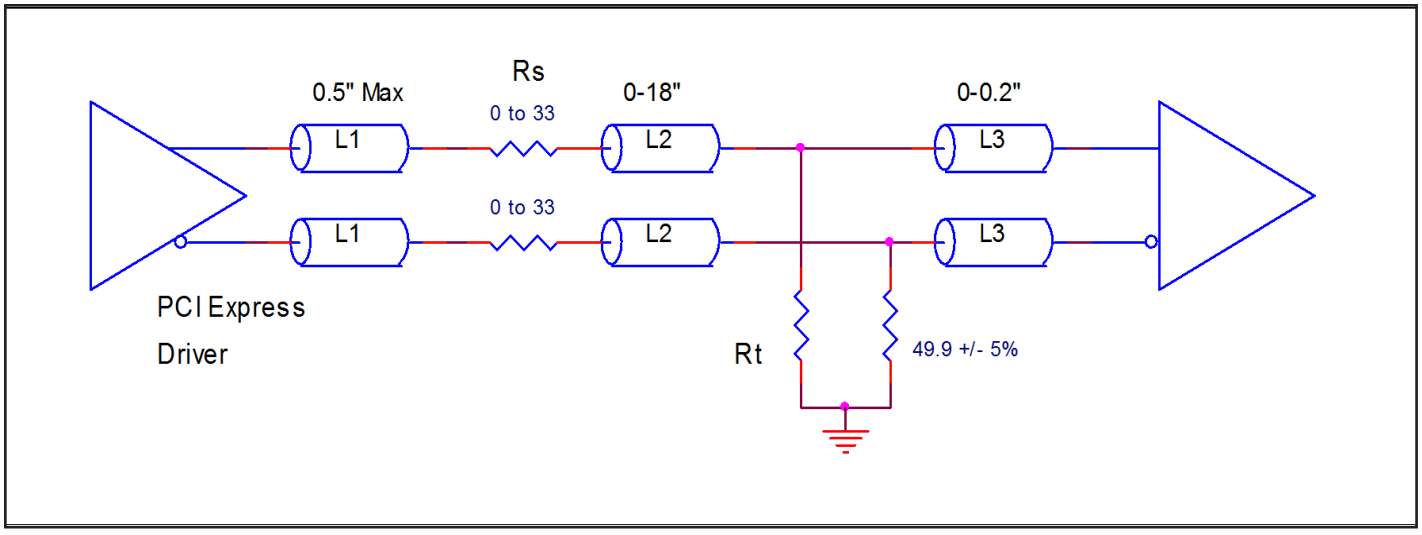


Figure 2B. Recommended Termination (where a point-to-point connection can be used)

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Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, HCSL and other differential signals. Both signals must meet the V_{PP} and V_{CMR} input requirements. *Figures 3A to 3F* show interface examples for the CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example, in Figure 3A, the input termination applies for IDT open emitter LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

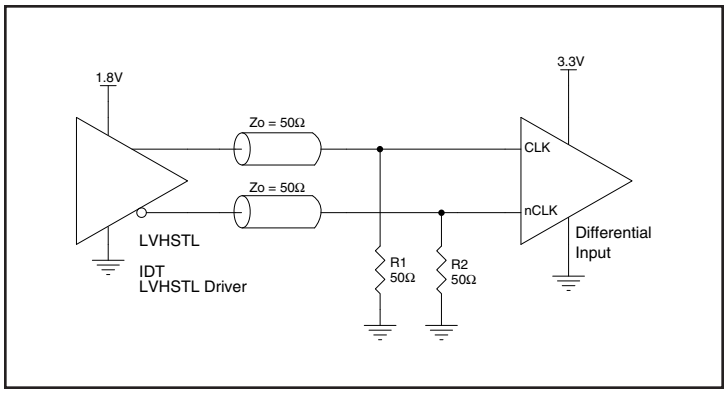


Figure 3A. CLK/nCLK Input Driven by an IDT Open Emitter LVHSTL Driver

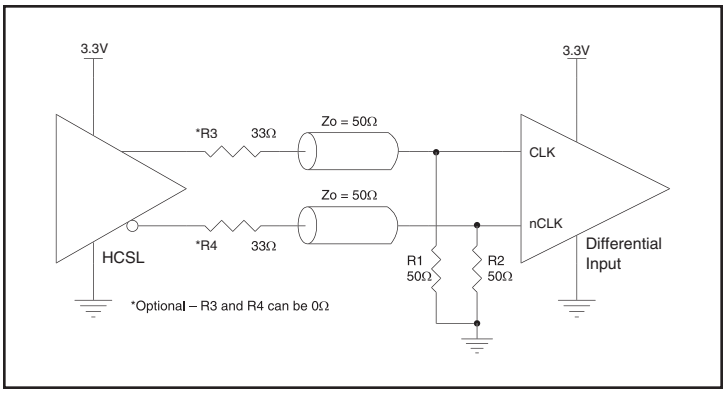


Figure 3B. CLK/nCLK Input Driven by a 3.3V HCSL Driver

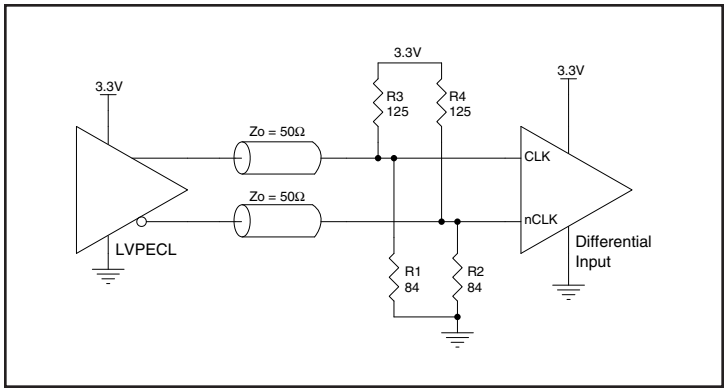


Figure 3C. CLK/nCLK Input Driven by a 3.3V LVPECL Driver

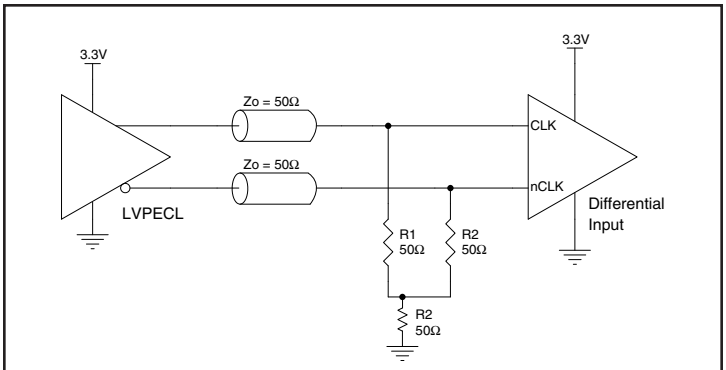


Figure 3D. CLK/nCLK Input Driven by a 3.3V LVPECL Driver

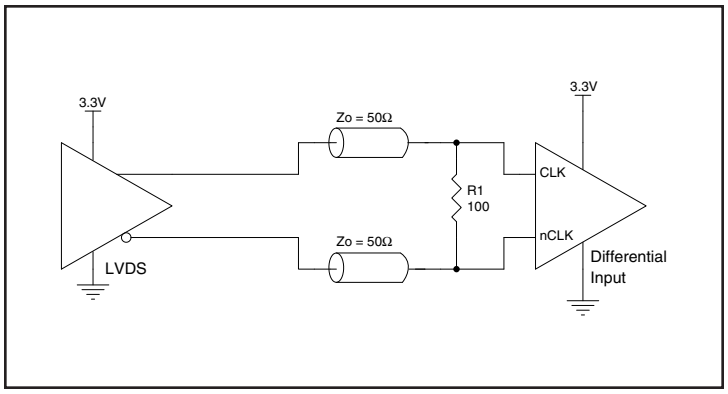


Figure 3E. CLK/nCLK Input Driven by a 3.3V LVDS Driver

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Power Considerations

This section provides information on power dissipation and junction temperature for the ICS831752I.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS831752I is the sum of the core power plus the analog power plus the power dissipated in the load(s). The following is the power dissipation for V_{DD} = 3.3V + 0.3V = 3.6V, which gives worst case results.

- Power $(core)_{MAX} = V_{DD_MAX} * I_{DD_MAX}$ = 3.6V * 26mA = **93.6mW**
- Power $(outputs)_{MAX}$ = **46.8mW/Loaded Output Pair**

Total Power$_{_MAX}$ (3.63V, with all outputs switching) = 93.6mW + 46.8mW = **140.4mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 100.3°C/W per Table 7 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.140W * 100.3°C/W = 99°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 7. Thermal Resistance θ_{JA} for 16-Lead TSSOP, Forced Convection

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	100.3°C/W	96.0°C/W	93.9°C/W

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The purpose of this section is to calculate power dissipation on the IC per HCSL output pair.

HCSL output driver circuit and termination are shown in *Figure 4.*

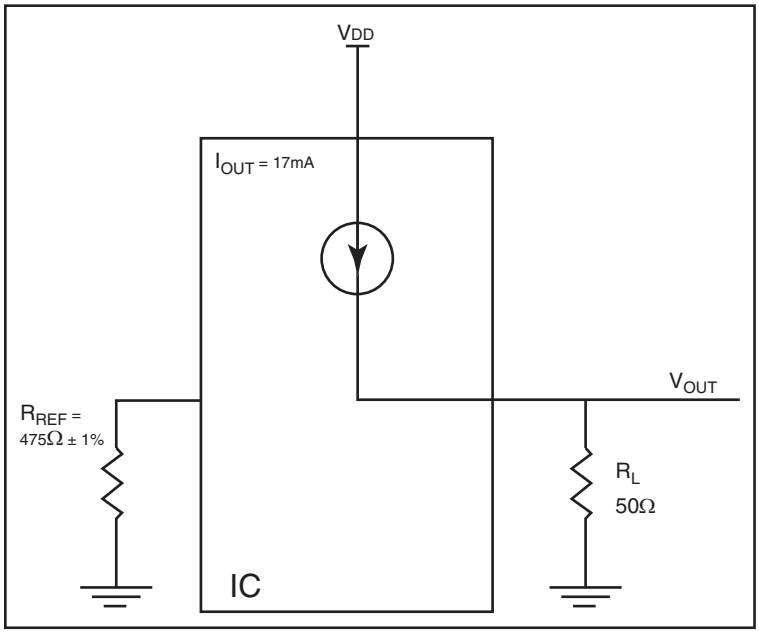


Figure 4. HCSL Driver Circuit and Termination

HCSL is a current steering output which sources a maximum of 17mA of current per output. To calculate worst case on-chip power dissipation, use the following equations which assume a 50Ω load to ground.

The highest power dissipation occurs when V_{DD_MAX}.

Power = $(V_{DD_MAX} - V_{OUT}) * I_{OUT}$,
since $V_{OUT} - I_{OUT} * R_L$

= $(V_{DD_MA} - I_{OUT} * R_L) * I_{OUT}$

= (3.6V – 17mA * 50Ω) * 17mA

Total Power Dissipation per output pair = **46.8mW**

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Package Outline and Package Dimensions

Table 8. θ_{JA} vs. Air Flow Table for a 16-Lead TSSOP

θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	100.3°C/W	96.0°C/W	93.9°C/W

Transistor Count

The transistor count for ICS831721I is: 632

Package Outline and Package Dimensions

Package Outline - G Suffix for 16-Lead TSSOP

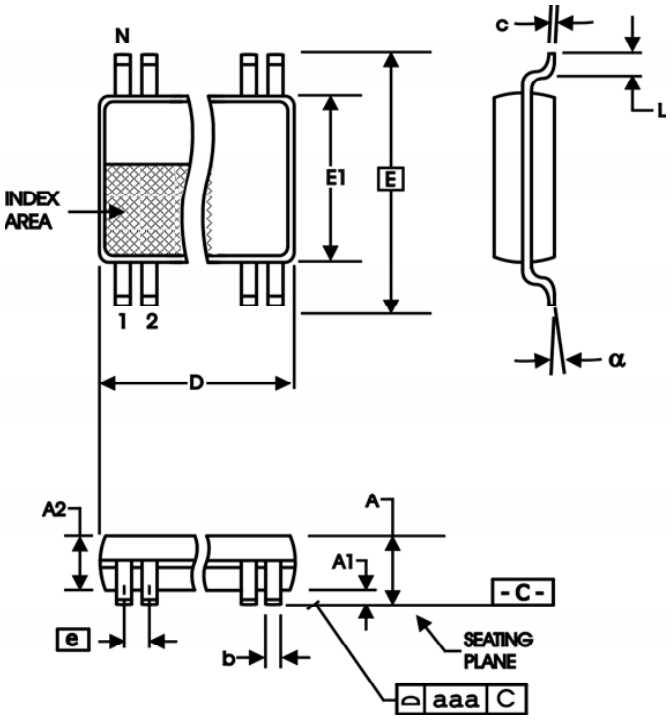


Table 9. Package Dimensions for 16-Lead TSSOP

All Dimensions in Millimeters		
Symbol	**Minimum**	**Maximum**
N	16	
A		1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	4.90	5.10
E	6.40 Basic	
E1	4.30	4.50
e	0.65 Basic	
L	0.45	0.75
α	0°	8°
aaa		0.10

Reference Document: JEDEC Publication 95, MO-153

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Ordering Information

Table 10. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
831721AGILF	31721AIL	Lead-Free, 16-Lead TSSOP	Tube	-40°C to 85°C
831721AGILFT	31721AIL	Lead-Free, 16-Lead TSSOP	Tape & Reel	-40°C to 85°C

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Revision History Sheet

Rev	Table	Page	Description of Change	Date
A	T2	2 9	Changed Parameter: ‘Input Pulldown Resistor’ to ‘Input Pullup Resistor’. Updated the ‘Wiring the Differential Input to Accept Single-Ended Levels’ Note.	2/3/2014

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