Low Skew, 1-to-18 LVPECL-TO-LVCMOS / LVTTL Fanout Buffer

83940D

DATASHEET

General Description

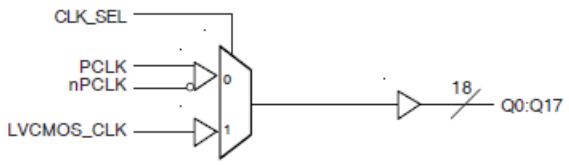
The 83940D is a low skew, 1-to-18 LVPECL-to-LVCMOS/LVTTL Fanout Buffer. The 83940D has two selectable clock inputs. The PCLK, nPCLK pair can accept LVPECL, CML, or SSTL input levels. The LVCMOS_CLK can accept LVCMOS or LVTTL input levels. The low impedance LVCMOS/LVTTL outputs are designed to drive 50Ω series or parallel terminated transmission lines.

The 83940D is characterized at full 3.3V and 2.5V or mixed3.3V core, 2.5V output operating supply modes. Guaranteed output and part-to-part skew characteristics make the 83940D ideal for those clock distribution applications demanding well defined performance and repeatability.

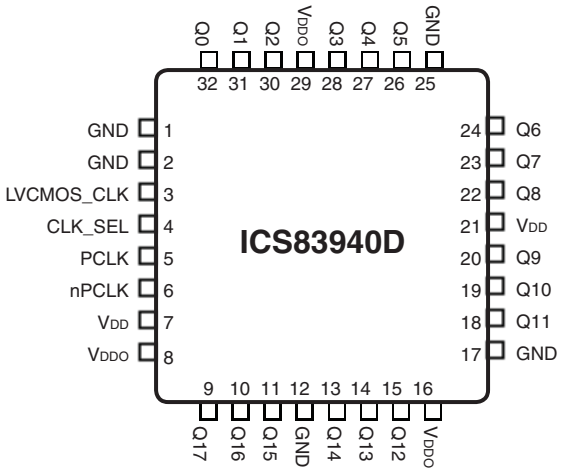
Features

- 18 LVCMOS/LVTTL outputs
- Selectable LVCMOS_CLK or LVPECL clock inputs
- PCLK, nPCLK supports the following input types: LVPECL, CML, SSTL
- LVCMOS_CLK accepts the following input levels: LVCMOS or LVTTL
- Maximum output frequency: 250MHz
- Output skew: 150ps (maximum)
- Part to part skew: 750ps (maximum)
- Additive phase jitter, RMS: < 0.03ps (typical)
- Full 3.3V and 2.5V or mixed 3.3V core, 2.5V output supply modes
- 0°C to 70°C ambient operating temperature
- Lead-Free package available

Block Diagram



Pin Assignment



32-Lead LQFP
7mm x 7mm x 1.4mm package body
Y Pacakge
Top View

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Table 1. Pin Descriptions

Number	Name	Type		Description
1, 2, 12, 17, 25	GND	Power		Power supply ground.
3	LVCMOS_CLK	Input	Pulldown	Clock input. LVCMOS / LVTTL interface levels.
4	CLK_SEL	Input	Pulldown	Clock select input. Selects LVCMOS / LVTTL clock input when HIGH. Selects PCLK, nPCLK inputs when LOW. LVCMOS / LVTTL interface levels.
5	PCLK	Input	Pulldown	Non-inverting differential LVPECL clock input.
6	nPCLK	Input	Pullup/ Pulldown	Inverting differential LVPECL clock input. $V_{DD}/2$ default when left floating.
7, 21	V_{DD}	Power		Core supply pins.
8, 16, 29	V_{DDO}	Power		Output supply pins.
9, 10, 11, 13, 14, 15, 18, 19, 20, 22, 23, 24, 26, 27, 28, 30, 31, 32	Q17, Q16, Q15, Q14, Q13, Q12, Q11, Q10, Q9, Q8, Q7, Q6, Q5, Q4, Q3, Q2, Q1, Q0	Output		Clock outputs. LVCMOS / LVTTL interface levels.

NOTE: *Pullup and Pulldown* refers to internal input resistors. See Table 2, Pin Characteristics, for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
C_{PD}	Power Dissipation Capacitance (per output)			6		pF
R_{PULLup}	Input Pullup Resistor			51		KΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		KΩ
R_{OUT}	Output Impedance		18		28	Ω

Table 3A. Clock Select Function Table

Control Input	Clock	
CLK_SEL	PCLK, nPCLK	LVCMOS_CLK
0	Selected	De-selected
1	De-selected	Selected

Table 3B. Clock Input Function Table

Inputs				Outputs	Input to Output Mode	Polarity
CLK_SEL	LVCMOS_CLK	PCLK	nPCLK	Q0:Q17		
0	—	0	1	LOW	Differential to Single Ended	Non Inverting
0	—	1	0	HIGH	Differential to Single Ended	Non Inverting
0	—	0	Biased; NOTE 1	LOW	Single Ended to Single Ended	Non Inverting
0	—	1	Biased; NOTE 1	HIGH	Single Ended to Single Ended	Non Inverting
0	—	Biased; NOTE 1	0	HIGH	Single Ended to Single Ended	Inverting
0	—	Biased; NOTE 1	1	LOW	Single Ended to Single Ended	Inverting
1	0	—	—	LOW	Single Ended to Single Ended	Non Inverting
1	1	—	—	HIGH	Single Ended to Single Ended	Non Inverting

NOTE 1: Please refer to the Application Information section, “Wiring the Differential Input to Accept Single Ended Levels”.

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Absolute Maximum Ratings

Supply Voltage, V_{DD}	3.6V
Inputs, V_I	-0.3V to V_{DD} + 0.3V
Outputs, V_O	-0.3V to V_{DDO} + 0.3V
Input Current, I_{IN}	±20mA
Storage Temperature, T_{STG}	-40°C to 125°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

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TABLE 4A. DC CHARACTERISTICS, $V_{DD} = V_{DDO} = 3.3V \pm 5\%$, $T_A = 0°$ TO 70°

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	LVCMOS_CLK		2.4		V_{DD}	V
V_{IL}	Input Low Voltage	LVCMOS_CLK				0.8	V
V_{PP}	Peak-to-Peak Input Voltage	PCLK, nPCLK		500		1000	mV
V_{CMR}	Input Common Mode Voltage; NOTE 1, 2	PCLK, nPCLK		V_{DD} - 1.4		V_{DD} - 0.6	V
I_{IN}	Input Current					±200	µA
V_{OH}	Output High Voltage		I_{OH} = -20mA	2.4			V
V_{OL}	Output Low Voltage		I_{OL} = 20mA			0.5	V
I_{DD}	Core Supply Current					25	mA

NOTE 1: For single ended applications, the maximum input voltage for PCLK, nPCLK is V_{DD} + 0.3V.
NOTE 2: Common mode voltage is defined as V_{IH}.

TABLE 5A. AC CHARACTERISTICS, $V_{DD} = V_{DDO} = 3.3V \pm 5\%$, $T_A = 0°$ TO 70°

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency					250	MHz
t_{pLH}	Propagation Delay	PCLK, nPCLK; NOTE 1, 5	f ≤ 150MHz	1.6		3.0	ns
		LVCMOS_CLK; NOTE 2, 5	f ≤ 150MHz	1.8		3.0	ns
t_{pLH}	Propagation Delay	PCLK, nPCLK; NOTE 1, 5	f > 150MHz	1.6		3.3	ns
		LVCMOS_CLK; NOTE 2, 5	f > 150MHz	1.8		3.2	ns
tsk(o)	Output Skew; NOTE 3, 5	PCLK, nPCLK	Measured on rising edge @V_{DDO}/2			150	ps
		LVCMOS_CLK				150	ps
tsk(pp)	Part-to-Part Skew; NOTE 6	PCLK, nPCLK	f ≤ 150MHz			1.4	ns
		LVCMOS_CLK	f ≤ 150MHz			1.2	ns
tsk(pp)	Part-to-Part Skew; NOTE 6	PCLK, nPCLK	f > 150MHz			1.7	ns
		LVCMOS_CLK	f > 150MHz			1.4	ns
tsk(pp)	Part-to-Part Skew; NOTE 4, 5	PCLK, nPCLK	Measured on rising edge @V_{DDO}/2			850	ps
		LVCMOS_CLK				750	ps
tjit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter section, NOTE 7				0.03		ps
t_R / t_F	Output Rise/Fall Time		0.5 to 2.4V	0.3		1.1	ns
odc	Output Duty Cycle		f < 134MHz	45	50	55	%
			134MHz ≤ f ≤ 250MHz	40	50	60	%

All parameters measured at 200MHz unless noted otherwise.
NOTE 1: Measured from the differential input crossing point to the output V_{DDO}/2.
NOTE 2: Measured from V_{DD}/2 to V_{DDO}/2.
NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at V_{DDO}/2.
NOTE 4: Defined as skew between outputs on different devices operating at the same supply voltages, same temperature, and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at V_{DDO}/2.
NOTE 5: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 6: Defined as skew between outputs on different devices, across temperature and voltage ranges, and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at V_{DDO}/2.
NOTE 7: Driving only one input clock.

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TABLE 4B. DC CHARACTERISTICS, V_{DD} = 3.3V ± 5%, V_{DDO} = 2.5V ± 5%, TA = 0° TO 70°

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	LVCMOS_CLK		2.4		V_{DD}	V
V_{IL}	Input Low Voltage	LVCMOS_CLK				0.8	V
V_{PP}	Peak-to-Peak Input Voltage	PCLK, nPCLK		300		1000	mV
V_{CMR}	Input Common Mode Voltage; NOTE 1, 2	PCLK, nPCLK		V_{DD} - 1.4		V_{DD} - 0.6	V
I_{IN}	Input Current					±200	µA
V_{OH}	Output High Voltage		I_{OH} = -20mA	1.8			V
V_{OL}	Output Low Voltage		I_{OL} = 20mA			0.5	V
I_{DD}	Core Supply Current					25	mA

NOTE 1: For single ended applications, the maximum input voltage for PCLK, nPCLK is V_{DD} + 0.3V.
NOTE 2: Common mode voltage is defined as V_{IH}.

TABLE 5B. AC CHARACTERISTICS, V_{DD} = 3.3V ± 5%, V_{DDO} = 2.5V ± 5%, TA = 0° TO 70°

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency					250	MHz
t_{pLH}	Propagation Delay	PCLK, nPCLK; NOTE 1, 5	f ≤ 150MHz	1.7		3.2	ns
		LVCMOS_CLK; NOTE 2, 5	f ≤ 150MHz	1.7		3.0	ns
t_{pLH}	Propagation Delay	PCLK, nPCLK; NOTE 1, 5	f > 150MHz	1.6		3.4	ns
		LVCMOS_CLK; NOTE 2, 5	f > 150MHz	1.8		3.3	ns
tsk(o)	Output Skew; NOTE 3, 5	PCLK, nPCLK	Measured on rising edge @V_{DDO}/2			150	ps
		LVCMOS_CLK				150	ps
tsk(pp)	Part-to-Part Skew; NOTE 6	PCLK, nPCLK	f ≤ 150MHz			1.5	ns
		LVCMOS_CLK	f ≤ 150MHz			1.3	ns
tsk(pp)	Part-to-Part Skew; NOTE 6	PCLK, nPCLK	f > 150MHz			1.8	ns
		LVCMOS_CLK	f > 150MHz			1.5	ns
tsk(pp)	Part-to-Part Skew; NOTE 4, 5	PCLK, nPCLK	Measured on rising edge @V_{DDO}/2			850	ps
		LVCMOS_CLK				750	ps
tjit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter section, NOTE 7				0.03		ps
t_R / t_F	Output Rise/Fall Time		0.5 to 1.8V	0.3		1.2	ns
odc	Output Duty Cycle		f < 134MHz	45	50	55	%

All parameters measured at 200MHz unless noted otherwise.
NOTE 1: Measured from the differential input crossing point to the output V_{DDO}/2.
NOTE 2: Measured from V_{DD}/2 to V_{DDO}/2.
NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at V_{DDO}/2.
NOTE 4: Defined as skew between outputs on different devices operating at the same supply voltages, same temperature, and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at V_{DDO}/2.
NOTE 5: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 6: Defined as skew between outputs on different devices, across temperature and voltage ranges, and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at V_{DDO}/2.
NOTE 7: Driving only one input clock.

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TABLE 4C. DC CHARACTERISTICS, $V_{DD} = V_{DDO} = 2.5V \pm 5\%$, $T_A = 0°$ TO $70°$

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	LVCMOS_CLK		2		V_{DD}	V
V_{IL}	Input Low Voltage	LVCMOS_CLK				0.8	V
V_{PP}	Peak-to-Peak Input Voltage	PCLK, nPCLK		300		1000	mV
V_{CMR}	Input Common Mode Voltage; NOTE 1, 2	PCLK, nPCLK		V_{DD} - 1.4		V_{DD} - 0.6	V
I_{IN}	Input Current					±200	µA
V_{OH}	Output High Voltage		I_{OH} = -12mA	1.8			V
V_{OL}	Output Low Voltage		I_{OL} = 12mA			0.5	V
I_{DD}	Core Supply Current					25	mA

NOTE 1: For single ended applications, the maximum input voltage for PCLK, nPCLK is V_{DD} + 0.3V.
NOTE 2: Common mode voltage is defined as V_{IH}.

TABLE 5C. AC CHARACTERISTICS, $V_{DD} = V_{DDO} = 2.5V \pm 5\%$, $T_A = 0°$ TO $70°$

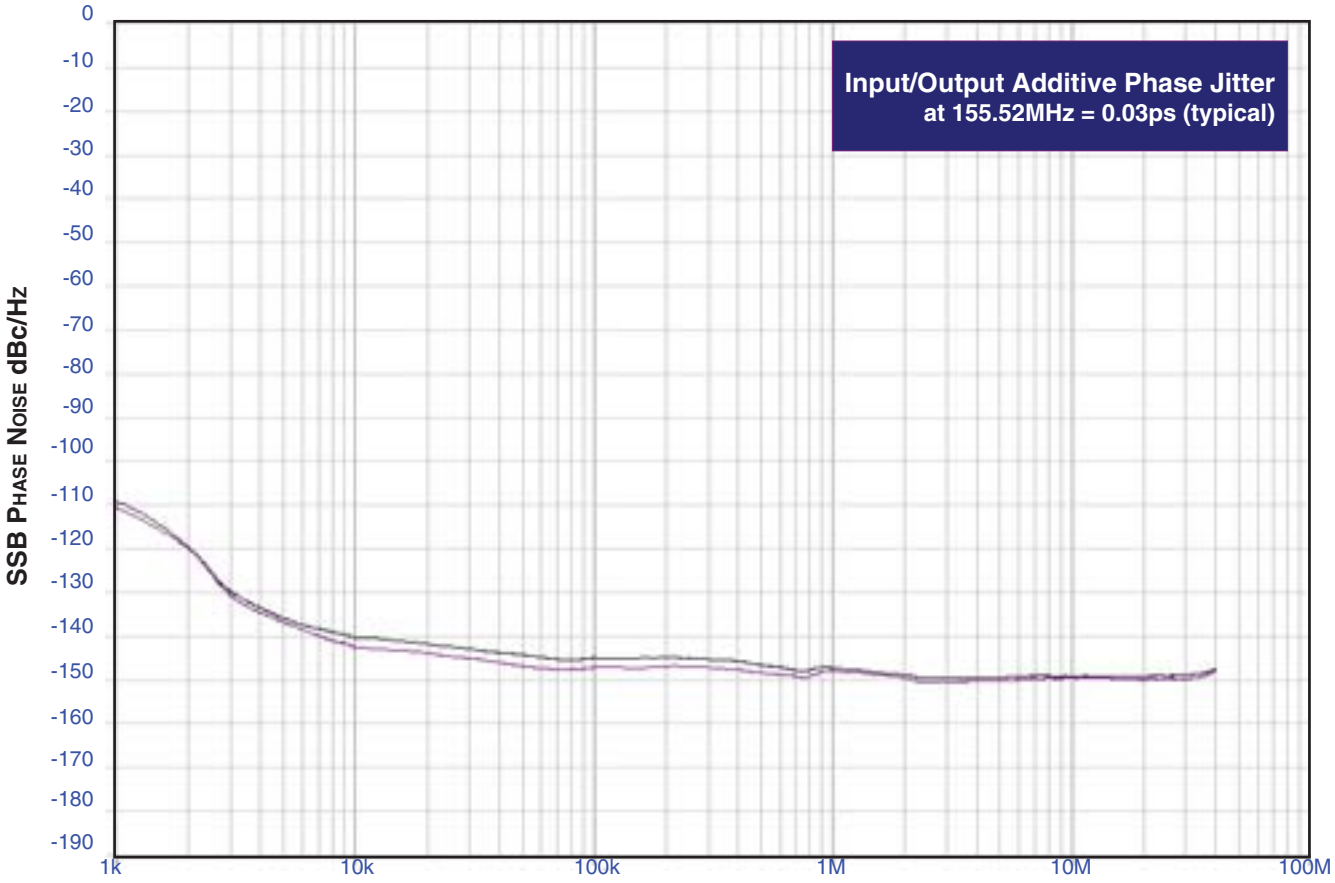
Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency					200	MHz
t_{pLH}	Propagation Delay;	PCLK, nPCLK; NOTE 1, 5	f ≤ 150MHz	1.2		3.8	ns
		LVCMOS_CLK; NOTE 2, 5	f ≤ 150MHz	1.5		3.2	ns
t_{pLH}	Propagation Delay;	PCLK, nPCLK; NOTE 1, 5	f > 150MHz	1.5		3.7	ns
		LVCMOS_CLK; NOTE 2, 5	f > 150MHz	2		3.6	ns
tsk(o)	Output Skew; NOTE 3, 5	PCLK, nPCLK	Measured on rising edge @V_{DDO}/2			200	ps
		LVCMOS_CLK				200	ps
tsk(pp)	Part-to-Part Skew; NOTE 6	PCLK, nPCLK	f ≤ 150MHz			2.6	ns
		LVCMOS_CLK	f ≤ 150MHz			1.7	ns
tsk(pp)	Part-to-Part Skew; NOTE 6	PCLK, nPCLK	f > 150MHz			2.2	ns
		LVCMOS_CLK	f > 150MHz			1.7	ns
tsk(pp)	Part-to-Part Skew; NOTE 4, 5	PCLK, nPCLK	Measured on rising edge @V_{DDO}/2			1.2	ns
		LVCMOS_CLK				1.0	ns
tjit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter section, NOTE 7				0.03		ps
t_R / t_F	Output Rise/Fall Time		0.5 to 1.8V	0.3		1.2	ns
odc	Output Duty Cycle		f < 134MHz	45		55	%

All parameters measured at 200MHz unless noted otherwise.
NOTE 1: Measured from the differential input crossing point to the output V_{DDO}/2.
NOTE 2: Measured from V_{DD}/2 to V_{DDO}/2.
NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at V_{DDO}/2.
NOTE 4: Defined as skew between outputs on different devices operating at the same supply voltages, same temperature, and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at V_{DDO}/2.
NOTE 5: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 6: Defined as skew between outputs on different devices, across temperature and voltage ranges, and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at V_{DDO}/2.
NOTE 7 Driving only one input clock.

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Additive Phase Jitter

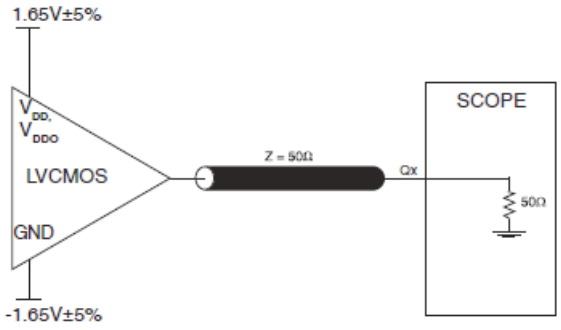
The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the ***dBc Phase Noise.*** This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a ***dBc*** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.



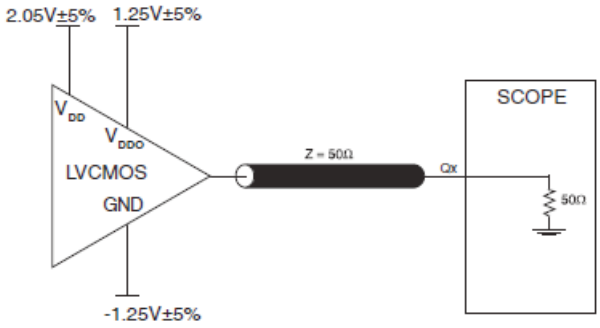
As with most timing specifications, phase noise measurements have issues. The primary issue relates to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This is illustrated above. The device meets the noise floor of what is shown, but can actually be lower. The phase noise is dependant on the input source and measurement equipment.

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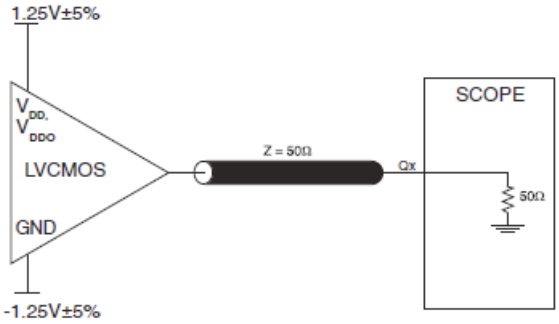
PARAMETER MEASUREMENT INFORMATION



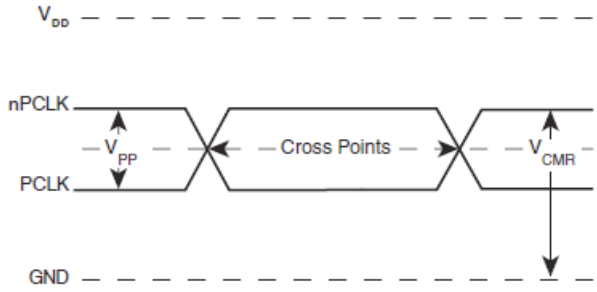
3.3V CORE/3.3V OUTPUT LOAD AC TEST CIRCUIT



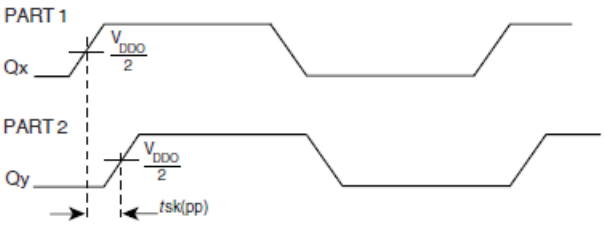
3.3V CORE/2.5V OUTPUT LOAD AC TEST CIRCUIT



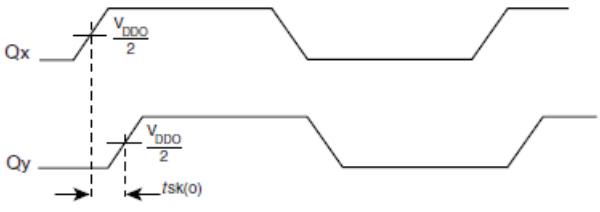
2.5V OUTPUT LOAD AC TEST CIRCUIT



DIFFERENTIAL INPUT LEVEL

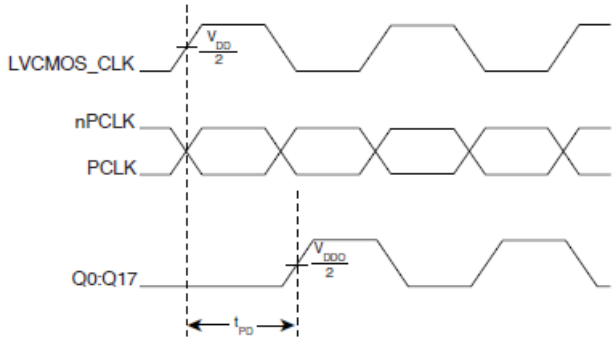


PART-TO-PART SKEW

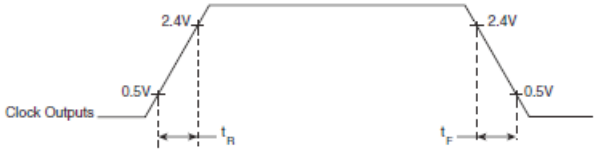


OUTPUT SKEW

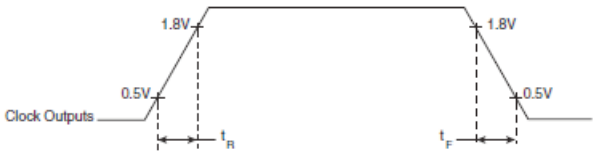
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PROPAGATION DELAY



3.3V OUTPUT RISE/FALL TIME



2.5V OUTPUT RISE/FALL TIME

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Application Information

Wiring the Differential Input to Accept Single Ended Levels

Figure 1 shows how the differential input can be wired to accept single ended levels. The reference voltage V_REF = V_{DD}/2 is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and V_{DD} = 3.3V, V_REF should be 1.25V and R2/R1 = 0.609.

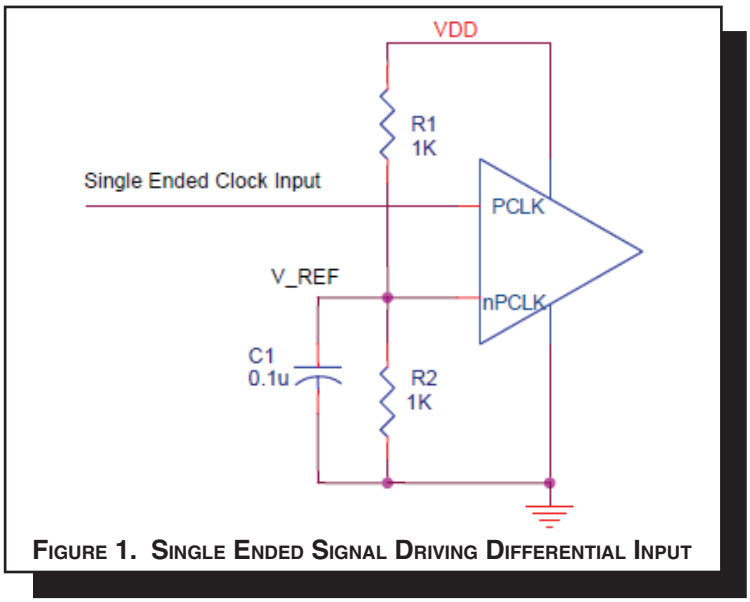


Figure 1. Single Ended Signal Driving Differential Input

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LVPECL Clock Input Interface

The PCLK /nPCLK accepts LVPECL, CML, SSTL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. *Figures 2A to 2F* show interface examples for the PCLK/nPCLK input driven by the most common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

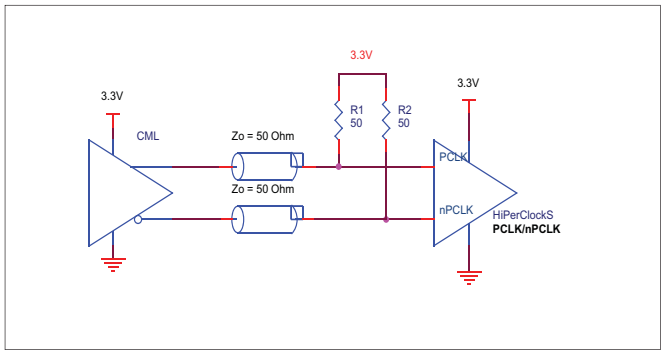


Figure 2A. PCLK/nPCLK Input Driven by an Open Collector CML Driver

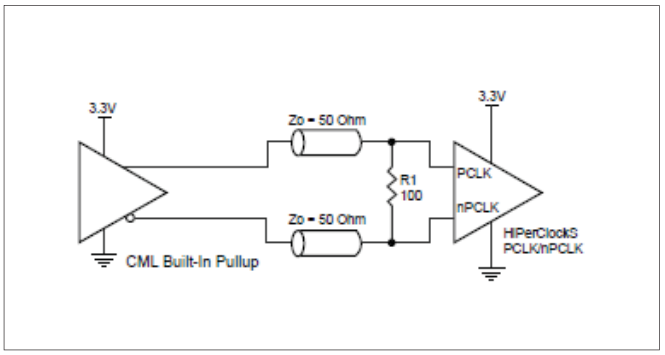


Figure 2B. PCLK/nPCLK Input Driven by a Built-In Pullup CML Driver

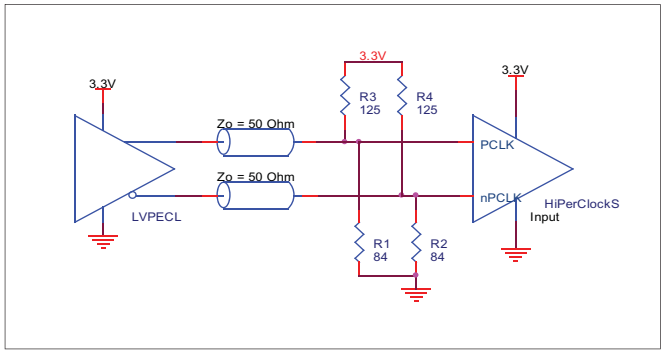


Figure 2C. PCLK/nPCLK Input Driven by a 3.3V LVPECL Driver

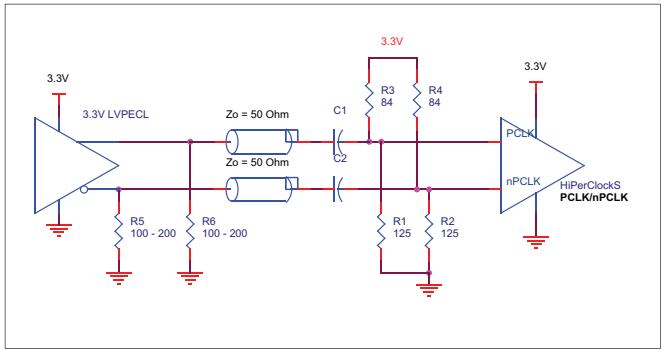


Figure 2D. PCLK/nPCLK Input Driven by a 3.3V LVPECL Driver with AC Couple

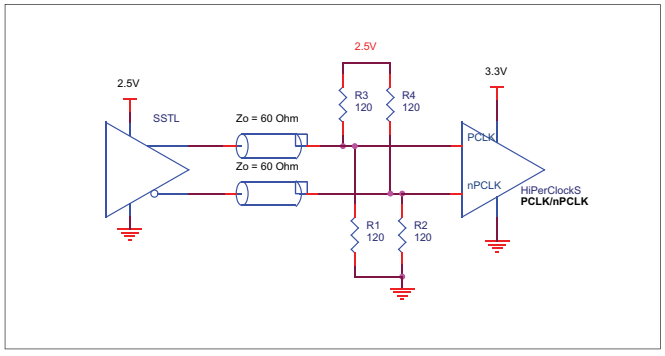


Figure 2E. PCLK/nPCLK Input Driven by an SSTL Driver

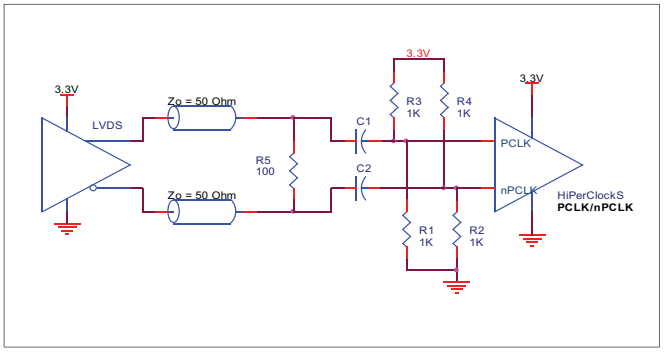


Figure 2F. PCLK/nPCLK Input Driven by a 3.3V LVDS Driver

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Reliability Information

Table 6. θ_{JA} vs. Air Flow Table for 32 Lead LQFP

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	67.8°C/W	55.9°C/W	50.1°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	47.9°C/W	42.1°C/W	39.4°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

Transistor Count

The transistor count for 83940D is: 820

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Package Outline - Y Suffix for 32 Lead LQFP

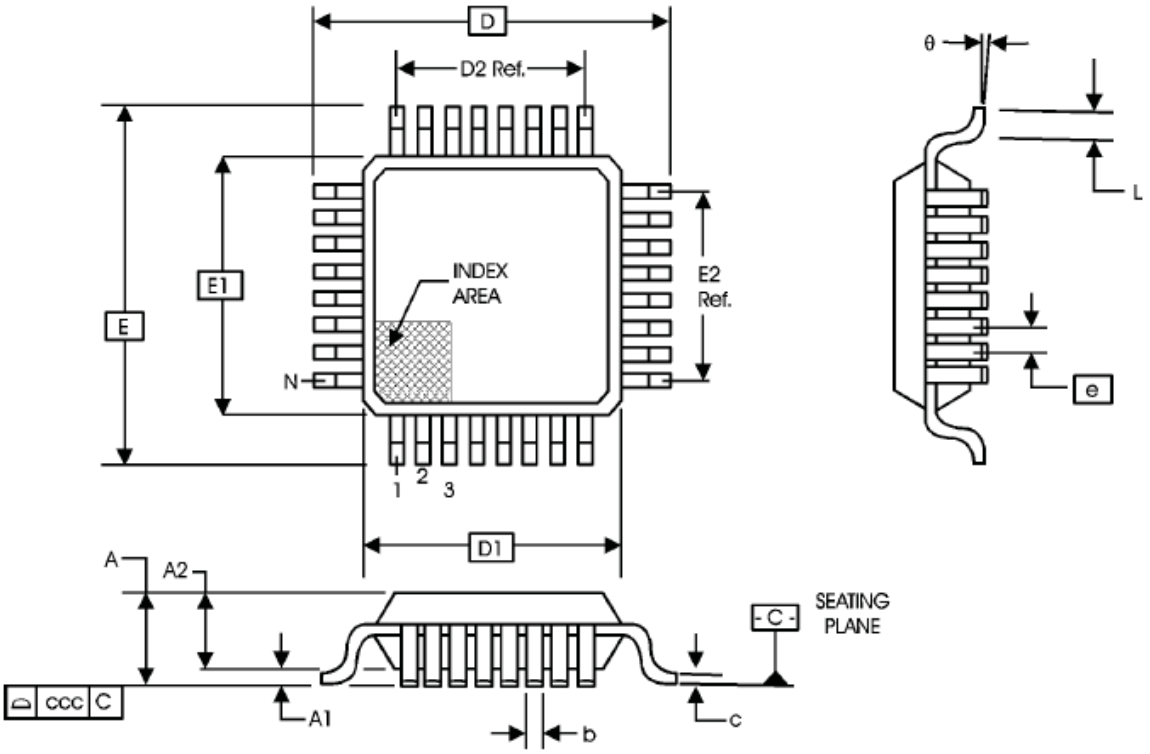


Table 7. Package Dimensions

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS			
SYMBOL	**BBA**		
	MINIMUM	**NOMINAL**	**MAXIMUM**
N		32	
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.30	0.37	0.45
c	0.09	--	0.20
D		9.00 BASIC	
D1		7.00 BASIC	
D2		5.60 Ref.	
E		9.00 BASIC	
E1		7.00 BASIC	
E2		5.60 Ref.	
e		0.80 BASIC	
L	0.45	0.60	0.75
θ	0°	--	7°
ccc	--	--	0.10

Reference Document: JEDEC Publication 95, MS-026

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TABLE 8. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
83940DYLF	ICS83940DYLF	32 Lead “Lead Free” LQFP	Tray	0°C to 70°C
83940DYLFT	ICS83940DYLF	32 Lead “Lead Free” LQFP	Tape and Reel	0°C to 70°C

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REVISION HISTORY SHEET				
Rev	**Table**	**Page**	**Description of Change**	**Date**
A	T5A	4	3.3V AC Characteristics table - • tsk(pp) Test Conditions, replaced “<” with “ ≤ “; corrected Units to “ns” from “ps”. • odc - corrected Test Conditions to read “134MHz ≤ f ≤ 250MHz”, from “f ≤ 250MHz”.	10/11/02
	T5B	5	3.3V/2.5V AC Characteristics table - tsk(pp) Test Conditions, replaced “<” with “ ≤ “; corrected Units to read “ns” from “ps”.	
	T5C	6	2.5V AC Characteristics table - tsk(pp) Test Conditions, replaced “<” with “ ≤ “; corrected Units to “ns” from “ps”.	
A	T2	2	Pin Characteristics table - changed R_{OUT} 25Ω maximum to 28Ω maximum. Delete R_{PULLUP} row.	12/12/02
			3.3V Output Load AC Test Circuit diagram - corrected GND equation to read -1.65V... from -1.165V...	
		7	Added LVTTL to title.	
			Updated format.	
B	T1	2	Pin Description Table - added Pullup and Pulldown to Pin 6, nPCLK.	10/9/03
		2	Pin Characteristics Table - added R_{PULLUP} row.	
	T2	4	Added tjit row.	
	T5A	5	Added tjit row.	
	T5B T5C	6	Added tjit row.	
		7	Added Additive Phase Jitter section.	
		10	Updated Single Ended Signal Driving Differential Input diagram.	
		11	Added LVPECL Clock Interface section.	
B	T5A - T5C	1	Added “Lead-Free” bullet to Features section.	6/15/04
		4 - 6	Added NOTE 7.	
		11	Updated LVPECL Clock Input Interface section.	
		14	Ordering Information table - added “Lead-Free” part number.	
B	T8	14	Updated datasheet’s header/footer with IDT from ICS.	8/9/10
		14	Removed ICS prefix from Part/Order Number column.	
		16	Added Contact Page.	
B	T8	14	Ordering Information - Removed leaded devices.	3/25/15
			Updated data sheet format.	

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