PRODUCT DISCONTINUATION NOTICE - LAST TIME BUY EXPIRES MAY 6, 2017

General Description

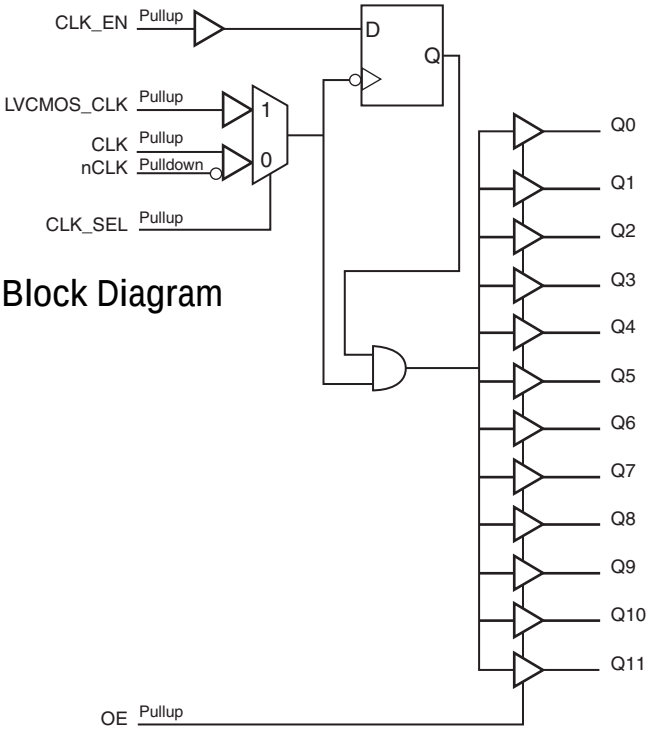
The 83948I is a low skew, 1-to-12 Differential-to-LVCMOS/LVTTL Fanout Buffer and a member of the family of High Performance Clock Solutions from IDT. The 83948I has two selectable clock inputs. The CLK, nCLK pair can accept most standard differential input levels. The LVCMOS_CLK can accept LVCMOS or LVTTL input levels. The low impedance LVCMOS/LVTTL outputs are designed to drive 50Ω series or parallel terminated transmission lines. The effective fanout can be increased from 12 to 24 by utilizing the ability of the outputs to drive two series terminated lines.

The 83948I is characterized at full 3.3V core/3.3V output. Guaranteed output and part-to-part skew characteristics make the 83948I ideal for those clock distribution applications demanding well defined performance and repeatability.

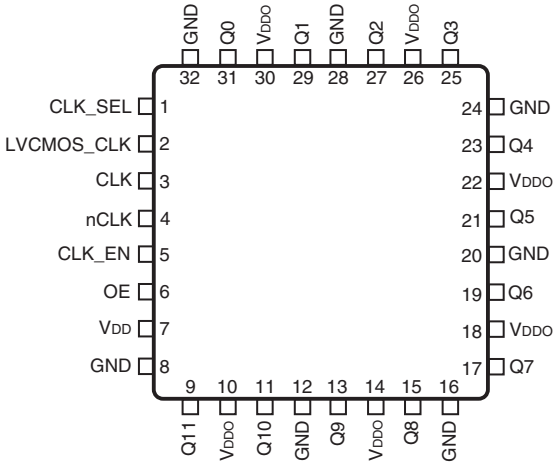
Features

- Twelve LVCMOS/LVTTL outputs
- Selectable differential CLK/nCLK or LVCMOS/LVTTL clock input
- CLK/nCLK pair can accept the following differential input levels: LVPECL, LVDS, LVHSTL, SSTL, HCSL
- LVCMOS_CLK supports the following input types: LVCMOS, LVTTL
- Maximum output frequency: 250MHz
- Output skew: 350ps (maximum)
- Part-to-part skew: 1.5ns (maximum)
- 3.3V core, 3.3V output
- -40°C to 85°C ambient operating temperature
- Available in lead-free (RoHS 6) package
- For drop in replacement part use 83948i-147

Block Diagram



Pin Assignment



83948I

32-Lead LQFP
7mm x 7mm x 1.4mm package body
Y Package
Top View

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Table 1. Pin Descriptions

Number	Name	Type		Description
1	CLK_SEL	Input	Pullup	Clock select input. When HIGH, selects LVCMOS_CLK input. When LOW, selects CLK/nCLK inputs. LVCMOS / LVTTL interface levels.
2	LVCMOS_CLK	Input	Pullup	Single-ended clock input. LVCMOS/LVTTL interface levels.
3	CLK	Input	Pullup	Non-inverting differential clock input.
4	nCLK	Input	Pulldown	Inverting differential clock input.
5	CLK_EN	Input	Pullup	Clock enable pin. LVCMOS/LVTTL interface levels.
6	OE	Input	Pullup	Output enable pin. LVCMOS/LVTTL interface levels.
7	V_{DD}	Power		Positive supply pin.
8, 12, 16, 20, 24, 28, 32	GND	Power		Power supply ground.
9, 11, 13, 15, 17, 19, 21, 23, 25, 27, 29, 31	Q11, Q10, Q9, Q8, Q7, Q6, Q5, Q4, Q3, Q2, Q1, Q0	Output		Single-ended clock outputs. LVCMOS/LVTTL interface levels.
10, 14, 18, 22, 26, 30	V_{DDO}	Power		Output supply pins.

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ
C_{PD}	Power Dissipation Capacitance (per output)			25		pF
R_{OUT}	Output Impedance			7		Ω

Function Tables

Table 3A. Clock Select Function Table

Control Input	Clock	
CLK_SEL	CLK/nCLK	LVCMOS_CLK
0	Selected	De-selected
1	De-selected	Selected

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Table 3B. Clock Input Function Table

Inputs				Outputs		
CLK_SEL	LVCMOS_CLK	CLK	nCLK	Q[0:11]	Input to Output Mode	Polarity
0	–	0	1	LOW	Differential to Single-Ended	Non-Inverting
0	–	1	0	HIGH	Differential to Single-Ended	Non-Inverting
0	–	0	Biased; NOTE 1	LOW	Single-Ended to Single-Ended	Non-Inverting
0	–	1	Biased; NOTE 1	HIGH	Single-Ended to Single-Ended	Non-Inverting
0	–	Biased; NOTE 1	0	HIGH	Single-Ended to Single-Ended	Inverting
0	–	Biased; NOTE 1	1	LOW	Single-Ended to Single-Ended	Inverting
1	0	–	–	LOW	Single-Ended to Single-Ended	Non-Inverting
1	1	–	–	HIGH	Single-Ended to Single-Ended	Non-Inverting

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5V
Outputs, V_O	-0.5V to V_{DDO} + 0.5V
Package Thermal Impedance, θ_{JA}	47.9°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, $V_{DD} = V_{DDO} = 3.3V \pm 0.3V$, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Positive Supply Voltage		3.0	3.3	3.6	V
V_{DDO}	Output Supply Voltage		3.0	3.3	3.6	V
I_{DD}	Power Supply Current				55	mA

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Table 4B. DC Characteristics, $V_{DD} = V_{DDO} = 3.3V \pm 0.3V$, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage		-0.3		0.8	V
V_{PP}	Peak-to-Peak Input Voltage; NOTE 1		0.15		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2		GND + 0.5		V_{DD} – 0.85	V
I_{IN}	Input Current				±100	µA
V_{OH}	Output High Voltage	I_{OH} = -20mA	2.5			V
V_{OL}	Output Low Voltage	I_{OL} = 20mA			0.4	V

NOTE 1: V_{IL} should not be less than -0.3V.
NOTE 2: Common mode voltage is defined as V_{IH}.

AC Electrical Characteristics

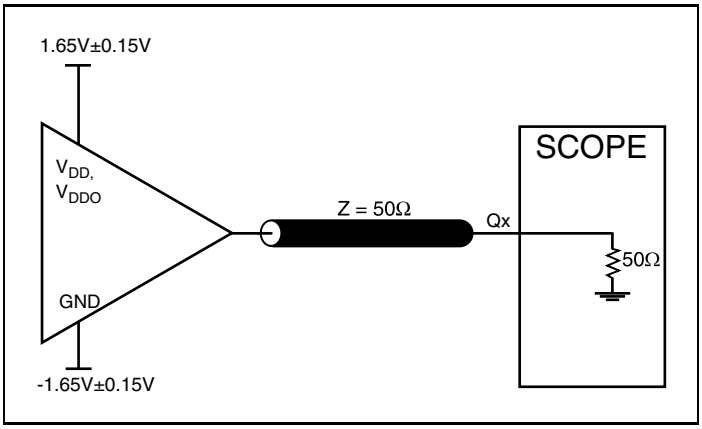
Table 5. AC Characteristics, $V_{DD} = V_{DDO} = 3.3V \pm 0.3V$, T_A = -40°C to 85°C

Parameter	Symbol		Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency					250	MHz
t_{PD}	Propagation Delay	CLK/nCLK; NOTE 1A	$f \leq$ 150MHz	2.25		3.75	ns
		LVCMOS_CLK; NOTE 1B	$f \leq$ 150MHz	2		4	ns
*t*sk(o)	Output Skew; NOTE 2, 6		Measured on Rising Edge @ $V_{DDO}/2$			350	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 3, 6	CLK/nCLK	Measured on Rising Edge @ $V_{DDO}/2$			1.5	ns
		LVCMOS_CLK				2	ns
t_R / t_F	Output Rise/Fall Time		0.8V to 2V	0.2		1.0	ns
t_{PW}	Output Pulse Width		f < 150MHz	$t_{Cycle}/2$ - 800		$t_{Cycle}/2$ + 800	ps
t_{PZL}, t_{PZH}	Output Enable Time; NOTE 4					11	ns
t_{PLZ}, t_{PHZ}	Output Disable Time; NOTE 4					11	ns
t_S	Clock Enable Setup Time; NOTE 5	CLK_EN to CLK/nCLK		1			ns
		CLK_EN to LVCMOS_CLK		0			ns
t_H	Clock Enable Hold Time; NOTE 5	CLK/nCLK to CLK_EN		1			ns
		LVCMOS_CLK to CLK_EN		1			ns

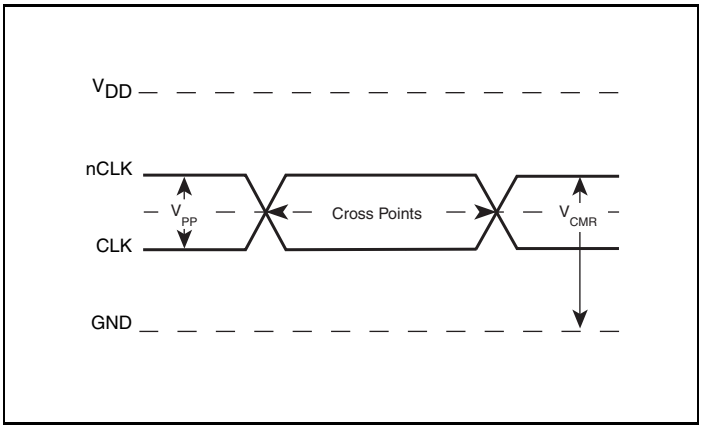
NOTE 1A: Measured from the differential input crossing point to $V_{DDO}/2$ of the output.
NOTE 1B: Measured from $V_{DD}/2$ or crosspoint of the input to $V_{DDO}/2$ of the output.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DDO}/2$.
NOTE 3: Defined as skew between outputs on different devices operating a the same supply voltage and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at $V_{DDO}/2$.
NOTE 4: These parameters are guaranteed by characterization. Not tested in production.
NOTE 5: Setup and Hold times are relative to the rising edge of the input clock.
NOTE 6: This parameter is defined in accordance with JEDEC Standard 65.

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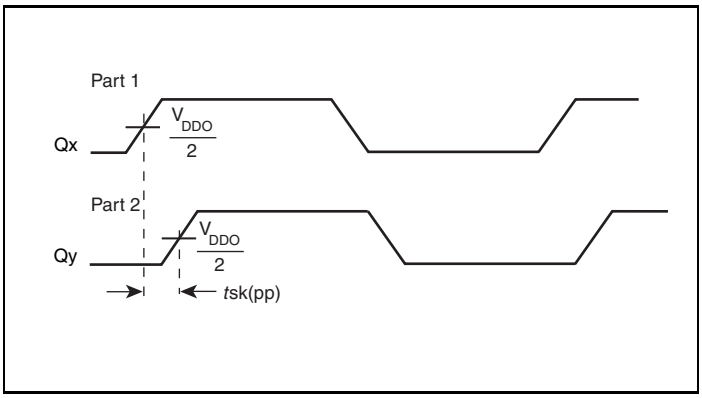
Parameter Measurement Information



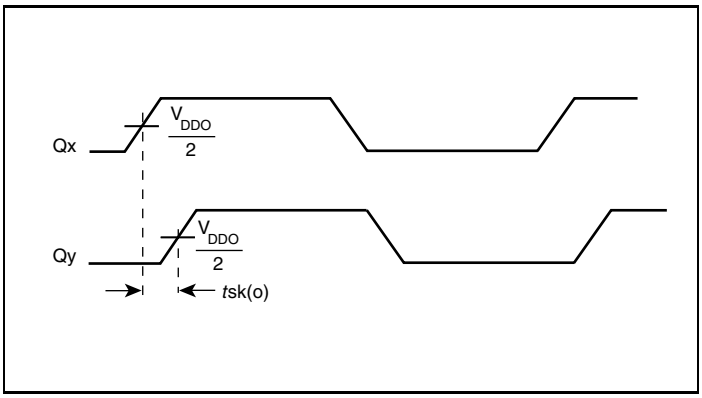
3.3V Core/3.3V LVCMOS Output Load AC Test Circuit



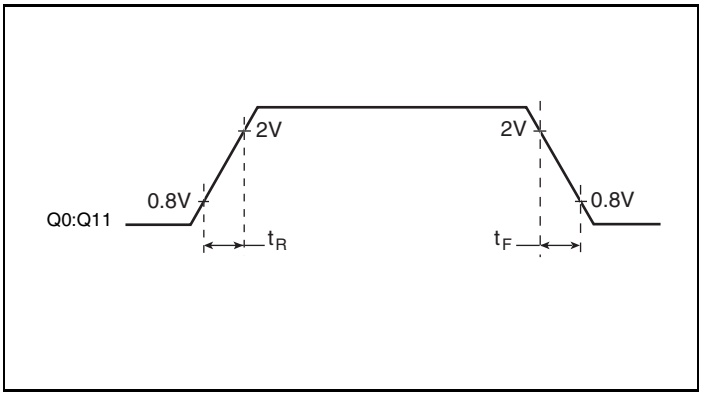
Differential Input Level



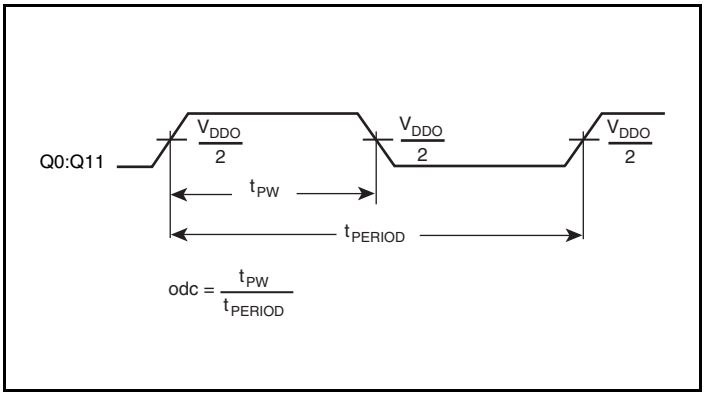
Part-to-Part Skew



Output Skew

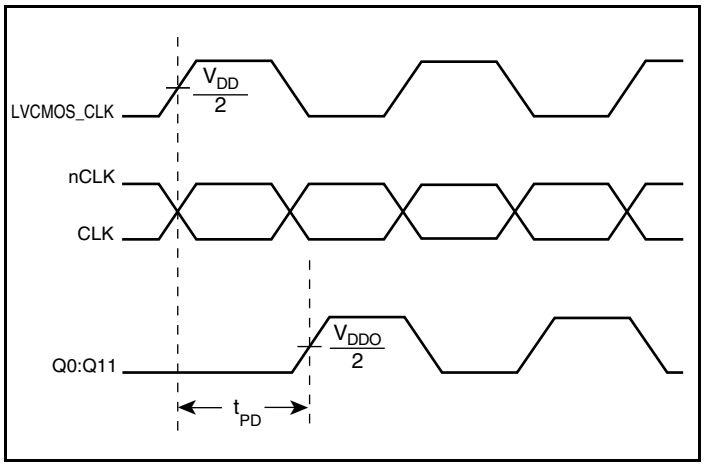


Output Rise/Fall Time



Output Pulse Width

Parameter Measurement Information, continued



Propagation Delay

Application Information

Wiring the Differential Input to Accept Single Ended Levels

Figure 1 shows how the differential input can be wired to accept single ended levels. The reference voltage V_REF = V_{DD}/2 is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and V_{DD} = 3.3V, V_REF should be 1.25V and R2/R1 = 0.609.

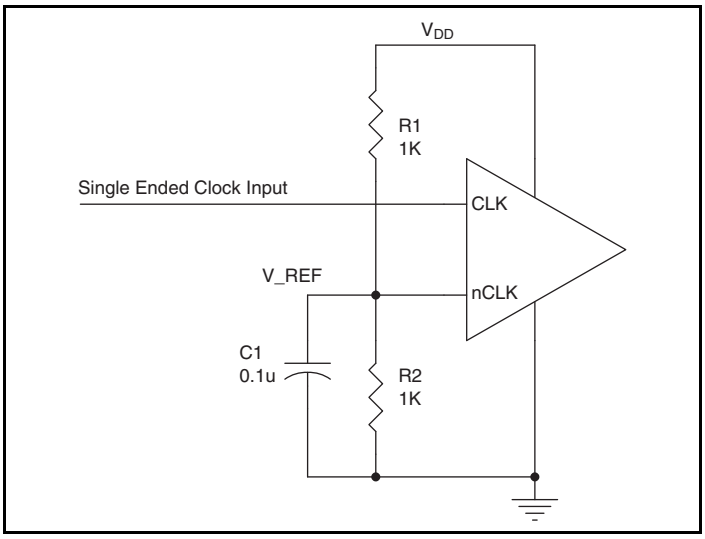


Figure 1. Single-Ended Signal Driving Differential Input

Recommendations for Unused Input and Output Pins

Inputs:

CLK/nCLK Inputs

For applications not requiring the use of the differential input, both CLK and nCLK can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from CLK to ground.

CLK Input

For applications not requiring the use of a clock input, it can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from the CLK input to ground.

LVCMOS Control Pins

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs:

LVCMOS Outputs

All unused LVCMOS output can be left floating. There should be no trace attached.

Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, SSTL, HCSL and other differential signals. Both signals must meet the V_{PP} and V_{CMR} input requirements. *Figures 2A to 2F* show interface examples for the HiPerClockS CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example, in Figure 2A, the input termination applies for IDT HiPerClockS open emitter LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

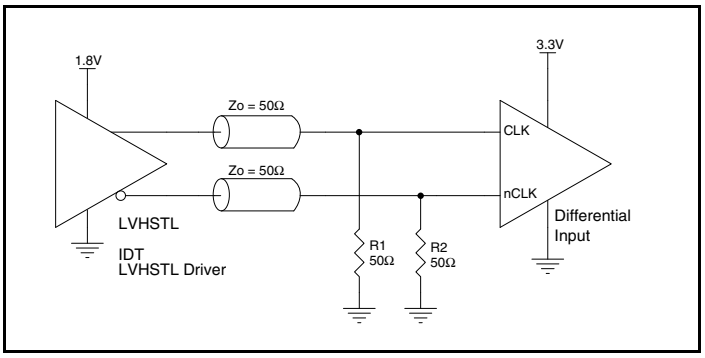


Figure 2A. HiPerClockS CLK/nCLK Input Driven by an IDT Open Emitter HiPerClockS LVHSTL Driver

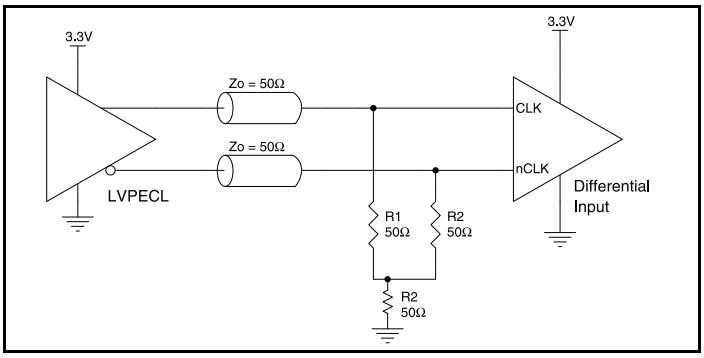


Figure 2B. HiPerClockS CLK/nCLK Input Driven by a 3.3V LVPECL Driver

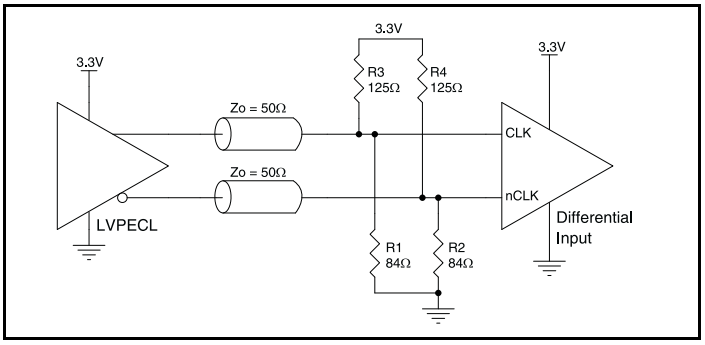


Figure 2C. HiPerClockS CLK/nCLK Input Driven by a 3.3V LVPECL Driver

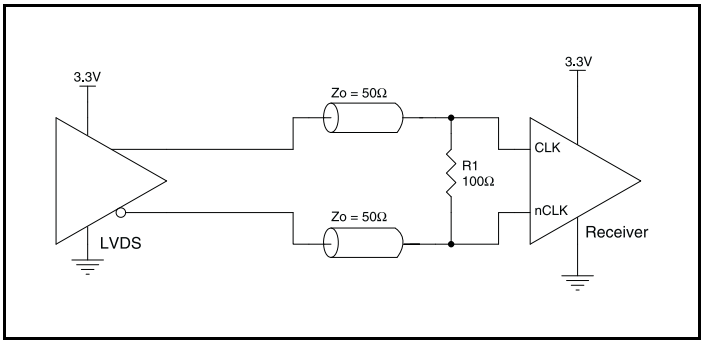


Figure 2D. HiPerClockS CLK/nCLK Input Driven by a 3.3V LVDS Driver

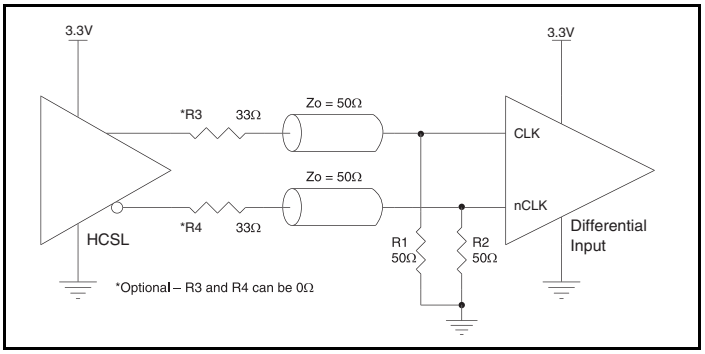


Figure 2E. HiPerClockS CLK/nCLK Input Driven by a 3.3V HCSL Driver

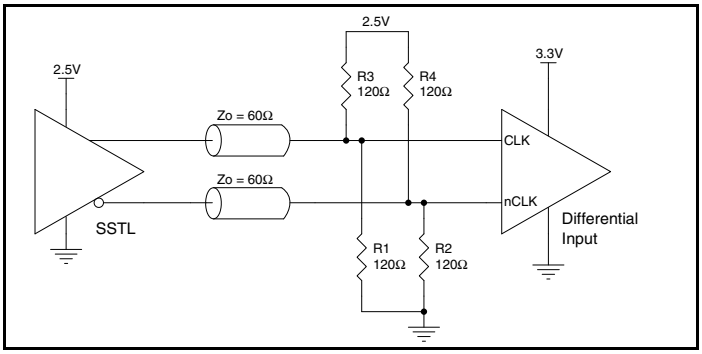


Figure 2F. HiPerClockS CLK/nCLK Input Driven by a 2.5V SSTL Driver

Reliability Information

Table 6. θ_{JA} vs. Air Flow Table for a 32 Lead LQFP

θ_{JA} by Velocity			
Linear Feet per Minute	**0**	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	67.8°C/W	55.9°C/W	50.1°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	47.9°C/W	42.1°C/W	39.4°C/W

Transistor Count

The transistor count for 83948I is: 1040
Pin compatible with the MPC948/948L

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Package Outline and Package Dimensions

Package Outline - Y Suffix for 32 Lead LQFP

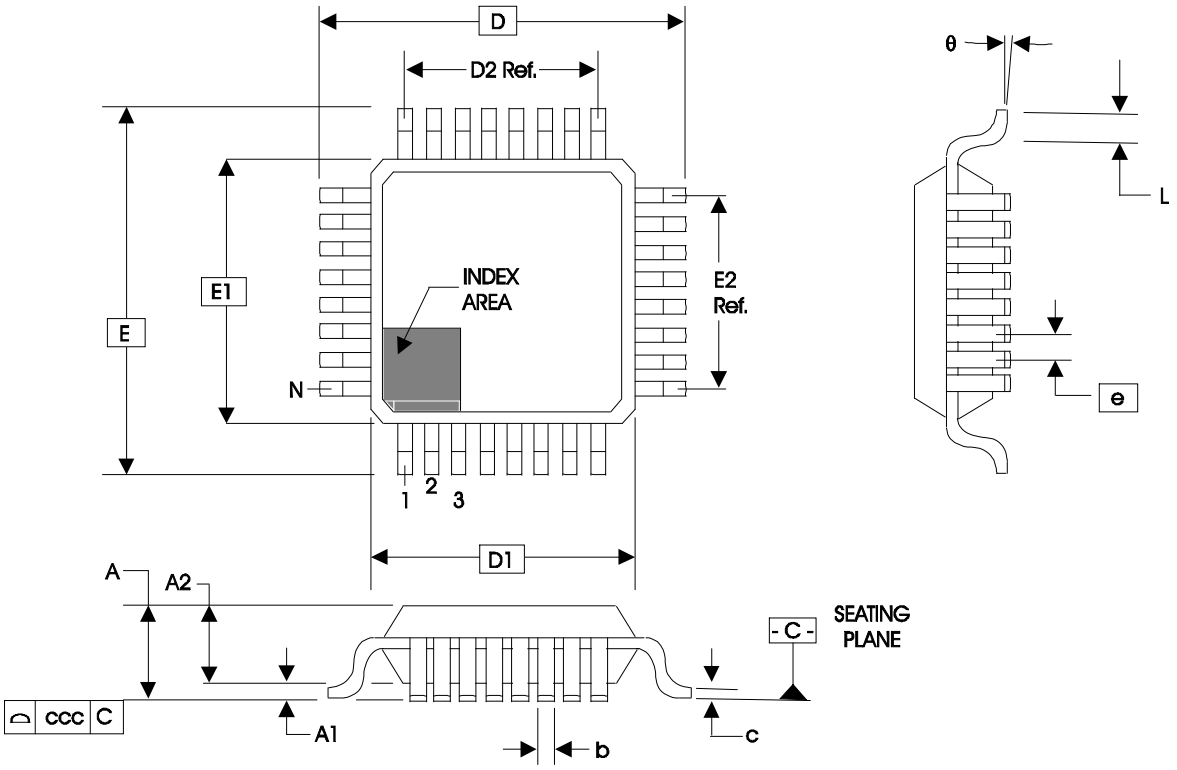


Table 7. Package Dimensions for 32 Lead LQFP

JEDEC Variation: ABC - HD All Dimensions in Millimeters			
Symbol	**Minimum**	**Nominal**	**Maximum**
N		32	
A			1.60
A1	0.05	0.10	0.15
A2	1.35	1.40	1.45
b	0.30	0.37	0.45
c	0.09		0.20
D & E		9.00 Basic	
D1 & E1		7.00 Basic	
D2 & E2		5.60 Ref.	
e		0.80 Basic	
L	0.45	0.60	0.75
θ	0°		7°
ccc			0.10

Reference Document: JEDEC Publication 95, MS-026

Ordering Information

Table 8. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
83948AYILF	ICS83948AYIL	“Lead-Free” 32 Lead LQFP	Tray	-40°C to 85°C
83948AYILFT	ICS83948AYI	“Lead-Free” 32 Lead LQFP	Tape & Reel	-40°C to 85°C

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Revision History Sheet

Rev	Table	Page	Description of Change	Date
B	T5	4	AC Characteristics table - tLZ, tHZ row changed symbol to read t_{PLZ}, t_{PHZ} and changed Parameter to read Output Enable Time. Added rows: t_S ""Clock Enable Setup Time"" and t_H ""Clock Enable Hold Time"".	5/20/02
B	T5	4	AC Characteristics table, t_S and t_H rows - replaced SYNC_OE with CLK_EN. Added an extra note to Propagation Delay row.	6/26/02
B	T5	4	AC Characteristics table, f_{MAX} row corrected typo error of 150MHz to 250MHz.	8/8/02
B	T5	4	AC Characteristics table - t_{PW} row, added f< 150MHz for t_{PW} Test Conditions.	11/11/02
C	T2 T8	1 2 6 9	Features Section - added Lead-Free bullet. Pin Characteristics Table - changed C_{IN} from 4pF max. to 4pF typical. Added Recommendations for Unused Output Pins. Ordering Information Table - added Lead-Free part number, marking and note.	12/15/05
C	T8	8 11	Added *Differential Clock Input Interface* Section. Ordering Information Table - corrected Temperature column. Updated datasheet format.	3/6/08
C	T8	11	Removed leaded orderable parts from Ordering Information table	11/14/12
C	T8	1 11	General Description - Removed ICS Chip and HiPerClockS. Features Section - Removed reference to leaded packages Removed ICS from the Part Number. Ordering Information - Removed ICS from the Part/Order Number. Removed 1000 from the Tape & Reel. Removed the LF note from below the table. Updated Header and Footer.	12/16/15
C			Product Discontinuation Notice - Last time buy expires May 6, 2017. PDN CQ-16-01	5/19/16

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(Rev.1.0 Mar 2020)

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