Description

The 841N254B is a 4-output clock synthesizer designed for S-RIO 1.3 and 2.0 reference clock applications. The device generates four copies of a selectable 250MHz, 156.25MHz, 125MHz or 100MHz clock signal with excellent phase jitter performance. The four outputs are organized in two banks of two LVDS and two HCSL ouputs. The device uses IDT's fourth generation FemtoClock® NG technology for an optimum of high clock frequency and low phase noise performance, combined with a low power consumption and high power supply noise rejection. The synthesized clock frequency and the phase-noise performance are optimized for driving RIO 1.3 and 2.0 SerDes reference clocks.

The device supports 3.3V and 2.5V voltage supplies and is packaged in a small 32-lead VFQFN package. The extended temperature range supports wireless infrastructure, telecommunication and networking end equipment requirements.

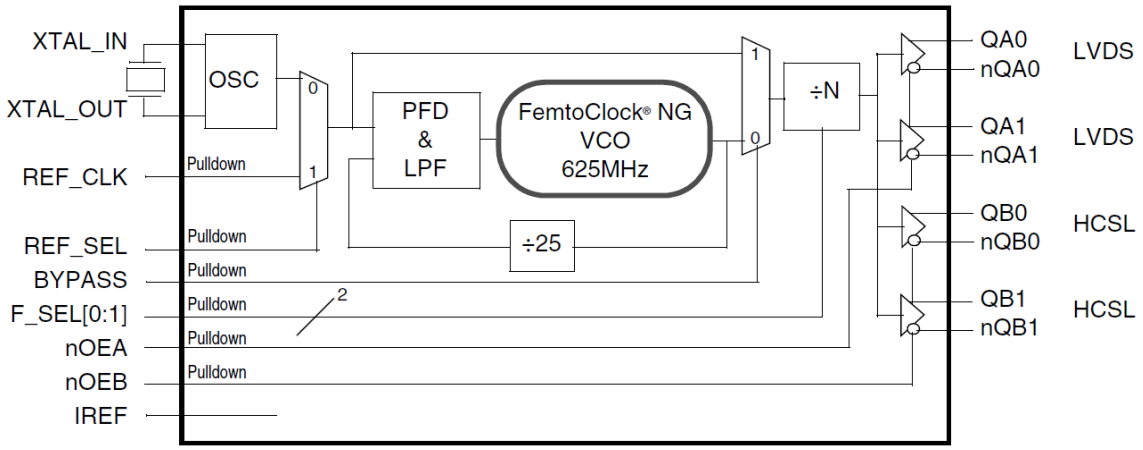
Function Table

Inputs		Output Frequency with f_{XTAL} = 25MHz
F_SEL1	F_SEL0	
0 (default)	0 (default)	156.25MHz
0	1	125MHz
1	0	100MHz
1	1	250MHz
NOTE: F_SEL[1:0] are asynchronous controls.		

Features

- Fourth generation FemtoClock® (NG) technology
- Selectable 250MHz, 156.25MHz, 125MHz or 100MHz output clock synthesized from a 25MHz fundamental mode crystal
- Four differential clock outputs (two LVDS and two HCSL outputs)
- Crystal interface designed for 25MHz, parallel resonant crystal
- RMS phase jitter at 156.25MHz, using a 25MHz crystal (1MHz - 20MHz): 0.27ps (typical)
- RMS phase jitter at 156.25MHz, using a 25MHz crystal (12kHz - 20MHz): 0.32ps (typical)
- Power supply noise rejection PSNR: -50dB (typical)
- LVCMOS interface levels for the frequency select input
- Full 3.3V or 2.5V supply voltage
- Lead-free (RoHS 6) packaging
- -40°C to 85°C ambient operating temperature

Block Diagram



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Pin Description and Pin Characteristic Tables

Table 1. Pin Descriptions

Number	Name	Type[a]		Description
1, 8, 13, 32	V_{DD}	Power		Core supply pins.
2, 4	nc	Unused		No connect.
3	V_{DDA}	Power		Analog power supply.
5, 17, 23, 25, 31	GND	Power		Power supply ground.
6	REF_CLK	Input	Pulldown	Alternative single-ended reference clock input. LVCMOS/LVTTL interface levels.
7	nOEA	Input	Pulldown	Output enable input. See Table 6 for function. LVCMOS/LVTTL interface levels.
9	nOEB	Input	Pulldown	Output enable input. See Table 7 for function. LVCMOS/LVTTL interface levels.
10	REF_SEL	Input	Pulldown	Reference select input. See Table 4 for function. LVCMOS/LVTTL interface levels.
11, 12	XTAL_IN, XTAL_OUT	Input		Crystal oscillator interface. XTAL_IN is the input, XTAL_OUT is the output.
14	BYPASS	Input	Pulldown	Bypass mode select pin. See Table 5 for function. LVCMOS/LVTTL interface levels.
15, 16	F_SEL0, F_SEL1	Input	Pulldown	Frequency select pin. See Table 3 for function. LVCMOS/LVTTL interface levels.
18, 19	QA1, nQA1	Output		Differential clock output. LVDS interface levels.
20	V_{DDOA}	Power		Output supply pin for QAx outputs.
21, 22	QA0, nQA0	Output		Differential clock output. LVDS interface levels.
24	IREF	Input		External fixed precision resistor (475Ω) from this pin to ground provides a reference current used for differential current-mode QBx, nQBx clock outputs.
26, 27	nQB1, QB1	Output		Differential clock output. HCSL interface levels.
28	V_{DDOB}	Power		Output supply pin for QBx outputs.
29, 30	nQB0, QB0	Output		Differential clock output. HCSL interface levels.

[a] *Pulldown* refers to internal input resistors. See Table 2 for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
$R_{PULLDOWN}$	Input Pulldown Resistor			100		kΩ

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Function Tables

Table 3. Output Divider and Output Frequency

Inputs[a]		Operation	f_{OUT} with f_{REF} = 25MHz
F_SEL1	F_SEL0		
0 (default)	0 (default)	$f_{OUT} = f_{REF} * 25 \div 4$	156.25MHz
0	1	$f_{OUT} = f_{REF} * 5$	125MHz
1	0	$f_{OUT} = f_{REF} * 4$	100MHz
1	1	$f_{OUT} = f_{REF} * 10$	250MHz

[a] F_SEL[1:0] are asynchronous controls.

Table 4. PLL Reference Clock Select Function Table

Input	Operation
REF_SEL[a]	
0 (default)	The crystal interface is selected as reference clock
1	The REF_CLK input is selected as reference clock

[a] REF_SEL is an asynchronous control.

Table 5. PLL BYPASS Function Table

Input	Operation
BYPASS[a]	
0 (default)	PLL is enabled. The reference frequency f_{REF} is multiplied by the PLL feedback divider of 25 and then divided by the selected output divider N.
1	PLL is bypassed. The reference frequency f_{REF} is divided by the selected output divider N. AC specifications do not apply in PLL bypass mode.

[a] BYPASS is an asynchronous control.

Table 6. nOEA Output Enable Function Table

Input	Operation
nOEA[a]	
0 (default)	QA0, nQA0 and QA1, nQA1 outputs are enabled
1	QA0, nQA0 and QA1, nQA1 outputs are disabled (high-impedance)

[a] nOEA is an asynchronous control.

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Table 7. nOEB Output Enable Function Table

Input	
nOEB[a]	Operation
0 (default)	QB0, nQB0 and QB1, nQB1 outputs are enabled
1	QB0, nQB0 and QB1, nQB1 outputs are disabled (high-impedance)

[a] nOEB is an asynchronous control.

Absolute Maximum Ratings

Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of the product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Table 8. Absolute Maximum Ratings

Item	Rating
Supply Voltage, V_{DD}	3.6V
Inputs, V_I XTAL_IN Other Inputs	 0V to 2V -0.5V to V_{DD} + 0.5V
Outputs, V_O (HCSL)	-0.5V to V_{DD} + 0.5V
Outputs, I_O (LVDS) Continuous Current Surge Current	 10mA 15mA
Package Thermal Impedance, θ_{JA}	37.7°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

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DC Electrical Characteristics

Table 9. Power Supply DC Characteristics, V_{DD} = V_{DDOA} = V_{DDOB} = 3.3V±5% or 2.5V±5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
			2.375	2.5	2.625	V
V_{DDA}	Analog Supply Voltage		V_{DD} – 0.30	3.3	V_{DD}	V
			V_{DD} – 0.30	2.5	V_{DD}	V
$V_{DDOA\&B}$	Output Supply Voltage		3.135	3.3	3.465	V
			2.375	2.5	2.625	V
I_{DDA}	Analog Supply Current				30	mA
I_{DD}	Power Supply Current				113	mA
$I_{DDOA\&B}$	Output Supply Current				72	mA

Table 10. LVCMOS/LVTTL Input DC Characteristics, V_{DD} = V_{DDOA} = V_{DDOB} = 3.3V±5% or 2.5V±5%, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		V_{DD} = 3.3V	2		V_{DD} + 0.3	V
			V_{DD} = 2.5V	1.7		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage		V_{DD} = 3.3V	-0.3		0.8	V
			V_{DD} = 2.5V	-0.3		0.7	V
I_{IH}	Input High Current	nOEA, nOEB, BYPASS, REF_SEL, REF_CLK, F_SEL[1:0]	V_{DD} = V_{IN} = 2.625V or 3.465V			150	µA
I_{IL}	Input Low Current	nOEA, nOEB, BYPASS, REF_SEL, REF_CLK, F_SEL[1:0]	V_{DD} = 2.625V or 3.465V, V_{IN} = 0V	-5			µA

Table 11. LVDS 3.3V DC Characteristics, V_{DD} = V_{DDOA} = 3.3V ± 5% or 2.5V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage		200		550	mV
ΔV_{OD}	V_{OD} Magnitude Change				50	mV
V_{OS}	Offset Voltage		1.1		1.3	V
ΔV_{OS}	V_{OS} Magnitude Change				50	mV

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Table 12. Crystal Characteristics

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency			25		MHz
Equivalent Series Resistance (ESR)				80	Ω
Shunt Capacitance				7	pF

DC Electrical Characteristics

Table 13. AC Characteristics, V_{DD} = V_{DDOA} = V_{DDOB} = 3.3V±5% or 2.5V±5%, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency		F_SEL [1:0] = 00		156.25		MHz
			F_SEL [1:0] = 01		125		MHz
			F_SEL [1:0] = 10		100		MHz
			F_SEL [1:0] = 11		250		MHz
f_{REF}	Reference Frequency		REF_CLK		25		MHz
*t*jit(Ø)	RMS Phase Jitter (Random); NOTE 1		156.25MHz, Integration Range: 1MHz – 20MHz		0.27		ps
			156.25MHz, Integration Range: 12kHz – 20MHz		0.32		ps
			125MHz, Integration Range: 1MHz – 20MHz		0.33		ps
			125MHz,Integration Range: 12kHz – 20MHz		0.37		ps
Φ_N	Single-Side Band Noise Power		156.25MHz, Offset: 100Hz		-91.6		dBc/Hz
			156.25MHz, Offset: 1kHz		-120.8		dBc/Hz
			156.25MHz, Offset: 10kHz		-132.2		dBc/Hz
			156.25MHz, Offset: 100kHz		-135.0		dBc/Hz
PSNR	Power Supply Noise Rejection		From DC to 50MHz		-50		dB
tsk(o)	Output Skew	NOTE 2, 3	Between QAx/nQAx & QBx/nQBx		1.8	2.7	ns
tsk(b)	Bank Skew	NOTE 3, 4				55	ps
t_R / t_F	Output Rise/Fall Time	QAx, nQAx	20% to 80%	100		400	ps
t_{LOCK}	PLL Lock Time					20	ms
V_{RB}	Ring-back Voltage Margin; NOTE 5, 6	QBx, nQBx		-100		100	mV
t_{STABLE}	Time before V_{RB} is Allowed; NOTE 5, 6	QBx, nQBx		500			ps

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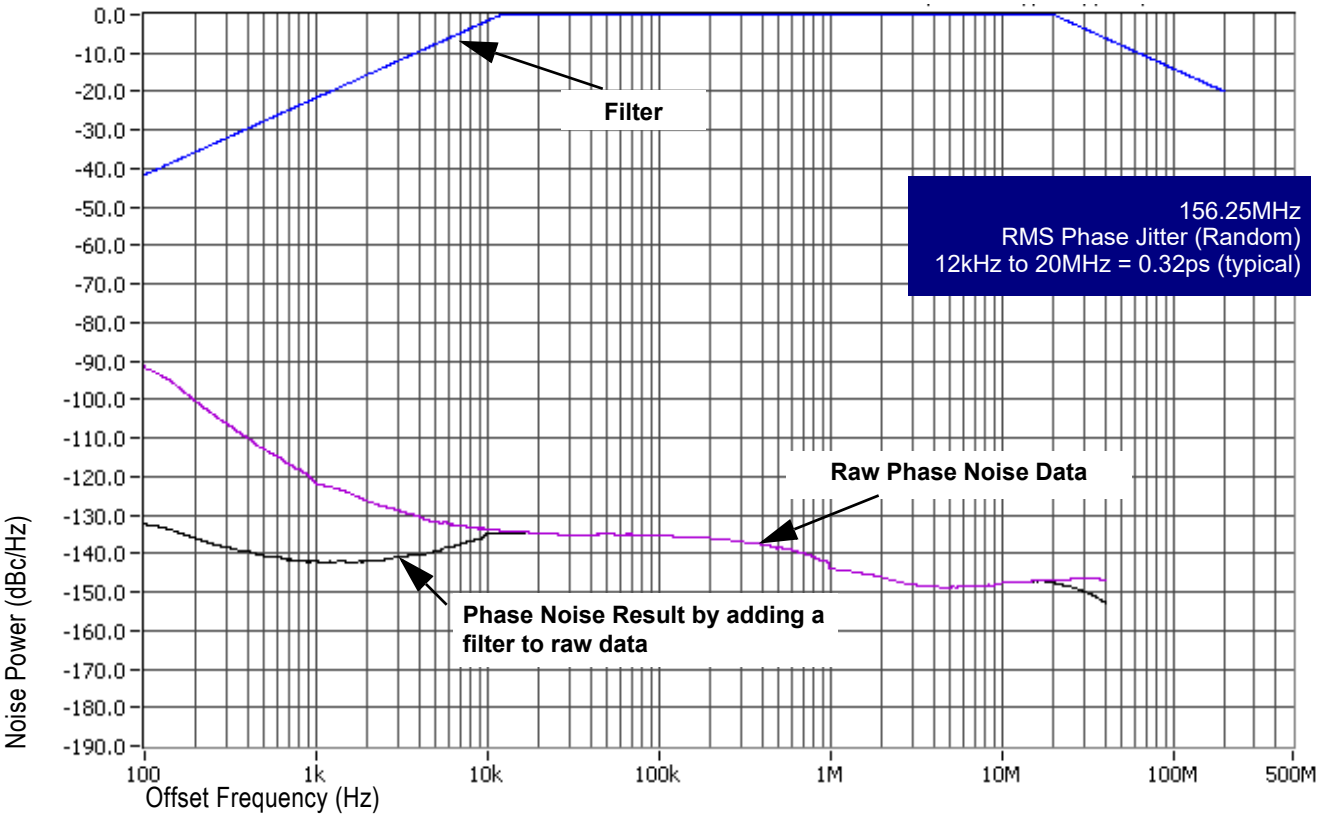
Table 13. AC Characteristics, V_{DD} = V_{DDOA} = V_{DDOB} = 3.3V±5% or 2.5V±5%, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{MAX}	Absolute Maximum Output Voltage; NOTE 7, 8	QBx, nQBx				1150	mV
V_{MIN}	Absolute Minimum Output Voltage; NOTE 7, 9	QBx, nQBx		-300			mV
V_{CROSS}	Absolute Crossing Voltage; NOTE 7, 10, 11	QBx, nQBx		100		350	mV
ΔV_{CROSS}	Total Variation of V_{CROSS} over all edges; NOTE 7, 10, 12	QBx, nQBx				140	mV
	Rise/Fall Edge Rate; NOTE 5, 13	QBx, nQBx	Measured between -150mV to 150mV	0.6		5.5	V/ns
odc	Output Duty Cycle; NOTE 5	QBx, nQBx		47		53	%
	Output Duty Cycle	QAx, nQAx		47		53	%

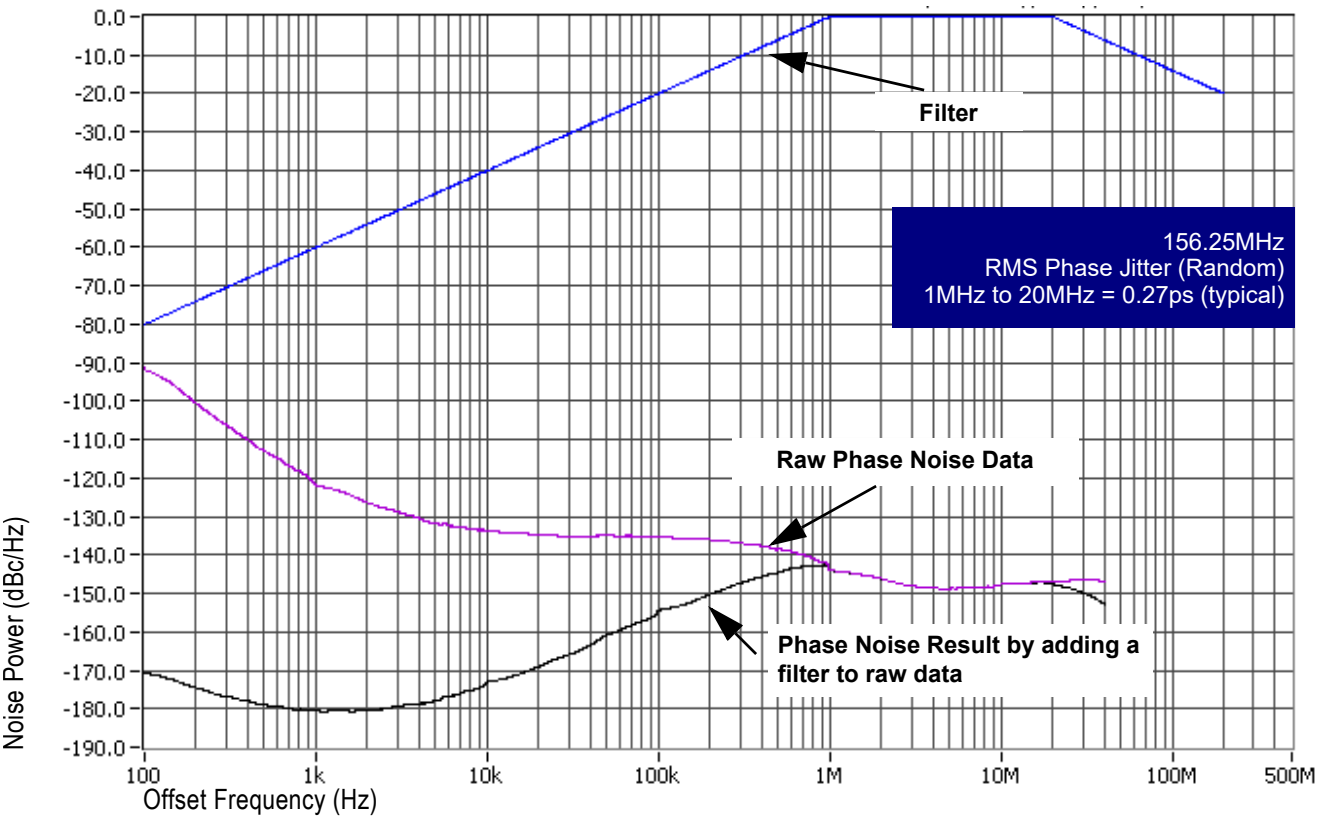
NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE: Characterized using a 25MHz crystal.
NOTE 1: Please refer to the phase noise plots.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential cross points.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 4: Defined as skew within a bank of outputs at the same voltage and with equal load conditions.
NOTE 5: Measurement taken from differential waveform.
NOTE 6: T_{STABLE} is the time the differential clock must maintain a minimum ±150mV differential voltage after rising/falling edges before it is allowed to drop back into the V_{RB} ±100mV differential range.
NOTE 7: Measurement taken from single ended waveform.
NOTE 8: Defined as the maximum instantaneous voltage including overshoot. See Parameter Measurement Information Section.
NOTE 9: Defined as the minimum instantaneous voltage including undershoot. See Parameter Measurement Information Section.
NOTE 10: Measured at crossing point where the instantaneous voltage value of the rising edge of Q equals the falling edge of nQ. See Parameter Measurement Information Section.
NOTE 11: Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement. See Parameter Measurement Information Section.
NOTE 12: Defined as the total variation of all crossing voltage of rising Q and falling nQ. This is the maximum allowed variance in the V_{CROSS} for any particular system. See Parameter Measurement Information Section.
NOTE 13: Measured from -150mV to +150mV on the differential waveform (derived from Q minus nQ). The signal must be monotonic through the measurement region for rise and fall time. The 300mV measurement window is centered on the differential zero crossing.

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Typical Phase Noise at 156.25MHz (3.3V)



Typical Phase Noise at 156.25MHz (3.3V)



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Parameter Measurement Information

Figure 1. 3.3V LVDS Output Load Test Circuit

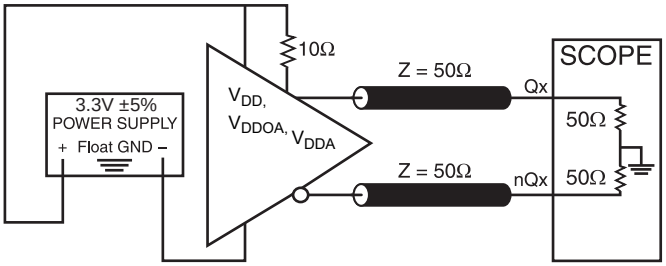


Figure 2. 3.3V HCSL Output Load Test Circuit

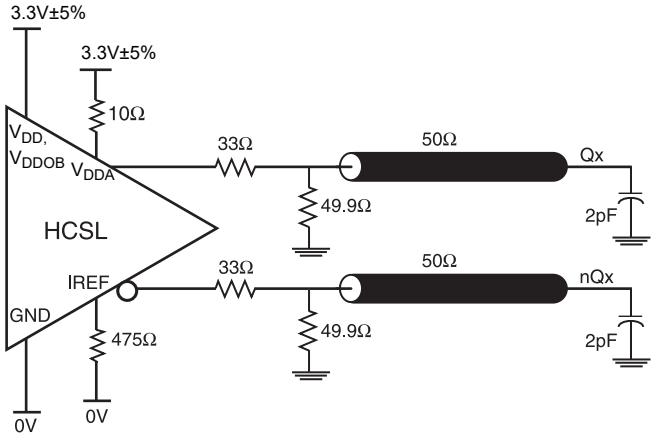


Figure 3. 2.5V HCSL Output Load Test Circuit

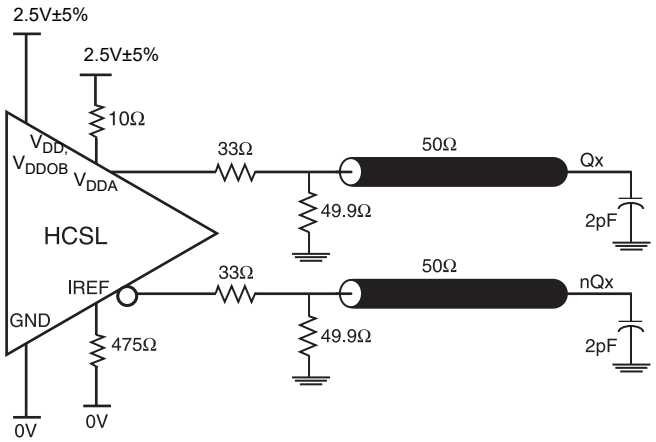


Figure 4. 2.5V LVDS Output Load Test Circuit

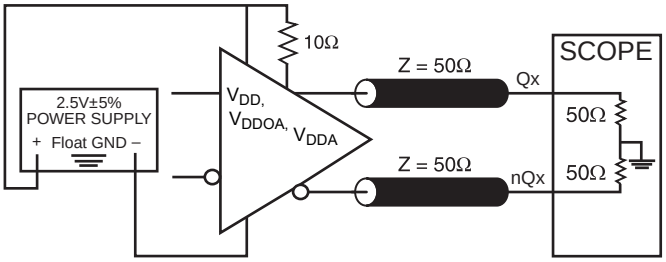
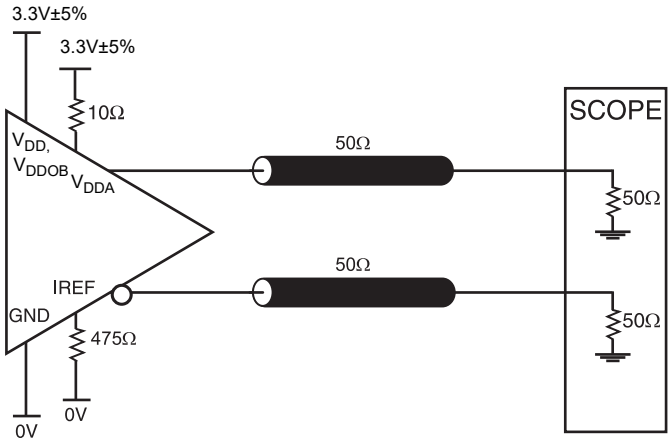
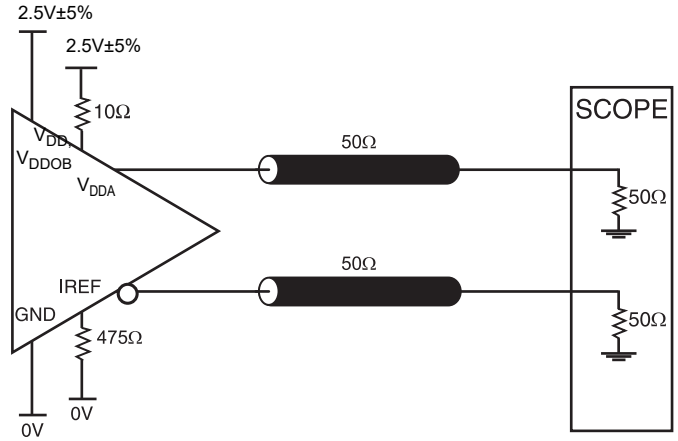


Figure 5. 3.3V HCSL Output Load Test Circuit



This load condition is used for $I_{DD,}$ tjit(Ø), tsk(b) and tsk(o) measurements.

Figure 6. 2.5V HCSL Output Load Test Circuit



This load condition is used for $I_{DD,}$ tjit(Ø), tsk(b) and tsk(o) measurements.

Figure 7. RMS Phase Jitter

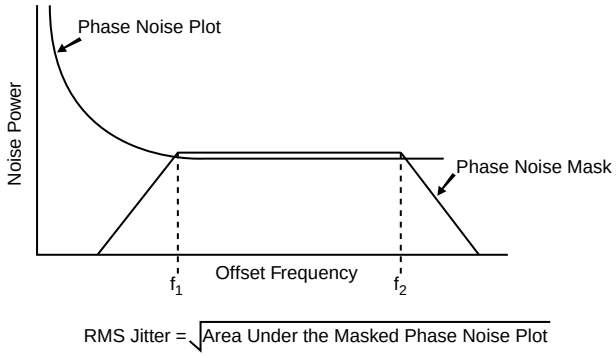


Figure 8. Output Skew

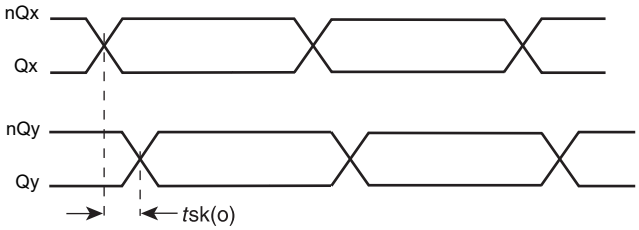


Figure 9. Differential Measurement Points for Ringback

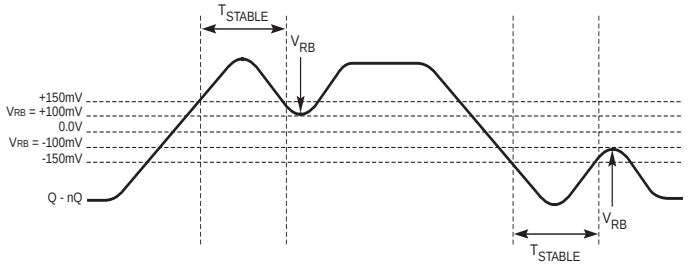
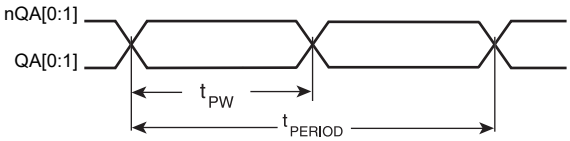
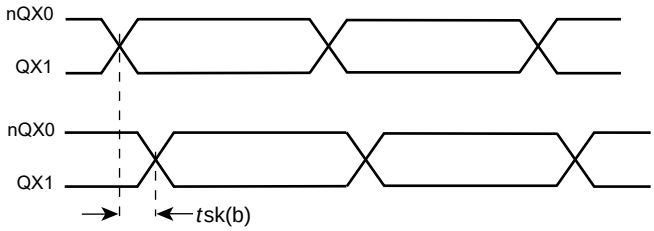


Figure 10. LVDS Output Duty Cycle/Pulse Width/Period



$$odc = \frac{t_{PW}}{t_{PERIOD}} \times 100\%$$

Figure 11. Bank Skew



Where X = Bank A or Bank B

Figure 12. Differential Measurement Points for Duty Cycle/Period

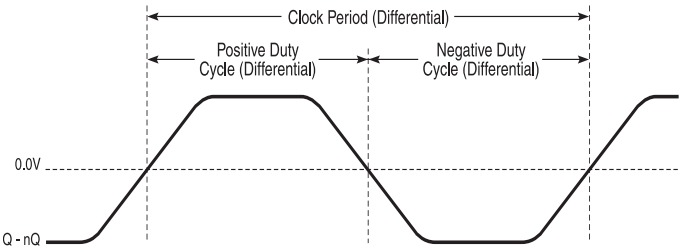


Figure 13. HCSL Differential Measurement Points for Rise/Fall Time

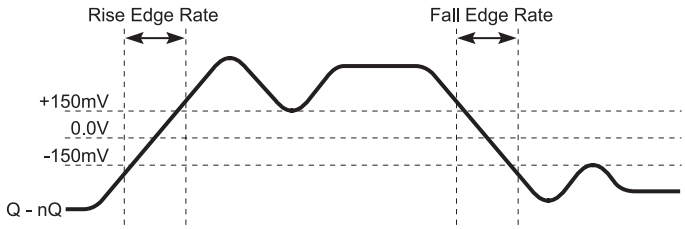


Figure 14. Single-ended Measurement Points for Delta Cross Point

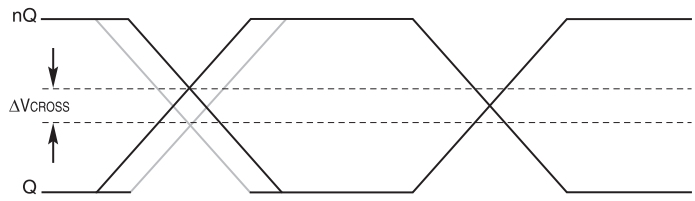


Figure 15. Offset Voltage Setup

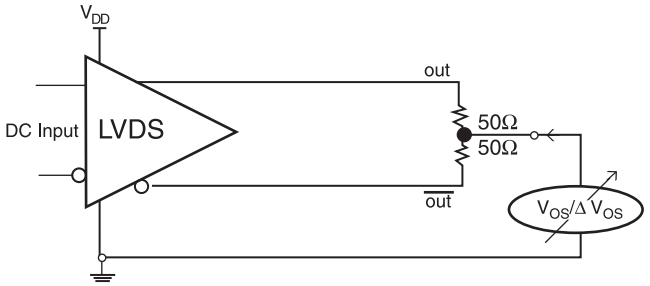


Figure 16. LVDS Rise/Fall Time

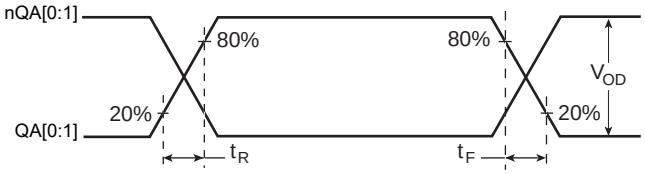


Figure 17. Single-ended Measurement Points for Absolute Cross Point/Swing

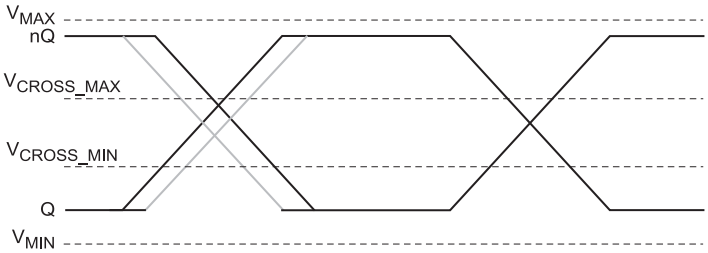
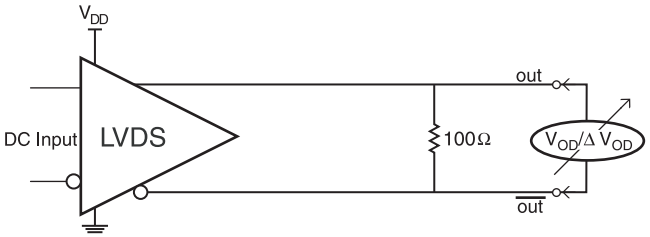


Figure 18. Differential Output Voltage Setup



Applications Information

Recommendations for Unused Input Pins

Inputs

REF_CLK Input

For applications not requiring the use of the reference clock, it can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from the REF_CLK to ground.

Crystal Inputs

For applications not requiring the use of the crystal oscillator input, both XTAL_IN and XTAL_OUT can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from XTAL_IN to ground.

LVCMOS Control Pins

All control pins have internal pulldowns; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs

LVDS Outputs

All unused LVDS output pairs can be either left floating or terminated with 100Ω across. If they are left floating, we recommend that there is no trace attached.

Differential Outputs

All unused differential outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

Interface to IDT S-RIO Switches

The 841N254B is designed for driving the differential reference clock input (REF_CLK) of IDT's S-RIO 1.3 and 2.0 switch devices. Both the LVDS and the HCSL outputs of the ICS841N254BI have the low-jitter, differential voltage and impedance characteristics required to provide a high-quality 156.25MHz clock signal for both S-RIO 1.3 and 2.0 switch devices. Please see Figure 19 and Figure 20 for suggested interfaces. The interfaces differ by the driving output, LVDS and HCSL, and the corresponding source termination method. In both figures, the AC-coupling capacitors are mandatory by the IDT S-RIO switch devices. The differential REF_CLK input is internally re-biased and AC-terminated. Both interface circuits are optimized for 50Ω transmission lines and generate the voltage swing required to reliably drive the clock reference input of a IDT S-RIO switch. Please refer to IDT's S-RIO device datasheet for more details.

Figure 19. LVDS-to-S-RIO 2.0 Reference Clock Interface

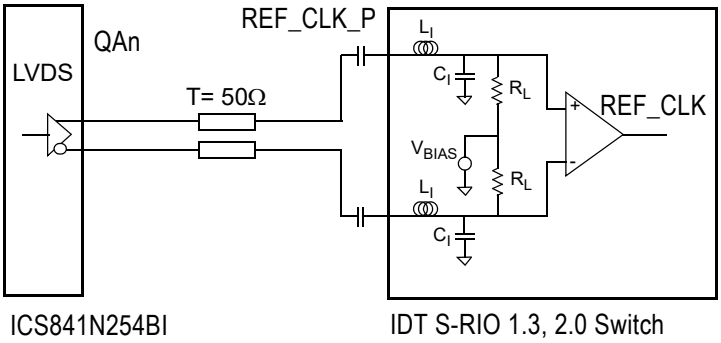
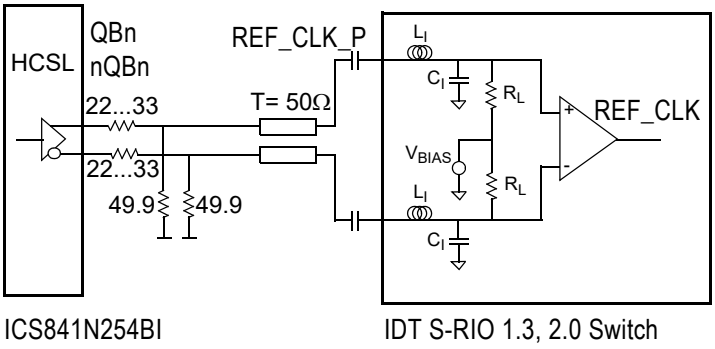


Figure 19 shows the recommended interface circuit for driving the 156.25MHz reference clock of an IDT S-RIO 2.0 switch by a LVDS output (QA0, QA1) of the ICS841N254BI. The LVDS-to-differential interface as shown in Figure 19 does not require any external termination resistors: the ICS841N254BI driver contains an internal source termination at QA0 and QA1. The differential REF_CLK input contains an internal AC-termination (R_L) and re-bias (V_{BIAS}).

Figure 20 shows the interface circuit for driving the 156.25MHz reference clock of an IDT S-RIO 2.0 switch by an HCSL output of the 841N254B (QB0, QB1): The HCSL-to-differential interface requires external termination resistors (22...33Ω and 50Ω) for source termination, which should be placed close the driver (QB0, QB1).

Figure 20. HCSL-to-S-RIO 2.0 Reference Clock Interface



Overdriving the XTAL Interface

The XTAL_IN input can be overdriven by an LVCMOS driver or by one side of a differential driver through an AC coupling capacitor. The XTAL_OUT pin can be left floating. The amplitude of the input signal should be between 500mV and 1.8V and the slew rate should not be less than 0.2V/nS. For 3.3V LVCMOS inputs, the amplitude must be reduced from full swing to at least half the swing in order to prevent signal interference with the power rail and to reduce internal noise. Figure 21 shows an example of the interface diagram for a high speed 3.3V LVCMOS driver. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance.

For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and changing R2 to 50Ω. The values of the resistors can be increased to reduce the loading for a slower and weaker LVCMOS driver. Figure 22 shows an example of the interface diagram for an LVPECL driver. This is a standard LVPECL termination with one side of the driver feeding the XTAL_IN input. It is recommended that all components in the schematics be placed in the layout. Though some components might not be used, they can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a quartz crystal as the input.

Figure 21. General Diagram for LVCMOS Driver to XTAL Input Interface

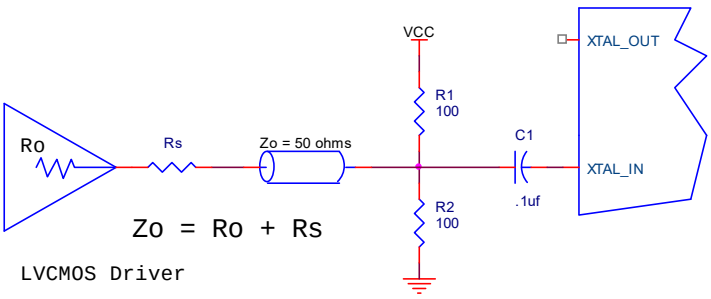
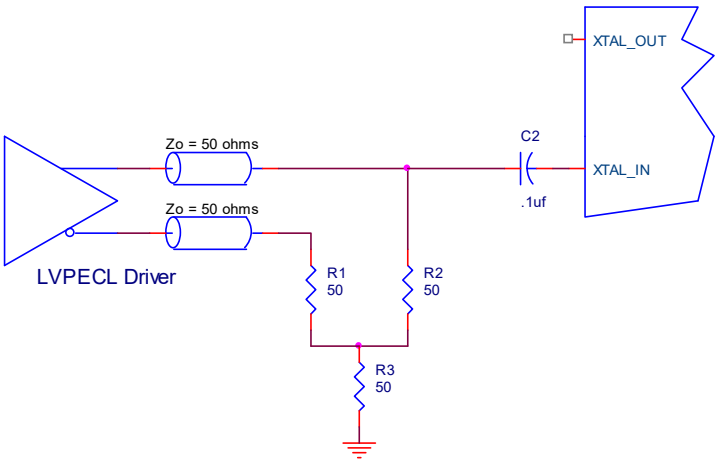


Figure 22. LVPECL Driver to XTAL Input Interface



HCSL Recommended Termination

Figure 23 is the recommended source termination for applications where the driver and receiver will be on a separate PCBs. This termination is the standard for PCI Express™ and HCSL output types. All traces should be 50Ω impedance single-ended or 100Ω differential

Figure 23. Recommended Source Termination (Where the driver and receiver will be on separate PCBs)

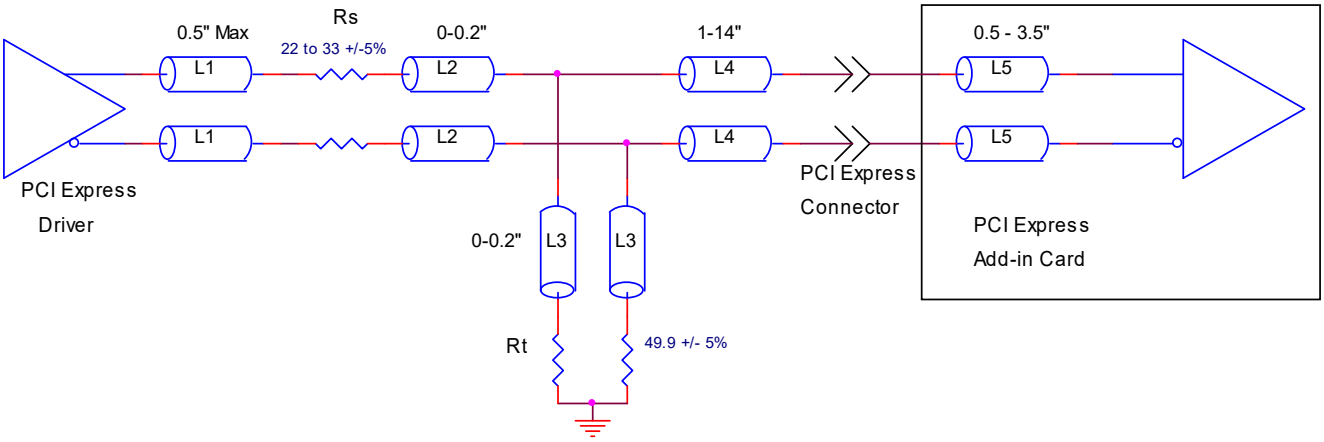
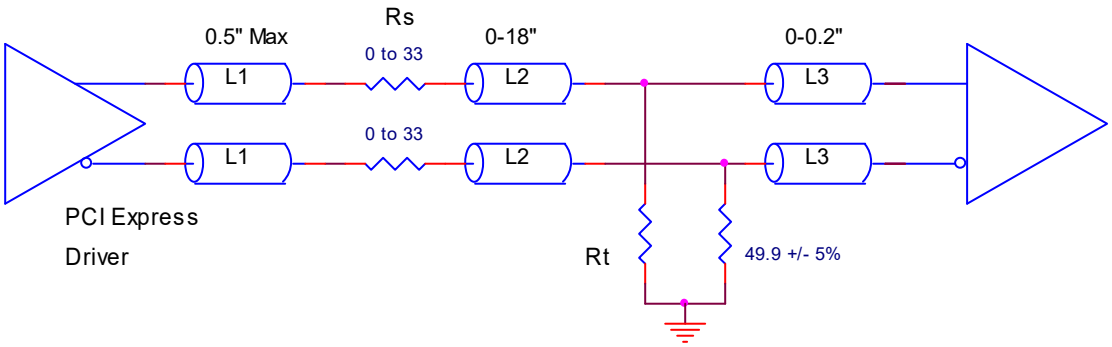


Figure 24 is the recommended termination for applications where a point-to-point connection can be used. A point-to-point connection contains both the driver and the receiver on the same PCB. With a matched termination at the receiver, transmission-line reflections will be minimized. In addition, a series resistor (Rs) at the driver offers flexibility and can help dampen unwanted reflections. The optional resistor can range from 0Ω to 33Ω. All traces should be 50Ω impedance single-ended or 100Ω differential.

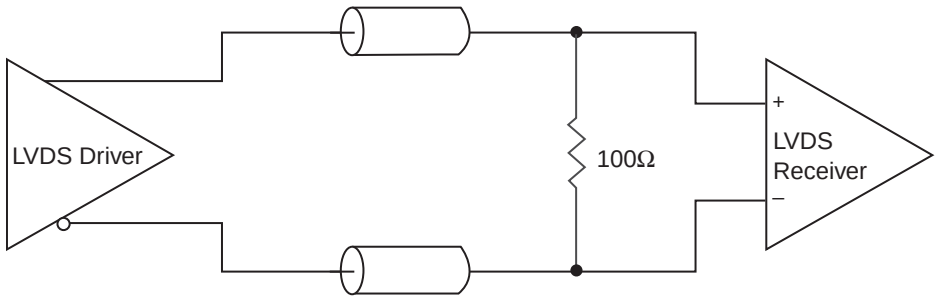
Figure 24. Recommended Termination (Where a point-to-point connection can be used)



LVDS Driver Termination

A general LVDS interface is shown in Figure 25. Standard termination for LVDS type output structure requires both a 100Ω parallel resistor at the receiver and a 100Ω differential transmission line environment. In order to avoid any transmission line reflection issues, the 100Ω resistor must be placed as close to the receiver as possible. IDT offers a full line of LVDS compliant devices with two types of output structures: current source and voltage source. The standard termination schematic as shown in Figure 25 can be used with either type of output structure. If using a non-standard termination, it is recommended to contact IDT and confirm if the output is a current source or a voltage source type structure. In addition, since these outputs are LVDS compatible, the amplitude and common mode input range of the input receivers should be verified for compatibility with the output.

Figure 25. Typical LVDS Driver Termination

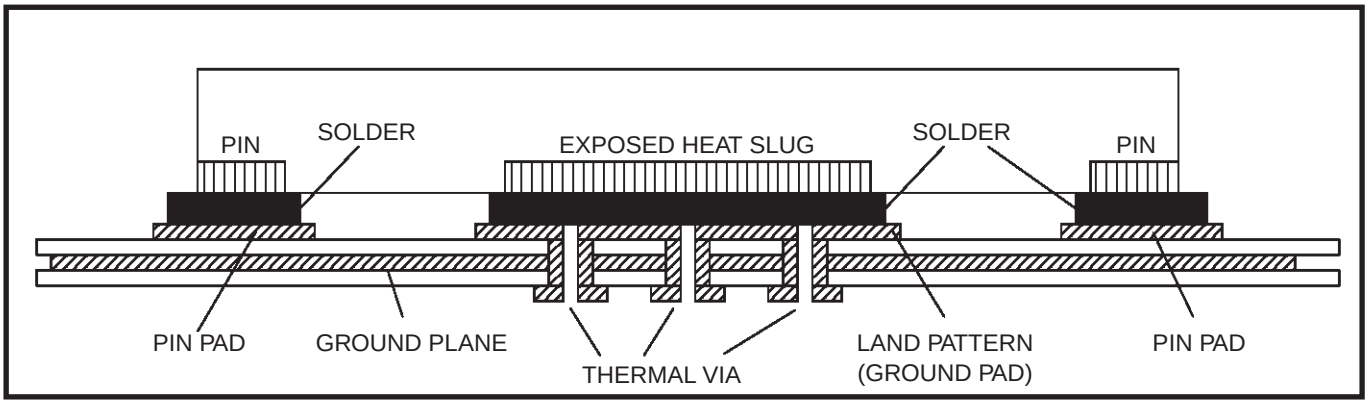


VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in Figure 26. The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor’s Thermally/ Electrically Enhance Leadframe Base Package, Amkor Technology.

Figure 26. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (Drawing not to scale)



Schematic Layout

Figure 27 shows an example of 841N254B application schematic. In this example, the device is operated at V_{DD} = V_{DDOA} = V_{DDOB} = 3.3V. The 12pF parallel resonant 25MHz crystal is used. The load capacitance C1 = 5pF and C2 = 5pF are recommended for frequency accuracy. Depending on the parasitic of the printed circuit board layout, these values might require a slight adjustment to optimize the frequency accuracy. Crystals with other load capacitance specifications can be used. This will require adjusting C1 and C2. For this device, the crystal load capacitors are required for proper operation.

As with any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The 841N254B provides separate power supplies to isolate any high switching noise from coupling into the internal PLL.

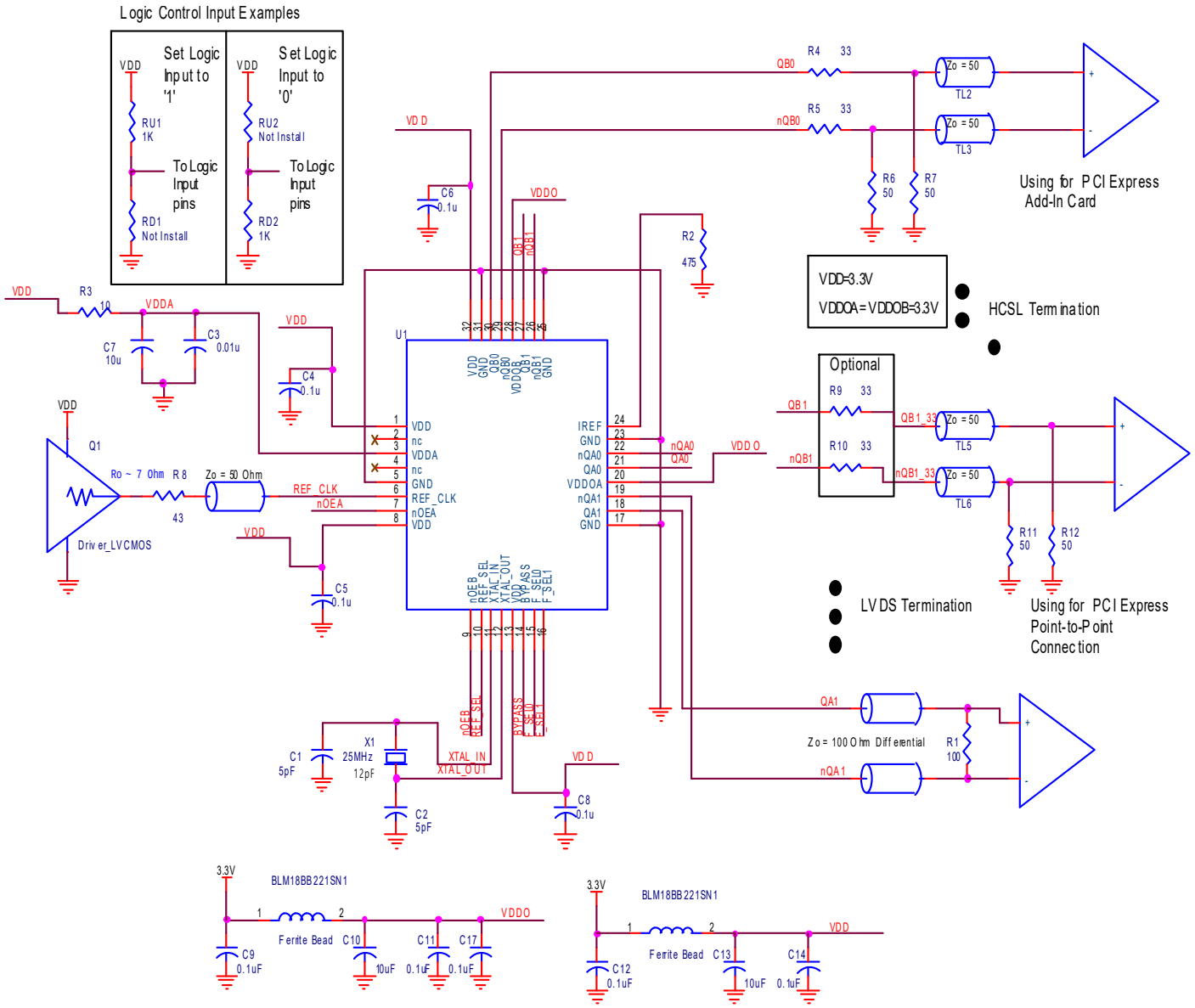
In order to achieve the best possible filtering, it is recommended that the placement of the filter components be on the device side of the PCB as close to the power pins as possible. If space is limited, the 0.1µF capacitor in each power pin filter should be placed on the device side. The other components can be on the opposite side of the PCB.

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Power supply filter recommendations are a general guideline to be used for reducing external noise from coupling into the devices. The filter performance is designed for a wide range of noise frequencies. This low-pass filter starts to attenuate noise at approximately 10kHz. If a specific frequency noise component is known, such as switching power supplies frequencies, it is recommended that component values be adjusted and if required, additional filtering be added. Additionally, good general design practices for power plane voltage stability suggests adding bulk capacitance in the local area of all devices.

The schematic example focuses on functional connections and is not configuration specific. Refer to the pin description and functional tables in the datasheet to ensure that the logic control inputs are properly set.

Figure 27. 841N254B Application Schematic



Power Considerations

This section provides information on power dissipation and junction temperature for the 841N254B.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the 841N254B is the sum of the core power plus the analog power plus the power dissipated in the load(s). The following is the power dissipation for V_{DD} = 3.3V + 5% = 3.465V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power $(core)_{MAX} = V_{DD_MAX} * (I_{DD_MAX} + I_{DDA_MAX} + I_{DDOA\&B_MAX})$ = 3.465V *(113mA + 30mA + 72mA) = 744.98mW
- Power $(HCSL_output)_{MAX}$ = 44.5mW * 2 = 89.0mW

Total $Power_{MAX}$ = (3.465V, with all outputs switching) = 744.98mW + 89.0mW = 833.98mW

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad, and directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 37.7°C/W per Table 14.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.834W * 37.7°C/W = 116.4°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 14. Thermal Resistance θ_{JA} for 32-Lead VFQFN, Forced Convection

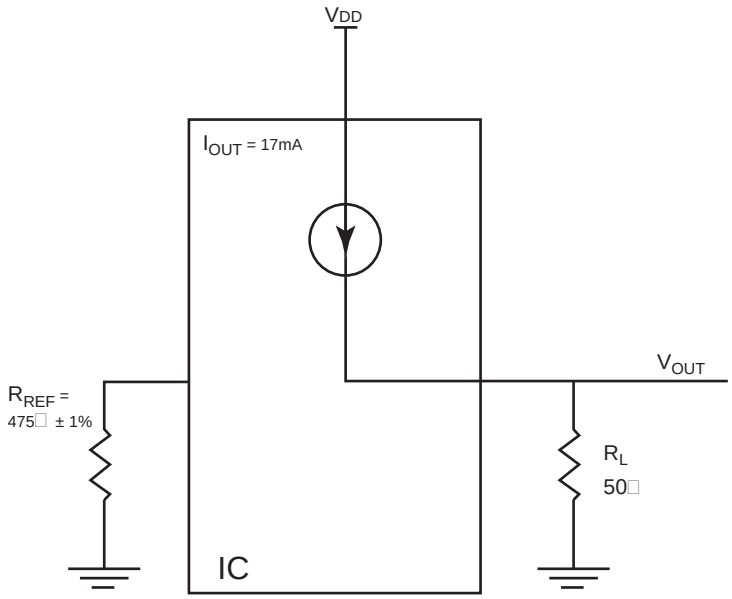
θ_{JA} Vs. Air Flow			
Meters per Second	0	1	2.5
Multi-Layer PCB, JEDEC Standard Test Boards	37.7°C/W	32.9°C/W	29.5°C/W

3. Calculations and Equations.

The purpose of this section is to calculate power dissipation on the IC per HCSL output pair.

HCSL output driver circuit and termination are shown in Figure 28.

Figure 28. HCSL Driver Circuit and Termination



HCSL is a current steering output which sources a maximum of 17mA of current per output. To calculate worst case on-chip power dissipation, use the following equations which assume a 50Ω load to ground.

The highest power dissipation occurs when $V_{DD–MAX}$.

Power= $(V_{DD_MAX} – V_{OUT}) * I_{OUT}$, since $V_{OUT} – I_{OUT} * R_L$

= $(V_{DD_MAX} – I_{OUT} * R_L) * I_{OUT}$

= (3.465V – 17mA * 50Ω) * 17mA

Total Power Dissipation per output pair = 44.5mW

Reliability Information

Table 15. θ_{JA} vs. Air Flow Table for a 32-lead VFQFN

θ_{JA} vs. Air Flow			
Meters per Second	0	1	2.5
Multi-Layer PCB, JEDEC Standard Test Boards	37.7°C/W	32.9°C/W	29.5°C/W

Transistor Count

The transistor count for 841N254B is: 23,445

Package Outline Drawings

The package outline drawings are appended at the end of this document and are accessible from the link below. The package information is the most current data available.

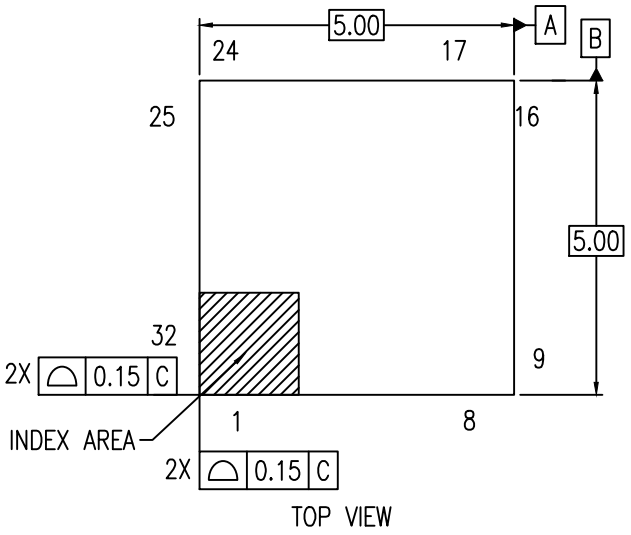
www.idt.com/document/psc/nlnlg-32-package-outline-50-x-50-mm-body-epad-315-x-315-050-mm-pitch-qfn

Ordering Information

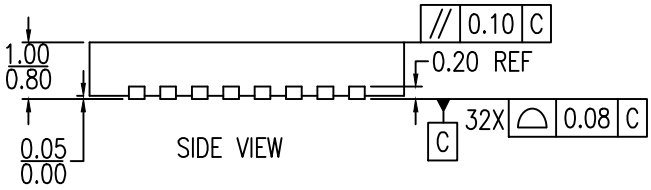
Orderable Part Number	Marking	Package	Carrier Type	Temperature
841N254BKILF	ICS1N254BIL	Lead-Free 32-Lead VFQFN	Tray	-40°C to 85°C
841N254BKILFT	ICS1N254BIL	Lead-Free 32-Lead VFQFN	Tape and Reel	-40°C to 85°C

Revision History

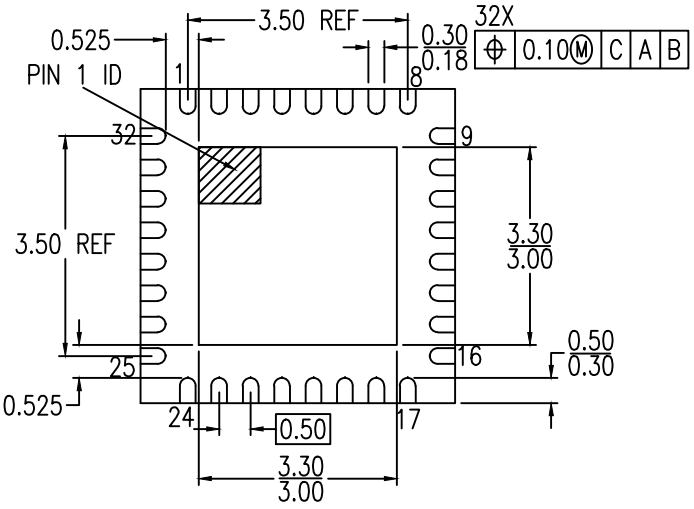
Revision Date	Description of Change
April 17, 2018	Updated the package out drawings; however, no technical changes Completed other minor changes throughout the document
May 23, 2016	Updated datasheet header/footer. Deleted “ICS” prefix from part number throughout the datasheet.
November 4, 2013	Replacement part for ICS841N254AKI, per PCN# N1309-01.



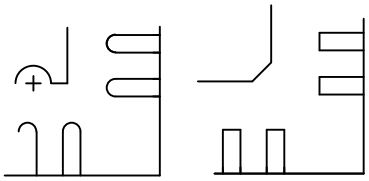
TOP VIEW



SIDE VIEW



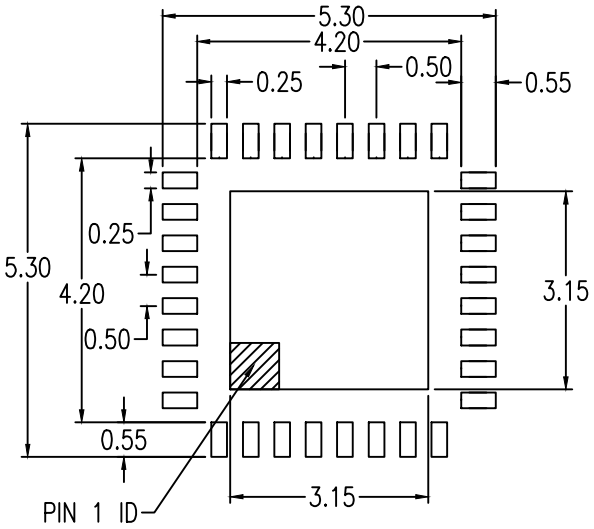
BOTTOM VIEW



PIN #1 ID OPTION

NOTE:
1. ALL DIMENSION ARE IN MM. ANGLES IN DEGREES.
2. COPLANARITY APPLIE TO THE EXPOSED PAD AS WELL AS THE TERMINALS. COPLANARITY SHALL NOT EXCEED 0.08 MM.
3. WARPAGE SHALL NOT EXCEED 0.10 MM.
4. PIN LOCATION IS UNDENTIFIED BY EITHER CHAMFER OR NOTCH.

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RECOMMENDED LAND PATTERN DIMENSION

1. ALL DIMENSIONS ARE IN MM. ANGLES IN DEGREES.
2. TOP DOWN VIEW. AS VIEWED ON PCB.
3. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

Package Revision History		
Date Created	Rev No.	Description
April 12, 2018	Rev 02	New Format
Feb 8, 2016	Rev 01	Added "k: Value

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