General Description

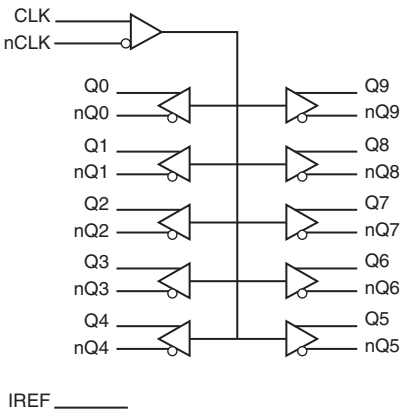
The ICS851010I is a 1-to-10 Differential HCSL Fanout Buffer. The ICS851010I is designed to translate any differential signal levels to differential HCSL output levels. An external reference resistor is used to set the value of the current supplied to an external load. The load resistor value is chosen to equal the value of the characteristic line impedance of 50Ω. The ICS851010I is characterized at an operating supply voltage of 3.3V.

The differential HCSL outputs, accurate crossover voltage and symmetric duty cycle makes the ICS851010I ideal for interfacing to PCI Express and FBDIMM applications.

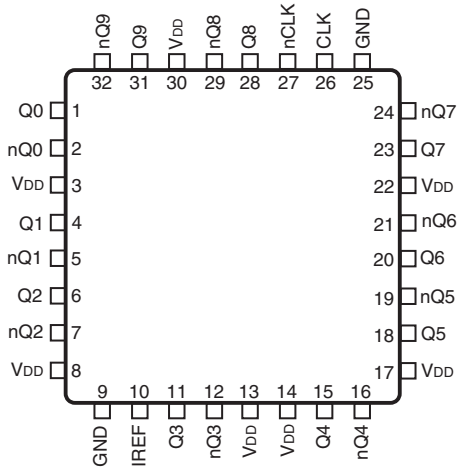
Features

- Ten differential HCSL outputs
- Translates any differential input signal (LVPECL, LVHSTL, LVDS, HCSL) to HCSL levels without external bias networks
- Maximum output frequency: 250MHz
- Output skew: 165ps (maximum)
- Output drift: 140ps (maximum)
- V_{OH}: 850mV (maximum)
- Additive phase jitter, RMS: 0.19ps (typical)
- Full 3.3V supply voltage
- Available in lead-free (RoHS 6) package
- -40°C to 85°C ambient operating temperature

Block Diagram



Pin Assignment



ICS851010I

32-Lead TQFP, E-Pad
7mm x 7mm x1mm package body
Y Package
Top View

© 2019 Renesas Electronics Corporation

Table 1. Pin Descriptions

Number	Name	Type	Description
1, 2	Q0, nQ0	Output	Differential output pair. Differential HCSL interface levels.
3, 8, 13, 14, 17, 22, 30	V_{DD}	Power	Positive supply pins.
4, 5	Q1, nQ1	Output	Differential output pair. Differential HCSL interface levels.
6, 7	Q2, nQ2	Output	Differential output pair. Differential HCSL interface levels.
9, 25	GND	Power	Power supply ground.
10	IREF	Input	Reference current input. Used to set the output current. Connect to 950Ω resistor to ground.
11, 12	Q3, nQ3	Output	Differential output pair. Differential HCSL interface levels.
15, 16	Q4, nQ4	Output	Differential output pair. Differential HCSL interface levels.
18, 19	Q5, nQ5	Output	Differential output pair. Differential HCSL interface levels.
20, 21	Q6, nQ6	Output	Differential output pair. Differential HCSL interface levels.
23, 24	Q7, nQ7	Output	Differential output pair. Differential HCSL interface levels.
26	CLK	Input	Non-inverting differential input.
27	nCLK	Input	Inverting differential clock input.
28, 29	Q8, nQ8	Output	Differential output pair. Differential HCSL interface levels.
31, 32	Q98, nQ9	Output	Differential output pair. Differential HCSL interface levels.

Output Driver Current

The ICS851010I outputs are HCSL differential current drive with the current being set with a resistor from I_{REF} to ground. For a *single load* and a 50Ω pc board trace, the drive current would typically be set with a R_{REF} of 950Ω which products an I_{REF} of 1.16mA. The I_{REF} is multiplied by a current mirror to an output drive of 12*1.16mA or 13.90mA. See *Figure 1* for current mirror and output drive details.

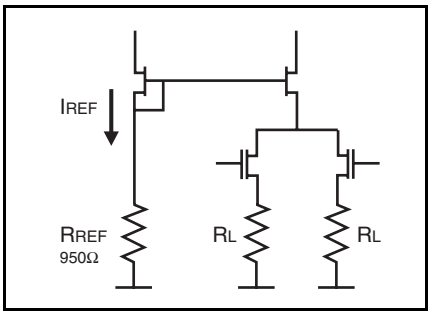


Figure 1. HCSL Current Mirror and Output Drive

© 2019 Renesas Electronics Corporation

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5V
Outputs, I_O	-0.5V to V_{DD} + 0.5V
Package Thermal Impedance, θ_{JA}	32.2°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 2A. Power Supply DC Characteristics, V_{DD} = 3.3V±5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current; NOTE 1				105	mA

NOTE 1: Measured using 200MHz input frequency.

Table 2B. Differential DC Characteristics, V_{DD} = 3.3V±5%, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	CLK, nCLK	$V_{DD} = V_{IN}$ = 3.465V			5	µA
I_{IL}	Input Low Current	CLK, nCLK	V_{DD} = 3.465V, V_{IN} = 0V			5	µA
V_{PP}	Peak-to-Peak Voltage; NOTE 1			0.15		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			GND + 0.5		V_{DD} – 0.85	V

NOTE 1: V_{IL} should not be less than -0.3V.
NOTE 2: Common mode input voltage is defined as V_{IH}.

© 2019 Renesas Electronics Corporation

AC Electrical Characteristics

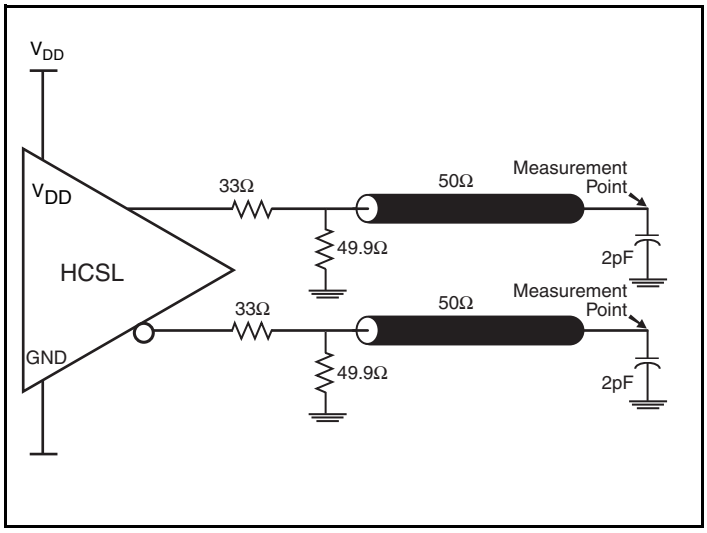
Table 3. HCSL AC Characteristics, V_{DD} = 3.3V±5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				250	MHz
t_{PD}	Propagation Delay, NOTE 1	Measured on at V_{OX}	1.5		2.75	ns
*t*sk(o)	Output Skew; NOTE 2, 3	Measured on at V_{OX}			165	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 3, 4				800	ps
*t*jit	Buffer Additive Phase Jitter, RMS	CLK = 155.52MHz, Integration Range: 12kHz – 20MHz		0.19		ps
*t*sk(drift)	Output Drift; NOTE 5				140	ps
V_{MAX}	Absolute Max Output Voltage; NOTE 6	$f \leq$ 150MHz	500		850	mV
V_{MIN}	Absolute Min Output Voltage; NOTE 6	$f \leq$ 150MHz	-150		150	mV
V_{CROSS}	Absolute Crossing Voltage; NOTE 7, 8, 9		250		550	mV
ΔV_{CROSS}	Total Variation of V_{CROSS} over all edges; NOTE 7, 8, 10				140	mV
t_R / t_F	Rise/Fall Edge Rate; NOTE 11, 12		0.6		4.0	V/ns
odc	Output Duty Cycle; NOTE 13		47		53	%

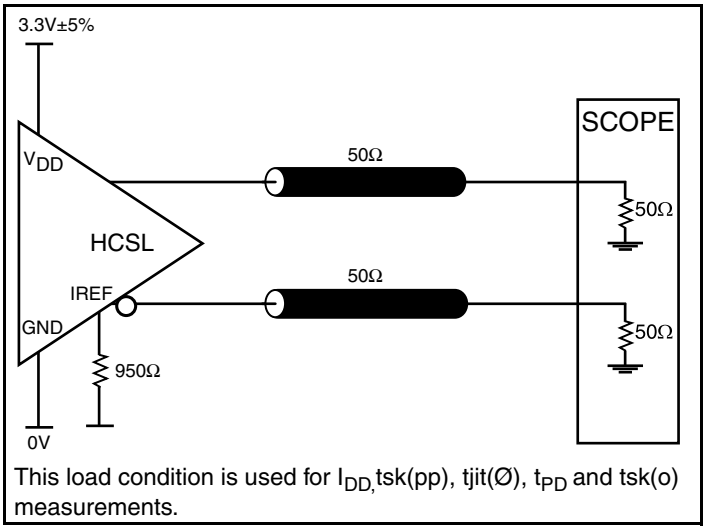
NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE: Current adjust set for V_{OH} = 0.7V. Measurements refer to PCIEX outputs only.
NOTE: Characterized using an R_{REF} value of 950Ω resistor.
NOTE 1: Measured from the differential input cross point to the differential output crossing point.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the differential output cross point.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 4: Defined as skew between outputs on different devices operating at the same supply voltage, same frequency, same temperature and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross point.
NOTE 5: Output Drift is measured as the change in the time placement of the differential cross point for each output on a given device due to a change in temperature and supply voltage. Measured at the differential cross point.
NOTE 6: Measurement using R_{REF} = to 950Ω, R_{LOAD} = to 50Ω.
NOTE 7: Measurement taken from single-ended waveform.
NOTE 8: Measured at crossing point where the instantaneous voltage value of the rising edge of Qx equals the falling edge of nQx. See Parameter Measurement Information Section.
NOTE 9: Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement. See Parameter Measurement Information Section.
NOTE 10: Defined as the total variation of all crossing voltage of rising Qx and falling nQx. This is the maximum allowed variance in the V_{CROSS} for any particular system. See Parameter Measurement Information Section.
NOTE 11: Measurement taken from differential waveform.
NOTE 12: Measurement from -150mV to +150mV on the differential waveform (derived from Qx minus nQx). The signal must be monotonic through the measurement region for rise and fall time. The 300mV measurement window is centered on the differential zero crossing.
NOTE 13: Assuming 50% input duty cycle. Data taken at $f \leq$ 200MHz, unless otherwise specified.

© 2019 Renesas Electronics Corporation

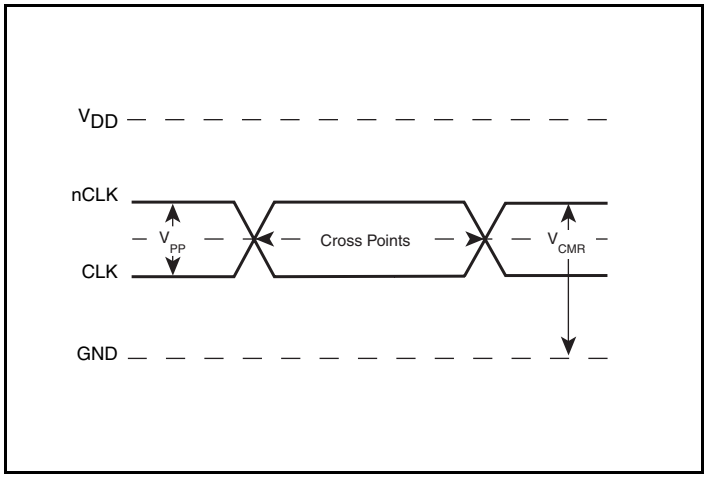
Parameter Measurement Information



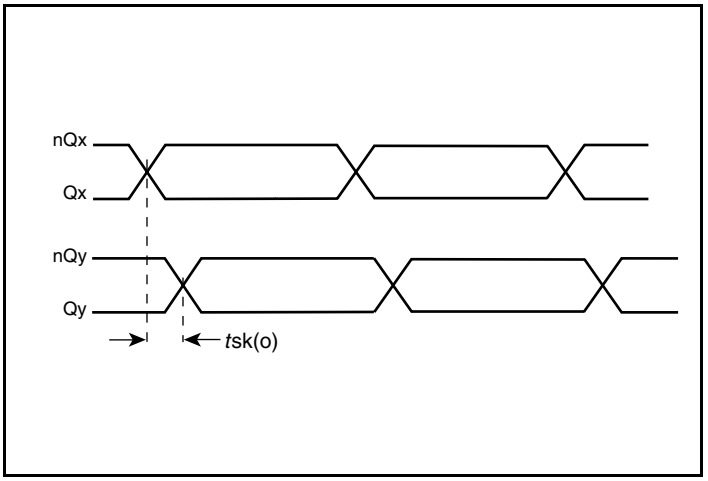
HCSL Output Load AC Test Circuit



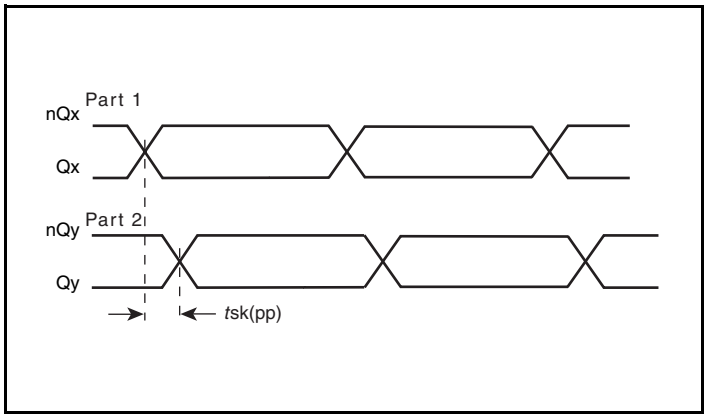
HCSL Output Load AC Test Circuit



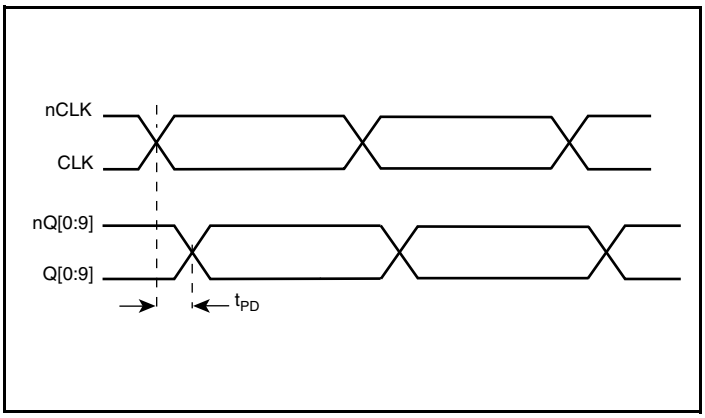
Differential Input Levels



Output Skew



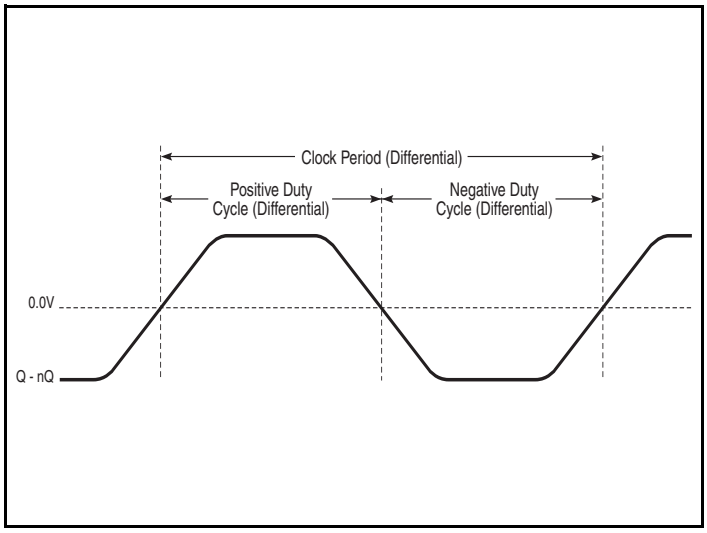
Part-to-Part Skew



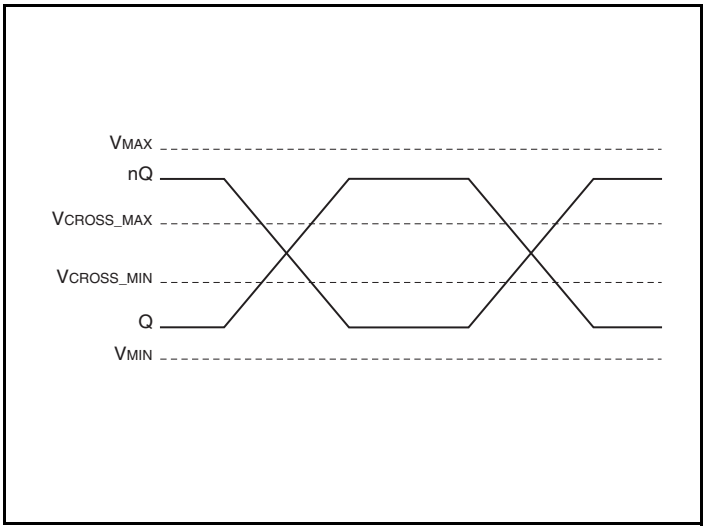
Propagation Delay

© 2019 Renesas Electronics Corporation

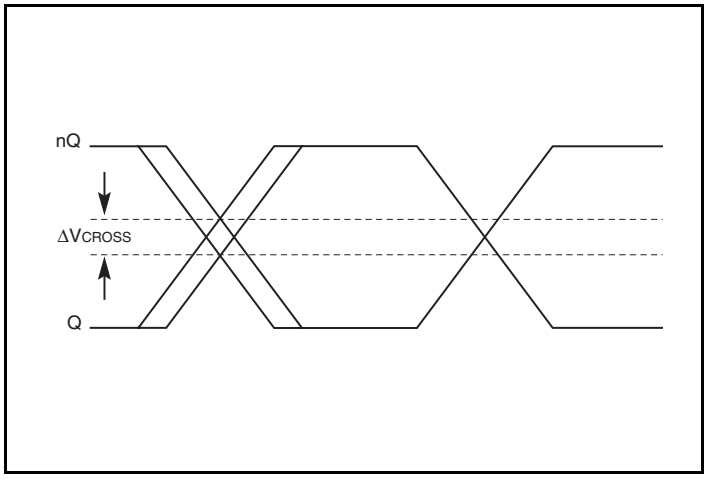
Parameter Measurement Information, continued



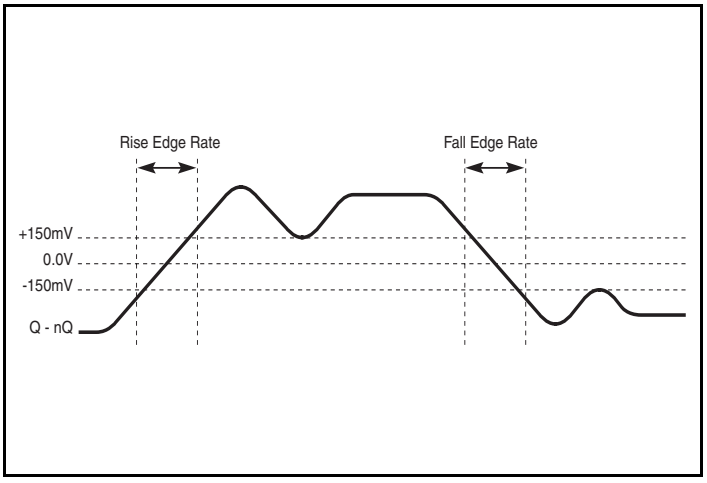
Differential Measurement Points for Duty Cycle/Period



Single-ended Measurement Points for Absolute Cross Point and Swing



Single-ended Measurement Points for Delta Cross Point



Differential Measurement Points for Rise/Fall Edge Rate

© 2019 Renesas Electronics Corporation

Applications Information

Recommendations for Unused Output Pins

Outputs:

Differential Outputs

All unused differential outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

Wiring the Differential Input to Accept Single-Ended Levels

Figure 2 shows how a differential input can be wired to accept single ended levels. The reference voltage $V_{REF} = V_{DD}/2$ is generated by the bias resistors R1 and R2. The bypass capacitor (C1) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of R1 and R2 might need to be adjusted to position the V_{REF} in the center of the input voltage swing. For example, if the input clock swing is 2.5V and V_{DD} = 3.3V, R1 and R2 value should be adjusted to set V_{REF} at 1.25V. The values below are for when both the single ended swing and V_{DD} are at the same voltage. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways. First, R3 and R4 in parallel should equal the transmission line impedance. For most 50Ω applications, R3 and R4 can be 100Ω. The values of the resistors can be increased to reduce the loading for slower and weaker LVCMOS driver. When using single-ended signaling, the noise rejection benefits of differential signaling are reduced. Even though the differential input can handle full rail LVCMOS signaling, it is recommended that the amplitude be reduced. The datasheet specifies a lower differential amplitude, however this only applies to differential signals. For single-ended applications, the swing can be larger, however V_{IL} cannot be less than -0.3V and V_{IH} cannot be more than V_{DD} + 0.3V. Though some of the recommended components might not be used, the pads should be placed in the layout. They can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a differential signal.

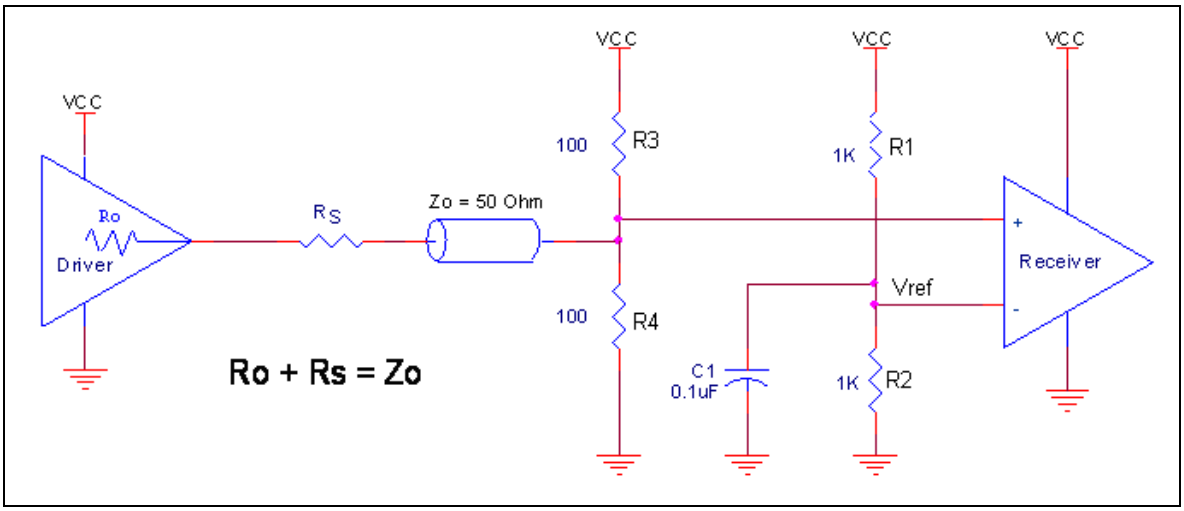


Figure 2. Recommended Schematic for Wiring a Differential Input to Accept Single-ended Levels

© 2019 Renesas Electronics Corporation

Differential Clock Input Interface

The CLK/nCLK accepts HCSL, LVDS, LVPECL and SSTL and other differential signals. Both differential signals must meet the V_{PP} and V_{CMR} input requirements. *Figures 3A to 3F* show interface examples for the CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example in Figure 3A, the input termination applies for IDT open emitter LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

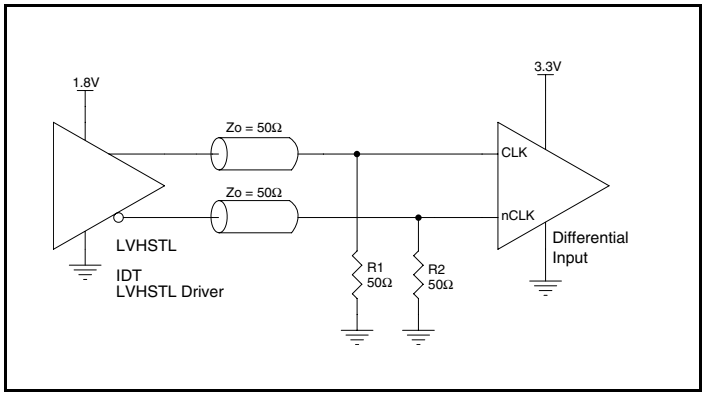


Figure 3A. CLK/nCLK Input Driven by an IDT Open Emitter LVHSTL Driver

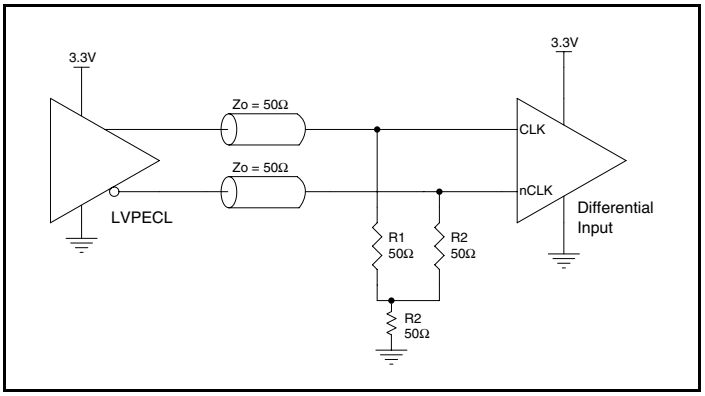


Figure 3B. CLK/nCLK Input Driven by a 3.3V LVPECL Driver

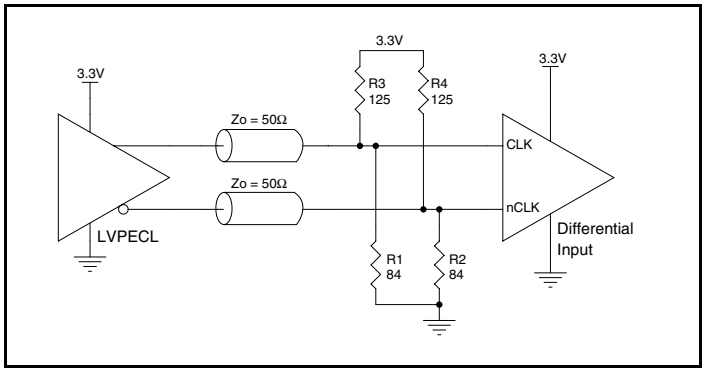


Figure 3C. CLK/nCLK Input Driven by a 3.3V LVPECL Driver

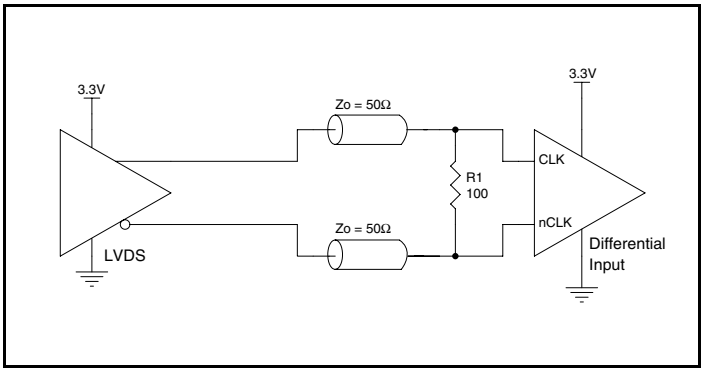


Figure 3D. CLK/nCLK Input Driven by a 3.3V LVDS Driver

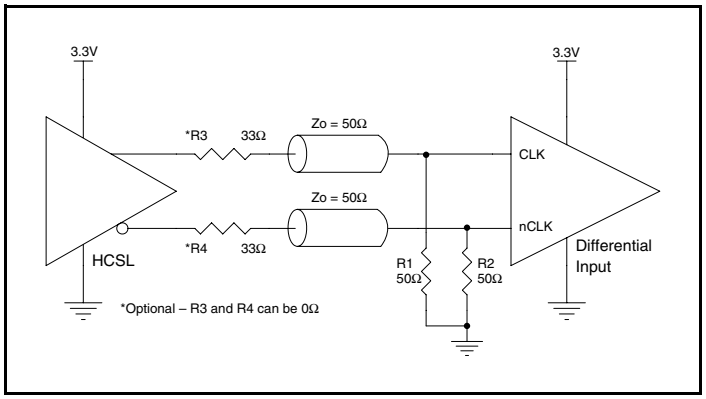


Figure 3E. CLK/nCLK Input Driven by a 3.3V HCSL Driver

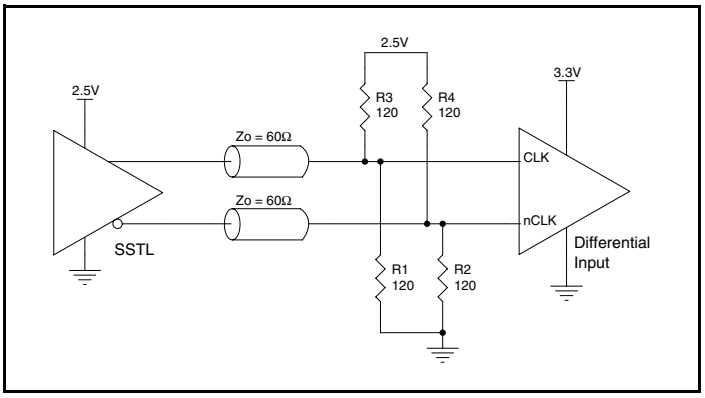


Figure 3F. CLK/nCLK Input Driven by an SSTL Driver

© 2019 Renesas Electronics Corporation

EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 4.* The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, refer to the Application Note on the *Surface Mount Assembly* of Amkor’s Thermally/Electrically Enhance Leadframe Base Package, Amkor Technology.

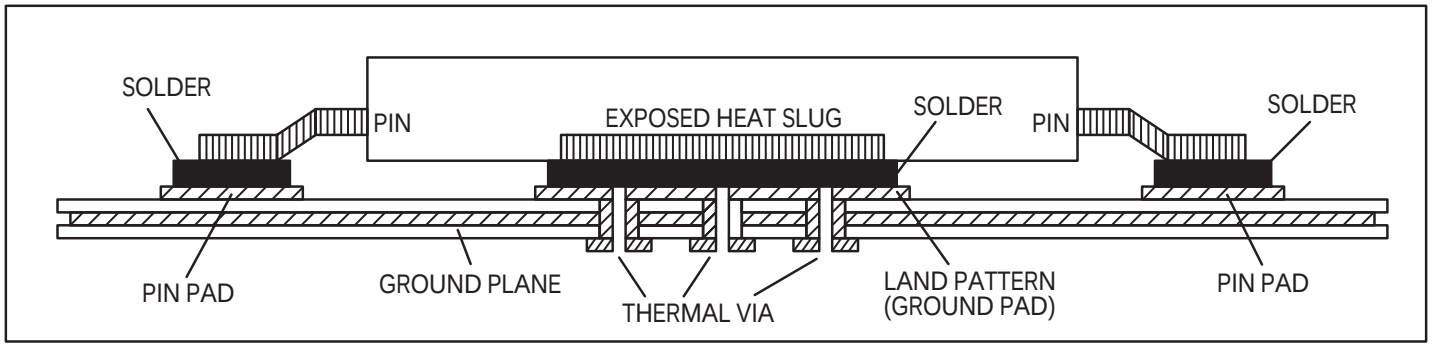


Figure 4. Assembly for Exposed Pad Thermal Release Path - Side View (drawing not to scale)

© 2019 Renesas Electronics Corporation

Recommended Termination

Figure 5A is the recommended termination for applications which require the receiver and driver to be on a separate PCB. All traces should be 50Ω impedance.

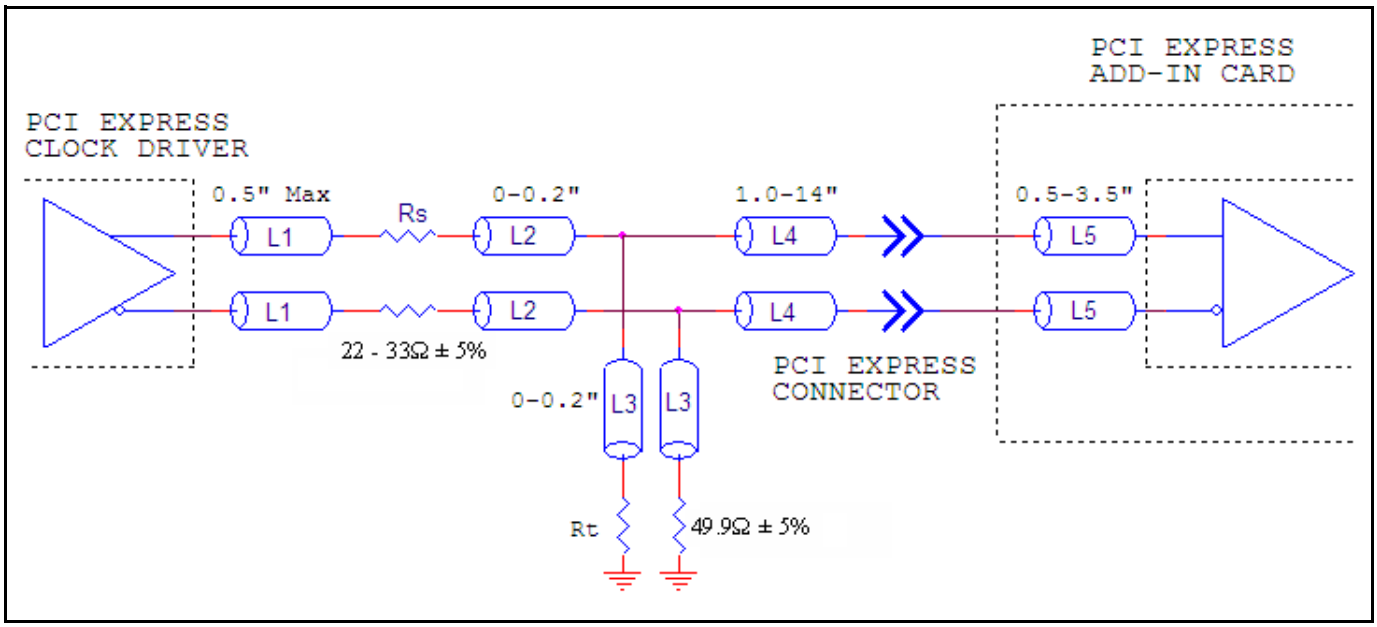


Figure 5A. Recommended Termination

Figure 5B is the recommended termination for applications which require a point to point connection and contain the driver and receiver on the same PCB. All traces should all be 50Ω impedance.

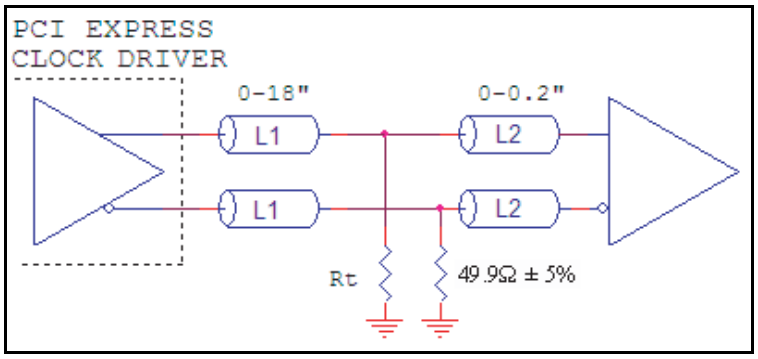


Figure 5B. Recommended Termination

© 2019 Renesas Electronics Corporation

Power Considerations

This section provides information on power dissipation and junction temperature for the ICS851010I.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS851010I is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for V_{DD} = 3.3V + 5% = 3.465V, which gives worst case results.

- Power $(core)_{MAX} = V_{DD_MAX} * I_{DD_MAX}$ = 3.465V * 105mA = **363.825mW**
- Power $(outputs)_{MAX}$ = **44.5mW/Loaded Output Pair**
  If all outputs are loaded, the total power is 10 * 44.5mW = **445mW**

Total Power$_{_MAX}$ (3.465V, with all outputs switching) = 363.825mW + 445mW = **808.825mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 32.2°C/W per Table 4 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.809W * 32.2°C/W = 111°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 4. Thermal Resistance θ_{JA} for 32 Lead TQFP, E-Pad, Forced Convection

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	32.2°C/W	26.3°C/W	24.7°C/W

© 2019 Renesas Electronics Corporation

The purpose of this section is to calculate power dissipation on the IC per HCSL output pair.

HCSL output driver circuit and termination are shown in *Figure 6.*

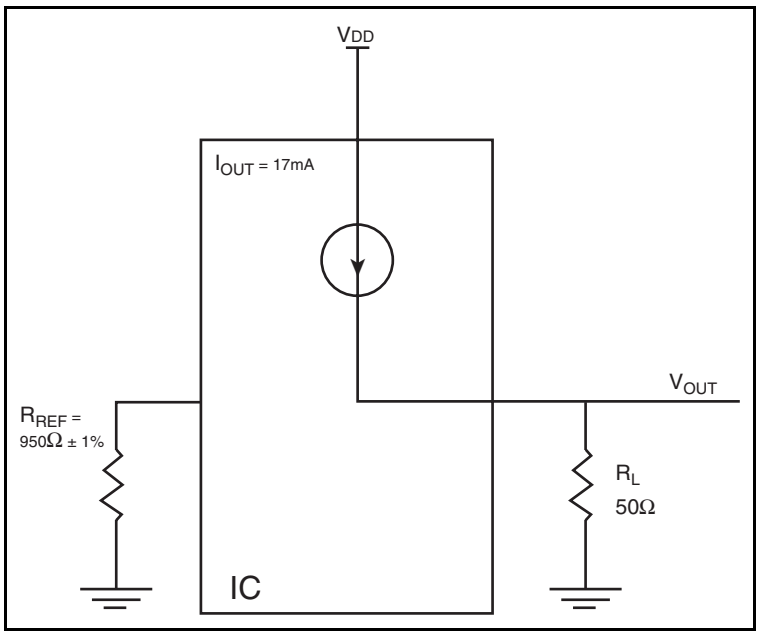


Figure 6. HCSL Driver Circuit and Termination

HCSL is a current steering output which sources a maximum of 17mA of current per output. To calculate worst case on-chip power dissipation, use the following equations which assume a 50Ω load to ground.

The highest power dissipation occurs when V_{DD_MAX}.

Power = $(V_{DD_MAX} - V_{OUT}) * I_{OUT}$,
since $V_{OUT} - I_{OUT} * R_L$

= $(V_{DD_MAX} - I_{OUT} * R_L) * I_{OUT}$

= (3.465V – 17mA * 50Ω) * 17mA

Total Power Dissipation per output pair = **44.5mW**

© 2019 Renesas Electronics Corporation

Reliability Information

Table 5. θ_{JA} vs. Air Flow Table for a 32 Lead TQFP, E-Pad

θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	32.2°C/W	26.3°C/W	24.7°C/W

Transistor Count

The transistor count for ICS851010I is: 843

© 2019 Renesas Electronics Corporation

Package Outline and Package Dimensions

Package Outline - Y Suffix for 32 Lead TQFP, E-Pad

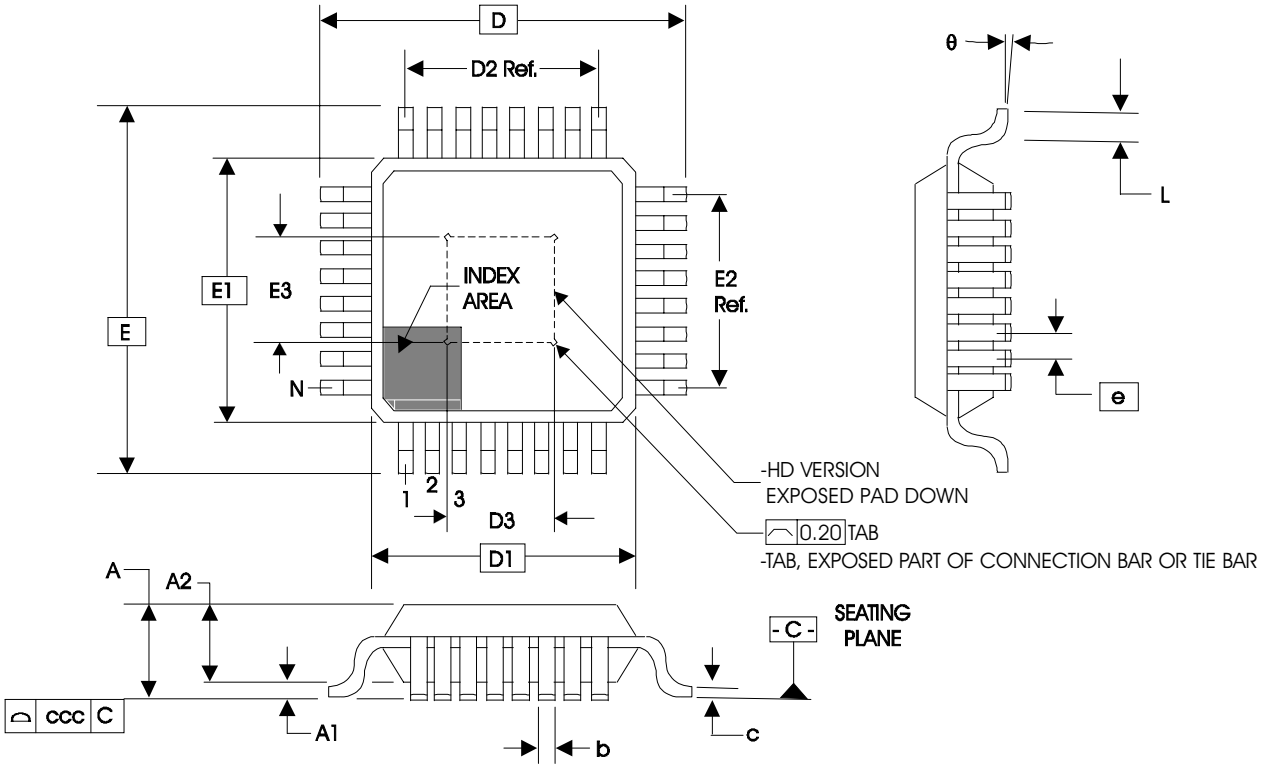


Table 6. Package Dimensions 32 Lead TQFP, E-Pad

JEDEC Variation: ABC - HD All Dimensions in Millimeters			
Symbol	**Minimum**	**Nominal**	**Maximum**
N		32	
A			1.20
A1	0.05	0.10	0.15
A2	0.95	1.00	1.05
b	0.30	0.35	0.40
c	0.09		0.20
D & E		9.00 Basic	
D1 & E1		7.00 Basic	
D2 & E2		5.60 Ref.	
D3 & E3	3.0		4.0
e		0.80 Basic	
L	0.45	0.60	0.75
θ	0°		7°
ccc			0.10

Reference Document: JEDEC Publication 95, MS-026

© 2019 Renesas Electronics Corporation

Ordering Information

Table 7. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
851010AYILF	ICS851010AIL	Lead-Free, 32 Lead TQFP, E-Pad	Tray	-40°C to 85°C
851010AYILFT	ICS851010AIL	Lead-Free, 32 Lead TQFP, E-Pad	1000 Tape & Reel	-40°C to 85°C

NOTE: Parts that are ordered with an “LF” suffix to the part number are the Pb-Free configuration and are RoHS compliant

© 2019 Renesas Electronics Corporation

Revision History Sheet

Rev	Table	Page	Description of Change	Date
A		2 7 14	Corrected *Output Driver Current.* Updated *Wiring the Differential Input to Accept Single-ended Levels.* Updated *Package Outline.* Converted datasheet format.	7/21/10
A		5	Parameter Measurement Information - corrected label names on output skew and part-to-part skew.	8/2/10

© 2019 Renesas Electronics Corporation

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers skilled in the art designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only for development of an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising out of your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Rev.1.0 Mar 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
www.renesas.com/contact/

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

© 2020 Renesas Electronics Corporation. All rights reserved.