Low Skew, 1-to-16 Differential-to-LVDS Clock Distribution Chip

ICS8516

DATASHEET

General Description

The ICS8516 is a low skew, high performance 1-to-16 Differential-to-LVDS Clock Distribution Chip. The ICS8516 CLK, nCLK pair can accept any differential input levels and translates them to 3.3V LVDS output levels. Utilizing Low Voltage Differential Signaling (LVDS), the ICS8516 provides a low power, low noise, point-to-point solution for distributing clock signals over controlled impedances of 100Ω.

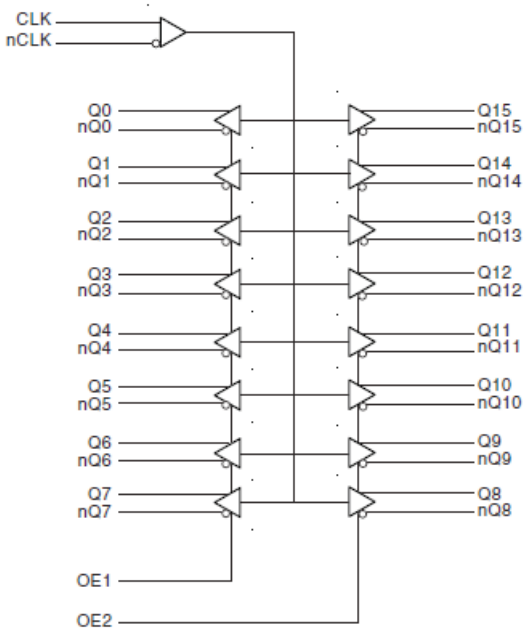
Dual output enable inputs allow the ICS8516 to be used in a 1-to-16 or 1-to-8 input/output mode.

Guaranteed output and part-to-part skew specifications make the ICS8516 ideal for those applications demanding well defined performance and repeatability.

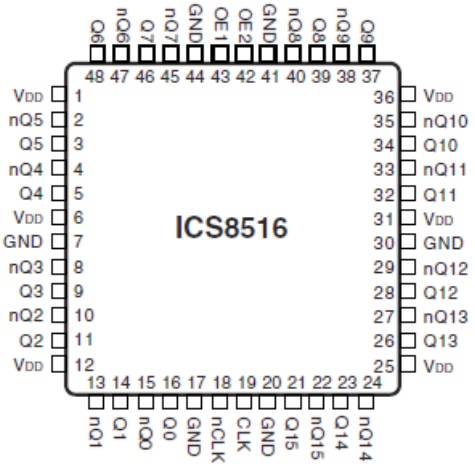
Features

- Sixteen differential LVDS outputs
- CLK, nCLK pair can accept the following differential input levels: LVPECL, LVDS, LVHSTL, HCSL, SSTL
- Maximum output frequency: 700MHz
- Translates any differential input signal (LVPECL, LVHSTL, SSTL, DCM) to LVDS levels without external bias networks
- Translates any single-ended input signal to LVDS with resistor bias on nCLK input
- Multiple output enable inputs for disabling unused outputs in reduced fanout applications
- LVDS compatible
- Output skew: 90ps (maximum)
- Part-to-part skew: 500ps (maximum)
- Propagation delay: 2.4ns (maximum)
- Additive phase jitter, RMS: 148fs (typical)
- 3.3V operating supply
- 0°C to 70°C ambient operating temperature
- Available in lead-free RoHS compliant package

Block Diagram



Pin Assignment



48-Lead LQFP
7mm x 7mm x 1.4mm body package
Y Package
Top View

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TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1, 6, 12, 25, 31, 36	V_{DD}	Power		Positive supply pins.
2, 3	nQ5, Q5	Output		Differential output pair. LVDS interface levels.
4, 5	nQ4, Q4	Output		Differential output pair. LVDS interface levels.
7, 17, 20, 30, 41, 44	GND	Power		Power supply ground.
8, 9	nQ3, Q3	Output		Differential output pair. LVDS interface levels.
10, 11	nQ2, Q2	Output		Differential output pair. LVDS interface levels.
13, 14	nQ1, Q1	Output		Differential output pair. LVDS interface levels.
15, 16	nQ0, Q0	Output		Differential output pair. LVDS interface levels.
18	nCLK	Input	Pullup	Inverting differential clock input.
19	CLK	Input	Pulldown	Non-inverting differential clock input.
21, 22	Q15, nQ15	Output		Differential output pair. LVDS interface levels.
23, 24	Q14, nQ14	Output		Differential output pair. LVDS interface levels.
26, 27	Q13, nQ13	Output		Differential output pair. LVDS interface levels.
28, 29	Q12, nQ12	Output		Differential output pair. LVDS interface levels.
32, 33	Q11, nQ11	Output		Differential output pair. LVDS interface levels.
34, 35	Q10, nQ10	Output		Differential output pair. LVDS interface levels.
37, 38	Q9, nQ9	Output		Differential output pair. LVDS interface levels.
39, 40	Q8, nQ8	Output		Differential output pair. LVDS interface levels.
42, 43	OE2, OE1	Input	Pullup	Output enable. OE2 controls outputs Q8, nQ8 thru Q15, nQ15; OE1 controls outputs Q0, nQ0 thru Q7, nQ7. LVCMOS/LVTTL interface levels.
45, 46	nQ7, Q7	Output		Differential output pair. LVDS interface levels.
47, 48	nQ6, Q6	Output		Differential output pair. LVDS interface levels.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

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TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ
C_{PD}	Power Dissipation Capacitance (per output)			4		pF

TABLE 3A. CONTROL INPUT FUNCTION TABLE

Inputs		Outputs			
OE1	OE2	Q0:Q7	nQ0:nQ7	Q8:Q15	nQ8:nQ15
0	0	Hi Z	Hi Z	Hi Z	Hi Z
1	0	ACTIVE	ACTIVE	Hi Z	Hi Z
0	1	Hi Z	Hi Z	ACTIVE	ACTIVE
1	1	ACTIVE	ACTIVE	ACTIVE	ACTIVE

In the active mode, the state of the outputs are a function of the CLK and nCLK inputs as described in Table 3B.

TABLE 3B. CLOCK INPUT FUNCTION TABLE

Inputs		Outputs		Input to Output Mode	Polarity
CLK	nCLK	Q0:Q15	nQ0:nQ15		
0	1	LOW	HIGH	Differential to Differential	Non Inverting
1	0	HIGH	LOW	Differential to Differential	Non Inverting
0	Biased; NOTE 1	LOW	HIGH	Single Ended to Differential	Non Inverting
1	Biased; NOTE 1	HIGH	LOW	Single Ended to Differential	Non Inverting
Biased; NOTE 1	0	HIGH	LOW	Single Ended to Differential	Inverting
Biased; NOTE 1	1	LOW	HIGH	Single Ended to Differential	Inverting

NOTE 1: Please refer to the Application Information section, “Wiring the Differential Input to Accept Single Ended Levels”.

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Absolute Maximum Ratings

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5 V
Outputs, V_O	-0.5V to V_{DD} + 0.5V
Package Thermal Impedance, θ_{JA}	47.9°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Table 4A. Power Supply DC Characteristics, V_{DD} = 3.3V±5%, TA = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Positive Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Static Power Supply Current	RL = 100Ω		135	165	mA
		No Load		60	75	mA

Table 4B. LVCMOS/LVTTL DC Characteristics, V_{DD} = 3.3V±5%, TA = 0°C to 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	OE1, OE2		2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage	OE1, OE2		-0.3		0.8	V
I_{IH}	Input High Current	OE1, OE2	$V_{DD} = V_{IN}$ = 3.465V			5	µA
I_{IL}	Input Low Current	OE1, OE2	V_{DD} = 3.465V, V_{IN} = 0V	-150			µA

Table 4C. Differential DC Characteristics, V_{DD} = 3.3V±5%, TA = 0°C to 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	CLK	$V_{IN} = V_{DD}$ = 3.465V			150	µA
		nCLK	$V_{IN} = V_{DD}$ = 3.465V			5	µA
I_{IL}	Input Low Current	CLK	V_{DD} = 3.465V, V_{IN} = 0V	-5			µA
		nCLK	V_{DD} = 3.465V, V_{IN} = 0V	-150			µA
V_{PP}	Peak-to-Peak Voltage			0.15		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			GND + 0.5		V_{DD} - 0.85	V

NOTE 1: For single ended applications, the maximum input voltage for CLK, nCLK is V_{DD} + 0.3V.
NOTE 2: Common mode voltage is defined ast V_{IH}.

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TABLE 4D. LVDS DC CHARACTERISTICS, V_{DD} = 3.3V±5%, T_A = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage		250	400	600	mV
ΔV_{OD}	V_{OD} Magnitude Change				50	mV
V_{OS}	Offset Voltage		1.125	1.4	1.6	V
ΔV_{OS}	V_{OS} Magnitude Change				50	mV
I_{OZ}	High Impedance Leakage Current		-10		+10	µA
I_{OFF}	Power Off Leakage		-1		+1	µA
I_{OSD}	Differential Output Short Circuit Current				-5.5	mA
I_{OS}/I_{OSB}	Output Short Circuit Current				-12	mA

TABLE 5. AC CHARACTERISTICS, V_{DD} = 3.3V±5%, T_A = 0°C TO 70°C

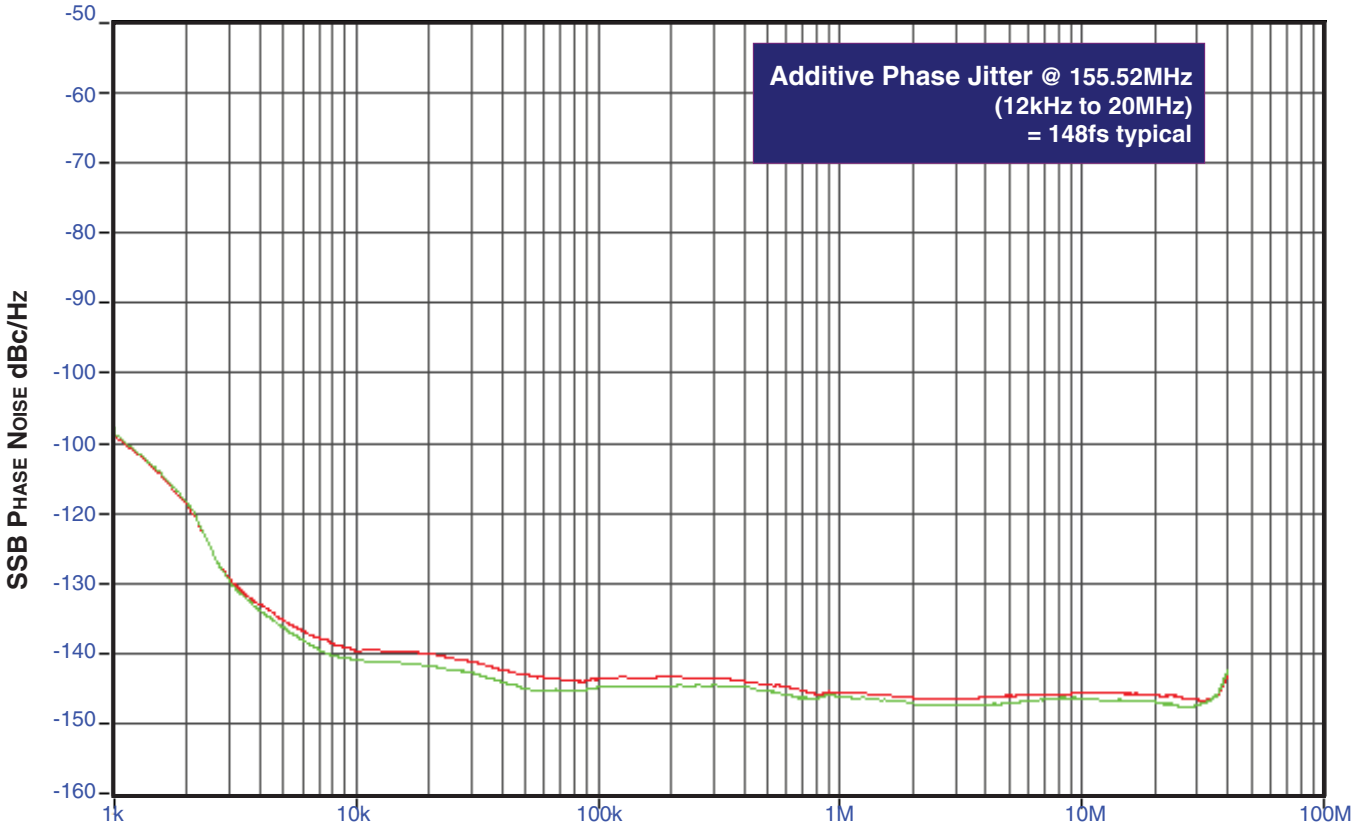
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				700	MHz
t_{PD}	Propagation Delay; NOTE 1		1.6	2.0	2.4	ns
*t*sk(o)	Output Skew; NOTE 2, 4				90	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 3, 4				500	ps
*t*jit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section	Integration Range: 12kHz - 20MHz		148		fs
t_R/t_F	Output Rise/Fall Time	20% to 80%	100		550	ps
odc	Output Duty Cycle		45	50	55	%
t_{PZL}, t_{PZH}	Output Enable Time; NOTE 5				5	ns
t_{PLZ}, t_{PHZ}	Output Disable Time; NOTE 5				5	ns

NOTE 1: Measured from the differential input crossing point to the differential output crossing point.
NOTE 2: Defined as skew between outputs at the same supply voltages and with equal load conditions. Measured at the output differential cross points.
NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 5: These parameters are guaranteed by characterization. Not tested in production.

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Additive Phase Jitter

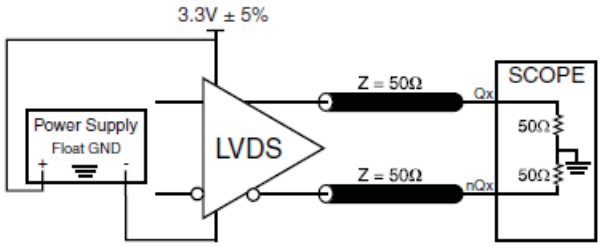
The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the ***dBc Phase Noise.*** This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a ***dBc*** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.



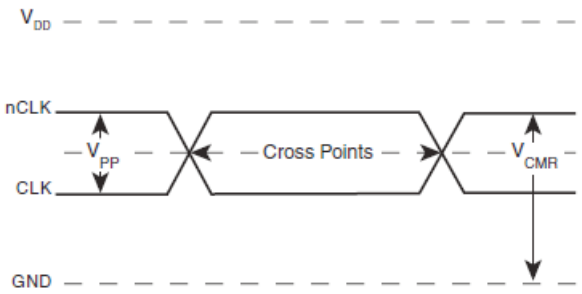
As with most timing specifications, phase noise measurements have issues. The primary issue relates to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This is illustrated above. The device meets the noise floor of what is shown, but can actually be lower. The phase noise is dependant on the input source and measurement equipment.

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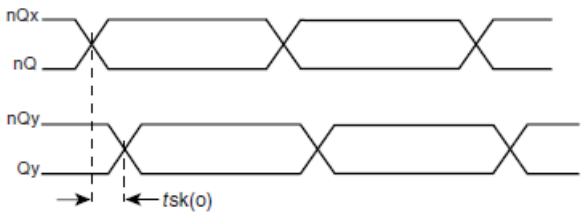
PARAMETER MEASUREMENT INFORMATION



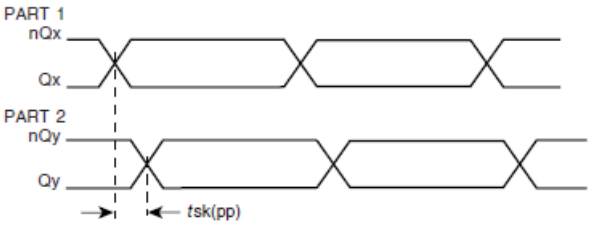
3.3V OUTPUT LOAD AC TEST CIRCUIT



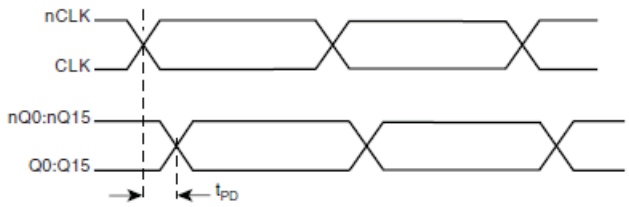
DIFFERENTIAL INPUT LEVEL



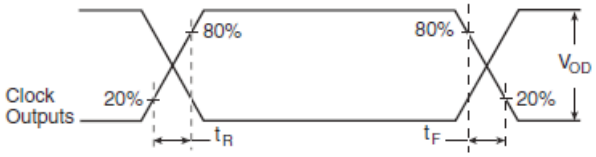
OUTPUT SKEW



PART-TO-PART SKEW

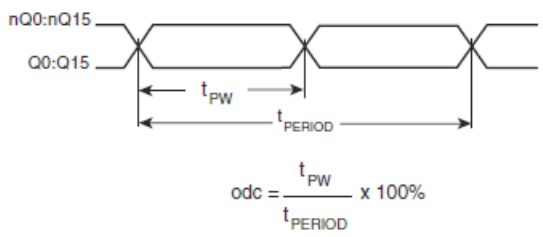


PROPAGATION DELAY

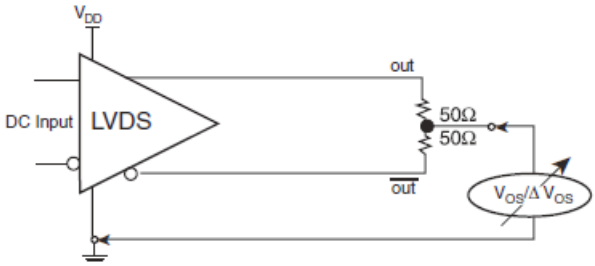


OUTPUT RISE/FALL TIME

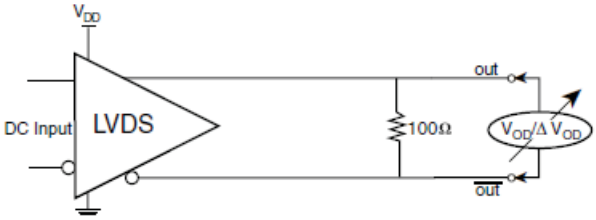
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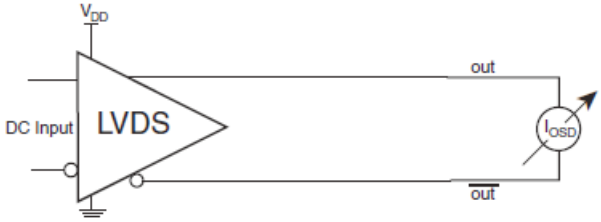
Output Duty Cycle/Pulse Width/Period



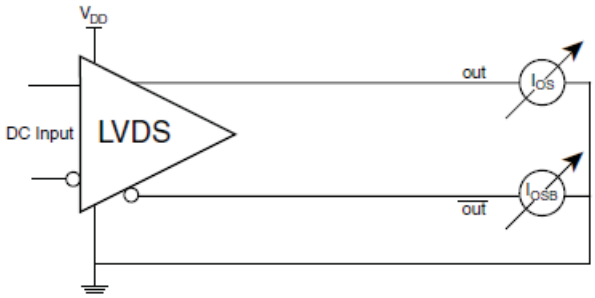
Offset Voltage Setup



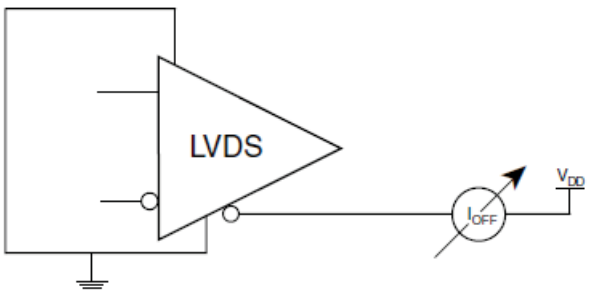
Differential Output Voltage Setup



Differential Output Short circuit Current Setup



Output Short Circuit Current Setup



Power Off Leakage Setup

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Application Information

Wiring the Differential Input to Accept Single Ended Levels

Figure 1 shows how the differential input can be wired to accept single ended levels. The reference voltage V_REF = V_{DD}/2 is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and V_{DD}= 3.3V, V_REF should be 1.25V and R2/R1 = 0.609.

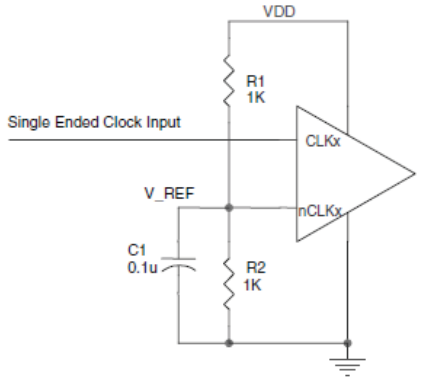


Figure 1. Single Ended Signal Driving Differential Input

Recommendations for Unused Input and Output Pins

Inputs:

LVCMOS Control Pins:

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs:

LVDS – Like Output

All unused LVDS output pairs can be either left floating or terminated with 100Ω across. If they are left floating, we recommend that there is no trace attached.

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Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, SSTL, HCSL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. Figures 2A to 2E show interface examples for the HiPerClockS CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example in *Figure 2A,* the input termination applies for ICS HiPerClockS LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

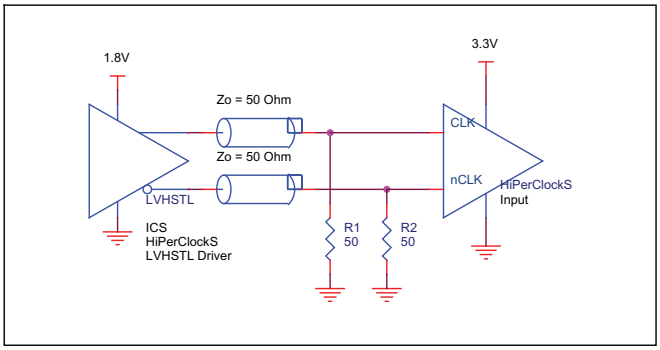


Figure 2A. HiPerClockS CLK/nCLK Input Driven by ICS HiPerClockS LVHSTL Driver

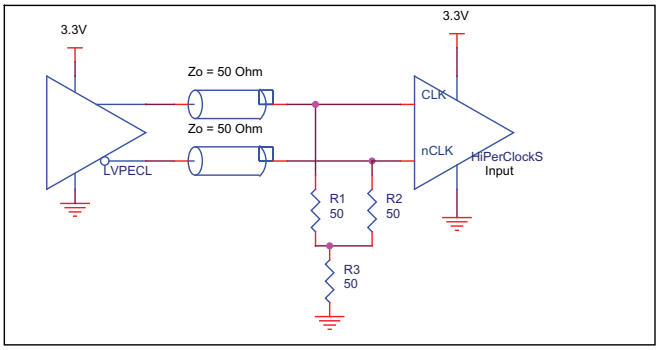


Figure 2B. HiPerClockS CLK/nCLK Input Driven by 3.3V LVPECL Driver

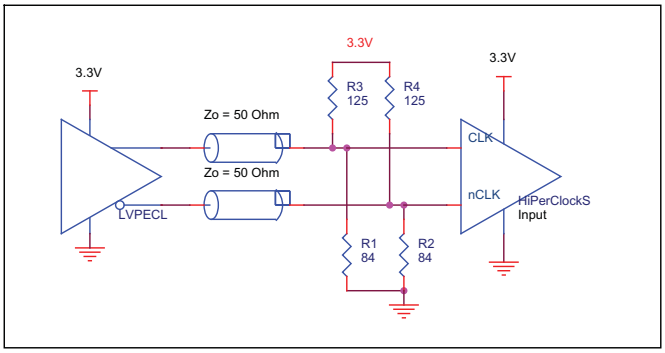


Figure 2C. HiPerClockS CLK/nCLK Input Driven by 3.3V LVPECL Driver

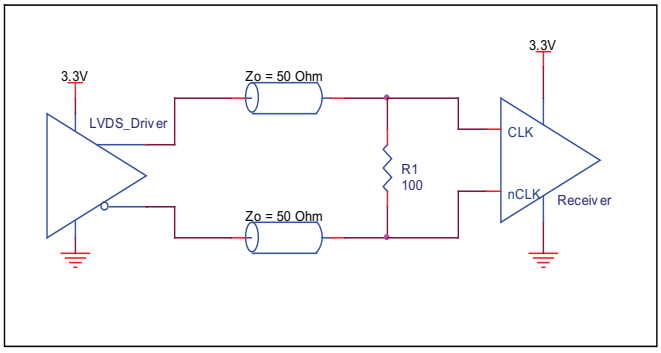


Figure 2D. HiPerClockS CLK/nCLK Input Driven by 3.3V LVDS Driver

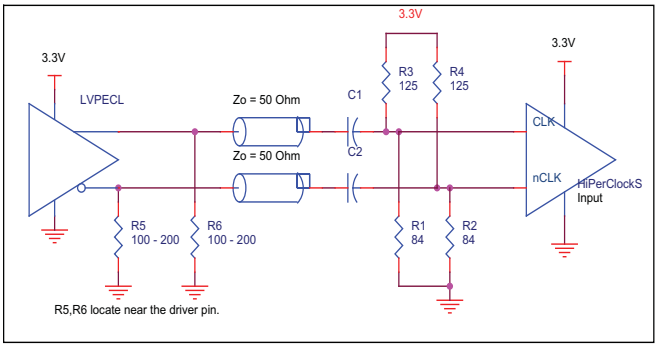


Figure 2E. HiPerClockS CLK/nCLK Input Driven by 3.3V LVPECL Driver with AC Couple

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LVDS Driver Termination

A general LVDS interface is shown in *Figure 3.* In a 100Ω differential transmission line environment, LVDS drivers require a matched load termination of 100Ω across near the receiver input. For a multiple LVDS outputs buffer, if only partial outputs are used, it is recommended to terminate the un-used outputs.

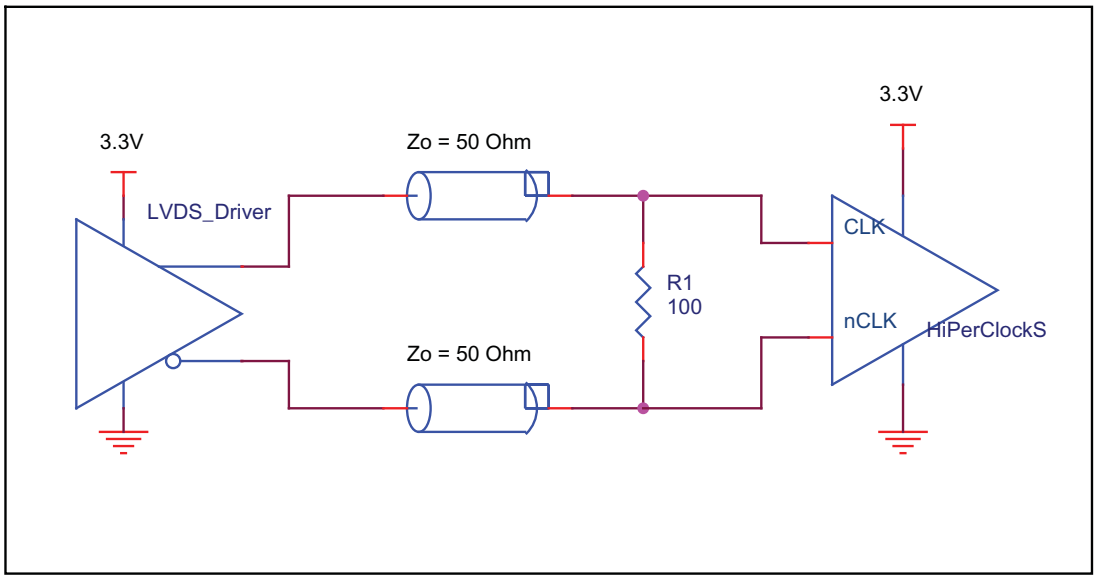


Figure 3. Typical LVDS Driver Termination

Schematic Example

Figure 4 shows a schematic example of ICS8516. In this example, the input is driven by an LVDS driver. For LVDS buffer, it is recommended to terminate the unused outputs for better signal integrity. The decoupling capacitors should be physically located near the power pin.

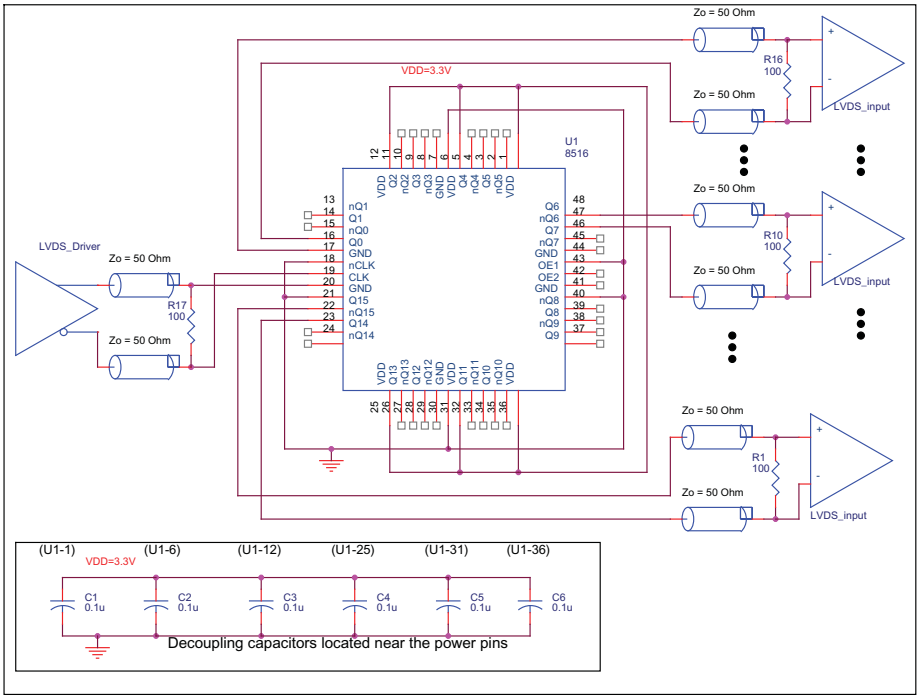


Figure 4. ICS8516 LVDS Buffer Schematic Example

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Reliability Information

Table 6. θ_{JA} vs. Air Flow Table for 48 Lead LQFP

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	67.8°C/W	55.9°C/W	50.1°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	47.9°C/W	42.1°C/W	39.4°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

Transistor Count

The transistor count for ICS8516 is: 1821

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Package Outline - Y Suffix for 48 Lead LQFP

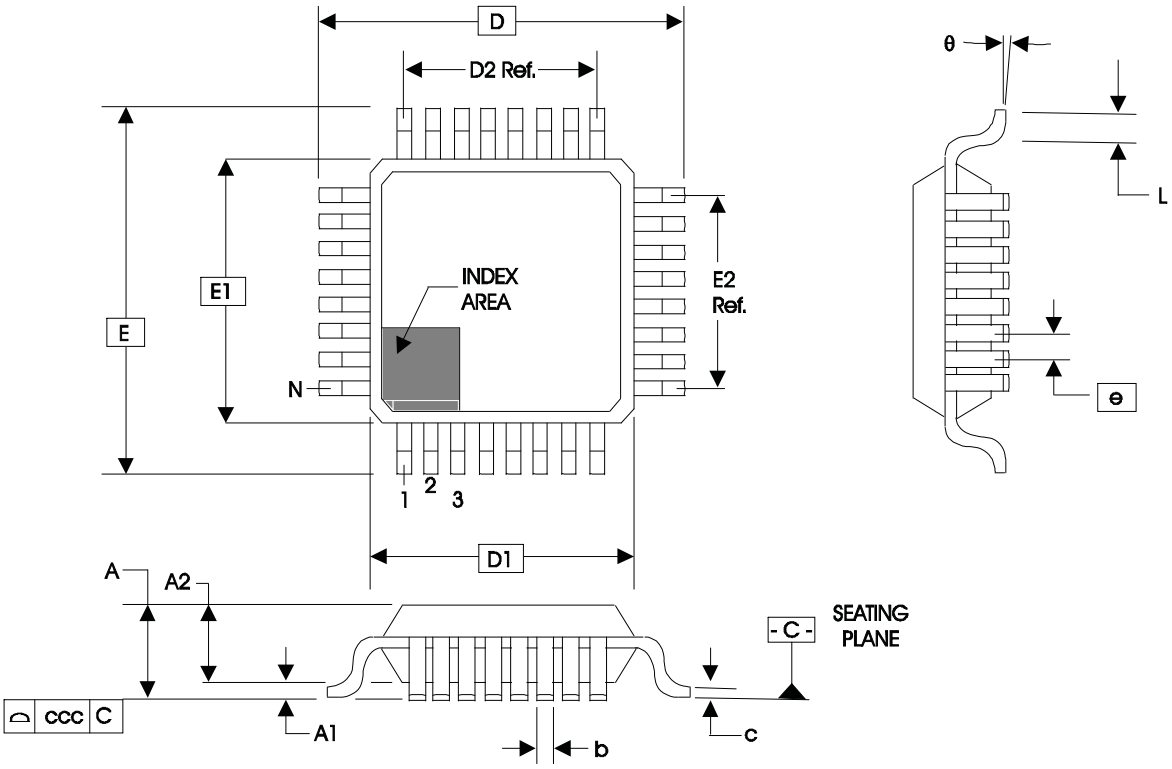


Table 7. Package Dimensions

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS			
SYMBOL	**BBC**		
	MINIMUM	**NOMINAL**	**MAXIMUM**
N		48	
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
c	0.09	--	0.20
D		9.00 BASIC	
D1		7.00 BASIC	
D2		5.50 Ref.	
E		9.00 BASIC	
E1		7.00 BASIC	
E2		5.50 Ref.	
e		0.50 BASIC	
L	0.45	0.60	0.75
θ	0°	--	7°
ccc	--	--	0.08

Reference Document: JEDEC Publication 95, MS-026

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TABLE 8. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
ICS8516FYLF	ICS8516FYLF	48 Lead “Lead-Free” LQFP	tray	0°C to 70°C
ICS8516FYLFT	ICS8516FYLF	48 Lead “Lead-Free” LQFP	tape & reel	0°C to 70°C

NOTE: Parts that are ordered with an “LF” suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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REVISION HISTORY SHEET				
Rev	**Table**	**Page**	**Description of Change**	**Date**
A	T1	2 8	Pin Description table - added pins 47 thru 48. Added LVDS Driver Termination in the Application Information section.	3/31/03
A	T1	2	Pin Description Table - switched pin names for 45, 46 & 47,48	5/6/03
A	T2 T8	3 9 12	Pin Characteristics Table - changed C_{IN} from 4pF max. to 4pF typical. Updated Differential Clock Input Interface section. Ordering Information Table - added Lead-Free part numbers.	7/30/04
B	T5	1 5 6 9	Feature Section - added Additive Phase Jitter bullet. AC Characteristics Table - added Additive Phase Jitter. Added Additive Phase Jitter section. Added *Recommendations for Unused Input and Output Pins*	2/21/06
B	T8	1 17	Features Section - removed reference to leaded devices. Ordering Information - removed leaded devices. Updated data sheet format.	6/12/15

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
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