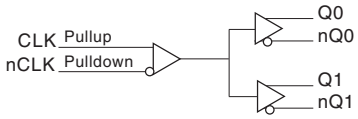
General Description

The 85211BI-03 is a low skew, high performance 1-to-2 Differential-to-LVHSTL Fanout Buffer. The CLK, nCLK pair can accept most standard differential input levels.The 85211BI-03 is characterized to operate from a 3.3V power supply. Guaranteed output and part-to-part skew characteristics make the 85211BI-03 ideal for those clock distribution applications demanding well defined performance and repeatability.

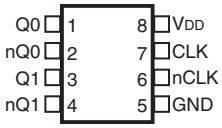
Features

- Two differential LVHSTL compatible outputs
- One differential CLK, nCLK input pair
- CLK, nCLK pair can accept the following differential input levels: LVDS, LVPECL, LVHSTL, SSTL, HCSL
- Maximum output frequency: 700MHz
- Translates any single ended input signal to LVHSTL levels with resistor bias on nCLK input
- Output skew: 30ps (maximum)
- Part-to-part skew: 250ps (maximum)
- Propagation delay: 1.3ns (maximum)
- Output duty cycle: 49% – 51% up to 266.6MHz
- V_{OH} = 1.15V (maximum)
- 3.3V operating supply
- -40°C to 85°C ambient operating temperature
- Available in lead-free (RoHS 6) package
- For functional replacement use 8523

Block Diagram



Pin Assignment



85211BI-03

8-Lead SOIC
3.90mm x 4.903mm x 1.37mm package body
M Package
Top View

© 2019 Renesas Electronics Corporation

Table 1. Pin Descriptions

Number	Name	Type		Description
1, 2	Q0, nQ0	Output		Differential output pair. LVHSTL interface levels.
3, 4	Q1, nQ1	Output		Differential output pair. LVHSTL interface levels.
5	GND	Power		Power supply ground.
6	nCLK	Input	Pulldown	Inverting differential clock input.
7	CLK	Input	Pullup	Non-inverting differential clock input.
8	V_{DD}	Power		Positive supply pin.

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ

Function Tables

Table 3. Clock Input Function Table

Inputs		Outputs		Input to Output Mode	Polarity
CLK	nCLK	Q0, Q1	nQ0, nQ1		
0	0	LOW	HIGH	Differential to Differential	Non-Inverting
1	1	HIGH	LOW	Differential to Differential	Non-Inverting
0	Biased; NOTE 1	LOW	HIGH	Single-Ended to Differential	Non-Inverting
1	Biased; NOTE 1	HIGH	LOW	Single-Ended to Differential	Non-Inverting
Biased; NOTE 1	0	HIGH	LOW	Single-Ended to Differential	Inverting
Biased; NOTE 1	1	LOW	HIGH	Single-Ended to Differential	Inverting

NOTE 1: Please refer to the Application Information section, ""Wiring the Differential Input to Accept Single Ended Levels"".

© 2019 Renesas Electronics Corporation

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5V
Outputs, I_O Continuous Current Surge Current	 50mA 100mA
Storage Temperature, T_{STG}	-65°C to 150°C
Package Thermal Impedance, θ_{JA}	112.7°C/W (0 lfpm)

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, V_{DD} = 3.3V±5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Positive Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current				55	mA

Table 4B. Differential DC Characteristics, V_{DD} = 3.3V±5%, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	CLK	$V_{DD} = V_{IN}$ = 3.465V			5	µA
		nCLK	$V_{DD} = V_{IN}$ = 3.465V			150	µA
I_{IL}	Input Low Current	CLK	V_{DD} = 3.465V, V_{IN} = 0V	-150			µA
		nCLK	V_{DD} = 3.465V, V_{IN} = 0V	-5			µA
V_{PP}	Peak-to-Peak Input Voltage; NOTE 1			0.15		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			GND + 0.5		V_{DD} – 0.85	V

NOTE 1: V_{IL} should not be less than -0.3V.
NOTE 2: Common mode voltage is defined as V_{IH}.

© 2019 Renesas Electronics Corporation

Table 4C. LVHSTL DC Characteristics, V_{DD} = 3.3V±5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Current; NOTE 1		0.7		1.15	V
V_{OL}	Output Low Current; NOTE 1		0		0.4	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.3	0.65	1.15	V

NOTE 1: Outputs terminated with 50Ω to ground.

AC Electrical Characteristics

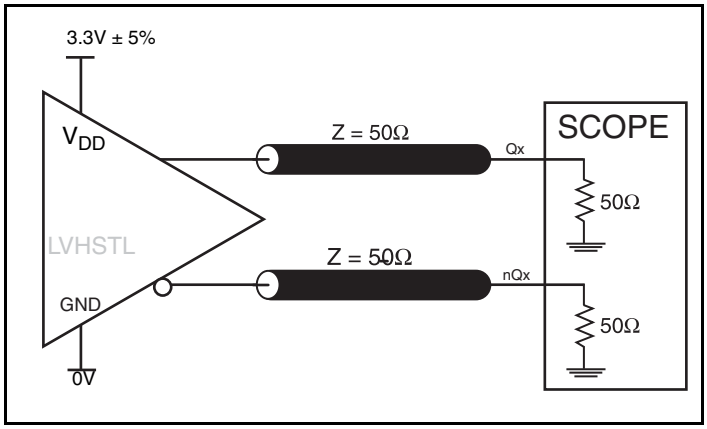
Table 5. AC Characteristics, V_{DD} = 3.3V±5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				700	MHz
t_{PD}	Propagation Delay; NOTE 1	$f \leq$ 600MHz	0.9		1.3	ns
*t*sk(o)	Output Skew; NOTE 2, 4				30	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 3, 4				250	ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	185		450	ps
odc	Output Duty Cycle		47		53	%
		$f \leq$ 266.6MHz	49		51	%

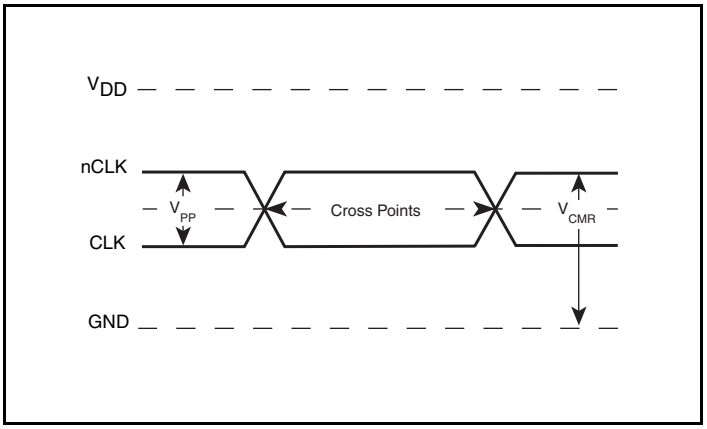
NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. Device will meet specifications after thermal equilibrium has been reached under these conditions.
The cycle-to-cycle jitter on the input will equal the jitter on the output. The part does not add jitter.
All parameters are measured 600MHz unless otherwise noted.
NOTE 1: Measured from the differential input crossing point to the differential output crossing point.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the differential cross points.
NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltage, same temperature and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

© 2019 Renesas Electronics Corporation

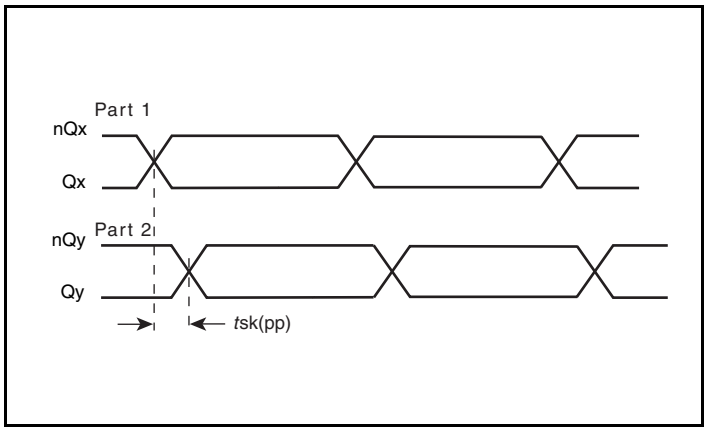
Parameter Measurement Information



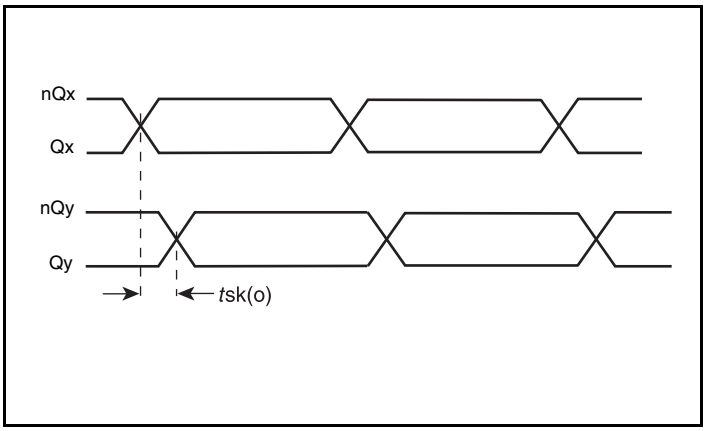
Output Load AC Test Circuit



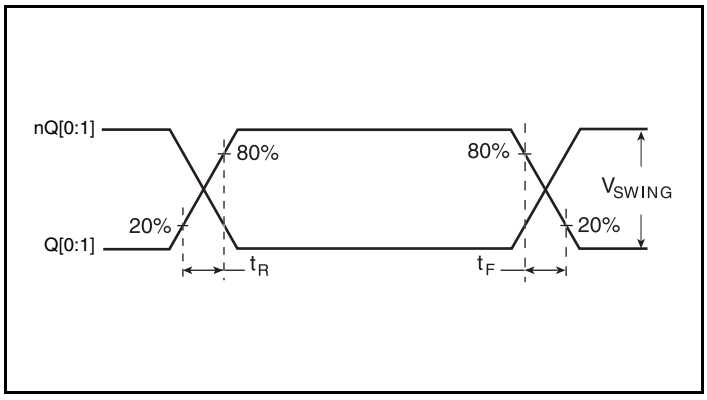
Differential Input Level



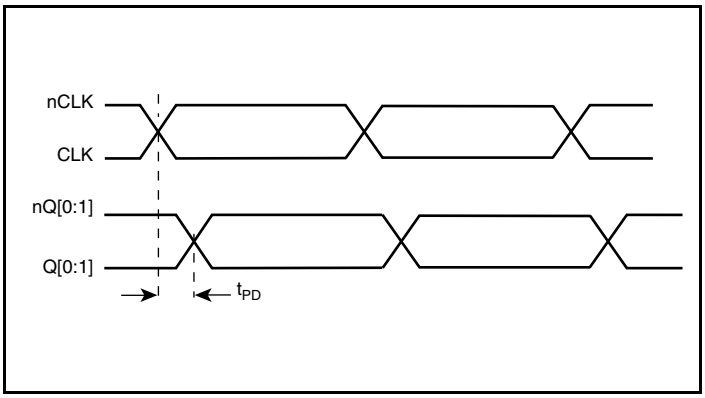
Part-to-Part Skew



Output Skew



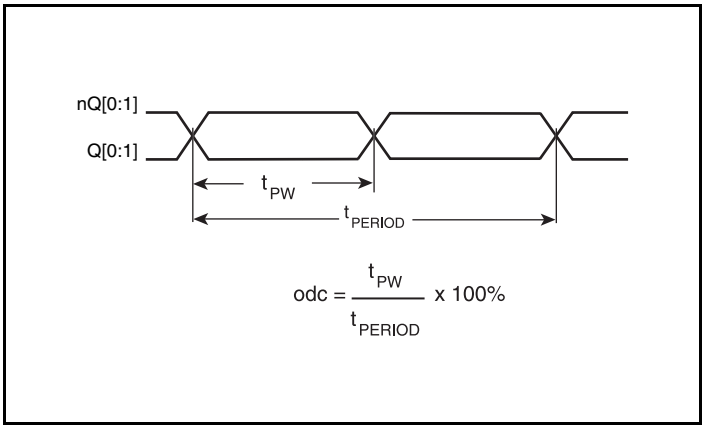
Output Rise/Fall Time



Propagation Delay

© 2019 Renesas Electronics Corporation

Parameter Measurement Information, continued



Output Duty Cycle/Pulse Width/Period

© 2019 Renesas Electronics Corporation

Application Information

Recommendations for Unused Output Pins

Outputs:

LVHSTL Outputs

All unused LVHSTL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

Wiring the Differential Input to Accept Single-Ended Levels

Figure 1 shows how a differential input can be wired to accept single ended levels. The reference voltage $V_{REF} = V_{CC}/2$ is generated by the bias resistors R1 and R2. The bypass capacitor (C1) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of R1 and R2 might need to be adjusted to position the V_{REF} in the center of the input voltage swing. For example, if the input clock swing is 2.5V and V_{CC} = 3.3V, R1 and R2 value should be adjusted to set V_{REF} at 1.25V. The values below are for when both the single ended swing and V_{CC} are at the same voltage. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways. First, R3 and R4 in parallel should equal the transmission line impedance. For most 50Ω applications, R3 and R4 can be 100Ω. The values of the resistors can be increased to reduce the loading for slower and weaker LVCMOS driver. When using single-ended signaling, the noise rejection benefits of differential signaling are reduced. Even though the differential input can handle full rail LVCMOS signaling, it is recommended that the amplitude be reduced. The datasheet specifies a lower differential amplitude, however this only applies to differential signals. For single-ended applications, the swing can be larger, however V_{IL} cannot be less than -0.3V and V_{IH} cannot be more than V_{CC} + 0.3V. Though some of the recommended components might not be used, the pads should be placed in the layout. They can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a differential signal.

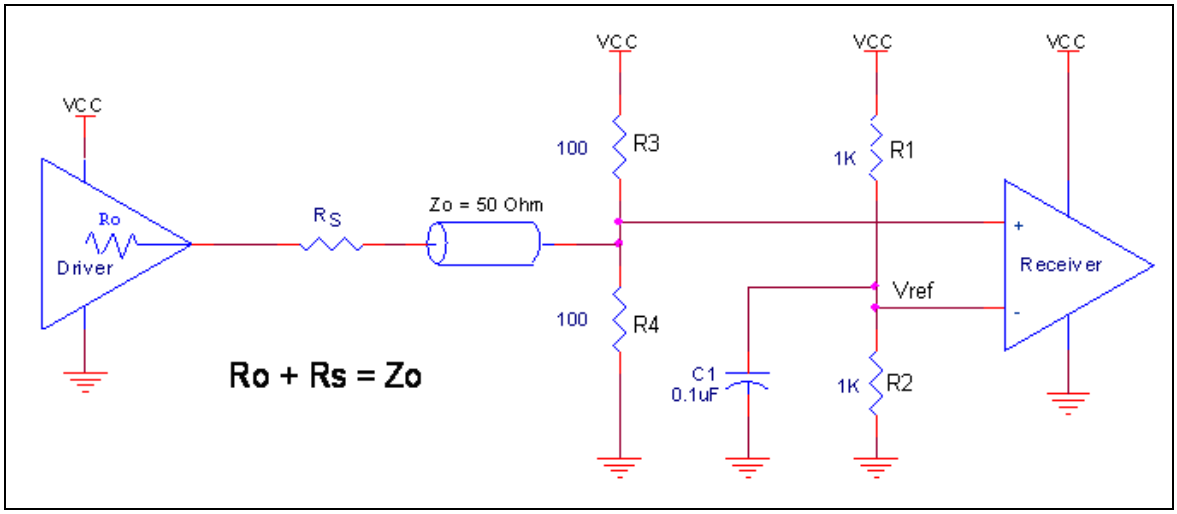


Figure 1. Recommended Schematic for Wiring a Differential Input to Accept Single-ended Levels

© 2019 Renesas Electronics Corporation

Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, SSTL, HCSL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. *Figures 2A to 2F* show interface examples for the CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only.

Please consult with the vendor of the driver component to confirm the driver termination requirements. For example, in Figure 2A, the input termination applies for IDT open emitter LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

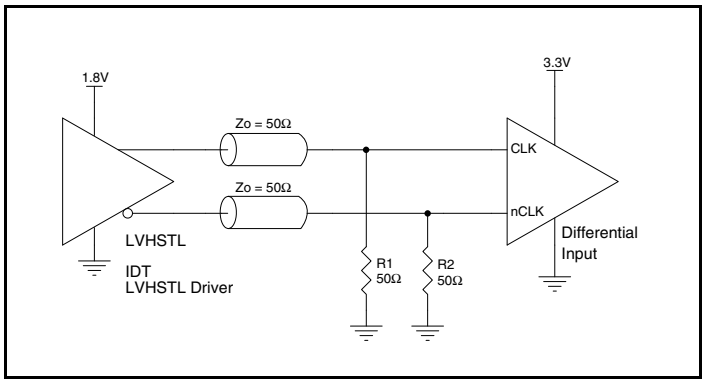


Figure 2A. CLK/nCLK Input Driven by an IDT Open Emitter LVHSTL Driver

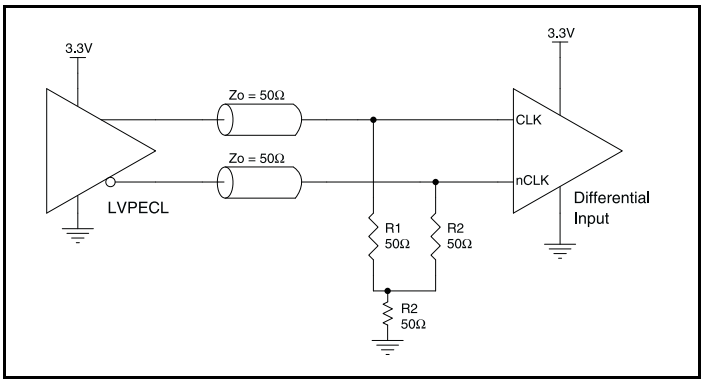


Figure 2B. CLK/nCLK Input Driven by a 3.3V LVPECLDriver

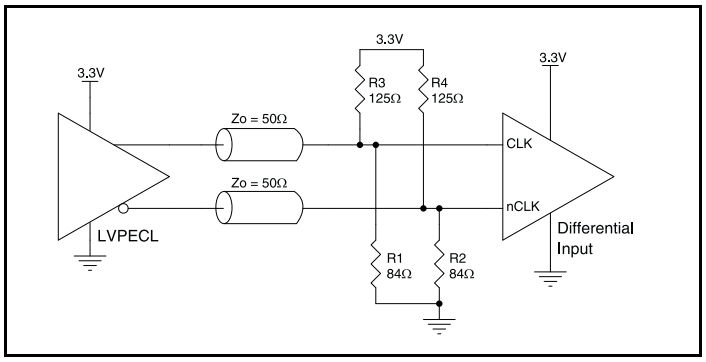


Figure 2C. CLK/nCLK Input Driven by a 3.3V LVPECL Driver

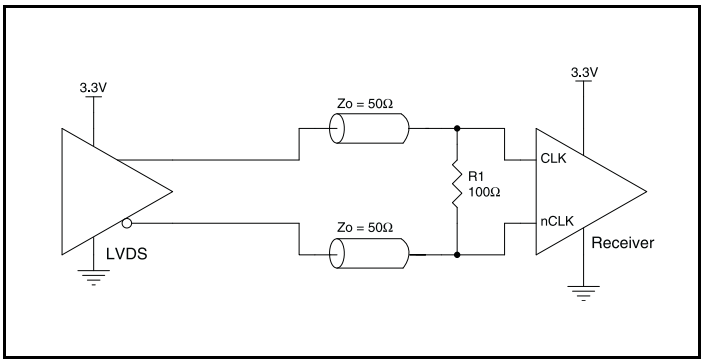


Figure 2D. CLK/nCLK Input Driven by a 3.3V LVDS Driver

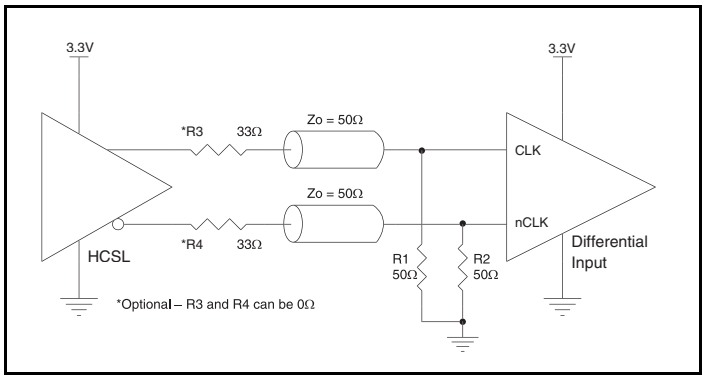


Figure 2E. CLK/nCLK Input Driven by a 3.3V HCSL Driver

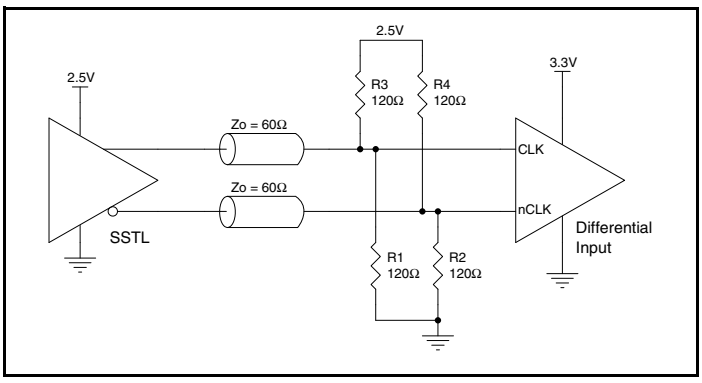


Figure 2F. CLK/nCLK Input Driven by a 2.5V SSTL Driver

© 2019 Renesas Electronics Corporation

Schematic Example

Figure 3 shows a schematic example of 85211BI-03. In this example, the input is driven by an IDT HiPerClockS LVHSTL driver. The decoupling capacitors should be physically located near the power pin.

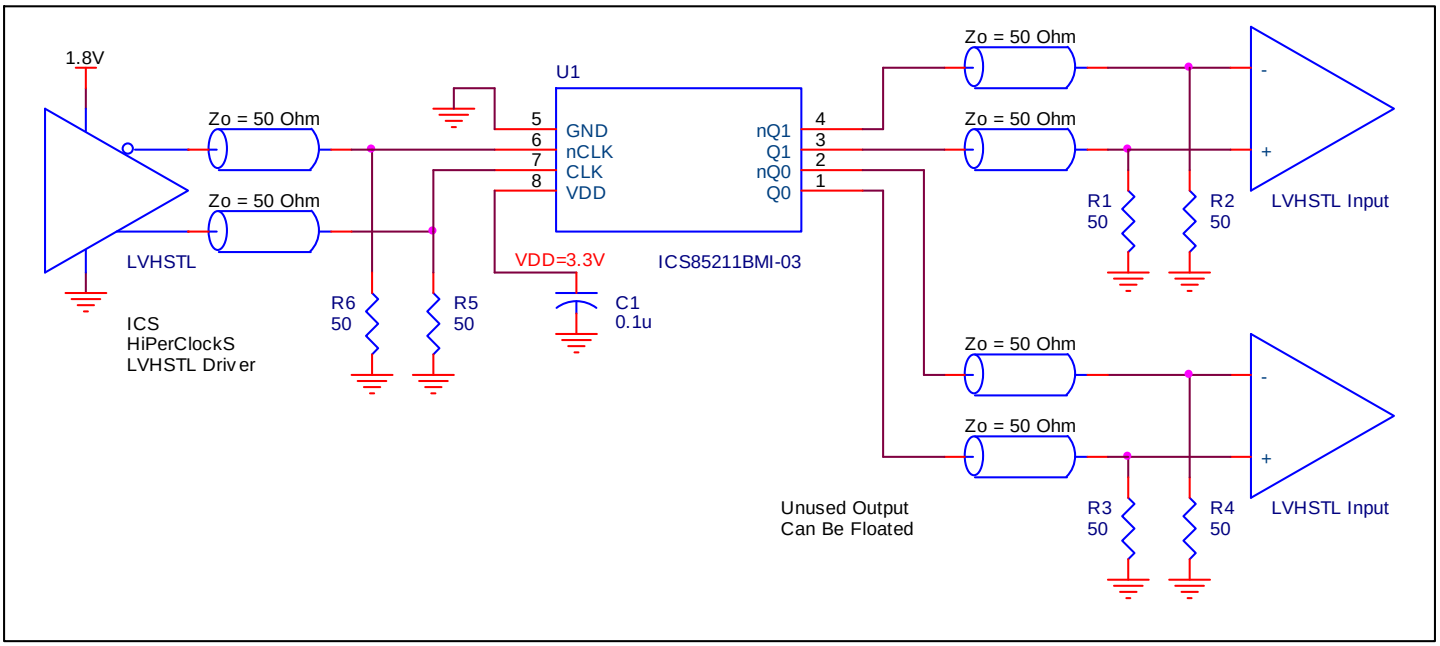


Figure 3. 85211BI-03 LVHSTL Buffer Schematic Example

© 2019 Renesas Electronics Corporation

Power Considerations

This section provides information on power dissipation and junction temperature for the 85211BI-03.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the 85211BI-03 is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{DD} = 3.3V + 5% = 3.465V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)$_{MAX}$ = V_{DD_MAX} * I_{DD_MAX} = 3.465V * 55mA = **190.6mW**
- Power (outputs)$_{MAX}$ = **77.76mW/Loaded Output pair**
  If all outputs are loaded, the total power is 2 * 77.76mW = **155.52mW**

Total Power$_{_MAX}$ (3.3V, with all outputs switching) =190.6mW + 155.52mW = **346.12mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad, and directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming a moderate air flow of 200 linear feet per minute and a multi-layer board, the appropriate value is 103.3°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.346W * 103.3°C/W = 120.7°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 6. Thermal Resistance θ_{JA} for 8 Lead SOIC, Forced Convection

θ_{JA} vs. Air Flow			
Linear Feet per Minute	**0**	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	153.3°C/W	128.5°C/W	115.5°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	112.7°C/W	103.3°C/W	97.1°C/W
NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.			

© 2019 Renesas Electronics Corporation

3. Calculations and Equations.

The purpose of this section is to calculate the power dissipation for the LVHSTL output pairs.

LVHSTL output driver circuit and termination are shown in *Figure 4.*

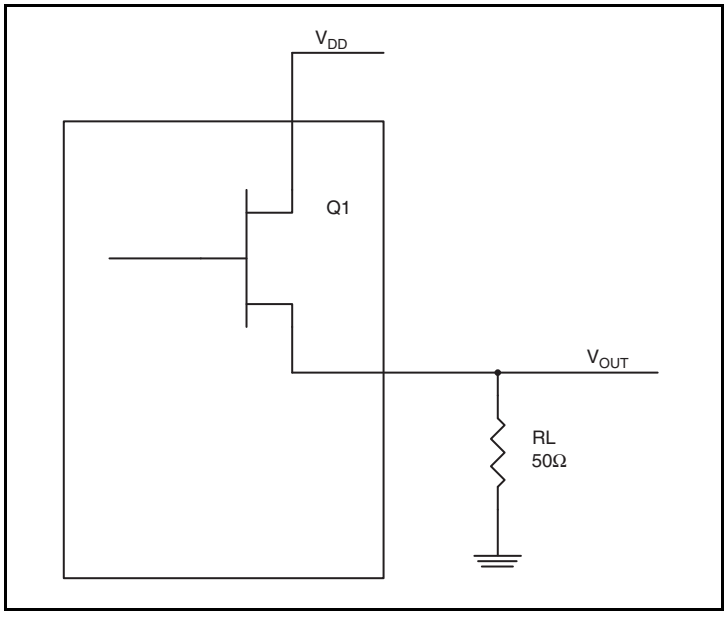


Figure 4. LVHSTL Driver Circuit and Termination

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load.

Pd_H is power dissipation when the output drives high.

Pd_L is the power dissipation when the output drives low.

$Pd_H = (V_{OH_MAX} / R_L) * (V_{DD_MAX} – (V_{OH_MAX})$

$Pd_L = (V_{OL_MAX} / R_L) * (V_{DD_MAX} – (V_{OL_MAX})$

Pd_H = (1.15V/50Ω) * (3.465V – 1.15V) = **53.24mW**

Pd_L = (0.4V/50Ω) * (3.465V – 0.4V) = **24.52mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **77.76mW**

© 2019 Renesas Electronics Corporation

Reliability Information

Table 7. θ_{JA} vs. Air Flow Table for a 8 Lead SOIC

θ_{JA} by Velocity			
Linear Feet per Minute	**0**	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	153.3°C/W	128.5°C/W	115.5°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	112.7°C/W	103.3°C/W	97.1°C/W
NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.			

Transistor Count

The transistor count for 85211BI-03 is: 472

Package Outline and Package Dimensions

Package Outline - M Suffix for 8 Lead SOIC

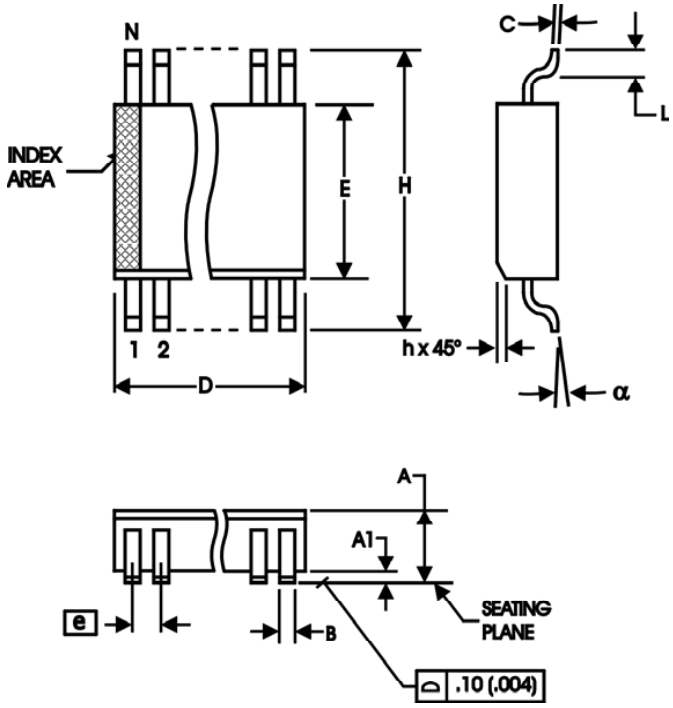


Table 8. Package Dimensions

All Dimensions in Millimeters		
Symbol	**Minimum**	**Maximum**
N	8	
A	1.35	1.75
A1	0.10	0.25
B	0.33	0.51
C	0.19	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 Basic	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.27
α	0°	8°

Reference Document: JEDEC Publication 95, MS-012

© 2019 Renesas Electronics Corporation

Ordering Information

Table 9. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
85211BMI-03LN	211BI03N	“Lead-Free” 8 Lead SOIC	Tube	-40°C to 85°C
85211BMI-03LNT	211BI03N	“Lead-Free” 8 Lead SOIC	2500 Tape & Reel	-40°C to 85°C

NOTE: Parts that are ordered with an "N" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

© 2019 Renesas Electronics Corporation

Revision History Sheet

Rev	Table	Page	Description of Change	Date
B	T4A	3	Power Supply Table - changed I_{DD} max. from 50mA to 55mA.	10/15/03
		8	Power Considerations - changed the I_{DD} limit from 50mA to 55mA to reflect Table 4A. Recalculated Power Dissipation and Junction Temperature formulas.	
B		1	Features Section - add Lead-Free bullet.	9/14/04
		7	Updated *Differential Clock Input Interface* section.	
	T8	12	Added Lead-Free part number to Ordering Information table.	
B	T8	12	Ordering Information Table - corrected Lead-Free P/N from "LF" to "LN".	10/11/04
B	T8	12	Ordering Information Table - corrected marking to read "211BMI02".	10/18/04
B		6	Added *Recommendations for Unused Input and Output Pins.*	11/15/05
		9-10	Corrected Power Considerations, Power Dissipation calculation.	
	T9	13	Ordering Information Table - added lead-free note.	
B	T9	13	Ordering Information Table - corrected lead-free marking.	8/23/06
C	T1	2	Pin Description Table - changed pin 6 resistor (nCLK) from a Pullup/Pulldown to Pulldown.	12/11/09
	T4B	3	Differential DC Characteristics Table - changed I_{IH} CLK from 150uA to 5uA max. Changed I_{IL} nCLK from -150uA to -5uA min., and CLK from -5uA to -150uA min. Updated NOTES.	
	T5	4	AC Characteristics Table - added thermal note.	
	T9	7	Ordering Information Table - deleted ICS prefix from the Part/Order Numbers.	
		13	Converted datasheet format.	
C		7	Updated “Wiring the Differential to Accept Single Ended Levels”.	3/3/10
D	T9	13	Ordering Information - removed leaded devices. PDN CQ-13-02. Updated datasheet format.	12/19/14
D		1	Product Discontinuation Notice - Last time buy expires September 7, 2016. PDN N-16-02	3/11/16

© 2019 Renesas Electronics Corporation

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers skilled in the art designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only for development of an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising out of your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Rev.1.0 Mar 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
www.renesas.com/contact/

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

© 2020 Renesas Electronics Corporation. All rights reserved.