1-to-2, LVCMOS/LVTTL- To- Differential HSTL Translator

ICS85222I-02

DATASHEET

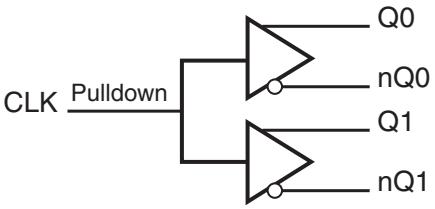
General Description

The ICS85222I-02 is a 1-to-2 LVCMOS / LVTTL-to- Differential HSTL translator. The ICS85222I-02 has one single-ended clock input. The single-ended clock input accepts LVCMOS or LVTTL input levels and translates them to HSTL levels. The small outline 8-pin SOIC package makes this device ideal for applications where space, high performance and low power are important.

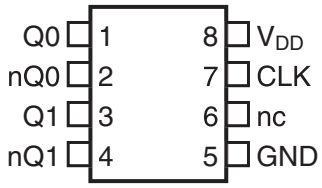
Features

- Two differential HSTL outputs
- One LVCMOS/LVTTL clock input
- CLK input can accept the following input levels: LVCMOS or LVTTL
- Maximum output frequency: 350MHz
- Part-to-part skew: 500ps (maximum)
- Propagation delay: 1.55ns (maximum)
- V_{OH}: 1.4V (maximum)
- Output crossover voltage: 0.5V - 0.9V
- Full 3.3V operating supply voltage
- -40°C to 85°C ambient operating temperature
- Lead-free RoHS compliant packaging

Block Diagram



Pin Assignment



ICS85222I-02

8-Lead SOIC
3.90mm x 4.92mm x 1.37mm body package
M Package

Top View

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Pin Descriptions and Characteristics

Table 1. Pin Descriptions

Number	Name	Type		Description
1	Q0	Output		Differential output pair. HSTL interface levels.
2	nQ0	Output		Differential output pair. HSTL interface levels.
3	Q1	Output		Differential output pair. HSTL interface levels.
4	nQ1	Output		Differential output pair. HSTL interface levels.
5	GND	Power		Power supply ground.
6	nc	Unused		No connect
7	CLK	Input	Pulldown	LVCMOS / LVTTL clock input.
8	V_{DD}	Power		Positive supply pin.

NOTE: *Pulldown* refers to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.
NOTE: Unused output pairs must be terminated.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ

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Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of the product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5V
Outputs, I_O Continuous Current Surge Current	 50mA 100mA
Junction Temperature, T_J	125°C
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 3A. Power Supply DC Characteristics, V_{DD} = 3.3V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Positive Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current	Outputs not loaded			50	mA

Table 3B. LVCMOS/LVTTL DC Characteristics, V_{DD} = 3.3V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage			-0.3		0.8	V
I_{IH}	Input High Current	CLK	V_{DD} = V_{IN} = 3.465V			150	µA
I_{IL}	Input Low Current	CLK	V_{DD} = 3.465V, V_{IN} = 0V	-5			µA

Table 3C. HSTL DC Characteristics, V_{DD} = 3.3V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		1.0		1.4	V
V_{OL}	Output Low Voltage; NOTE 1		0		0.4	V
V_{OX}	Output Crossover Voltage		0.5		0.9	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.6	1.0	1.4	V

NOTE 1: All outputs must be terminated with 50Ω to ground.

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AC Electrical Characteristics

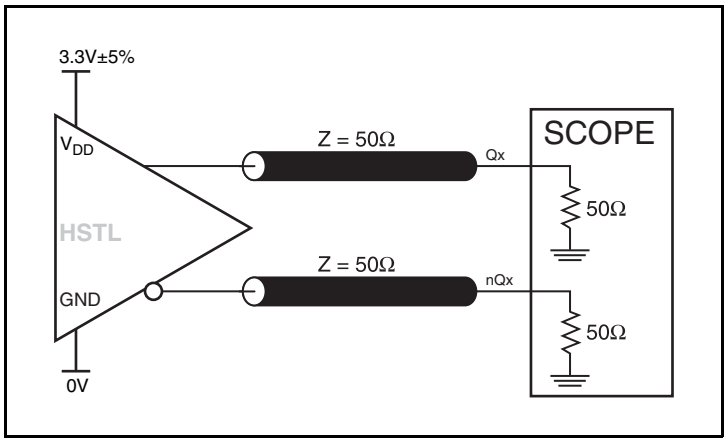
Table 4. AC Characteristics, V_{DD} = 3.3V ± 5%, T_A = -40°C to 85°C

Parameter	Symbol	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				350	MHz
t_{PD}	Propagation Delay; NOTE 1	$f \leq$ 350MHz	1.0		1.55	ns
*t*sk(o)	Output Skew; NOTE 2, 3				35	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 4				500	ps
t_R/t_F	Output Rise/Fall Time	20% to 80%	225		700	ps
odc	Output Duty Cycle	$f \leq$ 250MHz	40		60	%
		$f >$ 250MHz	35		65	%

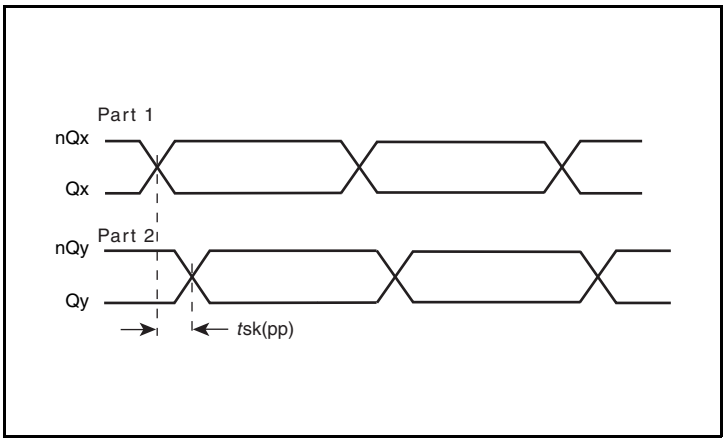
NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE: All outputs must be terminated with 50Ω to ground.
NOTE 1: Measured from $V_{DD}/2$ of the input to the differential output crossing point.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 4: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential crosspoints.

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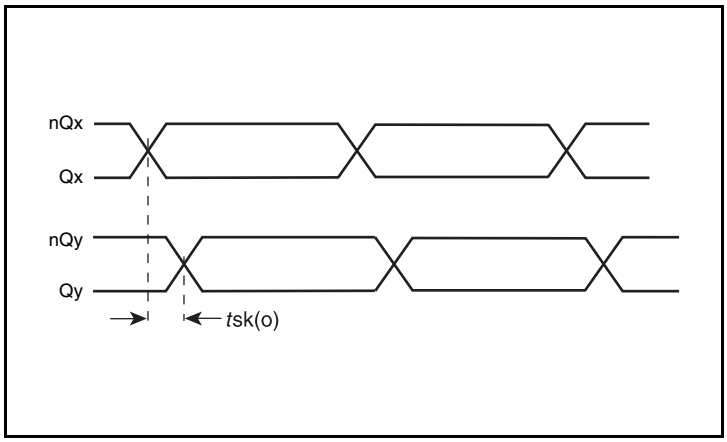
Parameter Measurement Information



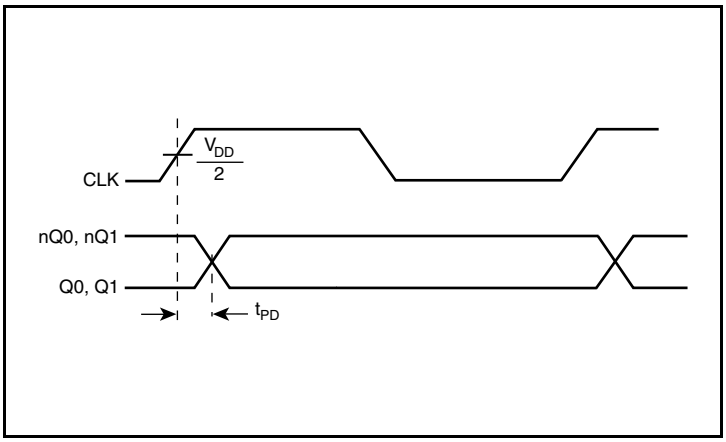
3.3V Core/3.3V Output Load AC Test Circuit



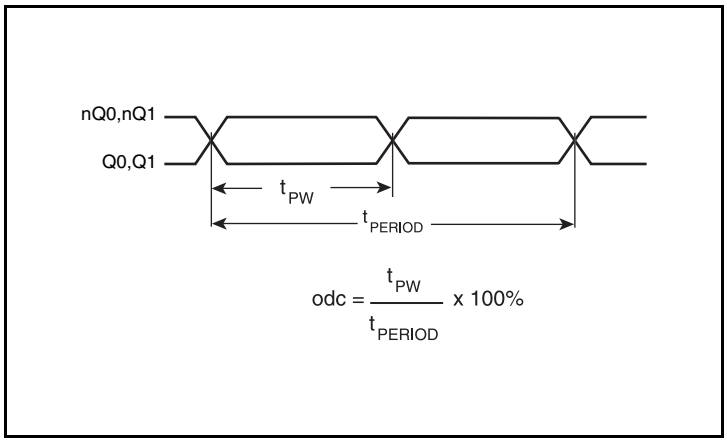
Part-to-Part Skew



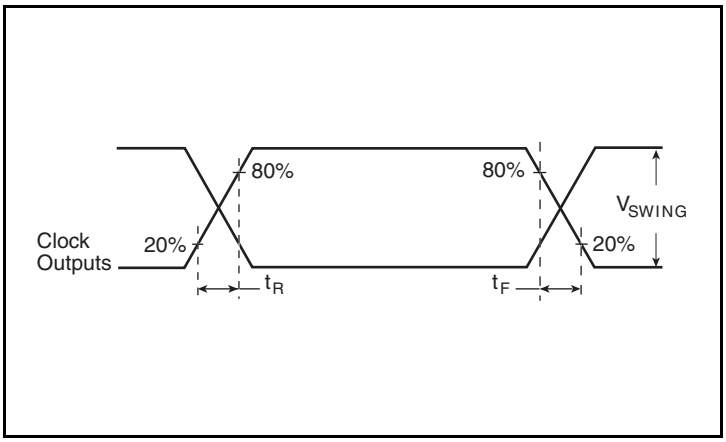
Output Skew



Propagation Delay



Output Duty Cycle/Pulse Width/Period



Output Rise/Fall Time

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Application Information

Recommendations for Unused Input and Output Pins

Outputs:

HSTL Outputs

All outputs must be terminated with 50Ω to ground.

Schematic Example

Figure 1 shows a schematic example of ICS85222I-02. In the example, the input is driven by a 7Ω LVCMOS driver with a series termination. The decoupling capacitor should be physically located near the power pin. For ICS85222I-02, the unused output need to be terminated.

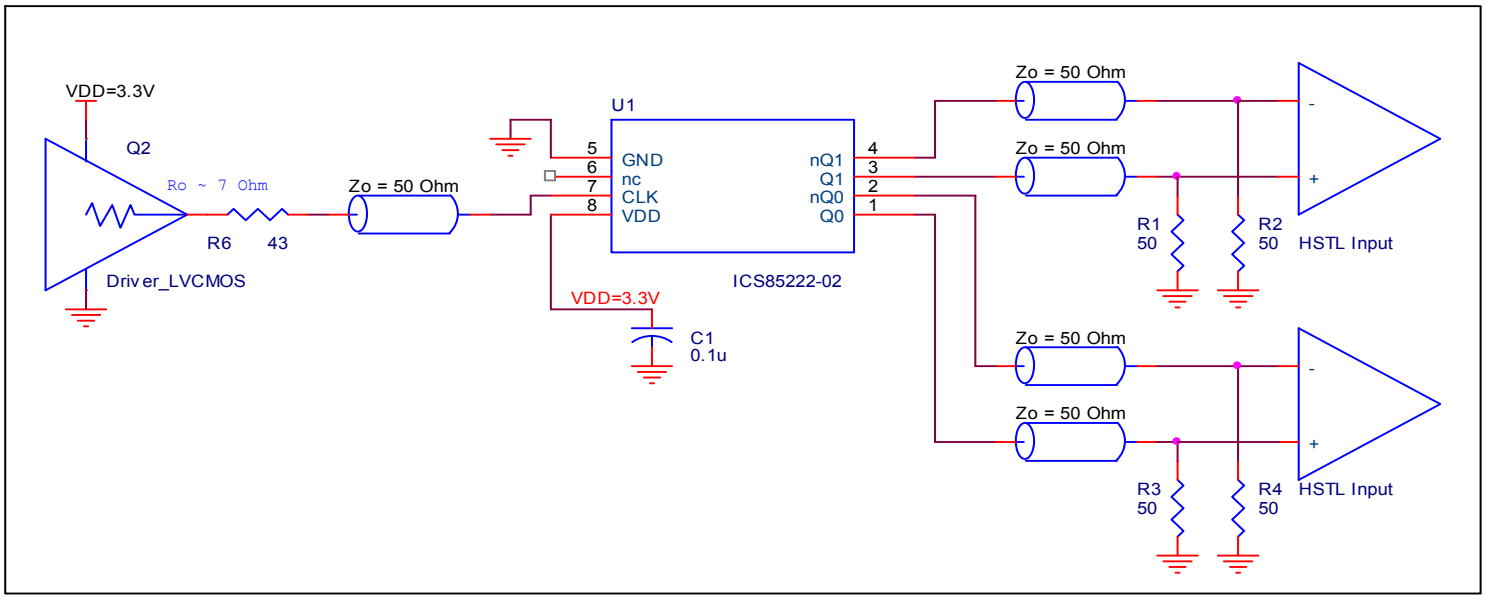


Figure 1. ICS85222I-02 HSTL Buffer Schematic Example

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Power Considerations

This section provides information on power dissipation and junction temperature for the ICS85222I-02.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS85222I-02 is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{DD} = 3.3V + 5% = 3.465V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power $(core)_{MAX} = V_{DD_MAX} * I_{DD_MAX}$ = 3.465V * 50mA = **173.25mW**
- Power $(outputs)_{MAX}$ = **82.3mW/Loaded Output pair**
  If all outputs are loaded, the total power is 2 x 82.3mW = **164.6mW**

Total Power$_{MAX}$ (3.465V, with all outputs switching) = 173.3mW + 164.6mW = **337.85mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature is 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 103°C/W per Table 5 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.338W * 103°C/W = 119.8°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (single layer or multi-layer).

Table 5. Thermal Resitance θ_{JA} for 8-Lead SOIC, Forced Convection

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	103°C/W	94°C/W	89°C/W

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3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

HSTL output driver circuit and termination are shown in *Figure 2.*

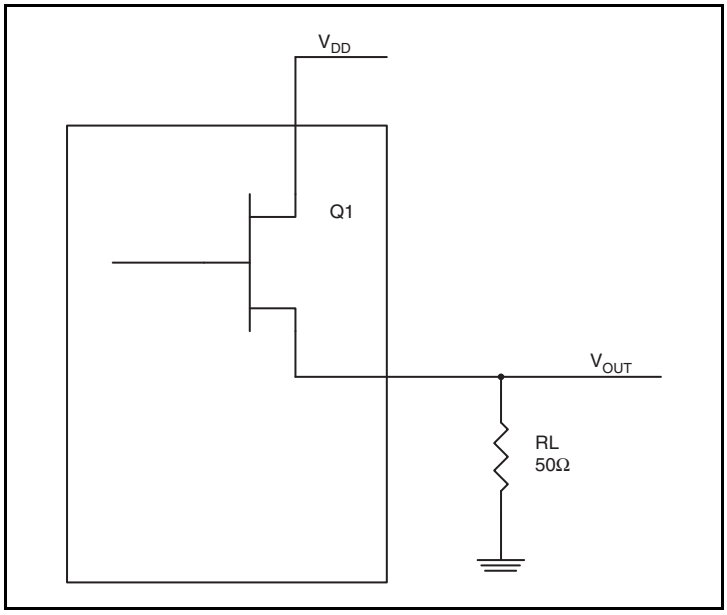


Figure 2. HSTL Driver Circuit and Termination

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load.

Pd_H is power dissipation when the output drives high.

Pd_L is the power dissipation when the output drives low.

$Pd_H = (V_{OH_MAX} / R_L) * (V_{DDO_MAX} - V_{OH_MAX})$

$Pd_L = (V_{OL_MAX} / R_L) * (V_{DDO_MAX} - V_{OL_MAX})$

Pd_H = (1.4V/50Ω) * (3.465V - 1.4V) = **57.8mW**

Pd_L = (0.4V/50Ω) * (3.465V - 0.4V) = **24.52mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **82.3mW**

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Reliability Information

Table 6. θ_{JA} vs. Air Flow Table for a 8-Lead SOIC

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	103°C/W	94°C/W	89°C/W

Transistor Count

The transistor count for ICS85222i-02 is: 411

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Package Outline and Package Dimension

Package Outline - M Suffix for 8-Lead SOIC

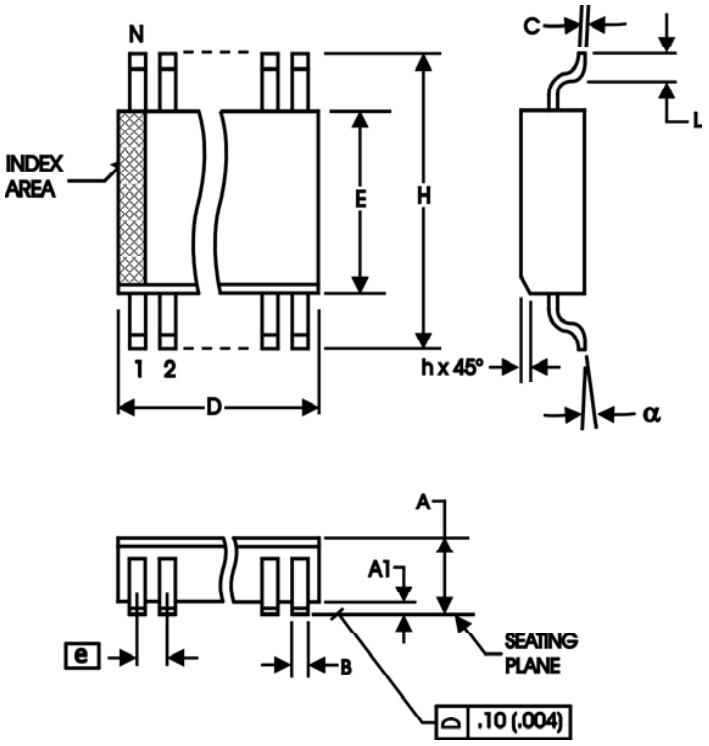


Table 7. Package Dimensions

All Dimensions in Millimeters		
Symbol	**Minimum**	**Maximum**
N	8	
A	1.35	1.75
A1	0.10	0.25
B	0.33	1.51
C	0.19	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 Basic	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.27
α	0°	8°

Reference Document: JEDEC Publication 95, MS-012

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Ordering Information

Table 8. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
ICS85222AMI-02LF	222AI02L	“Lead-free” 8-Lead SOIC	Tube	-40°C to 85°C
ICS85222AMI-02LFT	222AI02L	“Lead-free” 8-Lead SOIC	Tape and Reel	-40°C to 85°C

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