General Description

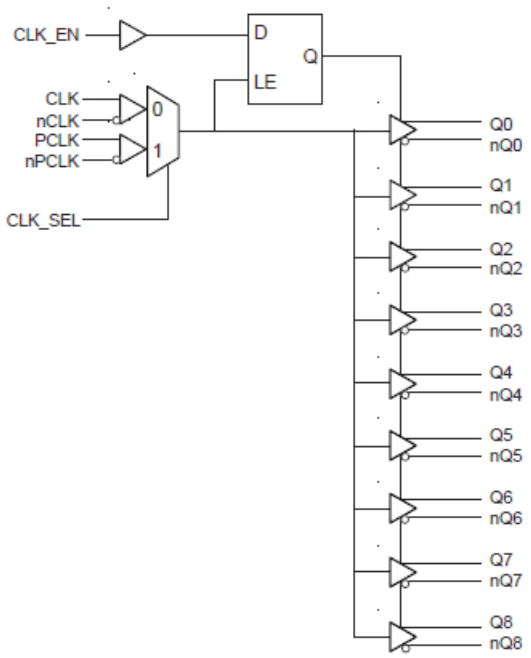
The 8531-01 is a low skew, high performance 1-to-9 Differential-to-3.3V LVPECL Fanout Buffer and a member of the family of High Performance Clock Solutions from IDT. The 8531-01 has two selectable clock inputs. The CLK, nCLK pair can accept most standard differential input levels. The PCLK, nPCLK pair can accept LVPECL, CML, or SSTL input levels. The clock enable is internally synchronized to eliminate runt pulses on the outputs during asynchronous assertion/deassertion of the clock enable pin.

Guaranteed output skew and part-to-part skew characteristics make the 8531-01 ideal for high performance workstation and server applications.

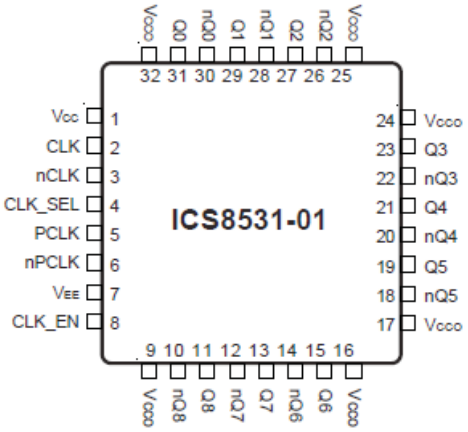
Features

- Nine differential 3.3V LVPECL outputs
- Selectable differential CLK, nCLK or LVPECL clock inputs
- CLK, nCLK pair can accept the following differential input levels: LVPECL, LVDS, LVHSTL, SSTL, HCSL
- PCLK, nPCLK supports the following input types: LVPECL, CML, SSTL
- Maximum output frequency: 500MHz
- Translates any single ended input signal (LVCMOS, LVTTL, GTL) to 3.3V LVPECL levels with resistor bias on nCLK input
- Additive phase jitter, RMS: 0.17ps (typical)
- Output skew: 50ps (maximum)
- Part-to-part skew: 250ps (maximum)
- Propagation delay: 2ns (maximum)
- 3.3V operating supply
- 0°C to 70°C ambient operating temperature
- Available in lead-free (RoHS 6) package
- Industrial Temperature information available upon request

Block Diagram



Pin Assignment



32-Lead LQFP
7mm x 7mm x 1.4mm package body
Y package
Top View

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Table 1. Pin Descriptions

Number	Name	Type		Description
1	V_{CC}	Power		Power supply pin.
2	CLK	Input	Pulldown	Non-inverting differential clock input.
3	nCLK	Input	Pullup	Inverting differential clock input.
4	CLK_SEL	Input	Pulldown	Clock Select input. When HIGH, selects PCLK, nPCLK inputs. When LOW, selects CLK, nCLK. LVTTL / LVCMOS interface levels.
5	PCLK	Input	Pulldown	Non-inverting differential LVPECL clock input.
6	nPCLK	Input	Pullup	Inverting differential LVPECL clock input.
7	V_{EE}	Power		Negative supply pin.
8	CLK_EN	Input	Pullup	Synchronizing clock enable. When HIGH, clock outputs follow clock input. When LOW, Q outputs are forced low, nQ outputs are forced high. LVTTL / LVCMOS interface levels.
9, 16, 17, 24, 25, 32	V_{CCO}	Power		Output supply pins.
10, 11	nQ8, Q8	Output		Differential output pair. LVPECL interface level.
12, 13	nQ7, Q7	Output		Differential output pair. LVPECL interface level.
14, 15	nQ6, Q6	Output		Differential output pair. LVPECL interface level.
18, 19	nQ5, Q5	Output		Differential output pair. LVPECL interface level.
20, 21	nQ4, Q4	Output		Differential output pair. LVPECL interface level.
22, 23	nQ3 Q3	Output		Differential output pair. LVPECL interface level.
26, 27	nQ2, Q2	Output		Differential output pair. LVPECL interface level.
28, 29	nQ1, Q1	Output		Differential output pair. LVPECL interface level.
30, 31	nQ0, Q0	Output		Differential output pair. LVPECL interface level.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ

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TABLE 3A. CONTROL INPUT FUNCTION TABLE

Inputs			Outputs	
CLK_EN	**CLK_SEL**	**Selected Sourced**	**Q0:Q8**	**nQ0:nQ8**
0	0	CLK, nCLK	Disabled; LOW	Disabled; HIGH
0	1	PCLK, nPCLK	Disabled; LOW	Disabled; HIGH
1	0	CLK, nCLK	Enabled	Enabled
1	1	PCLK, nPCLK	Enabled	Enabled

After CLK_EN switches, the clock outputs are disabled or enabled following a rising and falling input clock edge as shown in Figure 1.
In the active mode, the state of the outputs are a function of the CLK, nCLK and PCLK, nPCLK inputs as described in Table 3B.

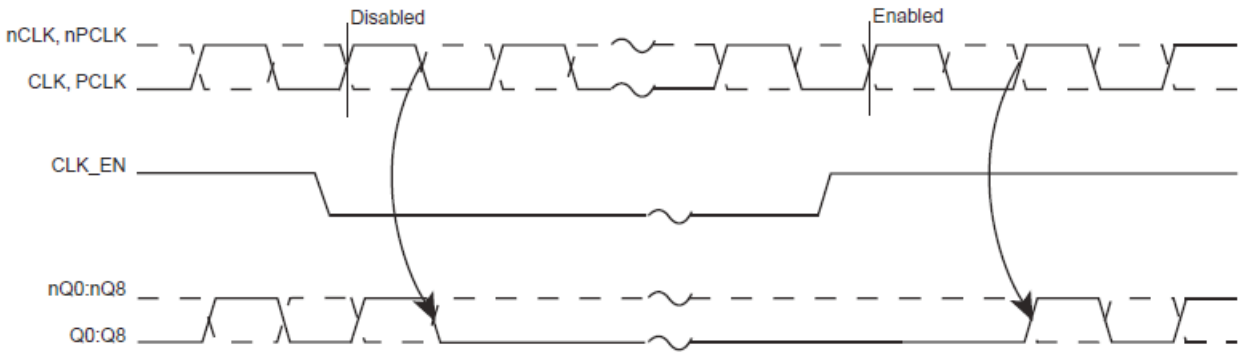


FIGURE 1. CLK_EN TIMING DIAGRAM

TABLE 3B. CLOCK INPUT FUNCTION TABLE

Inputs		Outputs		Input to Output Mode	Polarity
CLK or PCLK	**nCLK or nPCLK**	**Q0:Q8**	**nQ0:nQ8**		
0	1	LOW	HIGH	Differential to Differential	Non Inverting
1	0	HIGH	LOW	Differential to Differential	Non Inverting
0	Biased; NOTE 1	LOW	HIGH	Single Ended to Differential	Non Inverting
1	Biased; NOTE 1	HIGH	LOW	Single Ended to Differential	Non Inverting
Biased; NOTE 1	0	HIGH	LOW	Single Ended to Differential	Inverting
Biased; NOTE 1	1	LOW	HIGH	Single Ended to Differential	Inverting

NOTE 1: Please refer to the Application Information section, “Wiring the Differential Input to Accept Single Ended Levels”.

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Absolute Maximum Ratings

Supply Voltage, V_{CC}	4.6V
Inputs, V_I	-0.5V to V_{CC} + 0.5V
Outputs, I_O	
Continuous Current	50mA
Surge Current	100mA
Package Thermal Impedance, θ_{JA}	47.9°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Table 4A. Power Supply DC Characteristics, $V_{CC} = V_{CCO} = 3.3V \pm 5\%$, T_A = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Power Supply Voltage		3.135	3.3	3.465	V
V_{CCO}	Output Supply Voltage		3.135	3.3	3.465	V
I_{EE}	Power Supply Current				80	mA

Table 4B. LVCMOS / LVTTL DC Characteristics, $V_{CC} = V_{CCO} = 3.3V \pm 5\%$, T_A = 0°C to 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	CLK_EN, CLK_SEL			2		3.765	V
V_{IL}	CLK_EN, CLK_SEL			-0.3		0.8	V
I_{IH}	Input High Current	CLK_EN	$V_{CC} = V_{IN} = 3.465V$			5	µA
		CLK_SEL	$V_{CC} = V_{IN} = 3.465V$			150	µA
I_{IL}	Input Low Current	CLK_EN	$V_{IN} = 0V, V_{CC} = 3.465V$	-150			µA
		CLK_SEL	$V_{IN} = 0V, V_{CC} = 3.465V$	-5			µA

Table 4C. Differential DC Characteristics, $V_{CC} = V_{CCO} = 3.3V \pm 5\%$, T_A = 0°C to 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	CLK	$V_{CC} = V_{IN} = 3.465V$			150	µA
		nCLK	$V_{CC} = V_{IN} = 3.465V$			5	µA
I_{IL}	Input Low Current	CLK	$V_{IN} = 0V, V_{CC} = 3.465V$	-5			µA
		nCLK	$V_{IN} = 0V, V_{CC} = 3.465V$	-150			µA
V_{PP}	Peak-to-Peak Input Voltage			0.15		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			V_{EE} + 0.5		V_{CC} - 0.85	V

NOTE 1: For single ended applications, the maximum input voltage for CLK and nCLK is V_{CC} + 0.3V.
NOTE 2: Common mode input voltage is defined as V_{IH}.

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TABLE 4D. LVPECL DC CHARACTERISTICS, $V_{CC} = V_{CCO} = 3.3V \pm 5\%$, $T_A = 0°C$ TO $70°C$

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	PCLK	$V_{CC} = V_{IN} = 3.465V$			150	µA
		nPCLK	$V_{CC} = V_{IN} = 3.465V$			5	µA
I_{IL}	Input Low Current	PCLK	$V_{IN} = 0V, V_{CC} = 3.465V$	-5			µA
		nPCLK	$V_{IN} = 0V, V_{CC} = 3.465V$	-150			µA
V_{PP}	Peak-to-Peak Input Voltage			0.3		1	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			V_{EE} + 1.5		V_{CC}	V
V_{OH}	Output High Voltage; NOTE 3			V_{CCO} - 1.4		V_{CCO} - 0.9	V
V_{OL}	Output Low Voltage; NOTE 3			V_{CCO} - 2.0		V_{CCO} - 1.7	V
V_{SWING}	Peak-to-Peak Output Voltage Swing			0.6		1.0	V

NOTE 1: Common mode input voltage is defined as V_{IH}.
NOTE 2: For single ended applications, the maximum input voltage for PCLK and nPCLK is V_{CC} + 0.3V.
NOTE 3: Outputs terminated with 50Ω to V_{CCO} - 2V.

TABLE 5. AC CHARACTERISTICS, $V_{CC} = V_{CCO} = 3.3V \pm 5\%$, $T_A = 0°C$ TO $70°C$

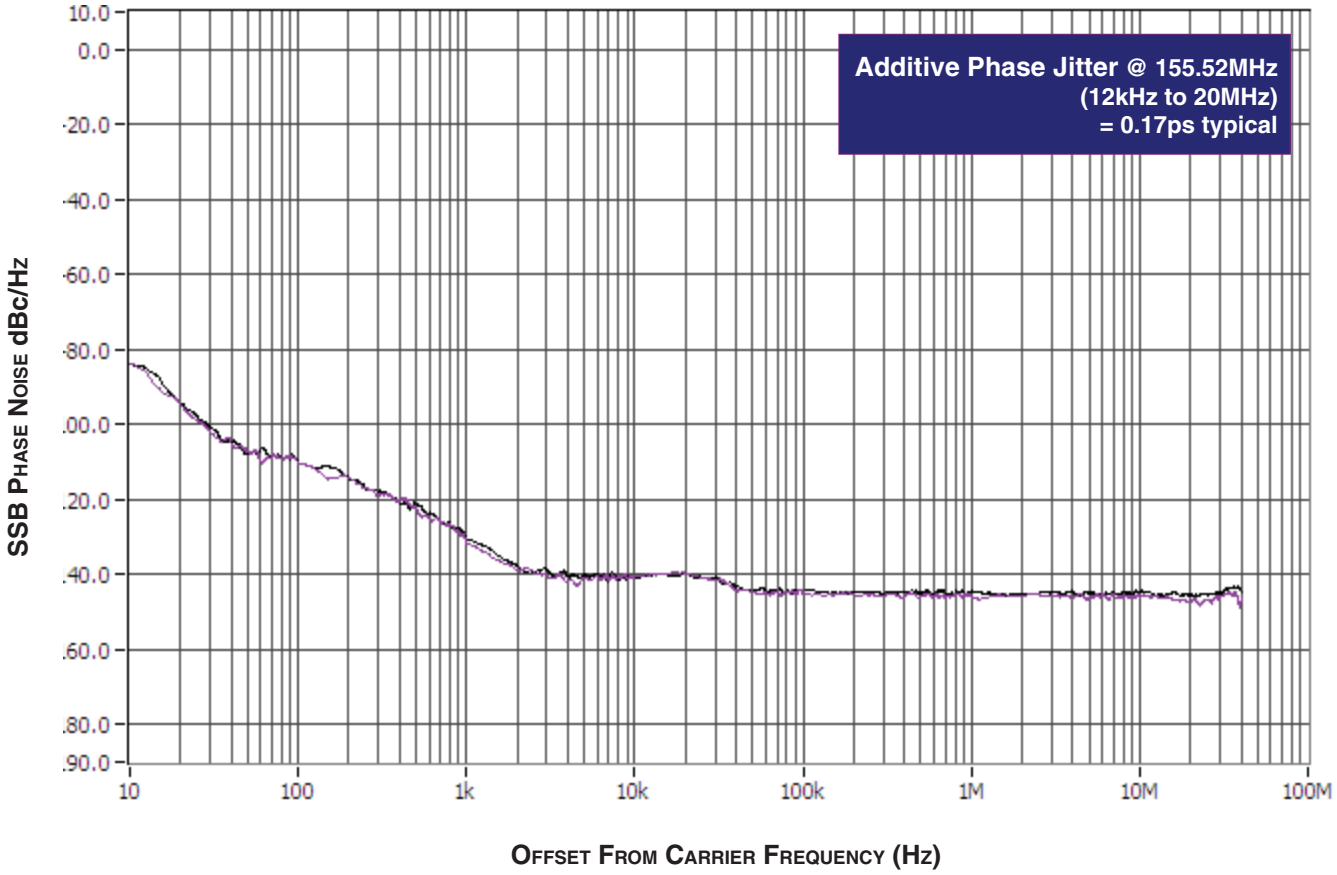
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				500	MHz
t_{PD}	Propagation Delay; NOTE 1	$f \leq 250MHz$	1		2	ns
*t*jit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section; NOTE 2	155.52MHz, (12kHz to 20MHz)		0.17		ps
*t*sk(o)	Output Skew; NOTE 3, 5				50	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 4, 5				250	ps
t_R / t_F	Output Rise/Fall Time	20% to 80% @ 50MHz	300		700	ps
odc	Output Duty Cycle		48	50	52	%

All parameters measured at 250MHz unless noted otherwise.
NOTE 1: Measured from the differential input crossing point to the differential output crossing point.
NOTE 2: Driving only one input clock.
NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential cross points.
NOTE 4: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.
NOTE 5: This parameter is defined in accordance with JEDEC Standard 65.

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Additive Phase Jitter

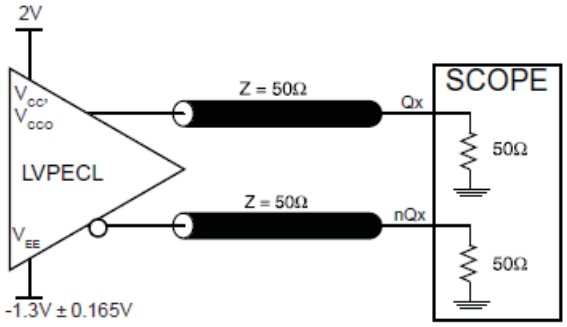
The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the ***dBc Phase Noise.*** This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a ***dBc*** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.



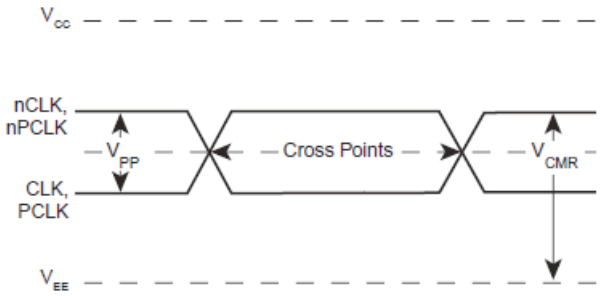
As with most timing specifications, phase noise measurements have issues. The primary issue relates to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This is illustrated above. The device meets the noise floor of what is shown, but can actually be lower. The phase noise is dependant on the input source and measurement equipment.

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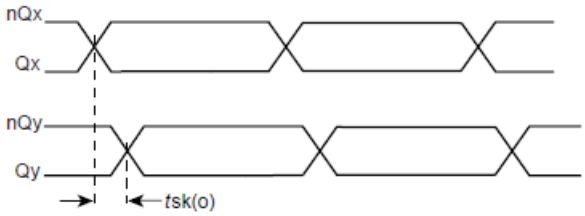
Parameter Measurement Information



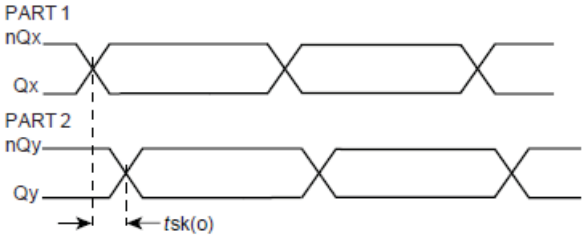
3.3V Output Load AC Test Circuit



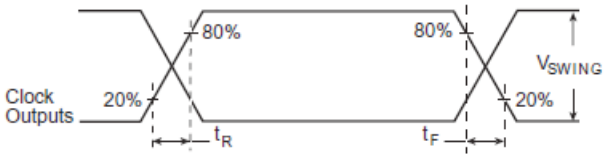
Differential Input Level



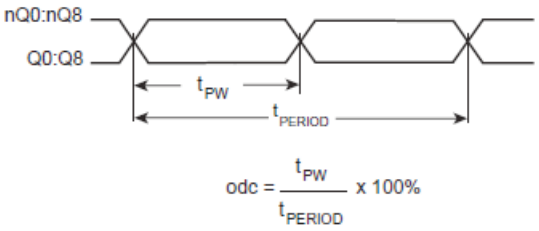
Output Skew



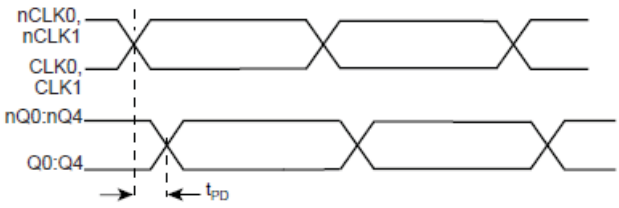
Part-to-Part Skew



Output Rise/Fall Time



Output Duty Cycle/Pulse Width/Period



Propagation Delay

Application Information

Wiring the Differential Input to Accept Single Ended Levels

Figure 2 shows how the differential input can be wired to accept single ended levels. The reference voltage V_REF ~ V_{cc}/2 is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and V_{cc} = 3.3V, V_REF should be 1.25V and R2/R1 = 0.609.

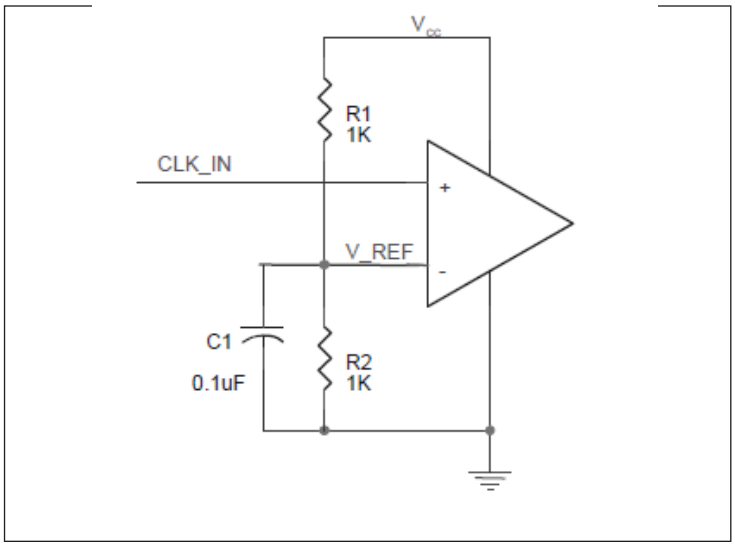


Figure 2. Single Ended Signal Driving Differential Input

Recommendations for Unused Input and Output Pins

Inputs:

CLK/nCLK Input:
For applications not requiring the use of the differential input, both CLK and nCLK can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from CLK to ground.

PCLK/nPCLK Input:
For applications not requiring the use of a differential input, both the PCLK and nPCLK pins can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from PCLK to ground.

LVCMOS Control Pins:
All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs:

LVPECL Outputs:
All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

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Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, SSTL, HCSL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. Figures 3A to 3E show interface examples for the HiPerClockS CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only.

Please consult with the vendor of the driver component to confirm the driver termination requirements. For example in *Figure 3A,* the input termination applies for IDT HiPerClockS LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

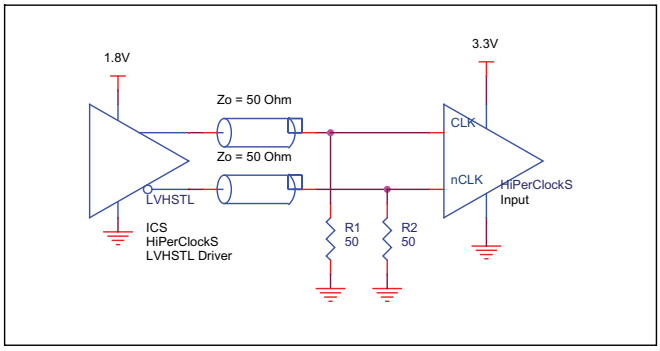


Figure 3A. HiPerClockS CLK/nCLK Input Driven by IDT HiPerClockS LVHSTL Driver

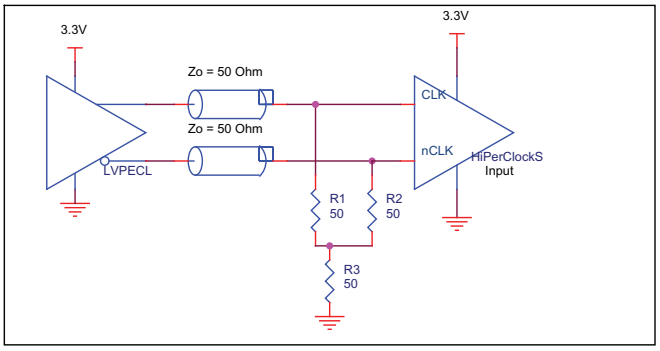


Figure 3B. HiPerClockS CLK/nCLK Input Driven by 3.3V LVPECL Driver

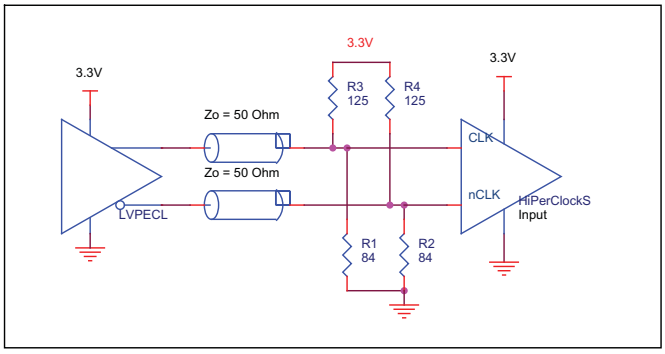


Figure 3C. HiPerClockS CLK/nCLK Input Driven by 3.3V LVPECL Driver

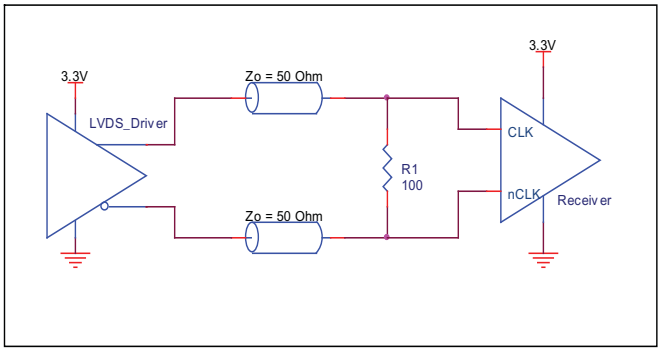


Figure 3D. HiPerClockS CLK/nCLK Input Driven by 3.3V LVDS Driver

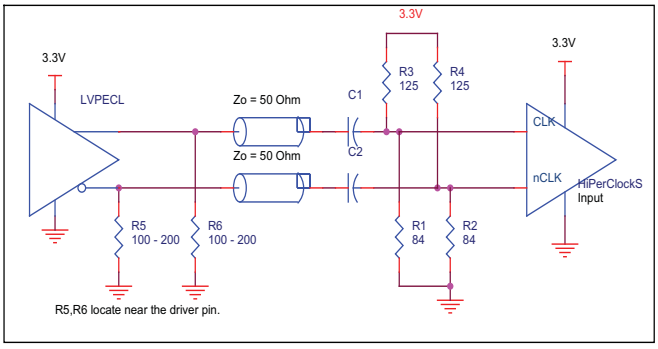


Figure 3E. HiPerClockS CLK/nCLK Input Driven by 3.3V LVPECL Driver with AC Couple

LVPECL Clock Input Interface

The PCLK /nPCLK accepts LVPECL, CML, SSTL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. *Figures 4A to 4E* show interface examples for the HiPerClockS PCLK/nPCLK input driven by the most common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

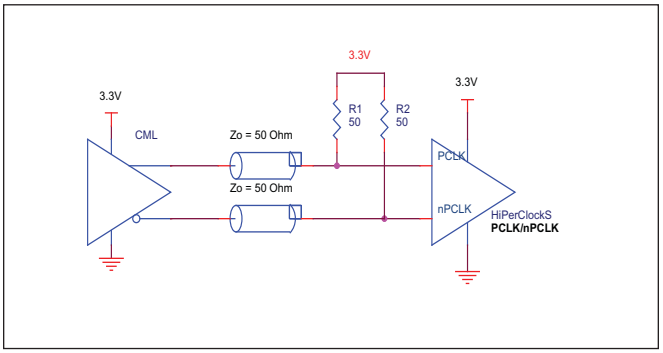


Figure 4A. HiPerClockS PCLK/nPCLK Input Driven by a CML Driver

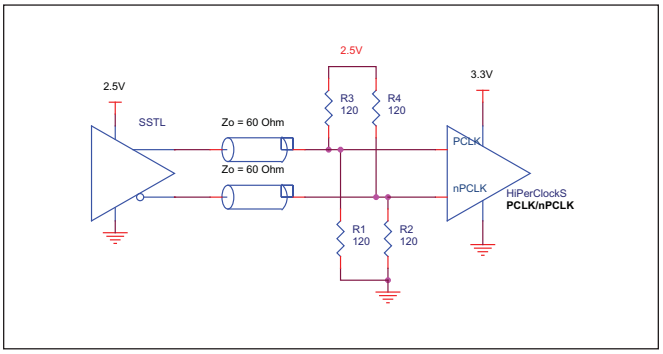


Figure 4B. HiPerClockS PCLK/nPCLK Input Driven by an SSTL Driver

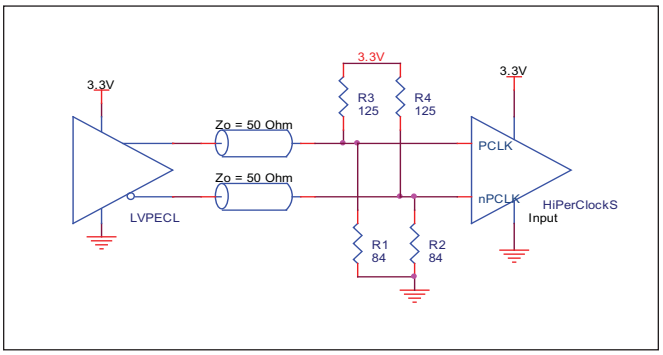


Figure 4C. HiPerClockS PCLK/nPCLK Input Driven by a 3.3V LVPECL Driver

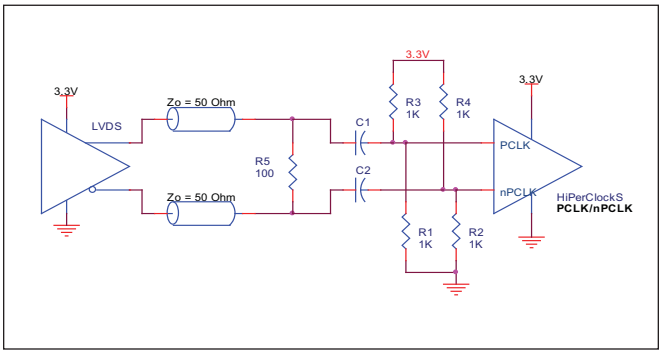


Figure 4D. HiPerClockS PCLK/nPCLK Input Driven by a 3.3V LVDS Driver

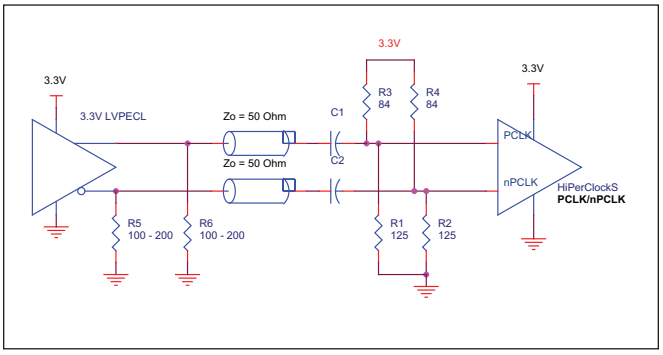


Figure 4E. HiPerClockS PCLK/nPCLK Input Driven by a 3.3V LVPECL Driver with AC Couple

Termination for LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 5A and 5B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

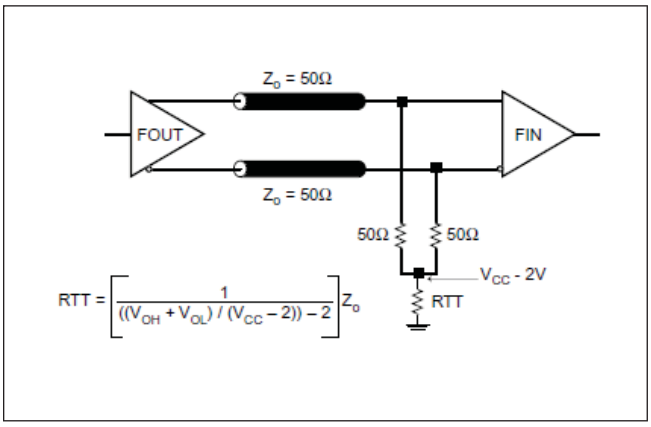


Figure 5A. LVPECL Output Termination

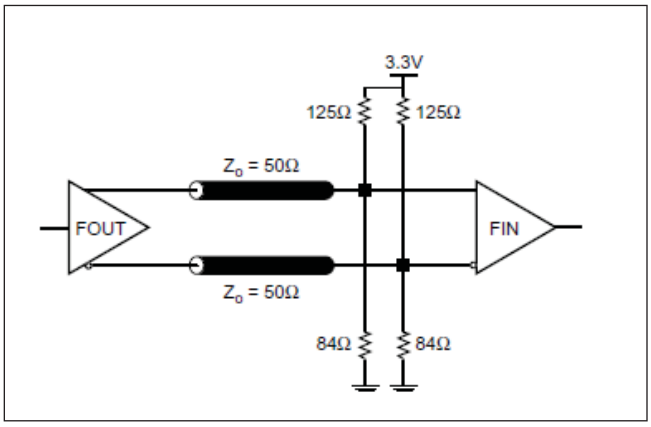


Figure 5B. LVPECL Output Termination

Power Considerations

This section provides information on power dissipation and junction temperature for the 8531-01.
Equations and example calculations are also provided.

1. Power Dissipation.
The total power dissipation for the 8531-01 is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{CC} = 3.3V + 5% = 3.465V, which gives worst case results.
NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power $(core)_{MAX} = V_{CC_MAX} * I_{EE_MAX}$ = 3.465V * 80mA = **277.2mW**
- Power $(outputs)_{MAX}$ = **30mW/Loaded Output pair**
  If all outputs are loaded, the total power is 9 * 30mW = **270mW**

  Total Power$_{_MAX}$ **(3.465V, with all outputs switching) = 277.2mW + 270mW =** 547.2mW

2. Junction Temperature.
Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd_total + T_A$

Tj = Junction Temperature

θ_{JA} = junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)
T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming a moderate air flow of 200 linear feet per minute and a multi-layer board, the appropriate value is 42.1°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 70°C with all outputs switching is:
70°C + 0.547W * 42.1°C/W = 93°C. This is well below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

Table 6. Thermal Resistance θ_{JA} for 32-pin LQFP Forced Convection

θ_{JA} by Velocity (Linear Feet per Minute)	0	200	500
Single-Layer PCB, JEDEC Standard Test Boards	67.8°C/W	55.9°C/W	50.1°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	47.9°C/W	42.1°C/W	39.4°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

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3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

LVPECL output driver circuit and termination are shown in *Figure 6.*

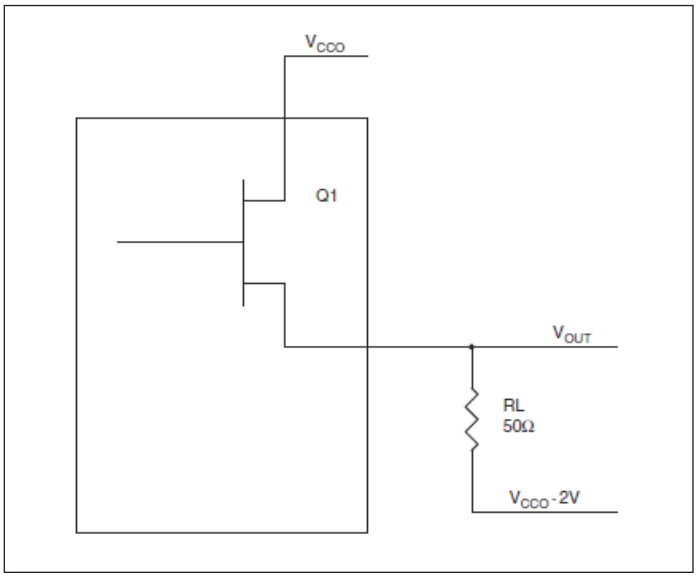


FIGURE 6. LVPECL DRIVER CIRCUIT AND TERMINATION

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of V_{CCO} - 2V.

- For logic high, $V_{OUT} = V_{OH_MAX} = \mathbf{V_{CCO_MAX} - 0.9V}$

  $(V_{CCO_MAX} - V_{OH_MAX}) = \mathbf{0.9V}$

- For logic low, $V_{OUT} = V_{OL_MAX} = \mathbf{V_{CCO_MAX} - 1.7V}$

  $(V_{CCO_MAX} - V_{OL_MAX}) = \mathbf{1.7V}$

Pd_H is power dissipation when the output drives high.
Pd_L is the power dissipation when the output drives low.

$Pd_H = [(V_{OH_MAX} – (V_{CCO_MAX} - 2V))/R_L] * (V_{CCO_MAX} - V_{OH_MAX}) = [(2V - (V_{CCO_MAX} - V_{OH_MAX}))/R_L] * (V_{CCO_MAX} - V_{OH_MAX}) =$
$[(2V - 0.9V)/50\Omega] * 0.9V =$ **19.8mW**

$Pd_L = [(V_{OL_MAX} – (V_{CCO_MAX} - 2V))/R_L] * (V_{CCO_MAX} - V_{OL_MAX}) = [(2V - (V_{CCO_MAX} - V_{OL_MAX}))/R_L] * (V_{CCO_MAX} - V_{OL_MAX}) =$
$[(2V - 1.7V)/50\Omega] * 1.7V =$ **10.2mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **30mW**

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RELIABILITY INFORMATION

TABLE 7. θ_{JA} VS. AIR FLOW TABLE FOR 32 LEAD LQFP

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	67.8°C/W	55.9°C/W	50.1°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	47.9°C/W	42.1°C/W	39.4°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TRANSISTOR COUNT

The transistor count for 8531-01 is: 632

Package Outline and Dimensions - Y Suffix for 32 Lead LQFP

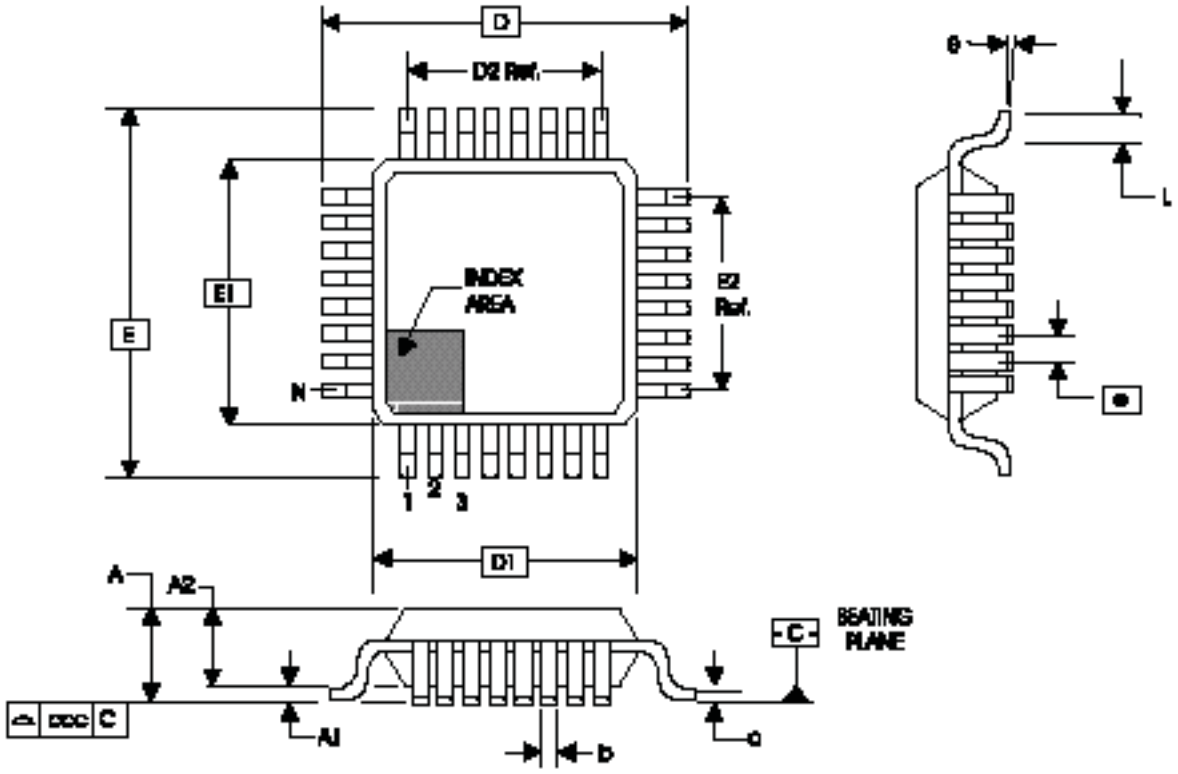


Table 8. Package Dimensions

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS			
SYMBOL	BBA		
	MINIMUM	NOMINAL	MAXIMUM
N		32	
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.30	0.37	0.45
c	0.09	--	0.20
D		9.00 BASIC	
D1		7.00 BASIC	
D2		5.60 Ref.	
E		9.00 BASIC	
E1		7.00 BASIC	
E2		5.60 Ref.	
e		0.80 BASIC	
L	0.45	0.60	0.75
θ	0°	--	7°
ccc	--	--	0.10

Reference Document: JEDEC Publication 95, MS-026

TABLE 9. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
8531AY-01LF	ICS8531AY01L	32 lead “Lead Free” LQFP	Tray	0°C to +70°C
8531AY-01LFT	ICS8531AY01L	32 lead “Lead Free” LQFP	Tape and Reel	0°C to +70°C

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REVISION HISTORY SHEET				
Rev	**Table**	**Page**	**Description of Change**	**Date**
B	4A 4C 4D 5	4 4 5 5	Separated LVCMOS rows into own table. Changed HSTL table to Differential table. Changed V_{PP} value from 0.1 Min. to 0.15 Min.0Changed V_{CMR} values from 0.13 Min, 1.3 Max. to 0.5 Min, V_{CC} - 0.85. In LVPECL table, changed V_{CMR} values from 0.7 Min, 2.5 Max. to 0.5 Min, V_{CC} - 0.85. Changed V_{OH} values from 1.9 Min., 2.3 Max. to V_{CC} - 1.4 Min., V_{CC} - 1.0 Max. Changed V_{OL} values from 1.2 Min, 1.6 Max. to V_{CC} - 2.0 Min, V_{CC} - 1.7 Max. Changed V_{SWING} values from 0.55 Min. to 0.6 Min. Changed tp_{LH} & tp_{HL} rows to t_{PD}. Values stayed same. t_R and t_F values changed from 100 Min, 600 Max. to 300 Min., 700 Max. Changed t_{DC} row to odc. Values stayed same. Deleted t_S and t_H rows.	6/15/01
B		1	Changed all V_{DDx} to V_{CCx}. Changed V_{CCO} to equal 3.3V ± 5% from 1.8V ± 0.2V. Updated Block Diagram.	6/18/01
B	4C 4D	4 5	Changed V_{CMR} value from 0.5 Min. to V_{EE} + 0.5 Min. Changed V_{PP} values from 0.15 Min, 1.3 Max, to 03. Min, 1 Max. Changed V_{CMR} values from 0.5 Min., V_{CC} - 0.85 Max. to V_{EE} + 1.5 Min., V_{CC} Max.	8/9/01
B		3 6 6, 7	Udated Figure 1, CLK_EN Timing Diagram. Updated Figure 2, Output Load Test Circuit. Revised labels on figures.	11/1/01
B		8	Added Termination for LVPECL Outputs section.	5/28/02
B		2 4 5	Pin Description table - V_{CC} description changed to “Core supply pin” from “Positive supply pin”. Power Supply Characteristics table - V_{CC} description changed to “Core Supply Voltage” from “Positive Supply Voltage”. Output Load Test Circuit diagram - corrected V_{EE} equation to read, V_{EE} = -1.3V ± 0.165V from V_{EE} = -1.3V ± 0.135V.	10/02/02
C	T2 T4A	2 4 4 7 8 9 10	Pin Characteristics table - changed C_{IN} 4pF max. to 4pF typical. Updated Absolute Maximum Ratings. Power Supply DC Characteristics table - changed I_{EE} 70mA max. to 80mA max and deleted 50mA typical. Updated LVPECL Output Termination drawings. Added Differential Clock Input Interface section. Added LVPECL Clock Input Interface section. Power Considerations - corrected Power Dissipation from 70mA to 80mA to correspond with I_{EE}. Updated format throughout the data sheet.	2/2/04
C	T9	14	Ordering Information Table - added Lead-Free part number.	10/15/04
D	T4D T9	5 7 15	LVPECL DC Characteristics - changed VSWING max. limit from 850mV to 1.0V. Added Recommendations for Unused Input and Output Pins. Ordering Information Table - added lead-free note.	6/23/06
E	1 T5	 5 6	Features Section - added RMS Phase Jitter bullet. AC Characteristics Table - add RMS Phase Jitter spec. Added Additve Phase Jitter Plot.	12/4/06
F	T4D	5 12 - 13	LVPECL DC Characteristics Table -corrected V_{OH} max. from V_{CCO} - 1.0V to V_{CCO} - 0.9V. Power Considerations - corrected power dissipation to reflect V_{OH} max in Table 4D.	4/11/07
F	T9	1 1 16	Removed ICS from the part number where needed. General Description - Removed ICS Chip and Hiperclocks. Features section - removed reference to leaded part. Ordering Information - removed quantity from tape and reel. Deleted LF note below the table. Updated header and footer.	1/19/16

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(Rev.1.0 Mar 2020)

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