LOW SKEW, 1-TO-4, CRYSTAL OSCILLATOR/ LVCMOS-TO-3.3V LVPECL FANOUT BUFFER

ICS8535-31

General Description

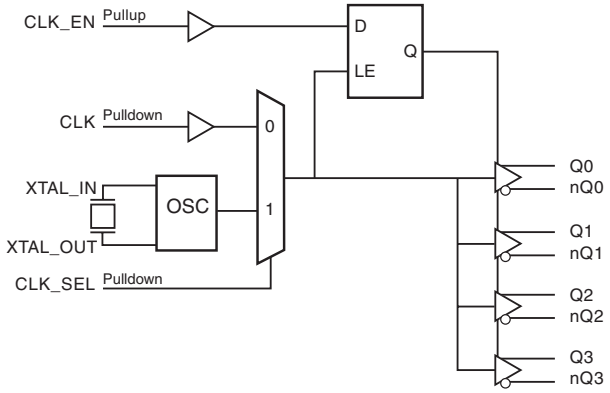
The ICS8535-31 is a low skew, high performance 1-to-4 3.3V Crystal Oscillator/LVCMOS-to-3.3V LVPECL fanout buffer and a member of the HiPerClockS™family of High Performance Clock Solutions from ICS. The ICS8535-31 has selectable single ended clock or crystal inputs. The single ended clock input accepts LVCMOS or LVTTL input levels and translate them to 3.3V LVPECL levels. The output enable is internally synchronized to eliminate runt pulses on the outputs during asynchronous assertion/deassertion of the clock enable pin.

Guaranteed output and part-to-part skew characteristics make the ICS8535-31 ideal for those applications demanding well defined performance and repeatability.

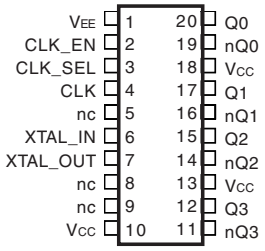
Features

- 4 differential 3.3V LVPECL outputs
- Selectable LVCMOS/LVTTL CLK or crystal inputs
- CLK can accept the following input levels: LVCMOS, LVTTL
- Maximum output frequency: 266MHz
- Output skew: 30ps (maximum)
- Part-to-part skew: 200ps (maximum)
- Propagation delay: 1.65ns (maximum)
- Additive phase jitter, RMS: 0.057ps (typical)
- 3.3V operating supply
- 0°C to 70°C ambient operating temperature
- Lead-Free package fully RoHS compliant
- Industrial Temperature information available upon request
- Replaces the ICS8535-11

Block Diagram



Pin Assignment



ICS8535-31
20-Lead TSSOP
6.5mm x 4.4mm x 0.92mm package body
G Package
Top View

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Table 1. Pin Descriptions

Number	Name	Type		Description
1	V_{EE}	Power		Negative supply pin.
2	CLK_EN	Input	Pullup	Synchronizing clock enable. When HIGH, clock outputs follows clock input. When LOW, Q outputs are forced low, nQ outputs are forced high. LVCMOS / LVTTL interface levels.
3	CLK_SEL	Input	Pulldown	Clock select input. When HIGH, selects XTAL inputs. When LOW, selects CLK input. LVCMOS / LVTTL interface levels.
4	CLK	Input	Pulldown	Clock input. LVCMOS / LVTTL interface levels.
5, 8, 9	nc	Unused		No connect.
6, 7	XTAL_IN, XTAL_OUT	Input		Crystal oscillator interface. XTAL_IN is the input. XTAL_OUT is the output.
10, 13, 18	V_{CC}	Power		Positive supply pins.
11, 12	nQ3, Q3	Output		Differential clock outputs. LVPECL interface levels.
14, 15	nQ2, Q2	Output		Differential clock outputs. LVPECL interface levels.
16, 17	nQ1, Q1	Output		Differential clock outputs. LVPECL interface levels.
19, 20	nQ0, Q0	Output		Differential clock outputs. LVPECL interface levels.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ

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TABLE 3A. CONTROL INPUT FUNCTION TABLE

Inputs			Outputs	
CLK_EN	**CLK_SEL**	**Selected Source**	**Q0:Q3**	**nQ0:nQ3**
0	0	CLK	Disabled; LOW	Disabled; HIGH
0	1	XTAL_IN, XTAL_OUT	Disabled; LOW	Disabled; HIGH
1	0	CLK	Enabled	Enabled
1	1	XTAL_IN, XTAL_OUT	Enabled	Enabled

After CLK_EN switches, the clock outputs are disabled or enabled following a rising and falling input clock or crystal oscillator edge as shown in *Figure* 1.
In the active mode, the state of the outputs are a function of the CLK input as described in Table 3B.

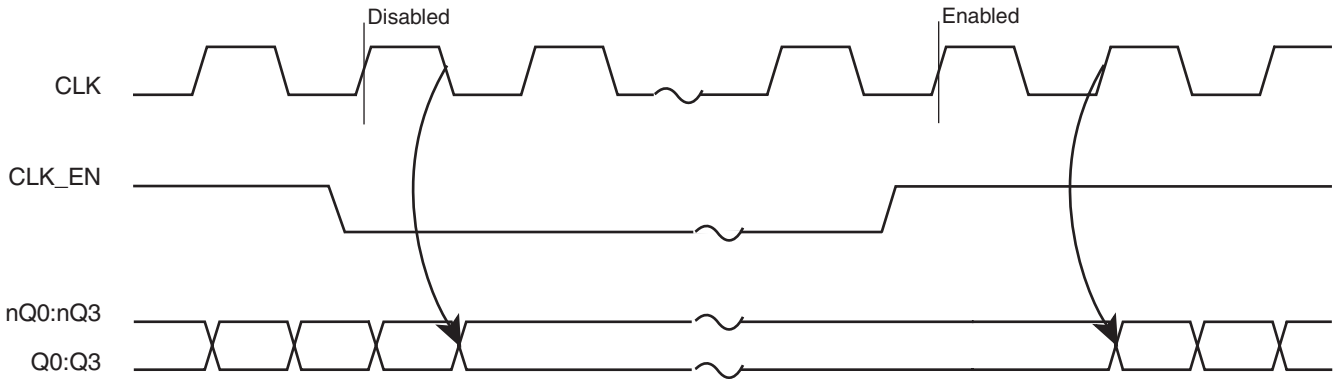


FIGURE 1. CLK_EN TIMING DIAGRAM

TABLE 3B. CLOCK INPUT FUNCTION TABLE

Inputs	Outputs	
CLK	**Q0:Q3**	**nQ0:nQ3**
0	LOW	HIGH
1	HIGH	LOW

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Absolute Maximum Ratings

Supply Voltage, V_{CC}	4.6V
Inputs, V_I	-0.5V to V_{CC} + 0.5V
Outputs, I_O	
Continuous Current	50mA
Surge Current	100mA
Package Thermal Impedance, θ_{JA}	73.2°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Table 4A. Power Supply DC Characteristics, V_{CC} = 3.3V±5%, TA = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Power Supply Voltage		3.135	3.3	3.465	V
I_{EE}	Power Supply Current				60	mA

Table 4B. LVCMOS / LVTTL DC Characteristics, V_{CC} = 3.3V±5%, TA = 0°C to 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			2		V_{CC} + 0.3V	V
V_{IL}	Input Low Voltage			-0.3		0.8	V
I_{IH}	Input High Current	CLK, CLK_SEL	V_{IN} = V_{CC} = 3.465V			150	µA
		CLK_EN	V_{IN} = V_{CC} = 3.465V			5	µA
I_{IL}	Input Low Current	CLK, CLK_SEL	V_{IN} = 0V, V_{CC} = 3.465V	-5			µA
		CLK_EN	V_{IN} = 0V, V_{CC} = 3.465V	-150			µA

Table 4C. LVPECL DC Characteristics, V_{CC} = 3.3V±5%, TA = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		V_{CC} - 1.4		V_{CC} - 0.9	V
V_{OL}	Output Low Voltage; NOTE 1		V_{CC} - 2.0		V_{CC} - 1.7	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.6		1.0	V

NOTE 1: Outputs terminated with 50Ω to V_{CC} - 2V.

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TABLE 5. CRYSTAL CHARACTERISTICS

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency		12		40	MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF
Drive Level				1	mW

TABLE 6. AC CHARACTERISTICS, V_{CC} = 3.3V±5%, T_A = 0°C TO 70°C

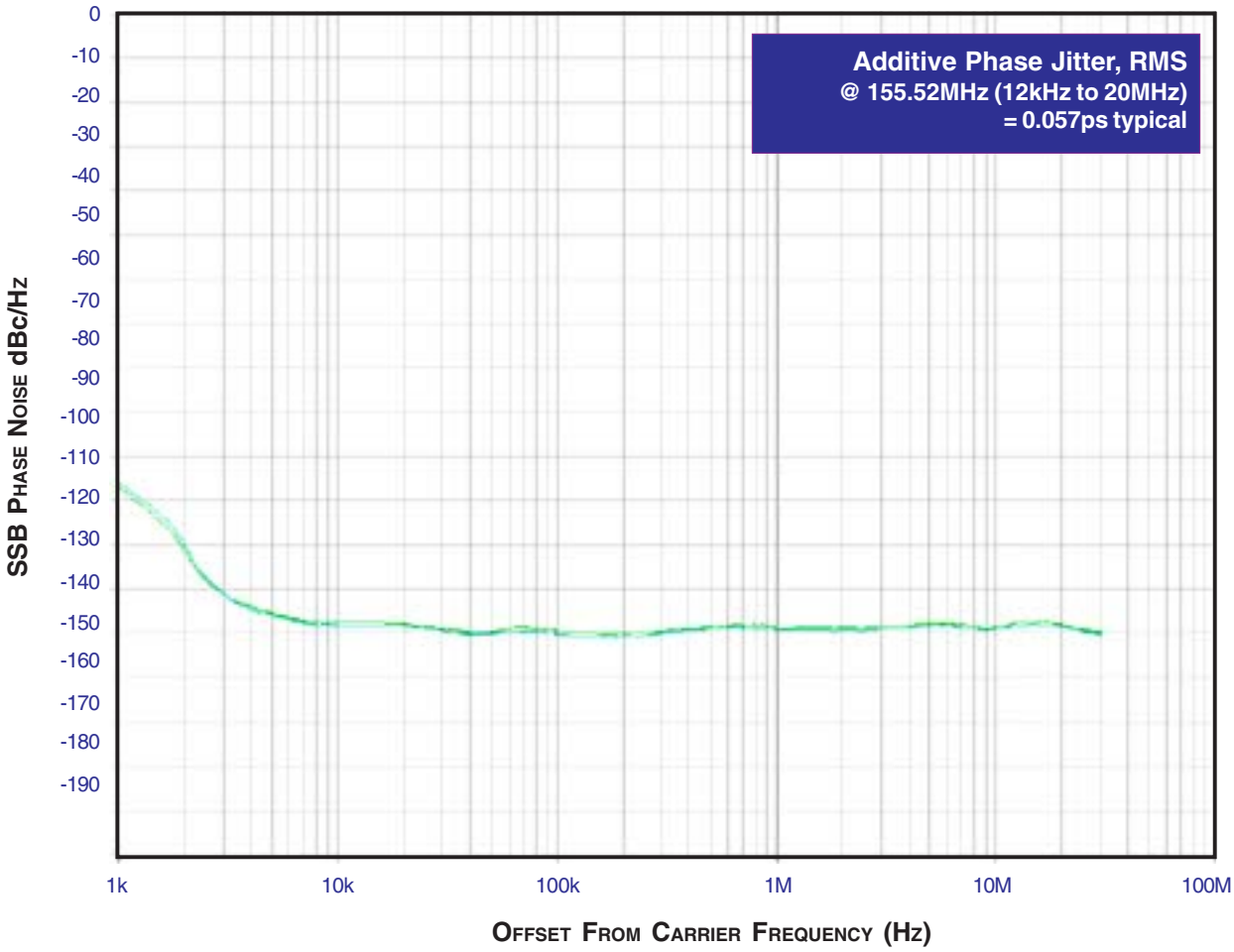
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				266	MHz
t_{PD}	Propagation Delay; NOTE 1		1.45		1.65	ns
*t*jit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section	155.52MHz, (Integration Range: 12kHz - 20MHz)		0.057		ps
*t*sk(o)	Output Skew; NOTE 2, 4				30	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 3, 4				200	ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	300		600	ps
odc	Output Duty Cycle		46		54	%

All parameters measured at $f \leq$ 266MHz unless noted otherwise.
NOTE 1: Measured from the V_{CC}/2 of the input to the differential output crossing point.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions.
Measured at the output differential cross points.
NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

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Additive Phase Jitter

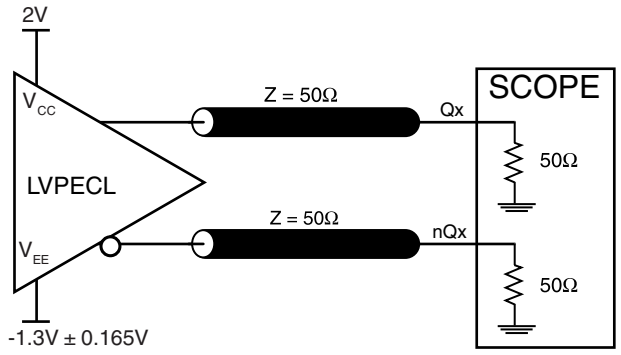
The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the ***dBc Phase Noise.*** This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a ***dBc*** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.



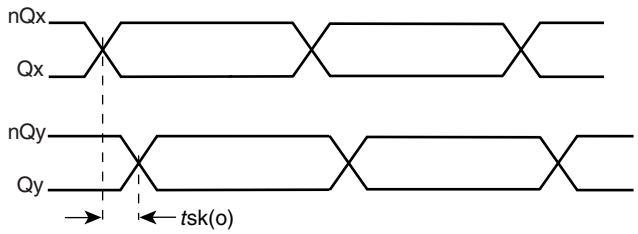
As with most timing specifications, phase noise measurements have issues. The primary issue relates to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This is illustrated above. The device meets the noise floor of what is shown, but can actually be lower. The phase noise is dependant on the input source and measurement equipment.

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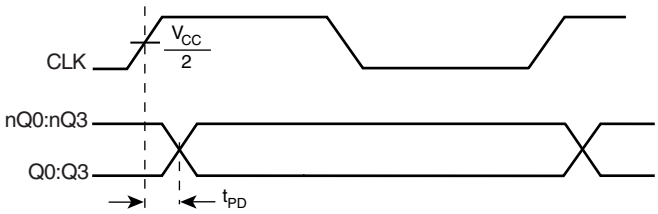
Parameter Measurement Information



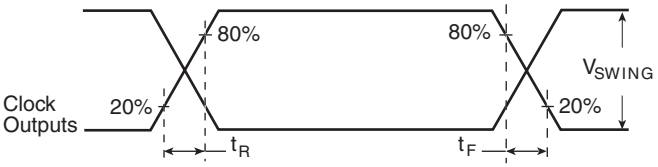
3.3V Output Load AC Test Circuit



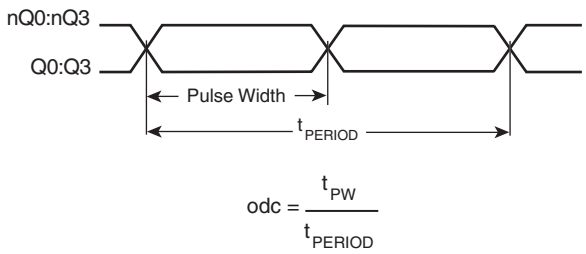
Output Skew



Propagation Delay



Output Rise/Fall Time



$$odc = \frac{t_{PW}}{t_{PERIOD}}$$

Output Duty Cycle/Pulse Width/Period

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APPLICATION INFORMATION

TERMINATION FOR LVPECL OUTPUTS

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 2A and 2B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

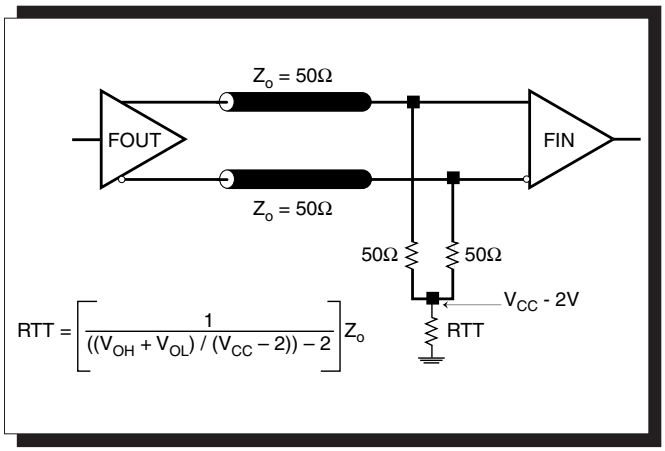


FIGURE 2A. LVPECL OUTPUT TERMINATION

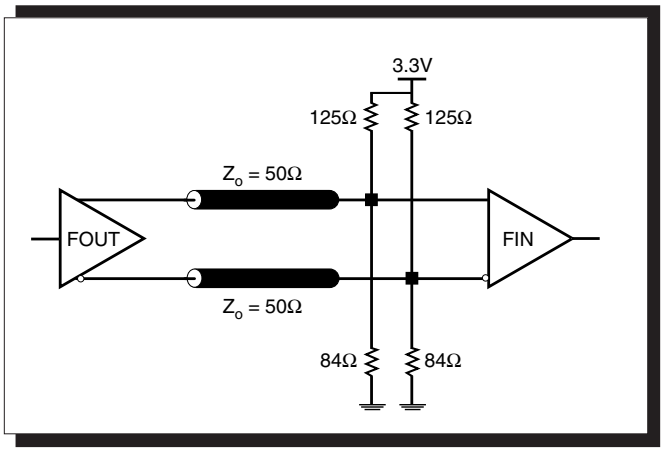


FIGURE 2B. LVPECL OUTPUT TERMINATION

CRYSTAL INPUT INTERFACE

The ICS8535-31 has been characterized with 18pF parallel resonant crystals. The capacitor values, C1 and C2, shown in *Figure 3* below were determined using an 18pF parallel resonant crystal and were chosen to minimize the ppm error. These same capacitor values will tune any 18pF parallel resonant crystal over the frequency range and other parameters specified in this data sheet. The optimum C1 and C2 values can be slightly adjusted for different board layouts.

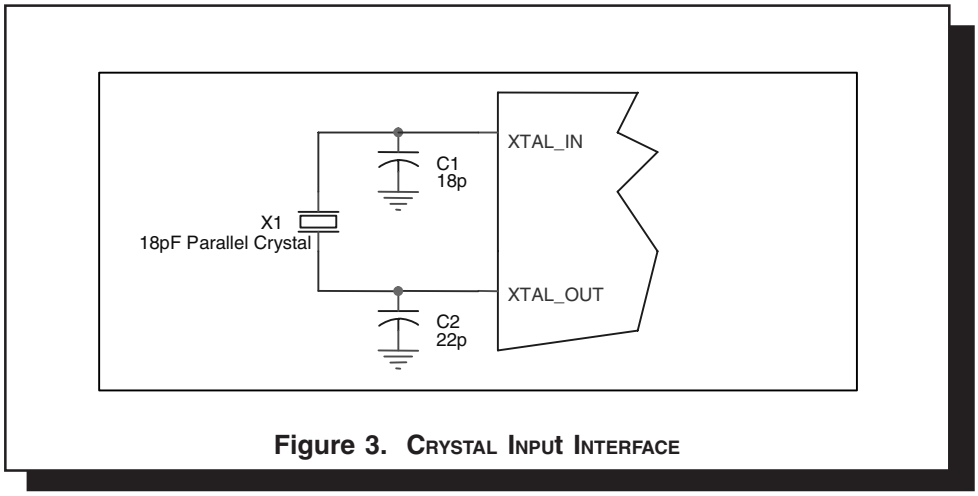


Figure 3. CRYSTAL INPUT INTERFACE

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Power Considerations

This section provides information on power dissipation and junction temperature for the ICS8535-31.
Equations and example calculations are also provided.

1. Power Dissipation.
The total power dissipation for the ICS8535-31 is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{CC} = 3.3V + 5% = 3.465V, which gives worst case results.
NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)$_{MAX}$ = V_{CC_MAX} * I_{EE_MAX} = 3.465V * 60mA = **207.9mW**
- Power (outputs)$_{MAX}$ = **30mW/Loaded Output pair**
  If all outputs are loaded, the total power is 4 * 30mW = **120mW**

Total Power$_{_MAX}$ (3.465V, with all outputs switching) = 207.9mW + 120mW **= 327.9mW**

2. Junction Temperature.
Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming a moderate air flow of 200 linear feet per minute and a multi-layer board, the appropriate value is 66.6°C/W per Table 7 below.

Therefore, Tj for an ambient temperature of 70°C with all outputs switching is:
70°C + 0.328W * 66.6°C/W = 92°C. This is well below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

Table 7. Thermal Resistance θ_{JA} for 20-pin TSSOP, Forced Convection

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	114.5°C/W	98.0°C/W	88.0°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	73.2°C/W	66.6°C/W	63.5°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

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3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

LVPECL output driver circuit and termination are shown in *Figure 4.*

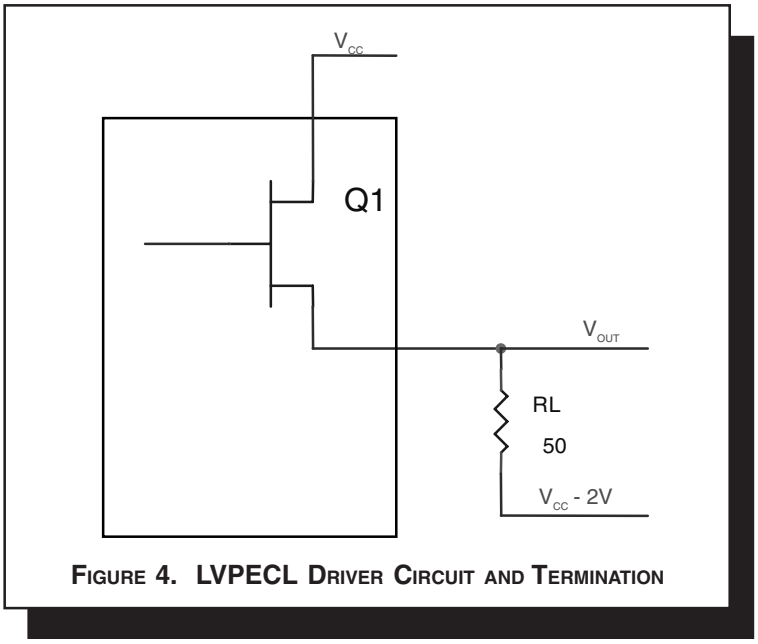


FIGURE 4. LVPECL DRIVER CIRCUIT AND TERMINATION

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of V_{CC} - 2V.

- For logic high, $V_{OUT} = V_{OH_MAX} = \mathbf{V_{CC_MAX} – 0.9V}$

  $(V_{CC_MAX} - V_{OH_MAX}) = \mathbf{0.9V}$

- For logic low, $V_{OUT} = V_{OL_MAX} = \mathbf{V_{CC_MAX} – 1.7V}$

  $(V_{CC_MAX} - V_{OL_MAX}) = \mathbf{1.7V}$

Pd_H is power dissipation when the output drives high.
Pd_L is the power dissipation when the output drives low.

$Pd_H = [(V_{OH_MAX} – (V_{CC_MAX} - 2V))/R_L] * (V_{CC_MAX} - V_{OH_MAX}) = [(2V - (V_{CC_MAX} - V_{OH_MAX}))/R_L] * (V_{CC_MAX} - V_{OH_MAX}) =$
$[(2V - 0.9V)/50\Omega] * 0.9V =$ **19.8mW**

$Pd_L = [(V_{OL_MAX} – (V_{CC_MAX} - 2V))/R_L] * (V_{CC_MAX} - V_{OL_MAX}) = [(2V - (V_{CC_MAX} - V_{OL_MAX}))/R_L] * (V_{CC_MAX} - V_{OL_MAX}) =$
$[(2V - 1.7V)/50\Omega] * 1.7V =$ **10.2mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **30mW**

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Reliability Information

Table 8. θ_{JA} vs. Air Flow Table for 20 Lead TSSOP

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	114.5°C/W	98.0°C/W	88.0°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	73.2°C/W	66.6°C/W	63.5°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

Transistor Count

The transistor count for ICS8535-31 is: 428

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Package Outline - G Suffix for 20 Lead TSSOP

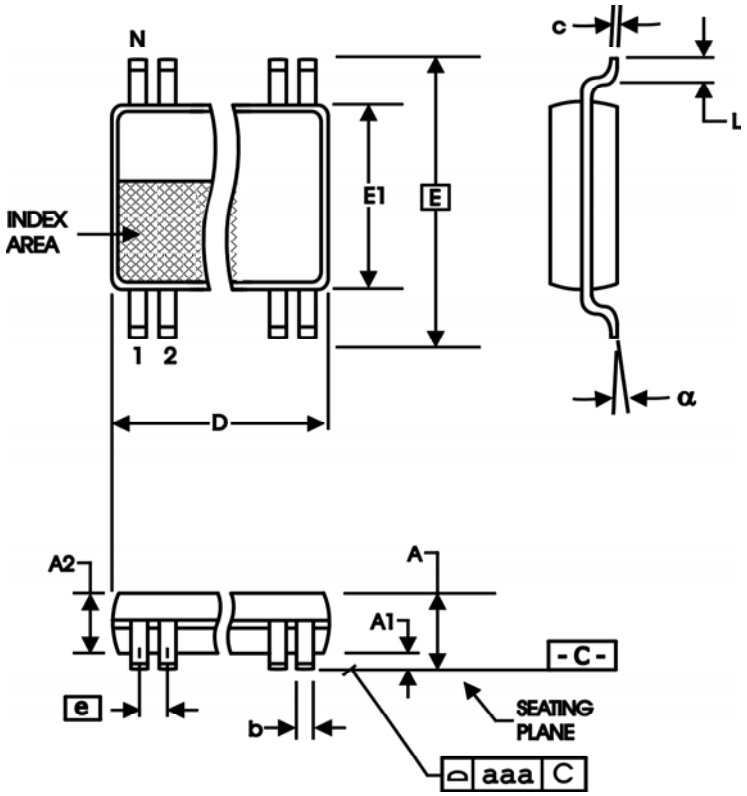


Table 9. Package Dimensions

SYMBOL	Millimeters	
	MIN	MAX
N	20	
A	--	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	6.40	6.60
E	6.40 BASIC	
E1	4.30	4.50
e	0.65 BASIC	
L	0.45	0.75
α	0°	8°
aaa	--	0.10

Reference Document: JEDEC Publication 95, MO-153

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TABLE 10. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
8535AG-31	ICS8535AG-31	20 lead TSSOP	tube	0°C to 70°C
8535AG-31T	ICS8535AG-31	20 lead TSSOP	2500 tape & reel	0°C to 70°C
8535AG-31LF	ICS8535AG31L	20 lead "Lead-Free" TSSOP	tube	0°C to 70°C
8535AG-31LFT	ICS8535AG31L	20 lead "Lead-Free" TSSOP	2500 tape & reel	0°C to 70°C

NOTE: Parts that are ordered with an “LF” suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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REVISION HISTORY SHEET				
Rev	**Table**	**Page**	**Description of Change**	**Date**
B	T6	1 5	Features Section - corrected Part-to-Part Skew bullet from 100ps max. to 200ps max. AC Characteristics Table - corrected Part-to-Part Skew from 100ps max. to 200ps max.	4/29/05

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