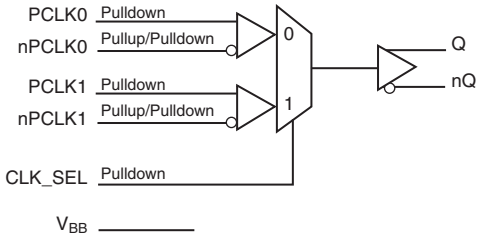
General Description

The 853S01 is a high performance 2:1 Differential-to-LVPECL Multiplexer. The 853S01 can also perform differential translation because the differential inputs accept LVPECL, LVDS and CML levels. The 853S01 is packaged in a small 3mm x 3mm 16 VFQFN package, making it ideal for use on space constrained boards.

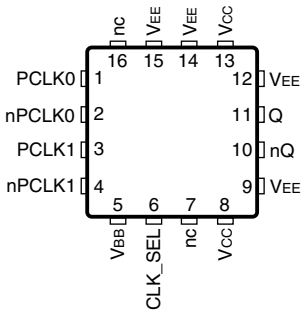
Features

- One LVPECL output pair
- Two selectable differential LVPECL clock inputs
- PCLKx, nPCLKx pairs can accept the following differential input levels: LVPECL, LVDS, CML
- Translates LVCMOS/LVTTL input signals to LVPECL levels by using a resistor bias network on nPCLKx, nPCLKx
- Part-to-part skew: 150ps (maximum)
- Propagation delay: 490ps (maximum)
- Full 3.3V or 2.5V operating supply
- -40°C to 85°C ambient operating temperature
- Available in lead-free (RoHS 6) packages

Block Diagram

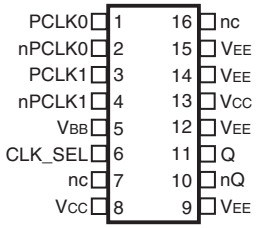


Pin Assignments



ICS853S01I

16-Lead VFQFN
3mm x 3mm x 0.925mm package body
K Package
Top View



853S01

16-Lead TSSOP
4.4mm x 5.0mm x 0.925mm package body
G Package
Top View

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Table 1. Pin Descriptions

Number	Name	Type		Description
1	PCLK0	Input	Pulldown	Non-inverting differential LVPECL clock input.
2	nPCLK0	Input	Pullup/ Pulldown	Inverting differential LVPECL clock input. $V_{CC}/2$ default when left floating.
3	PCLK1	Input	Pulldown	Non-inverting differential LVPECL clock input.
4	nPCLK1	Input	Pullup/ Pulldown	Inverting differential LVPECL clock input. $V_{CC}/2$ default when left floating.
5	V_{BB}	Output		Bias voltage.
6	CLK_SEL	Input	Pulldown	Clock select input. When HIGH, selects PCLK1, nPCLK1 inputs. When LOW, selects PCLK0, nPCLK0 inputs. LVCMOS/LVTTL interface levels.
7, 16	nc	Unused		No connect.
8, 13	V_{CC}	Power		Positive supply pins.
9, 12, 14, 15	V_{EE}	Power		Negative supply pins.
10, 11	nQ, Q	Output		Differential output pair. LVPECL interface levels.

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			2		pF
$R_{PULLDOWN}$	Input Pulldown Resistor			37		kΩ
R_{PULLUP}	Input Pullup Resistor			37		kΩ

Function Tables

Table 3. Control Input Function Table

CLK_SEL	Input Selected
0	PCLK0, nPCLK0
1	PCLK1, nPCLK1

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Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{CC}	4.6V
Inputs, V_I	-0.5V to V_{CC} + 0.5V
Outputs, I_O Continuous Current Surge Current	 50mA 100mA
V_{BB} Sink/Source, I_{BB}	±0.5mA
Package Thermal Impedance, θ_{JA} 16 VFQFN 16 TSSOP	 74.7°C/W (0 mps) 100°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, V_{CC} = 3.3V±5%; V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Positive Supply Voltage		3.135	3.3	3.465	V
I_{EE}	Power Supply Current				26	mA

Table 4B. Power Supply DC Characteristics, V_{CC} = 2.5V±5%; V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Positive Supply Voltage		2.375	2.5	2.625	V
I_{EE}	Power Supply Current				24	mA

Table 4C. LVCMOS/LVTTL DC Characteristics, V_{CC} = 3.3V±5% or 2.5V±5%; V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		V_{CC} = 3.3V	2.2		V_{CC} + 0.3	V
			V_{CC} = 2.5V	1.7		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage		V_{CC} = 3.3V	-0.3		0.8	V
			V_{CC} = 2.5V	-0.3		0.7	V
I_{IH}	Input High Current	CLK_SEL	V_{CC} = V_{IN} = 3.465V or 2.625V			150	µA
I_{IL}	Input Low Current	CLK_SEL	V_{CC} = 3.465V or 2.625V, V_{IN} = 0V	-10			µA

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Table 4D. LVPECL DC Characteristics, V_{CC} = 3.3V±5%; V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	PCLK0, PCLK1, nPCLK0, nPCLK1	$V_{CC} = V_{IN}$ = 3.465V			150	µA
I_{IL}	Input Low Current	PCLK0, PCLK1	V_{CC} = 3.465V, V_{IN} = 0V	-10			µA
		nPCLK0, nPCLK1	V_{CC} = 3.465V, V_{IN} = 0V	-150			µA
V_{PP}	Peak-to-Peak Voltage; NOTE 1			150		1200	mV
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			1.2		V_{CC}	V
V_{OH}	Output High Voltage; NOTE 3			V_{CC} – 1.125		V_{CC} – 0.875	V
V_{OL}	Output Low Voltage; NOTE 3			V_{CC} – 1.895		V_{CC} – 1.62	V
V_{SWING}	Peak-to-Peak Output Voltage Swing			0.495		0.975	V
V_{BB}	Bias Voltage			1.695		2.145	V

NOTE 1: V_{IL} should not be less than V_{EE} – 0.3V.
NOTE 2: Common mode input voltage is defined as V_{IH}.
NOTE 3: Outputs terminated with 50Ω to V_{CC} – 2V.

Table 4E. LVPECL DC Characteristics, V_{CC} = 2.5V±5%; V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	PCLK0, PCLK1, nPCLK0, nPCLK1	$V_{CC} = V_{IN}$ = 2.625V			150	µA
I_{IL}	Input Low Current	PCLK0, PCLK1	V_{CC} = 2.625V, V_{IN} = 0V	-10			µA
		nPCLK0, nPCLK1	V_{CC} = 2.625V, V_{IN} = 0V	-150			µA
V_{PP}	Peak-to-Peak Voltage; NOTE 1			150		1200	mV
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			1.2		V_{CC}	V
V_{OH}	Output High Voltage; NOTE 3			V_{CC} – 1.125		V_{CC} – 0.875	V
V_{OL}	Output Low Voltage; NOTE 3			V_{CC} – 1.895		V_{CC} – 1.62	V
V_{SWING}	Peak-to-Peak Output Voltage Swing			0.495		0.975	V
V_{BB}	Bias Voltage			0.935		1.305	V

NOTE 1: V_{IL} should not be less than V_{EE} – 0.3V.
NOTE 2: Common mode input voltage is defined as V_{IH}.
NOTE 3: Outputs terminated with 50Ω to V_{CC} – 2V.

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AC Electrical Characteristics

Table 5A. AC Characteristics, V_{CC} = 3.3V±5%; V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency				2.5	GHz
t_{PD}	Propagation Delay; NOTE 1		240		490	ps
*t*sk(i)	Input Skew				40	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 2, 3				150	ps
tjit	Buffer Additive Phase Jitter, RMS, refer to Additive Phase Jitter section; NOTE 4	622MHz, Integration Range: 12kHz - 20MHz		0.024		ps
t_R / t_F	Output Rise/ Fall Time	20% to 80%	100		240	ps
MUX_{ISOL}	MUX Isolation; NOTE 5	f_{OUT} = 622MHz		81		dB

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE: All parameters measured at $f \leq$ 1.0GHz unless otherwise noted.
NOTE 1: Measured from the differential input crossing point to the differential output crossing point.
NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltage, same temperature, same frequency and with equal load conditions at the same temperature. Using the same type of inputs on each device, the outputs are measured at the differential cross points.
NOTE 4: Driving only one input clock.
NOTE 5: Q, nQ output measured differentially. See *Parameter Measurement Information* for MUX Isolation diagram

Table 5B. AC Characteristics, V_{CC} = 2.5V±5%; V_{EE} = 0V, T_A = -40°C to 85°C

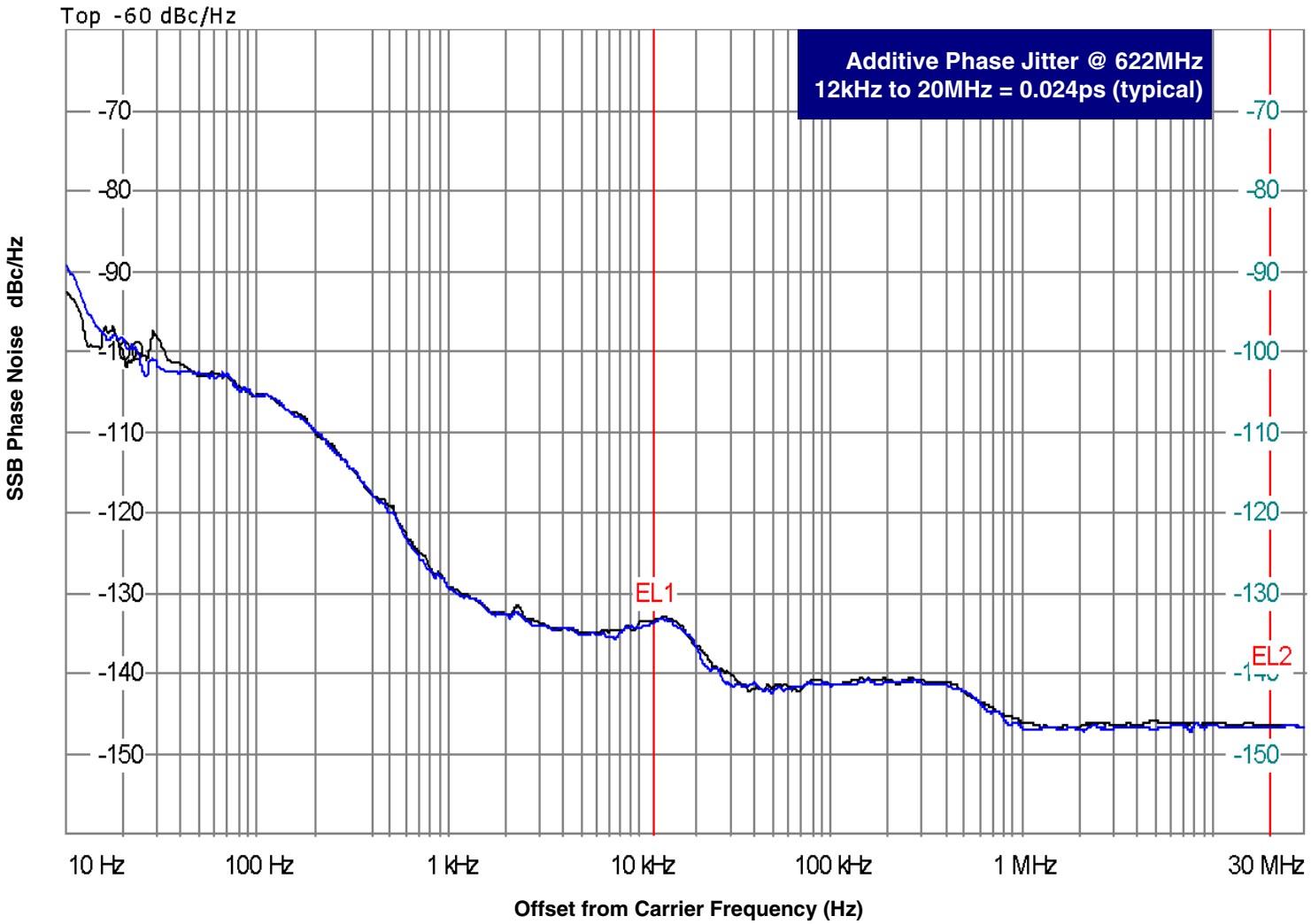
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency				2.5	GHz
t_{PD}	Propagation Delay; NOTE 1		240		490	ps
*t*sk(i)	Input Skew				40	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 2, 3				150	ps
tjit	Buffer Additive Phase Jitter, RMS, refer to Additive Phase Jitter section; NOTE 4	622MHz, Integration Range: 12kHz - 20MHz		0.024		ps
t_R / t_F	Output Rise/ Fall Time	20% to 80%	100		240	ps
MUX_{ISOL}	MUX Isolation; NOTE 5	f_{OUT} = 622MHz		81		dB

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE: All parameters measured at $f \leq$ 1.0GHz unless otherwise noted.
NOTE 1: Measured from the differential input crossing point to the differential output crossing point.
NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltage, same temperature, same frequency and with equal load conditions at the same temperature. Using the same type of inputs on each device, the outputs are measured at the differential cross points.
NOTE 4: Driving only one input clock.
NOTE 5: Q, nQ output measured differentially. See *Parameter Measurement Information* for MUX Isolation diagram

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Additive Phase Jitter

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the ***dBc Phase Noise.*** This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a ***dBc*** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.

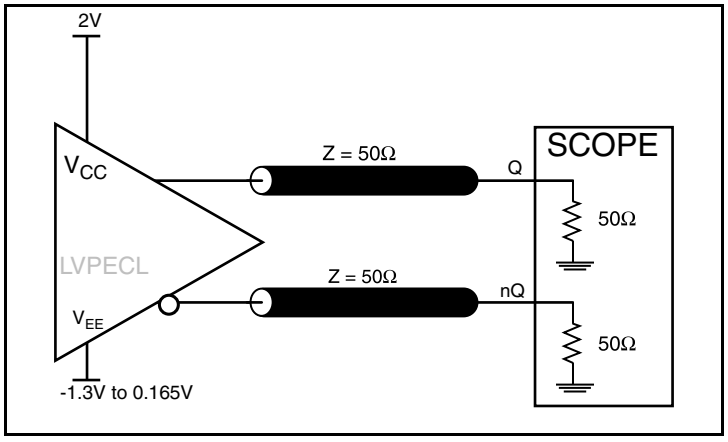


As with most timing specifications, phase noise measurements has issues relating to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This is illustrated above. The device meets the noise floor of what is shown, but can actually be lower. The phase noise is dependent on the input source and measurement equipment.

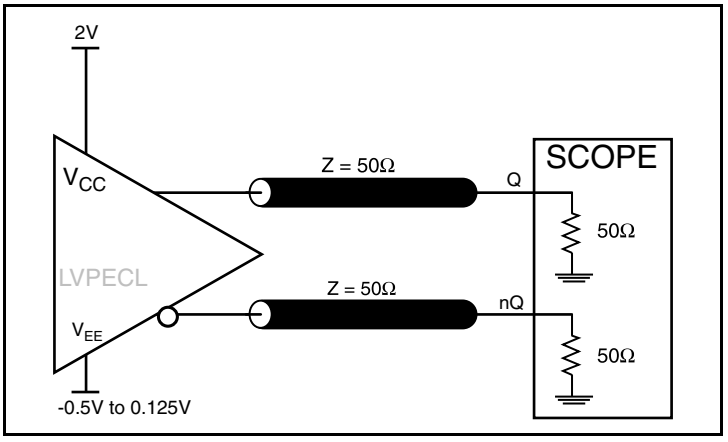
The source generator used is, "IFR2042 10kHz – 56.4GHz Low Noise Signal Generator as external input to an Agilent 8133A 3GHz Pulse Generator".

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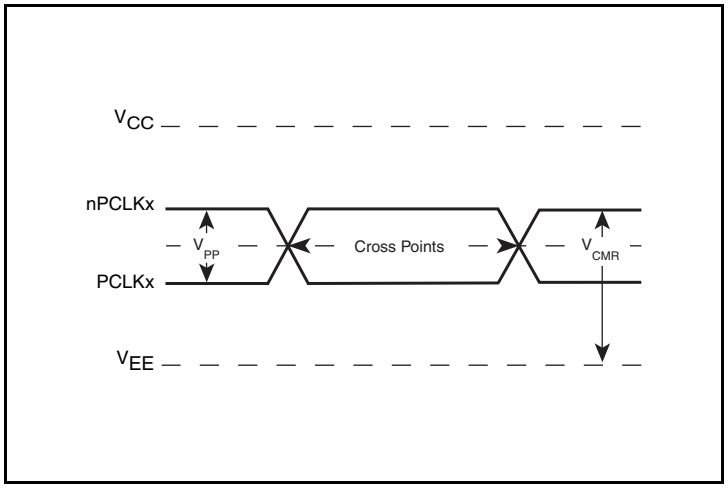
Parameter Measurement Information



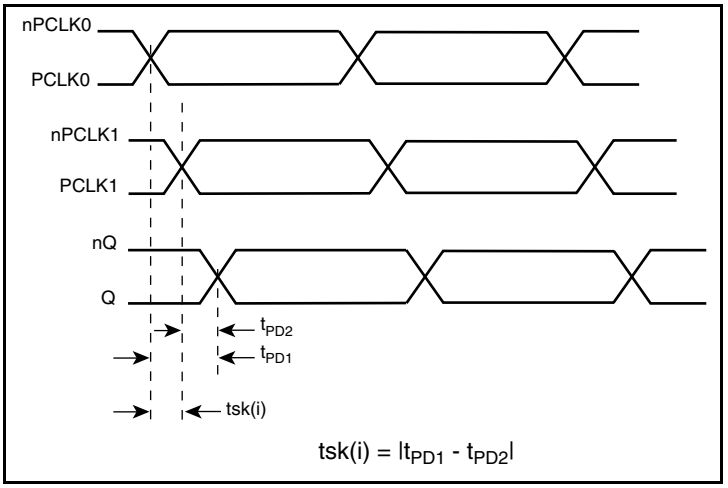
3.3V LVPECL Output Load AC Test Circuit



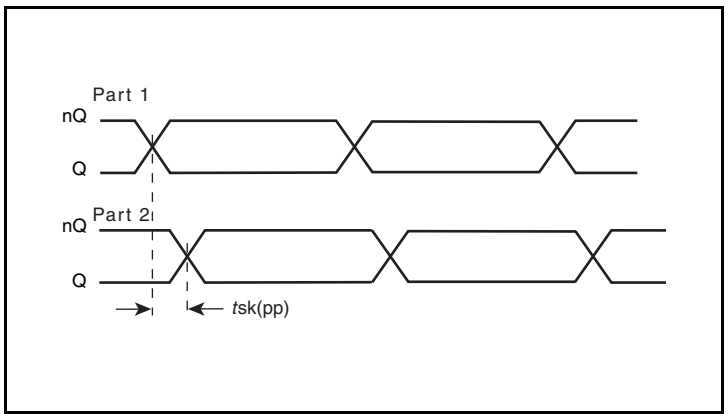
2.5V LVPECL Output Load AC Test Circuit



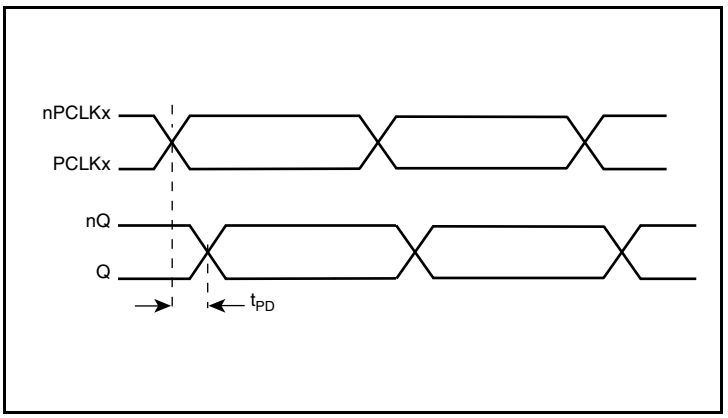
Differential Input Level



Input Skew

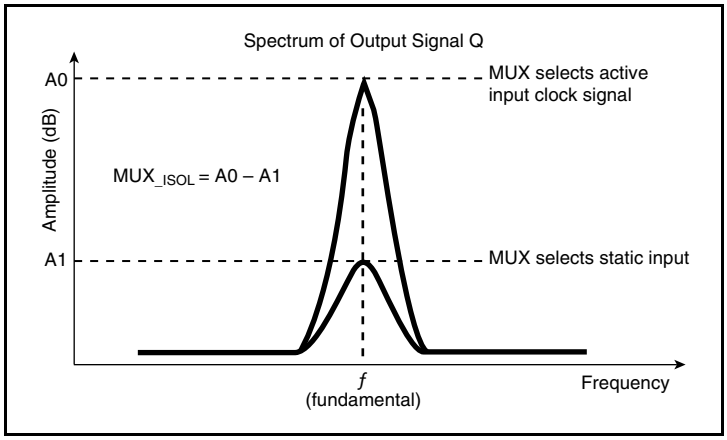


Part-to-Part Skew

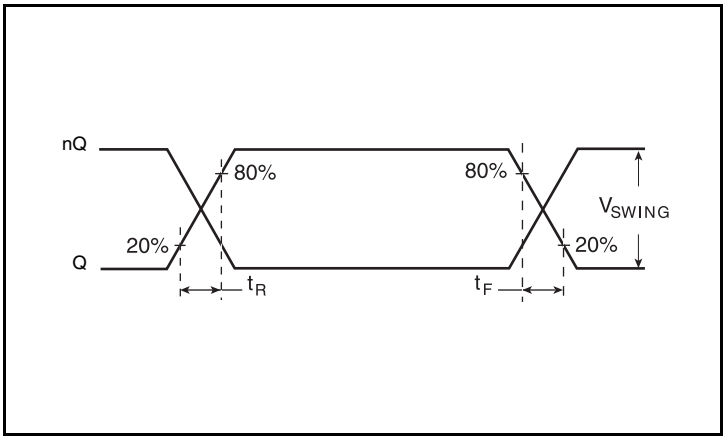


Propagation Delay

Parameter Measurement Information, continued



MUX Isolation



Output Rise/Fall Time

Applications Information

Wiring the Differential Input to Accept Single-Ended Levels

Figure 1A shows how a differential input can be wired to accept single ended levels. The reference voltage $V_{REF} = V_{CC}/2$ is generated by the bias resistors R1 and R2. The bypass capacitor (C1) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of R1 and R2 might need to be adjusted to position the V_{REF} in the center of the input voltage swing. For example, if the input clock swing is 2.5V and V_{CC} = 3.3V, R1 and R2 value should be adjusted to set V_{REF} at 1.25V. The values below are for when both the single ended swing and V_{CC} are at the same voltage. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways. First, R3 and R4 in parallel should equal the transmission line impedance. For most 50Ω applications, R3 and R4 can be 100Ω. The values of the resistors can be increased to reduce the loading for slower and weaker LVCMOS driver. When using single-ended signaling, the noise rejection benefits of differential signaling are reduced. Even though the differential input can handle full rail LVCMOS signaling, it is recommended that the amplitude be reduced. The datasheet specifies a lower differential amplitude, however this only applies to differential signals. For single-ended applications, the swing can be larger, however V_{IL} cannot be less than -0.3V and V_{IH} cannot be more than V_{CC} + 0.3V. Though some of the recommended components might not be used, the pads should be placed in the layout. They can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a differential signal.

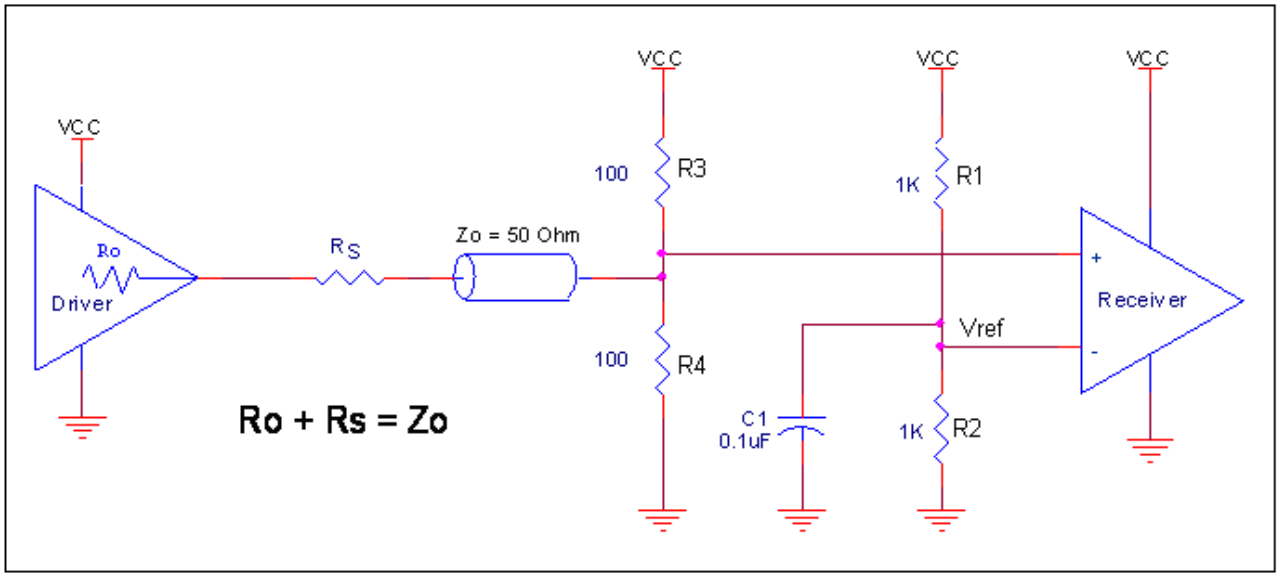


Figure 1A. Recommended Schematic for Wiring a Differential Input to Accept Single-ended Levels

Wiring the Differential Input to Accept Single-ended LVPECL Levels

Figure 1B shows an example of the differential input that can be wired to accept single-ended LVPECL levels. The reference voltage level V_{BB} generated from the device is connected to the negative input. The C1 capacitor should be located as close as possible to the input pin.

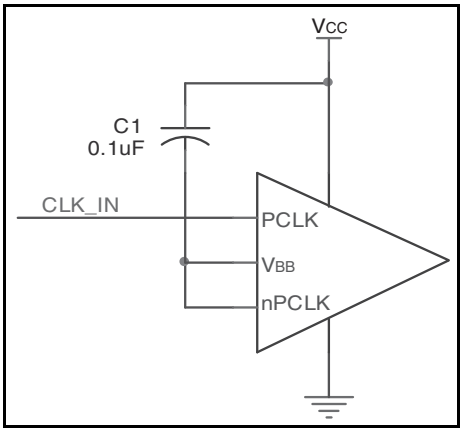


Figure 1B. Single-Ended LVPECL Signal Driving Differential Input

LVPECL Clock Input Interface (3.3V)

The PCLK/nPCLK accepts LVPECL, LVDS and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. *Figures 2A to 2C* show interface examples for the PCLK/nPCLK input driven by the most common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

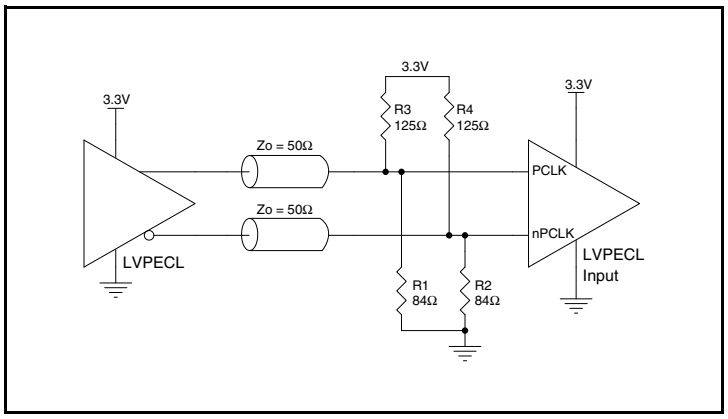


Figure 2A. PCLK/nPCLK Input Driven by a 3.3V LVPECL Driver

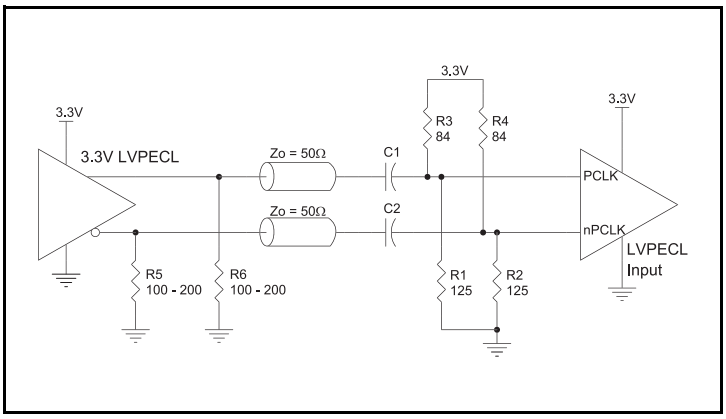


Figure 2B. PCLK/nPCLK Input Driven by a 3.3V LVPECL Driver with AC Couple

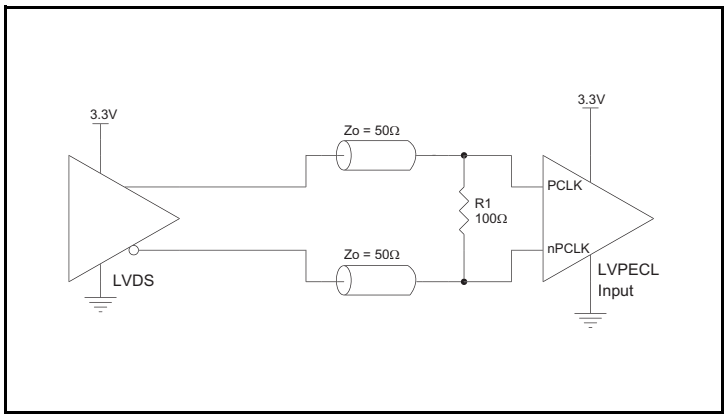


Figure 2C. PCLK/nPCLK Input Driven by a 3.3V LVDS Driver

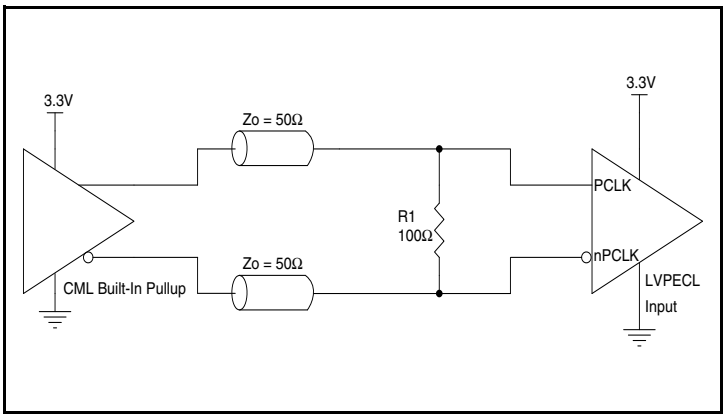


Figure 2D. PCLK/nPCLK Input Driven by a Built-In Pullup CML Driver

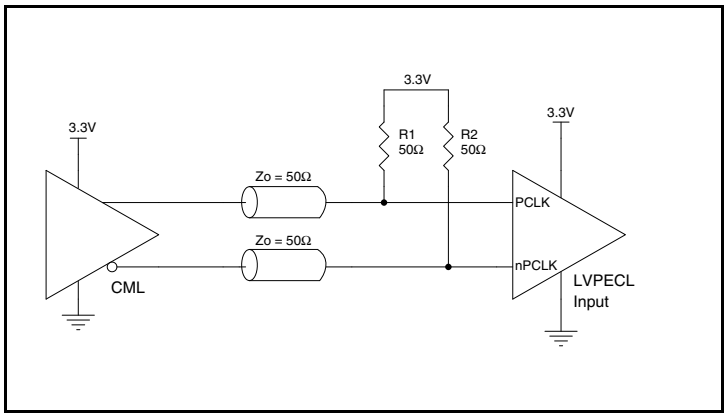


Figure 2E. PCLK/nPCLK Input Driven by a CML Driver

LVPECL Clock Input Interface (2.5V)

The PCLK /nPCLK accepts LVPECL, LVDS and other differential signals. The differential signal must meet the V_{PP} and V_{CMR} input requirements. *Figures 3A to 3C* show interface examples for the PCLK/nPCLK input driven by the most common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

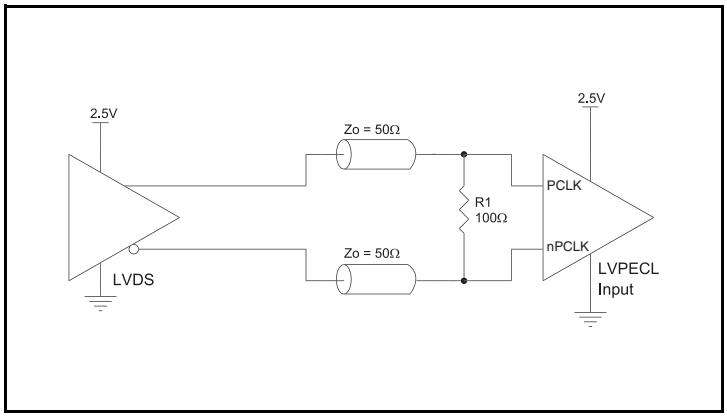


Figure 3A. PCLK/nPCLK Input Driven by a 2.5V LVDS Driver

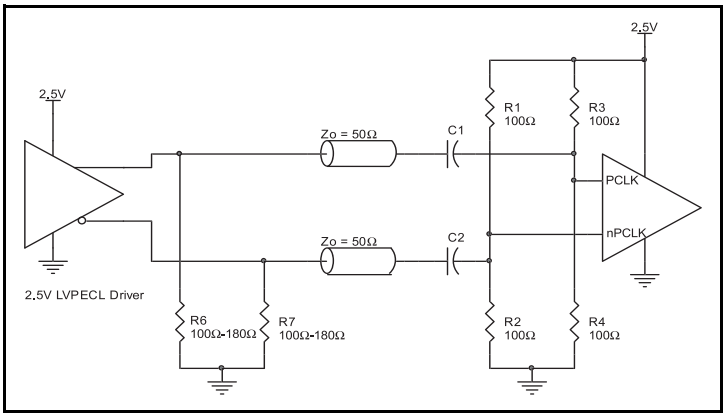


Figure 3B. PCLK/nPCLK Input Driven by a 3.3V LVPECL Driver with AC Couple

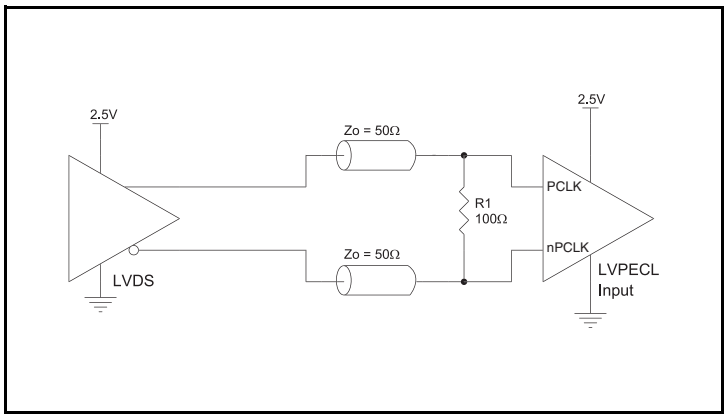


Figure 3C. PCLK/nPCLK Input Driven by a 2.5V LVPECL Driver

Recommendations for Unused Input Pins

Inputs:

PCLK/nPCLK Inputs

For applications not requiring the use of a differential input, both the PCLK and nPCLK pins can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from PCLK to ground. For applications

Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

The differential output pair is low impedance follower output that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 4A and 4B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

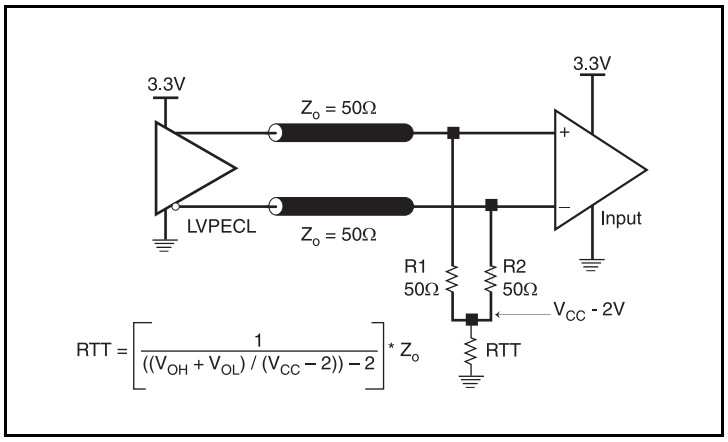


Figure 4A. 3.3V LVPECL Output Termination

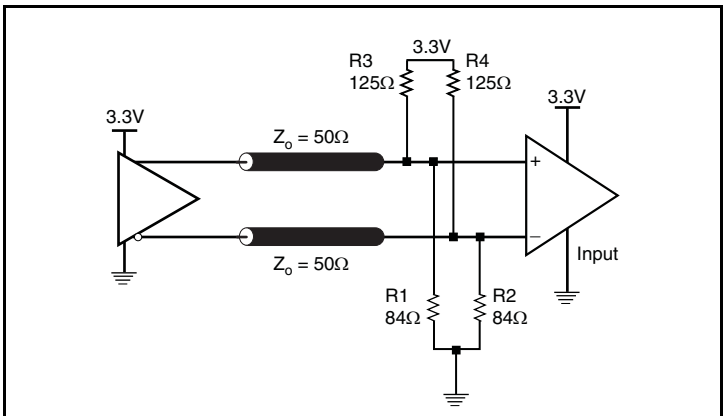


Figure 4B. 3.3V LVPECL Output Termination

Termination for 2.5V LVPECL Outputs

Figure 5A and *Figure 5B* show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to V_{CC} – 2V. For V_{CC} = 2.5V, the V_{CC} – 2V is very close to ground level. The R3 in Figure 5B can be eliminated and the termination is shown in *Figure 5C.*

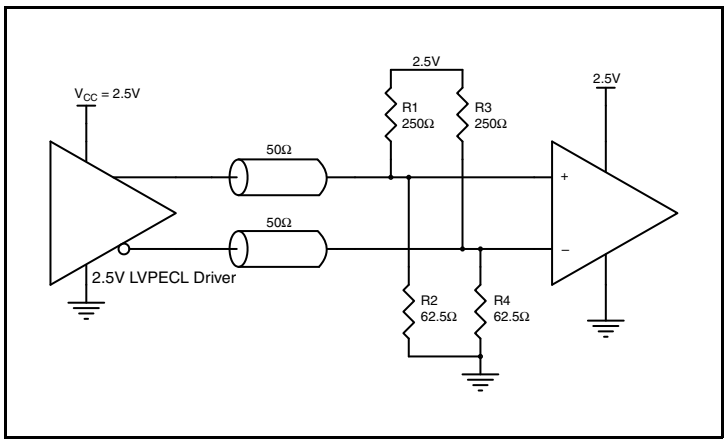


Figure 5A. 2.5V LVPECL Driver Termination Example

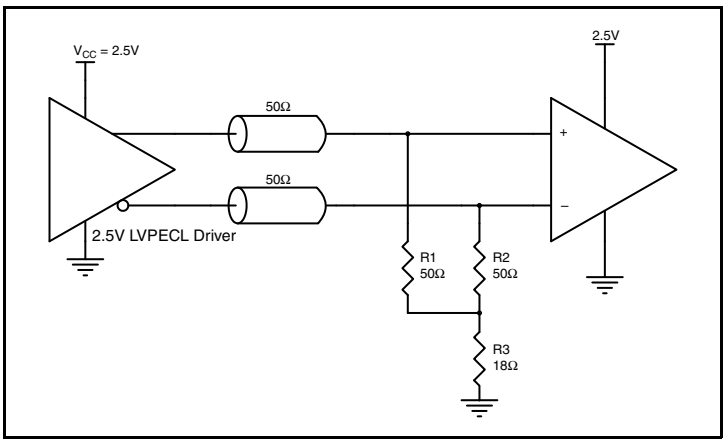


Figure 5B. 2.5V LVPECL Driver Termination Example

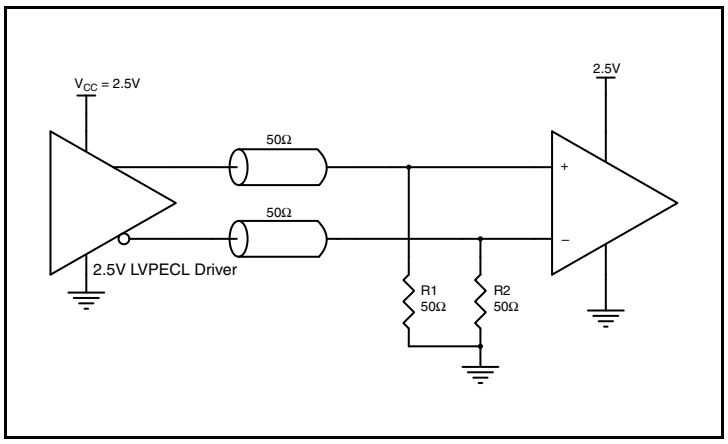


Figure 5C. 2.5V LVPECL Driver Termination Example

VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 6.* The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor’s Thermally/ Electrically Enhance Leadframe Base Package, Amkor Technology.

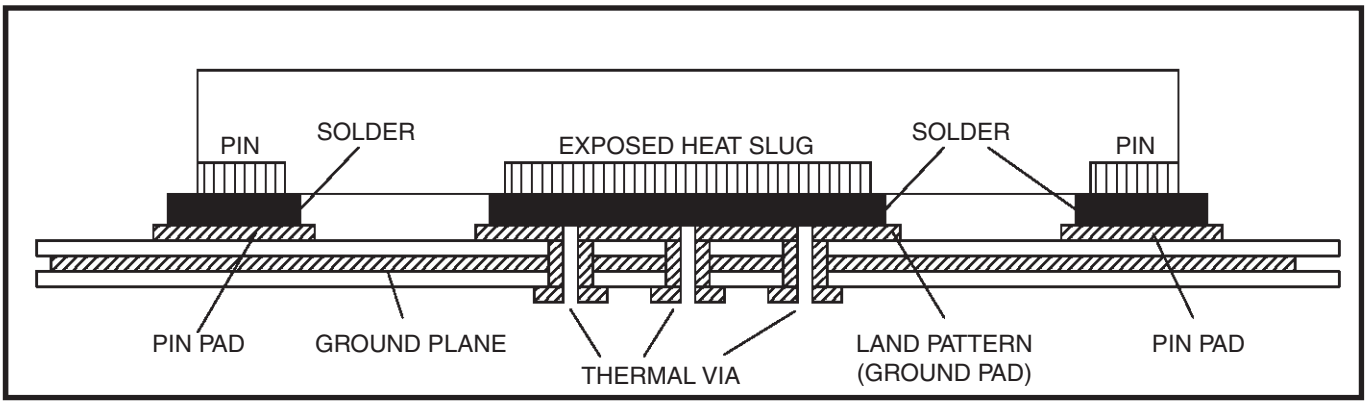


Figure 6. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (drawing not to scale)

Schematic Example

Figure 7 shows an example of 853S01 application schematic. This device can accept different types of input signal. In this example, the input is driven by a LVPECL driver. The decoupling capacitor should be located as close as possible to the power pin.

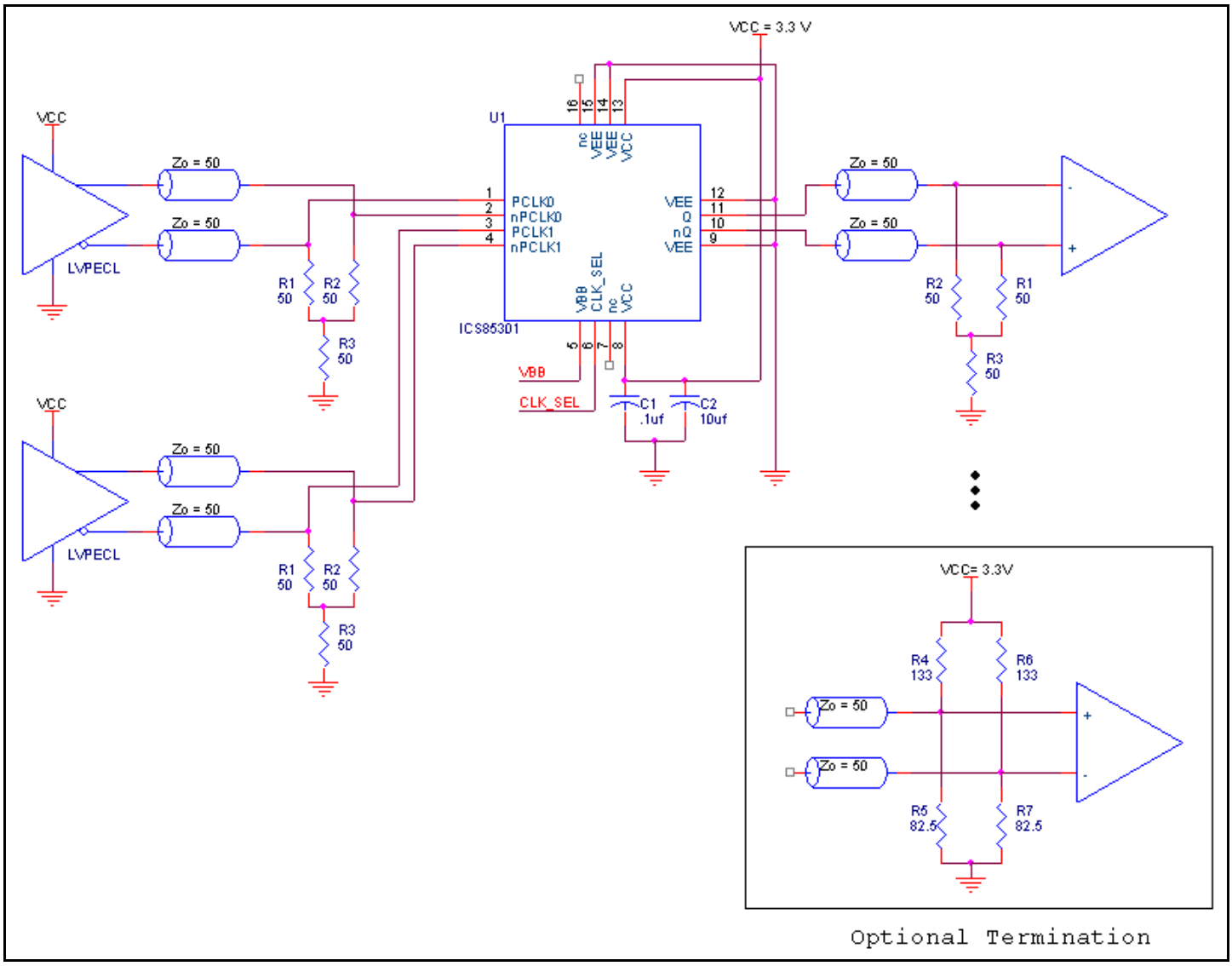


Figure 7. 853S01 Applications Schematic Example

Power Considerations

This section provides information on power dissipation and junction temperature for the 853S01.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the 853S01 is the sum of the core power plus the power dissipation in the load(s).
The following is the power dissipation for V_{CC} = 3.3V + 5% = 3.465V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipation in the load.

- Power $(core)_{MAX} = V_{CC_MAX} * I_{EE_MAX}$ = 3.465V * 26mA = **90.09mW**
- Power $(outputs)_{MAX}$ = **32mW/Loaded Output pair**

Total Power$_{_MAX}$ (3.3V, with all outputs switching) = 90.09mW + 32mW = **122.09mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 100°C/W per Table 6A below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.122W * 100°C/W = 97.2°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 6A. Thermal Resistance θ_{JA} for 16 Lead TSSOP, Forced Convection

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	100.0°C/W	94.2°C/W	90.2°C/W

Table 6B. Thermal Resistance θ_{JA} for 16 Lead VFQFN, Forced Convection

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	74.7°C/W	65.3°C/W	58.5°C/W

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3. Calculations and Equations.

The purpose of this section is to calculate the power dissipation for the LVPECL output pair.

The LVPECL output driver circuit and termination are shown in *Figure 8.*

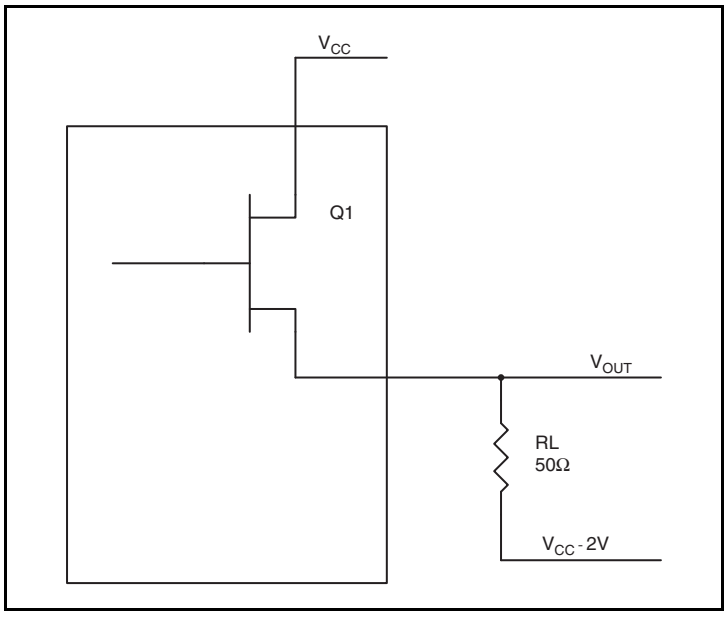


Figure 8. LVPECL Driver Circuit and Termination

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of V_{CC} – 2V.

- For logic high, $V_{OUT} = V_{OH_MAX} = \mathbf{V_{CC_MAX} – 0.875V}$
  $(V_{CC_MAX} – V_{OH_MAX}) = \mathbf{0.875V}$
- For logic low, $V_{OUT} = V_{OL_MAX} = \mathbf{V_{CC_MAX} – 1.62V}$
  $(V_{CC_MAX} – V_{OL_MAX}) = \mathbf{1.62V}$

Pd_H is power dissipation when the output drives high.

Pd_L is the power dissipation when the output drives low.

$Pd_H = [(V_{OH_MAX} – (V_{CC_MAX} – 2V))/R_L] * (V_{CC_MAX} – V_{OH_MAX}) = [(2V – (V_{CC_MAX} – V_{OH_MAX}))/R_L] * (V_{CC_MAX} – V_{OH_MAX}) =$
$[(2V – 0.875V)/50\Omega] * 0.875V =$ **19.691mW**

$Pd_L = [(V_{OL_MAX} – (V_{CC_MAX} – 2V))/R_L] * (V_{CC_MAX} – V_{OL_MAX}) = [(2V – (V_{CC_MAX} – V_{OL_MAX}))/R_L] * (V_{CC_MAX} – V_{OL_MAX}) =$
$[(2V – 1.62V)/50\Omega] * 1.62V =$ **12.31mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **32mW**

Reliability Information

Table 7A. θ_{JA} vs. Air Flow Table for a 16 Lead VFQFN

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	74.7°C/W	65.3°C/W	58.5°C/W

Table 7B. θ_{JA} vs. Air Flow Table for an 16 Lead TSSOP Forced Convection

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	100.0°C/W	94.2°C/W	90.2°C/W

Transistor Count

The transistor count for 853S01 is: 244

This device is pin and function compatible and a suggested replacement for ICS85301.

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Package Outline and Package Dimensions

Package Outline - G Suffix for 16 Lead TSSOP

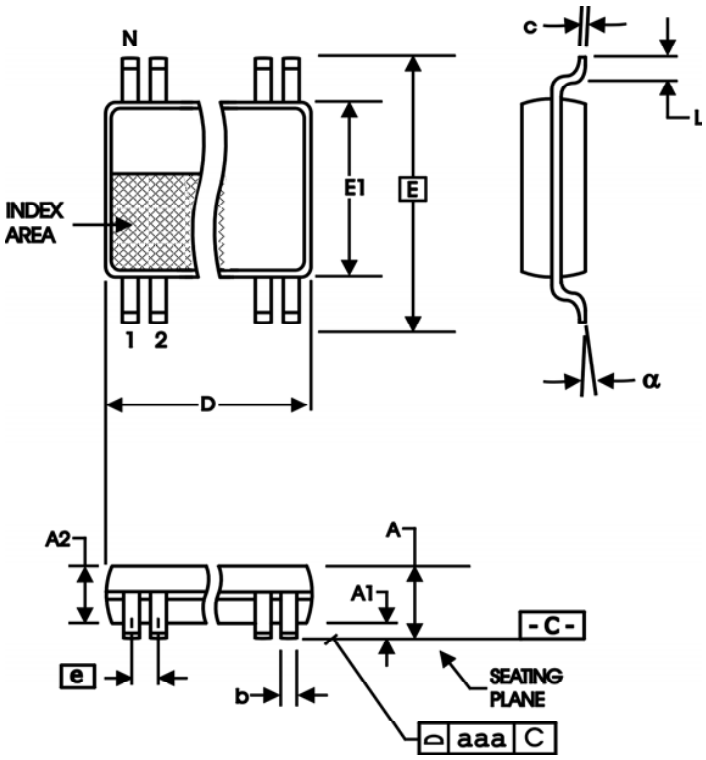


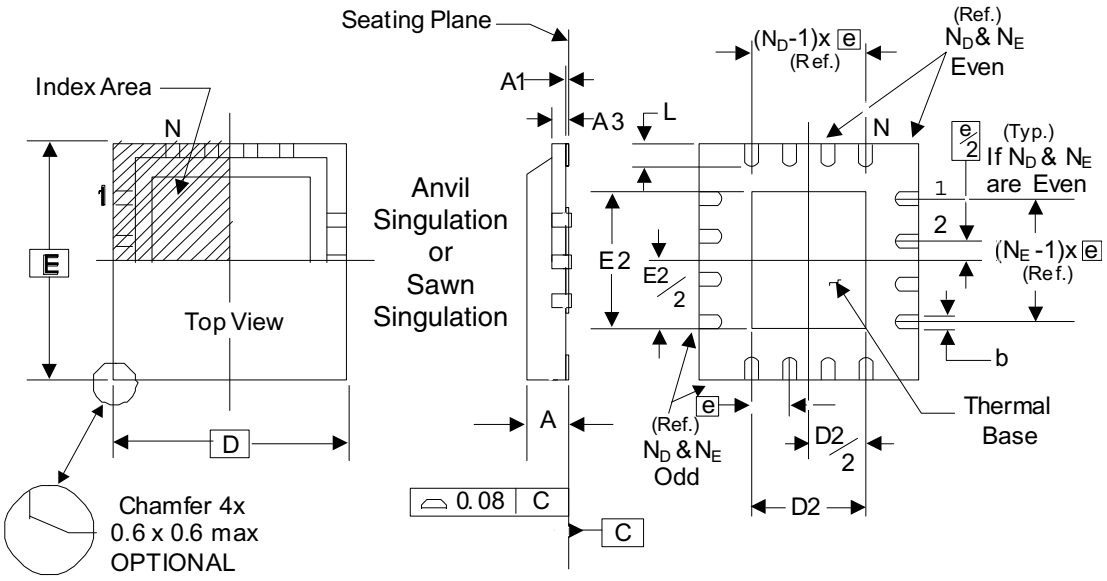
Table 8A. Package Dimensions

All Dimensions in Millimeters		
Symbol	**Minimum**	**Maximum**
N	16	
A		1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	4.90	5.10
E	6.40 Basic	
E1	4.30	4.50
e	0.65 Basic	
L	0.45	0.75
α	0°	8°
aaa		0.10

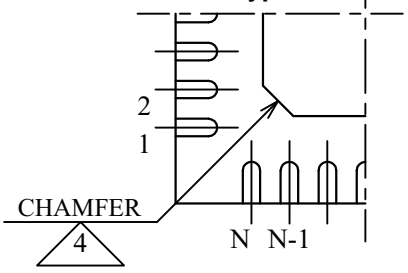
Reference Document: JEDEC Publication 95, MO-153

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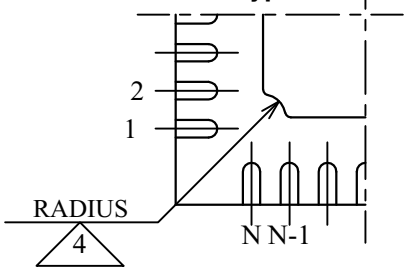
Package Outline - K Suffix for 16 Lead VFQFN



Bottom View w/Type A ID



Bottom View w/Type C ID



There are 2 methods of indicating pin 1 corner at the back of the VFQFN package:

1. Type A: Chamfer on the paddle (near pin 1)
2. Type C: Mouse bite on the paddle (near pin 1)

Table 8B. Package Dimensions

JEDEC Variation: VEED-2/-4 All Dimensions in Millimeters		
Symbol	**Minimum**	**Maximum**
N	16	
A	0.80	1.00
A1	0	0.05
A3	0.25 Ref.	
b	0.18	0.30
N_D & N_E	4	
D & E	3.00 Basic	
D2 & E2	1.00	1.80
e	0.50 Basic	
L	0.30	0.50

Reference Document: JEDEC Publication 95, MO-220

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Ordering Information

Table 9. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
853S01AGILF	53S01AIL	“Lead-Free” 16 Lead TSSOP	Tube	-40°C to 85°C
853S01AGILFT	53S01AIL	“Lead-Free” 16 Lead TSSOP	Tape & Reel	-40°C to 85°C
853S01AKILF	3S1A	“Lead-Free” 16 Lead VFQFN	Tube	-40°C to 85°C
853S01AKILFT	3S1A	“Lead-Free” 16 Lead VFQFN	Tape & Reel	-40°C to 85°C

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Revision History Sheet

Rev	Table	Page	Description of Change	Date
A		9 20	Updated *Wiring the Differential Inputs to Accept Single-ended Levels* section. Updated the 32 VFQFN Bottom View Package Drawing.	11/23/10
A		1 10 T9 21	Deleted HiperClockS Logo. Updated GD paragraph to include CML. Added CML to 3rd bullet. Added figures 2D and 2E. Deleted quantity from tape and reel.	10/29/12
B			Deleted part number's "I" prefix throughout the datasheet. Updated datasheet header/footer.	2/9/16
B	T9	21	Ordering Information- Deleted LF note below table. Corrected Data Sheet header from 12:1 to 2:1.	3/4/16

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