Low Skew, 1-to-9, Differential-to-3.3V, 2.5V LVPECL/ECL Fanout Buffer

ICS853S031I

DATA SHEET

General Description

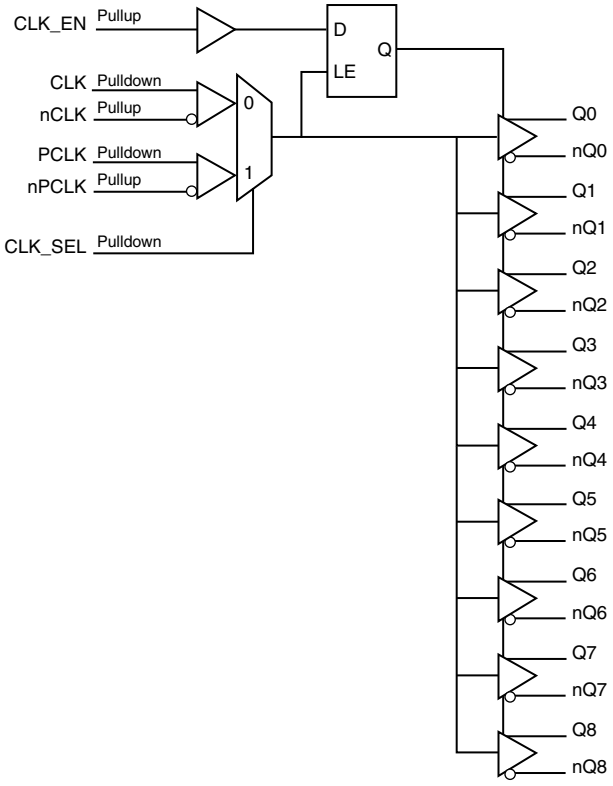
The ICS853S031I is a low skew, high performance 1-to-9 Differential-to-2.5V/3.3V LVPECL/ECL Fanout Buffer. The ICS853S031I has two selectable clock inputs. The CLK, nCLK pair can accept most standard differential input levels. The PCLK, nPCLK pair can accept LVPECL, LVDS, CML or SSTL input levels. The clock enable is internally synchronized to eliminate runt pulses on the outputs during asynchronous assertion/deassertion of the clock enable pin.

Guaranteed output and part-to-part skew characteristics make the ICS853S031I ideal for high performance workstation and server applications.

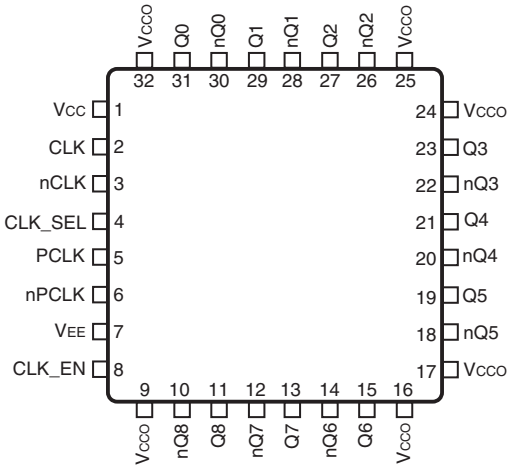
Features

- Nine differential 2.5V, 3.3V LVPECL/ECL outputs
- Selectable differential CLK, nCLK or LVPECL clock inputs
- CLK, nCLK pair can accept the following differential input levels: LVPECL, LVDS, LVHSTL, HCSL, SSTL
- PCLK, nPCLK supports the following input types: LVPECL, LVDS, CML, SSTL
- Output frequency: 1.6GHz (maximum)
- Translates any single-ended input signal (LVCMOS, LVTTL, GTL) to 3.3V LVPECL levels with resistor bias on nCLK or nPCLK inputs
- Output skew: 20ps (typical)
- Part-to-part skew: 90ps (typical)
- Propagation delay: 885ps (typical), PCLK
- LVPECL mode operating voltage supply range: V_{CC} = 2.375V to 3.465V, V_{EE} = 0V
- ECL mode operating voltage supply range: V_{CC} = 0V, V_{EE} = -3.465V to -2.375V
- -40°C to 85°C ambient operating temperature
- Available lead-free (RoHS 6) package

Block Diagram



Pin Assignment



ICS853S031I

32-Lead LQFP
7mm x 7mm x 1.4mm package body
Y Package
Top View

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Table 1. Pin Descriptions

Number	Name	Type		Description
1	V_{CC}	Power		Positive supply pin.
2	CLK	Input	Pulldown	Non-inverting differential clock input.
3	nCLK	Input	Pullup	Inverting differential clock input.
4	CLK_SEL	Input	Pulldown	Clock select input. When HIGH, selects PCLK/nPCLK inputs. When LOW, selects CLK/nCLK inputs. LVTTL / LVCMOS interface levels.
5	PCLK	Input	Pulldown	Non-inverting differential LVPECL clock input.
6	nPCLK	Input	Pullup	Inverting differential LVPECL clock input.
7	V_{EE}	Power		Negative supply pin.
8	CLK_EN	Input	Pullup	Synchronizing clock enable. When HIGH, clock outputs follow clock input. When LOW, Qx outputs are forced low, nQx outputs are forced high. LVTTL/LVCMOS interface levels.
9, 16, 17, 24, 25, 32	V_{CCO}	Power		Output supply pins.
10, 11	nQ8, Q8	Output		Differential output pair. LVPECL/ECL interface levels.
12, 13	nQ7, Q7	Output		Differential output pair. LVPECL/ECL interface levels.
14, 15	nQ6, Q6	Output		Differential output pair. LVPECL/ECL interface levels.
18, 19	nQ5, Q5	Output		Differential output pair. LVPECL/ECL interface levels.
20, 21	nQ4, Q4	Output		Differential output pair. LVPECL/ECL interface levels.
22, 23	nQ3, Q3	Output		Differential output pair. LVPECL/ECL interface levels.
26, 27	nQ2, Q2	Output		Differential output pair. LVPECL/ECL interface levels.
28, 29	nQ1, Q1	Output		Differential output pair. LVPECL/ECL interface levels.
30, 31	nQ0, Q0	Output		Differential output pair. LVPECL/ECL interface levels.

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$R_{PULLDOWN}$	Input Pulldown Resistor			50		kΩ
R_{PULLUP}	Input Pullup Resistor			50		kΩ

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Function Tables

Table 3A. Control Input Function Table

Inputs			Outputs	
CLK_EN	CLK_SEL	Selected Sources	Q0:Q8	nQ0:nQ8
0	0	CLK, nCLK	Disabled:LOW	Disabled: HIGH
0	1	PCLK, nPCLK	Disabled:LOW	Disabled: HIGH
1	0	CLK, nCLK	Enabled	Enabled
1	1	PCLK, nPCLK	Enabled	Enabled

After CLK_EN switches, the clock outputs are disabled or enabled following a rising and falling input clock edge as shown in Figure 1.
In the active mode, the state of the outputs are a function of the CLK, nCLK and PCLK, nPCLK inputs as described in Table 3B.

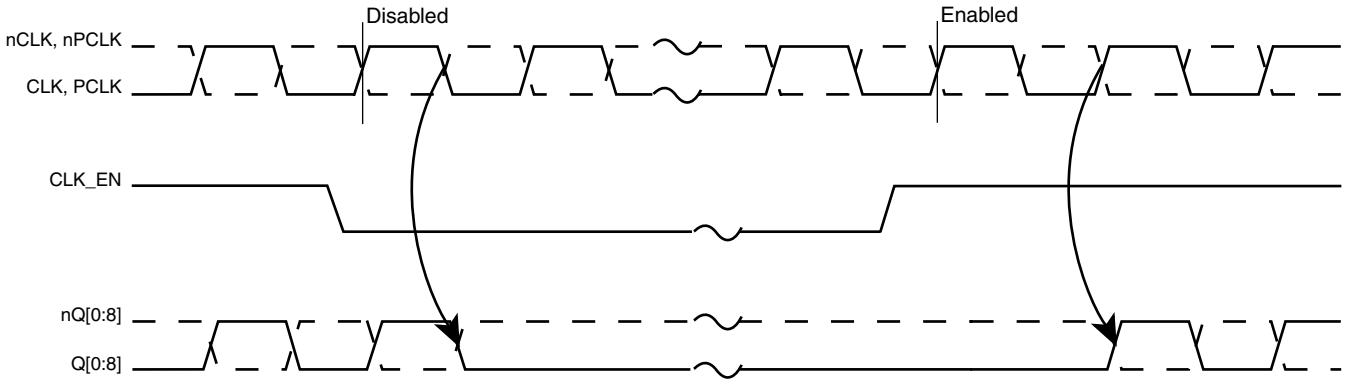


Figure 1. CLK_EN Timing Diagram

Table 3B. Clock Input Function Table

Inputs		Outputs			
CLK or PCLK	nCLK or nPCLK	Q0:Q8	nQ0:nQ8	Input to Output Mode	Polarity
0	1	LOW	HIGH	Differential to Differential	Non-Inverting
1	0	HIGH	LOW	Differential to Differential	Non-Inverting
0	Biased; NOTE 1	LOW	HIGH	Single-Ended to Differential	Non-Inverting
1	Biased; NOTE 1	HIGH	LOW	Single-Ended to Differential	Non-Inverting
Biased; NOTE 1	0	HIGH	LOW	Single-Ended to Differential	Inverting
Biased; NOTE 1	1	LOW	HIGH	Single-Ended to Differential	Inverting

Note 1: Please refer to the Applications Information, “Wiring the Differential Input to Accept Single Ended Levels”.

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Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{CC}	4.6V (LVPECL mode, V_{EE} = 0V)
Negative Supply Voltage, V_{EE}	-4.6V (ECL mode, V_{CC} = 0V)
Inputs, V_I (LVPECL mode)	-0.5V to V_{CC} + 0.5V
Inputs, V_I (ECL mode)	0.5V to V_{EE} – 0.5V
Outputs, I_O Continuous Current Surge Current	 50mA 100mA
Operating Temperature Range, T_A	-40°C to +85°C
Package Thermal Impedance, θ_{JA}	71.4°C/W (1 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, V_{CC} = V_{CCO} = 2.375V to 3.465V; V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Positive Supply Voltage		2.375	3.3	3.465	V
V_{CCO}	Output Supply Voltage		2.375	3.3	3.465	V
I_{EE}	Power Supply Current				70	mA

Table 4B. LVCMOS/LVTTL DC Characteristics, V_{CC} = V_{CCO} = 2.375V to 3.465V; V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		V_{CC} = 3.3V	2.2		3.465	V
			V_{CC} = 2.5V	1.7		3.465	V
V_{IL}	Input Low Voltage		V_{CC} = 3.3V	-0.3		0.8	V
			V_{CC} = 2.5V	-0.3		0.7	V
I_{IH}	Input High Current	CLK_EN	V_{CC} = V_{IN} = 3.465V or 2.625V			10	µA
		CLK_SEL	V_{CC} = V_{IN} = 3.465V or 2.625V			150	µA
I_{IL}	Input Low Current	CLK_EN	V_{CC} = 3.465V or 2.625V, V_{IN} = 0V	-150			µA
		CLK_SEL	V_{CC} = 3.465V or 2.625V, V_{IN} = 0V	-10			µA

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Table 4C. Differential DC Characteristics, $V_{CC} = V_{CCO} = 2.375V$ to $3.465V$; $V_{EE} = 0V$, $T_A = -40°C$ to $85°C$

Symbol	Parameter		-40°C			25°C			85°C			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{IH}	Input High Current	CLK			150			150			150	µA
		nCLK			10			10			10	µA
I_{IL}	Input Low Current	CLK	-10			-10			-10			µA
		nCLK	-150			-150			-150			µA
V_{PP}	Peak-to-Peak Voltage; NOTE 1		0.15		1.3	0.15		1.3	0.15		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2		V_{EE} + 0.7		V_{CC} – 0.85	V_{EE} + 0.7		V_{CC} – 0.85	V_{EE} + 0.7		V_{CC} – 0.85	V

NOTE 1: V_{IL} should not be less than -0.3V.
NOTE 2: Common mode input voltage is defined as V_{IH}.

Table 4D. LVPECL DC Characteristics, $V_{CC} = V_{CCO} = 3.3V±5\%$; $V_{EE} = 0V$, $T_A = -40°C$ to $85°C$

Symbol	Parameter		-40°C			25°C			85°C			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output High Voltage; NOTE 1		2.14	2.38	2.56	2.14	2.38	2.57	2.14	2.36	2.59	V
V_{OL}	Output Low Voltage; NOTE 1		1.45	1.61	1.79	1.45	1.58	1.80	1.45	1.57	1.82	V
V_{PP}	Peak-to-Peak Input Voltage		0.15	0.8	1.3	0.15	0.8	1.3	0.15	0.8	1.3	V
V_{CMR}	Input High Voltage Common Mode Range; NOTE 2		1.2		V_{CC}	1.2		V_{CC}	1.2		V_{CC}	V
V_{SWING}	Output Voltage Swing		0.6		1.0	0.6		1.0	0.6		1.0	V
I_{IH}	Input High Current	PCLK			150			150			150	µA
		nPCLK			10			10			10	µA
I_{IL}	Input Low Current	PCLK	-10			-10			-10			µA
		nPCLK	-150			-150			-150			µA

NOTE: Input and output parameters vary 1:1 with V_{CC}. This variation has been taken into account in the table above.
NOTE 1: Outputs terminated with 50Ω to V_{CCO} – 2V.
NOTE 2: Common mode voltage is defined as V_{IH}.

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Table 4E. LVPECL DC Characteristics, $V_{CC} = V_{CCO} = 2.5V±5\%$; $V_{EE} = 0V$, $T_A = -40°C$ to $85°C$

Symbol	Parameter		-40°C			25°C			85°C			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output High Voltage; NOTE 1		1.34	1.58	1.76	1.34	1.58	1.77	1.34	1.56	1.79	V
V_{OL}	Output Low Voltage; NOTE 1		0.65	0.81	0.99	0.65	0.78	1.00	0.65	0.77	1.02	V
V_{PP}	Peak-to-Peak Input Voltage		0.15	0.8	1.3	0.15	0.8	1.3	0.15	0.8	1.3	V
V_{CMR}	Input High Voltage Common Mode Range; NOTE 2		1.2		V_{CC}	1.2		V_{CC}	1.2		V_{CC}	V
V_{SWING}	Output Voltage Swing		0.6		1.0	0.6		1.0	0.6		1.0	V
I_{IH}	Input High Current	PCLK			150			150			150	µA
		nPCLK			10			10			10	µA
I_{IL}	Input Low Current	PCLK	-10			-10			-10			µA
		nPCLK	-150			-150			-150			µA

NOTE: Input and output parameters vary 1:1 with V_{CC}. This variation has been taken into account in the table above.
NOTE 1: Outputs terminated with 50Ω to $V_{CCO} – 2V$.
NOTE 2: Common mode voltage is defined as V_{IH}.

Table 4F. ECL DC Characteristics, $V_{CC} = 0V$; $V_{EE} = -3.465V$ to $-2.375V$, $T_A = -40°C$ to $85°C$

Symbol	Parameter		-40°C			25°C			85°C			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output High Voltage; NOTE 1		-1.16	-0.92	-0.74	-1.16	-0.92	-0.73	-1.16	-0.94	-0.71	V
V_{OL}	Output Low Voltage; NOTE 1		-1.85	-1.69	-1.51	-1.85	-1.72	-1.5	-1.85	-1.73	-1.48	V
V_{PP}	Peak-to-Peak Input Voltage		0.15	0.8	1.3	0.15	0.8	1.3	0.15	0.8	1.3	V
V_{CMR}	Input High Voltage Common Mode Range; NOTE 2		$V_{EE}+1.2$		0	$V_{EE}+1.2$		0	$V_{EE}+1.2$		0	V
V_{SWING}	Output Voltage Swing		0.6		1.0	0.6		1.0	0.6		1.0	V
I_{IH}	Input High Current	PCLK			150			150			150	µA
		nPCLK			10			10			10	µA
I_{IL}	Input Low Current	PCLK	-10			-10			-10			µA
		nPCLK	-150			-150			-150			µA

NOTE 1: Outputs terminated with 50Ω to $V_{CCO} – 2V$.
NOTE 2: Common mode voltage is defined as V_{IH}.

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AC Electrical Characteristics

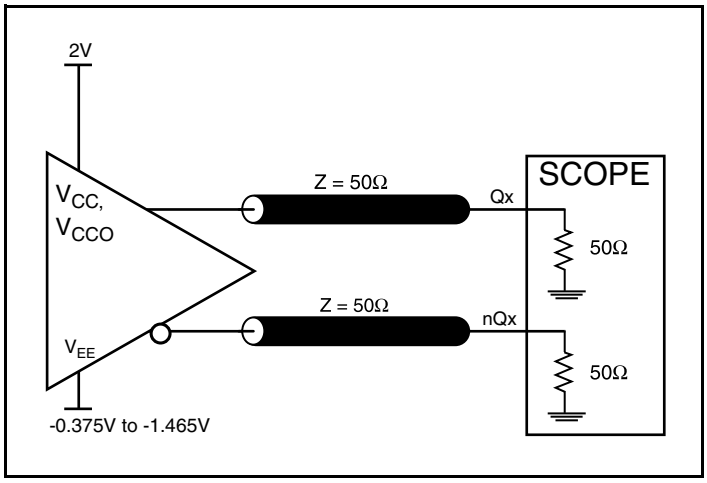
Table 5. AC Characteristics, $V_{CC} = V_{CCO}$ = -3.465V to -2.375V or , $V_{CC} = V_{CCO}$ = 2.375V to 3.465V; V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter		-40°C			25°C			85°C			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{OUT}	Output Frequency				1.6			1.6			1.6	GHz
t_{PD}	Propagation Delay; NOTE 1	PCLK, nPCLK	705	825	945	760	885	1005	835	960	1085	ps
		CLK, nCLK	770	885	995	825	945	1070	895	1025	1150	ps
*t*sk(o)	Output Skew; NOTE 2, 4			20	55		20	55		20	55	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 3, 4			85	225		90	245		95	250	ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	100	215	400	100	225	400	100	215	350	ps
odc	Output Duty Cycle	f ≤ 266MHz	48		52	48		52	48		52	%
		266MHz < f ≤ 500MHz	46		54	46		54	46		54	%

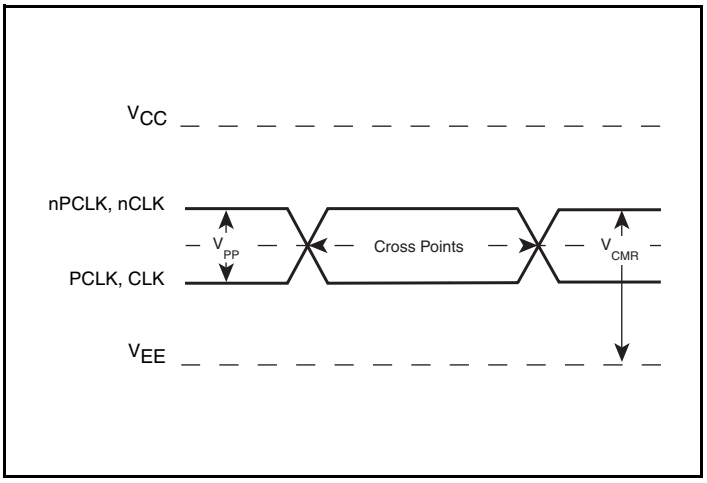
NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE: All parameters are measured at $f_{OUT} \leq$ 500 MHz, unless otherwise noted.
NOTE 1: Measured from the differential input crossing point to the differential output crossing point.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential cross points.
NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltage, same temperature and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

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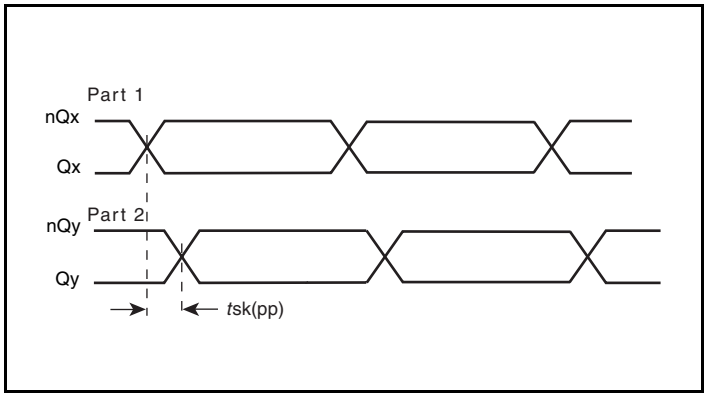
Parameter Measurement Information



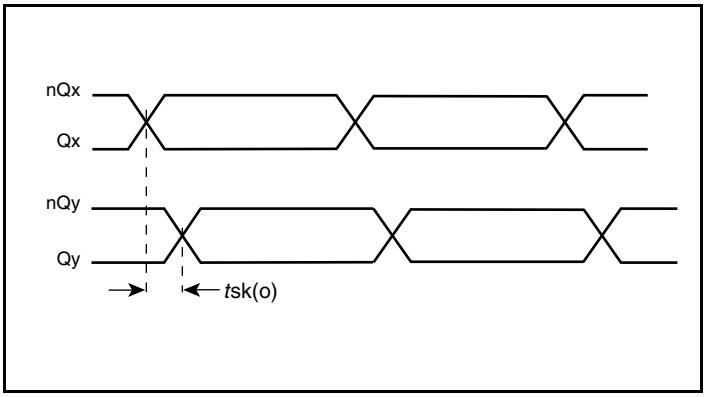
LVPECL Output Load AC Test Circuit



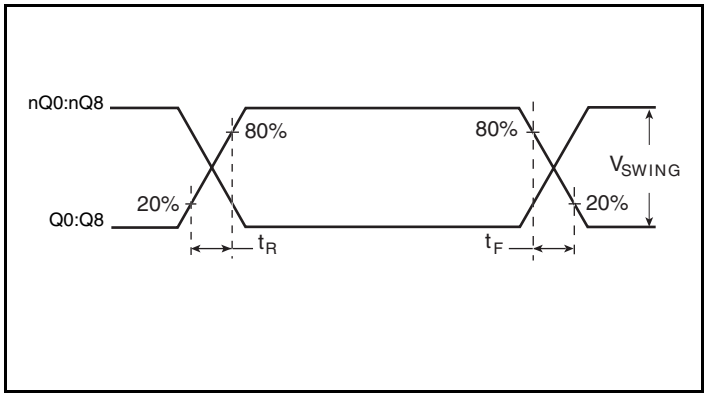
Differential Input Level



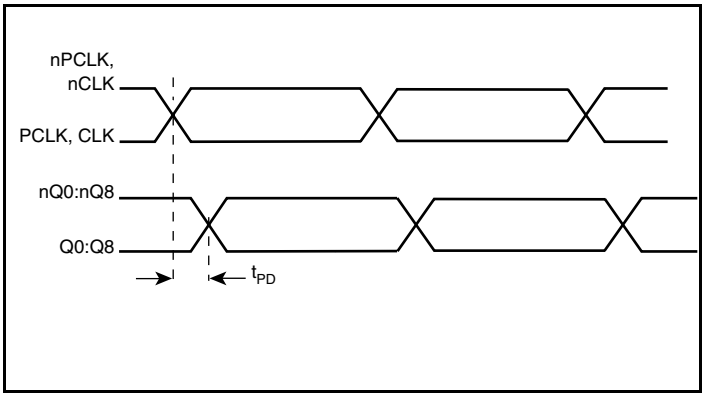
Part-to-Part Skew



Output Skew



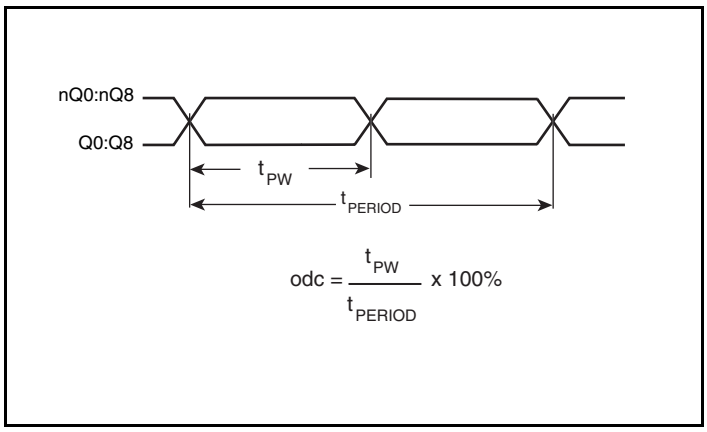
Output Rise/Fall Time



Propagation Delay

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Parameter Measurement Information, continued



Output Duty Cycle/Pulse Width/Period

Applications Information

Wiring the Differential Input to Accept Single-Ended Levels

Figure 2 shows how a differential input can be wired to accept single ended levels. The reference voltage $V_{REF} = V_{DD}/2$ is generated by the bias resistors R1 and R2. The bypass capacitor (C1) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of R1 and R2 might need to be adjusted to position the V_{REF} in the center of the input voltage swing. For example, if the input clock swing is 2.5V and V_{DD} = 3.3V, R1 and R2 value should be adjusted to set V_{REF} at 1.25V. The values below are for when both the single ended swing and V_{DD} are at the same voltage. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways. First, R3 and R4 in parallel should equal the transmission line impedance. For most 50Ω applications, R3 and R4 can be 100Ω. The values of the resistors can be increased to reduce the loading for slower and weaker LVCMOS driver. When using single-ended signaling, the noise rejection benefits of differential signaling are reduced. Even though the differential input can handle full rail LVCMOS signaling, it is recommended that the amplitude be reduced. The datasheet specifies a lower differential amplitude, however this only applies to differential signals. For single-ended applications, the swing can be larger, however V_{IL} cannot be less than -0.3V and V_{IH} cannot be more than V_{DD} + 0.3V. Though some of the recommended components might not be used, the pads should be placed in the layout. They can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a differential signal.

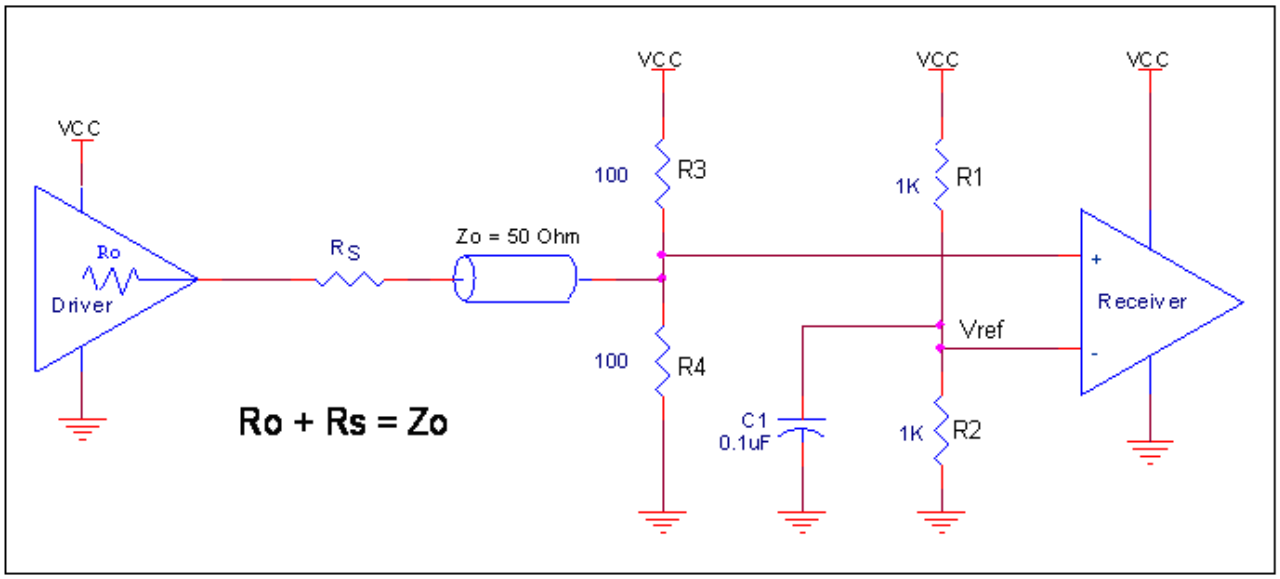


Figure 2. Recommended Schematic for Wiring a Differential Input to Accept Single-ended Levels

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LVPECL Clock Input Interface

The PCLK /nPCLK accepts LVPECL, LVDS, CML, SSTL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. *Figures 3A to 3F* show interface examples for the PCLK/nPCLK input driven by the most common driver types.

The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

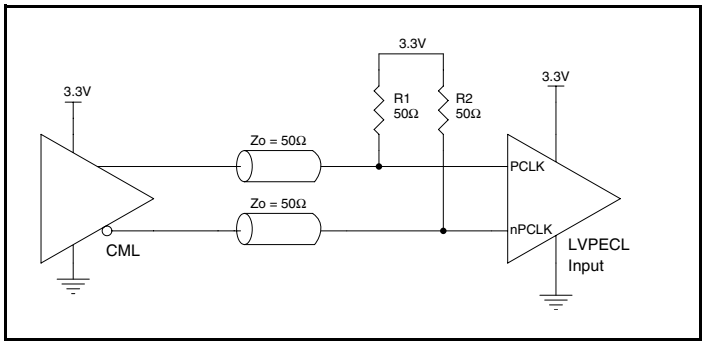


Figure 3A. PCLK/nPCLK Input Driven by a CML Driver

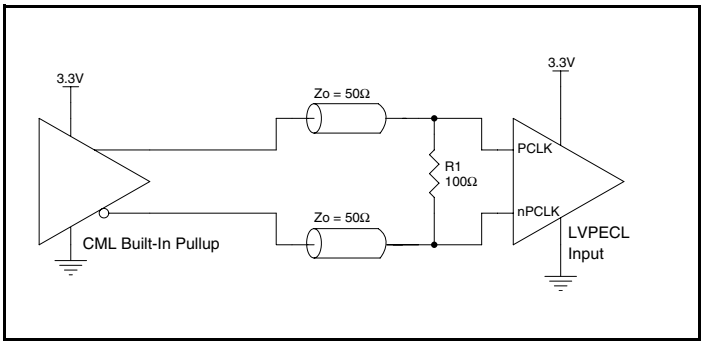


Figure 3B. PCLK/nPCLK Input Driven by a Built-In Pullup CML Driver

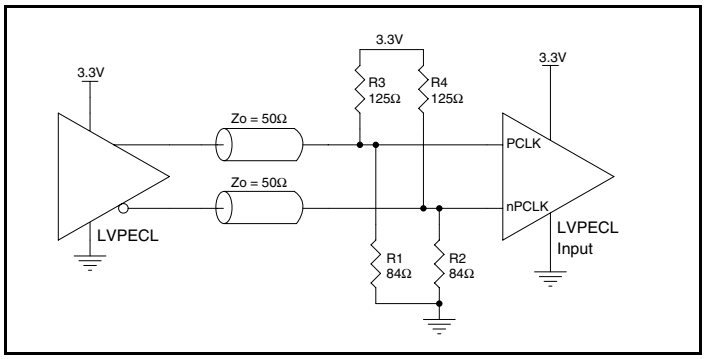


Figure 3C. PCLK/nPCLK Input Driven by a 3.3V LVPECL Driver

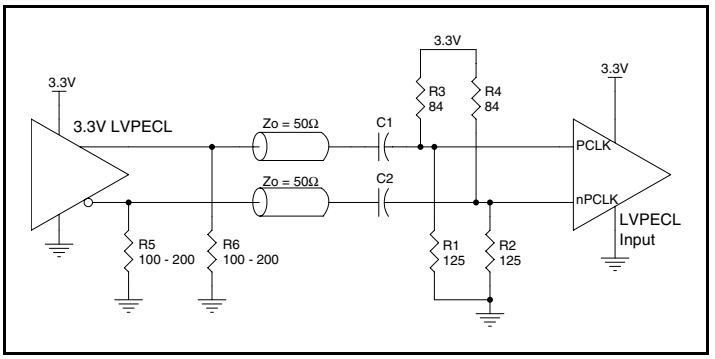


Figure 3D. PCLK/nPCLK Input Driven by a 3.3V LVPECL Driver with AC Couple

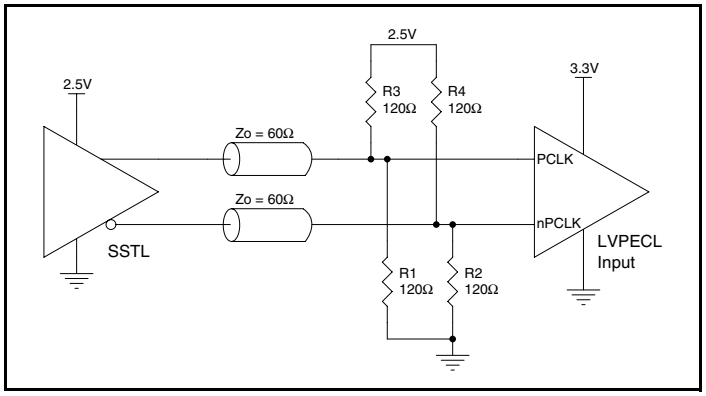


Figure 3E. PCLK/nPCLK Input Driven by an SSTL Driver

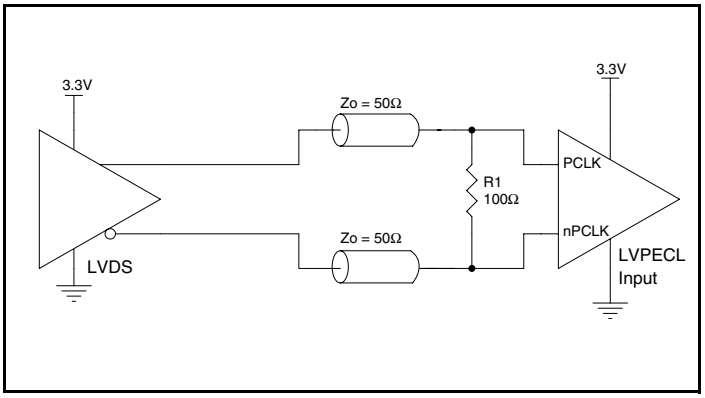


Figure 3F. PCLK/nPCLK Input Driven by a 3.3V LVDS Driver

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Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, SSTL, HCSL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. *Figures 4A to 4F* show interface examples for the CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only.

Please consult with the vendor of the driver component to confirm the driver termination requirements. For example, in Figure 4A, the input termination applies for IDT open emitter LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

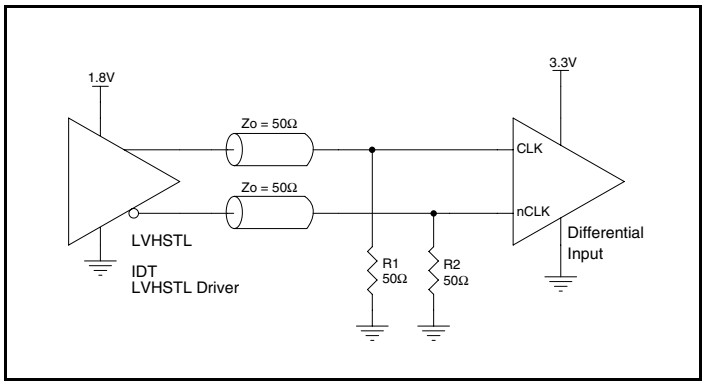


Figure 4A. CLK/nCLK Input Driven by an IDT Open Emitter LVHSTL Driver

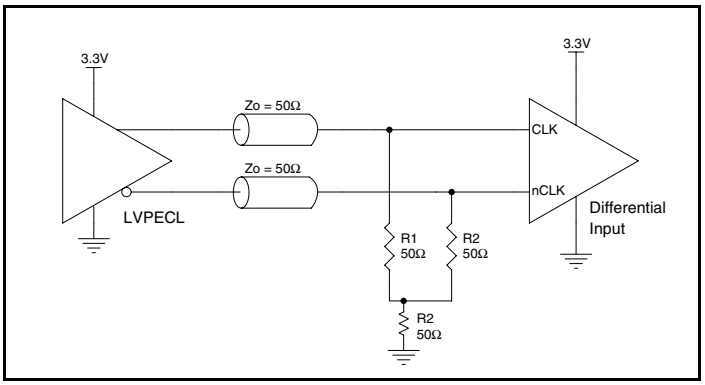


Figure 4B. CLK/nCLK Input Driven by a 3.3V LVPECL Driver

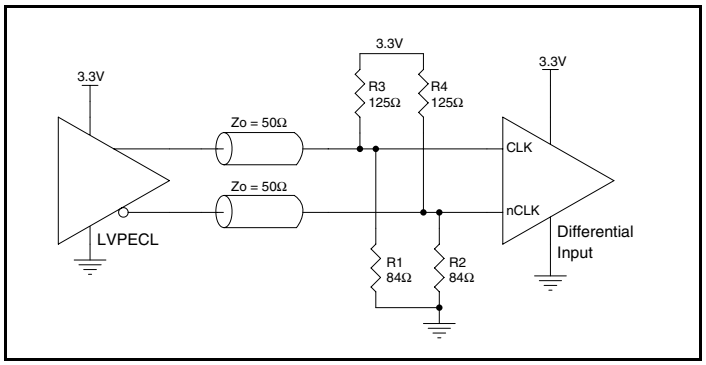


Figure 4C. CLK/nCLK Input Driven by a 3.3V LVPECL Driver

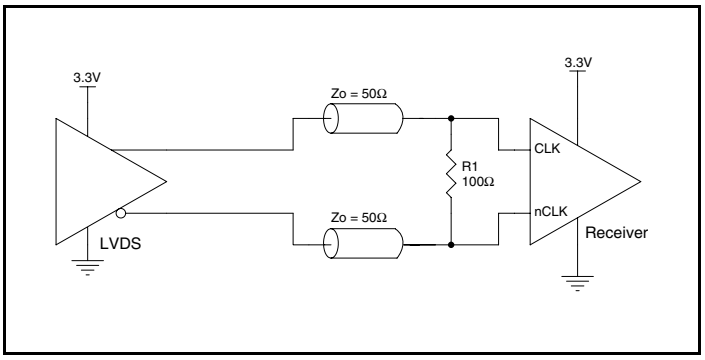


Figure 4D. CLK/nCLK Input Driven by a 3.3V LVDS Driver

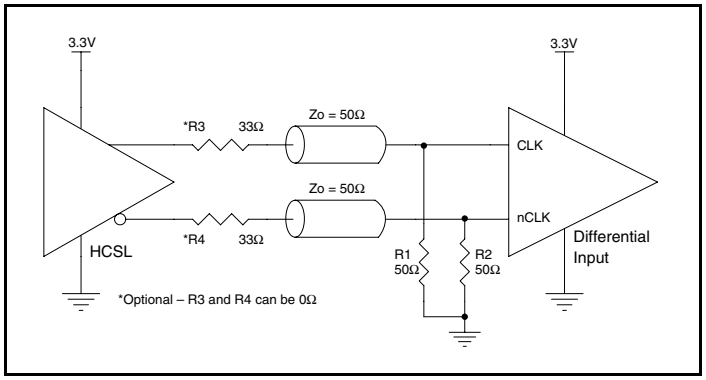


Figure 4E. CLK/nCLK Input Driven by a 3.3V HCSL Driver

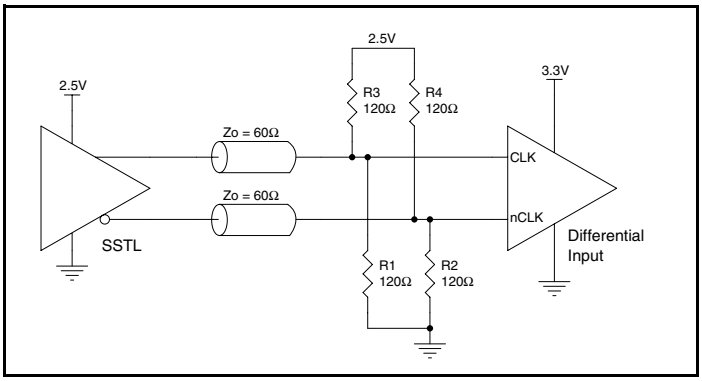


Figure 4F. CLK/nCLK Input Driven by a 2.5V SSTL Driver

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Recommendations for Unused Output Pins

Inputs:

PCLK/nPCLK Inputs

For applications not requiring the use of a differential input, both the PCLK and nPCLK pins can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from PCLK to ground. For applications

CLK/nCLK Inputs

For applications not requiring the use of the differential input, both CLK and nCLK can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from CLK to ground.

LVCMOS Control Pins

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs:

LVPECL Outputs

All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

The differential outputs are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 5A and 5B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

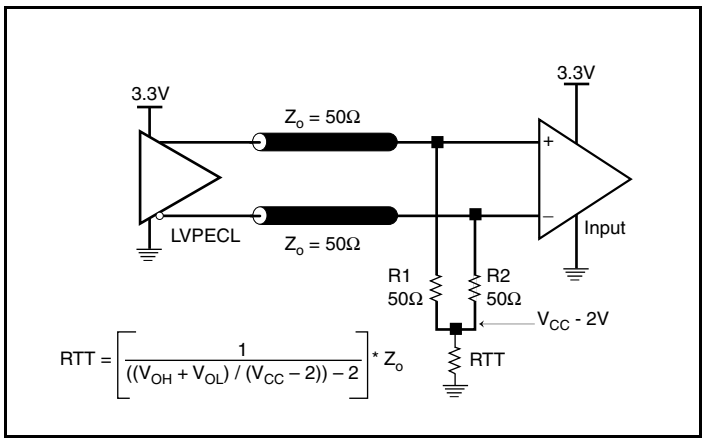


Figure 5A. 3.3V LVPECL Output Termination

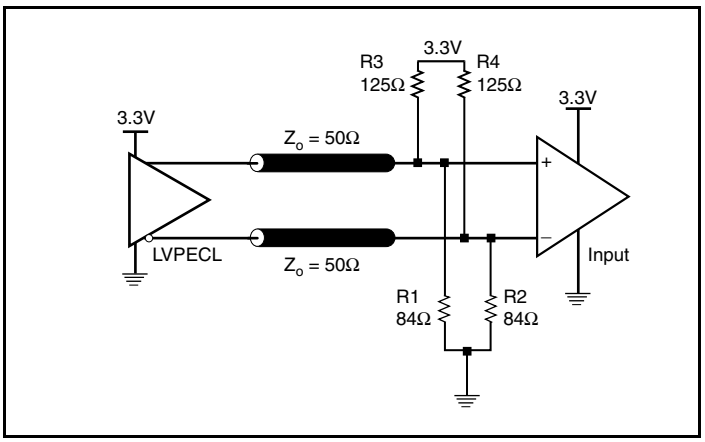


Figure 5B. 3.3V LVPECL Output Termination

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Termination for 2.5V LVPECL Outputs

Figure 6A and *Figure 6B* show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to V_{CCO} – 2V. For V_{CCO} = 2.5V, the V_{CCO} – 2V is very close to ground level. The R3 in Figure 6B can be eliminated and the termination is shown in *Figure 6C.*

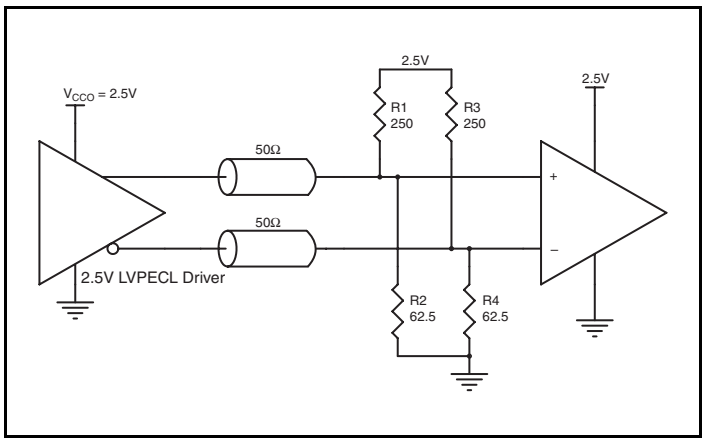


Figure 6A. 2.5V LVPECL Driver Termination Example

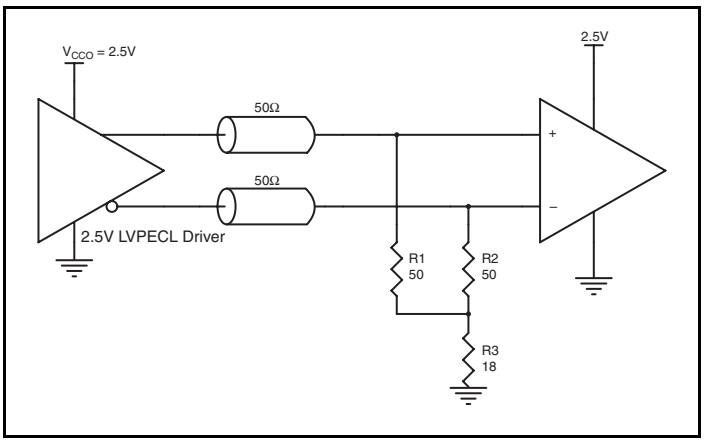


Figure 6B. 2.5V LVPECL Driver Termination Example

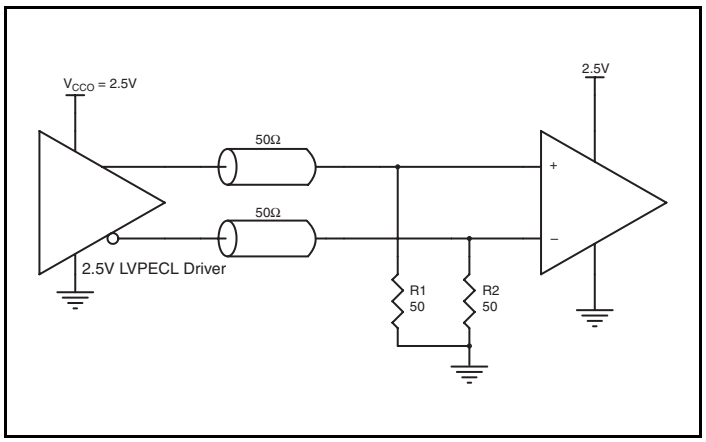


Figure 6C. 2.5V LVPECL Driver Termination Example

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Schematic Example

Figure 7 shows an example of ICS853S031I application schematic. In this example, the device is operated at V_{CC} = 3.3V. The decoupling capacitor should be located as close as possible to the power pin. The input is driven by a 3.3V LVPECL driver. Only two terminations examples are shown in this schematic. For more termination approaches, please refer to the LVPECL Termination Application Note.

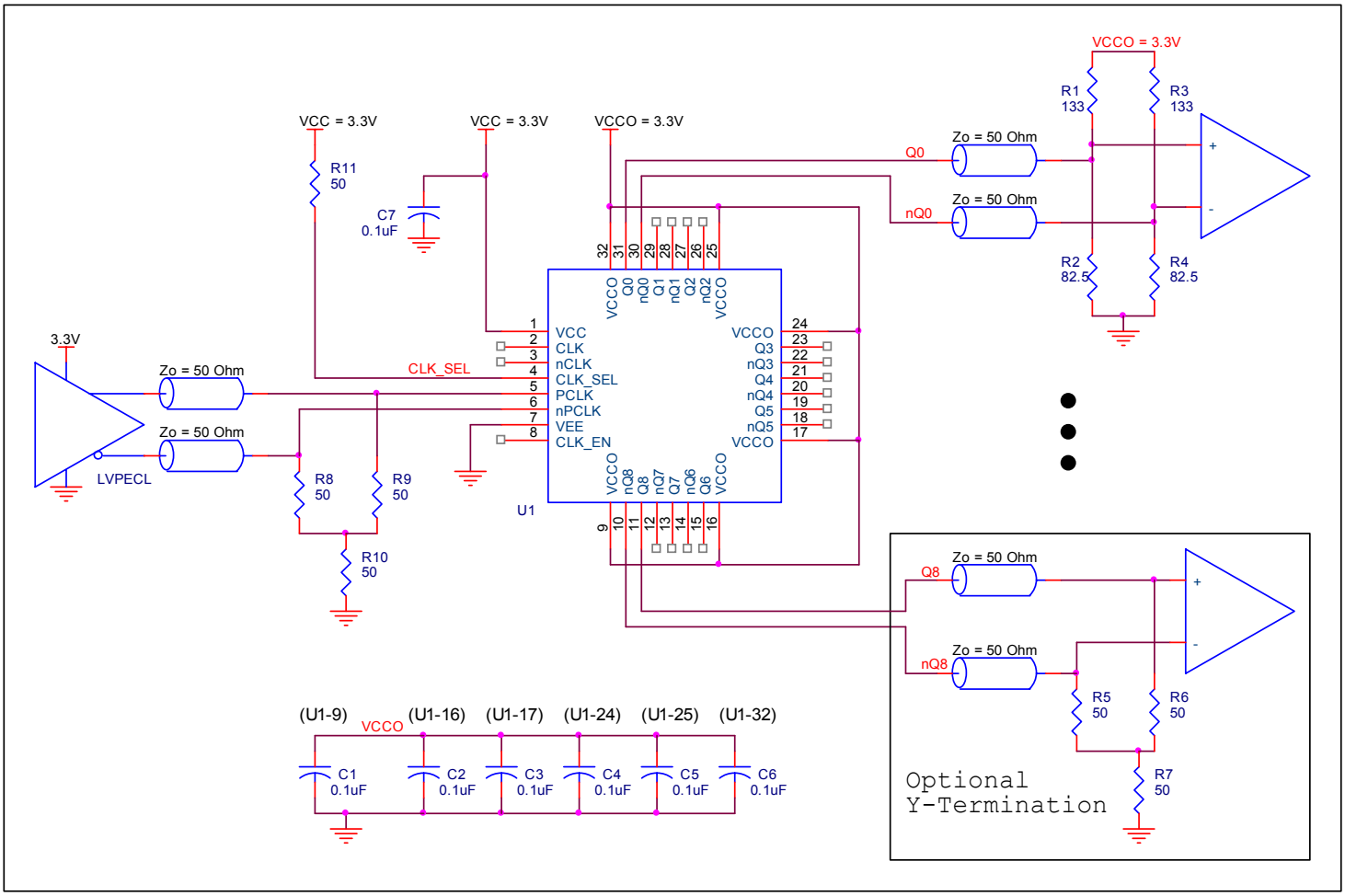


Figure 7. ICS853S031I Example LVPECL Clock Output Buffer Schematic

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Power Considerations

This section provides information on power dissipation and junction temperature for the ICS853S031I.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS853S031I is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{CC} = 3.465V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)$_{MAX}$ = V_{CC_MAX} * I_{EE_MAX} = 3.465V * 70mA = **242.55mW**
- Power (outputs)$_{MAX}$ = **33.71mW/Loaded Output pair**
  If all outputs are loaded, the total power is 9 * 33.71mW = **303.39mW**

Total Power$_{_MAX}$ (3.465V, with all outputs switching) = 303.39mW + 242.55mW = **545.94mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming a moderate air flow of 1 meter per second and a multi-layer board, the appropriate value is 71.4°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.546W * 71.4°C/W = 124°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 6. Thermal Resistance θ_{JA} for 32 Lead LQFP, Forced Convection

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	80.9°C/W	71.4°C/W	67.7°C/W

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3. Calculations and Equations.

The purpose of this section is to calculate power dissipation on the LVPECL output pairs.

LVPECL output driver circuit and termination are shown in *Figure 8.*

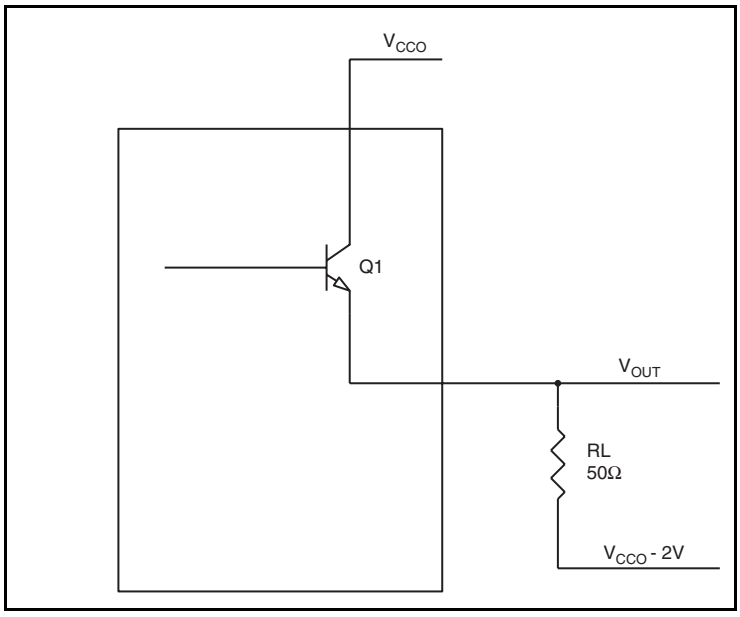


Figure 8. LVPECL Driver Circuit and Termination

To calculate typical case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of V_{CCO} – 2V.

- For logic high, $V_{OUT} = V_{OH_MAX} = \mathbf{V_{CCO_MAX}} - \mathbf{0.71V}$
  $(V_{CCO_MAX} - V_{OH_MAX}) = \mathbf{0.71V}$
- For logic low, $V_{OUT} = V_{OL_MAX} = \mathbf{V_{CCO_MAX}} - \mathbf{1.48V}$
  $(V_{CCO_MAX} - V_{OL_MAX}) = \mathbf{1.48V}$

Pd_H is power dissipation when the output drives high.

Pd_L is the power dissipation when the output drives low.

$Pd_H = [(V_{OH_MAX} – (V_{CCO_MAX} – 2V))/R_L] * (V_{CCO_MAX} – V_{OH_MAX}) = [(2V – (V_{CCO_MAX} – V_{OH_MAX}))/R_L] * (V_{CCO_MAX} – V_{OH_MAX}) =$
$[(2V – 0.71V)/50Ω] * 0.71V =$ **18.32mW**

$Pd_L = [(V_{OL_MAX} – (V_{CCO_MAX} – 2V))/R_L] * (V_{CCO_MAX} – V_{OL_MAX}) = [(2V – (V_{CCO_MAX} – V_{OL_MAX}))/R_L] * (V_{CCO_MAX} – V_{OL_MAX}) =$
$[(2V – 1.48V)/50Ω] * 1.48V =$ **15.39mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **33.71mW**

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Reliability Information

Table 7. θ_{JA} vs. Air Flow Table for a 32 Lead LQFP

θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	80.9°C/W	71.4°C/W	67.7°C/W

Transistor Count

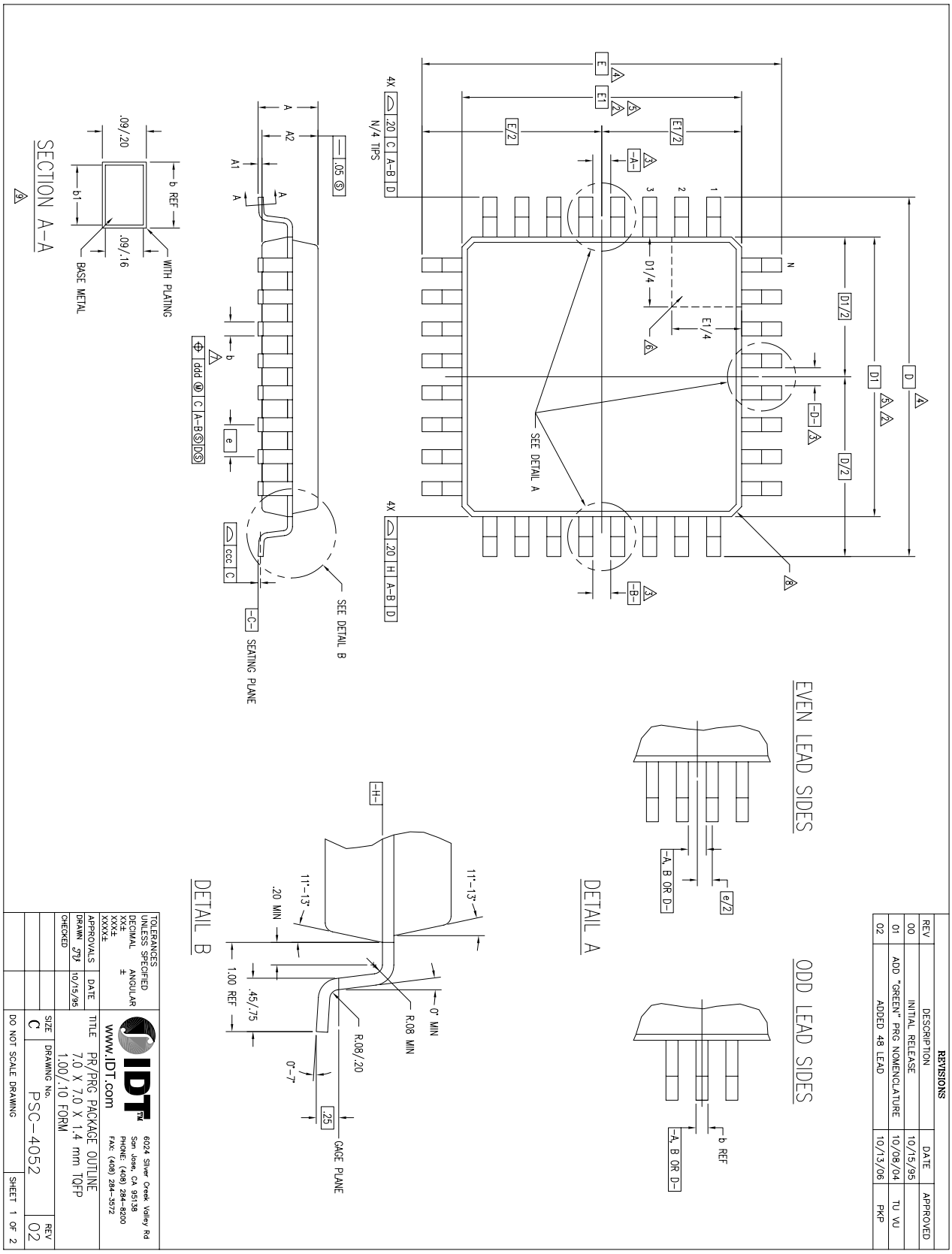
The transistor count for ICS853S031I is: 383

Pin compatible with ICS8531-01
This device is pin and functional compatible, and is the suggested replacement for the ICS853031.

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Package Outline and Package Dimensions

Package Outline - Y Suffix for 32 Lead LQFP



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Package Outline and Package Dimensions, continued

Package Outline - Y Suffix for 32 Lead LQFP

SYMBOL	JEDEC VARIATION BBA			NOTE
	MIN	NOM	MAX	
A	–	–	1.60	
A1	.05	.10	.15	
A2	1.35	1.40	1.45	
D	9.00 BSC			4
D1	7.00 BSC			5,2
E	9.00 BSC			4
E1	7.00 BSC			5,2
N	32			
e	.80 BSC			
b	.30	.37	.45	7
b1	.30	.35	.40	
ccc	–	–	.10	
ddd	–	–	.20	

SYMBOL	JEDEC VARIATION BBC			NOTE
	MIN	NOM	MAX	
A	–	–	1.60	
A1	.05	.10	.15	
A2	1.35	1.40	1.45	
D	9.00 BSC			4
D1	7.00 BSC			5,2
E	9.00 BSC			4
E1	7.00 BSC			5,2
N	48			
e	.50 BSC			
b	.17	.22	.27	7
b1	.17	.20	.23	
ccc	–	–	.08	
ddd	–	–	.08	

NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982
2. TOP PACKAGE MAY BE SMALLER THAN BOTTOM PACKAGE BY .15 mm
3. DATUMS [A-B] AND [-D-] TO BE DETERMINED AT DATUM PLANE [-H-]
4. DIMENSIONS D AND E ARE TO BE DETERMINED AT SEATING PLANE [-C-]
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS .25 mm PER SIDE. D1 AND E1 ARE MAXIMUM BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH
6. DETAILS OF PIN 1 IDENTIFIER IS OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED
7. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS .08 mm IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.
8. EXACT SHAPE OF EACH CORNER IS OPTIONAL
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .10 AND .25 mm FROM THE LEAD TIP
10. ALL DIMENSIONS ARE IN MILLIMETERS
11. THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MS-026, VARIATIONS BBA & BBC.

LAND PATTERN DIMENSIONS

	MIN	MAX
P	9.80	10.00
P1	6.80	7.00
P2	5.60 BSC	
X	.40	.60
e	.80 BSC	
N	32	

	MIN	MAX
P	9.80	10.00
P1	6.80	7.00
P2	5.50 BSC	
X	.25	.35
e	.50 BSC	
N	48	

REVISIONS

DCN	REV	DESCRIPTION	DATE	APPROVED
28215	00	INITIAL RELEASE	10/15/95	TU VU
	01	ADD "GREEN" PRG NOMENCLATURE	10/08/04	TU VU
	02	ADDED 48 LEAD	10/13/06	PKP

TOLERANCES UNLESS SPECIFIED
DECIMAL ANGULAR
XX± ±
XXX±
XXXX±
APPROVALS DATE
DRAWN 10/15/95
CHECKED

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San Jose, CA 95138
PHONE: (408) 284-8200
FAX: (408) 284-3572
www.IDT.com

TITLE PR/PRG PACKAGE OUTLINE
7.0 X 7.0 X 1.4 mm TQFP
1.00/.10 FORM

SIZE C
DRAWING No. PSC-4052
REV 02

DO NOT SCALE DRAWING
SHEET 2 OF 2

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Ordering Information

Table 8. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
853S031BYILF	ICS53S031BIL	Lead-Free, 32 Lead LQFP	Tray	-40°C to 85°C
853S031BYILFT	ICS53S031BIL	Lead-Free, 32 Lead LQFP	1000 Tape & Reel	-40°C to 85°C

NOTE: Parts that are ordered with an “LF” suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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Revision History Sheet

Rev	Table	Page	Description of Change	Date
A		18	Corrected package information.	8/17/11

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(Rev.1.0 Mar 2020)

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