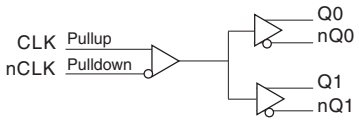
General Description

The 85411 is a low skew, high performance 1-to-2 Differential-to-LVDS Fanout Buffer and a member of the family of High Performance Clock Solutions from IDT. The CLK, nCLK pair can accept most standard differential input levels.The 85411 is characterized to operate from a 3.3V power supply. Guaranteed output and part-to-part skew characteristics make the 85411 ideal for those clock distribution applications demanding well defined performance and repeatability.

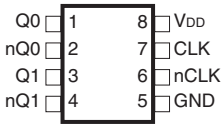
Features

- Two differential LVDS outputs
- One differential CLK, nCLK clock input
- CLK, nCLK pair can accept the following differential input levels: LVPECL, LVDS, LVHSTL, SSTL, HCSL
- Maximum output frequency: 650MHz
- Translates any single ended input signal to LVDS levels with resistor bias on nCLK input
- Output skew: 20ps (maximum)
- Part-to-part skew: 250ps (maximum)
- Additive phase jitter, RMS: 0.05ps (typical)
- Propagation delay: 2.5 ns (maximum)
- 3.3V operating supply
- 0°C to 70°C ambient operating temperature
- Available in lead free (RoHS 6) package

Block Diagram



Pin Assignment



85411
8-Lead SOIC
3.90mm x 4.90mm x 1.37mm package body
M Package
Top View

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Table 1. Pin Descriptions

Number	Name	Type		Description
1, 2	Q0, nQ0	Output		Differential output pair. LVDS interface levels.
3, 4	Q1, nQ1	Output		Differential output pair. LVDS interface levels.
5	GND	Power		Power supply ground.
6	nCLK	Input	Pulldown	Inverting differential clock input.
7	CLK	Input	Pullup	Non-inverting differential clock input.
8	V_{DD}	Power		Positive supply pin.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ

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Absolute Maximum Ratings

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5V
Outputs, I_O	
Continuous Current	10mA
Surge Current	15mA
Package Thermal Impedance, θ_{JA}	112.7°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Table 3A. Power Supply DC Characteristics, V_{DD} = 3.3V±10%, T_A = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Positive Supply Voltage		2.97	3.3	3.63	V
I_{DD}	Power Supply Current				50	mA

Table 3B. Differential DC Characteristics, V_{DD} = 3.3V±10%, T_A = 0°C to 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	CLK	$V_{DD} = V_{IN}$ = 3.63V			5	µA
		nCLK	$V_{DD} = V_{IN}$ = 3.63V			150	µA
I_{IL}	Input Low Current	CLK	V_{DD} = 3.63, V_{IN} = 0V	-150			µA
		nCLK	V_{DD} = 3.63V, V_{IN} = 0V	-5			µA
V_{PP}	Peak-to-Peak Input Voltage; NOTE 1			0.15		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			0.5		V_{DD} - 0.85	V

NOTE 1: V_{IL} should not be less than -0.3V.
NOTE 2: Common mode voltage is defined as V_{IH}.

Table 3C. LVDS DC Characteristics, V_{DD} = 3.3V±10%, T_A = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage		247	325	454	mV
ΔV_{OD}	VOD Magnitude Change			0	50	mV
V_{OS}	Offset Voltage		1.325	1.45	1.575	V
ΔV_{OS}	VOS Magnitude Change			5	50	mV
I_{OFF}	Power Off Leakage		-20	±1	+20	µA
I_{OSD}	Differential Output Short Circuit Current			-3.5	-5	mA
I_{OS}	Output Short Circuit Current			-3.5	-5	mA

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TABLE 4. AC CHARACTERISTICS, V_{DD} = 3.3V±10% T_A = 0°C TO 70°C

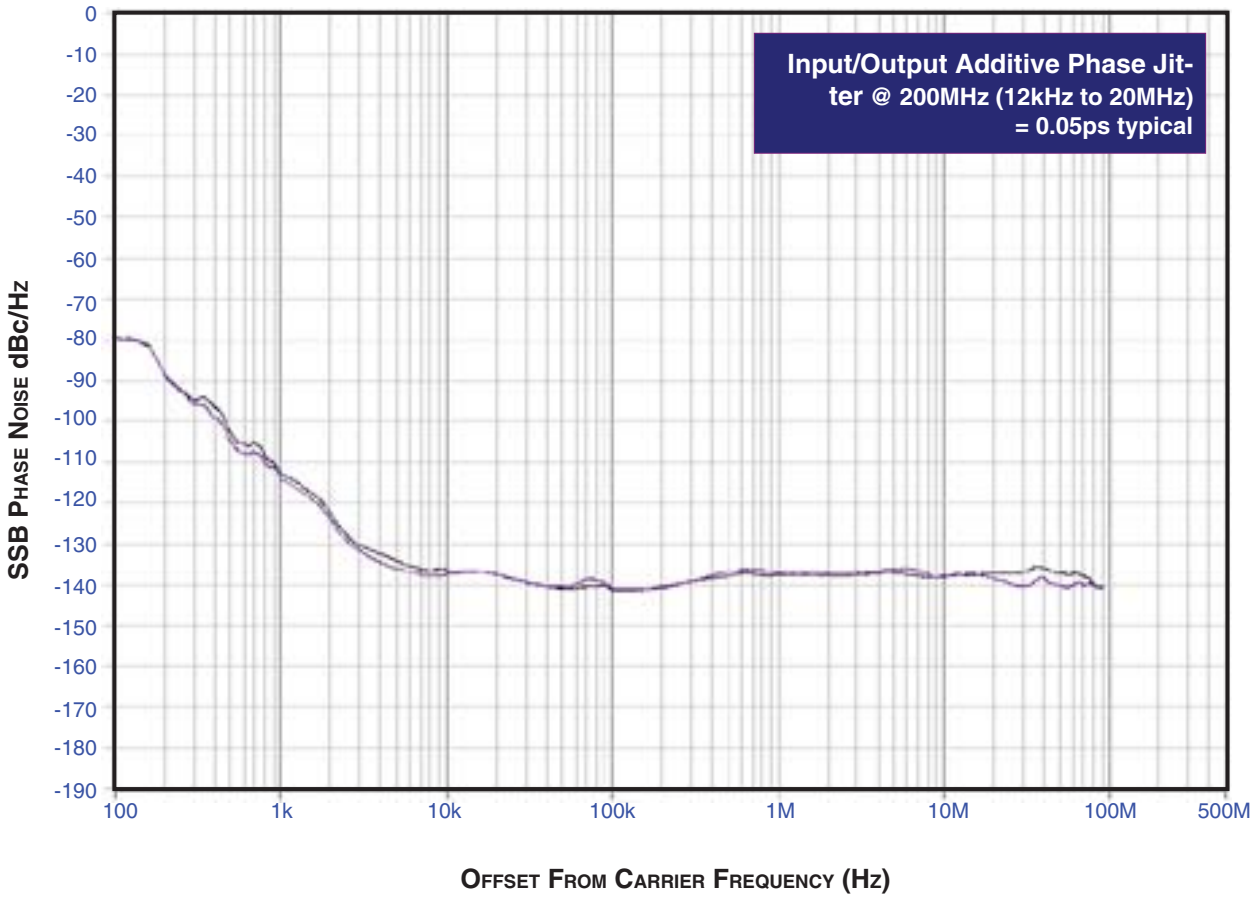
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				650	MHz
t_{PD}	Propagation Delay; NOTE 1		1.5		2.5	ns
*t*sk(o)	Output Skew; NOTE 2, 4				20	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 3, 4				250	ps
*t*jit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section	(12kHz to 20MHz)		0.05		ps
t_R / t_F	Output Rise/Fall Time	20% to 80% @ 50MHz	150		350	ps
odc	Output Duty Cycle	> 500MHz	47		53	%
		≤ 500MHz	48		52	%

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
All parameters measured at $f \leq 650$MHz unless noted otherwise.
NOTE 1: Measured from the differential input crossing point to the differential output crossing point.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential cross points.
NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

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Additive Phase Jitter

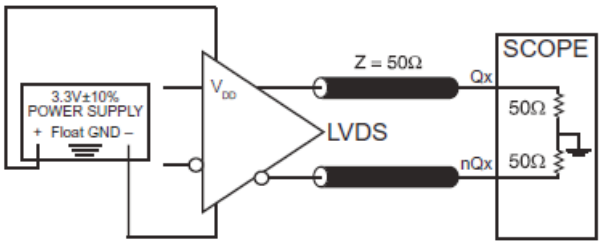
The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the ***dBc Phase Noise.*** This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a ***dBc*** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.



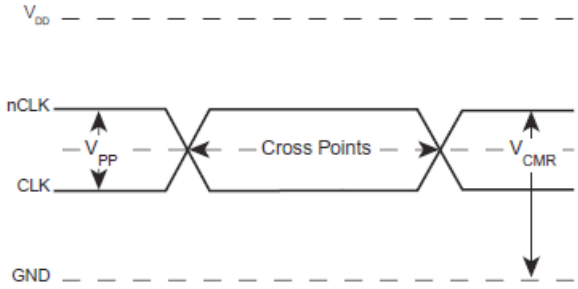
As with most timing specifications, phase noise measurements has issues relating to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This is illustrated above. The device meets the noise floor of what is shown, but can actually be lower. The phase noise is dependent on the input source and measurement equipment.

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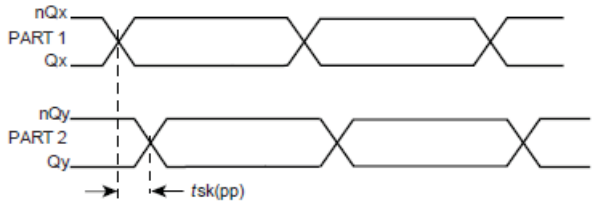
Parameter Measurement Information



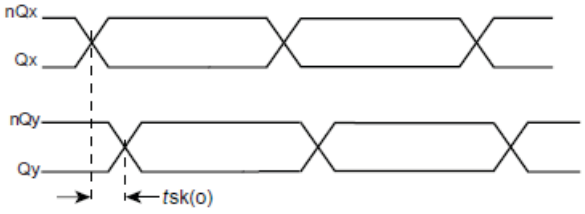
3.3V Output Load AC Test Circuit



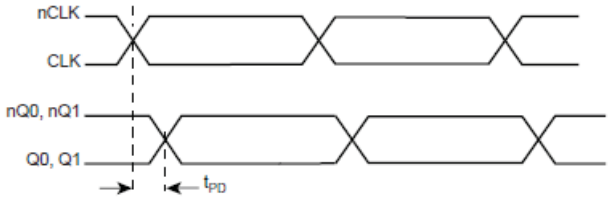
Differential Input Level



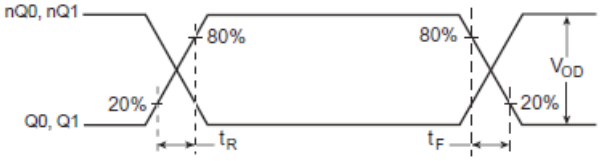
Part-to-Part Skew



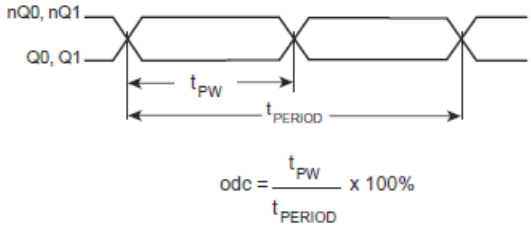
Output Skew



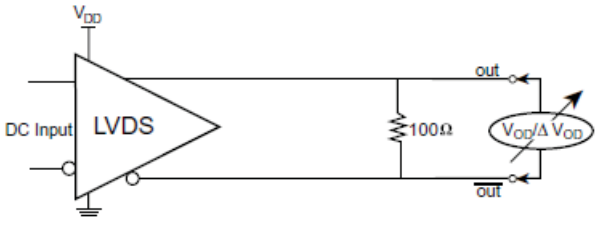
Propagation Delay



Output Rise/Fall Time

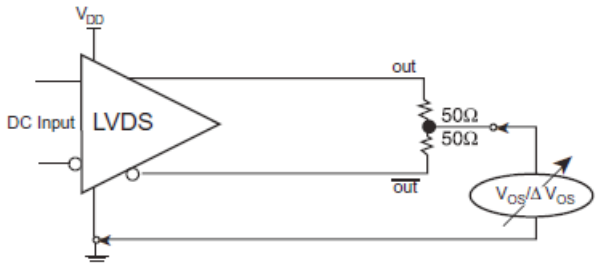


Output Duty Cycle/Pulse Width/Period

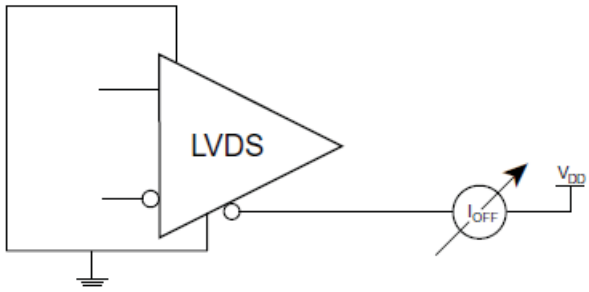


Differential Output Voltage Setup

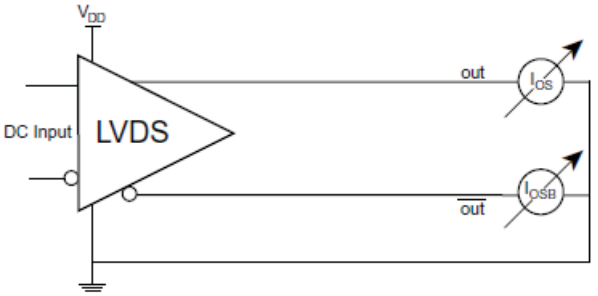
PARAMETER MEASUREMENT INFORMATION, CONTINUED



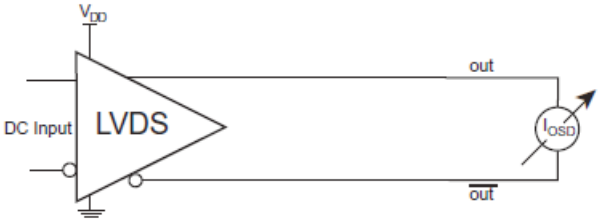
OFFSET VOLTAGE SETUP



POWER OFF LEAKAGE SETUP



OUTPUT SHORT CIRCUIT CURRENT SETUP



DIFFERENTIAL OUTPUT SHORT CIRCUIT CURRENT SETUP

Application Information

Wiring the Differential Input to Accept Single Ended Levels

Figure 1 shows how the differential input can be wired to accept single ended levels. The reference voltage V_REF = V_{DD}/2 is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and V_{DD} = 3.3V, V_REF should be 1.25V and R2/R1 = 0.609.

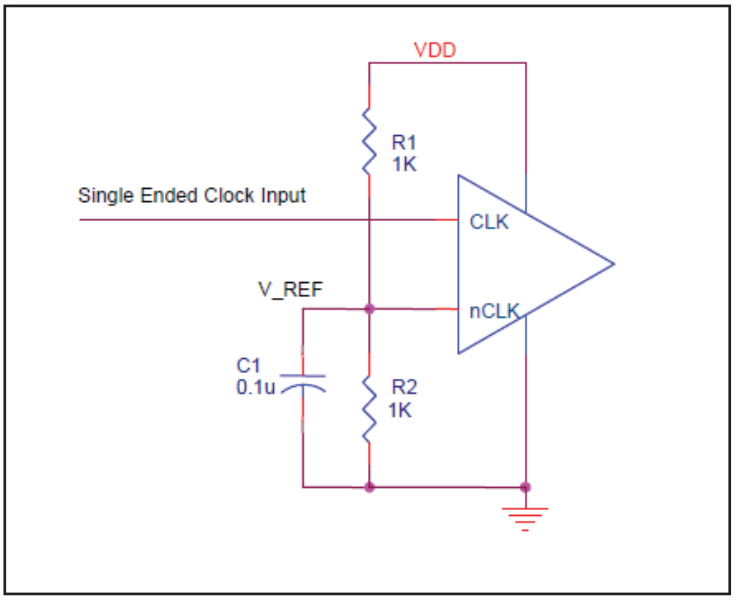


Figure 1. Single Ended Signal Driving Differential Input

Recommendations for Unused Output Pins

Outputs:

LVDS

All unused LVDS output pairs can be either left floating or terminated with 100Ω across. If they are left floating, there should be no trace attached.

Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, SSTL, HCSL and other differential signals. Both signals must meet the V_{PP} and V_{CMR} input requirements. Figures 2A to 2E show interface examples for the HiPerClockS CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only.

Please consult with the vendor of the driver component to confirm the driver termination requirements. For example in *Figure 2A,* the input termination applies for IDT HiPerClockS LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

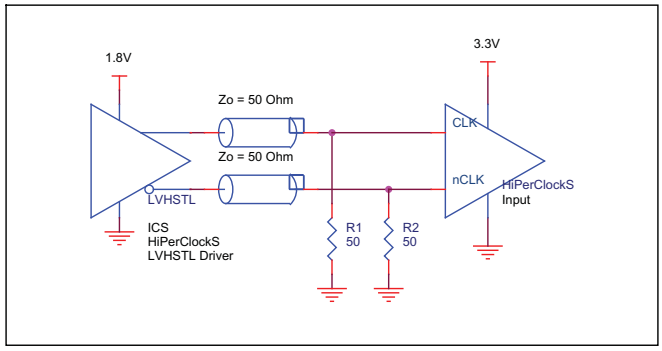


Figure 2A. HiPerClockS CLK/nCLK Input Driven by IDT HiPerClockS LVHSTL Driver

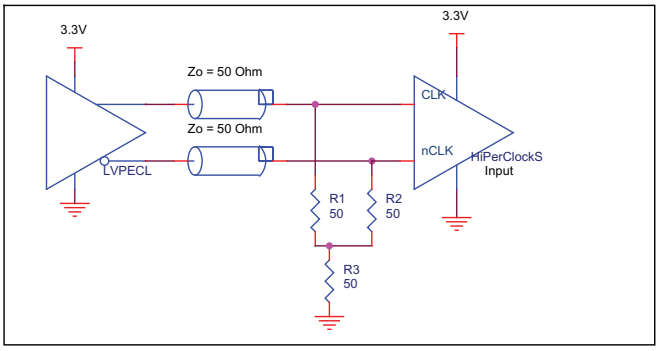


Figure 2B. HiPerClockS CLK/nCLK Input Driven by 3.3V LVPECL Driver

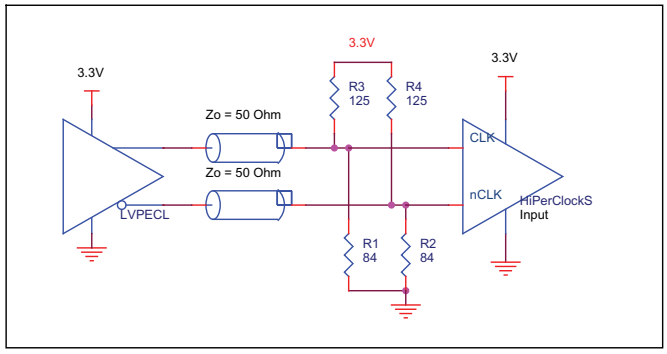


Figure 2C. HiPerClockS CLK/nCLK Input Driven by 3.3V LVPECL Driver

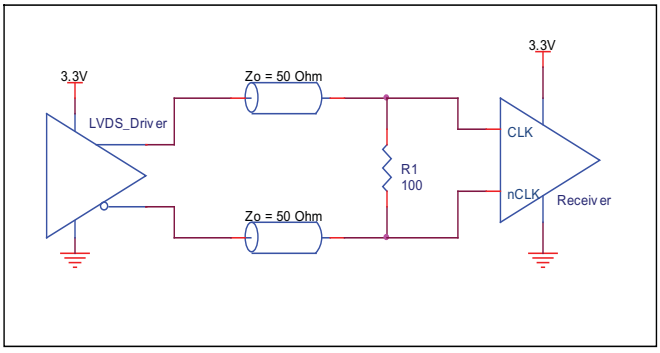


Figure 2D. HiPerClockS CLK/nCLK Input Driven by 3.3V LVDS Driver

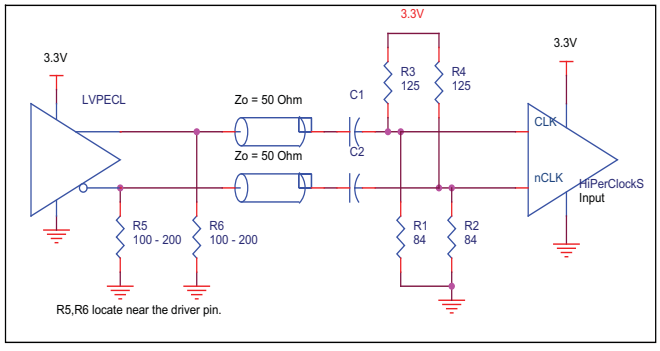


Figure 2E. HiPerClockS CLK/nCLK Input Driven by 3.3V LVPECL Driver with AC Couple

LVDS Driver Termination

A general LVDS interface is shown in *Figure 3.* In a 100Ω differential transmission line environment, LVDS drivers require a matched load termination of 100Ω across near the receiver input. For a multiple LVDS outputs buffer, if only partial outputs are used, it is recommended to terminate the unused outputs.

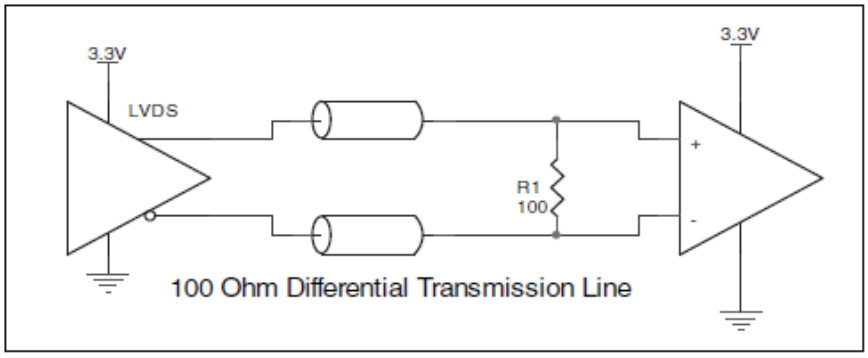


Figure 3. Typical LVDS Driver Termination

Power Considerations

This section provides information on power dissipation and junction temperature for the 85411.
Equations and example calculations are also provided.

1. Power Dissipation.
The total power dissipation for the 85411 is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{DD} = 3.3V + 10% = 3.63V, which gives worst case results.

- Power (core)$_{MAX}$ = V_{DD_MAX} * I_{DD_MAX} = 3.63V * 50mA = **181.5mW**

2. Junction Temperature.
Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)
T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming a moderate air flow of 200 linear feet per minute and a multi-layer board, the appropriate value is 103.3°C/W per Table 5 below.

Therefore, Tj for an ambient temperature of 70°C with all outputs switching is:
70°C + 0.182W * 103.3°C/W = 88.8°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (multi-layer).

Table 5. Thermal Resistance θ_{JA} for 8-Lead SOIC, Forced Convection

θ_{JA} by Velocity (Linear Feet per Minute)	0	200	500
Single-Layer PCB, JEDEC Standard Test Boards	153.3°C/W	128.5°C/W	115.5°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	112.7°C/W	103.3°C/W	97.1°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

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Reliability Information

Table 6. θ_{JA} vs. Air Flow Table for 8 Lead SOIC

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	153.3°C/W	128.5°C/W	115.5°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	112.7°C/W	103.3°C/W	97.1°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

Transistor Count

The transistor count for 85411 is: 636

Package Outline & Dimensions

Package Outline - M Suffix for 8 Lead SOIC

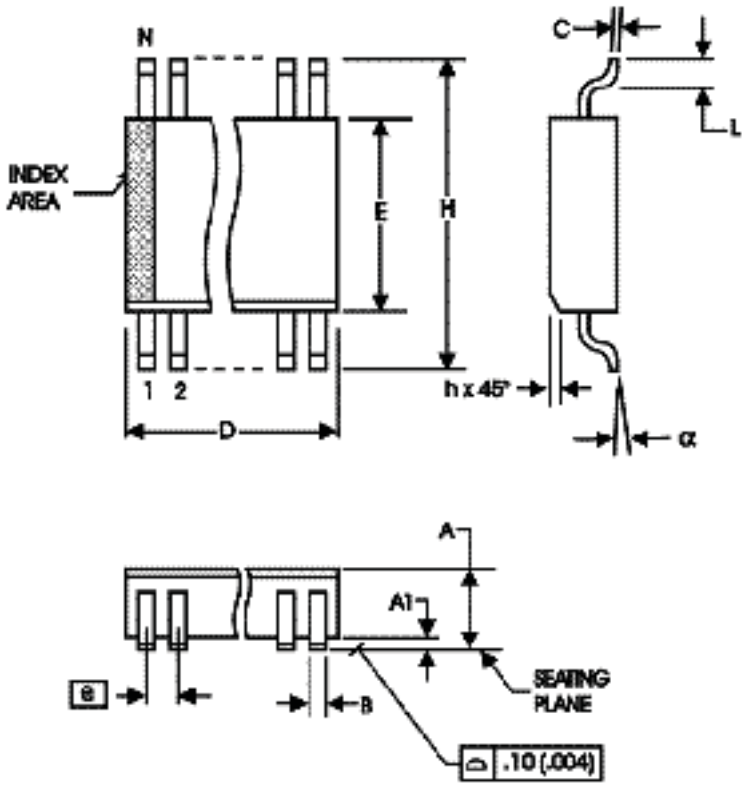


Table 7. Package Dimensions

SYMBOL	Millimeters	
	MINIMUN	MAXIMUM
N	8	
A	1.35	1.75
A1	0.10	0.25
B	0.33	0.51
C	0.19	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BASIC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.27
α	0°	8°

Reference Document: JEDEC Publication 95, MS-012

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TABLE 8. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
85411AMLF	85411ALF	8 lead “Lead Free” SOIC	Tray	0°C to +70°C
85411AMLFT	85411ALF	8 lead “Lead Free” SOIC	Tape and Reel	0°C to +70°C

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REVISION HISTORY SHEET				
Rev	**Table**	**Page**	**Description of Change**	**Date**
B	T4	1 4 5	Features - added Additive Phase Jitter bullet. AC Characteristics table - added tjit row. Added Additive Phase Jitter Application Note	6/9/04
B	T7	12	Ordering Information Table - added Lead Free Part Number.	6/16/04
C	T3C	3 8 11	Changed V_{DD} from ±5% to ±10% throughout datasheet. LVDS DC Characteristics Table - changed V_{OD} range from 200mV min./360mV max. to 247mV min./454mV max. Changed ΔV_{OD} from 40mV max. to 50mV max. Changed V_{OS} from 1.125mV min./1.375mV max. to 1.325mV min./1.575mV max. Changed ΔV_{OS} from 25mV max. to 50mV max. Added *Recommendations for Unused Output Pins.* Added *Power Considerations.*	9/19/06
C	T8	14	Ordering Information Table - corrected lead-free marking.	1/17/07
C	T3C	3	LVDS DC Characteristics Table - deleted V_{OH} & V_{OL} rows.	1/20/09
C	T8	 1 1 13	Removed ICS from part numbers where needed. General Description - Deleted the ICS chip and removed HiPerClockS. Features - removed reference to leaded part numbers. Ordering Information - removed quantity for tape and reel. Deleted LF note below the table. Updated header and footer.	1/20/16

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(Rev.1.0 Mar 2020)

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