Low Skew, 1-to-5, Differential-to-LVDS/LVPECL Fanout Buffer

ICS854S015I-01

DATA SHEET

General Description

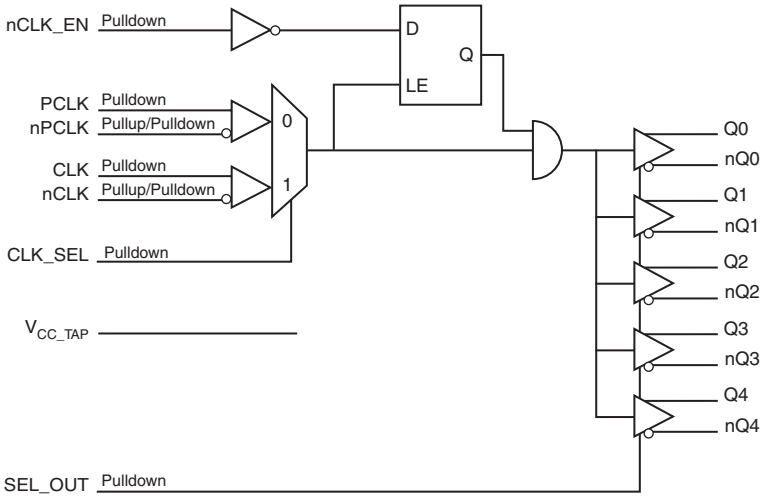
The ICS854S015I-01 is a low skew, high performance 1-to-5, 2.5V, 3.3V Differential-to-LVPECL/LVDS Fanout Buffer. The ICS854S015I-01 has two selectable differential clock inputs.

Guaranteed output and part-to-part skew characteristics make the ICS854S015I-01 ideal for those applications demanding well defined performance and repeatability.

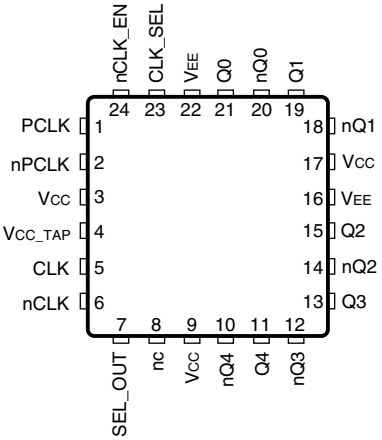
Features

- Five differential LVPECL or LVDS output pairs
- Two differential clock input pairs
- CLK, nCLK pair can accept the following differential input levels: LVDS, LVPECL, LVHSTL, HCSL
- PCLK, nPCLK can accept the following input levels: LVPECL, LVDS, CML
- Either CLK or PCLK inputs can be configured to accept single-ended inputs
- Maximum output frequency: 2GHz
- Additive phase jitter, RMS: 0.065ps (maximum), 3.3V, 156.25MHz, 12kHz – 5MHz)
- Output Skew: 55ps (maximum)
- Propagation delay: 570ps (typical) @ 3.3V
- Full 3.3V or 2.5V supply modes
- -40°C to 85°C ambient operating temperature
- Available in lead-free (RoHS 6) package

Block Diagram



Pin Assignment



ICS854S015I-01

24-Lead VFQFN

4mm x 4mm x 0.925mm package body

K Package

Top View

© 2019 Renesas Electronics Corporation

Table 1. Pin Descriptions

Number	Name	Type		Description
1	PCLK	Input	Pulldown	Non-inverting differential LVPECL clock input.
2	nPCLK	Input	Pullup/ Pulldown	Inverting differential LVPECL clock input. V_{CC}/2 default when left floating.
3, 9, 17	V_{CC}	Power		Positive supply pins.
4	V_{CC_TAP}	Power		Power supply pin. See Table 3C.
5	CLK	Input	Pulldown	Non-inverting differential clock input.
6	nCLK	Input	Pullup/ Pulldown	Inverting differential clock input. V_{CC}/2 default when left floating.
7	SEL_OUT	Input	Pulldown	Output select pin. When LOW, selects LVDS output levels. When HIGH, selects LVPECL output levels. See Table 3. LVCMOS/LVTTL interface levels.
8	nc	Unused		No-connect.
10, 11	nQ4, Q4	Output		Differential output pair. LVDS or LVPECL interface levels.
12, 13	nQ3, Q3	Output		Differential output pair. LVDS or LVPECL interface levels.
14, 15	nQ2, Q2	Output		Differential output pair. LVDS or LVPECL interface levels.
16, 22	V_{EE}	Power		Negative supply pins.
18, 19	nQ1, Q1	Output		Differential output pair. LVDS or LVPECL interface levels.
20, 21	nQ0, Q0	Output		Differential output pair. LVDS or LVPECL interface levels.
23	CLK_SEL	Input	Pulldown	Clock select input. When HIGH, selects CLK, nCLK inputs. When LOW, selects PCLK, nPCLK inputs. LVTTL / LVCMOS interface levels.
24	nCLK_EN	Input	Pulldown	Synchronizing clock enable. When LOW, clock outputs follow clock input. When HIGH, Qx outputs are forced low, nQx outputs are forced high. LVTTL / LVCMOS interface levels.

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			2		pF
$R_{PULLDOWN}$	Input Pulldown Resistor			50		kΩ
$R_{VCC}/2$	Pullup/Pulldown Resistor			50		kΩ

© 2019 Renesas Electronics Corporation

Function Tables

Table 3A. Control Input Function Table

Inputs			Outputs	
nCLK_EN	**CLK_SEL**	**Selected Source**	**Q[0:4]**	**nQ[0:4]**
0	0	PCLK, nPCLK	Enabled	Enabled
0	1	CLK, nCLK	Enabled	Enabled
1	0	PCLK, nPCLK	Disabled; Low	Disabled; High
1	1	CLK, nCLK	Disabled; Low	Disabled; High

After nCLK_EN switches, the clock outputs are disabled or enabled following a falling input clock edge as shown in Figure 1. In the active mode, the state of the outputs are a function of the PCLK, nPCLK and CLK, nCLK inputs as described in Table 3B.

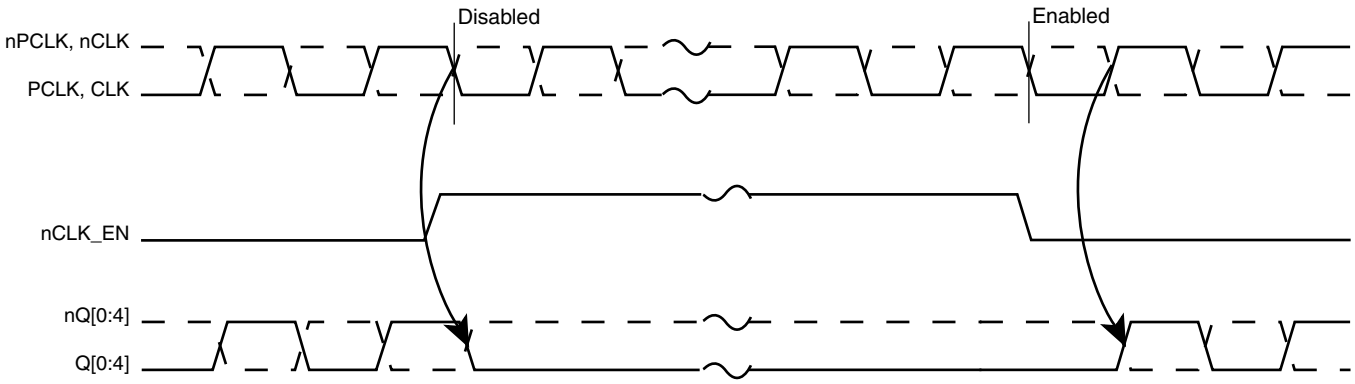


Figure 1. nCLK_EN Timing Diagram

Table 3B. Clock Input Function Table

Inputs		Outputs			
PCLK or CLK	**nPCLK or nCLK**	**Q[0:4]**	**nQ[0:4]**	**Input to Output Mode**	**Polarity**
0	1	LOW	HIGH	Differential to Differential	Non-Inverting
1	0	HIGH	LOW	Differential to Differential	Non-Inverting

Table 3C. V_{CC_TAP} Function Table

Outputs		
Q[0:4], nQ[0:4]	**Output Level Supply**	**V_{CC_TAP}**
LVPECL	2.5V	2.5V
LVPECL	**3.3V**	**3.3V**
LVDS	2.5V	2.5V
LVDS	3.3V	Float

Table 3D. SEL_OUT Function Table

Input	Outputs
SEL_OUT	**Q[0:4], nQ[0:4]**
0 (default)	LVDS
1	LVPECL

© 2019 Renesas Electronics Corporation

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{CC}	4.6V
Inputs, V_I	-0.5V to V_{CC} + 0.5V
Outputs, I_O (LVPECL) Continuous Current Surge Current Outputs, I_O (LVDS) Continuous Current Surge Current	 50mA 100mA 10mA 15mA
Package Thermal Impedance, θ_{JA}	49.5°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. LVPECL Power Supply DC Characteristics, $V_{CC} = V_{CC_TAP} = 3.3V \pm 5\%$, $V_{EE} = 0V$, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Positive Supply Voltage		3.135	3.3	3.465	V
V_{CC_TAP}	Power Supply Voltage		3.135	3.3	3.465	V
I_{EE}	Power Supply Current				85	mA
I_{TAP}	Power Supply Current				5	mA

Table 4B. LVPECL Power Supply DC Characteristics, $V_{CC} = V_{CC_TAP} = 2.5V \pm 5\%$, $V_{EE} = 0V$, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Positive Supply Voltage		2.375	2.5	2.625	V
V_{CC_TAP}	Power Supply Voltage		2.375	2.5	2.625	V
I_{EE}	Power Supply Current				78	mA
I_{TAP}	Power Supply Current				5	mA

© 2019 Renesas Electronics Corporation

Table 4C. LVDS Power Supply DC Characteristics, V_{CC} = 3.3V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Positive Supply Voltage		3.135	3.3	3.465	V
I_{CC}	Power Supply Current				160	mA

NOTE: V_{CC_TAP} is left floating for 3.3V operation.

Table 4D. LVDS Power Supply DC Characteristics, V_{CC} = V_{CC_TAP} = 2.5V ± 5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Positive Supply Voltage		2.375	2.5	2.625	V
V_{CC_TAP}	Power Supply Voltage		2.375	2.5	2.625	V
I_{CC}	Power Supply Current				150	mA
I_{CC_TAP}	Power Supply Current				5	mA

Table 4E. LVCMOS/LVTTL DC Characteristics, V_{CC} = 3.3V ± 5% or V_{CC} = V_{CC_TAP} = 2.5V ± 5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		V_{CC} = 3.465V	2.2		V_{CC} + 0.3	V
			V_{CC} = 2.625V	1.7		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage		V_{CC} = 3.465V	-0.3		0.8	V
			V_{CC} = 2.625V	-0.3		0.7	V
I_{IH}	Input High Current	CLK_SEL, SEL_OUT, nCLK_EN	V_{CC} = V_{IN} = 3.465V or 2.625V			150	µA
I_{IL}	Input Low Current	CLK_SEL, SEL_OUT, nCLK_EN	V_{CC} = 3.465V or 2.625V, V_{IN} = 0V	-10			µA

Table 4F. Differential DC Characteristics, V_{CC} = 3.3V ± 5% or V_{CC} = V_{CC_TAP} = 2.5V ± 5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	CLK, nCLK	V_{CC} = V_{IN} = 3.465V			150	µA
I_{IL}	Input Low Current	CLK	V_{CC} = 3.465V, V_{IN} = 0V	-10			µA
		nCLK	V_{CC} = 3.465V, V_{IN} = 0V	-150			µA
V_{PP}	Peak-to-Peak Input Voltage	CLK, nCLK		0.15		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1	CLK, nCLK		V_{EE} + 0.5		V_{CC} – 0.85	V

NOTE 1. Common mode voltage is defined as V_{IH}.

© 2019 Renesas Electronics Corporation

Table 4G. LVPECL DC Characteristics, $V_{CC} = V_{CC_TAP} = 3.3V \pm 5\%$, $V_{EE} = 0V$, $T_A = -40°C$ to $85°C$

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	PCLK, nPCLK	$V_{CC} = V_{IN} = 3.465V$			150	µA
I_{IL}	Input Low Current	PCLK	$V_{CC} = 3.465V$, $V_{IN} = 0V$	-10			µA
		nPCLK	$V_{CC} = 3.465V$, $V_{IN} = 0V$	-150			µA
V_{PP}	Peak-to-Peak Input Voltage	PCLK, nPCLK		0.15		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1	PCLK, nPCLK		$V_{EE} + 1.2$		V_{CC}	V
V_{OH}	Output High Voltage; NOTE 2		SEL_OUT = 1	$V_{CC} - 1.4$		$V_{CC} - 0.9$	V
V_{OL}	Output Low Voltage; NOTE 2		SEL_OUT = 1	$V_{CC} - 2.0$		$V_{CC} - 1.7$	V
V_{SWING}	Peak-to-peak Output Voltage Swing		SEL_OUT = 1	0.6		1.0	V

NOTE 1. Common mode voltage is defined as V_{IH}.
NOTE 2: Outputs terminated with 50Ω to $V_{CC} - 2V$.

Table 4H. LVPECL DC Characteristics, $V_{CC} = V_{CC_TAP} = 2.5V \pm 5\%$, $V_{EE} = 0V$, $T_A = -40°C$ to $85°C$

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	PCLK, nPCLK	$V_{CC} = V_{IN} = 2.625V$			150	µA
I_{IL}	Input Low Current	PCLK	$V_{CC} = 2.625V$, $V_{IN} = 0V$	-10			µA
		nPCLK	$V_{CC} = 2.625V$, $V_{IN} = 0V$	-150			µA
V_{PP}	Peak-to-Peak Input Voltage	PCLK, nPCLK		0.15		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1	PCLK, nPCLK		$V_{EE} + 1.2$		V_{CC}	V
V_{OH}	Output High Voltage; NOTE 2		SEL_OUT = 1	$V_{CC} - 1.4$		$V_{CC} - 0.9$	V
V_{OL}	Output Low Voltage; NOTE 2		SEL_OUT = 1	$V_{CC} - 2.0$		$V_{CC} - 1.5$	V
V_{SWING}	Peak-to-peak Output Voltage Swing		SEL_OUT = 1	0.4		1.0	V

NOTE 1. Common mode voltage is defined as V_{IH}.
NOTE 2: Outputs terminated with 50Ω to $V_{CC} - 2V$.

Table 4I. LVDS DC Characteristics, $V_{CC} = 3.3V \pm 5\%$, $T_A = -40°C$ to $85°C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage	SEL_OUT = 0	247		454	mV
ΔV_{OD}	V_{OD} Magnitude Change	SEL_OUT = 0			50	mV
V_{OS}	Offset Voltage	SEL_OUT = 0	1.125		1.375	V
ΔV_{OS}	V_{OS} Magnitude Change	SEL_OUT = 0			50	mV

Table 4J. LVDS DC Characteristics, $V_{CC} = V_{CC_TAP} = 2.5V \pm 5\%$, $T_A = -40°C$ to $85°C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage	SEL_OUT = 0	247		454	mV
ΔV_{OD}	V_{OD} Magnitude Change	SEL_OUT = 0			50	mV
V_{OS}	Offset Voltage	SEL_OUT = 0	1.105		1.375	V
ΔV_{OS}	V_{OS} Magnitude Change	SEL_OUT = 0			50	mV

© 2019 Renesas Electronics Corporation

AC Electrical Characteristics

Table 5A. LVPECL AC Characteristics, $V_{CC} = V_{CC_TAP} = 3.3V \pm 5\%$, $V_{EE} = 0V$, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency				2	GHz
t_{PD}	Propagation Delay, Low-to-High; NOTE 1		300		800	ps
tsk(o)	Output Skew; NOTE 2, 3				55	ps
tsk(pp)	Part-to-Part Skew; NOTE 3, 4				250	ps
tjit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section	156.25MHz, Integration Range: 12kHz - 5MHz		0.046	0.065	ps
		156.25MHz, Integration Range: 12kHz - 20MHz		0.083	0.120	ps
		245.76MHz, Integration Range: 12kHz - 5MHz		0.034	0.059	ps
		245.76MHz, Integration Range: 12kHz - 20MHz		0.068	0.094	ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	80		220	ps
odc	Output Duty Cycle		45		55	%
$MUX_{ISOLATION}$	MUX Isolation	@ 100MHz		85		dB

All parameters measured at $f_{OUT} \leq$ 1GHz unless noted otherwise.
NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE 1: Measured from the differential input crossing point to the differential output crossing point.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions.
Measured from the output differential cross points.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 4: Defined as skew between outputs on different devices operating at the same supply voltage, same temperature, same frequency and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.

Table 5B. LVPECL AC Characteristics, $V_{CC} = V_{CC_TAP} = 2.5V \pm 5\%$, $V_{EE} = 0V$, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency				2	GHz
t_{PD}	Propagation Delay, Low-to-High; NOTE 1		300		800	ps
tsk(o)	Output Skew; NOTE 2, 3				55	ps
tsk(pp)	Part-to-Part Skew; NOTE 3, 4				250	ps
tjit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section	156.25MHz, Integration Range: 12kHz - 5MHz		0.054	0.079	ps
		156.25MHz, Integration Range: 12kHz - 20MHz		0.097	0.134	ps
		245.76MHz, Integration Range: 12kHz - 5MHz		0.050	0.067	ps
		245.76MHz, Integration Range: 12kHz - 20MHz		0.099	0.131	ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	80		210	ps
odc	Output Duty Cycle		45		55	%
$MUX_{ISOLATION}$	MUX Isolation	@ 100MHz		85		dB

For NOTES, see Table 5A above.

© 2019 Renesas Electronics Corporation

Table 5C. LVDS AC Characteristics, V_{CC} = 3.3V ± 5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency				2	GHz
t_{PD}	Propagation Delay, Low-to-High; NOTE 1		300		800	ps
tsk(o)	Output Skew; NOTE 2, 3				55	ps
tsk(pp)	Part-to-Part Skew; NOTE 3, 4				250	ps
tjit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section	156.25MHz, Integration Range: 12kHz - 5MHz		0.048	0.074	ps
		156.25MHz, Integration Range: 12kHz - 20MHz		0.096	0.146	ps
		245.76MHz, Integration Range: 12kHz - 5MHz		0.035	0.054	ps
		245.76MHz, Integration Range: 12kHz - 20MHz		0.074	0.097	ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	80		200	ps
odc	Output Duty Cycle		45		55	%
$MUX_{ISOLATION}$	MUX Isolation	@ 100MHz		85		dB

All parameters measured at $f_{OUT} \leq$ 1GHz unless noted otherwise.
NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE 1: Measured from the differential input crossing point to the differential output crossing point.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions.
Measured from the output differential cross points.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 4: Defined as skew between outputs on different devices operating at the same supply voltage, same temperature, same frequency and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.

Table 5D. LVDS AC Characteristics, V_{CC} = V_{CC_TAP} = 2.5V ± 5%, V_{EE} = 0V, T_A = -40°C to 85°C

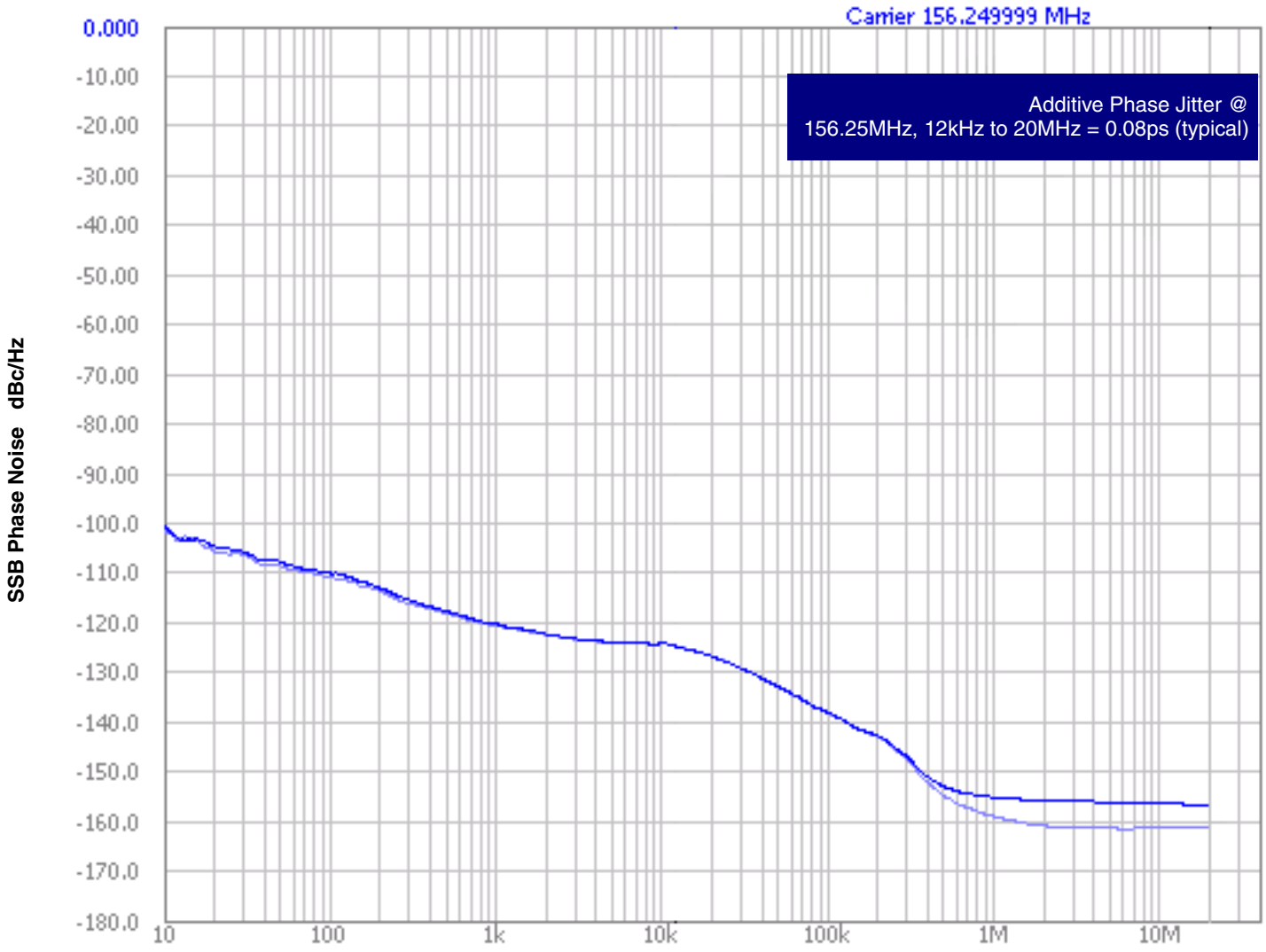
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency				2	GHz
t_{PD}	Propagation Delay, Low-to-High; NOTE 1		300		800	ps
tsk(o)	Output Skew; NOTE 2, 3				55	ps
tsk(pp)	Part-to-Part Skew; NOTE 3, 4				250	ps
tjit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section	156.25MHz, Integration Range: 12kHz - 5MHz		0.049	0.074	ps
		156.25MHz, Integration Range: 12kHz - 20MHz		0.098	0.139	ps
		245.76MHz, Integration Range: 12kHz - 5MHz		0.037	0.060	ps
		245.76MHz, Integration Range: 12kHz - 20MHz		0.076	0.102	ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	80		200	ps
odc	Output Duty Cycle		45		55	%
$MUX_{ISOLATION}$	MUX Isolation	@ 100MHz		85		dB

For NOTES, see Table 5C above.

© 2019 Renesas Electronics Corporation

Additive Phase Jitter

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the ***dBc Phase Noise.*** This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a ***dBc*** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.

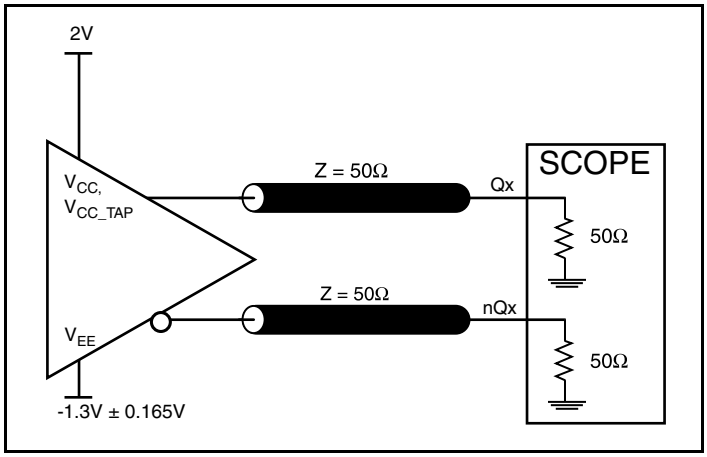


As with most timing specifications, phase noise measurements has issues relating to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This is illustrated above. The device meets the noise floor of what is shown, but can actually be lower. The phase noise is dependent on the input source and measurement equipment.

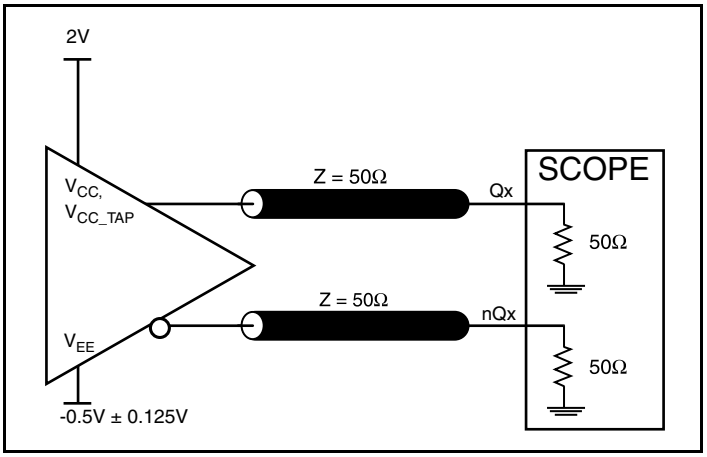
The source generator used is, “Rhode & Schwarz SMA 100A Signal Generator, via the clock synthesis as the external input to drive the input clock.”

© 2019 Renesas Electronics Corporation

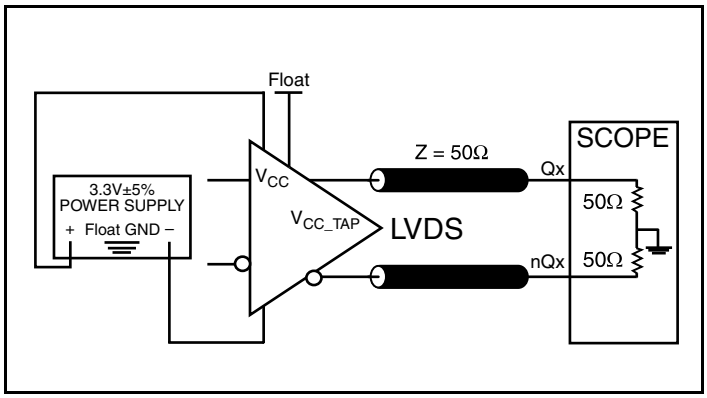
Parameter Measurement Information



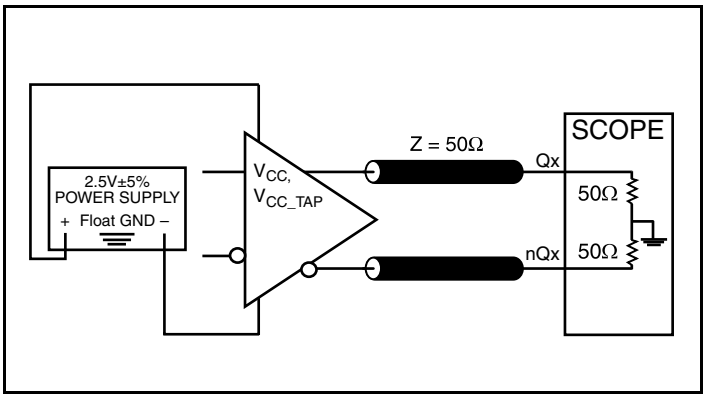
3.3V LVPECL Output Load AC Test Circuit



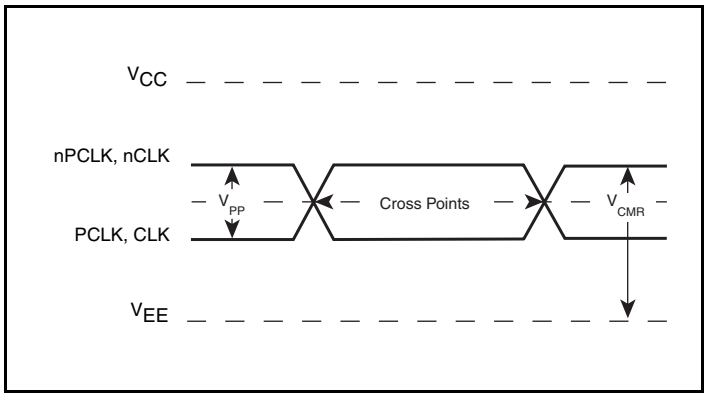
2.5V LVPECL Output Load AC Test Circuit



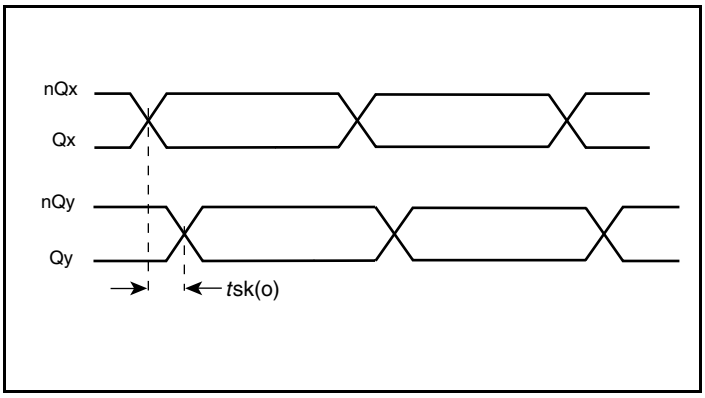
3.3V LVDS Output Load AC Test Circuit



2.5V LVDS Output Load AC Test Circuit



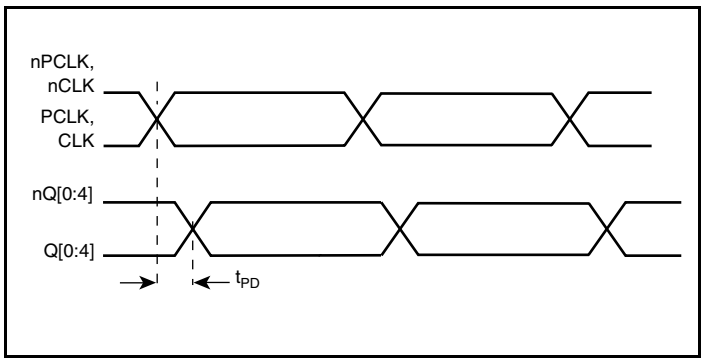
Differential Input Level



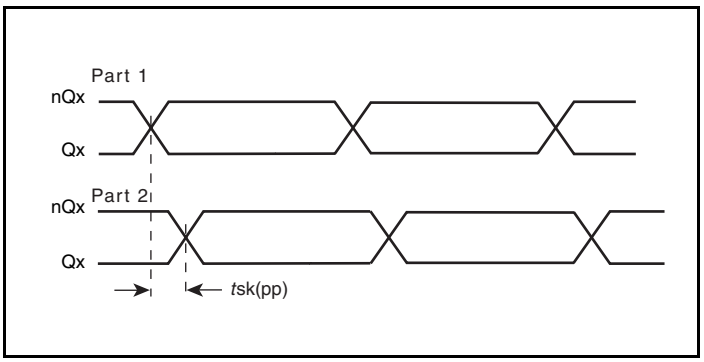
Output Skew

© 2019 Renesas Electronics Corporation

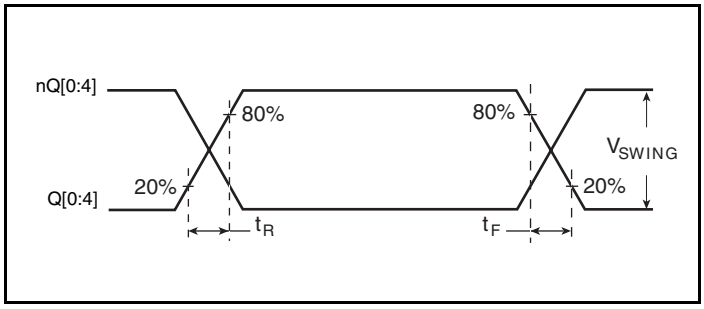
Parameter Measurement Information, continued



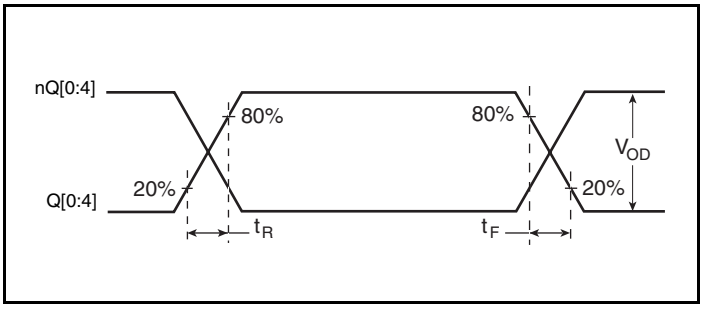
Propagation Delay



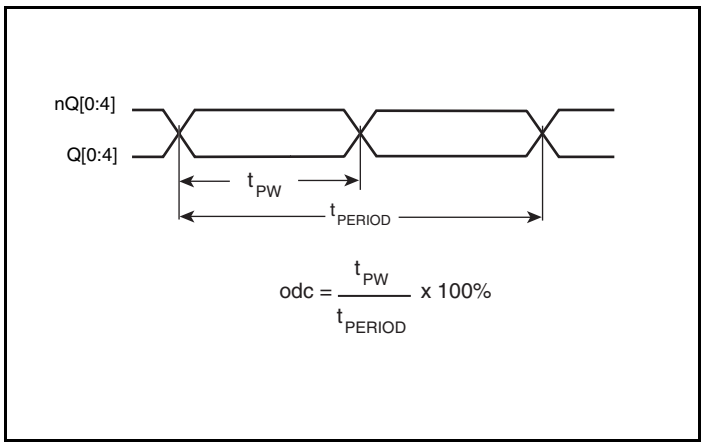
Part-to-Part Skew



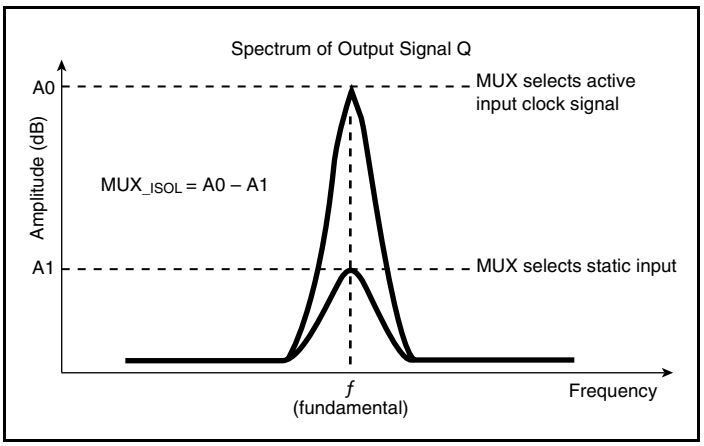
LVPECL Output Rise/Fall Time



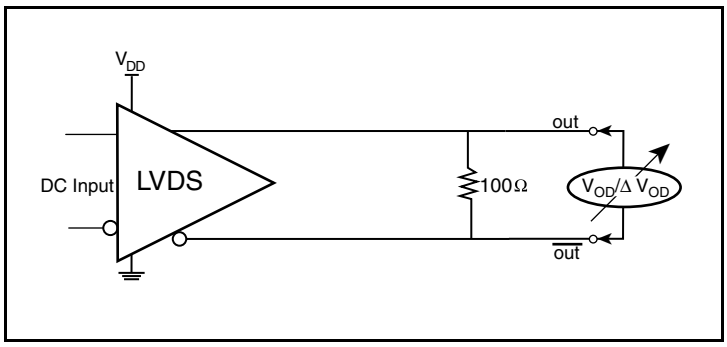
LVDS Output Rise/Fall Time



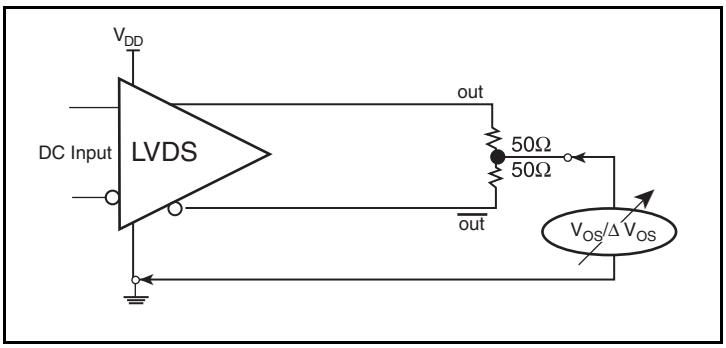
Output Duty Cycle/Pulse Width/Period



MUX Isolation



Differential Output Voltage Setup



Offset Voltage Setup

© 2019 Renesas Electronics Corporation

Applications Information

Recommendations for Unused Input and Output Pins

Inputs:

PCLK/nPCLK Inputs

For applications not requiring the use of a differential input, both the PCLK and nPCLK pins can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from PCLK to ground.

CLK/nCLK Inputs

For applications not requiring the use of a differential input, both the CLK and nCLK pins can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from CLK to ground.

LVCMOS Control Pins

All control pins have internal pulldowns; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs:

LVPECL Outputs

All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

LVDS Outputs

All unused LVDS output pairs can be either left floating or terminated with 100Ω across. If they are left floating, there should be no trace attached.

Wiring the Differential Input to Accept Single-Ended Levels

Figure 2 shows how a differential input can be wired to accept single ended levels. The reference voltage $V_{REF} = V_{CC}/2$ is generated by the bias resistors R1 and R2. The bypass capacitor (C1) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of R1 and R2 might need to be adjusted to position the V_{REF} in the center of the input voltage swing. For example, if the input clock swing is 2.5V and V_{CC} = 3.3V, R1 and R2 value should be adjusted to set V_{REF} at 1.25V. The values below are for when both the single ended swing and V_{CC} are at the same voltage. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways. First, R3 and R4 in parallel should equal the transmission line impedance. For most 50Ω applications, R3 and R4 can be 100Ω. The values of the resistors can be increased to reduce the loading for slower and weaker LVCMOS driver. When using single-ended signaling, the noise rejection benefits of differential signaling are reduced. Even though the differential input can handle full rail LVCMOS signaling, it is recommended that the amplitude be reduced. The datasheet specifies a lower differential amplitude, however this only applies to differential signals. For single-ended applications, the swing can be larger, however V_{IL} cannot be less than -0.3V and V_{IH} cannot be more than V_{CC} + 0.3V. Though some of the recommended components might not be used, the pads should be placed in the layout. They can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a differential signal.

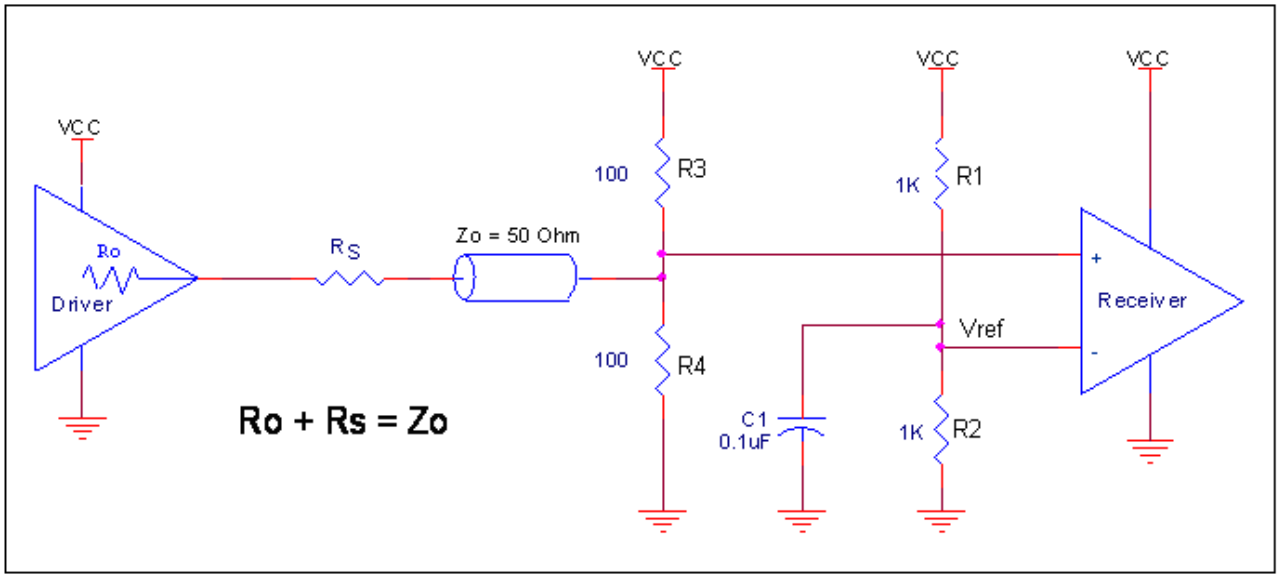


Figure 2. Recommended Schematic for Wiring a Differential Input to Accept Single-ended Levels

© 2019 Renesas Electronics Corporation

3.3V LVPECL Clock Input Interface

The PCLK /nPCLK accepts LVPECL, CML, LVDS and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. *Figures 3A to 3E* show interface examples for the PCLK/nPCLK input driven by the most common driver types.

The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

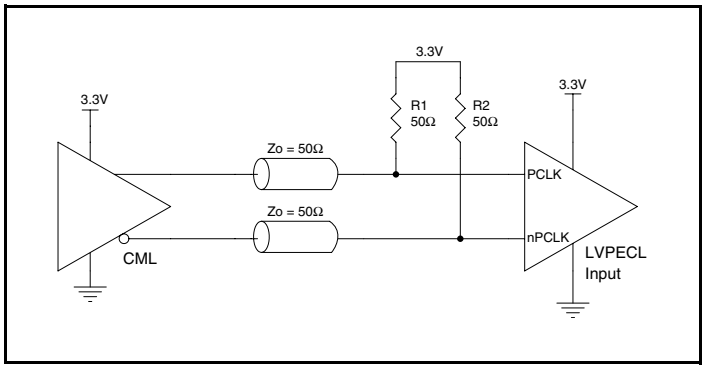


Figure 3A. PCLK/nPCLK Input Driven by an Open Collector CML Driver

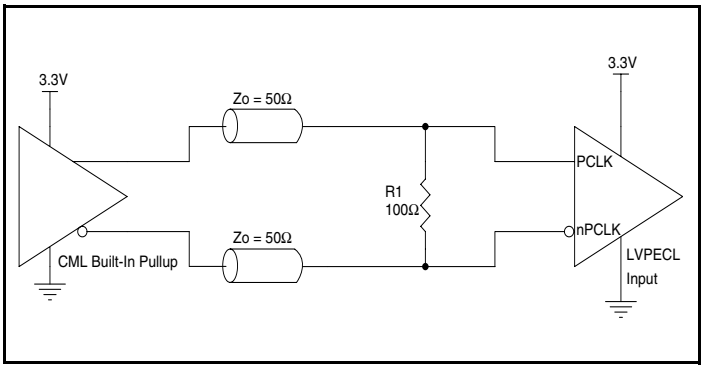


Figure 3B. PCLK/nPCLK Input Driven by a Built-In Pullup CML Driver

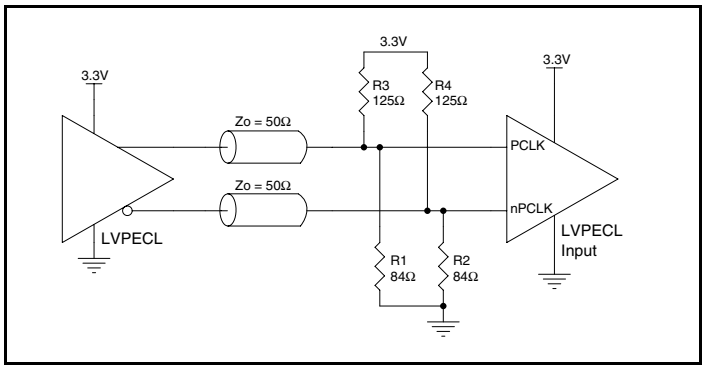


Figure 3C. PCLK/nPCLK Input Driven by a 3.3V LVPECL Driver

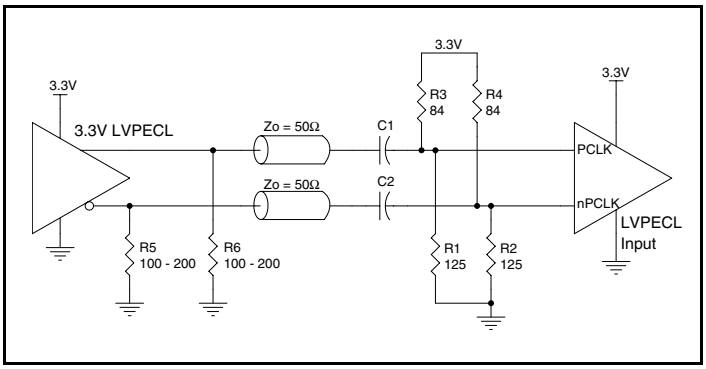


Figure 3D. PCLK/nPCLK Input Driven by a 3.3V LVPECL Driver with AC Couple

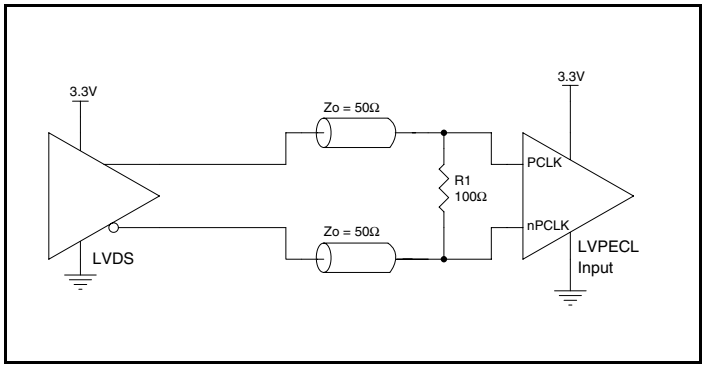


Figure 3E. PCLK/nPCLK Input Driven by a LVDS Driver

© 2019 Renesas Electronics Corporation

2.5V LVPECL Clock Input Interface

The PCLK /nPCLK accepts LVPECL, CML, LVDS and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. *Figures 4A to 4E* show interface examples for the PCLK/nPCLK input driven by the most common driver types.

The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

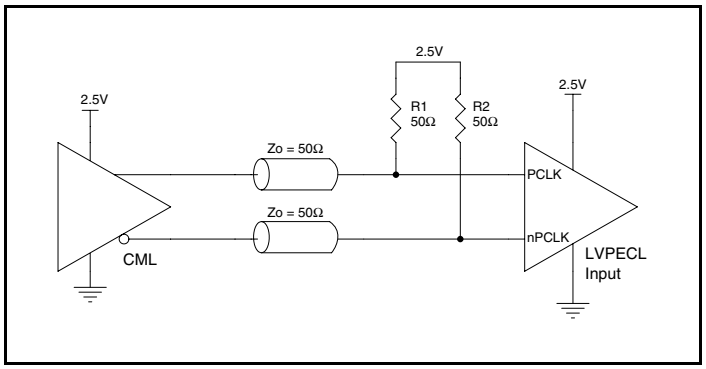


Figure 4A. PCLK/nPCLK Input Driven by an Open Collector CML Driver

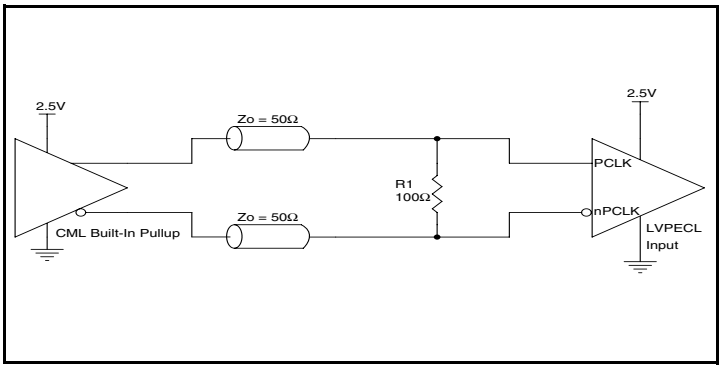


Figure 4B. PCLK/nPCLK Input Driven by a Built-In Pullup CML Driver

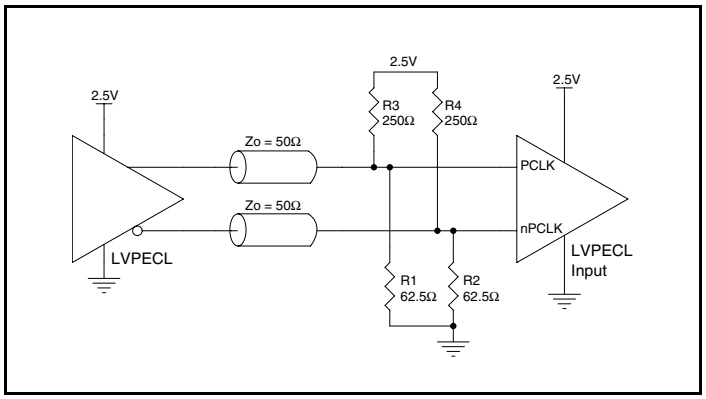


Figure 4C. PCLK/nPCLK Input Driven by a 3.3V LVPECL Driver

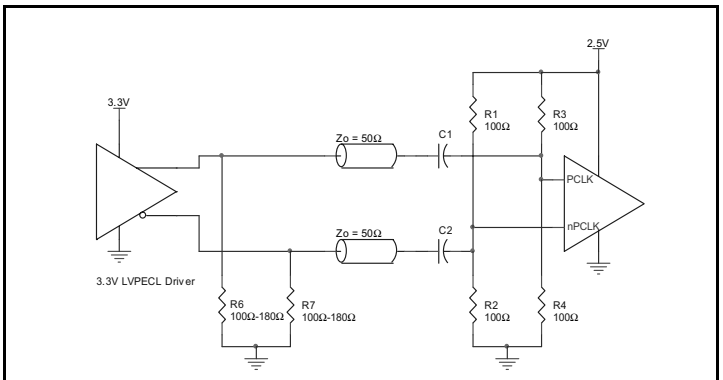


Figure 4D. PCLK/nPCLK Input Driven by a 3.3V LVPECL Driver with AC Couple

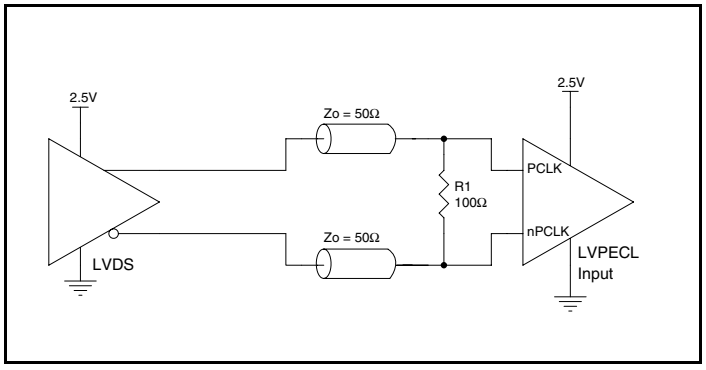


Figure 4E. PCLK/nPCLK Input Driven by a LVDS Driver

© 2019 Renesas Electronics Corporation

3.3V Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, HCSL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. *Figures 5A to 5E* show interface examples for the CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example, in Figure 5A, the input termination applies for IDT open emitter LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

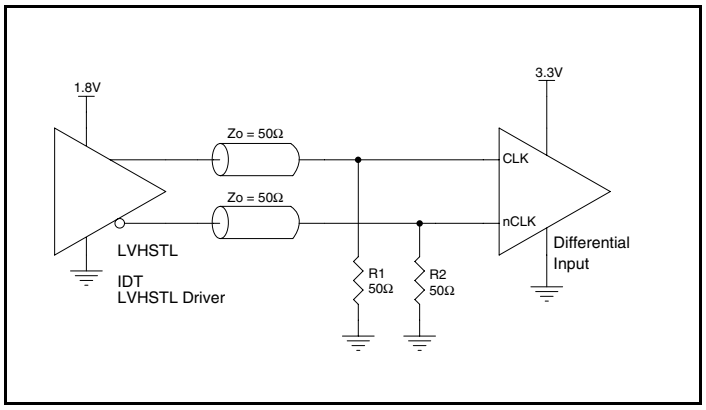


Figure 5A. CLK/nCLK Input Driven by an IDT Open Emitter LVHSTL Driver

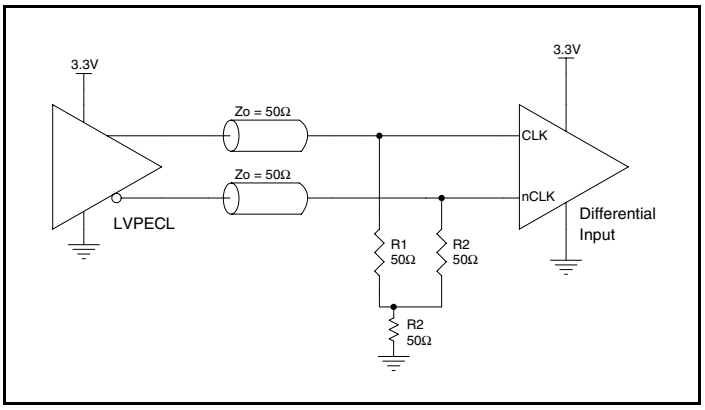


Figure 5B. CLK/nCLK Input Driven by a 3.3V LVPECL Driver

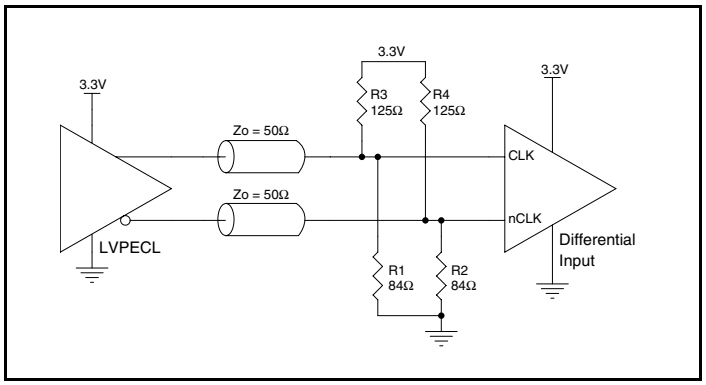


Figure 5C. CLK/nCLK Input Driven by a 3.3V LVPECL Driver

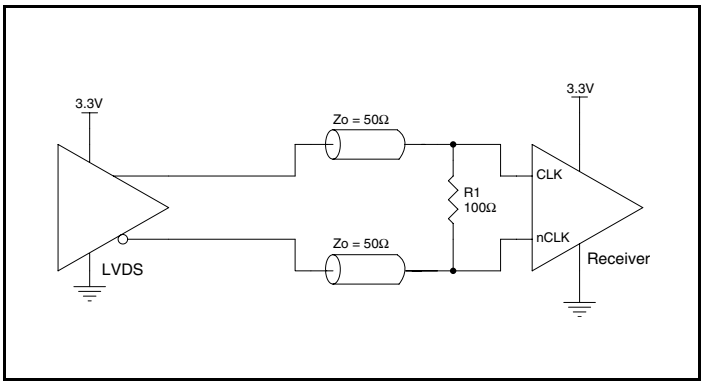


Figure 5D. CLK/nCLK Input Driven by a 3.3V LVDS Driver

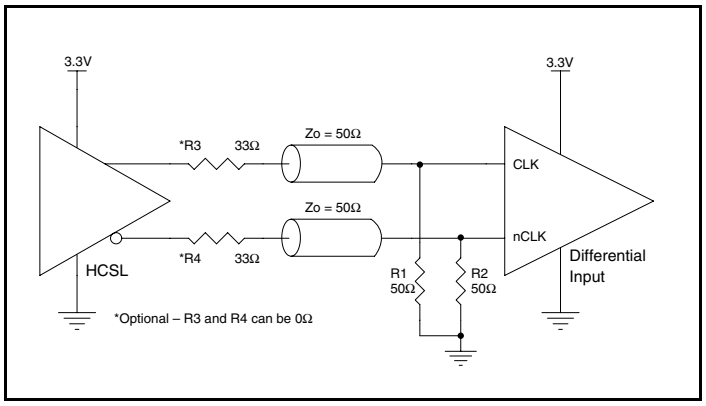


Figure 5E. CLK/nCLK Input Driven by a 3.3V HCSL Driver

© 2019 Renesas Electronics Corporation

2.5V Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, HCSL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. *Figures 6A to 6E* show interface examples for the CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example, in Figure 6A, the input termination applies for IDT open emitter LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

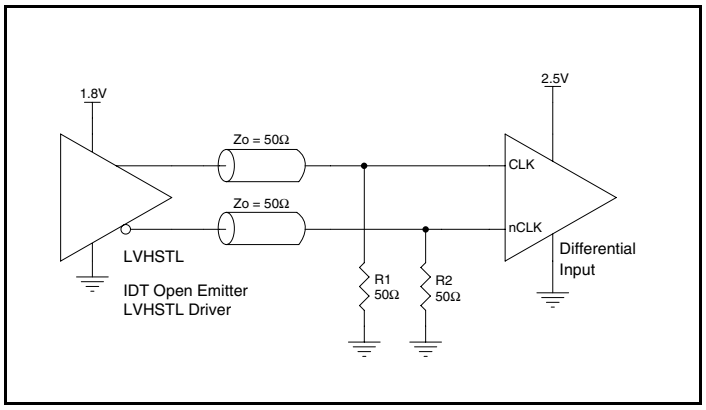


Figure 6A. CLK/nCLK Input Driven by an IDT Open Emitter LVHSTL Driver

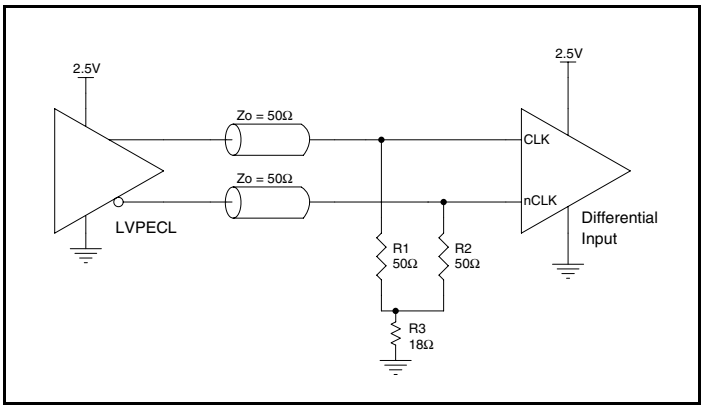


Figure 6B. CLK/nCLK Input Driven by a 2.5V LVPECL Driver

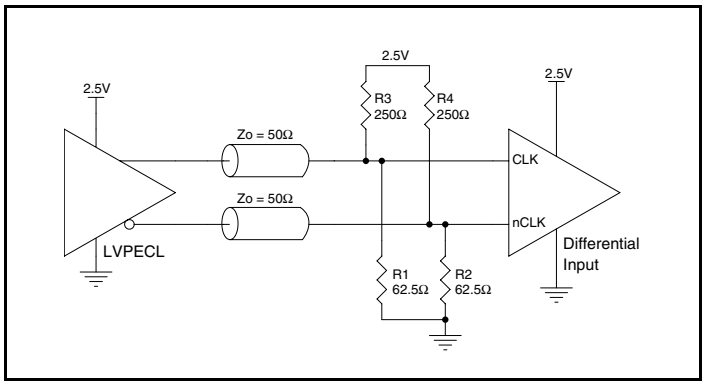


Figure 6C. CLK/nCLK Input Driven by a 2.5V LVPECL Driver

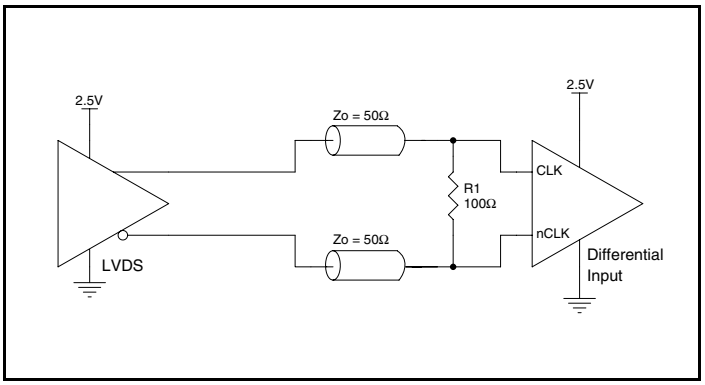


Figure 6D. CLK/nCLK Input Driven by a 2.5V LVDS Driver

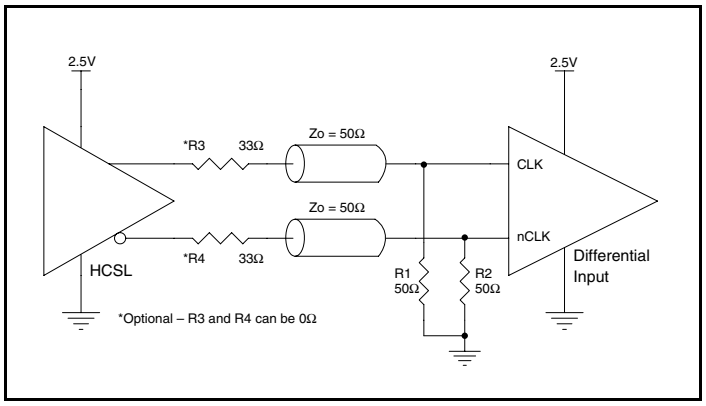


Figure 6E. CLK/nCLK Input Driven by a 2.5V HCSL Driver

© 2019 Renesas Electronics Corporation

LVDS Driver Termination

For a general LVDS interface, the recommended value for the termination impedance (Z_T) is between 90Ω and 132Ω. The actual value should be selected to match the differential impedance (Z_0) of your transmission line. A typical point-to-point LVDS design uses a 100Ω parallel resistor at the receiver and a 100Ω differential transmission-line environment. In order to avoid any transmission-line reflection issues, the components should be surface mounted and must be placed as close to the receiver as possible. IDT offers a full line of LVDS compliant devices with two types of output structures: current source and voltage source. The standard termination schematic as shown in *Figure 7A* can be used with either type of output structure. *Figure 7B*, which can also be used with both output types, is an optional termination with center tap capacitance to help filter common mode noise. The capacitor value should be approximately 50pF. If using a non-standard termination, it is recommended to contact IDT and confirm if the output structure is current source or voltage source type. In addition, since these outputs are LVDS compatible, the input receiver's amplitude and common-mode input range should be verified for compatibility with the output.

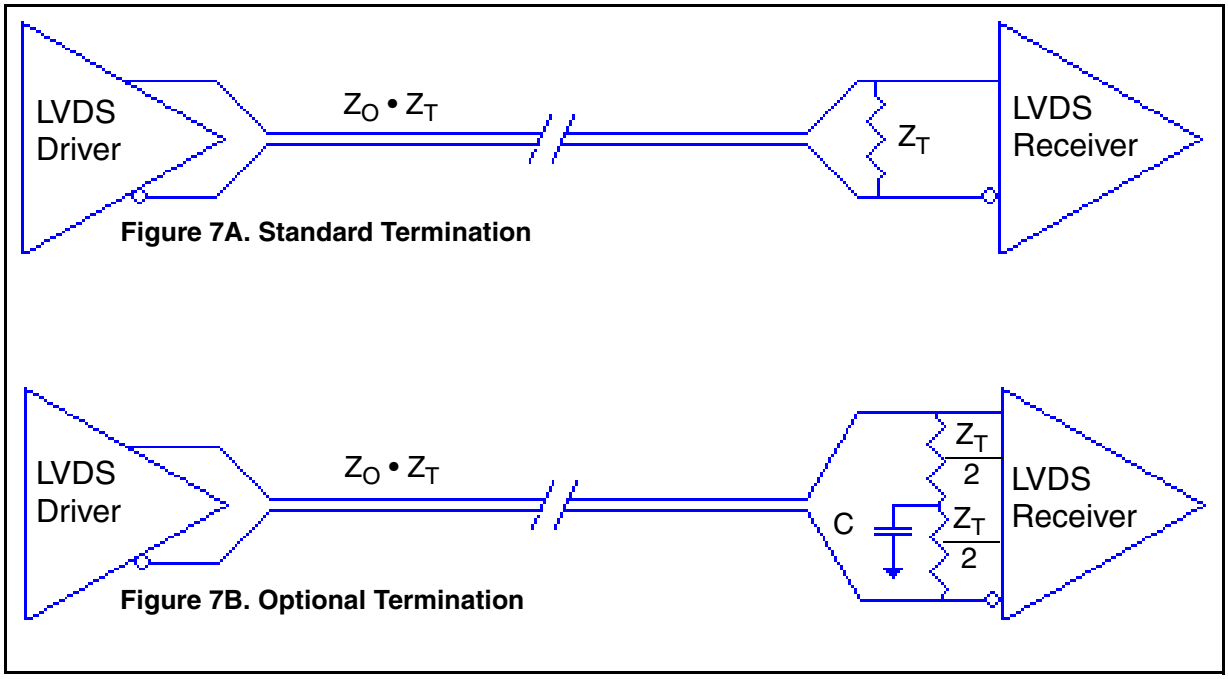


Figure 7A. Standard Termination

Figure 7B. Optional Termination

LVDS Termination

© 2019 Renesas Electronics Corporation

Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

The differential outputs are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 8A and 8B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

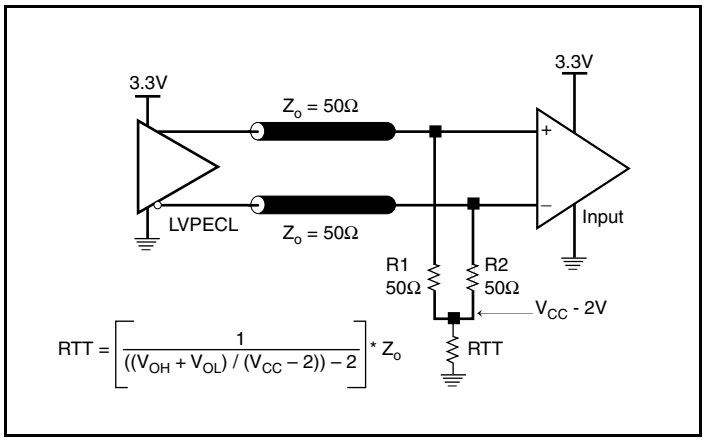


Figure 8A. 3.3V LVPECL Output Termination

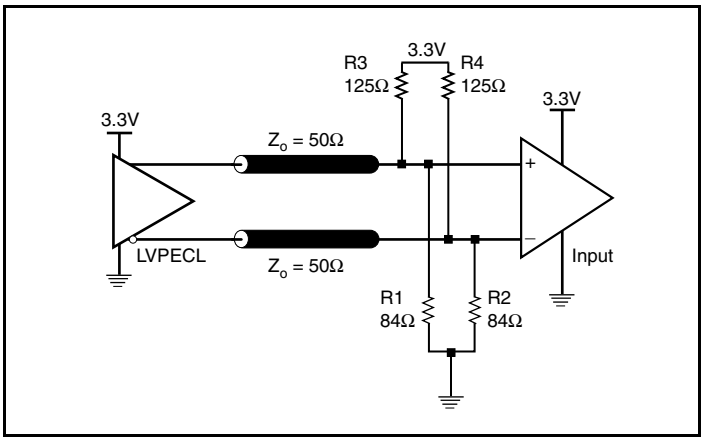


Figure 8B. 3.3V LVPECL Output Termination

© 2019 Renesas Electronics Corporation

Termination for 2.5V LVPECL Outputs

Figure 9A and *Figure 9B* show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to V_{CC} – 2V. For V_{CC} = 2.5V, the V_{CC} – 2V is very close to ground level. The R3 in Figure 9B can be eliminated and the termination is shown in *Figure 9C.*

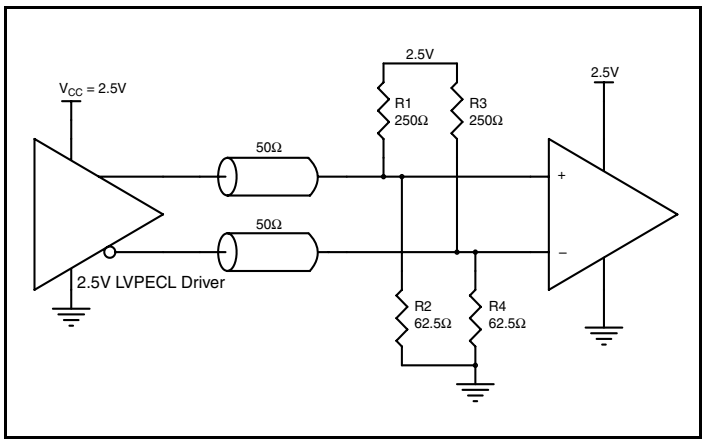


Figure 9A. 2.5V LVPECL Driver Termination Example

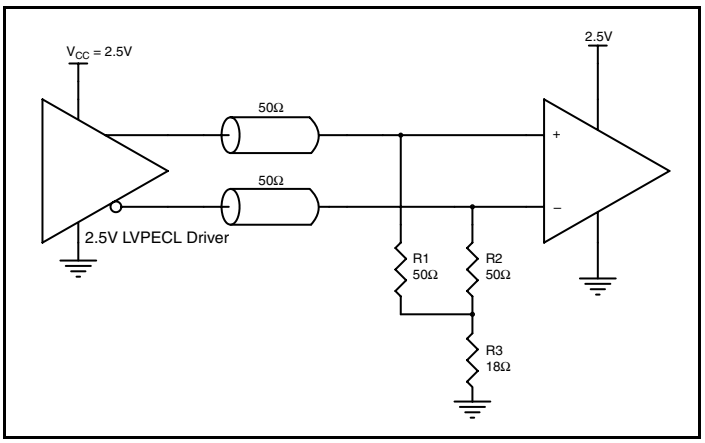


Figure 9B. 2.5V LVPECL Driver Termination Example

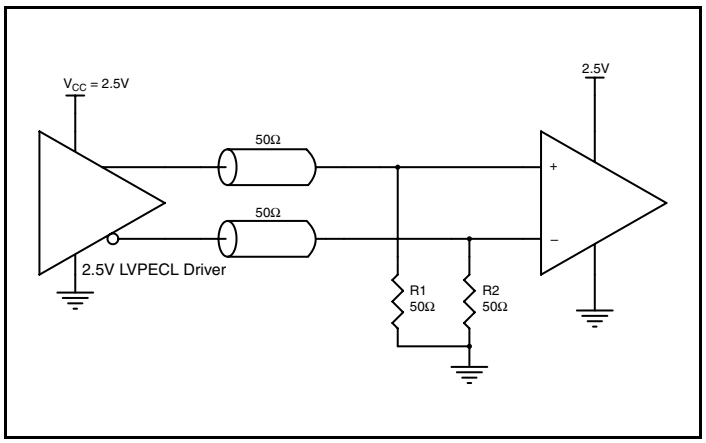


Figure 9C. 2.5V LVPECL Driver Termination Example

© 2019 Renesas Electronics Corporation

VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 10.* The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor’s Thermally/ Electrically Enhance Leadframe Base Package, Amkor Technology.

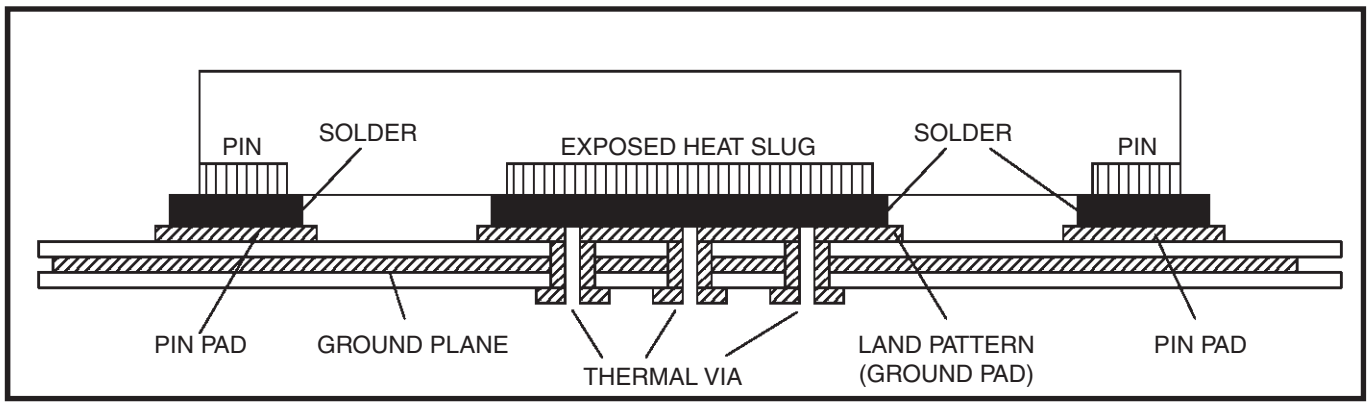


Figure 10. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (drawing not to scale)

© 2019 Renesas Electronics Corporation

LVPECL Power Considerations

This section provides information on power dissipation and junction temperature for the ICS854S015I-01.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS854S015I-01 is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{CC} = 3.3V + 5% = 3.465V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power $(core)_{MAX} = V_{CC_MAX} * I_{EE_MAX}$ = 3.465V * 85mA = **294.53mW**
- Power $(outputs)_{MAX}$ = **30mW/Loaded Output pair**
  If all outputs are loaded, the total power is 5 * 30mW = **150mW**

Total Power$_{_MAX}$ (3.3V, with all outputs switching) = 294.53mW +150mW = **444.55mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 49.5°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.445W * 49.5°C/W = 107°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 6. Thermal Resistance θ_{JA} for 24 Lead VFQFN, Forced Convection

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	49.5°C/W	43.3°C/W	38.8°C/W

© 2019 Renesas Electronics Corporation

3. Calculations and Equations.

The purpose of this section is to calculate the power dissipation for the LVPECL output pair.

LVPECL output driver circuit and termination are shown in *Figure 11.*

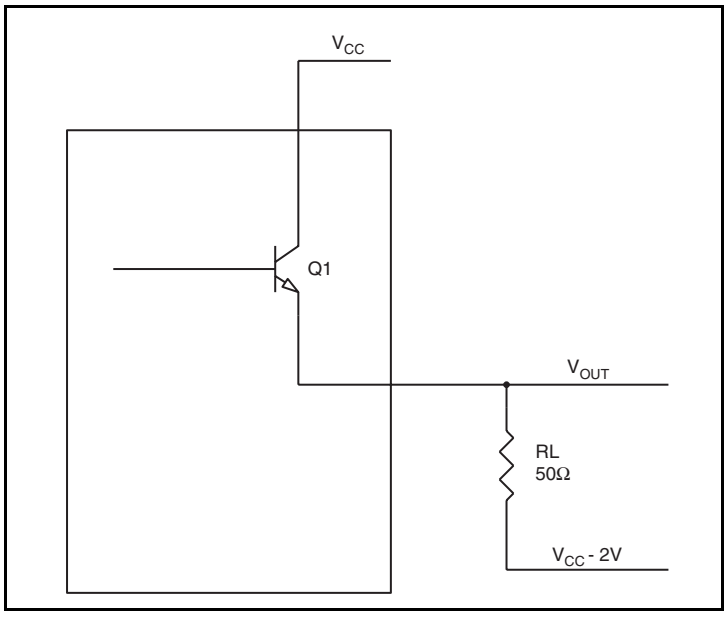


Figure 11. LVPECL Driver Circuit and Termination

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of V_{CC} – 2V.

- For logic high, $V_{OUT} = V_{OH_MAX} = \mathbf{V_{CC_MAX} – 0.9V}$
  $(V_{CC_MAX} – V_{OH_MAX}) = \mathbf{0.9V}$
- For logic low, $V_{OUT} = V_{OL_MAX} = \mathbf{V_{CC_MAX} – 1.7V}$
  $(V_{CC_MAX} – V_{OL_MAX}) = \mathbf{1.7V}$

Pd_H is power dissipation when the output drives high.

Pd_L is the power dissipation when the output drives low.

$Pd_H = [(V_{OH_MAX} – (V_{CC_MAX} – 2V))/R_L] * (V_{CC_MAX} – V_{OH_MAX}) = [(2V – (V_{CC_MAX} – V_{OH_MAX}))/R_L] * (V_{CC_MAX} – V_{OH_MAX}) =$
$[(2V – 0.9V)/50\Omega] * 0.9V =$ **19.8mW**

$Pd_L = [(V_{OL_MAX} – (V_{CC_MAX} – 2V))/R_L] * (V_{CC_MAX} – V_{OL_MAX}) = [(2V – (V_{CC_MAX} – V_{OL_MAX}))/R_{L]} * (V_{CC_MAX} – V_{OL_MAX}) =$
$[(2V – 1.7V)/50\Omega] * 1.7V =$ **10.2mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **30mW**

© 2019 Renesas Electronics Corporation

LVDS Power Considerations

This section provides information on power dissipation and junction temperature for the ICS854S015I-01.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS854S015I-01 is the sum of the core power plus the analog power plus the power dissipated in the load(s). The following is the power dissipation for V_{CC} = 3.3V + 5% = 3.465V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power $(core)_{MAX} = V_{CC_MAX} * I_{CC_MAX}$ = 3.465V * 150mA = **519.75mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 49.5°C/W per Table 7 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.520W * 49.5°C/W = 110.7°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 7. Thermal Resistance θ_{JA} for 24 Lead VFQFN, Forced Convection

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	49.5°C/W	43.3°C/W	38.8°C/W

© 2019 Renesas Electronics Corporation

Reliability Information

Table 8. θ_{JA} vs. Air Flow Table for a 24 Lead VFQFN

θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	49.5°C/W	43.3°C/W	38.8°C/W

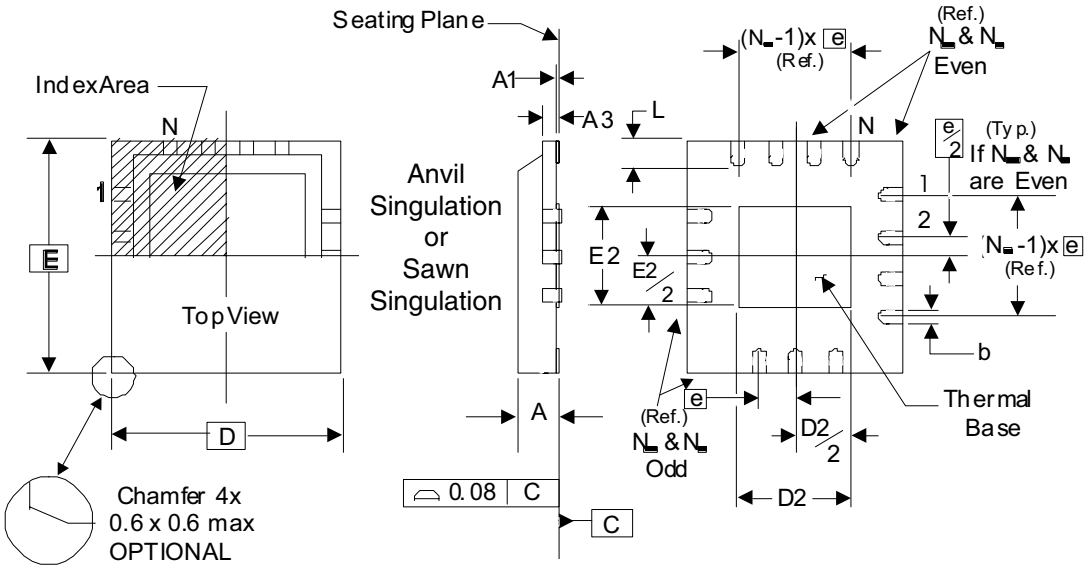
Transistor Count

The transistor count for ICS854S015I-01 is: 521

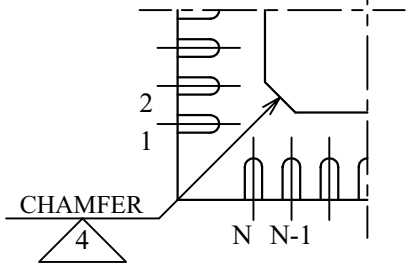
© 2019 Renesas Electronics Corporation

Package Outline and Package Dimensions

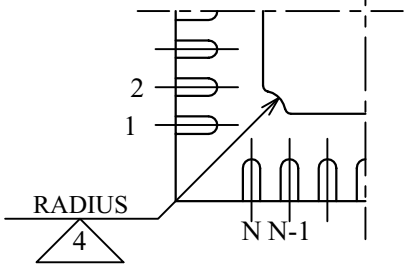
Package Outline - K Suffix for 24 Lead VFQFN



Bottom View w/Type A ID



Bottom View w/Type C ID



There are 2 methods of indicating pin 1 corner at the back of the VFQFN package are:

1. Type A: Chamfer on the paddle (near pin 1)
2. Type C: Mouse bite on the paddle (near pin 1)

Table 9. K Package Dimensions for 24 Lead VFQFN

All Dimensions in Millimeters		
Symbol	**Minimum**	**Maximum**
N	24	
A	0.80	1.0
A1	0	0.05
A3	0.25 Reference	
b	0.18	0.30
e	0.50 Basic	
D, E	4	
D2, E2	2.30	2.55
L	0.30	0.50
N_D N_E	6	

Reference Document: JEDEC Publication 95, MO-220

NOTE: The following package mechanical drawing is a generic drawing that applies to any pin count VFQFN package. This drawing is not intended to convey the actual pin count or pin layout of this device. The pin count and pinout are shown on the front page. The package dimensions are in Table 9.

© 2019 Renesas Electronics Corporation

Ordering Information

Table 10. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
854S015CKI-01LF	15CI01L	“Lead-Free” 24 Lead VFQFN	Tube	-40°C to 85°C
854S015CKI-01LFT	15CI01L	“Lead-Free” 24 Lead VFQFN	2500 Tape & Reel	-40°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

© 2019 Renesas Electronics Corporation