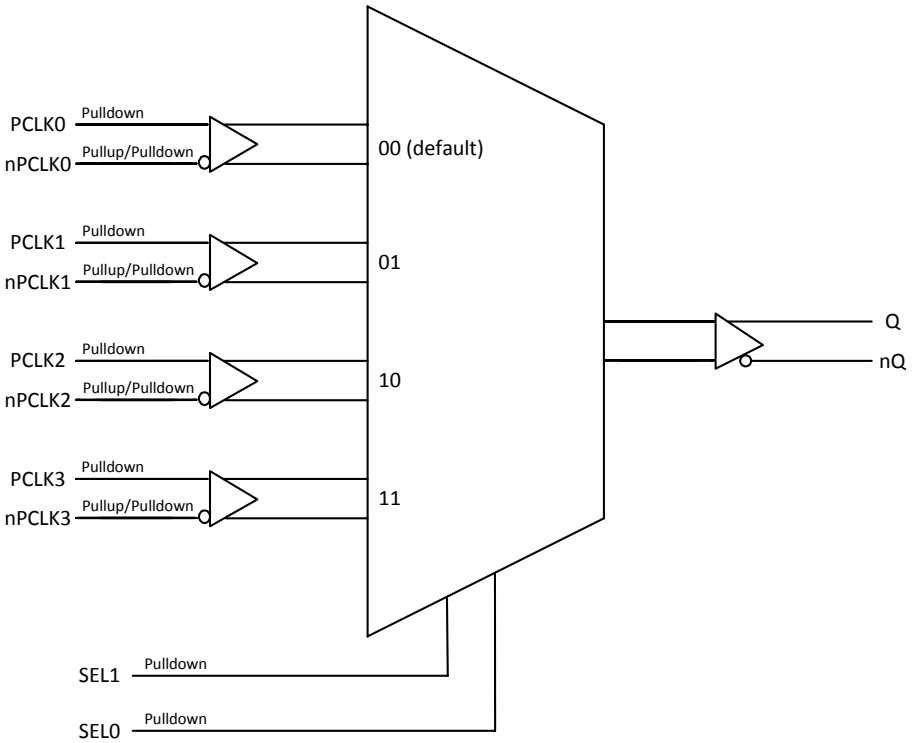
General Description

The ICS854S054I is a 4:1 Differential-to-LVDS Clock Multiplexer which can operate up to 2.5GHz. The ICS854S054I has 4 selectable differential clock inputs. The PCLK, nPCLK input pairs can accept LVPECL, LVDS or CML levels. The fully differential architecture and low propagation delay make it ideal for use in clock distribution circuits. The select pins have internal pulldown resistors. The SEL1 pin is the most significant bit and the binary number applied to the select pins will select the same numbered data input (i.e., 00 selects PCLK0, nPCLK0).

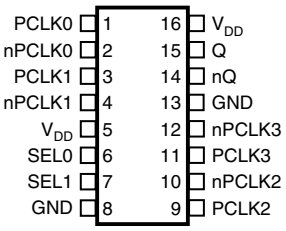
Features

- High speed 4:1 differential multiplexer
- One differential LVDS output pair
- Four selectable differential PCLK, nPCLK input pairs
- PCLKx, nPCLKx pairs can accept the following differential input levels: LVPECL, LVDS, CML
- Maximum output frequency: 2.5GHz
- Translates any single ended input signal to LVDS levels with resistor bias on nPCLKx input
- Additive phase jitter, RMS: 0.147ps (typical)
- Part-to-part skew: 300ps (maximum)
- Propagation delay: 700ps (maximum)
- Supply voltage range: 3.135V to 3.465V
- -40°C to 85°C ambient operating temperature
- Available in lead-free (RoHS 6) package

Block Diagram



Pin Assignment



ICS854S054I
16-Lead TSSOP
5.0mm x 4.4mm x 0.92mm package body
G Package
Top View

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Table 1. Pin Descriptions

Number	Name	Type		Description
1	PCLK0	Input	Pulldown	Non-inverting differential clock input.
2	nPCLK0	Input	Pullup/ Pulldown	Inverting differential clock input. $V_{DD}/2$ default when left floating.
3	PCLK1	Input	Pulldown	Non-inverting differential clock input.
4	nPCLK1	Input	Pullup/ Pulldown	Inverting differential clock input. $V_{DD}/2$ default when left floating.
5, 16	V_{DD}	Power		Positive supply pins.
6, 7	SEL0, SEL1	Input	Pulldown	Clock select input pins. LVCMOS/LVTTL interface levels.
9	PCLK2	Input	Pulldown	Non-inverting differential clock input.
10	nPCLK2	Input	Pullup/ Pulldown	Inverting differential clock input. $V_{DD}/2$ default when left floating.
11	PCLK3	Input	Pulldown	Non-inverting differential clock input.
12	nPCLK3	Input	Pullup/ Pulldown	Inverting differential clock input. $V_{DD}/2$ default when left floating.
8, 13	GND	Power		Power supply ground.
14, 15	nQ, Q	Output		Differential output pair. LVDS interface levels.

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			2		pF
$R_{PULLDOWN}$	Pulldown Resistor			75		kΩ
$R_{VDD}/2$	RPullup/Pulldown Resistor			50		kΩ

Table 3. Clock Input Function Table

Inputs		Outputs	
SEL1	SEL0	Q	nQ
0	0	PCLK0	nPCLK0
0	1	PCLK1	nPCLK1
1	0	PCLK2	nPCLK2
1	1	PCLK3	nPCLK3

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Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5V
Outputs, I_O Continuous Current Surge Current	 10mA 15mA
Package Thermal Impedance, θ_{JA}	100°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, V_{DD} = 3.3V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Positive Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current			57	68	mA

Table 4B. LVCMOS/LVTTL DC Characteristics, V_{DD} = 3.3V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			2.2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage			-0.3		0.8	V
I_{IH}	Input High Current	SEL[1:0]	V_{DD} = V_{IN} = 3.465V			150	µA
I_{IL}	Input Low Current	SEL[1:0]	V_{DD} = 3.465V, V_{IN} = 0V	-10			µA

Table 4C. Differential LVPECL Input DC Characteristics, V_{DD} = 3.3V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	PCLK[0:3], nPCLK[0:3]	V_{DD} = V_{IN} = 3.465V			150	µA
I_{IL}	Input Low Current	PCLK[0:3]	V_{DD} = 3.465V, V_{IN} = 0V	-10			µA
		nPCLK[0:3]	V_{DD} = 3.465V, V_{IN} = 0V	-150			µA
V_{PP}	Peak-to-Peak Voltage			0.15		1.2	V
V_{CMR}	Common Mode Input Voltage; NOTE 1			GND + 1.2		V_{DD}	V

NOTE 1: Common mode input voltage is defined as V_{IH}.

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Table 4D. LVDS DC Characteristics, V_{DD} = 3.3V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage		247	380	454	mV
ΔV_{OD}	V_{OD} Magnitude Change				50	mV
V_{OS}	Offset Voltage		1.125	1.28	1.375	V
ΔV_{OS}	V_{OS} Magnitude Change				50	mV

AC Electrical Characteristics

Table 5. AC Characteristics, V_{DD} = 3.3V ± 5%, T_A = -40°C to 85°C

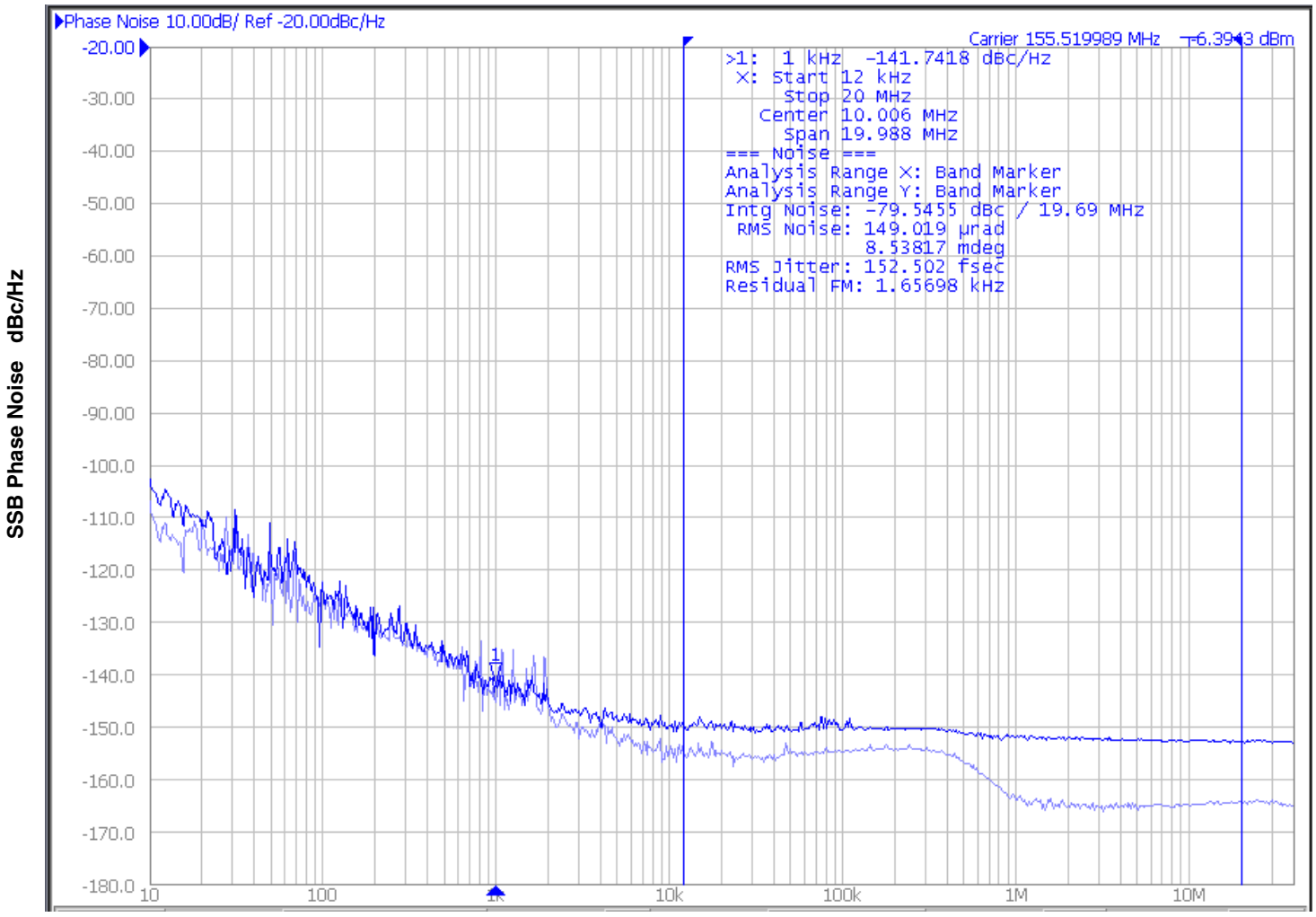
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency				2.5	GHz
t_{PD}	Propagation Delay; NOTE 1		295	470	700	ps
*tj*it(Ø)	Buffer Additive Phase Jitter, RMS; Refer to Additive Phase Jitter Section	155.52MHz, Integration Range: 12kHz – 20MHz		0.147		ps
tsk(pp)	Part-to-Part Skew; NOTE 2, 3				300	ps
tsk(i)	Input Skew			10	50	ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	70	150	250	ps
$MUX_{ISOLATION}$	MUX Isolation; NOTE 4	155.52MHz, V_{PP} = 800mV		86		dB

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
All parameters measured ≤ 1.0GHz unless noted otherwise.
NOTE 1: Measured from the differential input crossing point to the differential output crossing point.
NOTE 2: Defined as skew between outputs on different devices operating at the same supply voltage, same temperature, same frequency and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 4: Q, nQ output measured differentially. See *Parameter Measurement Information* for MUX Isolation diagram.

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Additive Phase Jitter

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the ***dBc Phase Noise.*** This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a ***dBc*** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.

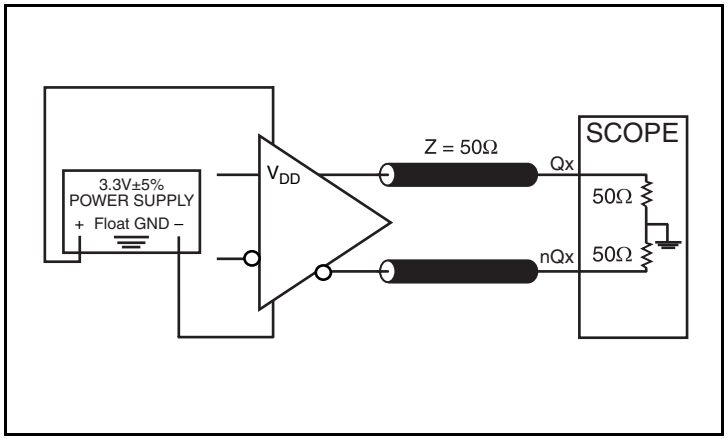


As with most timing specifications, phase noise measurements has issues relating to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This is illustrated above. The device meets the noise floor of what is shown, but can actually be lower. The phase noise is dependent on the input source and measurement equipment.

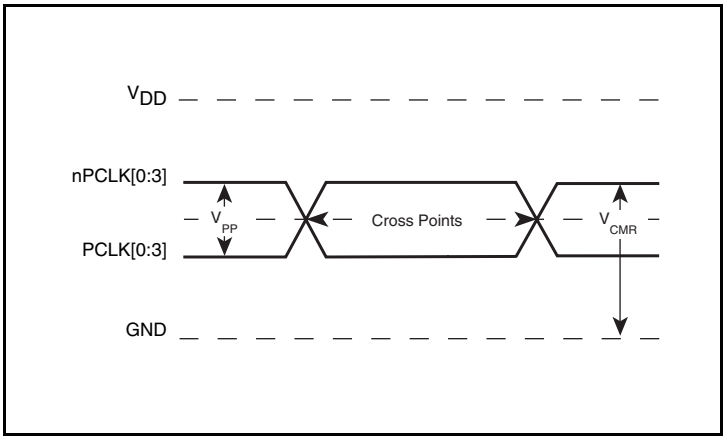
Measured using a Rohde & Schwarz SMA100 as the input source.

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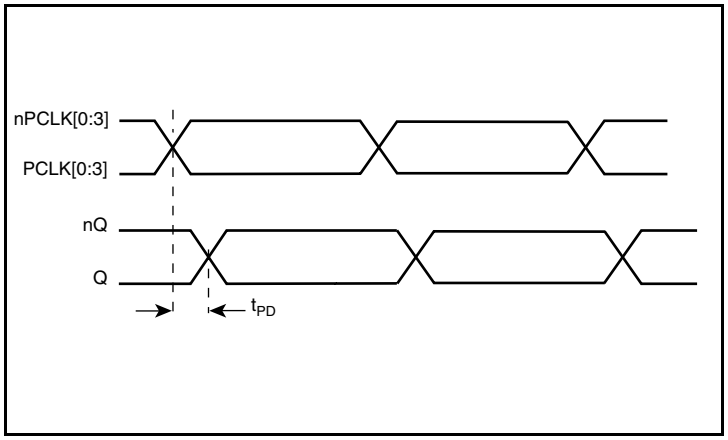
Parameter Measurement Information



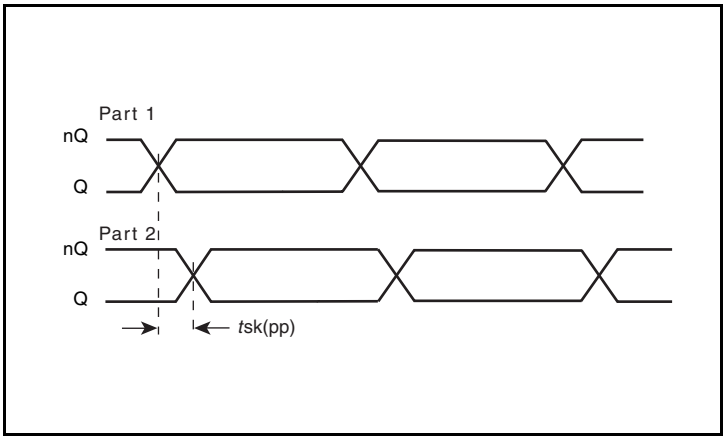
3.3V Output Load AC Test Circuit



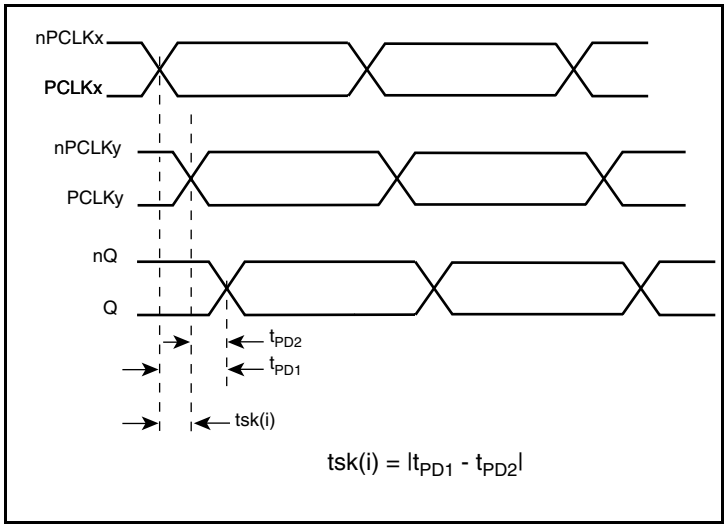
Differential Input Level



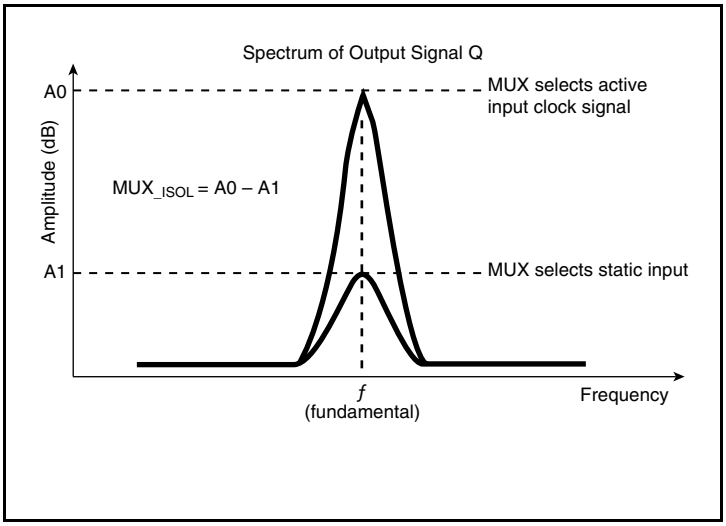
Propagation Delay



Part-to-Part Skew



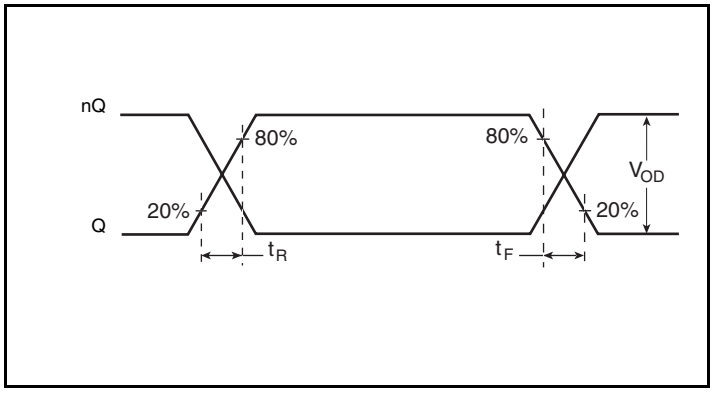
Input Skew



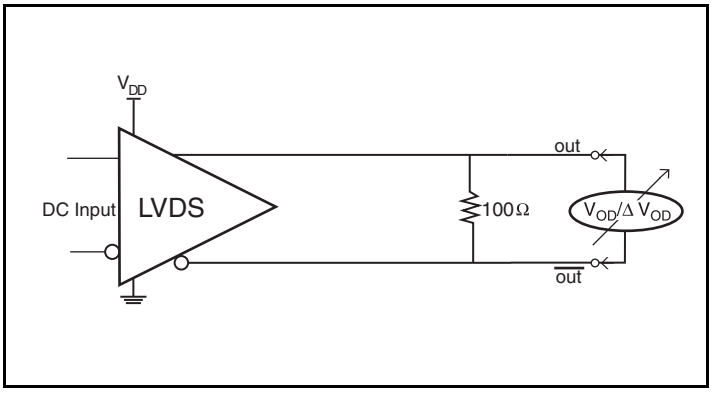
MUX Isolation

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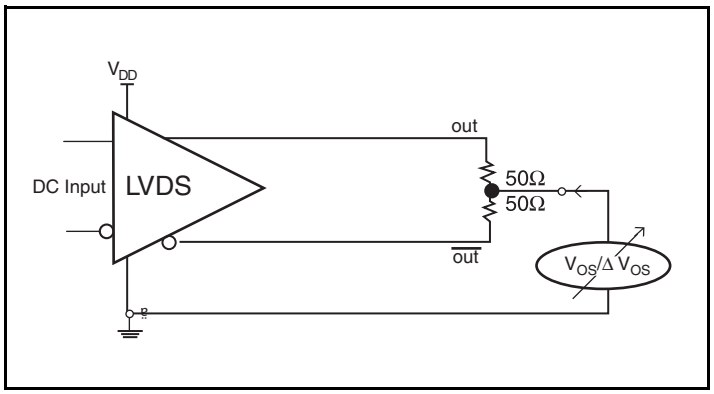
Parameter Measurement Information, continued



Output Rise/Fall Time



Differential Output Voltage Setup



Offset Voltage Setup

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Applications Information

Recommendations for Unused Input Pins

Inputs:

PCLK/nPCLK Inputs

For applications not requiring the use of a differential input, both the PCLK and nPCLK pins can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from PCLK to ground.

Wiring the Differential Input to Accept Single-Ended Levels

Figure 1 shows how a differential input can be wired to accept single ended levels. The reference voltage $V_1 = V_{CC}/2$ is generated by the bias resistors R1 and R2. The bypass capacitor (C1) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of R1 and R2 might need to be adjusted to position the V_1 in the center of the input voltage swing. For example, if the input clock swing is 2.5V and V_{CC} = 3.3V, R1 and R2 value should be adjusted to set V_1 at 1.25V. The values below are for when both the single ended swing and V_{CC} are at the same voltage. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways. First, R3 and R4 in parallel should equal the transmission line impedance. For most 50Ω applications, R3 and R4 can be 100Ω. The values of the resistors can be increased to reduce the loading for slower and weaker LVCMOS driver. When using single-ended signaling, the noise rejection benefits of differential signaling are reduced. Even though the differential input can handle full rail LVCMOS signaling, it is recommended that the amplitude be reduced. The datasheet specifies a lower differential amplitude, however this only applies to differential signals. For single-ended applications, the swing can be larger, however V_{IL} cannot be less than -0.3V and V_{IH} cannot be more than V_{CC} + 0.3V. Though some of the recommended components might not be used, the pads should be placed in the layout. They can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a differential signal.

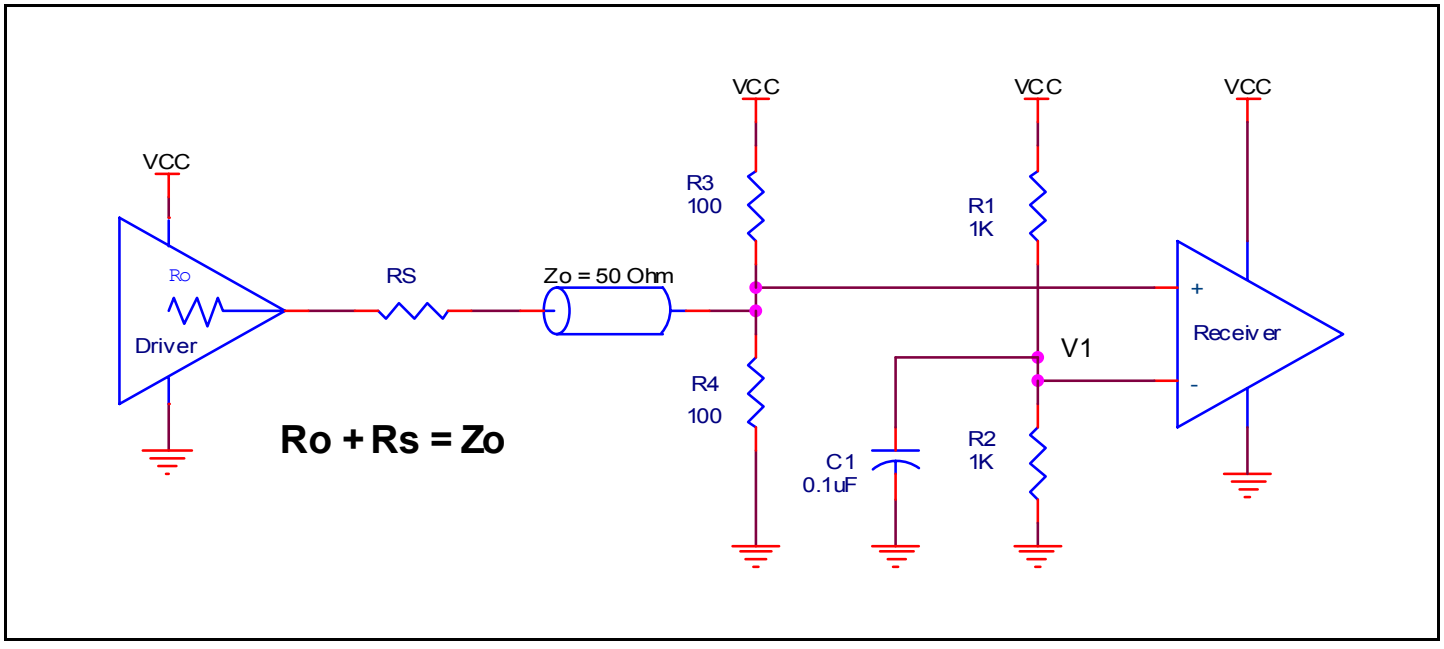


Figure 1. Recommended Schematic for Wiring a Differential Input to Accept Single-ended Levels

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3.3V LVPECL Clock Input Interface

The PCLK /nPCLK accepts LVPECL, LVDS, CML and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. *Figures 2A to 2E* show interface examples for the PCLK/nPCLK input driven by the most common driver types.

The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

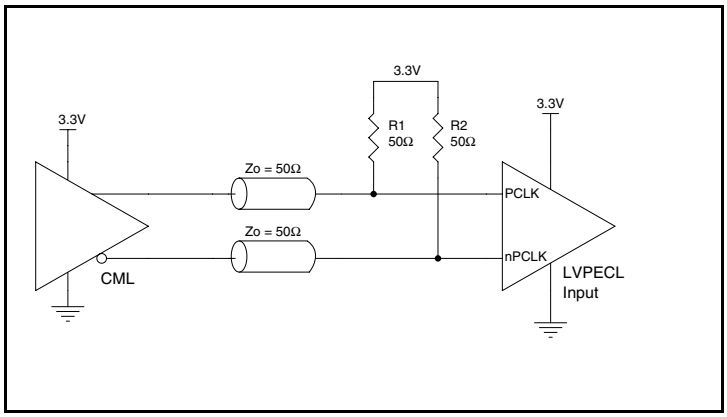


Figure 2A. PCLK/nPCLK Input Driven by a CML Driver

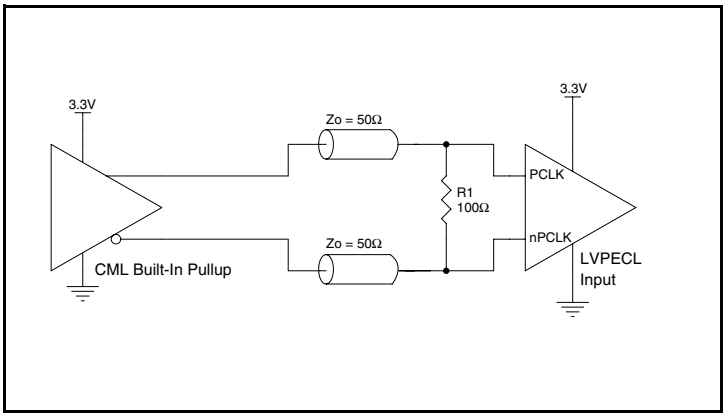


Figure 2B. PCLK/nPCLK Input Driven by a Built-In Pullup CML Driver

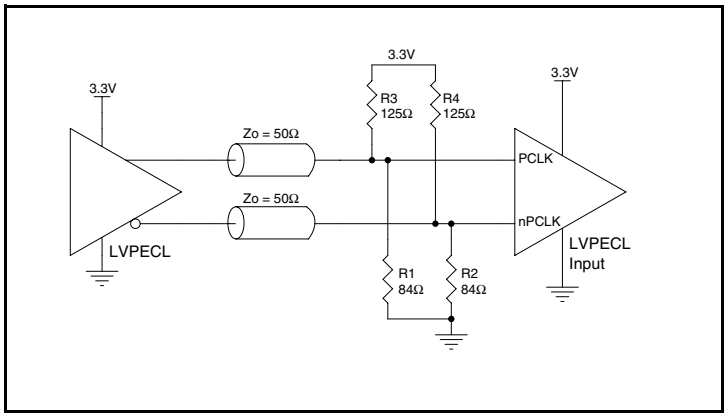


Figure 2C. PCLK/nPCLK Input Driven by a 3.3V LVPECL Driver

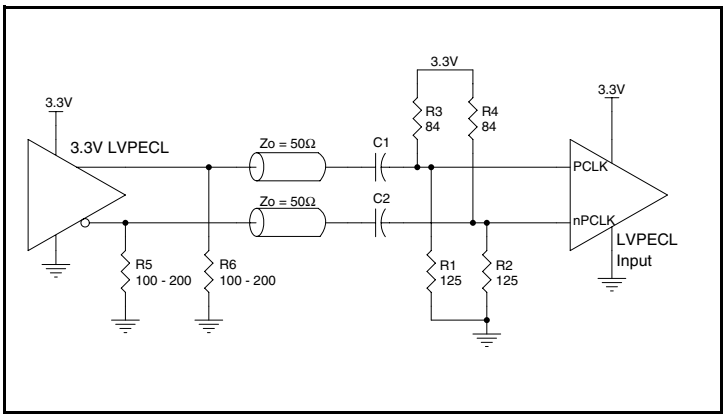


Figure 2D. PCLK/nPCLK Input Driven by a 3.3V LVPECL Driver with AC Couple

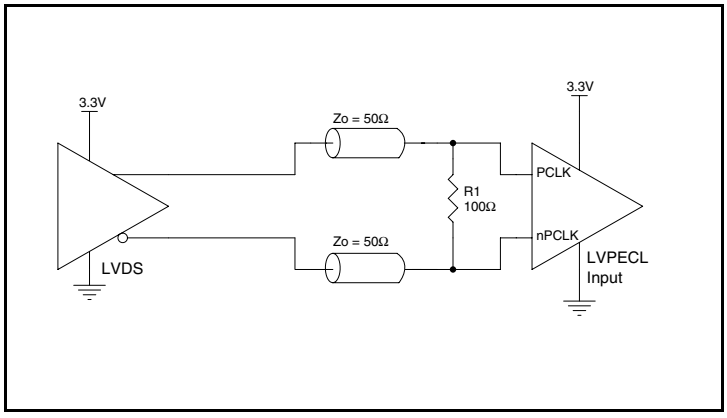


Figure 2E. PCLK/nPCLK Input Driven by a 3.3V LVDS Driver

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LVDS Driver Termination

For a general LVDS interface, the recommended value for the termination impedance (Z_T) is between 90Ω and 132Ω. The actual value should be selected to match the differential impedance (Z_0) of your transmission line. A typical point-to-point LVDS design uses a 100Ω parallel resistor at the receiver and a 100Ω differential transmission-line environment. In order to avoid any transmission-line reflection issues, the components should be surface mounted and must be placed as close to the receiver as possible. IDT offers a full line of LVDS compliant devices with two types of output structures: current source and voltage source. The standard termination schematic as shown in *Figure 3A* can be used with either type of output structure. *Figure 3B*, which can also be used with both output types, is an optional termination with center tap capacitance to help filter common mode noise. The capacitor value should be approximately 50pF. If using a non-standard termination, it is recommended to contact IDT and confirm if the output structure is current source or voltage source type. In addition, since these outputs are LVDS compatible, the input receiver's amplitude and common-mode input range should be verified for compatibility with the output.

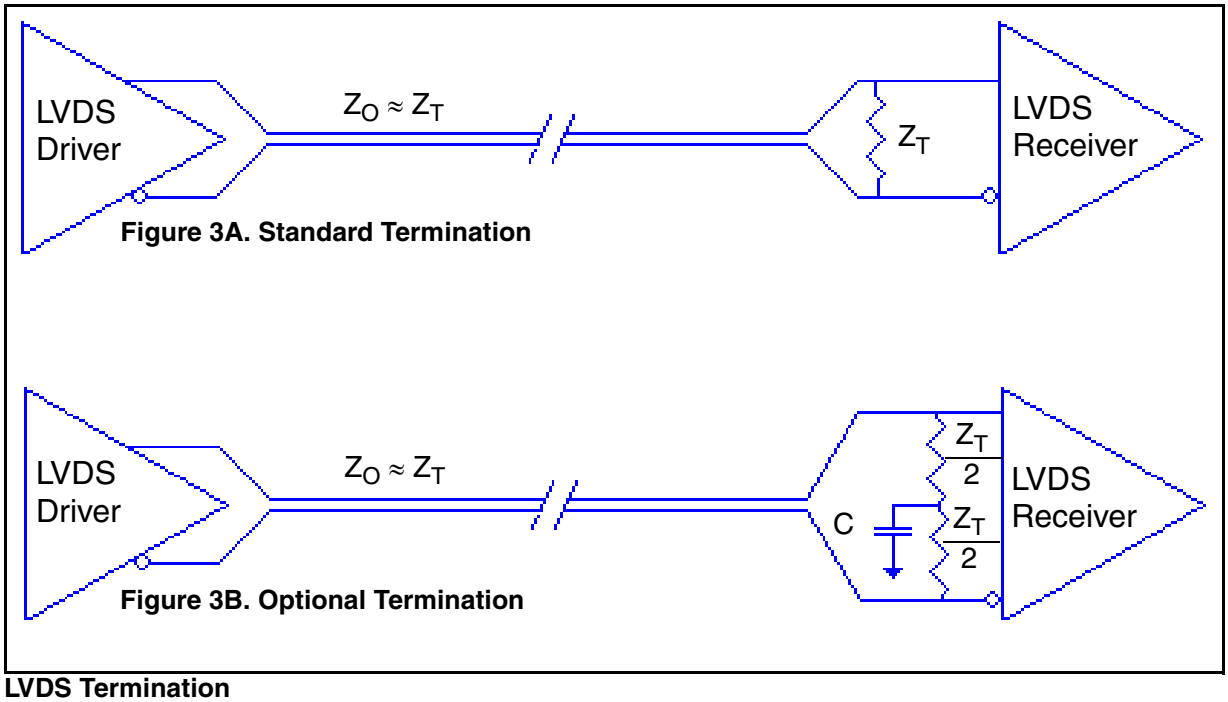


Figure 3A. Standard Termination

Figure 3B. Optional Termination

LVDS Termination

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LVDS Power Considerations

This section provides information on power dissipation and junction temperature for the ICS854S054I.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS854S054I is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{DD} = 3.3V + 5% = 3.465V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power $(core)_{MAX} = V_{DD_MAX} * I_{DD_MAX}$ = 3.465V * 68mA = **235.62mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 100°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.236W * 100°C/W = 108.6°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 6. Thermal Resistance θ_{JA} for 16 Lead TSSOP, Forced Convection

θ_{JA} **by Velocity**			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	100°C/W	94.2°C/W	90.2°C/W

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Reliability Information

Table 7. θ_{JA} vs. Air Flow Table for a 16 Lead TSSOP

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	100°C/W	94.2°C/W	90.2°C/W

Transistor Count

The transistor count for ICS854S054I is: 450

This device is pin and function compatible, and a suggested replacement for ICS854054I.

Package Outline and Package Dimensions

Package Outline - G Suffix for 16 Lead TSSOP

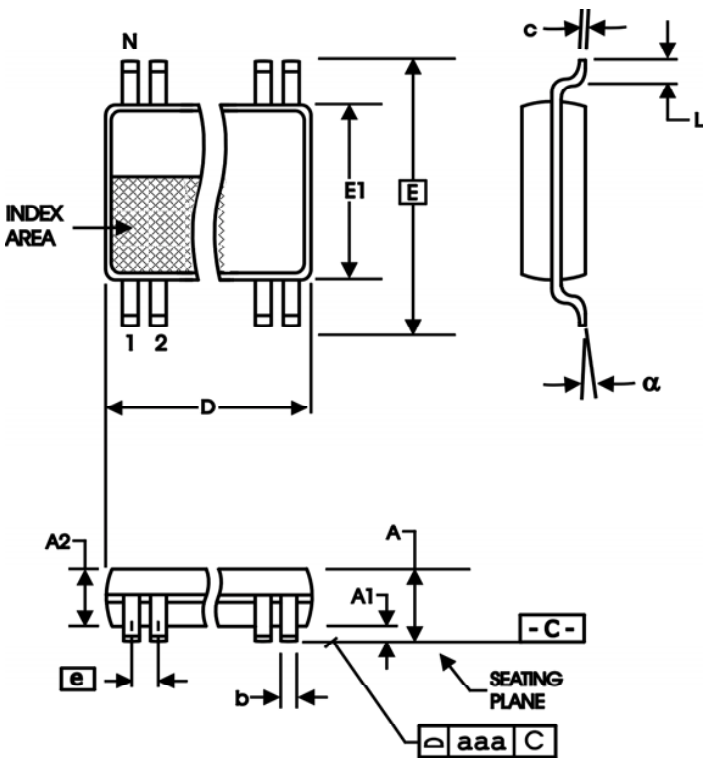


Table 8. Package Dimensions

All Dimensions in Millimeters		
Symbol	**Minimum**	**Maximum**
N	16	
A		1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	4.90	5.10
E	6.40 Basic	
E1	4.30	4.50
e	0.65 Basic	
L	0.45	0.75
α	0°	8°
aaa		0.10

Reference Document: JEDEC Publication 95, MO-153

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Ordering Information

Table 9. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
854S054AGILF	4S054AIL	“Lead-Free” 16 Lead TSSOP	Tube	-40°C to 85°C
854S054AGILFT	4S054AIL	“Lead-Free” 16 Lead TSSOP	Tape & Reel	-40°C to 85°C

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