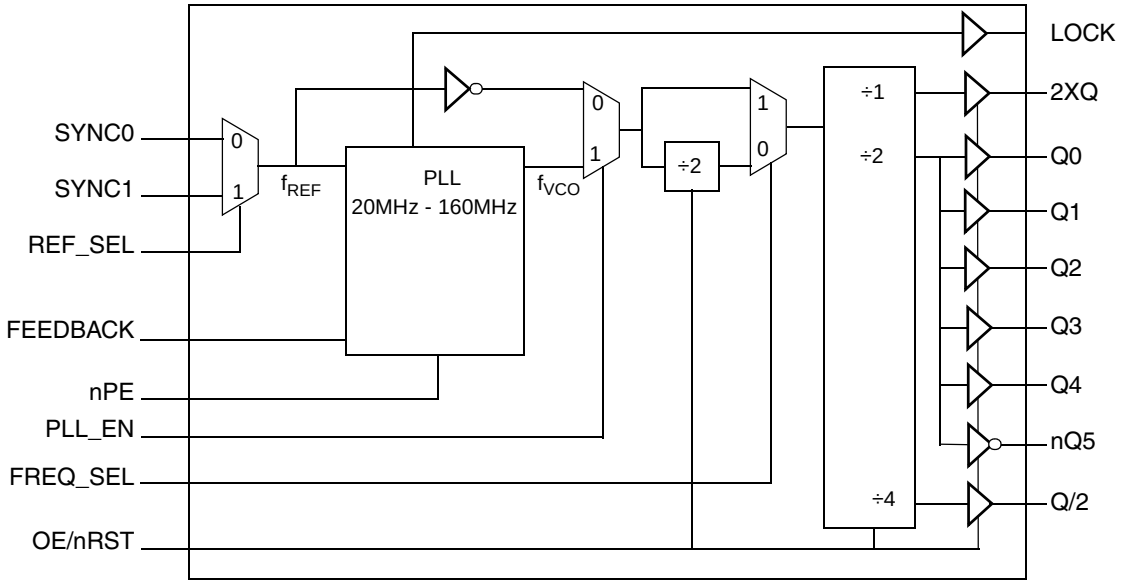
General Description

The 870919I-01 is an LVCMOS clock generator that uses an internal phase lock loop (PLL) for frequency multiplication and to lock the low-skew outputs to the selected reference clock. The device offers eight outputs. The PLL loop filter is completely internal and does not require external components. Several output configurations of the PLL feedback and a divide-by-2 (controlled by FREQ_SEL) allow applications to optimize frequency generation over a wide range of input reference frequencies. The PLL can also be disabled by the PLL_EN control signal to allow for low frequency or DC testing. The LOCK output asserts to indicate when phase-lock has been achieved. The 870919I-01 device is a member of the family of high performance clock solutions from IDT.

Features

- Two selectable single-ended input reference clocks
- Eight single-ended clock outputs
- Internal PLL does not require external loop filter components
- 5V tolerant inputs
- Maximum output frequency: 160MHz, (2XQ output)
- Maximum output frequency: 80MHz, (Q0:Q4 and nQ5 outputs)
- LVCMOS interface levels for all inputs and outputs
- PLL disable feature for low-frequency testing
- PLL lock output
- Selectable synchronization of output to input edge
- Output drive capability: ±24mA
- Output skew: 300ps (maximum), Q0:Q4
- Output skew: 500ps (maximum), all outputs
- Full 3.3V supply voltage
- Available in lead-free packages
- -40°C to 85°C ambient operating temperature
- Fully pin and function compatible with the IDT QS5LV919 (including 55, 70, 100, 133 and 160MHz options)
- For functional replacement part use 8T49N285

Block Diagram



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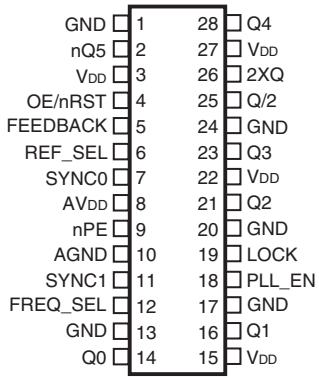
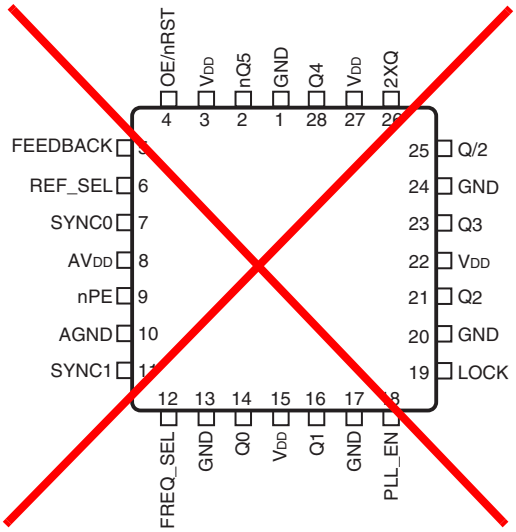
Pin Assignments



870919I-01
28-Lead QSOP, 150Mil
3.9mm x 9.9mm x 1.5mm package body
R Package
Top View



870919I-01
28-Lead PLCC
11.5mm x 11.5mm x 4.4mm package body
V Package
Top View

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Table 1. Pin Descriptions

Number	Name	Type		Description
1, 13, 17, 20, 24	GND	Power		Power supply ground.
2	nQ5	Output		Single-ended clock output (phase is inverted with respect to other outputs). LVCMOS/LVTTL interface levels
3, 15, 22, 27	V_{DD}	Power		Positive power supply pins.
4	OE/nRST	Input		Output enable and asynchronous reset. Resets all outputs. Logic LOW, the outputs are in a high impedance state. Logic HIGH enables all outputs. Internally a Power On reset circuit will ensure that the nQ5 output is inverted relative to Q[4:0]. If OE/nRST is pulsed low, it must be held low for a minimum of 10 ns for a complete reset operation. This reset may be applied asynchronously to the input reference.
5	FEEDBACK	Input		PLL feedback input which is connected to one of the clock outputs to close the PLL feedback loop. LVCMOS/LVTTL interface levels.
6	REF_SEL	Input		Input reference clock select. Logic LOW selects the SYNC0. Logic HIGH selects the SYNC1 input as the PLL reference input. LVCMOS/LVTTL interface levels.
7, 11	SYNC0, SYNC1	Input		Single-ended reference clock inputs. LVCMOS/LVTTL interface levels.
8	AVDD	Power		Positive power supply for the PLL.
9	nPE	Input	Pulldown	Output phase synchronization. In PLL mode (PLL_EN = HIGH) and when logic LOW, the rising edges of the outputs (2XQ, Q0:Q4, Q/2) are synchronized to the rising edge of the selected reference clock (SYNCn). In PLL mode (PLL_EN = HIGH) and when logic HIGH, the falling edges of the outputs (2XQ, Q0:Q4, Q/2) are synchronized to the falling edge of the selected reference clock (SYNCn). LVCMOS/LVTTL interface levels.
10	AGND	Power		Power supply ground for the PLL. Internally connected to GND.
12	FREQ_SEL	Input		Frequency select. Logic LOW level inserts a divide-by-2 into the PLL output and feedback path. Logic HIGH inserts a divide-by-1 into the PLL output and feedback path. LVCMOS/LVTTL interface levels.
14, 16, 21, 23, 28	Q0, Q1, Q2, Q3, Q4	Output		Single-ended clock outputs. LVCMOS/LVTTL interface levels.
18	PLL_EN	Input		PLL enable. Enable and disables the PLL. Logic HIGH enables the PLL. Logic LOW disables the PLL and the input reference signal is routed to the output dividers (PLL bypass). LVCMOS/LVTTL interface levels.
19	LOCK	Output		PLL lock indication output. Logic HIGH indicates PLL lock. Logic LOW indicates PLL is not locked. LVCMOS/LVTTL interface levels.
25	Q/2	Output		Single-ended clock output. LVCMOS/LVTTL interface levels.
26	2XQ	Output		Single-ended clock output. LVCMOS/LVTTL interface levels.

NOTE: *Pulldown* refers to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

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Table 2. Pin Characteristics

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance				4		pF
C_{PD}	Power Dissipation Capacitance (total)		V_{DD} = AV_{DD} = 3.6V		330		pF
$R_{PULLDOWN}$	Input Pulldown Resistor	nPE			56		kΩ
R_{OUT}	Output Impedance				11		Ω

Device Configuration

The 870919I-01 requires a connection of one of the clock outputs to the FEEDBACK input to close the PLL feedback path. The selection of the output (output divider) for PLL feedback will impact the device configuration and input to output frequency ratio and frequency ranges. See Table 3G for details.

Function Tables

Table 3A. OE/nRST Mode Configuration Table

Input	
OE/nRST	**Operation**
0	Device is reset and the outputs Q0:Q4, nQ5, 2XQ, Q/2 are in high-impedance state. This control is asynchronous.
1	Outputs are enabled.

Table 3B. REF_SEL Mode Configuration Table

Input	
REF_SEL	**Operation**
0	SYNC0 is the selected PLL reference clock.
1	SYNC1 is the selected PLL reference clock.

Table 3C. nPE Mode Configuration Table

Input	
nPE	**Operation**
0	The rising edge of the 2XQ, Q0:Q4 and Q/2 outputs and the falling edge of the nQ5 output are synchronized.
1	The falling edge of the 2XQ, Q0:Q4 and Q/2 outputs and the rising edge of the nQ5 output are synchronized.

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Table 3D. FREQ_SEL Mode Configuration Table

Input	
FREQ_SEL	**Operation**
0	The VCO output is frequency-divided by 2. This setting allows for a lower input frequency range. See also table 3G for available frequency ranges.
1	The VCO output is frequency-divided by 1. This setting allows for a higher input frequency range. See also table 3G for available frequency ranges.

Table 3E. PLL_EN Mode Configuration Table

Input	
PLL_EN	**Operation**
0	The PLL is bypassed. The selected input reference clock is routed to the output dividers for low-frequency board test purpose. The PLL-related AC specifications do not apply in PLL bypass mode.
1	The PLL is enabled and locks to the selected input reference signal.

Table 3F. LOCK Mode Configuration Table

Output	
LOCK	**Operation**
0	PLL is not locked to the selected input reference clock.
1	PLL is locked to the selected input reference clock.

Table 3G. Frequency Configuration Table

Outputs Used for PLL Feedback	FREQ_SEL	Input Frequency Range (MHz)	Output Frequency Range (MHz) and Output-to-Input Frequency Multiplication Factor		
		SYNC[0:1]	Q[0:4], nQ5[NOTE1]	2XQ	Q/2
Q0, Q1, Q2, Q3, Q4 or nQ5	0	5 - 40	5 - 40 (1x)	10 - 80 (2x)	2.5 - 20 (0.5x)
	1	10 - 80	10 - 80 (1x)	20 - 160 (2x)	5 - 40 (0.5x)
2XQ	0	10 - 80	5 - 40 (0.5x)	10 - 80 (1x)	2.5 - 20 (0.25x)
	1	20 - 100[NOTE2]	10 - 50 (0.5x)	20 - 100 (1x)	5 - 25 (0.25x)
Q/2	0	2.5 - 20	5 - 40 (2x)	10 - 80 (4x)	2.5 - 20 (1x)
	1	5 - 40	10 - 80 (2x)	20 - 160 (4x)	5 - 40 (1x)

NOTE 1: The nQ5 output is inverted (180° phase shift) with respect to Q0:Q4.
NOTE 2: The input reference frequency is limited to 100MHz maximum.

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Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, $V_{DD(ABS\ MAX)}$	4.6V
Inputs, V_I	-0.5V to $V_{DD(ABS\ MAX)}$ + 0.5V
Outputs, V_O	-0.5V to $V_{DD(ABS\ MAX)}$ + 0.5V
Package Thermal Impedance, θ_{JA} 28 Lead QSOP 28 Lead PLCC	 66.0°C/W (0 lfpm) 46.4°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, V_{DD} = AV_{DD} = 3.3V ± 0.3V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}, AV_{DD}	Positive Supply Voltage		3.0	3.3	3.6	V
I_{DDQ}	Quiescent Power Supply Current	V_{DD} = AV_{DD} = max., OE/nRST = 0, SYNCx = 0, all outputs open			5	mA

Table 4B. LVCMOS/LVTTL DC Characteristics, V_{DD} = AV_{DD} = 3.3V ± 0.3V, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage			-0.3		0.8	V
I_{IH}	Input High Current	FREQ_SEL, FEEDBACK, SYNCn, OE/nRST, REF_SEL, PLL_EN	V_{DD} = V_{IN} = 3.3V			5	µA
		nPE	V_{DD} = V_{IN} = 3.3V			150	µA
I_{IL}	Input Low Current	FREQ_SEL, FEEDBACK, nPE, SYNCn, OE/nRST, REF_SEL, PLL_EN	V_{DD} = 3.3V, V_{IN} = 0V	-5			µA
V_{OH}	Output High Voltage	Q0:Q4, nQ5, 2XQ, Q/2, LOCK	I_{OH} = -24mA	2.6			V
V_{OL}	Output Low Voltage	Q0:Q4, nQ5, 2XQ, Q/2, LOCK	I_{OL} = 24mA			0.5	V
I_{OZ}	Output Leakage Current	Q0:Q4, nQ5, 2XQ, Q/2	OE/nRST = 0, V_{OUT} = 0V or V_{DD}, V_{DD} = 3.6V			±5	µA

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Table 5. AC Electrical Characteristics, V_{DD} = AV_{DD} = 3.3V ± 0.3V, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{REF}	SYNC[0:1] Input Reference Frequency		Feedback of Q[0:4] or nQ5, FREQ_SEL = 0	5		40	MHz
			Feedback of Q[0:4] or nQ5, FREQ_SEL = 1	10		80	MHz
			Feedback of 2XQ, FREQ_SEL = 0	10		80	MHz
			Feedback of 2XQ or FREQ_SEL = 1	20		100	MHz
			Feedback of Q/2, FREQ_SEL = 0	2.5		20	MHz
			Feedback of Q/2 or FREQ_SEL = 1	5		40	MHz
f_{OUT}	Output Frequency		2XQ			160	MHz
			Q[0:4], nQ5			80	MHz
			Q/2			40	MHz
idc	Input Duty Cycle		SYNC0, SYNC1	25		75	%
t_R / t_F	Input Rise/ Fall Time		SYNC0, SYNC1			3	ns
tsk(o)	Output Skew; NOTE 1, 2		Rising edges of Q[0:4] (incl. Q/2 if nPE = 0)			300	ps
	Output Skew; NOTE 1, 2		Falling edges of Q[0:4] (incl. Q/2 if nPE = 1)			300	ps
	Output Skew; NOTE 1, 2, 3		Rising edge of Q[0:4] 2XQ, Q/2 and Falling edge of nQ5			500	ps
t_{PW}	Pulse Width	2XQ	>40MHz	t_{PERIOD}/2 - 0.62		t_{PERIOD}/2 + 0.62	ns
		Q[0:4], nQ5	80MHz	t_{PERIOD}/2 - 0.45		t_{PERIOD}/2 + 0.45	ns
		Q/2	40MHz	t_{PERIOD}/2 - 0.6		t_{PERIOD}/2 + 0.6	ns
tjit(cc)	Cycle-to-Cycle Jitter	Q[0:4], nQ5	20MHz, FREQ_SEL = 0			150	ps
		Q[0:4], nQ5	20MHz, FREQ_SEL = 1			320	ps
t(ϕ)	Static Phase Offset, (SYNC[0:1] to FEEDBACK delay); NOTE 2, 4	Q[0:4], nQ5	80MHz and nPE = 0	0		300	ps
		Q[0:4], nQ5	80MHz and nPE = 1	-80		300	ps
t_{PZH}, t_{PZL}	Output Enable Time; NOTE 5	OE/nRST	Low-to-High			14	ns
t_{PHZ}, t_{PLZ}	Output Disable Time; NOTE 5	OE/nRST	High-to-Low			14	ns
t_R / t_F	Output Rise/ Fall Time	Q[0:4], nQ5, 2XQ, Q/2	0.8V – 2.0V	0.2		2	ns
t_{LOCK}	PLL Lock Time					10	ms

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE 1: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at V_{DD}/2.
NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 3: Measured between coincident rising output edges of Q0:Q4, 2XQ, Q/2 and the falling edge of nQ5.
NOTE 4: Defined as the time difference between the input reference clock and the average feedback input signal when the PLL is locked and the input reference frequency is stable.
NOTE 5: These parameters are guaranteed by characterization. Not tested in production.

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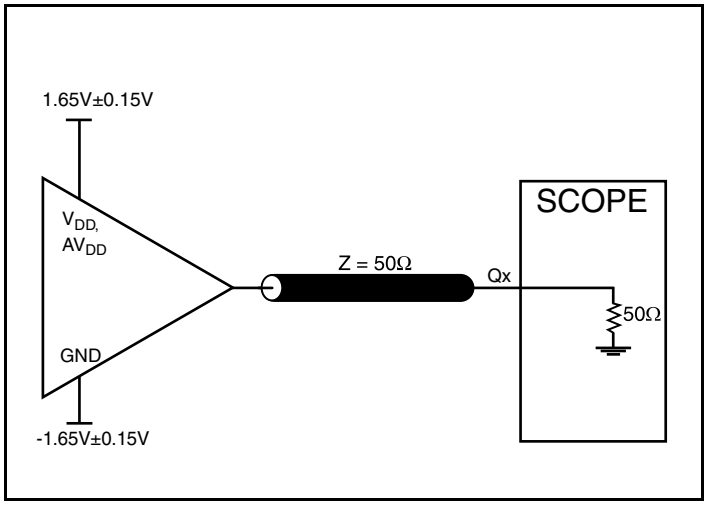
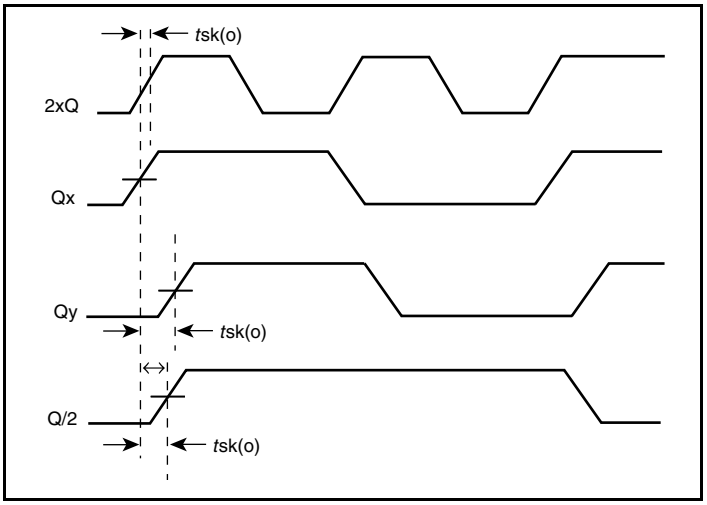
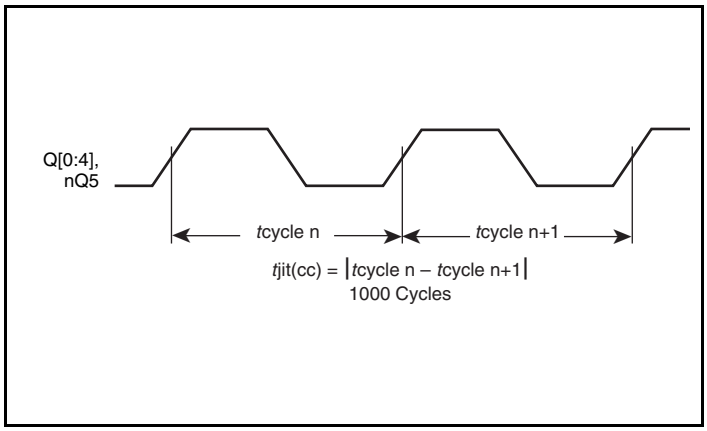
Parameter Measurement Information



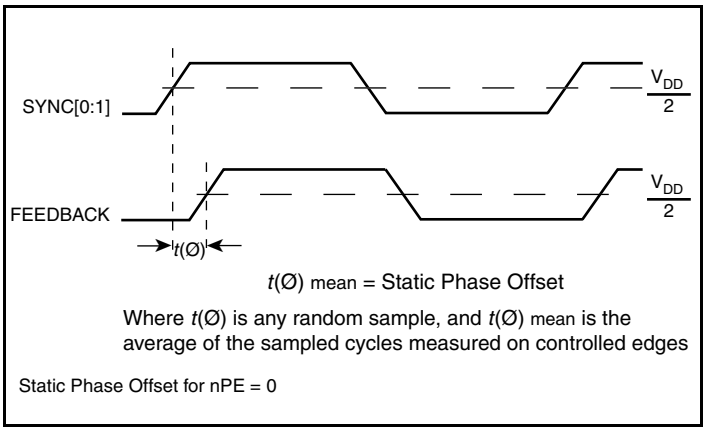
3.3V Output Load AC Test Circuit



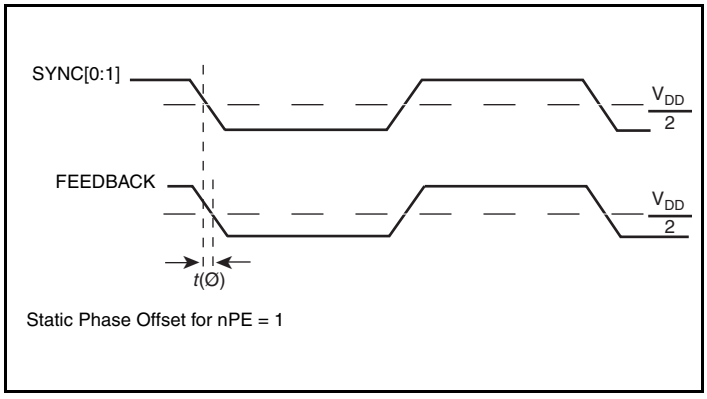
Output Skew



Cycle-to-Cycle Jitter



Static Phase Offset



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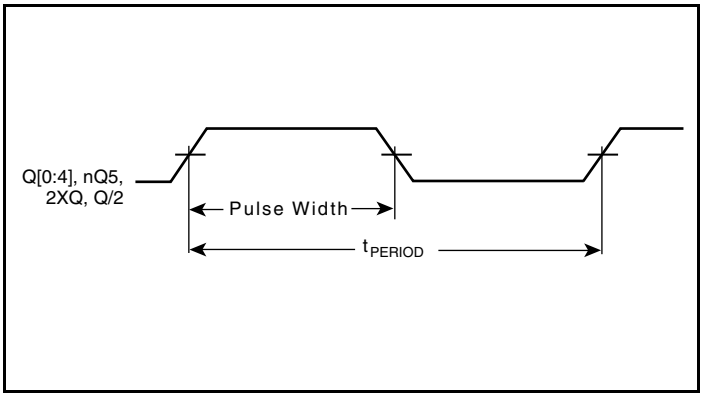

Output Pulse Width

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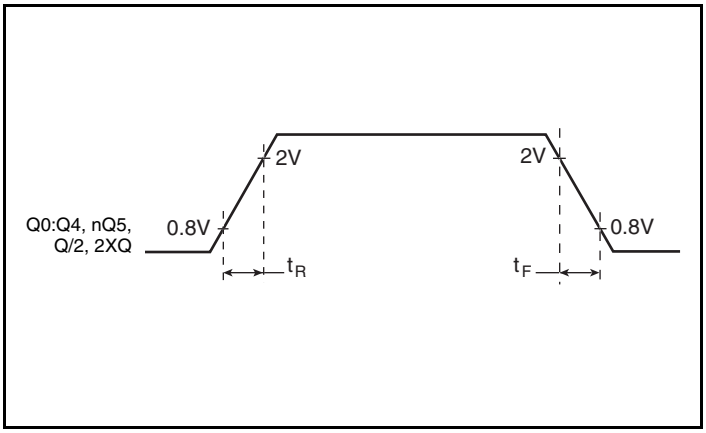
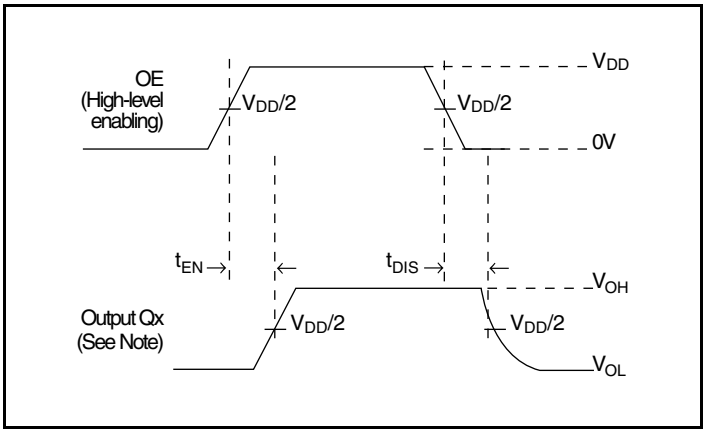
Parameter Measurement Information



Output Rise/Fall Time



Output Enable/Disable

Application Information

Recommendations for Unused Output Pins

Outputs:

LVCMOS Outputs

All unused LVCMOS output can be left floating. There should be no trace attached.

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Schematic Layout

Figure 1 shows an example of 870919I-01 application schematic. In this example, the device is operated at VDD=AVDD=3.3V. As with any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The 870919I-01 provides separate power supplies to isolate any high switching noise from coupling into the internal PLL.

In order to achieve the best possible filtering, it is recommended that the placement of the filter components be on the device side of the PCB as close to the power pins as possible. If space is limited, the 0.1µFcapacitor in each power pin filter should be placed on the device side. The other components can be on the opposite side of the PCB. Power supply filter recommendations are a general guideline to be used for reducing external noise from coupling into the devices.

The filter performance is designed for a wide range of noise frequencies. This low-pass filter starts to attenuate noise at approximately 10 kHz. If a specific frequency noise component is known, such as switching power supplies frequencies, it is recommended that component values be adjusted and if required, additional filtering be added. Additionally, good general design practices for power plane voltage stability suggests adding bulk capacitance in the local area of all devices.

The schematic example focuses on functional connections and is not configuration specific. Refer to the pin description and functional tables in the datasheet to ensure that the logic control inputs are properly set.

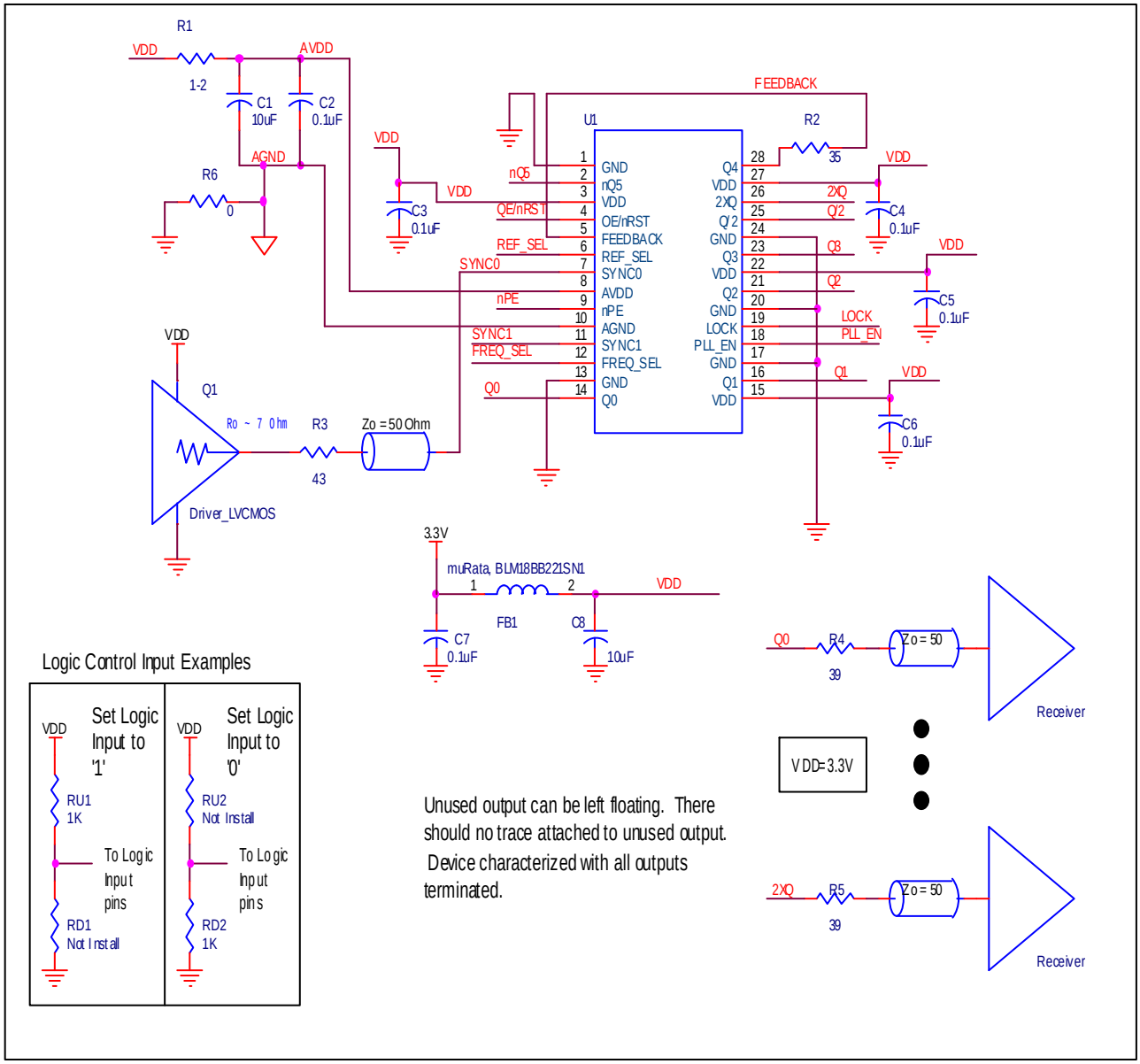

Figure 1. 870919I-01 Application Schematic

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Power Considerations

This section provides information on power dissipation and junction temperature for the 870919I-01.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the 870919I-01 is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{DD} = 3.3V + 0.3V = 3.6V, which gives worst case results.

- Power $(core)_{MAX} = V_{DD_MAX} * I_{DD_MAX}$= 3.6V *5mA = **18mW**
- Output Impedance R_{OUT} Power Dissipation due to Loading 50Ω to $V_{DD}/2$
  Output Current $I_{OUT} = V_{DD_MAX} / [2 * (50Ω + R_{OUT})] = 3.6V / [2 * (50Ω + 11Ω)]$ = **29.5mA**
- Power Dissipation on the R_{OUT} per LVCMOS output
  Power $(R_{OUT}) = R_{OUT} * (I_{OUT})^2 = 11Ω * (29.5mA)^2$ = **9.57mW per output**
- Total Power (R_{OUT}) = R_{OUT} (per output) * number of outputs = 9.57mW * 8 outputs = **76.56mW**

Dynamic Power Dissipation for Q = 80MHz

Power (80MHz) = C_{PD} * Frequency * $(V_{DD})^2$ = 330pF * 80MHz * $(3.6V)^2$ = **342mW**

Total Power

= $(core)_{MAX}$ + Total Power (R_{OUT}) + Power (80MHz)
= 18mW + 76.56mW + 342mW
= 436.56mW

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for the devices is 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 66°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.437W * 66°C/W = 113.8°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 6. Thermal Resistance θ_{JA} for a 28 Lead QSOP, Forced Convection

θ_{JA} by Velocity			
Linear Feet per Minute	**0**	**200**	**500**
Multi-Layer PCB, JEDEC Standard Test Boards	66.0°C/W	58.3°C/W	55.2°C/W

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Package Outline - R Suffix for 28 Lead QSOP, 150MIL

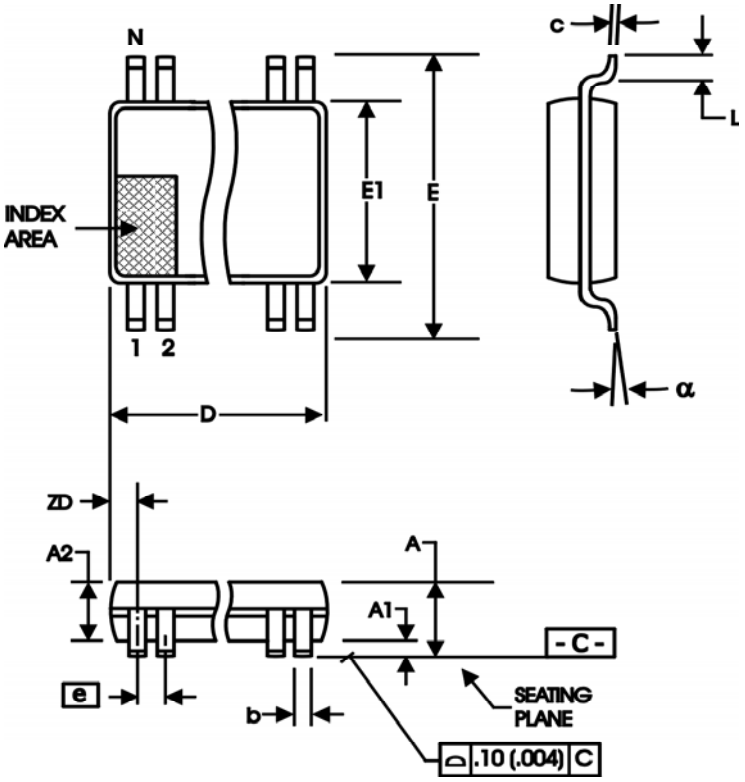

Table 7B. Package Dimensions for 28 Lead QSOP

All Dimensions in Millimeters		
Symbol	**Minimum**	**Maximum**
N	28	
A	1.35	1.75
A1	0.10	0.25
A2		1.50
b	0.20	0.30
c	0.18	0.25
D	9.80	10.00
E	5.80	6.20
E1	3.80	4.00
e	0.635 Basic	
L	0.40	1.27
α	0°	8°
ZD	0.84 Ref	

Reference Document: JEDEC Publication 95, MO-137

Reliability Information

Table 8A. θ_{JA} vs. Air Flow Table for a 28 Lead QSOP, 150MIL

θ_{JA} vs. Air Flow			
Linear Feet per Minute	**0**	**200**	**500**
Multi-Layer PCB, JEDEC Standard Test Boards	66.0°C/W	58.3°C/W	55.2°C/W

Table 8B. θ_{JA} vs. Air Flow Table for a 28 Lead PLCC

θ_{JA} vs. Air Flow			
Linear Feet per Minute	**0**	**200**	**500**
Multi-Layer PCB, JEDEC Standard Test Boards	46.4°C/W	38.6°C/W	36.2°C/W

Transistor Count

The transistor count for 870919I-01: 1654

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Ordering Information

Table 9. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
870919BRI-01LF	870919BRI-01L	“Lead-Free” 28 Lead QSOP	Tube	-40°C to 85°C
870919BRI-01LFT	870919BRI-01L	“Lead-Free” 28 Lead QSOP	2500 Tape & Reel	-40°C to 85°C

NOTE: "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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Revision History Sheet

Rev	Table	Page	Description of Change	Date
A		2	QSOP Pin Assignment - added dimensions.	7/7/09
B		3, 6	Updated Pin 4, OE/nRST Description; changed V_{DD} to $V_{DD\ (ABS\ MAX)}$.	11/15/11
C		10	Added Application Schematic	1/6/12
C	T9	14	Removed leaded orderable parts from the Ordering Information table	11/15/12
C	 9	2 12 14	Crossed out PLCC package. Removed PLCC package drawing. Ordering Information - removed PLCC part number.	11/6/15

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