General Description

The 874005 is a high performance Differential-to-LVDS Jitter Attenuator designed for use in PCI Express systems. In some PCI Express systems, such as those found in desktop PCs, the PCI Express clocks are generated from a low bandwidth, high phase noise PLL frequency synthesizer. In these systems, a jitter attenuator may be required to attenuate high frequency random and deterministic jitter components from the PLL synthesizer and from the system board. The 874005 has 3 PLL bandwidth modes: 200kHz, 400kHz, and 800kHz. The 200kHz mode will provide maximum jitter attenuation, but with higher PLL tracking skew and spread spectrum modulation from the motherboard synthesizer may be attenuated. The 400kHz provides an intermediate bandwidth that can easily track triangular spread profiles, while providing good jitter attenuation. The 800kHz bandwidth provides the best tracking skew and will pass most spread profiles, but the jitter attenuation will not be as good as the lower bandwidth modes. Because some 2.5Gb serdes have x20 multipliers while others have than x25 multipliers, the 874005 can be set for 1:1 mode or 5/4 multiplication mode (i.e. 100MHz input/125MHz output) using the F_SEL pins.

The 874005 uses IDT's 3rd Generation FemtoClock® PLL technology to achive the lowest possible phase noise. The device is packaged in a 24 Lead TSSOP package, making it ideal for use in space constrained applications such as PCI Express add-in cards.

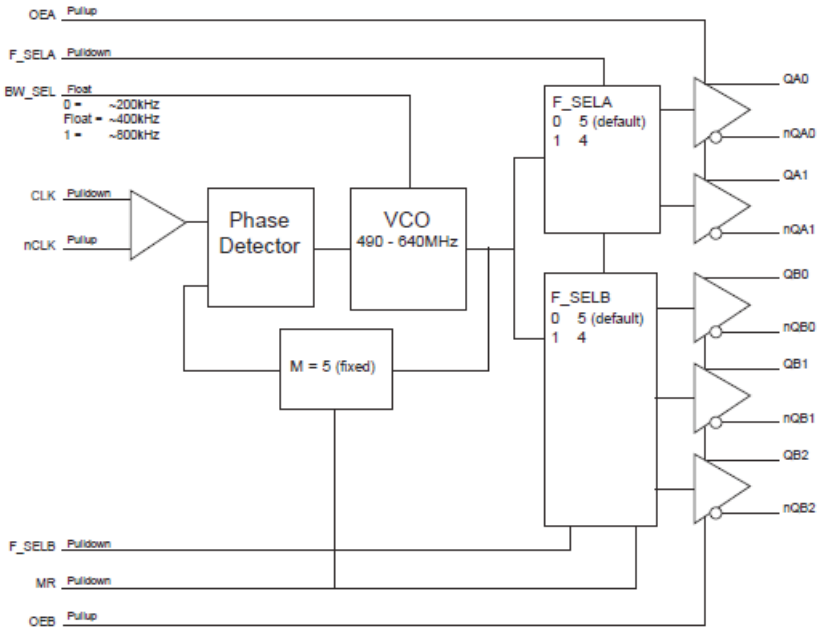
Features

- Five differential LVDS output pairs
- One differential clock input
- CLK and nCLK supports the following input types: LVPECL, LVDS, LVHSTL, SSTL, HCSL
- Output frequency range: 98MHz - 160MHz
- Input frequency range: 98MHz - 128MHz
- VCO range: 490MHz - 640MHz
- Cycle-to-cycle jitter: 30ps (maximum)
- 3.3V operating supply
- 3 bandwidth modes allow the system designer to make jitter attenuation/tracking skew design trade-offs
- 0°C to 70°C ambient operating temperature
- Available in lead-free RoHS compliant package

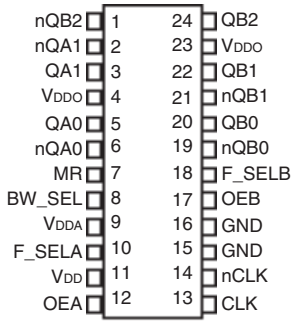
PLL Bandwidth

BW_SEL
0 = PLL Bandwidth: ~200kHz
Float = PLL Bandwidth: ~400kHz (Default)
1 = PLL Bandwidth: ~800kHz

Block Diagram



Pin Assignment



874005

24-Lead TSSOP

4.40mm x 7.8mm x 0.92mm package body

G Package

Top View

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Table 1. Pin Descriptions

Number	Name	Type		Description
1, 24	nQB2, QB2	Output		Differential output pair. LVDS interface levels.
2, 3	nQA1, QA1	Output		Differential output pair. LVDS interface levels.
4, 23	V_{DDO}	Power		Output supply pins.
5, 6	QA0, nQA0	Output		Differential output pair. LVDS interface levels.
7	MR	Input	Pulldown	Active HIGH Master Reset. When logic HIGH, the internal dividers are reset causing the true outputs (nQx) to go low and the inverted outputs (Qx) to go high. When logic LOW, the internal dividers and the outputs are enabled. LVCMOS/LVTTL interface levels.
8	BW_SEL	Input	Pullup/ Pulldown	PLL Bandwidth input. See Table 3B.
9	V_{DDA}	Power		Analog supply pin.
10	F_SELA	Input	Pulldown	Frequency select pin for QAx,nQAx outputs. LVCMOS/LVTTL interface levels.
11	V_{DD}	Power		Core supply pin.
12	OEA	Input	Pullup	Output enable pin for QA pins. When HIGH, the QAx/nQAx outputs are active. When LOW, the QAx,nQAx outputs are in a high impedance state. LVCMOS/LVTTL interface levels.
13	CLK	Input	Pulldown	Non-inverting differential clock input.
14	nCLK	Input	Pullup	Inverting differential clock input.
15, 16	GND	Power		Power supply ground.
17	OEB	Input	Pullup	Output enable pin for QB pins. When HIGH, the QBx/nQBx outputs are active. When LOW, the QBx,nQBx outputs are in a high impedance state. LVCMOS/LVTTL interface levels.
18	F_SELB	Input	Pulldown	Frequency select pin for QBx,nQBx outputs. LVCMOS/LVTTL interface levels.
19, 20	nQB0, QB0	Output		Differential output pair. LVDS interface levels.
21, 22	nQB1, QB1	Output		Differential output pair. LVDS interface levels.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ

Table 3A. Output Enable Function Table

Inputs	Outputs	
OEA/OEB	QAx/nQAx	QBx/nQBx
0	HiZ	HiZ
1	Enabled	Enabled

Table 3B. PLL Bandwidth/PLL Bypass Control

Inputs	PLL Band-width
PLL_BW	
0	~200kHz
1	~800kHz
Float	~400kHz

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Absolute Maximum Ratings

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5 V
Outputs, V_O	-0.5V to V_{DDO} + 0.5V
Package Thermal Impedance, θ_{JA}	70°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Table 4A. Power Supply DC Characteristics, $V_{DD} = V_{DDA} = V_{DDO} = 3.3V \pm 5\%$, T_A = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		3.135	3.3	3.465	V
V_{DDO}	Output Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current				85	mA
I_{DDA}	Analog Supply Current				15	mA
I_{DDO}	Output Supply Current				115	mA

Table 4B. LVCMOS/LVTTL DC Characteristics, $V_{DD} = V_{DDA} = V_{DDO} = 3.3V \pm 5\%$, T_A = 0°C to 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	OEA, OEB, MR, F_SELA, F_SELB		2		V_{DD} + 0.3	V
		BW_SEL		V_{DD} - 0.4			V
V_{IL}	Input Low Voltage	OEA, OEB, MR, F_SELA, F_SELB		-0.3		0.8	V
		BW_SEL				0.4	V
V_{IM}	Input Mid Voltage	BW_SEL		$V_{DD}/2$ - 0.1		$V_{DD}/2$ + 0.1	V
I_{IH}	Input High Current	OEA, OEB	$V_{DD} = V_{IN} = 3.465V$			5	µA
		F_SELA, F_SELB MR, BW_SEL	$V_{DD} = V_{IN} = 3.465V$			150	µA
I_{IL}	Input Low Current	BW_SEL, OEA, OEB	$V_{DD} = 3.465V$, $V_{IN} = 0V$	-150			µA
		MR, F_SELA, F_SELB	$V_{DD} = 3.465V$, $V_{IN} = 0V$	-5			µA

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TABLE 4C. DIFFERENTIAL DC CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDO} = 3.3V \pm 5\%$, T_A = 0°C TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	CLK	$V_{DD} = V_{IN} = 3.465V$			150	µA
		nCLK	$V_{DD} = V_{IN} = 3.465V$			5	µA
I_{IL}	Input Low Current	CLK	$V_{DD} = V_{IN} = 3.465V$	-5			µA
		nCLK	$V_{DD} = V_{IN} = 3.465V$	-150			µA
V_{PP}	Peak-to-Peak Input Voltage			0.15		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			GND + 0.5		V_{DD} - 0.85	V

NOTE 1: Common mode voltage is defined as V_{IH}.
NOTE 2: For single ended applications, the maximum input voltage for CLK, nCLK is V_{DD} + 0.3V.

TABLE 4D. LVDS DC CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDO} = 3.3V \pm 5\%$, T_A = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage		275	375	485	mV
ΔV_{OD}	V_{OD} Magnitude Change				50	mV
V_{OS}	Offset Voltage		1.2	1.35	1.5	V
ΔV_{OS}	V_{OS} Magnitude Change				50	mV

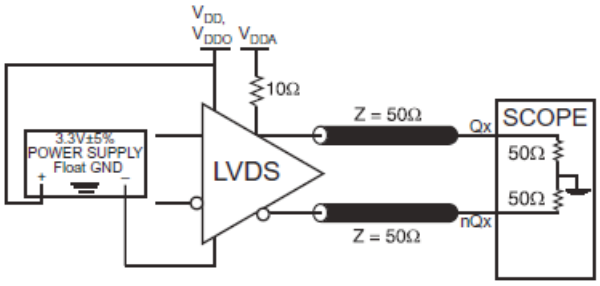
TABLE 5. AC CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDO} = 3.3V \pm 5\%$, T_A = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency		98		160	MHz
tjit(cc)	Cycle-to-Cycle Jitter, NOTE 1			15	30	ps
tsk(o)	Output Skew; NOTE 2, 3				90	ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	300		550	ps
odc	Output Duty Cycle		48		52	%

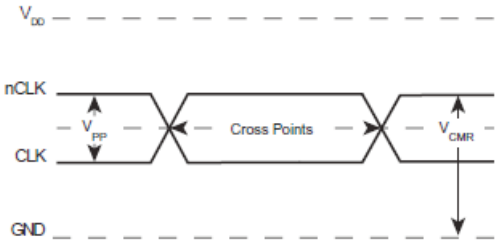
NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditons.
NOTE 1: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at V_{DDO}/2.
NOTE 3: These parameters are guaranteed by characterization. Not tested in production.

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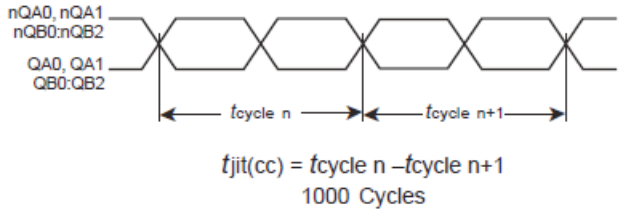
PARAMETER MEASUREMENT INFORMATION



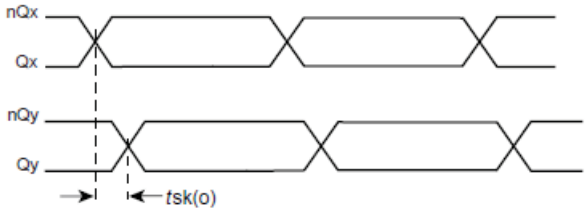
3.3V LVDS OUTPUT LOAD AC TEST CIRCUIT



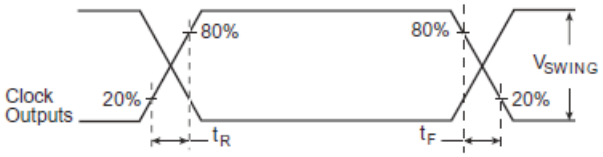
DIFFERENTIAL INPUT LEVEL



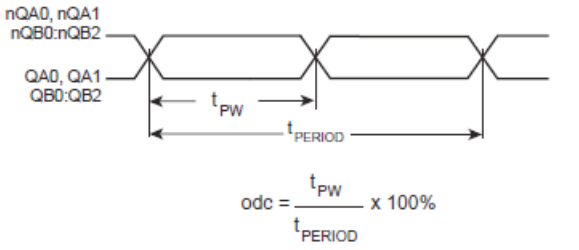
CYCLE-TO-CYCLE JITTER



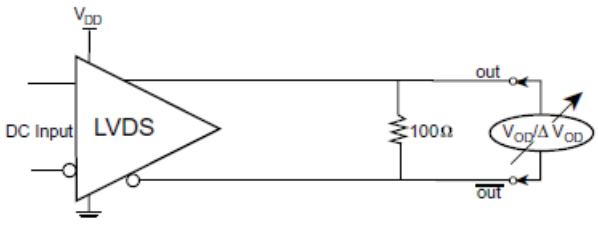
OUTPUT SKEW



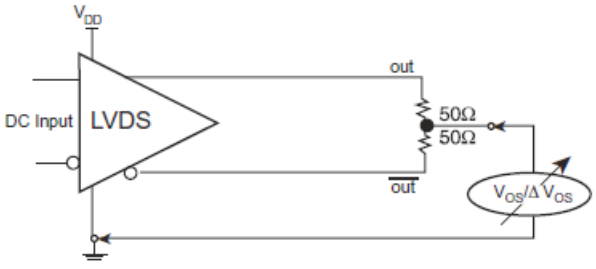
OUTPUT RISE/FALL TIME



OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD



DIFFERENTIAL OUTPUT VOLTAGE SETUP



OFFSET VOLTAGE SETUP

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Applications Information

Wiring the Differential Input to Accept Single Ended Levels

Figure 2 shows how a differential input can be wired to accept single ended levels. The reference voltage $V_{REF} = {}_{VDD}/2$ is generated by the bias resistors R1 and R2. The bypass capacitor (C1) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of R1 and R2 might need to be adjusted to position the V_{REF} in the center of the input voltage swing. For example, if the input clock swing is 2.5V and $_{VDD}$ = 3.3V, R1 and R2 value should be adjusted to set V_{REF} at 1.25V. The values below are for when both the single ended swing and V_{DD} are at the same voltage. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways. First, R3 and R4 in parallel should equal the transmission line impedance. For most 50W applications, R3 and R4 can be 100W. The values of the resistors can be increased to reduce the loading for slower and weaker LVCMOS driver. When using single-ended signaling, the noise rejection benefits of differential signaling are reduced. Even though the differential input can handle full rail LVCMOS signaling, it is recommended that the amplitude be reduced. The datasheet specifies a lower differential amplitude, however this only applies to differential signals. For single-ended applications, the swing can be larger, however V_{IL} cannot be less than -0.3V and V_{IH} cannot be more than V_{CC} + 0.3V. Though some of the recommended components might not be used, the pads should be placed in the layout. They can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a differential signal.

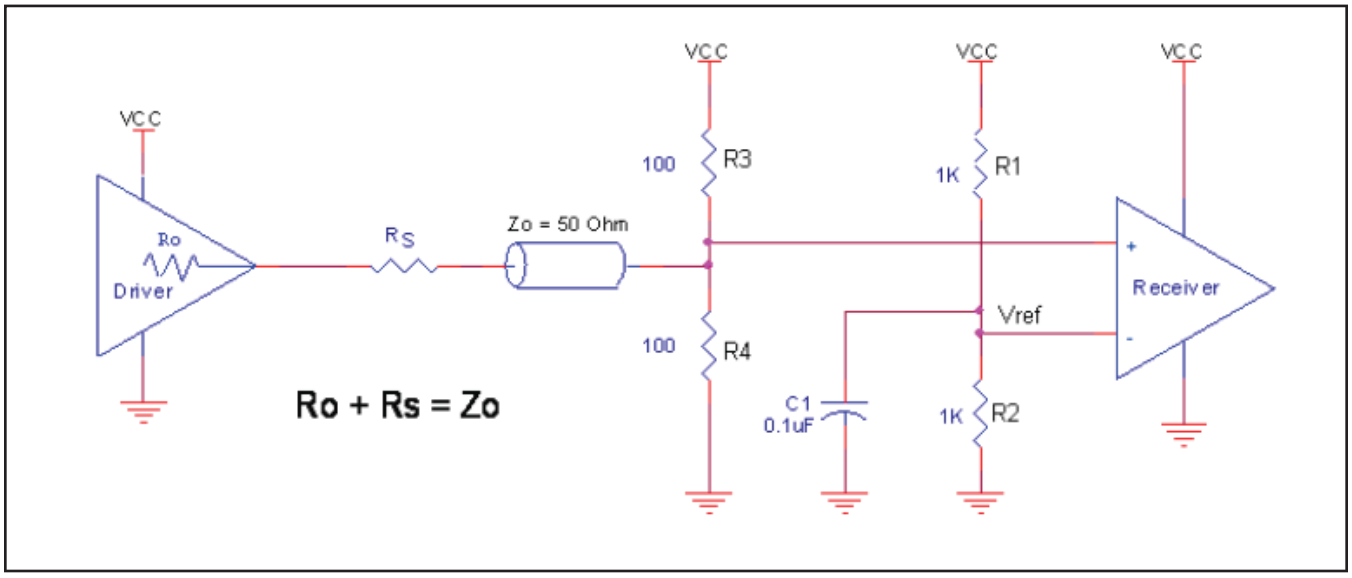


Figure 2. Recommended Schematic for Wiring a Differential Input to Accept Single-ended Levels

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Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, SSTL, HCSL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. Figures 3A to 3D show interface examples for the CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example in *Figure 3A,* the input termination applies for LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

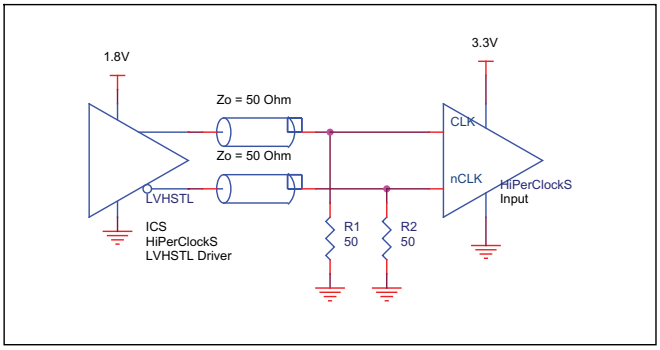


Figure 3A. CLK/nCLK Input Driven by LVHSTL Driver

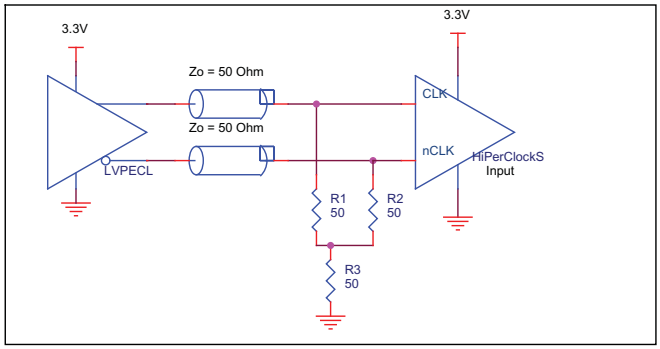


Figure 3B. CLK/nCLK Input Driven by 3.3V LVPECL Driver

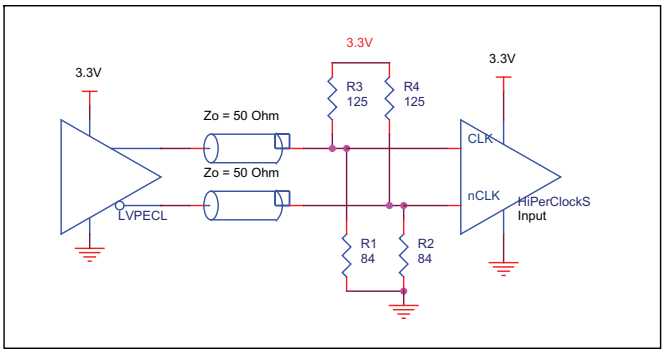


Figure 3C. CLK/nCLK Input Driven by 3.3V LVPECL Driver

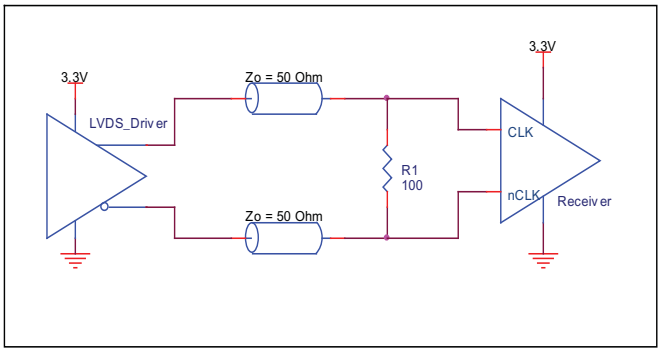


Figure 3D. CLK/nCLK Input Driven by 3.3V LVDS Driver

Recommendations for Unused Input and Output Pins

Inputs:

LVCMOS Control Pins:

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs:

LVDS

All unused LVDS output pairs can be either left floating or terminated with 100Ω across. If they are left floating, we recommend that there is no trace attached.

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LVDS Driver Termination

A general LVDS interface is shown in *Figure 4.* In a 100Ω differential transmission line environment, LVDS drivers require a matched load termination of 100Ω across near the receiver input. For a multiple LVDS outputs buffer, if only partial outputs are used, it is recommended to terminate the unused outputs.

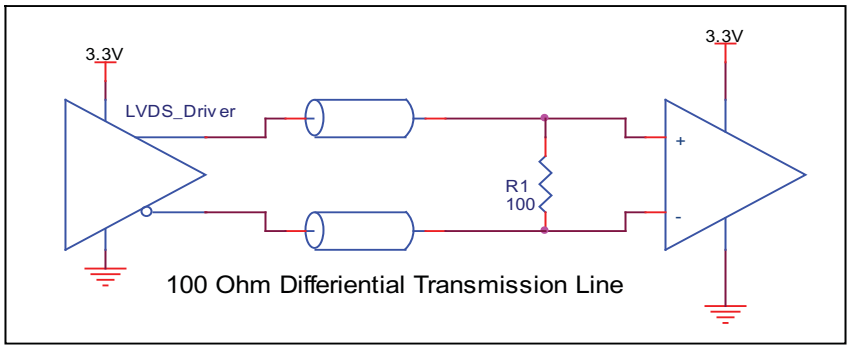


Figure 4. Typical LVDS Driver Termination

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Schematic Example

Differential Clock Input Interface

Figure 5 is an 874005 application example schematic. The schematic focuses on functional connections and is not configuration specific. Refer to the pin description and functional tables in the datasheet to ensure that the logic control inputs are properly set. The input is provided by 3.3V LVPECL driver with a Y-termination for simplicity, ease of layout and better control of the termination power over device variations. As with any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The 874005 provides separate VDD and VDDO power supplies to isolate any high switching noise from coupling into the internal PLL. In order to achieve the best possible filtering, it is recommended that the placement of the filter components be on the device side of the PCB as close to the power pins as possible. If space is limited, the 0.1uF capacitor in each power pin filter should be placed on the device side. The other components can be on the opposite side of the PCB. Power supply filter recommendations are a general guideline to be used for reducing external noise from coupling into the devices. The VCC and VCCO filters start to attenuate noise at approximately 10kHz. If a specific frequency noise component is known, such as switching power supplies frequencies, it is recommended that component values be adjusted and if required, additional filtering be added. Additionally, good general design practices for power plane voltage stability suggests adding bulk capacitance in the local area of all devices.

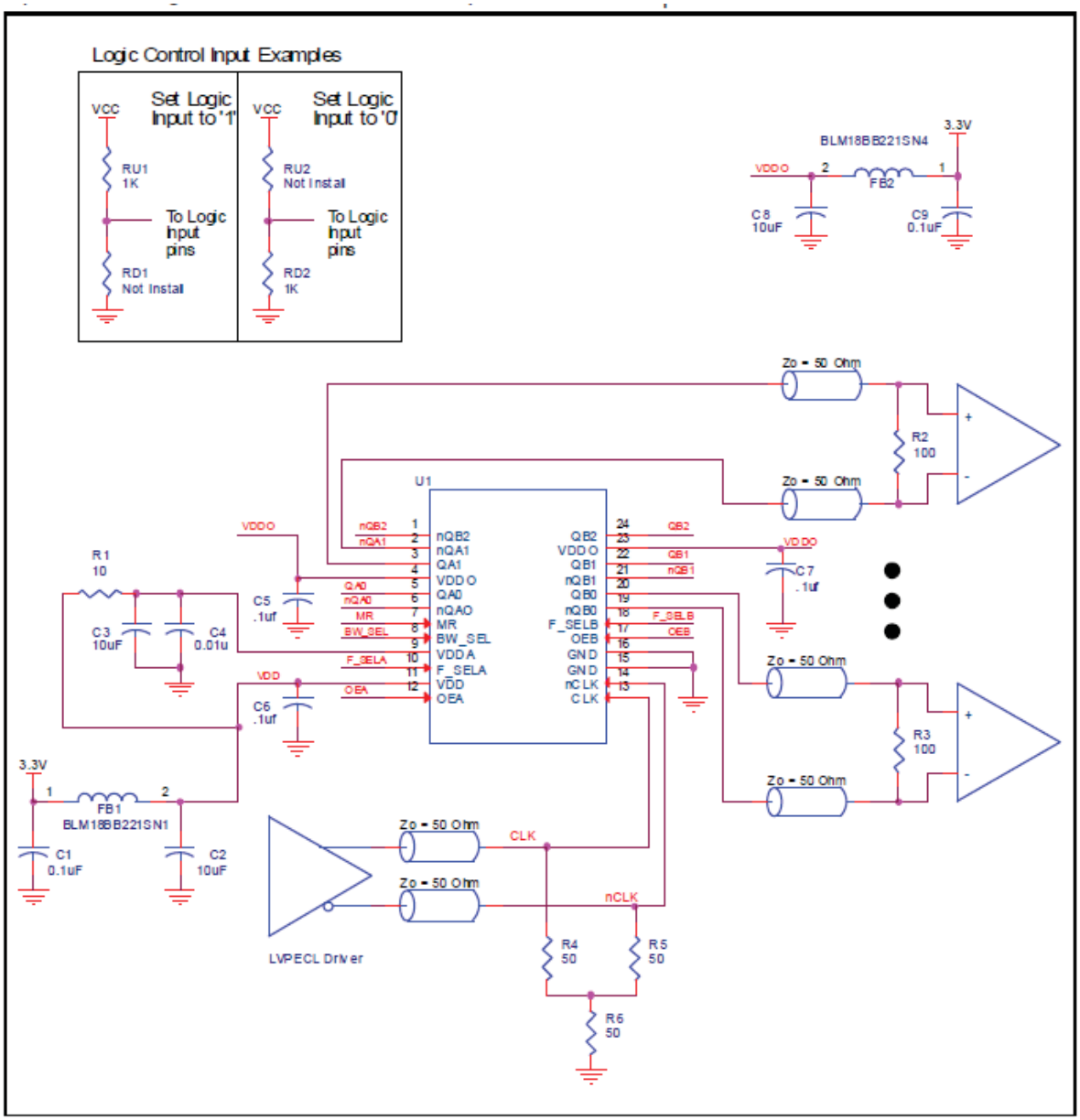


Figure 5. 874005 Schematic Example

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POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the 874005. Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the 874005 is the sum of the core power plus the power dissipated in the load(s).

The following is the power dissipation for V_{DD} = 3.3V + 5% = 3.465V, which gives worst case results.

- Power (core)$_{MAX}$ = V_{DD_MAX} * (I_{DD_MAX} + I_{DDA_MAX}) = 3.465V * (85mA + 15mA) = **346.5mW**
- Power (outputs)$_{MAX}$ = V_{DDO_MAX} * I_{DDO_MAX} = 3.465V * 115mA = **398.48mW**

Total Power$_{_MAX}$ = 3.465mW + 398.48mW = **745mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for the devices is 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd_total + T_A$

Tj = Junction Temperature

q_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming a moderate air flow of 200 linear feet per minute and a multi-layer board, the appropriate value is 63°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 70°C with all outputs switching is:

70°C + 0.745W * 63°C/W = 117°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (multi-layer).

TABLE 6. THERMAL RESISTANCE θ_{JA} FOR 24-LEAD TSSOP, FORCED CONVECTION

θ_{JA} by Velocity (Linear Feet per Minute)	0	200	500
Multi-Layer PCB, JEDEC Standard Test Boards	70°C/W	63°C/W	60°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

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Reliability Information

Table 7. θ_{JA} vs. Air Flow Table for 24 Lead TSSOP

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	**200**	**500**
Multi-Layer PCB, JEDEC Standard Test Boards	70°C/W	63°C/W	60°C/W

Transistor Count

The transistor count for 874005 is: 1206

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Package Outline - G Suffix for 24 Lead TSSOP

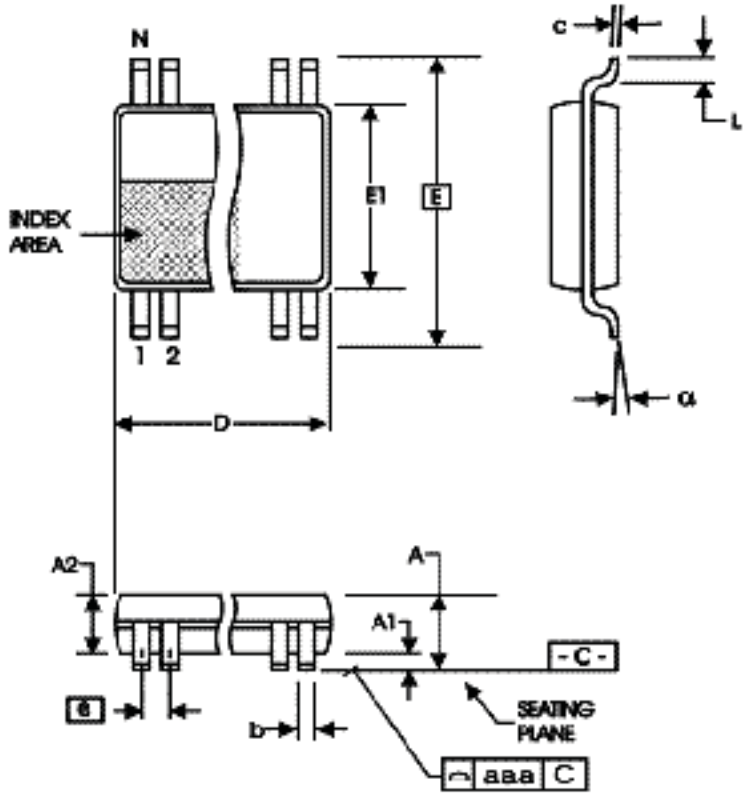


Table 8. Package Dimensions

SYMBOL	Millimeters	
	Minimum	Maximum
N	24	
A	--	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	7.70	7.90
E	6.40 BASIC	
E1	4.30	4.50
e	0.65 BASIC	
L	0.45	0.75
α	0°	8°
aaa	--	0.10

Reference Document: JEDEC Publication 95, MO-153

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TABLE 9. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
874005AGLF	ICS874005AGLF	24 Lead “Lead-Free” TSSOP	tube	0°C to 70°C
874005AGLFT	ICS874005AGLF	24 Lead “Lead-Free” TSSOP	tape & reel	0°C to 70°C

NOTE: Parts that are ordered with an “LF” suffix to the part number are the Pb-Free configuration and are RoHS complaint.

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REVISION HISTORY SHEET				
Rev	**Table**	**Page**	**Description of Change**	**Date**
A	T9	12 14	Updated datasheet's header/footer with IDT from ICS. Ordering Information Table - removed ICS prefix from Part/Order Number column. Added LF marking. Added Contact Page.	10/5/10
B	1 4C	1 2 4 7 9	Updated datasheet's header/footer with IDT format. Change Block Diagram to update OEA input to Pullup from Pulldown. Removed nFB_OUT from Pin Descriptions. Added I_{IH} Min and I_{IL} Max ratings. Added new figure 2. Added New Application Schematic.	1/12/12
B	T9	13	Ordering Information - removed leaded devices. Updated data sheet format.	7/20/15

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