IDT™ EB-LOGAN-23 Evaluation Board Manual

(Evaluation Board: 18-691-001)

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Table of Contents

Notes

Description of the EB-LOGAN-23 Evaluation Board

Introduction 1-1
Board Features 1-2
Hardware 1-2
Software 1-2
Other 1-2
Revision History 1-2

Installation of the EB-LOGAN-23 Evaluation Board

EB-LOGAN-23 Installation 2-1
PCI Express Mezzanine and Edge Adapters 2-1
Hardware Description 2-3
Reference Clocks 2-4
Global Reference Input Clocks 2-4
Local Port Input Clocks 2-6
CLKMODE Selection 2-8
Power Sources 2-9
PCI Express Analog Power Voltage Regulator 2-10
PCI Express Digital Power Voltage Converter 2-10
PCI Express Transmitter Analog Voltage Converter 2-10
Core Logic Voltage Converter 2-10
3.3V I/O Voltage Regulator 2-10
Power-up Sequence for PES32NT24AG2 2-10
Heatsink Requirement 2-10
Reset 2-10
Fundamental Reset 2-10
Downstream Reset 2-11
Stack Configuration 2-11
Boot Configuration Vector 2-11
SMBus Interfaces 2-12
SMBus Slave Interface 2-12
SMBus Master Interface 2-13
JTAG Header 2-13
Miscellaneous Jumpers, Headers 2-14
LEDs 2-15
EB-LOGAN-23 Board Figure 2-23

Software For EB-LOGAN-23

Introduction 3-1
Device Management Software 3-1
Device Drivers 3-1

Schematics

Schematics 4-1

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Notes

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List of Figures

Notes

Figure 1.1 Function Block Diagram of the EB-LOGAN-23 Evaluation Board 1-1
Figure 2.1 Bifurcated and Merged Mezzanine Cards 2-1
Figure 2.2 MiniSAS Mezzanine Adapter 2-2
Figure 2.3 EB-LOGAN-23 iSAS-to-SATA Breakout Cable 2-2
Figure 2.4 EB-LOGAN-23 iSAS-to-iSAS Cable 2-2
Figure 2.5 PCIe x4 Edge-to-SATA Adapter 2-3
Figure 2.6 PCIe x8 Edge-to-SAS Adapter 2-3
Figure 2.7 EB-LOGAN-23 Evaluation Main Board 2-4
Figure 2.8 12-PACK PCIe Slots Breakout Board 2-4
Figure 2.9 Differential Jumper Arrangement Example 2-5
Figure 2.10 Reference Clock Configuration 2-5
Figure 2.11 EB32NT24AG2 Evaluation Board 2-23

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Notes

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List of Tables

Notes

Table 2.1 EB-LOGAN-23 Global Clock Select 2-5
Table 2.2 Clock Buffer Input Sources 2-6
Table 2.3 Global Reference Input Clock Frequency Select 2-6
Table 2.4 Onboard Clock Generator Frequency Select 2-6
Table 2.5 Onboard Reference Clock Generator Access Points 2-6
Table 2.6 EB-LOGAN-23 Port (0, 2, 4, 6, 12, 20) Clock Select 2-7
Table 2.7 EB-LOGAN-23 Port 8 Clock Source Select 2-7
Table 2.8 EB-LOGAN-23 Port 16 Clock Source Select 2-7
Table 2.9 EB-LOGAN-23 Slot Clock Select 2-8
Table 2.10 CLKMODE Selection for the PES32NT24AG2 2-9
Table 2.11 EPS12V 24-pin Power Connector - J69 2-9
Table 2.12 EPS12V 8-Pin Connector - J68 2-9
Table 2.13 Ports in Each Stack 2-11
Table 2.14 Boot Configuration Vector Signals 2-11
Table 2.15 Boot Configuration Vector Switch SW10 2-12
Table 2.16 Slave SMBus Interface Connector 2-12
Table 2.17 SMBus Slave Interface Address Configuration 2-13
Table 2.18 JTAG Connector Pin Out 2-13
Table 2.19 Miscellaneous Jumpers, Headers 2-14
Table 2.20 LED Indicators 2-15

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Notes

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Description of the EB-LOGAN-23 Evaluation Board

Notes

Introduction

The 89H32NT24AG2 switch (also referred to as PES32NT24AG2 in this manual) is a member of the IDT PCI Express® Inter-Domain Switch family of products. It is a PCIe® Base Specification 2.1 compliant (Gen2) 32-lane, 24-port switch. The EB-LOGAN-23 Evaluation Board provides an evaluation platform for both the PES32NT24AG2 and PES32NT24BG2 switches and for several other members of this switch family including PES24NT24AG2, PES32NT8AG2, and PES24NT6AG2 .

Detailed information related to configuration of number of ports and lanes in the switch device can be found in the Device User Manual and the Device Data Sheet. The evaluation board, along with additional adapters and daughter boards provide by IDT, can be configured to test every possible combination of the number of lanes and ports offered by the switch. Advanced capabilities such as switch partitioning, NTB, DMA, and local port clocking can be evaluated with the evaluation board.

The EB-LOGAN-23 brings out all 32 lanes of the device to 4 Mezzanine connectors (see Figure 1.1) located close to the device — one connector per stack of 8 lanes. Various types of daughter cards (provided by IDT) can then be plugged into these connectors to facilitate connectivity to one x8 or two x4 or four x2 or eight x1 link partners. Link partners may be plugged directly into these daughter cards, or they can be connected to these daughter cards via SAS or SATA cables and a different board with PCIe slots known as the 12-PACK board (provided by IDT). Given that the majority of the hosts/servers offer PCIe standard slots, IDT provides the necessary adapter cards that may be plugged into these host/server slots as well as the cables that connect such adapters to the daughter cards, which in turn are plugged into the main evaluation board on which the IDT PCIe switch device is populated.

The EB-LOGAN-23 is also used by IDT to reproduce system-level hardware or software issues reported by customers. Figure 1.1 illustrates the functional block diagram representing the main parts of the EB-LOGAN-23 board.

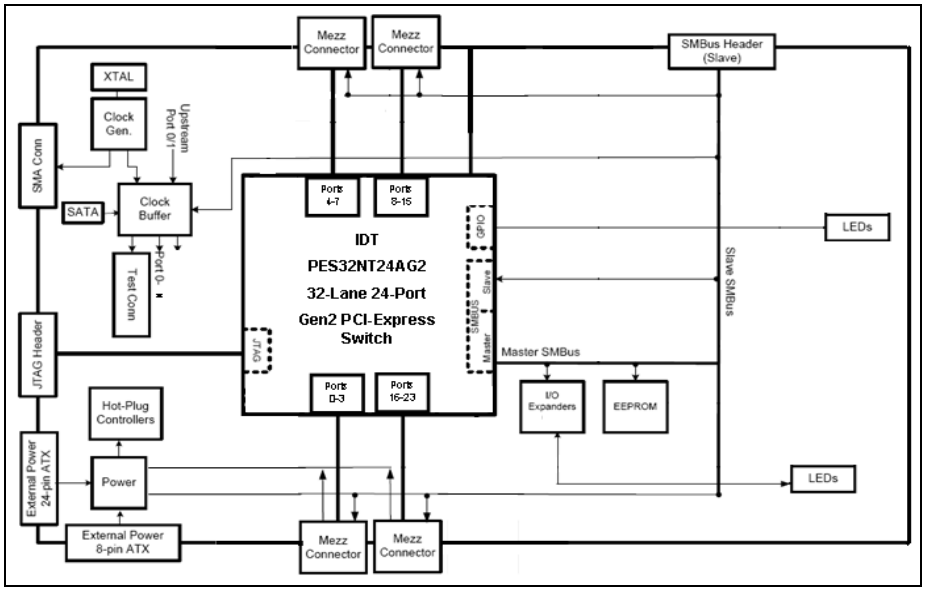


Figure 1.1 Function Block Diagram of the EB-LOGAN-23 Evaluation Board

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Notes

Board Features

Hardware

- 32NT24AG2 PCIe 24-port switch
  - Twenty four ports (8 x2 and 16 x1) — adjacent ports may be combined to create x4 or x8 ports
  - PCIe Base Specification Revision 2.1 compliant (Gen2 SerDes speeds of 5 GT/S)
  - Up to 2048 byte maximum Payload Size
  - Automatic lane reversal and polarity inversion supported on all lanes
  - Automatic per port link width negotiation to x8, x4, x2, x1
  - Power on reconfiguration via optional serial EEPROM connected to the SMBUS Master interface
- Upstream, Downstream Ports
  - The EB-LOGAN-23 has a minimum of one port configured as an upstream port to be plugged into a host slot through an adaptor and a cable.
  - Up to 23 ports can be configured as downstream ports, for PCIe endpoint add-on cards to be plugged in. The slot connectors can be configured to be x1, x2, x4, or x8, but are mechanically open-ended on one side to allow card widths greater than x8 (e.g. x16) to be populated.
  - When used in multi-partition mode, the device can be programmed through the serial EEPROM to generate the appropriate number of upstream and downstream ports per partition.
- Numerous user selectable configurations set using onboard jumpers and DIP-switches
  - Source of clock - host clock or onboard clock generator
  - Two clock rates (100/125 MHz) from an onboard clock generator
  - Flexible clocking modes
    - *Common clock*
    - *Non-common clock*
    - *Local port clocking on ports that support this feature*
  - Boot mode selection
- SMBUS Slave Interface (4 pin header)
- SMBUS Master Interface connected to the Serial EEPROMs and I/O Expanders
- Push button for Warm Reset
- Many LEDs to display status, reset, power, hot-plug, etc.
- JTAG connector to the 32NT24AG2 JTAG pins.

Software

There is no software or firmware executed on the board. However, useful software is provided along with the Evaluation Board to facilitate configuration and evaluation of the 32NT24AG2 within host systems running popular operating systems.

- Installation programs
  - Operating Systems Supported: WindowsServer200x, WindowsXP, Vista, Linux
- GUI based application for Windows and Linux
  - Allows users to view and modify registers in the 32NT24AG2
  - Binary file generator for programming the serial EEPROMs attached to the SMBUS.

Other

- SMBUS cable/dongle may be required for certain evaluation exercises.
- SMA/SATA connectors are provided on the EB-LOGAN-23 board for clock outputs.

Revision History

March 15, 2010: Initial publication of evaluation board manual.

April 23, 2010: Updated Schematics in Chapter 4.

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August 11, 2010: Updated the manual for Rev. 2.0 board.

February 16, 2011: Changed default settings from Off to On in Tables 2.3 and 2.4.

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Installation of the EB-LOGAN-23 Evaluation Board

Notes

EB-LOGAN-23 Installation

This chapter discusses the steps required to configure and install the EB-LOGAN-23 evaluation board. All available DIP switches and jumper configurations are explained in detail.

The primary installation steps are:

1. Configure jumper/switch options suitable for the evaluation or application requirements.
2. Connect PCI Express endpoint cards to the downstream port PCIe slots on the daughter cards plugged into the evaluation board. Daughter cards are provided by IDT. In some cases the 12-PACK board will be required as well (specifically when more ports than those supported by the main board are required).
3. Make sure that the host system (e.g. server with root complex chipset) is powered off.
4. Connect the evaluation board to the host system via the adapter card and cable provided by IDT.
5. Apply power to the host system and to the IDT board.

The EB-LOGAN-23 board is typically shipped with all jumpers and switches configured to their default settings which will satisfy the initial needs of the majority of the users. In most cases, the board does not require further modification or setup. However, please visit the IDT website and fill out the Technical Support Request form at http://www.idt.com/?app=TechSupport for other configurations.

PCI Express Mezzanine and Edge Adapters

The PCI Express lanes are broken out to four Mezzanine connectors on the EB-LOGAN-23 Evaluation Board. The adapter cards are used to convert Mezzanine connectors into PCI Express slot connector(s) or Internal mini SAS (iSAS) connectors or both. A Bifurcated Mezzanine Card has two mechanical x8 PCIe Slots (x4 electrically) while a Merged Mezzanine Card has single x8 PCIe Slot. Pictured in Figure 2.1.

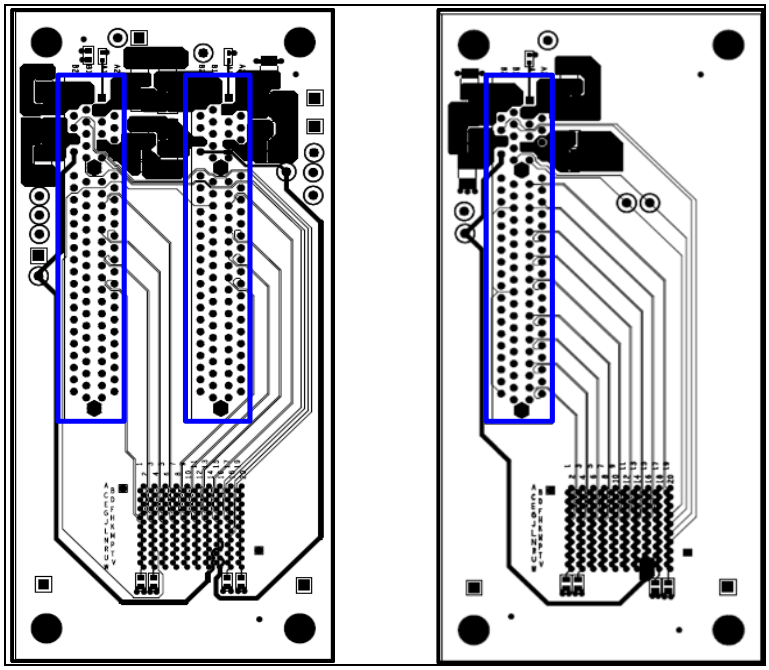


Figure 2.1 Bifurcated and Merged Mezzanine Cards

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Pictured in Figure 2.2 is the mini-SAS Mezzanine card which consists of two iSAS and two SATA connectors. Each iSAS connector supports up to two PCI Express x4 width and the SATA connectors are used for clock and reset signals of each x4 or less stack/port. An iSAS-to-SATA breakout cable shown in Figure 2.3 is used connect from iSAS to edge adapter and/or 12PACK. An iSAS-to-iSAS cable shown in Figure 2.4 is used to connect from iSAS to x8 edge adapter.

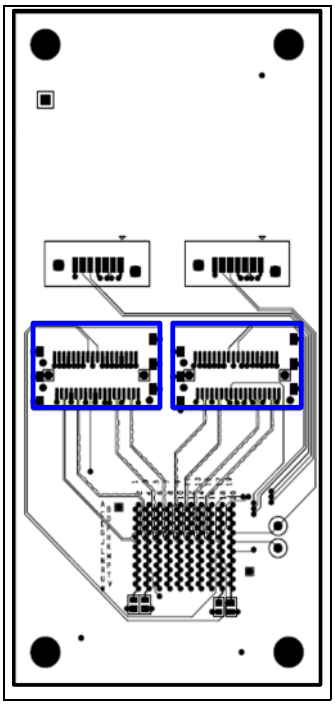


Figure 2.2 MiniSAS Mezzanine Adapter

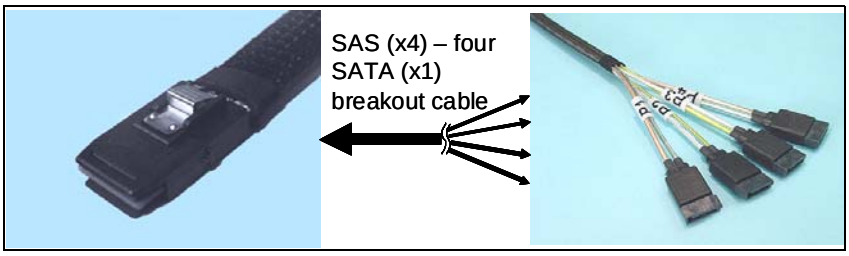


Figure 2.3 EB-LOGAN-23 iSAS-to-SATA Breakout Cable

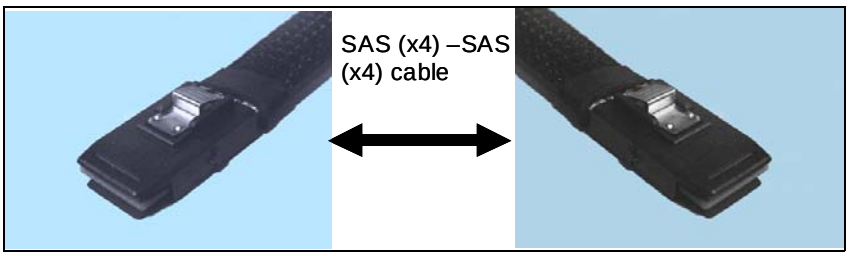


Figure 2.4 EB-LOGAN-23 iSAS-to-iSAS Cable

The PCI Express Edge to SATA Adapter, pictured in Figure 2.5 and Figure 2.6, can be inserted into any physical PCIe slot on a host system and in combination with mini-SAS Mezzanine Card, such as the one in Figure 2.2, to form a link between evaluation main board and the host system. There are 5 SATA connec-

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tors: one connector is for clock and reset, and the remainder support one PICe lane per SATA connector. The PCI Express Edge to SAS Adapter shown in Figure 2.6 is similar to the SATA adapter in that it supports up to a x8 width using two SAS cables. The edge adapters can be inserted into a mechanical x4/x8 or greater slot and supports x1, x2, x4, and x8 widths.

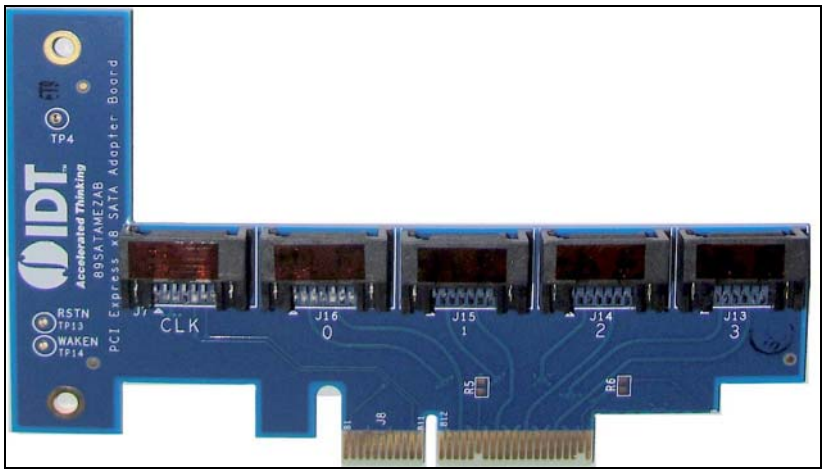


Figure 2.5 PCIe x4 Edge-to-SATA Adapter

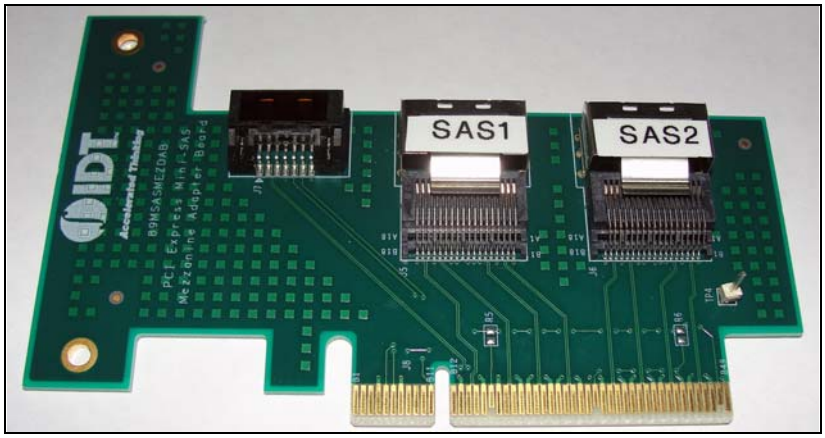


Figure 2.6 PCIe x8 Edge-to-SAS Adapter

Hardware Description

The PES32NT24AG2 is a 32-lane, 24-port PCI Express® switch. It is a peripheral chip that performs PCI Express based switching with a feature set optimized for high performance applications such as servers and storage. It provides fan-out and switching functions between a PCI Express upstream port and downstream ports or peer-to-peer switching between downstream ports. Furthermore, up to eight ports can be configured as NTB ports for multi-root applications. The device offers additional features such as DMA and local port clocking support (a feature required for enabling multiple spread spectrum clocks in the system).

The EB-LOGAN-23 Main Board, shown in Figure 2.7, supports up to 6 PCI Express downstream ports and up to 23 ports when using two 12-PACK Boards.

Basic requirements for the board function are:

- Host system with a PCI Express root complex supporting x8 configuration through a PCI Express x8 slot. (If your host system does not offer a x8 slot, please contact ssdhelp@idt.com for alternative solutions.)
- – x1, x2, x4, or x8 PCI Express Endpoint Cards.

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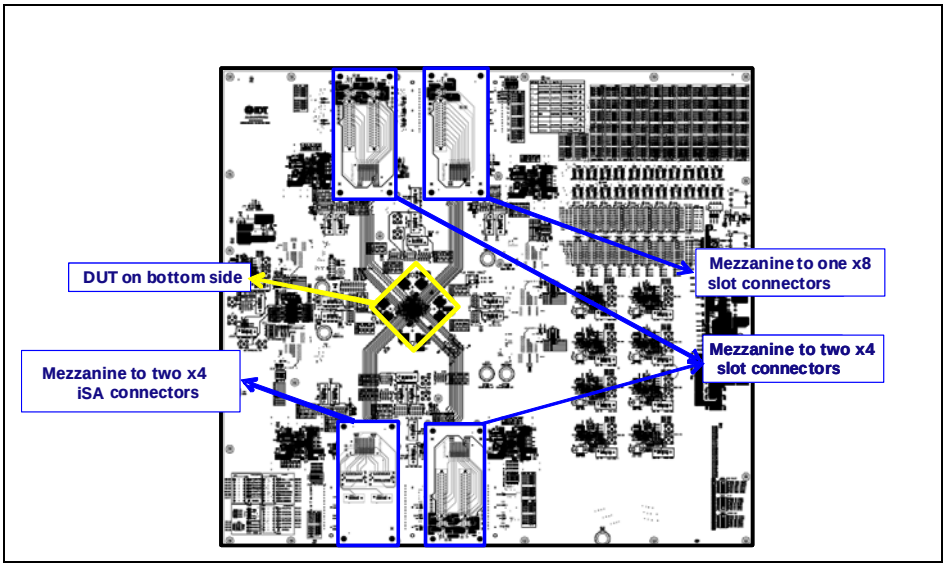


Figure 2.7 EB-LOGAN-23 Evaluation Main Board

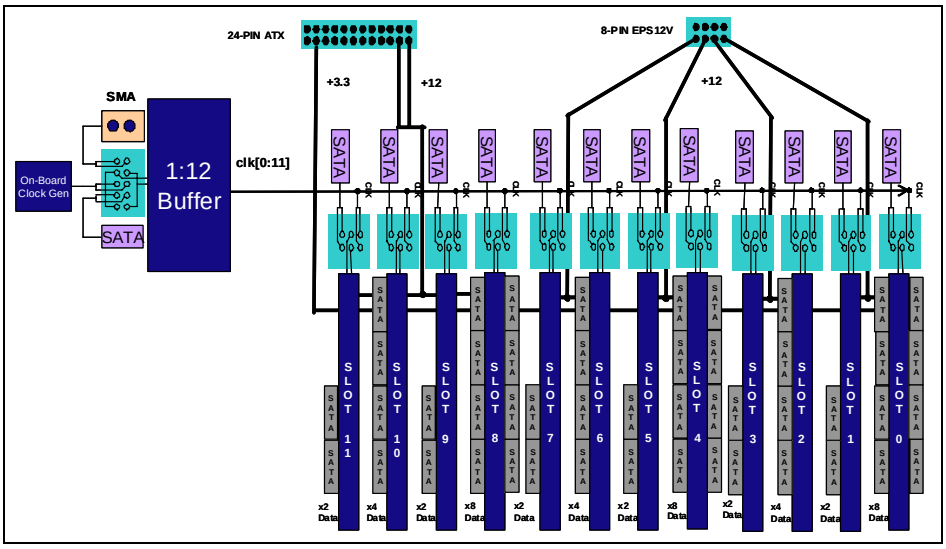


Figure 2.8 12-PACK PCIe Slots Breakout Board

Reference Clocks

Global Reference Input Clocks

The PES32NT24AG2 requires two differential reference clocks. The EB-LOGAN-23 derives these clocks from SMA connectors (J17/J20, J66/J67), clock buffer (U51) with on board clock generator (U49), SMA (J5/J7) or SATA (J8) connectors via jumpers (J6) as described in Table 2.2, or SATA connectors (J21, J22) as described in Table 2.1 and Figures 2.9 and 2.10. Both reference clocks are mandatory and must come from the same reference clock source. The switch will not function normally if only one clock is used.

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Notes

Global Clock#	Jumper	Selection
GCLK0	J18	[1-3 / 2-4] SMA (J66/J67) [5-7 /6-8] From Clock Buffer U51 (default) [7-9 / 8-10] SATA, J21
GCLK1	J19	[1-3 / 2-4] SMA (J17/J20) [5-7 /6-8] From Clock Buffer U51 (default) [7-9 / 8-10] SATA, J22

Table 2.1 EB-LOGAN-23 Global Clock Select

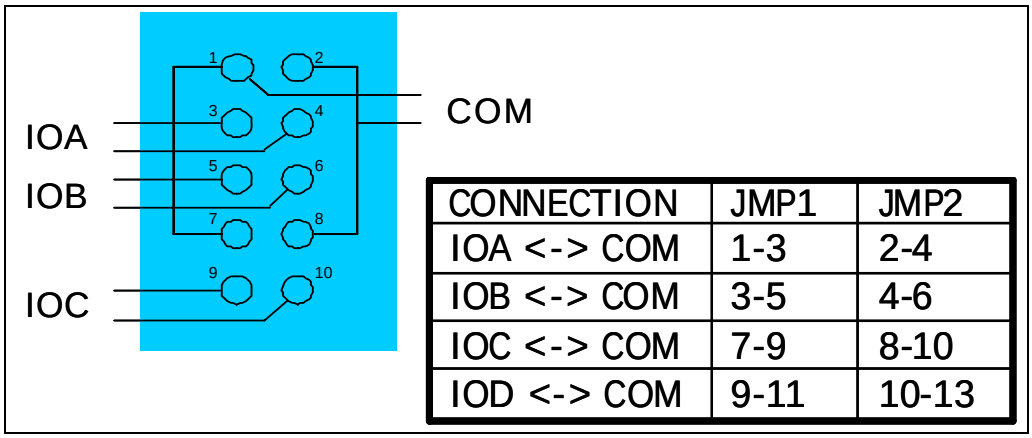


Figure 2.9 Differential Jumper Arrangement Example

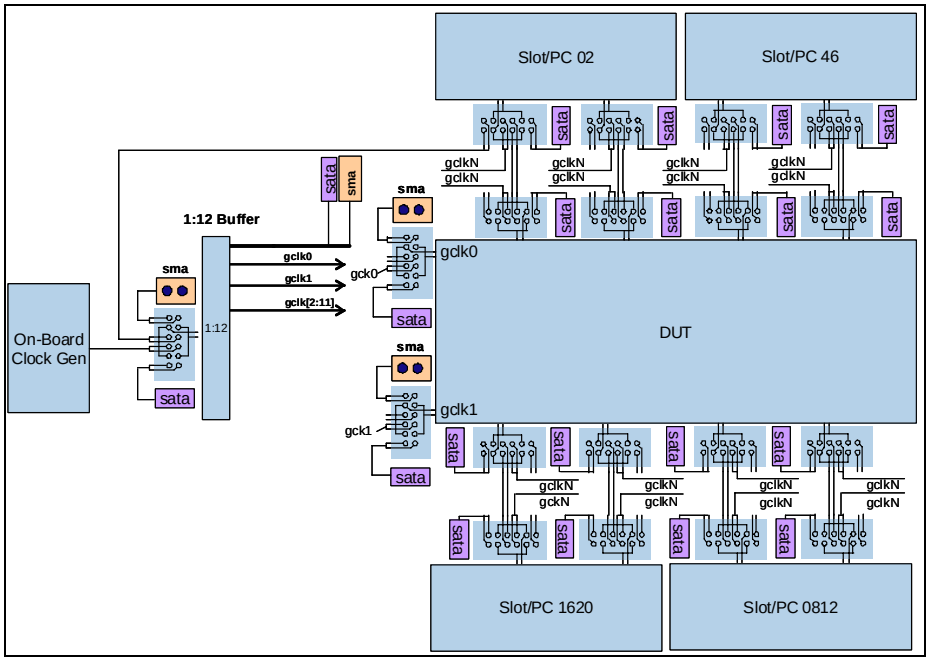


Figure 2.10 Reference Clock Configuration

By default, the clock buffer derives its clock from a common source. The common source can be the host system reference clock via a SATA connector, the onboard clock generator, or SMA connectors. See Table 2.2.

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Notes

Jumper	Selection
J6	[1-3 / 2-4] SMA (J5/J7) [5-7 / 6-8] Onboard Clock Generator (U49) [7-9 / 8-10] SATA (J8) (default)

Table 2.2 Clock Buffer Input Sources

The frequency of the global reference clock input may be either 100 MHz or 125 MHz, as shown in Table 2.3, and is selected by the Clock Frequency Select (GCLKFEL) pin.

Global Clock Frequency Switch - SW10[2]	
SW10[2]	Clock Frequency
ON	100 MHz (Default)
OFF	125 MHz

Table 2.3 Global Reference Input Clock Frequency Select

The source for the onboard clock is the ICS841484 clock generator device (U49) connected to a 25MHz oscillator (X1). When using the onboard clock generator, the output frequency can be selected using ICS_FS (SW10, bit 1). The default setting is ON. See Table 2.4.

Onboard Clock Frequency Switch - SW10[1]	
SW10[1]	Clock Frequency
ON	100 MHz (Default)
OFF	125 MHz

Table 2.4 Onboard Clock Generator Frequency Select

The output of the onboard clock generator is accessible through SMA or SATA connectors. See Table 2.5. This can be used to connect a scope for probing or capturing purposes and cannot be used to drive the clock from an external source.

Onboard Reference Clock Output (Differential)	
TP119	Positive Reference Clock (SMA)
TP120	Negative Reference Clock (SMA)
J121	Differential Reference Clock (SATA)

Table 2.5 Onboard Reference Clock Generator Access Points

Local Port Input Clocks

Associated with some ports is a local port reference clock input (PxCLK). Depending on the port clocking mode, a differential reference clock can be driven into the device on the corresponding PxCLKP and PxCLKN pins. The frequency of a port reference clock input MUST always at 100 MHz. Table 2.6 lists the possible sources for the port reference clock input, and Table 2.9 lists the possible sources for the slot clock input. Additional information on port clocking usage and configuration can be found in the Device User Manuals and in IDT's Application Note AN-715.

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Notes

Port #	Header	Selection
0	J9	[1-3 / 2-4] Onboard Clock Generator (U116) [3-5 / 4-6] SATA (J58)
2	J10	[1-3 / 2-4] Onboard Clock Generator (U122) [3-5 / 4-6] SATA (J59)
4	J11	[1-3 / 2-4] Onboard Clock Generator (U123) [3-5 / 4-6] SATA (J60)
6	J12	[1-3 / 2-4] Onboard Clock Generator (U117) [3-5 / 4-6] SATA (J61)
12	J14	[1-3 / 2-4] Onboard Clock Generator (U119) [3-5 / 4-6] SATA (J63)
20	J16	[1-3 / 2-4] Onboard Clock Generator (U121) [3-5 / 4-6] SATA (J65)

Table 2.6 EB-LOGAN-23 Port (0, 2, 4, 6, 12, 20) Clock Select

Local port clock sources for ports 8 and 16 are selected by DIP switch (S17 and S19) via a clock mux/buffer. See Tables 2.7 and 2.8.

Port 8 Clock Source Select - S19[1]	
S19[1]	Clock Source
OFF	SATA J62
ON	Port 8 Clock Generator (U118)

Table 2.7 EB-LOGAN-23 Port 8 Clock Source Select

Port 16 Clock Source Select - S17[1]	
S17[1]	Clock Source
OFF	SATA J64
ON	Port 16 Clock Generator (U120)

Table 2.8 EB-LOGAN-23 Port 16 Clock Source Select

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Notes

Slot #	Jumper	Selection
0	J23	[1-3 / 2-4] Onboard Clock Generator (U115) [3-5 / 4-6] Clock Buffer (U51) [7-9 / 8-10] P08CLK Clock Mux (U18) [9-11 / 10-12] SATA (J27)
2	J24	[1-3 / 2-4] Onboard Clock Generator (U122) [3-5 / 4-6] Clock Buffer (U51) [7-9 / 8-10] P08CLK Clock Mux (U18) [9-11 / 10-12] SATA (J28)
4	J25	[1-3 / 2-4] Onboard Clock Generator (U123) [3-5 / 4-6] Clock Buffer (U51) [7-9 / 8-10] P08CLK Clock Mux (U18) [9-11 / 10-12] SATA (J29)
6	J26	[1-3 / 2-4] Onboard Clock Generator (U117) [3-5 / 4-6] Clock Buffer (U51) [7-9 / 8-10] P16CLK Clock Mux (U16) [9-11 / 10-12] SATA (J30)
8	J31	[1-3 / 2-4] Onboard Clock Generator (U118) [3-5 / 4-6] Clock Buffer (U51) [7-9 / 8-10] P16CLK Clock Mux (U16) [9-11 / 10-12] SATA (J31)
12	J32	[1-3 / 2-4] Onboard Clock Generator (U119) [3-5 / 4-6] Clock Buffer (U51) [7-9 / 8-10] P16CLK Clock Mux (U16) [9-11 / 10-12] SATA (J32)
16	J33	[1-3 / 2-4] Onboard Clock Generator (U120) [3-5 / 4-6] Clock Buffer (U51) [7-9 / 8-10] P08CLK Clock Mux (U18) [9-11 / 10-12] SATA (J33)
20	J34	[1-3 / 2-4] Onboard Clock Generator (U121) [3-5 / 4-6] Clock Buffer (U51) [7-9 / 8-10] P16CLK Clock Mux (U16) [9-11 / 10-12] SATA (J34)

Table 2.9 EB-LOGAN-23 Slot Clock Select

CLKMODE Selection

All ports in the PES32NT24AG2 device (upstream and downstream) use global clocked mode by default. The port clocking mode of a port is determined by the state of the CLKMODE[1:0] pins in the boot configuration vector as shown in Table 2.10. This field determines the initial value of the Slot Clock Configuration (SCLK) field in each port's PCI Express Link Status (PCIELSTS) register. The SCLK field controls the advertisement of whether or not the port uses the same reference clock source as the link partner. A one in the SCLK field indicates that the port and its link partner use the same reference clock source. This is defined as Common Clock Configuration by the PCI Express Base Specification. A zero in the SCLK field indicates that the port and its link partner do not use the same reference clock source.

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Notes

SW10[8] CLKMODE[0]	SW10[7] CLKMODE[1]	Port 0 SCLK	Port[15:1] SCLK
ON	ON	0	0
OFF	ON	1	0
ON	OFF	0	1
OFF	OFF	1	1

Table 2.10 CLKMODE Selection for the PES32NT24AG2

Power Sources

Power for the PES32NT24AG2 and all downstream ports is generated from a 12V supply via an external power connector. See Table 2.11. A 12V to 3.3V DC-DC converter is used to provide power to five switching regulators to generate V_{DD}CORE, V_{DD}PEA, V_{DD}PETA, V_{DD}PEHA, and V_{DD}IO voltages. The 3.3V from the DC-DC converter will be used to power the clock buffers and circuitries.

The external power supply connectors are 24-pin (J69) and 8-pin (J68) molex connectors as described in Tables 2.11 and 2.12. The +12V3 is used to power the PES32NT24AG2 and downstream slots 0, 2, 16, and 20. The +12V2 is used to power downstream slots 4, 6, 8, and 12.

Pin	Signal	Pin	Signal
1	+3.3V	13	+3.3V
2	+3.3V	14	-12V
3	GND	15	GND
4	+5V	16	PS_ON
5	GND	17	GND
6	+5V	18	GND
7	GND	19	GND
8	PWR_OK	20	NC
9	5VSB	21	+5V
10	+12V3	22	+5V
11	+12V3	23	+5V
12	+3.3V	24	GND

Table 2.11 EPS12V 24-pin Power Connector - J69

Pin	Signal	Pin	Signal
1	GND	5	+12V1
2	GND	6	+12V1
3	GND	7	+12V2
4	GND	8	+12V2

Table 2.12 EPS12V 8-Pin Connector - J68

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Notes

The power switch located at S1 can be used to control the supply power from the external power supply connector. Add a shunt to W27 to enable power on switch.

PCI Express Analog Power Voltage Regulator

A voltage regulator (U65) provides a 2.5V PCI Express analog power voltage (shown as VDDPEHA) to the PES32NT24AG2.

PCI Express Digital Power Voltage Converter

A separate voltage regulator (U62) provides a 1.0V PCI Express analog power voltage (shown as VDDPEA) to the PES32NT24AG2.

PCI Express Transmitter Analog Voltage Converter

A separate voltage regulator (U68) provides a 1.0V PCI Express transmitter analog voltage (shown as VDDPETA) to the PES32NT24AG2.

Core Logic Voltage Converter

A separate voltage regulator (U59) provides the 1.0V core voltage (VDDCORE) to the PES32NT24AG2.

3.3V I/O Voltage Regulator

A separate voltage regulator (U56) provides the 3.3V I/O voltage (VDDIO) to the PES32NT24AG2.

Power-up Sequence for PES32NT24AG2

During power supply ramp-up, VDDCORE must remain at least 1.0V below VDDIO at all times. There are no other power-up sequence requirements for the various operating supply voltages.

Heatsink Requirement

The EB-LOGAN-23 evaluation board utilizes a heatsink with integrated fan. All initial shipments of the board are made with the heatsink whether or not one is truly required. There may be low link usage applications within which the heatsink may, in fact, not be required.

Reset

The PES32NT24AG2 supports two types of reset mechanisms as described in the PCI Express specification:

- Fundamental Reset: This is a system-generated reset that propagates along the PCI Express tree through a single side-band signal PERST# which is connected to the Root Complex, the PES32NT24AG2, and the endpoints.
- Hot Reset: This is an In-band Reset, communicated downstream via a link from one device to another. Hot Reset may be initiated by software. This is further discussed in the PES32NT24xG2 User Manual. The EB-LOGAN-23 evaluation board provides seamless support for Hot Reset.

Fundamental Reset

There are two types of Fundamental Resets which may occur on the EB-LOGAN-23 evaluation board:

- Cold Reset: During initial power-on, the onboard voltage monitor (TLC7733D) will assert the PCI Express Reset (PERSTN) input pin of the PES32NT24AG2.
- Warm Reset: This is triggered by hardware while the device is powered on. Warm Reset can be initiated by two methods:
  - *Pressing a push-button switch (S3) located on EB-LOGAN-23 board*
  - *The host system board IO Controller Hub asserting PERST# signal, which propagates through the PCIe upstream edge connector of the EB-LOGAN-23.*

  Both events cause the onboard voltage monitor (TLC7733D) to assert the PCI Express Reset (PERSTN) input of the PES32NT24AG2 while power is on.

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Notes

Downstream Reset

Single Partition Mode without Hot Plug:

When the evaluation board initially powers on, it assumes the following:

- The switch is configured in single partition mode.
- Slot 0 is the root port and controls the downstream port resets.
- Ports 1-23 are downstream ports.
- Hot Plug is disabled.

The following behavior should be observed:

- The resets to slots 1-23 should initially be asserted and remain this way until after the fundamental reset is initially de-asserted.
- The assertion of slot 0 reset should propagate to slots 1-23.

Stack Configuration

The PES32NT24AG2 contains four stack blocks labeled Stack 0, Stack 1, Stack 2, and Stack 3. Stacks 0 and 1 have four x2 ports each, and stacks 2 and 3 have eight x1 ports each. This provides a total of 24 ports in the device labeled port 0 through port 23. Table 2.13 lists the ports associated with each stack.

Stack	Ports Associated with the Stack
Stack 0	0, 1, 2, 3
Stack 1	4, 5, 6, 7
Stack 2	8, 9, 10, 11, 12, 13, 14, 15
Stack 3	16, 17, 18, 19, 20, 21, 22, 23

Table 2.13 Ports in Each Stack

Boot Configuration Vector

A boot configuration vector consisting of the signals listed in Table 2.14 is sampled by the PES32NT24AG2 during a fundamental reset (while PERSTN is active). The boot configuration vector defines the essential parameters for switch operation and is set using DIP switches S5, SW8, SW9, and SW10 as defined in Table 2.15.

Signal	Description
GCLKFSEL	**Global Clock Frequency Select.** This pin specifies the frequency of the GCLKP and GCLKN signals. **Default: low**
CLKMODE[1:0]	**Clock Mode.** These pins specify the clocking mode used by switch ports. See Table 2.10 for a definition of the encoding of these signals. The value of these signals may be overridden by modifying the Port Clocking Mode (PCLKMODE) register.
RSTHALT	**Reset Halt.** When this pin is asserted during a switch fundamental reset sequence, the switch remains in a quasi-reset state with the Master and Slave SMBuses active. This allows software to read and write registers internal to the device before normal device operation begins. The device exits the quasi-reset state when the RSTHALT bit is cleared in the SWCTL register by an SMBus master. Refer to section Switch Fundamental Reset on page 3-2 for further details. **Default: low**
SSMBADDR[2:1]	**Slave SMBus Address.** SMBus address of the switch on the slave SMBus. **Default: 0x3**

Table 2.14 Boot Configuration Vector Signals (Part 1 of 2)

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Notes

Signal	Description
SWMODE[3:0]	Switch Mode. These pins specify the switch operating mode.
STK0CFG[1:0]	Stack 0 Configuration. These pins select the configuration of stack 0 during a switch fundamental reset.
STK1CFG[1:0]	Stack 1 Configuration. These pins select the configuration of stack 1 during a switch fundamental reset.
STK2CFG[4:0]	Stack 2 Configuration. These pins select the configuration of stack 2 during a switch fundamental reset.
STK3CFG[4:0]	Stack 3 Configuration. These pins select the configuration of stack 3 during a switch fundamental reset.

Table 2.14 Boot Configuration Vector Signals (Part 2 of 2)

Location	Signal	Default
SW10[2]	GCLKFSEL	ON
SW10[4]	RSTHALT	ON
SW10[5]	SSMBADDR[2]	OFF
SW10[6]	SSMBADDR[1]	OFF

Table 2.15 Boot Configuration Vector Switch SW10

SMBus Interfaces

The System Management Bus (SMBus) is a two-wire interface through which various system component chips can communicate. It is based on the principles of operation of I^2C. Implementation of the SMBus signals in the PCI Express connector is optional and may not be present on the host system. The SMBus interface consists of an SMBus clock pin and an SMBus data pin.

The PES32NT24AG2 contains two SMBus interfaces: a slave SMBus interface and a master SMBus interface. The slave SMBus interface allows a SMBus Master device full access to all software-visible registers. The Master SMBus interface provides a connection to the external serial EEPROM used for initialization and the I/O expanders used for hot-plug signals.

SMBus Slave Interface

On the PES32NT24AG2 board, the slave SMBus interface is accessible through a 4-pin header as described in Table 2.16.

.

Slave SMBus Interface Connector J71	
Pin	Signal
1	SDA
2	GND
3	SCL
4	NC

Table 2.16 Slave SMBus Interface Connector

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Notes

For a fixed address, the SMBus address of the PES32NT24AG2 slave interface is 0b1110111 by default and is configurable using DIP Switches SW10[5] and SW10[6] as described in Table 2.17.

Slave Interface Address Configuration	
Address Bit	Signal
1	SSMBUSADDR[1]
2	SSMBUSADDR[2]
3	1
4	0
5	1
6	1
7	1

Table 2.17 SMBus Slave Interface Address Configuration

The slave SMBus interface responds to the following SMBus transactions initiated by an SMBus master. Initiation of any SMBus transaction other than those listed above produces undefined results. See the SMBus 2.0 specification for a detailed description of the following transactions:

- Byte and Word Write/Read
- Block Write/Read

SMBus Master Interface

Connected to the master SMBus interface are twenty-two 16-bit I/O Expanders (MAX7311AUG) and a serial EEPROM, U77 (24LC512). The I/O Expanders are used as the interface for the onboard hot-plug controllers (MIC2591B). The lower three bits of the bus address for the I/O Expander 0 through 20 are fixed through the stuffing resistor as 0x20, 0x22, 0x24, 0x26, 0x28, 0x2A, 0x2C, 0x2E, 0x50, 0x52, x54, 0x56, 0x58, 0x5A, 0x5C, 0x5E, 0xB0, 0xA2, 0xA4, 0xA6, 0xA8, and 0xAA, respectively.

Note: Hot-plug is not implemented when the PES32NT24AG2 is installed.

The seven bits address for the selected EEPROM device is fixed at **0b1010_000** by default.

JTAG Header

The PES32NT24AG2 provides a JTAG connector J73 for access to the PES32NT24AG2 JTAG interface. The connector is a 2.54 x 2.54 mm pitch male 14-pin connector. Refer to Table 2.18 for the JTAG Connector J73 pin out.

JTAG Connector J5					
Pin	Signal	Direction	Pin	Signal	Direction
1	/TRST - Test reset	Input	2	GND	—
3	TDI - Test data	Input	4	GND	—
5	TDO - Test data	Output	6	GND	—
7	TMS - Test mode select	Input	8	GND	—
9	TCK - Test clock	Input	10	GND	—
11	3.3V		12	N/C	—
13	GND	—	14	3.3V	

Table 2.18 JTAG Connector Pin Out

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Notes

Miscellaneous Jumpers, Headers

Miscellaneous Jumpers, Headers			
Ref. Designator	Type	Default	Description
W1	Header	1-2 Shunted	1-2: GPIO 8 to DS414 when ALT1 (Default) 2-3: GPIO 8 to IO Expander Interrupt when ALT0
W5	Header	Shunted	2-3: Slot 0, 3.3Vaux source from Direct Power (Default) 1-2: Slot 0, 3.3Vaux source from hot-plug controller
W6	Header	2-3 Shunted	2-3: Slot 2, 3.3Vaux source from Direct Power (Default) 1-2: Slot 2, 3.3Vaux source from hot-plug controller
W11	Header	2-3 Shunted	2-3: Slot 4, 3.3Vaux source from Direct Power (Default) 1-2: Slot 4, 3.3Vaux source from hot-plug controller
W12	Header	2-3 Shunted	2-3: Slot 6, 3.3Vaux source from Direct Power (Default) 1-2: Slot 6, 3.3Vaux source from hot-plug controller
W17	Header	2-3 Shunted	2-3: Slot 8, 3.3Vaux source from Direct Power (Default) 1-2: Slot 8, 3.3Vaux source from hot-plug controller
W18	Header	2-3 Shunted	2-3: Slot 12, 3.3Vaux source from Direct Power (Default) 1-2: Slot 12, 3.3Vaux source from hot-plug controller
W23	Header	2-3 Shunted	2-3: Slot 16, 3.3Vaux source from Direct Power (Default) 1-2: Slot 16, 3.3Vaux source from hot-plug controller
W24	Header	2-3 Shunted	2-3: Slot 20, 3.3Vaux source from Direct Power (Default) 1-2: Slot 20, 3.3Vaux source from hot-plug controller
W4	Header	2-3 Shunted	2-3: Slot 0, +12V source from Direct Power (Default) 1-2: Slot 0, +12V source from hot-plug controller
W8	Header	2-3 Shunted	2-3: Slot 2, +12V source base on W57(Default) 1-2: Slot 2, +12V source from hot-plug controller
W10	Header	2-3 Shunted	2-3: Slot 4, +12V source from Direct Power (Default) 1-2: Slot 4, +12V source from hot-plug controller
W14	Header	2-3 Shunted	2-3: Slot 6, +12V source from Direct Power (Default) 1-2: Slot 6, +12V source from hot-plug controller
W16	Header	2-3 Shunted	2-3: Slot 8, +12V source from Direct Power (Default) 1-2: Slot 8, +12V source from hot-plug controller
W20	Header	2-3 Shunted	2-3: Slot 12, +12V source from Direct Power (Default) 1-2: Slot 12, +12V source from hot-plug controller
W22	Header	2-3 Shunted	2-3: Slot 16, +12V source from Direct Power (Default) 1-2: Slot 16, +12V source from hot-plug controller
W26	Header	2-3 Shunted	2-3: Slot 20, +12V source from Direct Power (Default) 1-2: Slot 20, +12V source from hot-plug controller
W3	Header	2-3 Shunted	2-3: Slot 0, +3.3V source from Direct Power (Default) 1-2: Slot 0, +3.3V source from hot-plug controller
W7	Header	2-3 Shunted	2-3: Slot 2, +3.3V source from Direct Power (Default) 1-2: Slot 2, +3.3V source from hot-plug controller
W9	Header	2-3 Shunted	2-3: Slot 4, +3.3V source from Direct Power (Default) 1-2: Slot 4, +3.3V source from hot-plug controller

Table 2.19 Miscellaneous Jumpers, Headers (Part 1 of 2)

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Notes

Miscellaneous Jumpers, Headers			
Ref. Designator	Type	Default	Description
W13	Header	2-3 Shunted	2-3: Slot 6, +3.3V source from Direct Power (Default) 1-2: Slot 6, +3.3V source from hot-plug controller
W15	Header	2-3 Shunted	2-3: Slot 8, +3.3V source from Direct Power (Default) 1-2: Slot 8, +3.3V source from hot-plug controller
W19	Header	2-3 Shunted	2-3: Slot 12, +3.3V source from Direct Power (Default) 1-2: Slot 12, +3.3V source from hot-plug controller
W21	Header	2-3 Shunted	2-3: Slot 16, +3.3V source from Direct Power (Default) 1-2: Slot 16, +3.3V source from hot-plug controller
W25	Header	2-3 Shunted	2-3: Slot 20, +3.3V source from Direct Power (Default) 1-2: Slot 20, +3.3V source from hot-plug controller

Table 2.19 Miscellaneous Jumpers, Headers (Part 2 of 2)

LEDs

There are many LED indicators on the EB-LOGAN-23 which convey status feedback. A description of each is provided in Table 2.20.

Location	Color	Definition
DS1	Green	Board Power Indicator (5V)
DS2	Green	Board Power Indicator (3.3V)
DS4	Green	VDDIO Indicator (3.3V)
DS158	Orange	Port23: Attention Push Button Input
DS159	Orange	Port22: Attention Push Button Input
DS160	Orange	Port21: Attention Push Button Input
DS161	Orange	Port20: Attention Push Button Input
DS162	Orange	Port19: Attention Push Button Input
DS163	Orange	Port18: Attention Push Button Input
DS164	Orange	Port17: Attention Push Button Input
DS165	Orange	Port16: Attention Push Button Input
DS166	Orange	Port15: Attention Push Button Input
DS167	Orange	Port14: Attention Push Button Input
DS168	Orange	Port13: Attention Push Button Input
DS169	Orange	Port12: Attention Push Button Input
DS170	Orange	Port11: Attention Push Button Input
DS171	Orange	Port10: Attention Push Button Input
DS172	Orange	Port9: Attention Push Button Input
DS173	Orange	Port8: Attention Push Button Input

Table 2.20 LED Indicators (Part 1 of 8)

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Notes

Location	Color	Definition
DS174	Orange	Port7: Attention Push Button Input
DS175	Orange	Port6: Attention Push Button Input
DS176	Orange	Port5: Attention Push Button Input
DS177	Orange	Port4: Attention Push Button Input
DS178	Orange	Port3: Attention Push Button Input
DS179	Orange	Port2: Attention Push Button Input
DS180	Orange	Port1: Attention Push Button Input
DS181	Orange	Port0: Attention Push Button Input
DS182	Yellow	Port23: Presence Detect Input
DS183	Yellow	Port22: Presence Detect Input
DS184	Yellow	Port21: Presence Detect Input
DS185	Yellow	Port20: Presence Detect Input
DS186	Yellow	Port19: Presence Detect Input
DS187	Yellow	Port18: Presence Detect Input
DS188	Yellow	Port17: Presence Detect Input
DS189	Yellow	Port16: Presence Detect Input
DS190	Yellow	Port15: Presence Detect Input
DS191	Yellow	Port14: Presence Detect Input
DS192	Yellow	Port13: Presence Detect Input
DS193	Yellow	Port12: Presence Detect Input
DS194	Yellow	Port11: Presence Detect Input
DS195	Yellow	Port10: Presence Detect Input
DS196	Yellow	Port9: Presence Detect Input
DS197	Yellow	Port8: Presence Detect Input
DS198	Yellow	Port7: Presence Detect Input
DS199	Yellow	Port6: Presence Detect Input
DS200	Yellow	Port5: Presence Detect Input
DS201	Yellow	Port4: Presence Detect Input
DS202	Yellow	Port3: Presence Detect Input
DS203	Yellow	Port2: Presence Detect Input
DS204	Yellow	Port1: Presence Detect Input
DS205	Yellow	Port0: Presence Detect Input
DS5	Red	Port23: Power Fault Input
DS6	Red	Port22: Power Fault Input
DS7	Red	Port21: Power Fault Input
DS8	Red	Port20: Power Fault Input
DS9	Red	Port19: Power Fault Input

Table 2.20 LED Indicators (Part 2 of 8)

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Notes

Location	Color	Definition
DS10	Red	Port18: Power Fault Input
DS11	Red	Port17: Power Fault Input
DS12	Red	Port16: Power Fault Input
DS13	Red	Port15: Power Fault Input
DS14	Red	Port14: Power Fault Input
DS15	Red	Port13: Power Fault Input
DS16	Red	Port12: Power Fault Input
DS17	Red	Port11: Power Fault Input
DS18	Red	Port10: Power Fault Input
DS19	Red	Port9: Power Fault Input
DS20	Red	Port8: Power Fault Input
DS21	Red	Port7: Power Fault Input
DS22	Red	Port6: Power Fault Input
DS23	Red	Port5: Power Fault Input
DS24	Red	Port4: Power Fault Input
DS25	Red	Port3: Power Fault Input
DS26	Red	Port2: Power Fault Input
DS27	Red	Port1: Power Fault Input
DS28	Red	Port0: Power Fault Input
DS29	Green	Port23: Power Good Input
DS30	Green	Port22: Power Good Input
DS31	Green	Port21: Power Good Input
DS32	Green	Port20: Power Good Input
DS33	Green	Port19: Power Good Input
DS34	Green	Port18: Power Good Input
DS35	Green	Port17: Power Good Input
DS36	Green	Port16: Power Good Input
DS37	Green	Port15: Power Good Input
DS38	Green	Port14: Power Good Input
DS39	Green	Port13: Power Good Input
DS40	Green	Port12: Power Good Input
DS41	Green	Port11: Power Good Input
DS42	Green	Port10: Power Good Input
DS43	Green	Port9: Power Good Input
DS44	Green	Port8: Power Good Input
DS45	Green	Port7: Power Good Input
DS46	Green	Port6: Power Good Input

Table 2.20 LED Indicators (Part 3 of 8)

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Notes

Location	Color	Definition
DS47	Green	Port5: Power Good Input
DS48	Green	Port4: Power Good Input
DS49	Green	Port3: Power Good Input
DS50	Green	Port2: Power Good Input
DS51	Green	Port1: Power Good Input
DS52	Green	Port0: Power Good Input
DS206	Orange	Port23: Attention Indicator Output
DS207	Orange	Port22: Attention Indicator Output
DS208	Orange	Port21: Attention Indicator Output
DS209	Orange	Port20: Attention Indicator Output
DS210	Orange	Port19: Attention Indicator Output
DS211	Orange	Port18: Attention Indicator Output
DS212	Orange	Port17: Attention Indicator Output
DS213	Orange	Port16: Attention Indicator Output
DS214	Orange	Port15: Attention Indicator Output
DS215	Orange	Port14: Attention Indicator Output
DS216	Orange	Port13: Attention Indicator Output
DS217	Orange	Port12: Attention Indicator Output
DS218	Orange	Port11: Attention Indicator Output
DS219	Orange	Port10: Attention Indicator Output
DS220	Orange	Port9: Attention Indicator Output
DS221	Orange	Port8: Attention Indicator Output
DS222	Orange	Port7: Attention Indicator Output
DS223	Orange	Port6: Attention Indicator Output
DS224	Orange	Port5: Attention Indicator Output
DS225	Orange	Port4: Attention Indicator Output
DS226	Orange	Port3: Attention Indicator Output
DS227	Orange	Port2: Attention Indicator Output
DS228	Orange	Port1: Attention Indicator Output
DS229	Orange	Port0: Attention Indicator Output
DS230	Green	Port23: Power Indicator Output
DS231	Green	Port22: Power Indicator Output
DS232	Green	Port21: Power Indicator Output
DS233	Green	Port20: Power Indicator Output
DS234	Green	Port19: Power Indicator Output
DS235	Green	Port18: Power Indicator Output
DS236	Green	Port17: Power Indicator Output

Table 2.20 LED Indicators (Part 4 of 8)

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Notes

Location	Color	Definition
DS237	Green	Port16: Power Indicator Output
DS238	Green	Port15: Power Indicator Output
DS239	Green	Port14: Power Indicator Output
DS240	Green	Port13: Power Indicator Output
DS241	Green	Port12: Power Indicator Output
DS242	Green	Port11: Power Indicator Output
DS243	Green	Port10: Power Indicator Output
DS244	Green	Port9: Power Indicator Output
DS245	Green	Port8: Power Indicator Output
DS246	Green	Port7: Power Indicator Output
DS247	Green	Port6: Power Indicator Output
DS248	Green	Port5: Power Indicator Output
DS249	Green	Port4: Power Indicator Output
DS250	Green	Port3: Power Indicator Output
DS251	Green	Port2: Power Indicator Output
DS252	Green	Port1: Power Indicator Output
DS253	Green	Port0: Power Indicator Output
DS53	Green	Port23: Power Enable Output
DS54	Green	Port22: Power Enable Output
DS55	Green	Port21: Power Enable Output
DS56	Green	Port20: Power Enable Output
DS57	Green	Port19: Power Enable Output
DS58	Green	Port18: Power Enable Output
DS59	Green	Port17: Power Enable Output
DS60	Green	Port16: Power Enable Output
DS61	Green	Port15: Power Enable Output
DS62	Green	Port14: Power Enable Output
DS63	Green	Port13: Power Enable Output
DS64	Green	Port12: Power Enable Output
DS65	Green	Port11: Power Enable Output
DS66	Green	Port10: Power Enable Output
DS67	Green	Port9: Power Enable Output
DS68	Green	Port8: Power Enable Output
DS69	Green	Port7: Power Enable Output
DS70	Green	Port6: Power Enable Output
DS71	Green	Port5: Power Enable Output
DS72	Green	Port4: Power Enable Output

Table 2.20 LED Indicators (Part 5 of 8)

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Notes

Location	Color	Definition
DS73	Green	Port3: Power Enable Output
DS74	Green	Port2: Power Enable Output
DS75	Green	Port1: Power Enable Output
DS76	Green	Port0: Power Enable Output
DS77	Red	Slot 23 Reset Output
DS78	Red	Slot 22 Reset Output
DS79	Red	Slot 21 Reset Output
DS80	Red	Slot 20 Reset Output
DS81	Red	Slot 19 Reset Output
DS82	Red	Slot 18 Reset Output
DS83	Red	Slot 17 Reset Output
DS84	Red	Slot 16 Reset Output
DS85	Red	Slot 15 Reset Output
DS86	Red	Slot 14 Reset Output
DS87	Red	Slot 13 Reset Output
DS88	Red	Slot 12 Reset Output
DS89	Red	Slot 11 Reset Output
DS90	Red	Slot 10 Reset Output
DS91	Red	Slot 9 Reset Output
DS92	Red	Slot 8 Reset Output
DS93	Red	Slot 7 Reset Output
DS94	Red	Slot 6 Reset Output
DS95	Red	Slot 5 Reset Output
DS96	Red	Slot 4 Reset Output
DS97	Red	Slot 3 Reset Output
DS98	Red	Slot 2 Reset Output
DS99	Red	Slot 1 Reset Output
DS100	Red	Slot 0 Reset Output
DS326	Red	Partition 7 Fundamental Reset Input
DS327	Red	Partition 6 Fundamental Reset Input
DS328	Red	Partition 5 Fundamental Reset Input
DS329	Red	Partition 4 Fundamental Reset Input
DS330	Red	Partition 3 Fundamental Reset Input
DS331	Red	Partition 2 Fundamental Reset Input
DS332	Red	Partition 1 Fundamental Reset Input
DS333	Red	Partition 0 Fundamental Reset Input
DS415	Red	Slot 20 Reset Header (J131)

Table 2.20 LED Indicators (Part 6 of 8)

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Notes

Location	Color	Definition
DS416	Red	Slot 16 Reset Header (J130)
DS417	Red	Slot 12 Reset Header (J129)
DS418	Red	Slot 4 Reset Header (J125)
DS419	Red	Slot 6 Reset Header (J128)
DS420	Red	Slot 4 Reset Header (J127)
DS421	Red	Slot 2 Reset Header (J126)
DS422	Red	Slot 0 Reset Header (J125)
DS334	Green	Port23: Link Up Status Output
DS335	Green	Port22: Link Up Status Output
DS336	Green	Port21: Link Up Status Output
DS337	Green	Port20: Link Up Status Output
DS338	Green	Port19: Link Up Status Output
DS339	Green	Port18: Link Up Status Output
DS340	Green	Port17: Link Up Status Output
DS341	Green	Port16: Link Up Status Output
DS342	Green	Port15: Link Up Status Output
DS343	Green	Port14: Link Up Status Output
DS344	Green	Port13: Link Up Status Output
DS345	Green	Port12: Link Up Status Output
DS346	Green	Port11: Link Up Status Output
DS347	Green	Port10: Link Up Status Output
DS348	Green	Port9: Link Up Status Output
DS349	Green	Port8: Link Up Status Output
DS350	Green	Port7: Link Up Status Output
DS351	Green	Port6: Link Up Status Output
DS352	Green	Port5: Link Up Status Output
DS353	Green	Port4: Link Up Status Output
DS354	Green	Port3: Link Up Status Output
DS355	Green	Port2: Link Up Status Output
DS356	Green	Port1: Link Up Status Output
DS357	Green	Port0: Link Up Status Output
DS358	Blue	Port23: Link Activity Status Output
DS359	Blue	Port22: Link Activity Status Output
DS360	Blue	Port21: Link Activity Status Output
DS361	Blue	Port20: Link Activity Status Output
DS362	Blue	Port19: Link Activity Status Output
DS363	Blue	Port18: Link Activity Status Output

Table 2.20 LED Indicators (Part 7 of 8)

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Notes

Location	Color	Definition
DS364	Blue	Port17: Link Activity Status Output
DS365	Blue	Port16: Link Activity Status Output
DS366	Blue	Port15: Link Activity Status Output
DS367	Blue	Port14: Link Activity Status Output
DS368	Blue	Port13: Link Activity Status Output
DS369	Blue	Port12: Link Activity Status Output
DS370	Blue	Port11: Link Activity Status Output
DS371	Blue	Port10: Link Activity Status Output
DS372	Blue	Port9: Link Activity Status Output
DS373	Blue	Port8: Link Activity Status Output
DS374	Blue	Port7: Link Activity Status Output
DS375	Blue	Port6: Link Activity Status Output
DS376	Blue	Port5: Link Activity Status Output
DS377	Blue	Port4: Link Activity Status Output
DS378	Blue	Port3: Link Activity Status Output
DS379	Blue	Port2: Link Activity Status Output
DS380	Blue	Port1: Link Activity Status Output
DS381	Blue	Port0: Link Activity Status Output

Table 2.20 LED Indicators (Part 8 of 8)

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Notes

EB-LOGAN-23 Board Figure

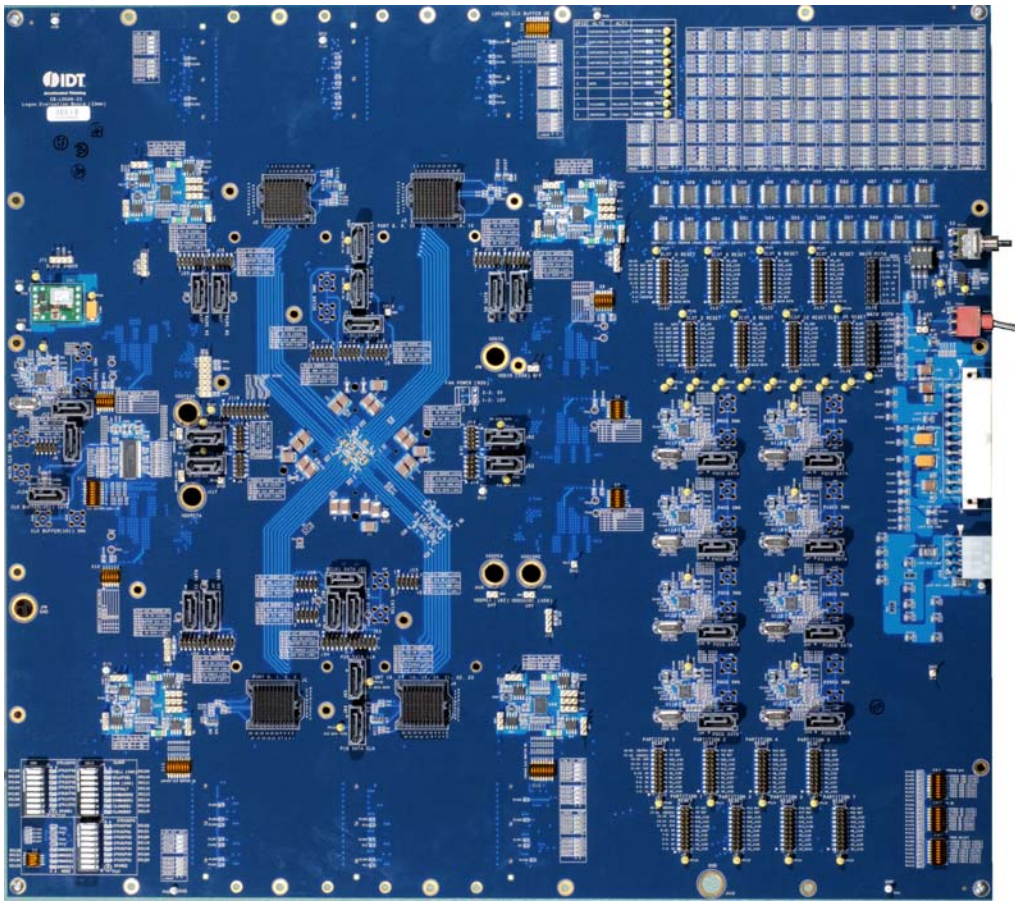


Figure 2.11 EB32NT24AG2 Evaluation Board

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Notes

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Software For EB-LOGAN-23

Notes

Introduction

This chapter discusses some of the main features of the available software to give users a better understanding of what can be achieved with the EB-LOGAN-23 evaluation board using the device management software.

Device management software and related user documentation are available on a CD which is included in the Evaluation Board Kit. This information is also available on IDT FTP site and also at my.idt.com. For more information, please go to: http://www.idt.com/?app=TechSupport&prodFamily=PCIe%20Switches or email IDT at ssdhelp@idt.com.

Device Management Software

The primary use of the Device Management Software package is to enable users of the evaluation board to access all the registers in the PES32NT24AG2 device. This access can be achieved using the PCI Express in-band configuration cycles through the upstream port on the PES32NT24AG2 or through the SMBUS salve interface available on the IDT PCIe switch.

This software also enables users to save a snapshot of the current register set into a dump file which can be used for debugging purposes. An export/import facility is also available to create and use “Configuration” files which can be used to initialize the switch device with specific values in specific registers.

A conversion utility is also provided to translate a configuration file into an EEPROM programmable data structure. This enables the user to program an appropriate serial EEPROM with desirable register settings for the PES32NT24AG2, and then to populate that EEPROM onto the Evaluation Board. It is also possible to program the EEPROM directly on the Evaluation Board using a feature provided by the software package.

The front-end of the Device Management Software is a user-friendly Graphical User Interface which allows the user to quickly read or write the registers of interest. The GUI also permits the user to run the software in “simulation” mode with no real hardware attached, allowing the creation of configuration files for the PES32NT24AG2 in the absence of the actual device.

Much of the Device Management Software is written with device-independent and OS-independent code. The software is expected to work on Linux (/sys interface) and MS Windows XP. It may function well on various flavors of MS Windows, but may not be validated on all. The fact that the software is device-independent assures its scalability to future PCIe parts from IDT. Once users are familiar with the GUI, they will be able to use the same GUI on all PCIe parts from IDT. This software is customized for each device through an XML device description file which includes information on the number of ports, registers, types of registers, information on bit-fields within each register, etc.

The actual program name of the Device Management Software is “PCIeBrowser” (an executable file under Windows or Linux). Revision 5.0.1 or later is required for devices in the PES32NT24AG2 product family family.

Device Drivers

The PES32NT24AG2 and other members of this switch family offer Non-Transparent Bridging and built-in DMA capability inside the device. Device drivers are needed to take advantage of these features. Sample code for these drivers is available from IDT for the Linux operating system. Additionally, there a few other software packages available from IDT. These packages are not related to the evaluation board per se, and therefore not listed here. However, several of these packages may prove to be useful for specific device or system functionality. For more information, please go to http://www.idt.com/?app=TechSupport&prodFamily=PCIe%20Switches or email IDT at ssdhelp@idt.com.

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Notes

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Schematics

Notes

Schematics

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REVISIONS				
DCN	REV	DESCRIPTION	DATE	CHANGE BY
	1.0	INITIAL RELEASE	2009-12-05	T. TRAN

1. TITLE PAGE / TABLE OF CONTENTS

2. MEZZANINE CONNECTOR PORTS 0, 2
3. MEZZANINE CONNECTOR PORTS 4, 6
4. MEZZANINE CONNECTOR PORTS 8, 12
5. MEZZANINE CONNECTOR PORTS 16, 20
6. 32NT24AG2 - SERDES
7. 32NT24AG2 - CLK, CONFIG, GPIO
8. 32NT24AG2 - POWER, GND
9. IOEXPANDER 0-3
10. IOEXPANDER 4-7
11. IOEXPANDER 8-11
12. IOEXPANDER 12-13
13. IOEXPANDER 16-19
14. IOEXPANDER 20-21
15. HOT PLUG CONTROL PORTS 0-2
16. HOT PLUG CONTROL PORTS 4-6
17. HOT PLUG CONTROL PORTS 8-12
18. HOT PLUG CONTROL PORTS 16-20
19. SLOT RESETS AND WAKE PULL-UPS
20. CLOCK GENERATOR / SOURCE INPUT
21. CLOCK BUFFER - 1
22. CLOCK SELECTOR DUT PCLK 8
23. CLOCK SELECTOR DUT PCLK 16
24. CLOCK SELECTOR - DUT PCLK 0-20, GCLK 1-2
25. CLOCK SELECTOR - SLOTS 0-20
26. POWER CONNECTORS
27. POWER REGULATOR - VDDIO
28. POWER REGULATOR - VDDCORE
29. POWER REGULATOR - VDDPEA
30. POWER REGULATOR - VDDPEHA
31. POWER REGULATOR - VDDPETA
32. RESET, SMBUS, EEPROM, JTAG
33. DIP SWITCHES
34. LED - PORT STATUS (1 OF 7)
35. LED - PORT STATUS (2 OF 7)
36. LED - PORT STATUS (3 OF 7)
37. LED - PORT STATUS (4 OF 7)
38 LED - PORT STATUS (5 OF 7)
39. LED - PORT STATUS (6 OF 7)
40. LED - PORT STATUS (7 OF 7)
41. MIN LOAD RESISTORS
42. 12PK RIBBON CONNECTORS
43. PARTITION RESET SELECT HEADERS
44. SLOT RESET SELECT HEADERS
45. PORT 0 CLOCK GENERATOR
46. PORT 2 CLOCK GENERATOR
47. PORT 4 CLOCK GENERATOR
48. PORT 6 CLOCK GENERATOR
49. PORT 8 CLOCK GENERATOR
50. PORT 12 CLOCK GENERATOR
51. PORT 16 CLOCK GENERATOR
52. PORT 20 CLOCK GENERATOR

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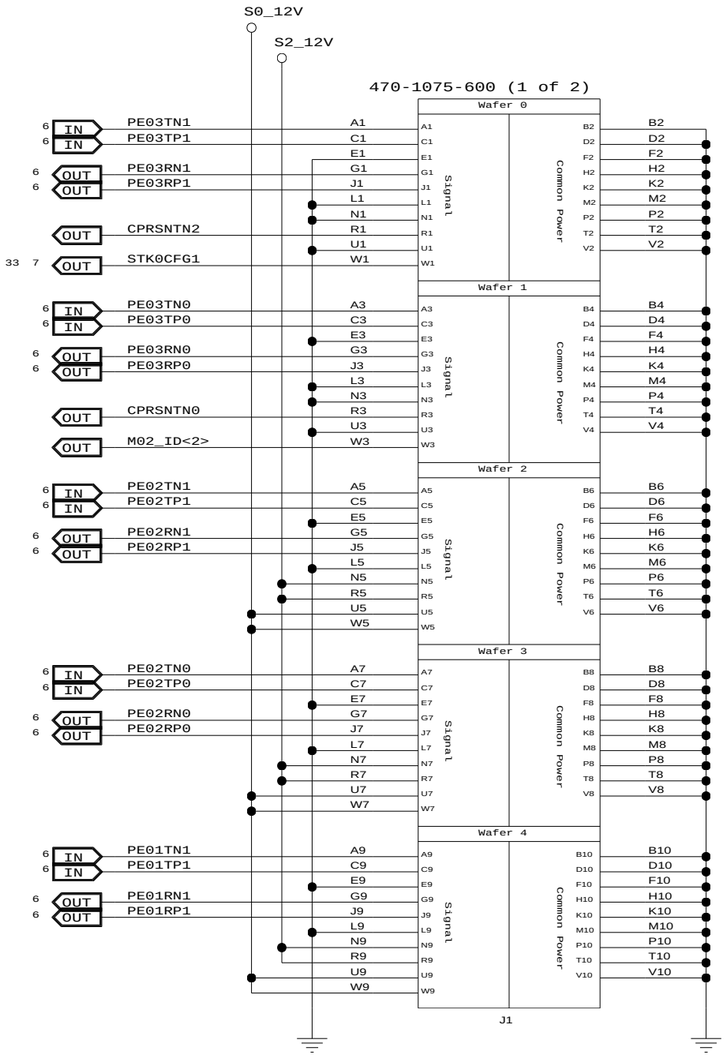
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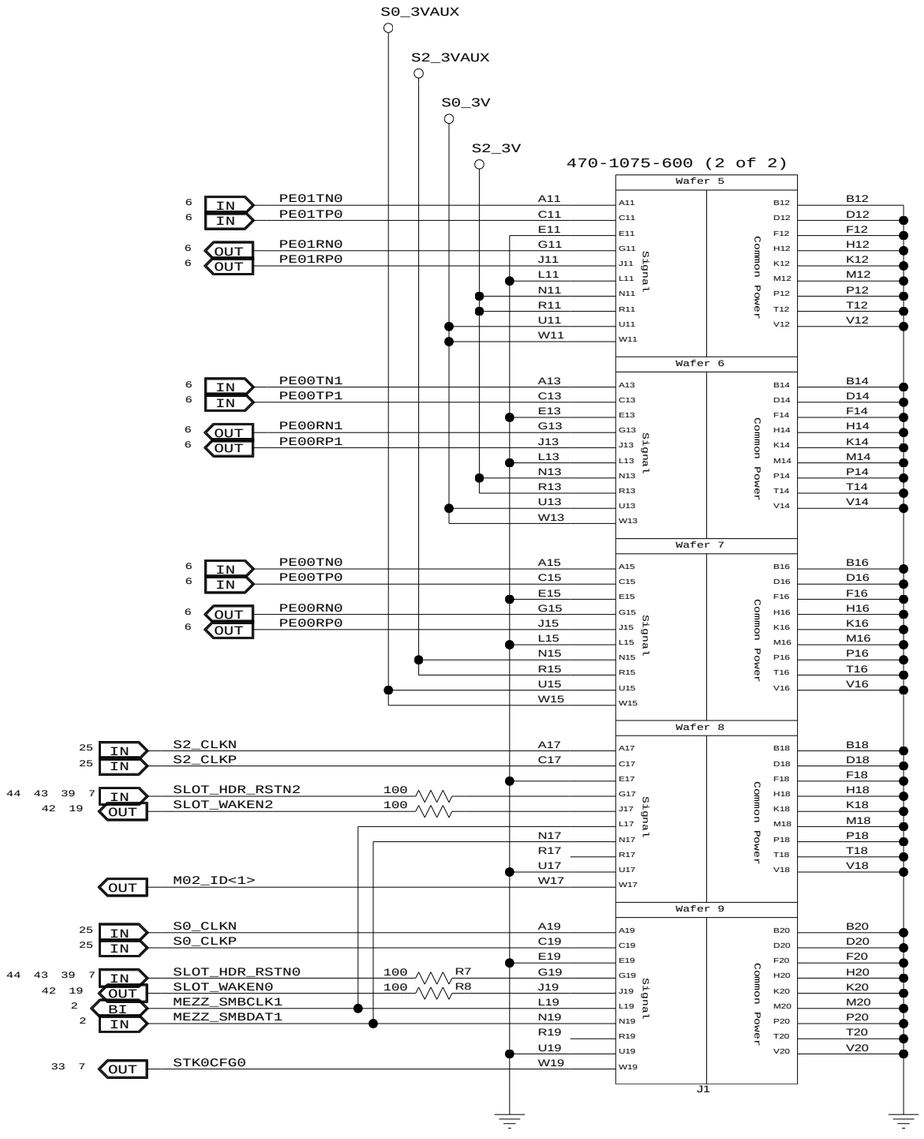
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B	SCH-PESEB-001	18-691-001	2.0

AUTHOR	CHECKED BY
Tony Tran	Derek Huang

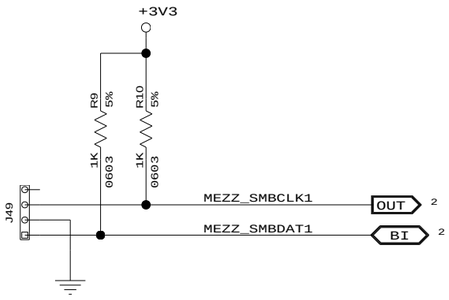
Thu Jul 01 15:00:52 2010 SHEET 1 OF 52

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STK0CFG1 & STK0CFG0 SET BY MEZZ CARDS
X8 - STK0CFG1 = 0, STK0CFG0 = 0
X4 - STK0CFG1 = 0, STK0CFG0 = 1



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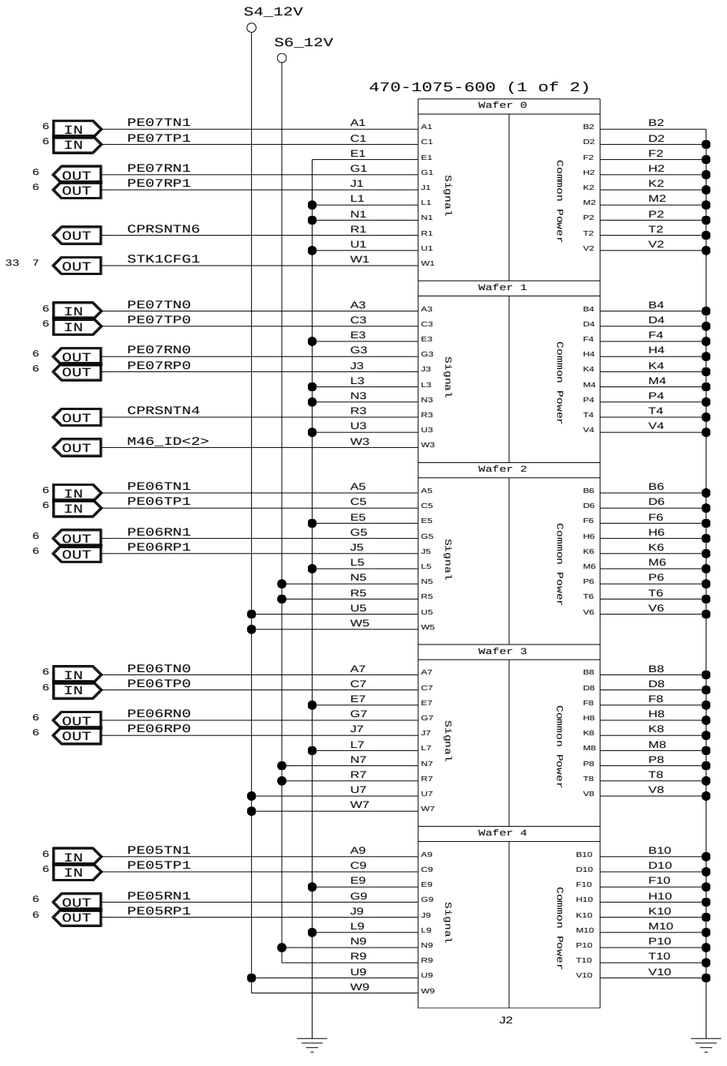
MEZZANINE CONNECTOR PORTS 0/2

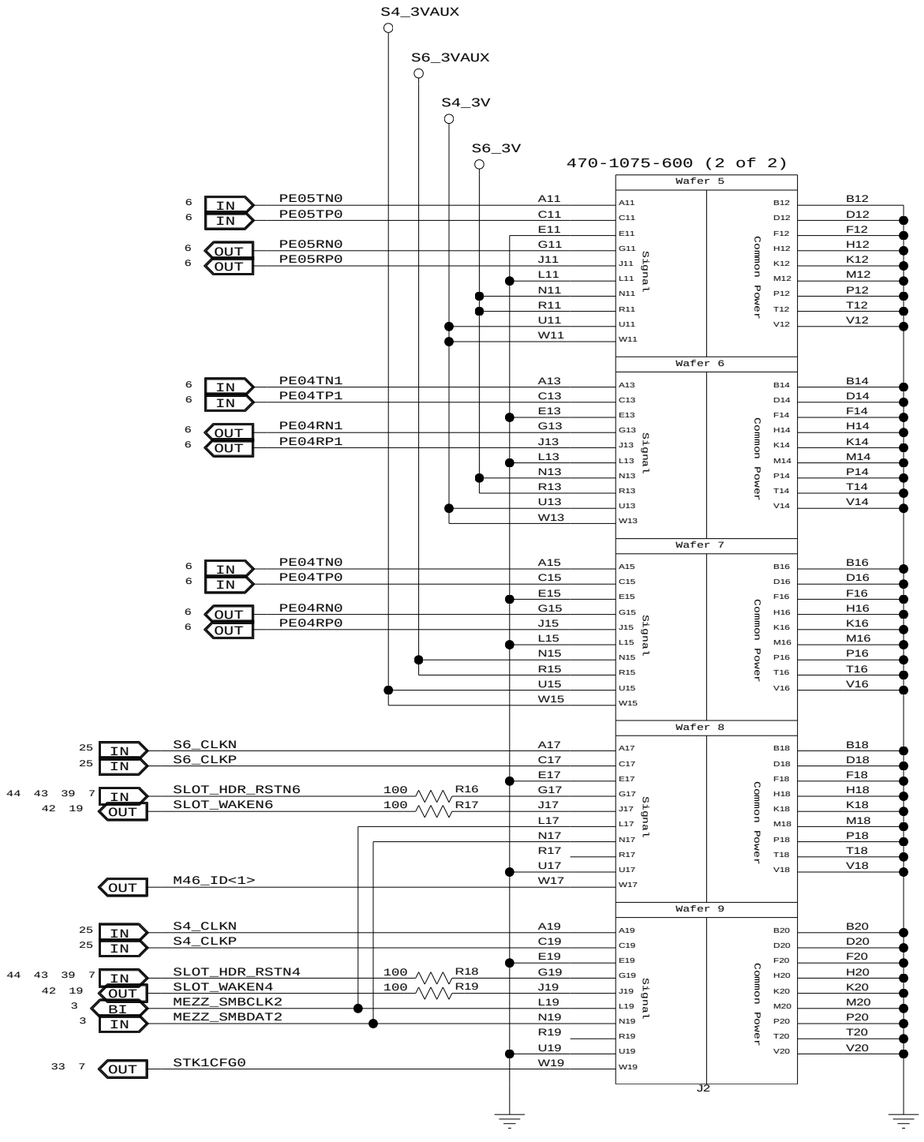
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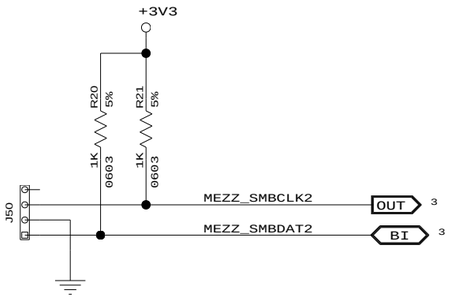
Thu Jul 01 15:00:53 2010 SHEET 2 OF 52

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STK1CFG1 & STK1CFG0 SET BY MEZZ CARDS
X8 - STK1CFG1 = 0, STK1CFG0 = 0
X4 - STK1CFG1 = 0, STK1CFG0 = 1



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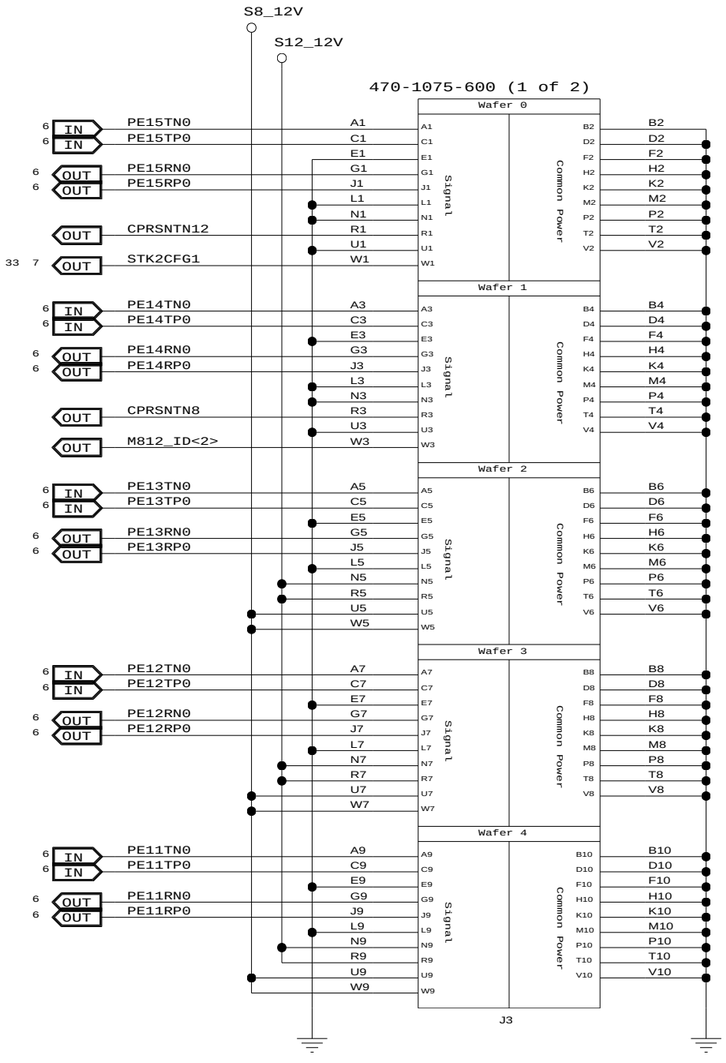
MEZZANINE CONNECTOR PORTS 4/6

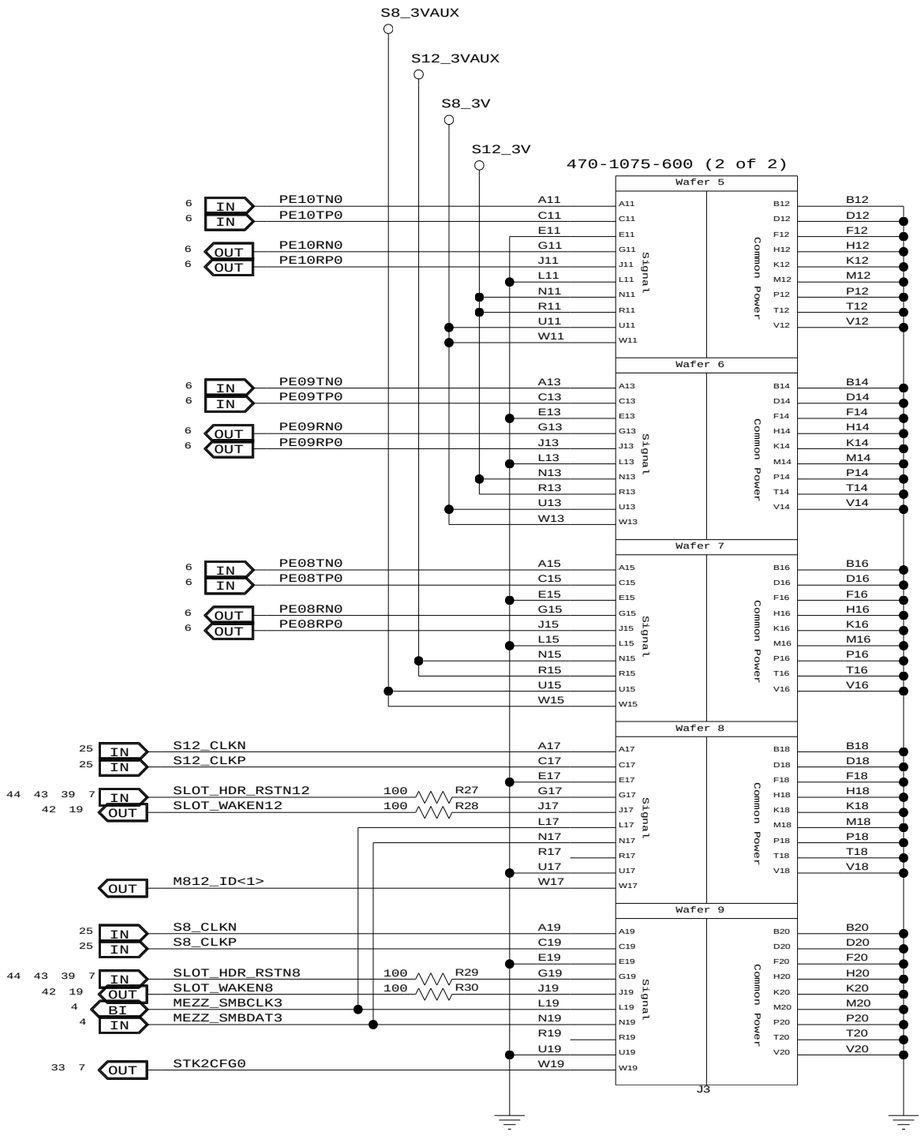
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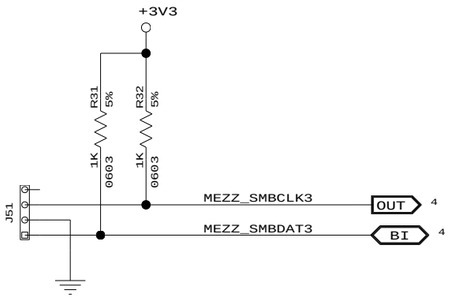
Thu Jul 01 15:00:53 2010 SHEET 3 OF 52

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STK2CFG1 & STK2CFG0 SET BY MEZZ CARDS
X8 - STK2CFG1 = 0, STK2CFG0 = 0
X4 - STK2CFG1 = 0, STK2CFG0 = 1



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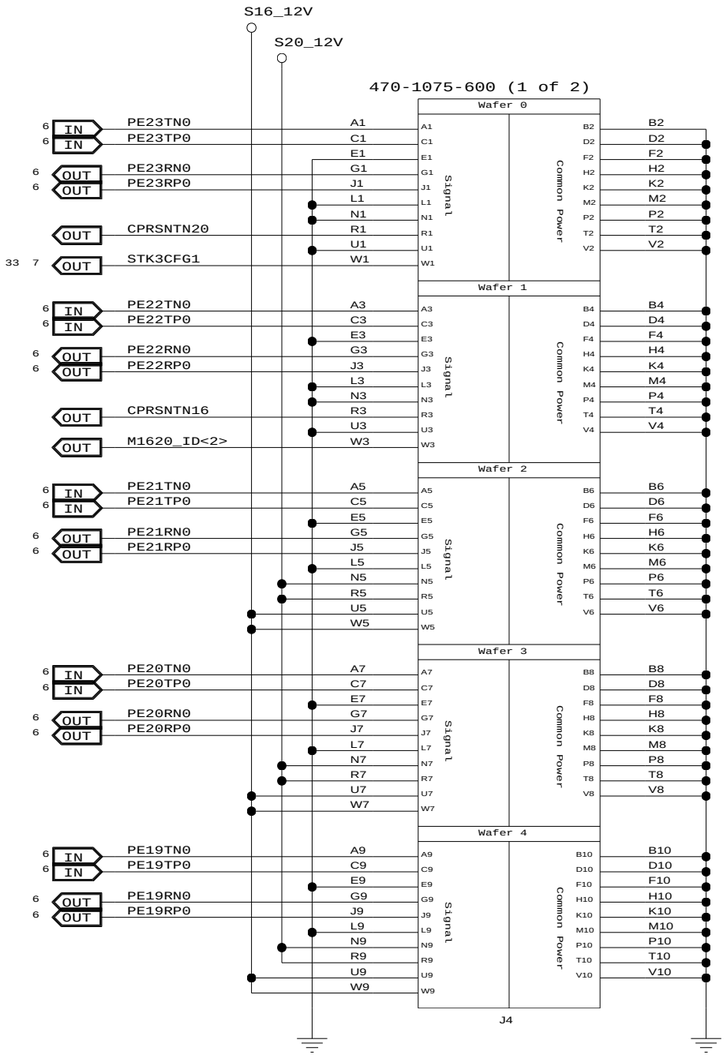
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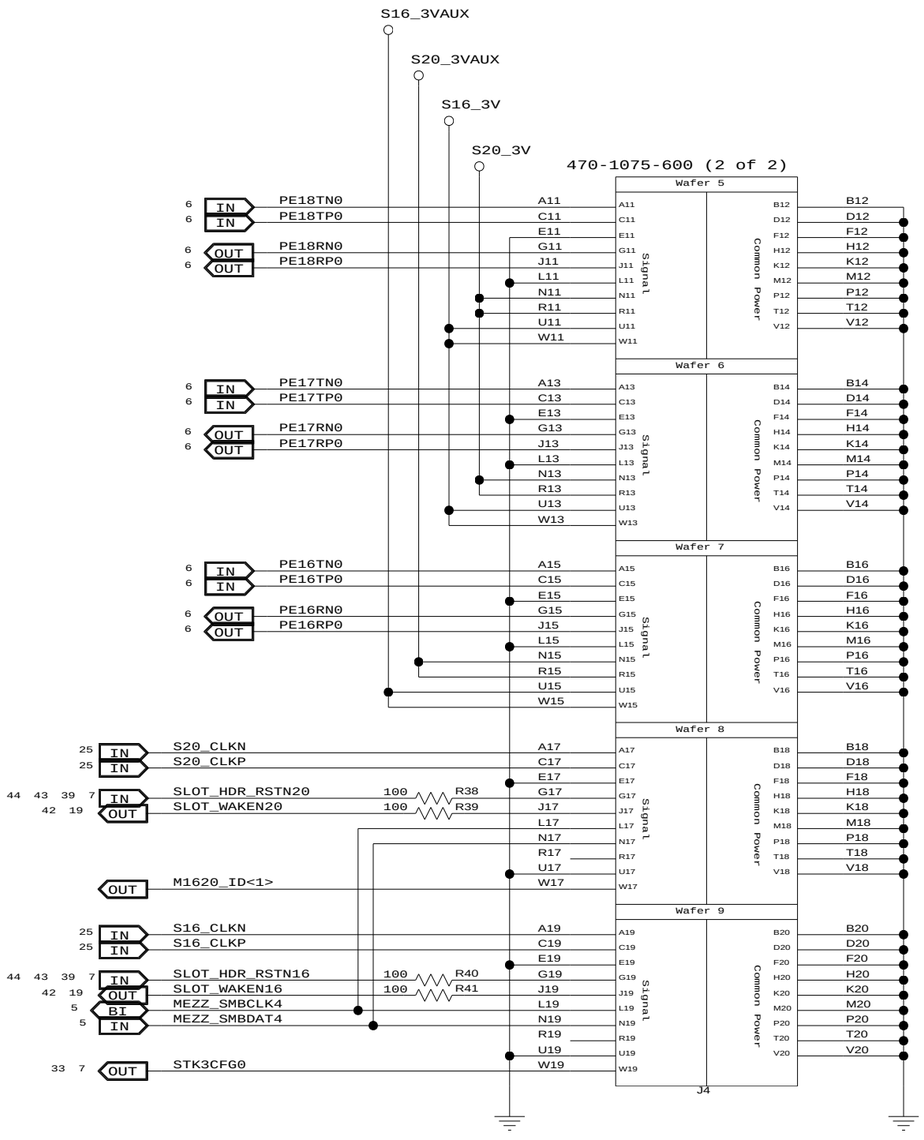
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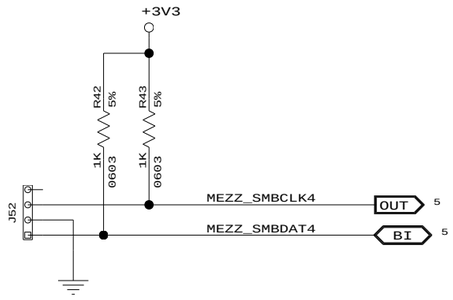
Thu Jul 01 15:00:53 2010 SHEET 4 OF 52

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STK3CFG1 & STK3CFG0 SET BY MEZZ CARDS
X8 - STK3CFG1 = 0, STK3CFG0 = 0
X4 - STK3CFG1 = 0, STK3CFG0 = 1



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MEZZANINE CONNECTOR PORTS 16/20

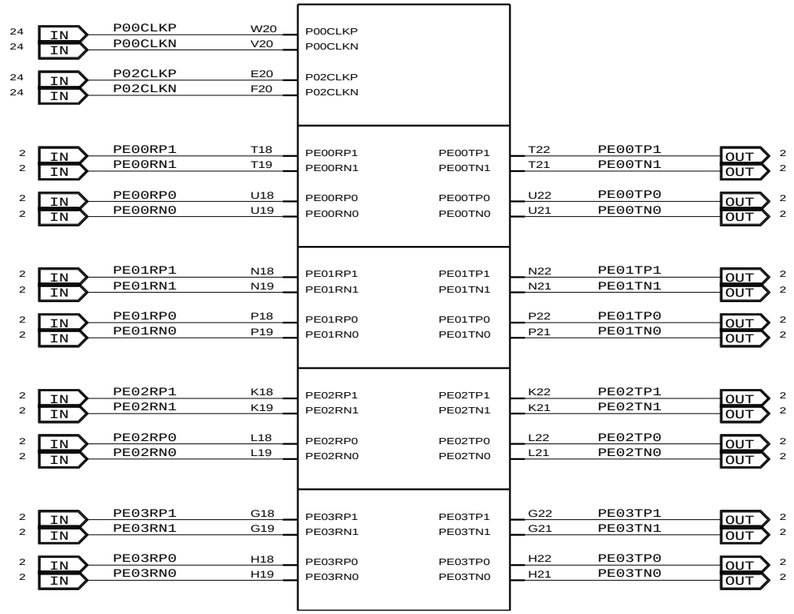
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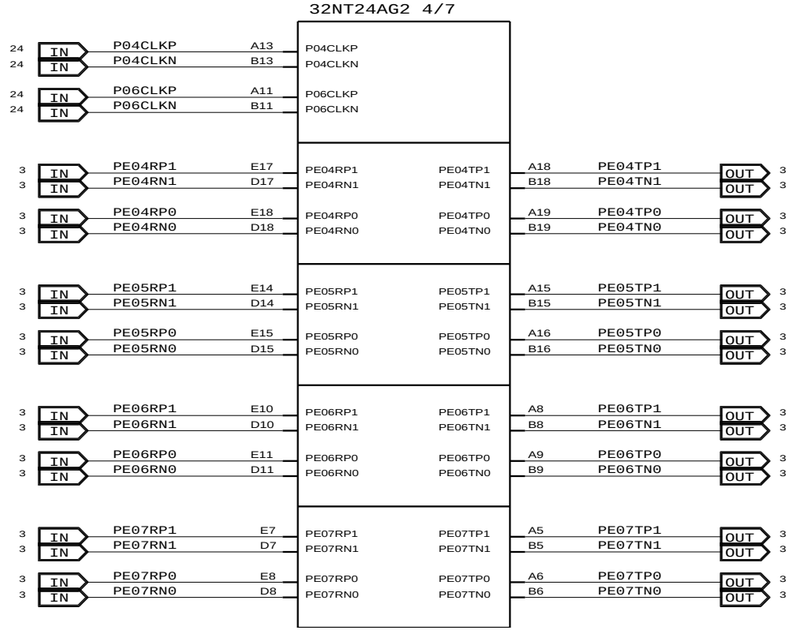
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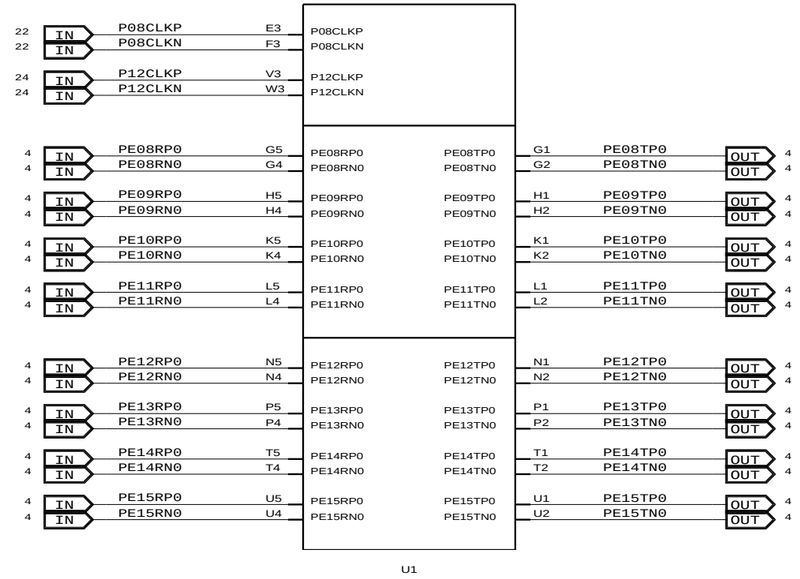
32NT24AG2 3/7



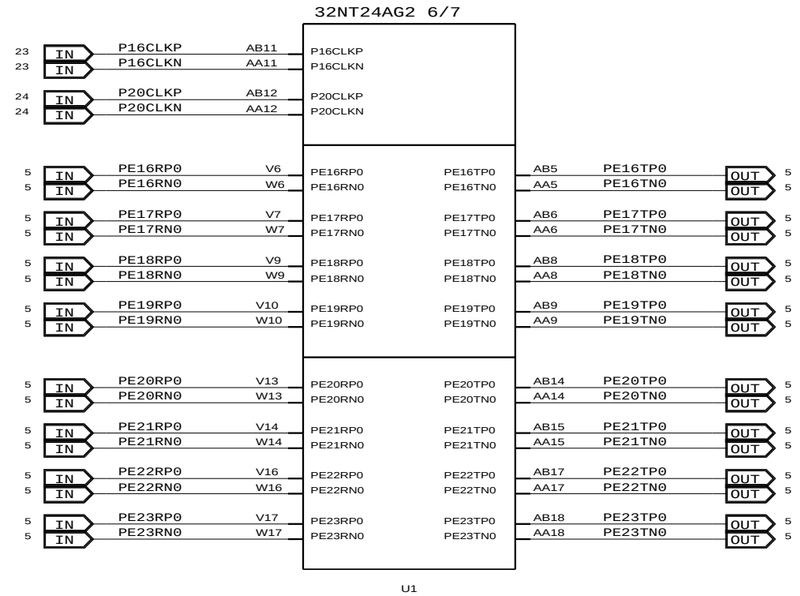
32NT24AG2 4/7



32NT24AG2 5/7



32NT24AG2 6/7



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32NT24AG2 - SERDES

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Thu Jul 01 15:00:54 2010 SHEET 6 OF 52

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DUT RESET

HDR_2x10

J118

MAIN_RSTN	1	2	2
SLOT_HDR_RSTN0	3	4	4
SLOT_HDR_RSTN2	5	6	6
SLOT_HDR_RSTN4	7	8	8
SLOT_HDR_RSTN6	9	10	10
SLOT_HDR_RSTN8	11	12	12
SLOT_HDR_RSTN12	13	14	14
SLOT_HDR_RSTN16	15	16	16
SLOT_HDR_RSTN20	17	18	18
	19	20	20

TP108 YEL

32NT24AG2 1/6

GCLK1P	Y11	GCLKP1		
GCLK1N	Y12	GCLKN1		
GCLK0P	A12	GCLKP0		
GCLK0N	B12	GCLKN0		
GCLKFSEL	AB2	GCLKFSEL		
PERSTN	B20	PERSTN		
RSTHALT	AA4	RSTHALT		
			REFRES07	Y14
SWMODE3	Y5	SWMODE3	REFRES06	Y9
SWMODE2	Y4	SWMODE2	REFRES05	N6
SWMODE1	AA3	SWMODE1	REFRES04	K6
SWMODE0	Y3	SWMODE0	REFRES03	C9
			REFRES02	D13
G3	C2	G3	REFRES01	K17
G2	D2	G2	REFRES00	N17
G1	D3	G1	REFRESPLL	D12
G0	D1	G0		
			NC	C16
CLKMODE1	B22	CLKMODE1	NC	Y8
CLKMODE0	AA1	CLKMODE0		
STK0CFG1	AB21	STK0CFG1		
STK0CFG0	Y1	STK0CFG0		
STK1CFG1	AB20	STK1CFG1		
STK1CFG0	AB1	STK1CFG0		
STK2CFG4	B1	STK2CFG4		
STK2CFG3	A3	STK2CFG3		
STK2CFG2	A2	STK2CFG2		
STK2CFG1	A1	STK2CFG1		
STK2CFG0	AA2	STK2CFG0		
STK3CFG4	C3	STK3CFG4		
STK3CFG3	C1	STK3CFG3		
STK3CFG2	B3	STK3CFG2		
STK3CFG1	B2	STK3CFG1		
STK3CFG0	Y2	STK3CFG0		

U1

PLACE RESISTORS AS CLOSE TO U1 AS POSSIBLE

REFRES07	3.01K	R46	
REFRES06	3.01K	R47	
REFRES05	3.01K	R48	
REFRES04	3.01K	R49	
REFRES03	3.01K	R50	
REFRES02	3.01K	R51	
REFRES01	3.01K	R52	
REFRES00	3.01K	R53	
REFRESPLL	3.01K	R54	

+3V3

R24 1K 0603 5%

R55 1K 0603 5%

MSMBCLK

MSMBDAT

0 R45

32NT24AG2 2/7

			JTAG_TCK	C22
			JTAG_TDI	D20
MSMBCLK	A20	MSMBCLK	JTAG_TDO	A21
MSMBDAT	C20	MSMBDAT	JTAG_TMS	B21
		JTAG_TRST_N		A22
SSMBADDR2	D22	SSMBADDR2		
SSMBADDR1	Y22	SSMBADDR1	GPIO00	AA19
			GPIO01	Y18
SSMBCLK	D21	SSMBCLK	GPIO02	AA20
SSMBDAT	C21	SSMBDAT	GPIO03	Y19
			GPIO04	Y20
			GPIO05	AB22
			GPIO06	AA21
			GPIO07	AA22
			GPIO08	Y21

DUT_JTAG_TCK	IN	32
DUT_JTAG_TDI	IN	32
DUT_JTAG_TDO	OUT	32
DUT_JTAG_TMS	IN	32
DUT_JTAG_TRST_N	IN	32
GPIO0	OUT	34
GPIO1	OUT	34
GPIO2	OUT	34
GPIO3	OUT	34
GPIO4	OUT	34
GPIO5	OUT	34
GPIO6	OUT	34
GPIO7	OUT	34
GPIO8	OUT	34

U1

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TITLE EB-LOGAN-23

32NT24AG2 CLK, CONFIG, GPIO

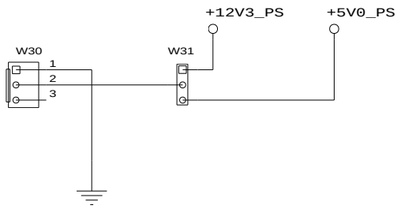
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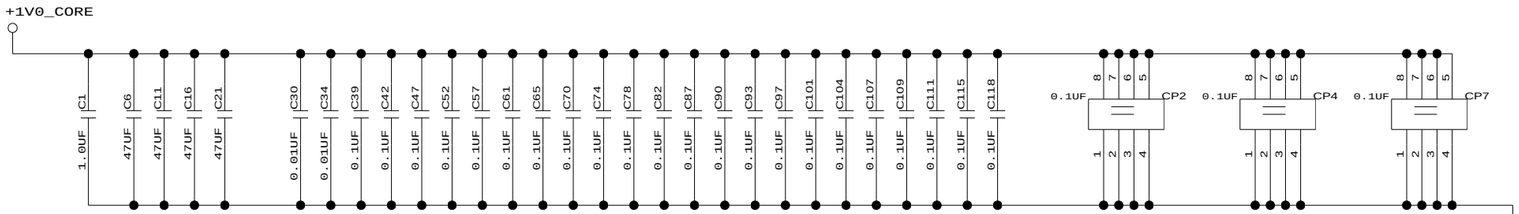
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Tony Tran	Derek Huang

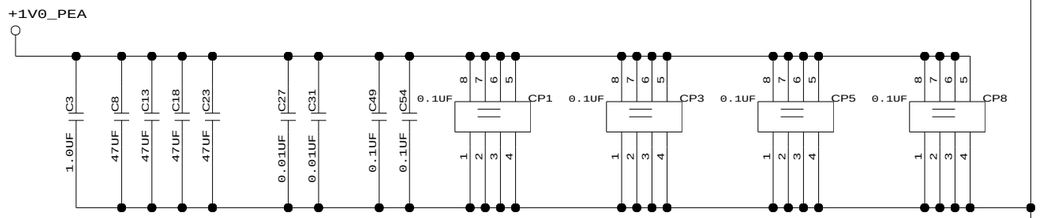
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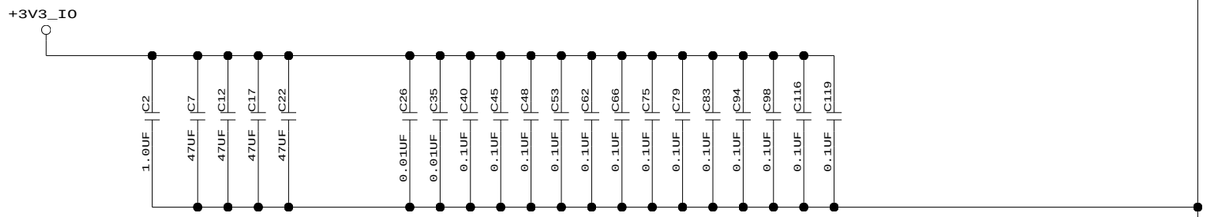
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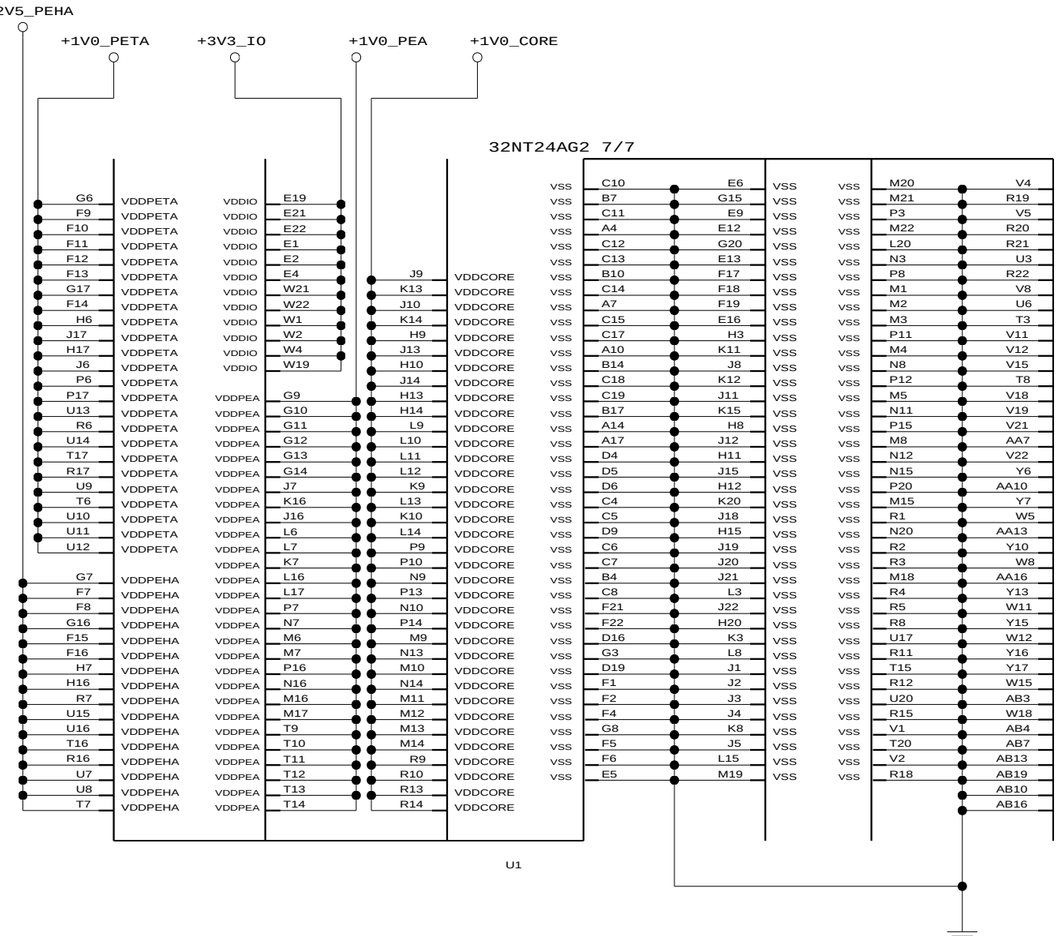
LABEL: FAN
LABEL:
1 GND
2 12V/5V
3 NC

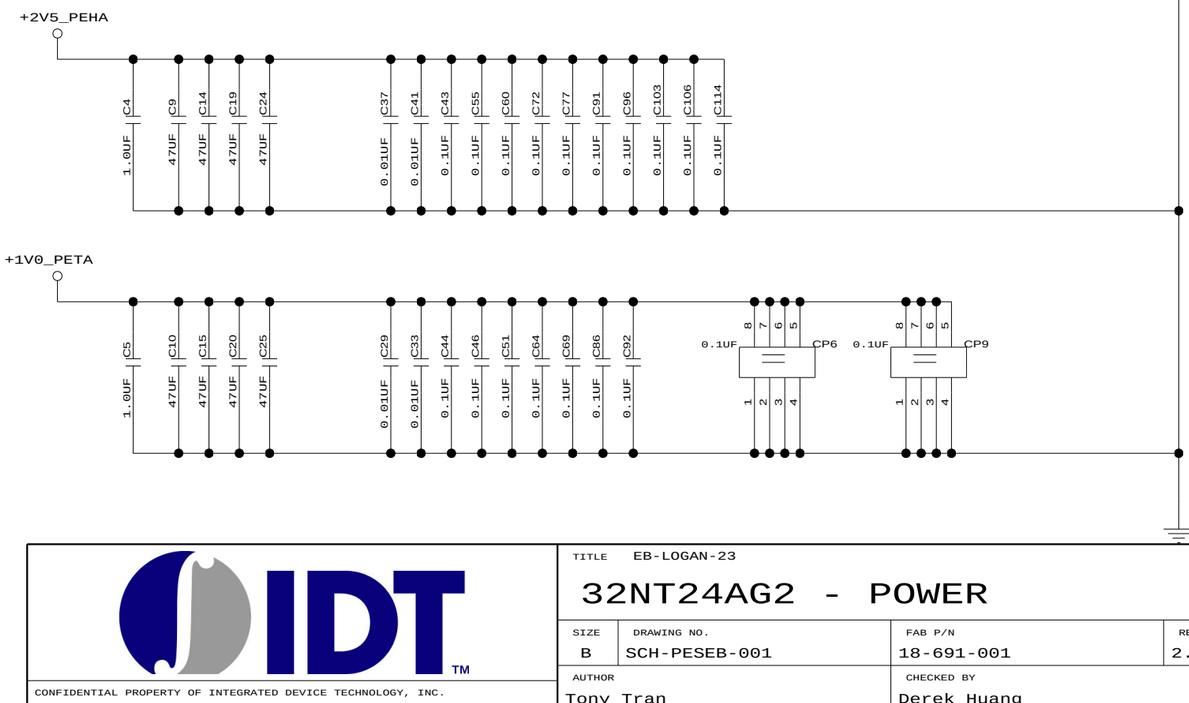












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TITLE EB-LOGAN-23

32NT24AG2 - POWER

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PLACE RESISTORS ON CLOSE AND ON SAME SIDE OF BOARD

+3V3

U20 MAX7311AUG

R59 0, R60 0, R61 0

MSMBCLK 0 R65, MSMBDAT 0 R66

R69 1K

C184 0.1UF

R1612 0 IOEXPINTN

P0_APN P0_PDN P0_PFN P0_PWRGDN P0_AIN P0_PIN P0_PEP P0_RSTN P4_APN P4_PDN P4_PFN P4_PWRGDN P4_AIN P4_PIN P4_PEP P4_RSTN

IOEXPANDER 0

ADDR: 0X20

PLACE RESISTORS ON CLOSE AND ON SAME SIDE OF BOARD

+3V3

U22 MAX7311AUG

R71 0, R72 2.7K, R73 0

MSMBCLK 0 R77, MSMBDAT 0 R78

C186 0.1UF

R1614 0 IOEXPINTN

P2_APN P2_PDN P2_PFN P2_PWRGDN P2_AIN P2_PIN P2_PEP P2_RSTN P6_APN P6_PDN P6_PFN P6_PWRGDN P6_AIN P6_PIN P6_PEP P6_RSTN

IOEXPANDER 2

ADDR: 0X24

PLACE RESISTORS ON CLOSE AND ON SAME SIDE OF BOARD

+3V3

U21 MAX7311AUG

R62 2.7K, R63 0, R64 0

MSMBCLK 0 R67, MSMBDAT 0 R68

C185 0.1UF

R1613 0 IOEXPINTN

P8_APN P8_PDN P8_PFN P8_PWRGDN P8_AIN P8_PIN P8_PEP P8_RSTN P16_APN P16_PDN P16_PFN P16_PWRGDN P16_AIN P16_PIN P16_PEP P16_RSTN

IOEXPANDER 1

ADDR: 0X22

PLACE RESISTORS ON CLOSE AND ON SAME SIDE OF BOARD

+3V3

U23 MAX7311AUG

R74 2.7K, R75 2.7K, R76 0

MSMBCLK 0 R79, MSMBDAT 0 R80

C187 0.1UF

R1615 0 IOEXPINTN

P12_APN P12_PDN P12_PFN P12_PWRGDN P12_AIN P12_PIN P12_PEP P12_RSTN P20_APN P20_PDN P20_PFN P20_PWRGDN P20_AIN P20_PIN P20_PEP P20_RSTN

IOEXPANDER 3

ADDR: 0X26

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TITLE EB-LOGAN-23

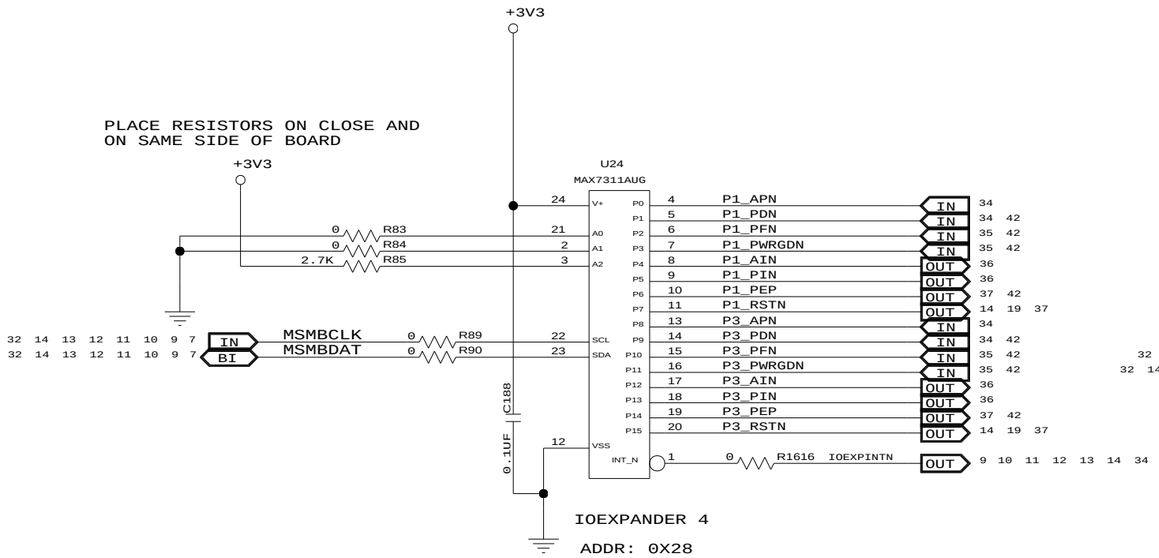
IOEXPANDER 0-3

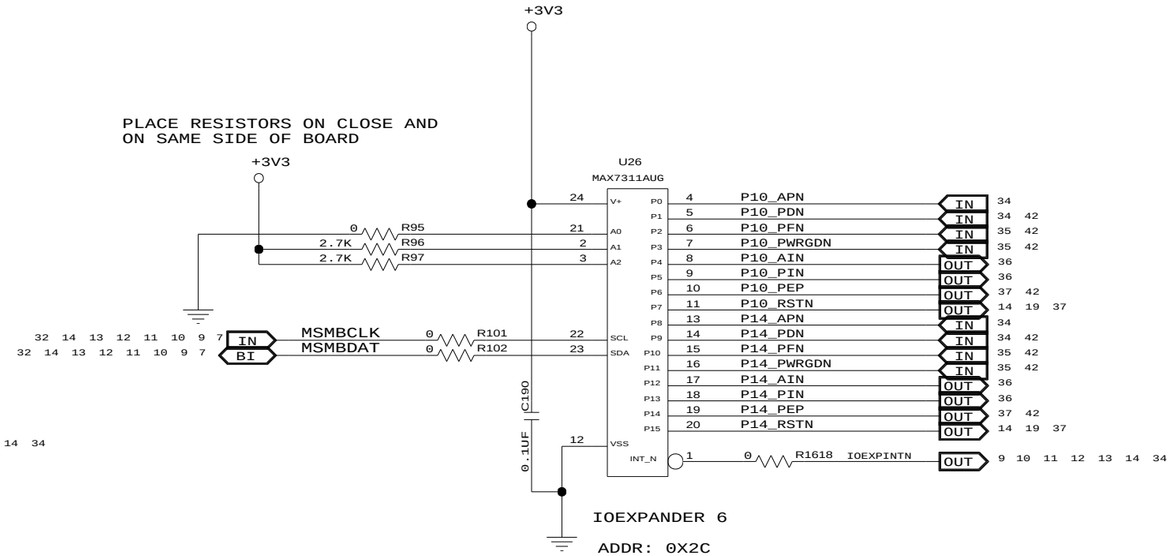
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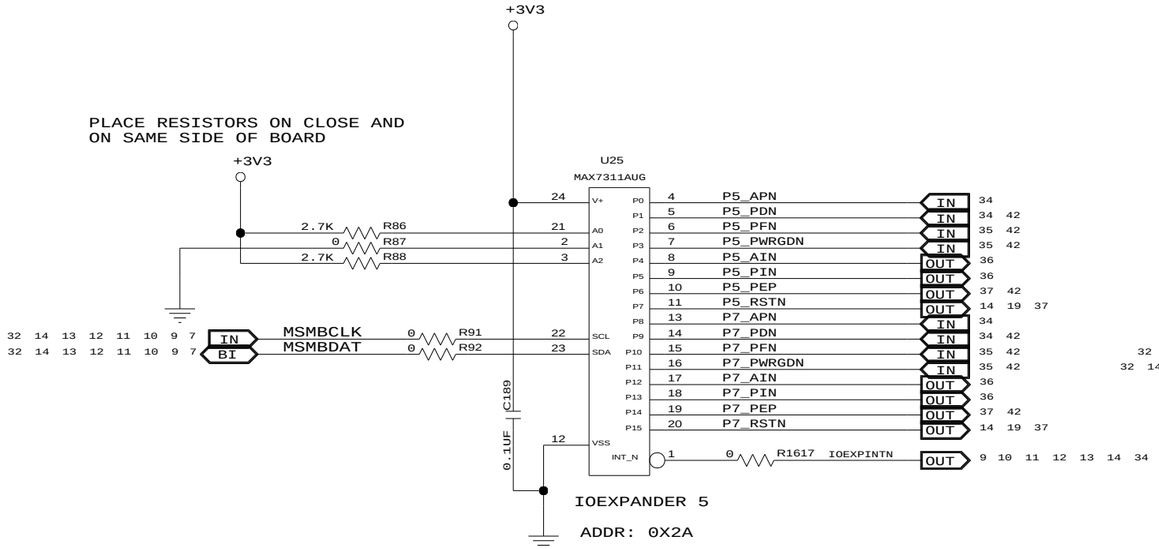
AUTHOR	CHECKED BY
Tony Tran	Derek Huang

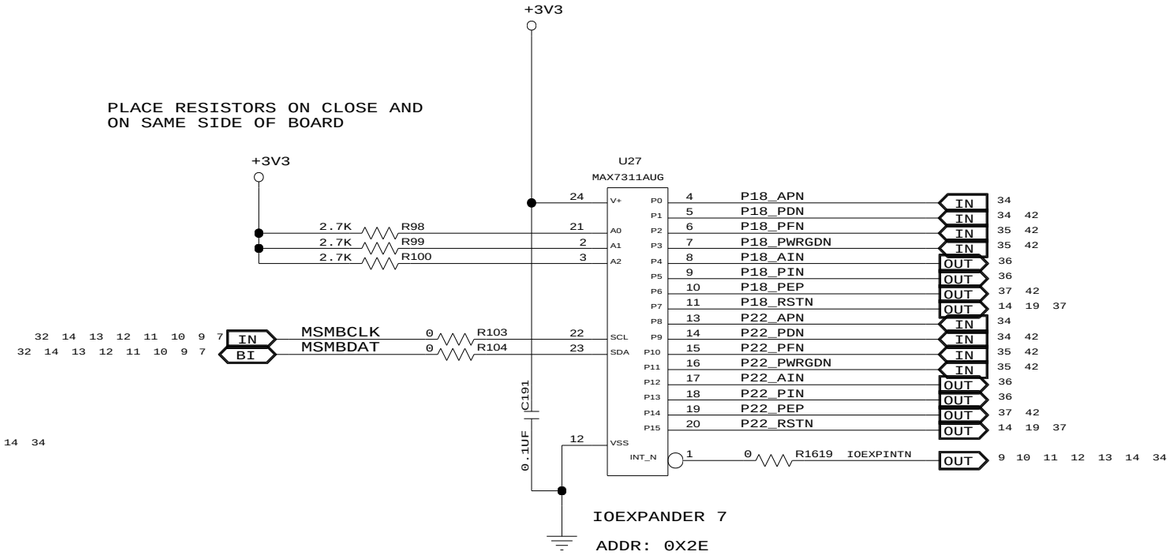
Thu Jul 01 15:00:55 2010 SHEET 9 OF 52

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IOEXPANDER 4-7

SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-PESEB-001	18-691-001	2.0

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Thu Jul 01 15:00:55 2010 SHEET 10 OF 52

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PLACE RESISTORS ON CLOSE AND
ON SAME SIDE OF BOARD

+3V3

U28
MAX7311AUG

R107 0
R108 0
R109 0

MSMBCLK R113 0
MSMBDAT R114 0

C192 0.1UF

R1620 0 IOEXPINTN

IOEXPANDER 8

ADDR: 0X50

PLACE RESISTORS ON CLOSE AND
ON SAME SIDE OF BOARD

+3V3

U30
MAX7311AUG

R119 0
R120 2.7K
R121 0

MSMBCLK R125 0
MSMBDAT R126 0

C194 0.1UF

R1622 0 IOEXPINTN

IOEXPANDER 10

ADDR: 0X54

PLACE RESISTORS ON CLOSE AND
ON SAME SIDE OF BOARD

+3V3

U29
MAX7311AUG

R110 0
R111 0
R112 0

MSMBCLK R115 0
MSMBDAT R116 0

C193 0.1UF

R1621 0 IOEXPINTN

IOEXPANDER 9

ADDR: 0X52

PLACE RESISTORS ON CLOSE AND
ON SAME SIDE OF BOARD

+3V3

U31
MAX7311AUG

R122 0
R123 2.7K
R124 0

MSMBCLK R127 0
MSMBDAT R128 0

C195 0.1UF

R1623 0 IOEXPINTN

IOEXPANDER 11

ADDR: 0X56

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TITLE EBI/LCX Validation Board

IOEXPANDER 8-11

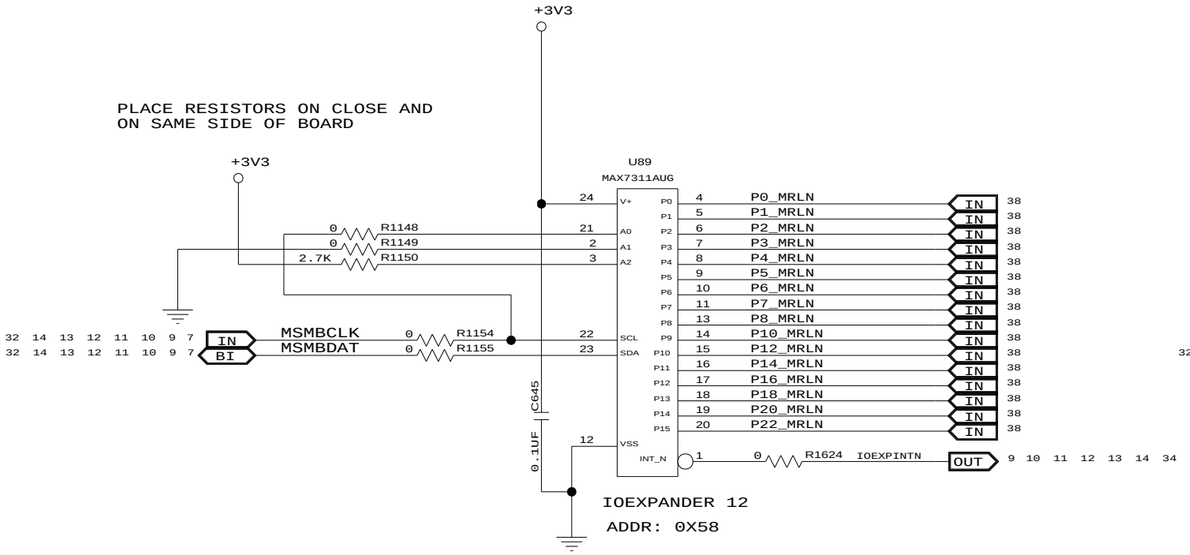
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B	SCH-PESEB-001	18-691-001	2.0

AUTHOR	CHECKED BY
Tony Tran	Derek Huang

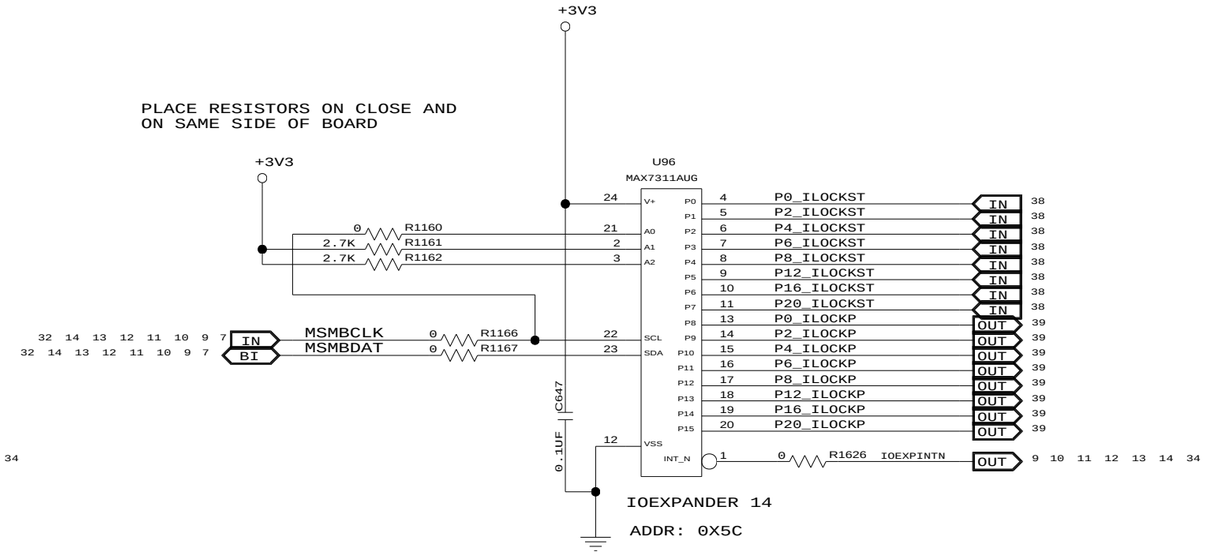
Thu Jul 01 15:00:55 2010 SHEET 11 OF 52

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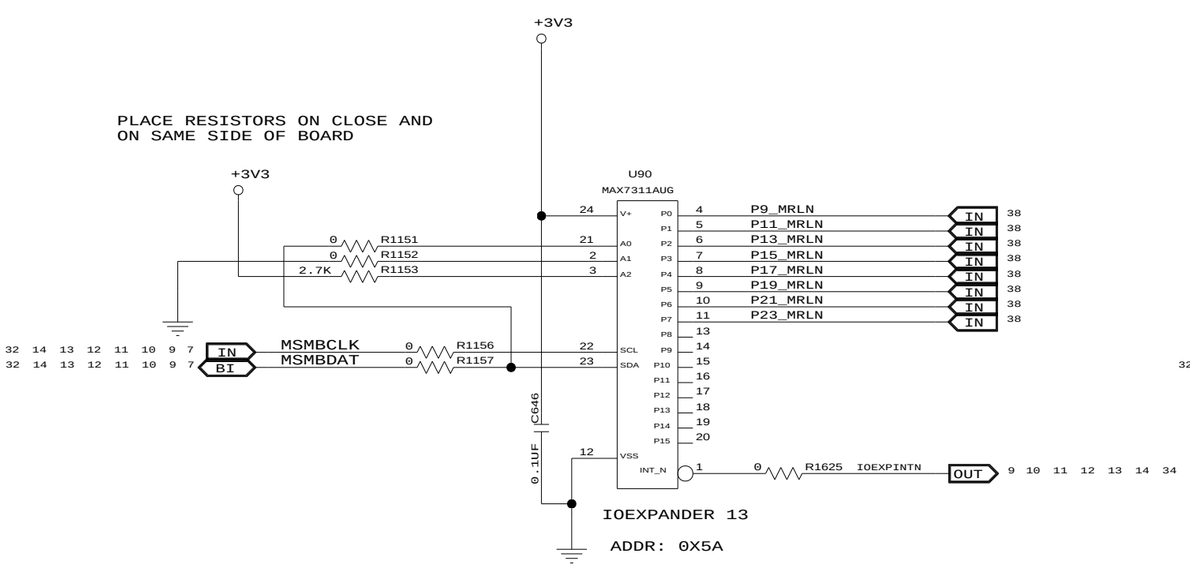
PLACE RESISTORS ON CLOSE AND
ON SAME SIDE OF BOARD



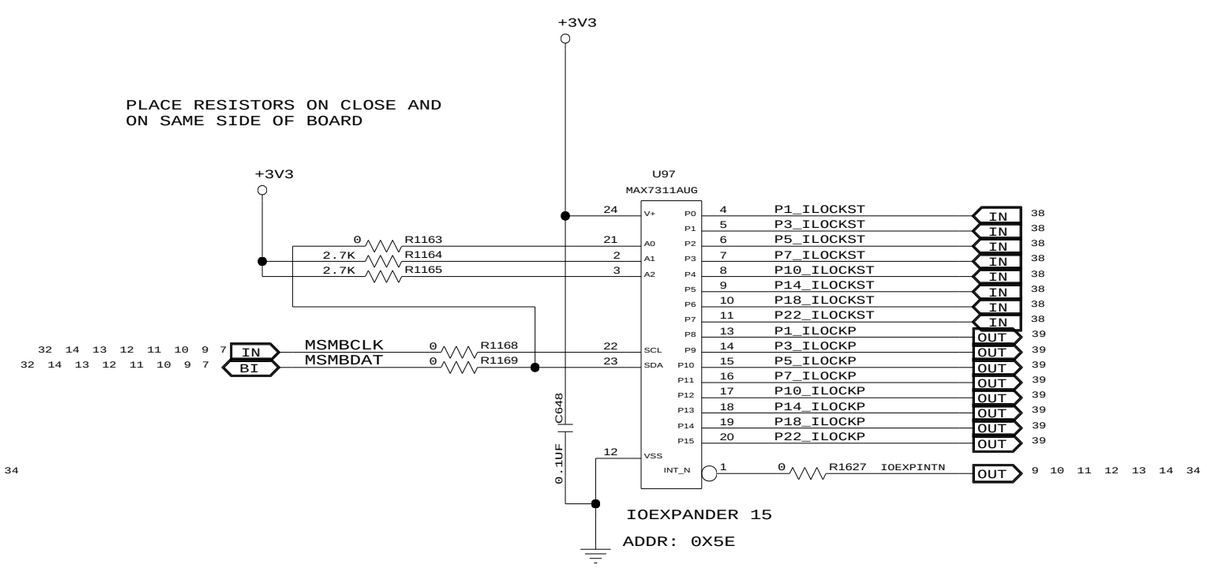
PLACE RESISTORS ON CLOSE AND
ON SAME SIDE OF BOARD



PLACE RESISTORS ON CLOSE AND
ON SAME SIDE OF BOARD



PLACE RESISTORS ON CLOSE AND
ON SAME SIDE OF BOARD



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TITLE EB-LOGAN-23

IOEXPANDER 12-15

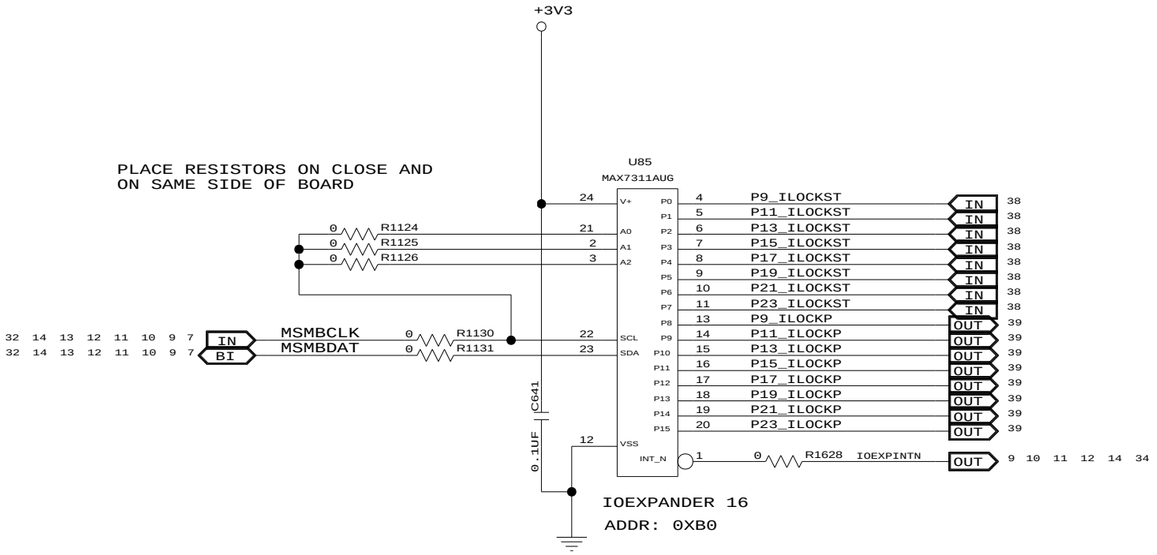
SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-PESEB-001	18-691-001	2.0

AUTHOR	CHECKED BY
Tony Tran	Derek Huang

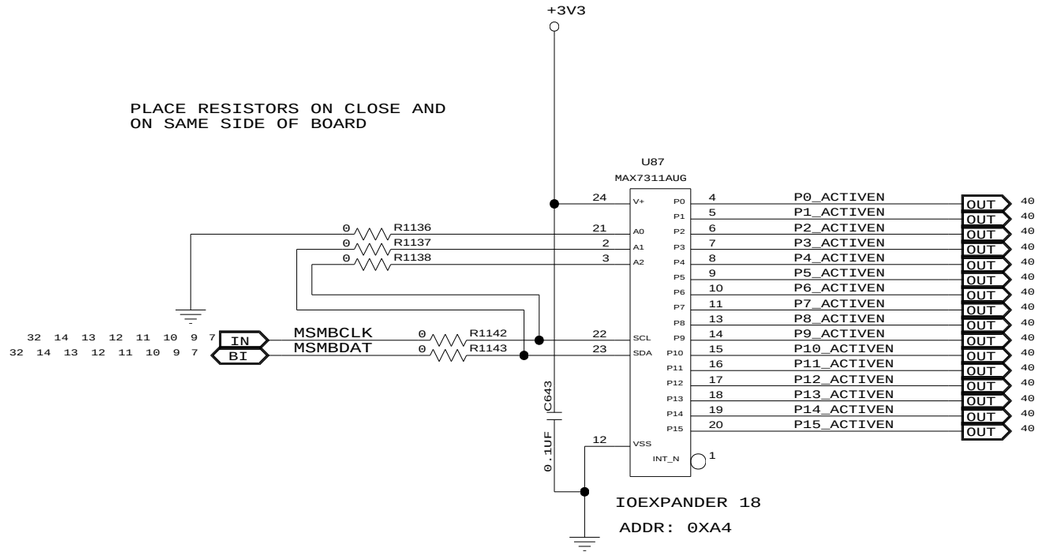
Thu Jul 01 15:00:55 2010 SHEET 12 OF 52

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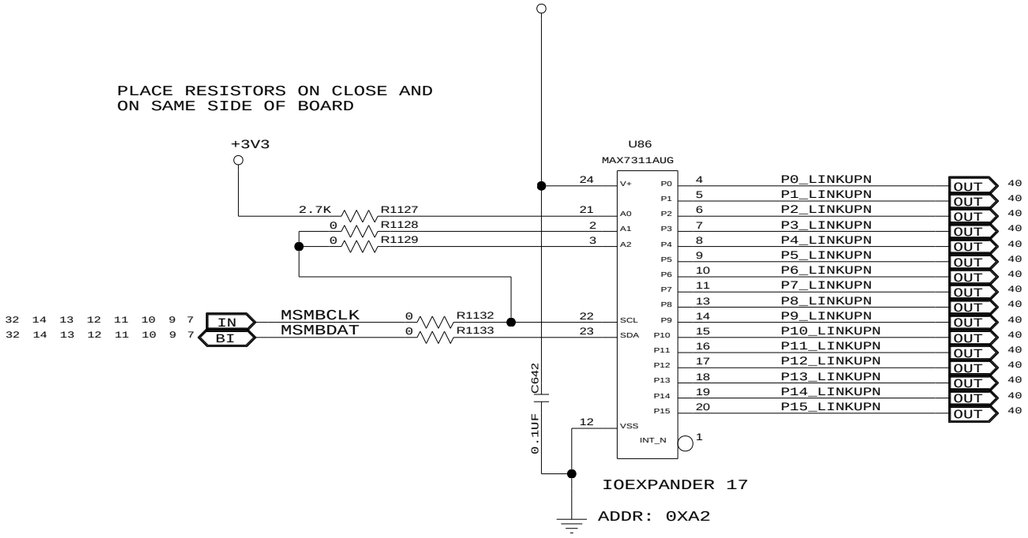
PLACE RESISTORS ON CLOSE AND
ON SAME SIDE OF BOARD



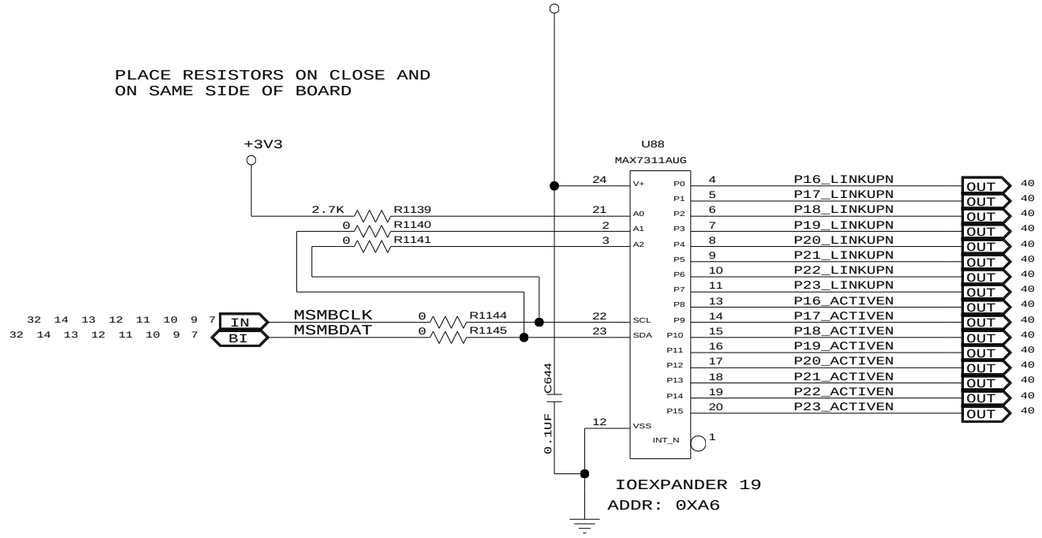
PLACE RESISTORS ON CLOSE AND
ON SAME SIDE OF BOARD



PLACE RESISTORS ON CLOSE AND
ON SAME SIDE OF BOARD



PLACE RESISTORS ON CLOSE AND
ON SAME SIDE OF BOARD



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TITLE EB-LOGAN-23

IOEXPANDER 16-19

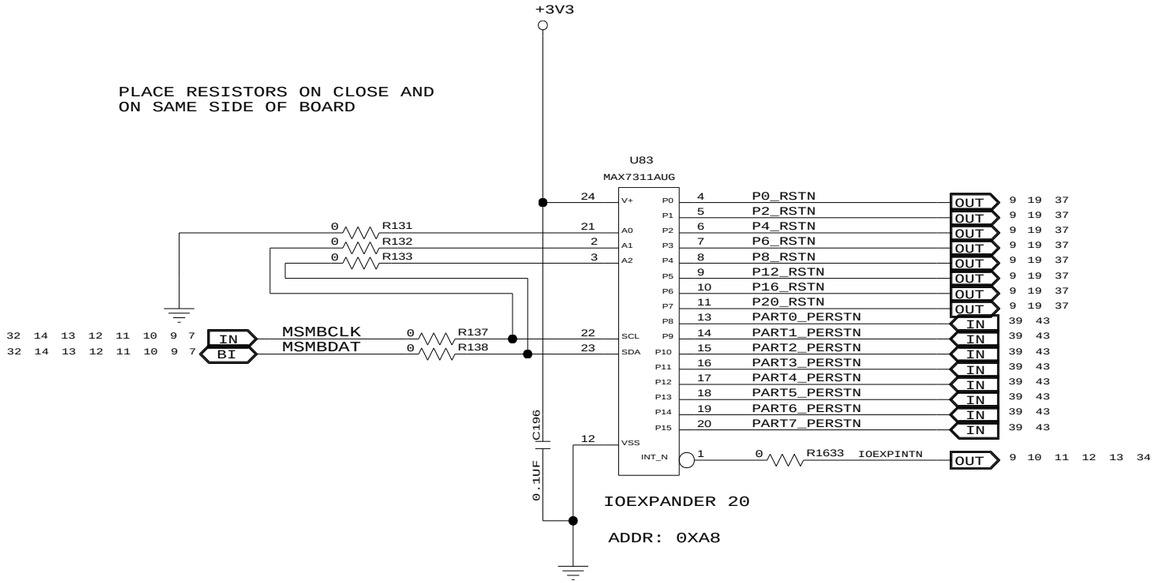
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B	SCH-PESEB-001	18-691-001	2.0

AUTHOR	CHECKED BY
Tony Tran	Derek Huang

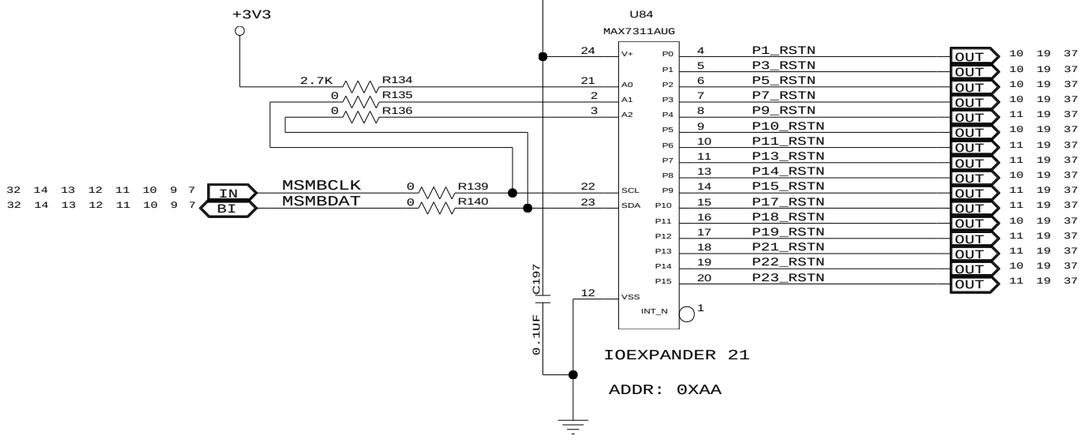
Thu Jul 01 15:00:56 2010 SHEET 13 OF 52

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PLACE RESISTORS ON CLOSE AND
ON SAME SIDE OF BOARD



PLACE RESISTORS ON CLOSE AND
ON SAME SIDE OF BOARD



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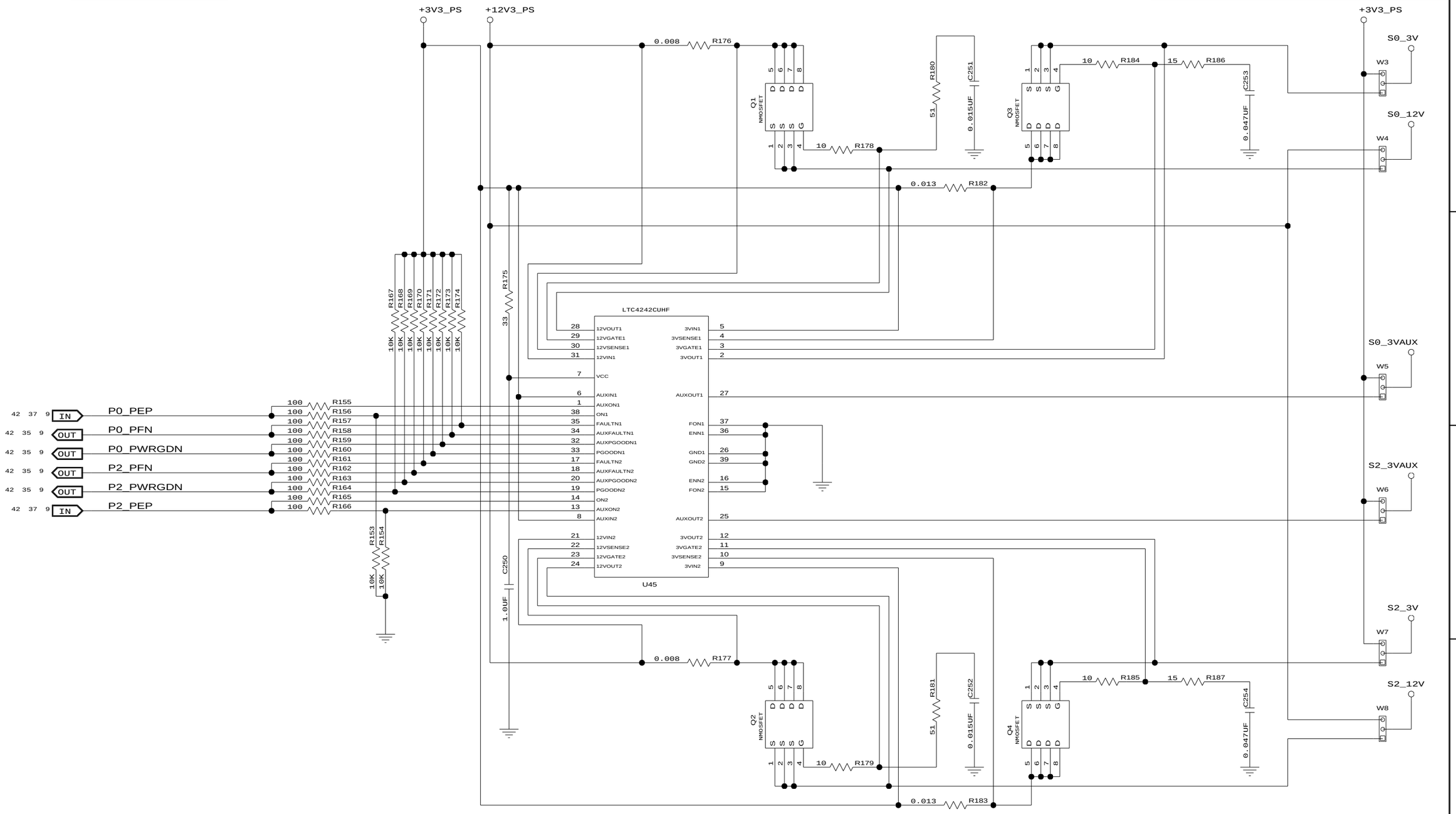
IOEXPANDER 20-21

SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-PESEB-001	18-691-001	2.0

AUTHOR	CHECKED BY
Tony Tran	Derek Huang

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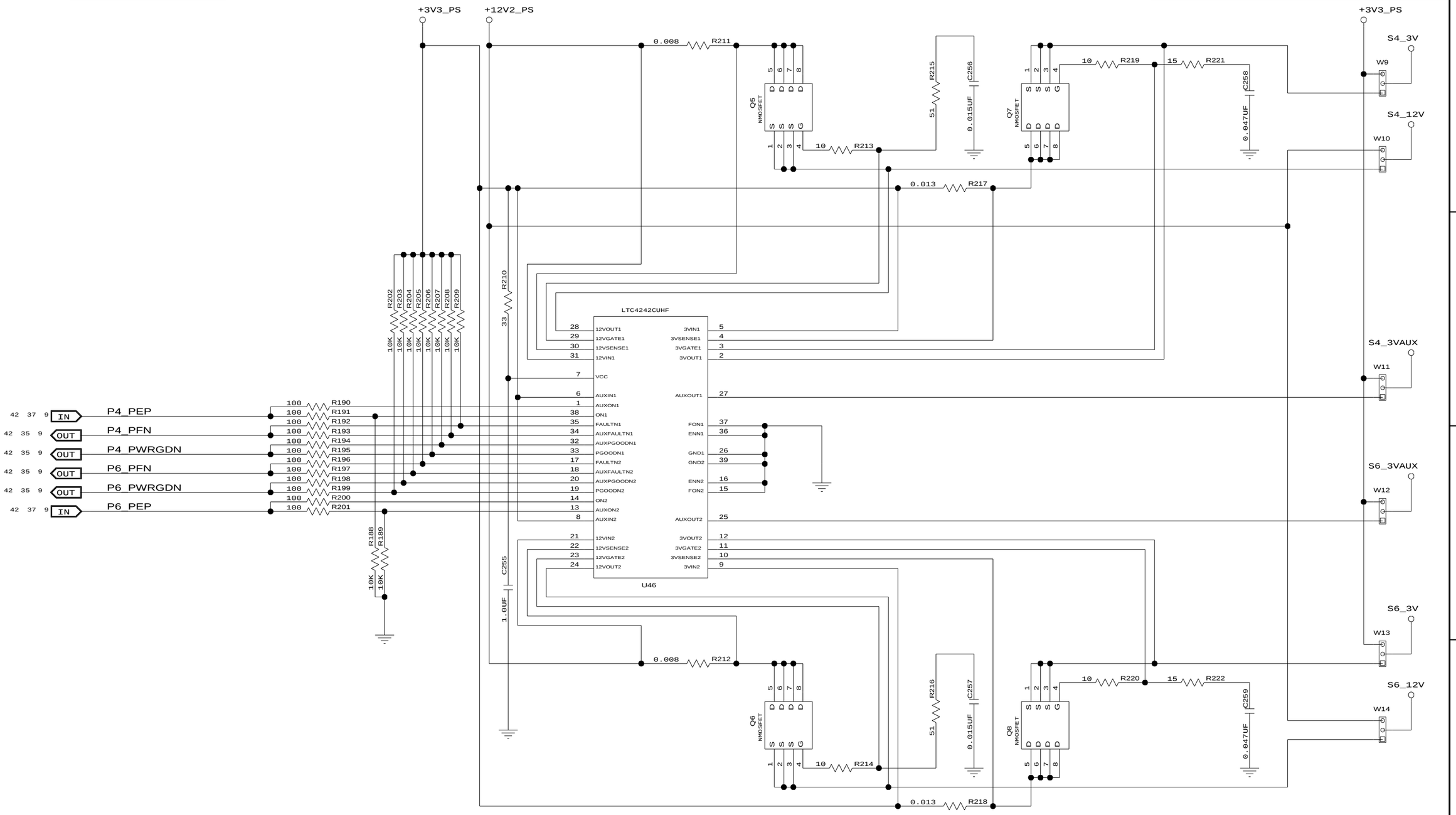


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TITLE	EB-LOGAN-23		
HOT PLUG CONTROL PORTS 0-2			
SIZE: B	DRAWING NO.: SCH-PESEB-001	FAB P/N: 18-691-001	REV.: 2.0
AUTHOR: Tony Tran		CHECKED BY: Derek Huang	
Thu Jul 01 15:00:56 2010		SHEET 15 OF 52	

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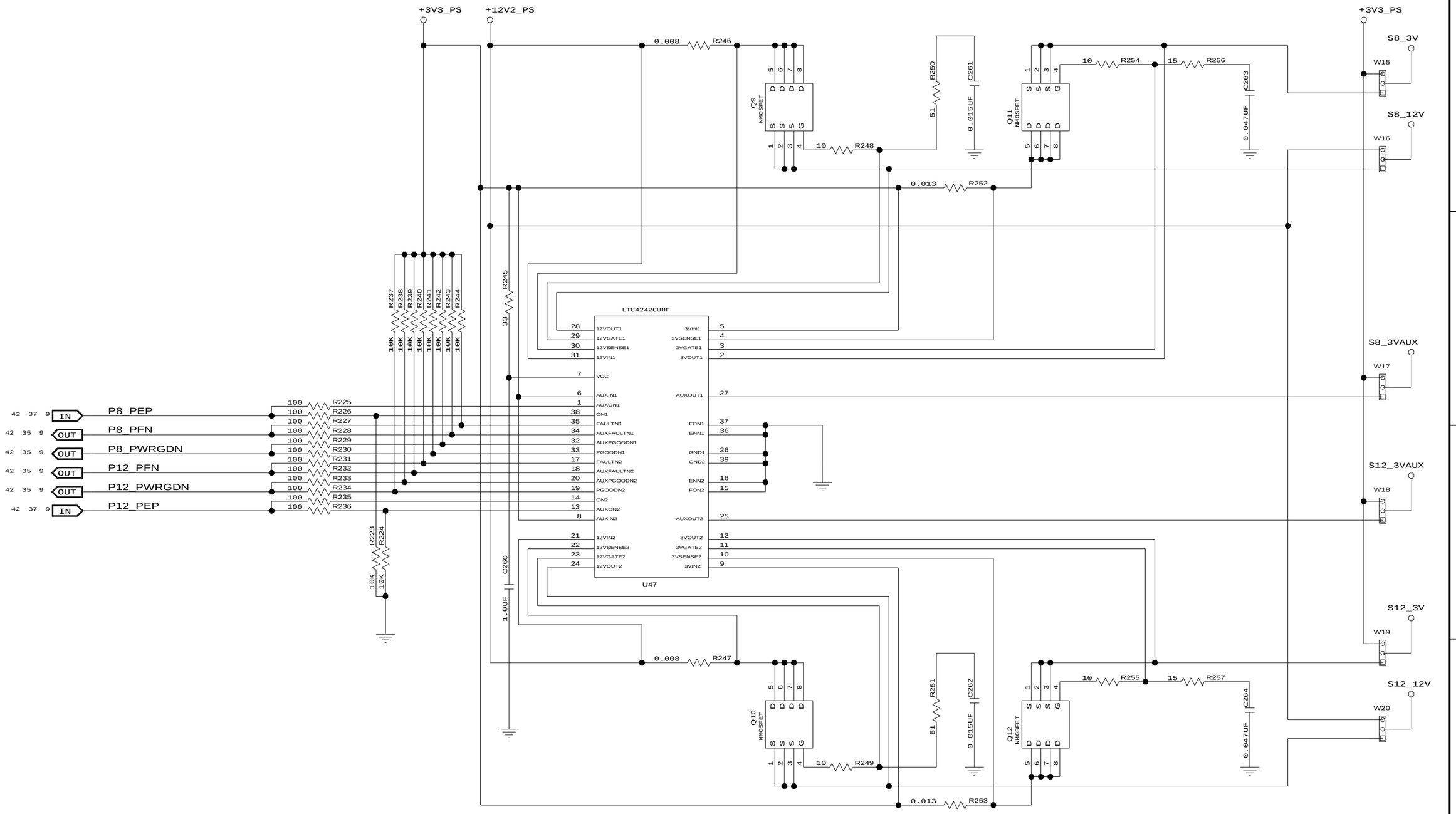


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TITLE	EB-LOGAN-23		
HOT PLUG CONTROL PORTS 4-6			
SIZE: B	DRAWING NO.: SCH-PESEB-001	FAB P/N: 18-691-001	REV.: 2.0
AUTHOR: Tony Tran		CHECKED BY: Derek Huang	
Thu Jul 01 15:00:57 2010		SHEET 16 OF 52	

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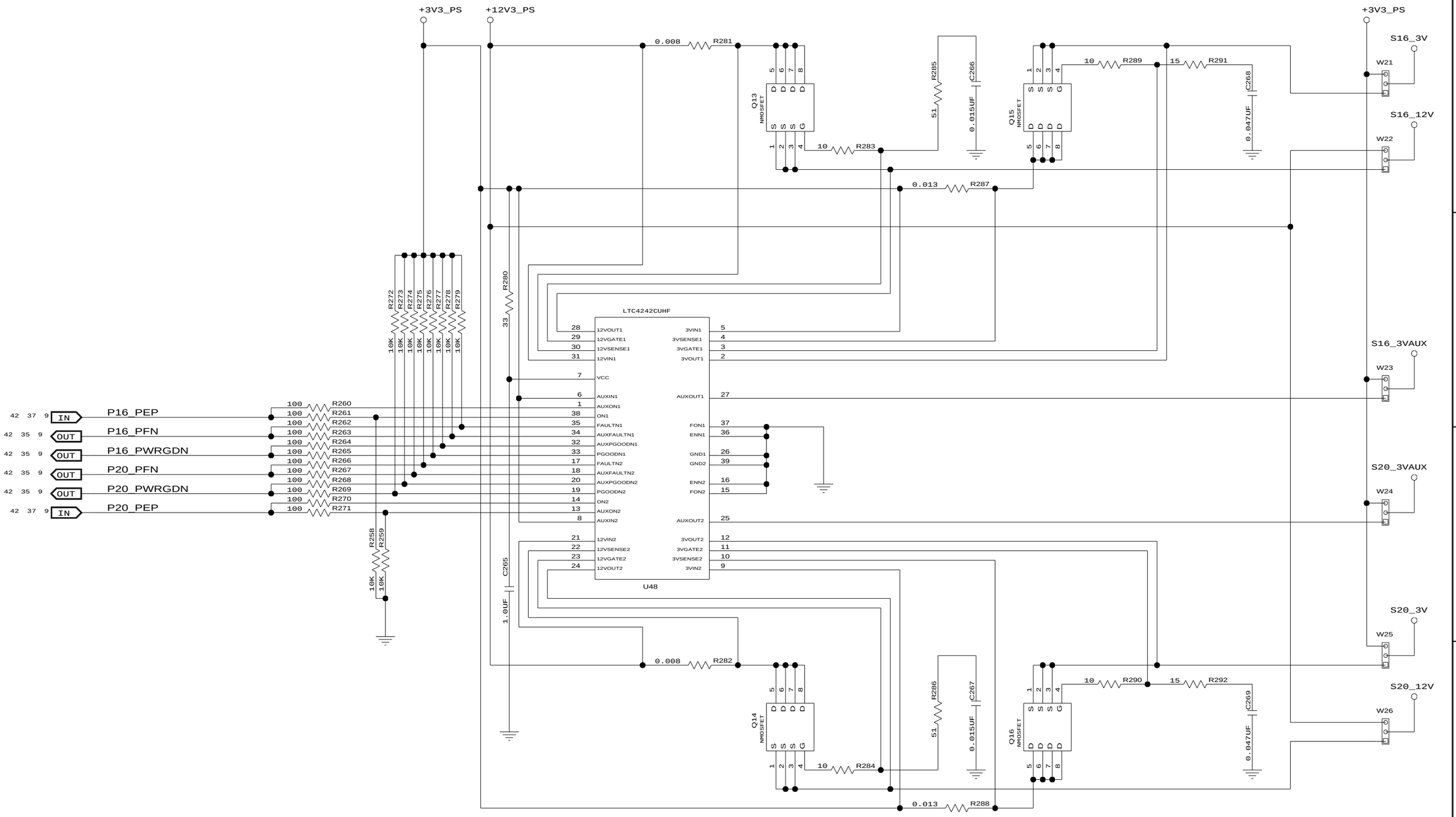


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TITLE	EB-LOGAN-23		
HOT PLUG CONTROL PORTS 8-12			
SIZE: B	DRAWING NO.: SCH-PESEB-001	FAB P/N: 18-691-001	REV.: 2.0
AUTHOR: Tony Tran		CHECKED BY: Derek Huang	
Thu Jul 01 15:00:57 2010		SHEET 17 OF 52	

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TITLE EB-LOGAN-23

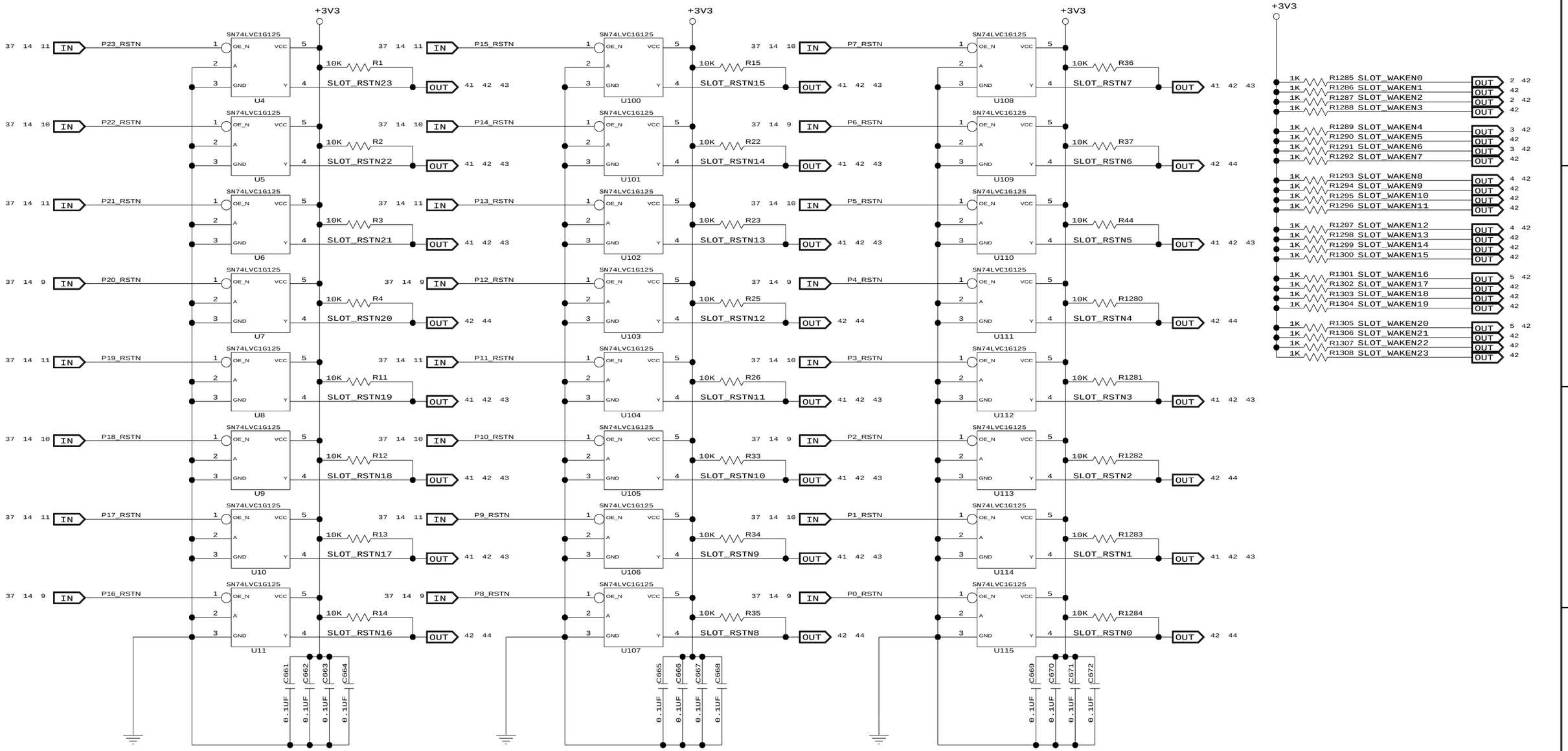
HOT PLUG CONTROL PORTS 16-20

SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-PESEB-001	18-691-001	2.0

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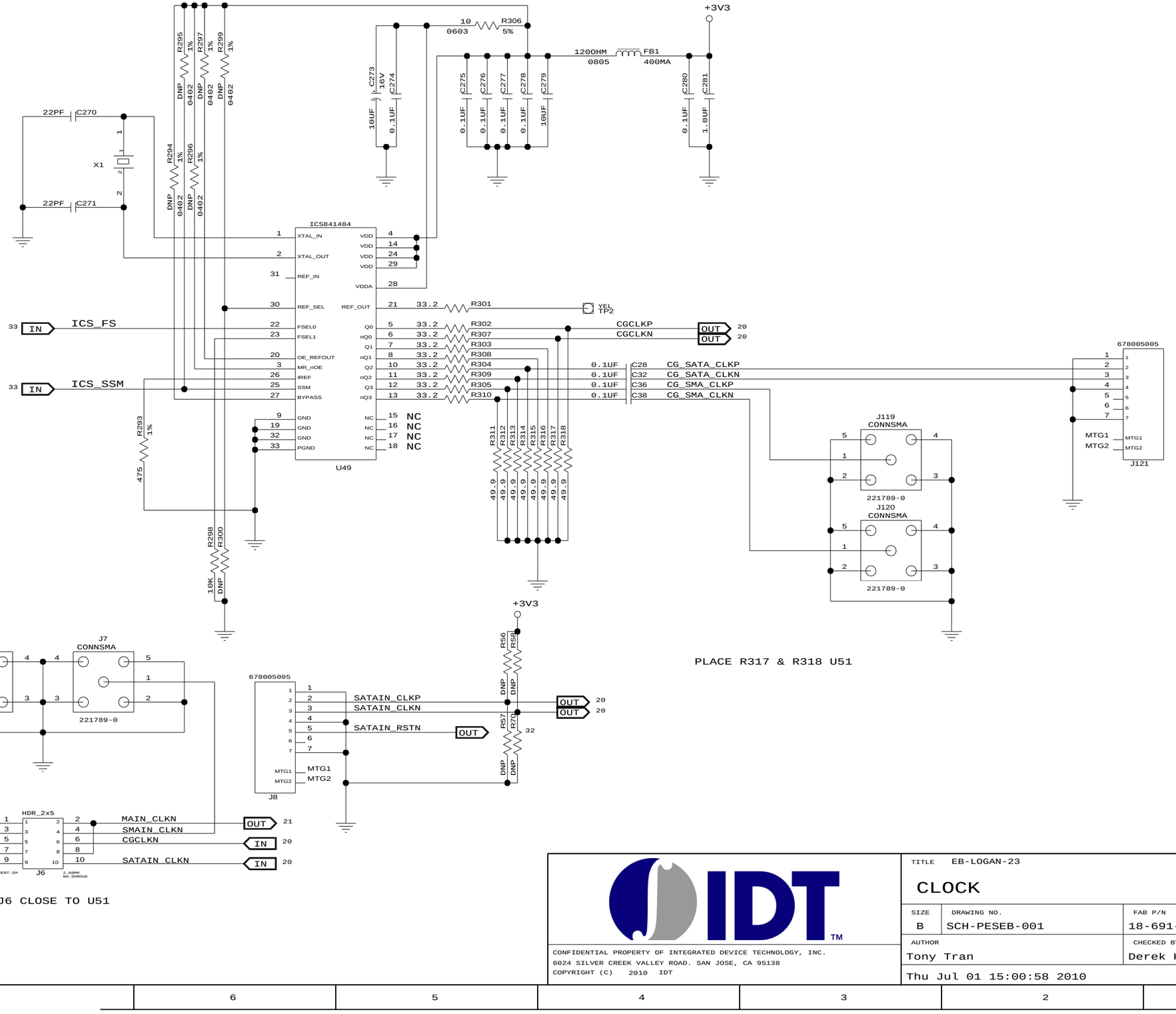
SLOT RESETS AND WAKE PULL-UPS

SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-PESEB-001	18-691-001	2.0

AUTHOR	CHECKED BY
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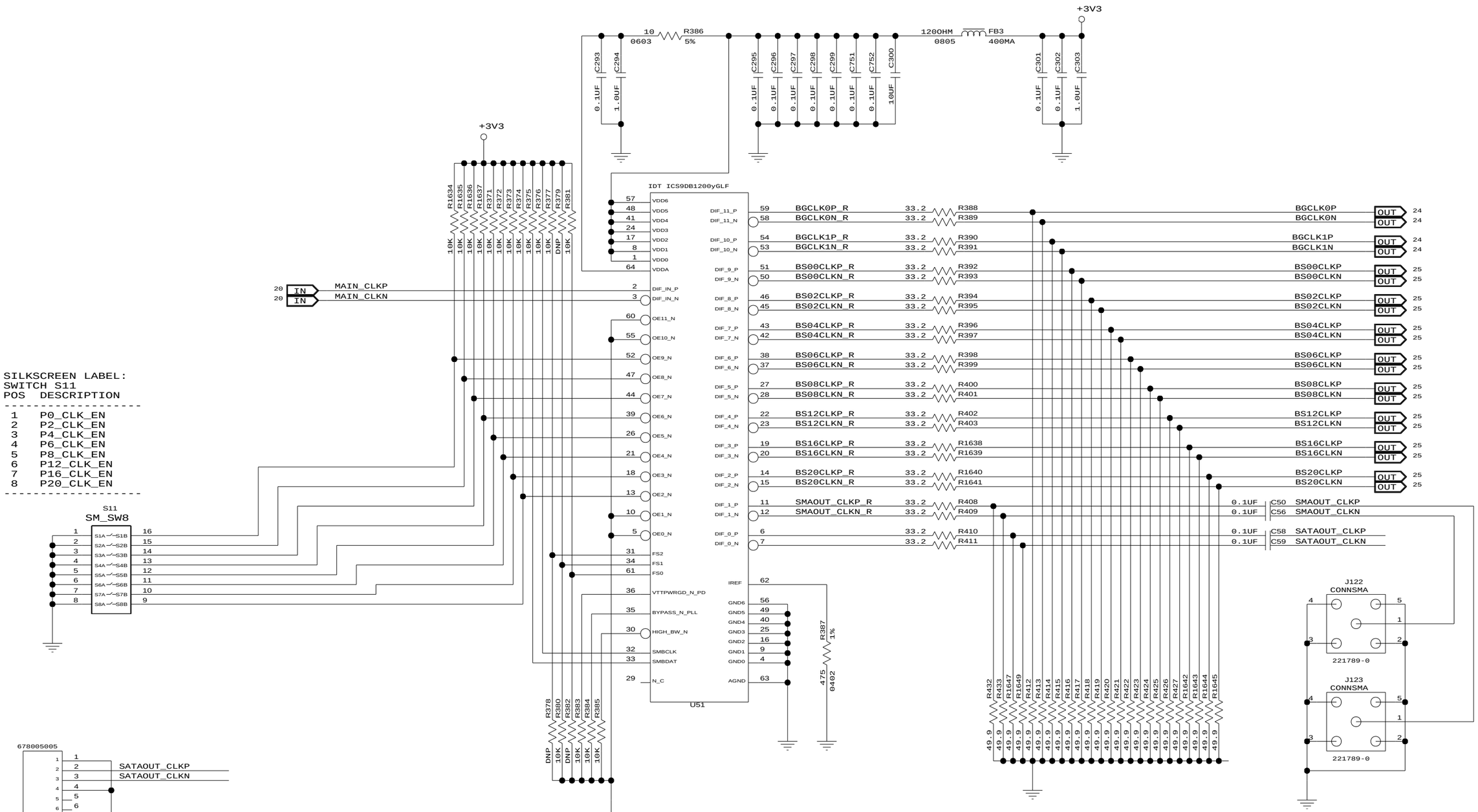
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TITLE	EB-LOGAN-23		
	CLOCK		
SIZE: B	DRAWING NO.: SCH-PESEB-001	FAB P/N: 18-691-001	REV.: 2.0
AUTHOR: Tony Tran		CHECKED BY: Derek Huang	
Thu Jul 01 15:00:58 2010		SHEET 20 OF 52	

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SILKSCREEN LABEL:
SWITCH S11
POS DESCRIPTION

1	P0_CLK_EN
2	P2_CLK_EN
3	P4_CLK_EN
4	P6_CLK_EN
5	P8_CLK_EN
6	P12_CLK_EN
7	P16_CLK_EN
8	P20_CLK_EN



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TITLE EB-LOGAN-23

CLOCK BUFFER - 1

SIZE	DRAWING NO.	FAB P/N	REV.
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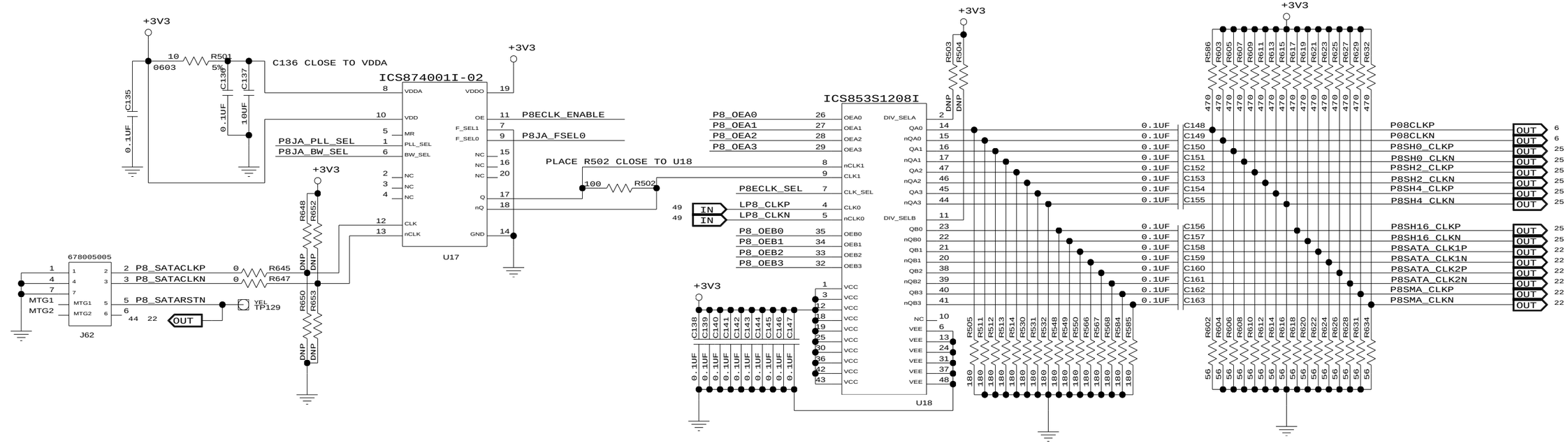
AUTHOR	CHECKED BY
Tony Tran	Derek Huang

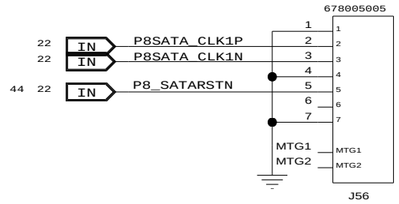
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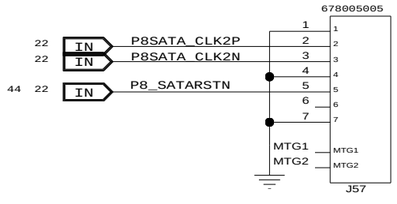
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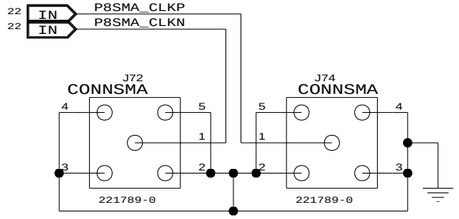
P08CLK - DUT PORT 8 CLK
LP8CLK - LOCAL CLOCK GEN. PORT 8 CLK
P8SHXXCLK - TO SLOT CLK HEADERS

PLACE 470 AND 56 OHM RESISTORS CLOSE TO DESTINATION.

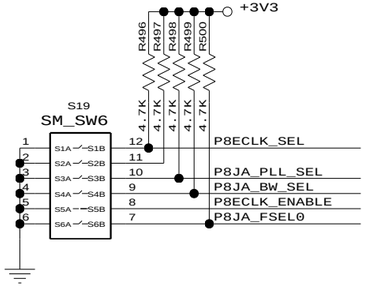




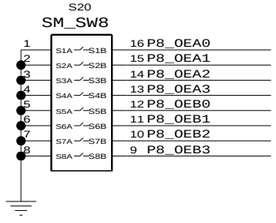




DEFAULT DIPSW SETTING
S19:1 OFF (SATACLK)
S19:3 OFF (PLL)
S19:4 OFF (2.2MHZ)
S19:5 OFF (U17 OUTPUT ON)
S19:6 ON (100MHZ)



U18 OUTPUTS
OFF (ENABLE)
ON (DISABLE)



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TITLE EB-LOGAN-23

CLOCK SELECTOR DUT PCLK 8

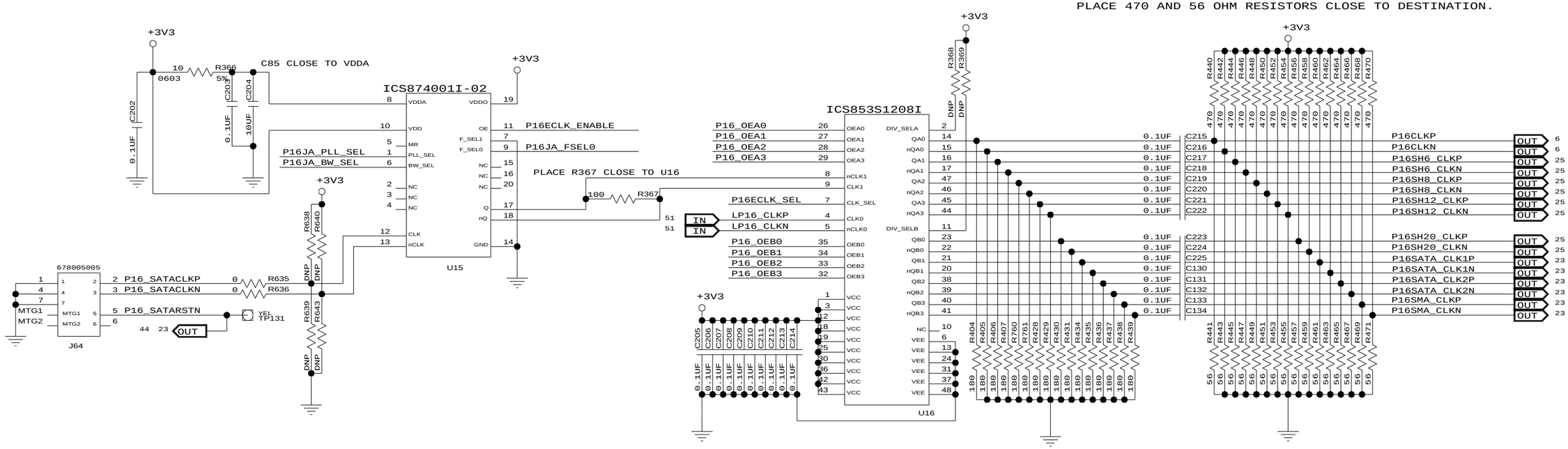
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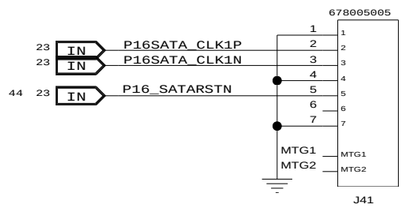
AUTHOR	CHECKED BY
Tony Tran	Derek Huang

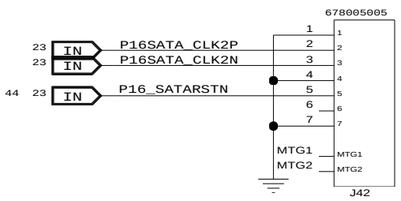
Tue Aug 10 13:51:12 2010 SHEET 22 OF 52

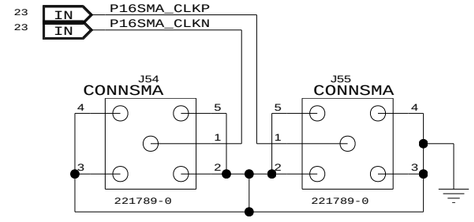
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P16CLK - DUT PORT 16 CLK
LP16CLK - LOCAL CLOCK GEN. PORT 16 CLK
P16SHXXCLK - TO SLOT CLK HEADERS



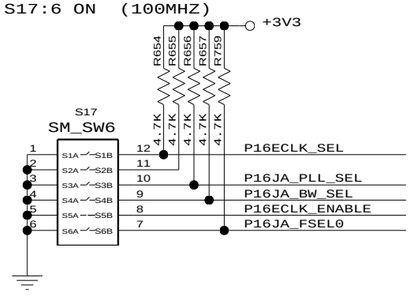




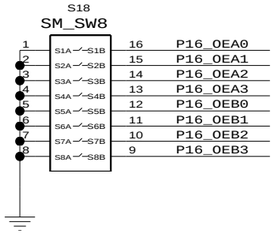


DEFAULT DIPSW SETTING

S17:1 OFF (SATACLK)
S17:3 OFF (PLL)
S17:4 OFF (2.2MHZ)
S17:5 OFF (U15 OUTPUT ON)
S17:6 ON (100MHZ)



U16 OUTPUTS
OFF (ENABLE)
ON (DISABLE)



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TITLE EB-LOGAN-23

CLOCK SELECTOR DUT PCLK 16

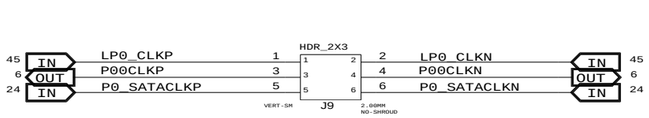
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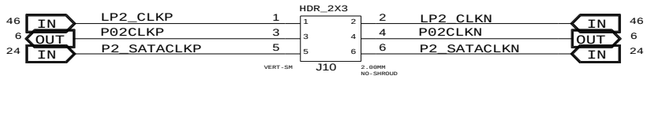
AUTHOR	CHECKED BY
Tony Tran	Derek Huang

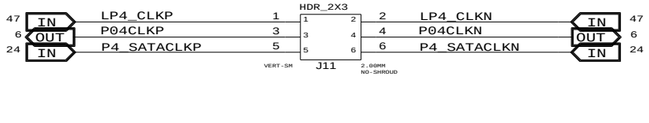
Tue Aug 10 13:51:21 2010 SHEET 23 OF 52

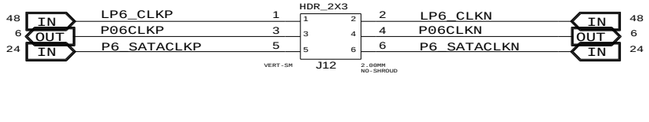
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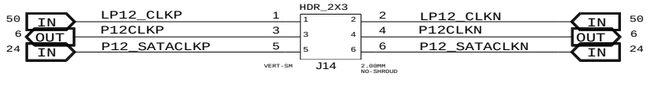
PXXCLK - DUT CLK
LPXXLCK - LOCAL CLOCK GEN. PORT CLK
SHXXCLK - SLOT HDR. CLK

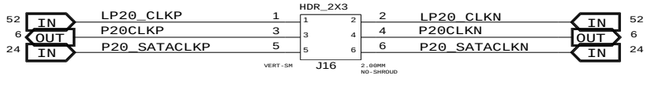


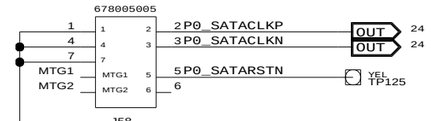


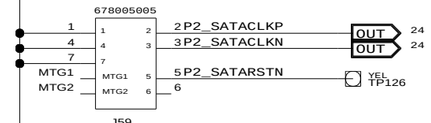


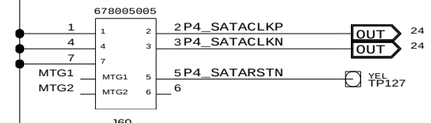


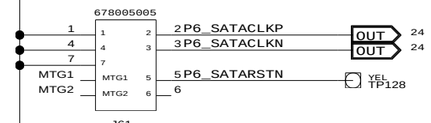


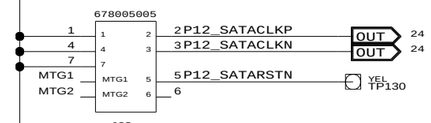


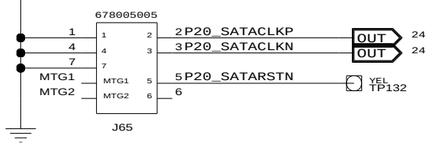


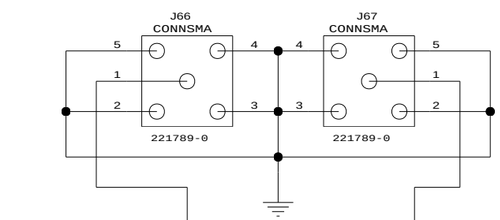


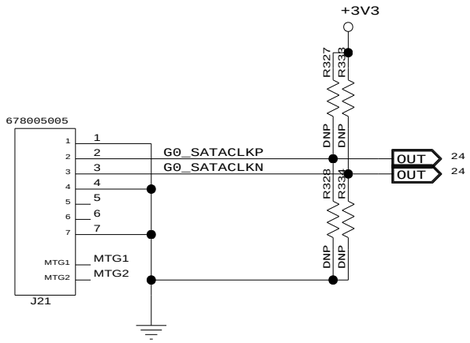


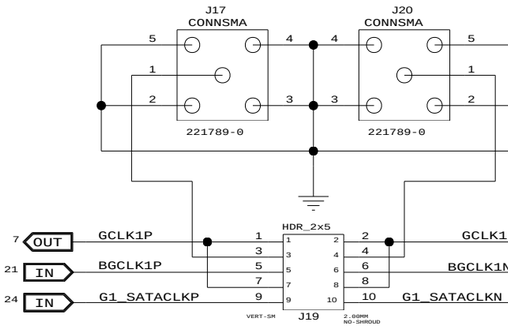


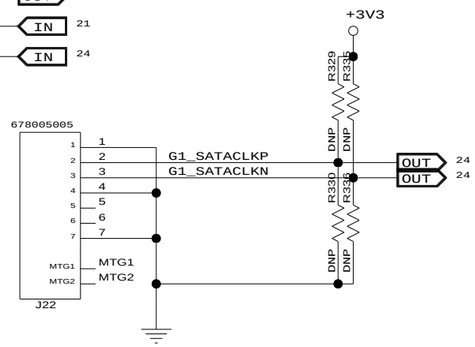


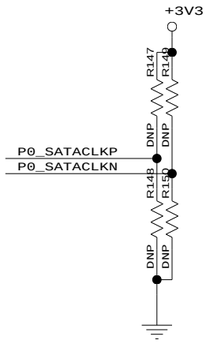


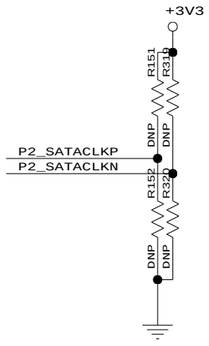


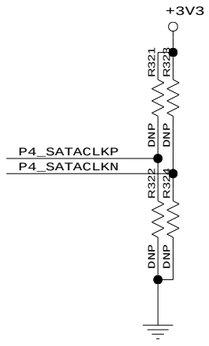


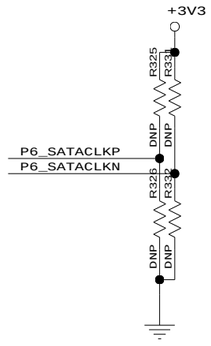


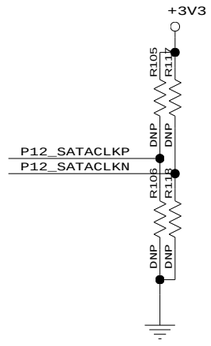


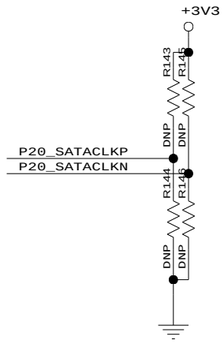










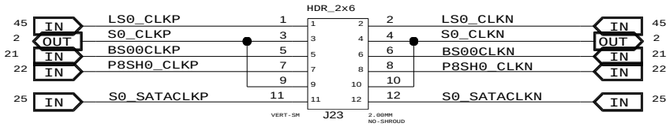


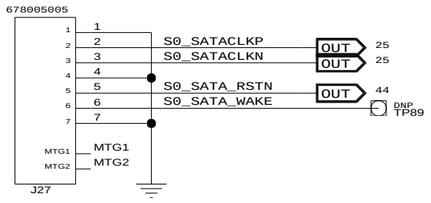
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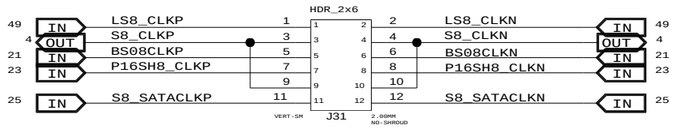
TITLE	EB-LOGAN-23		
	CLOCK SELECTOR DUT PCLK 0-20, GCLK 0-1		
SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-PESEB-001	18-691-001	2.0
AUTHOR		CHECKED BY	
Tony Tran		Derek Huang	
Thu Jul 01 15:00:59 2010		SHEET 24 OF 52	

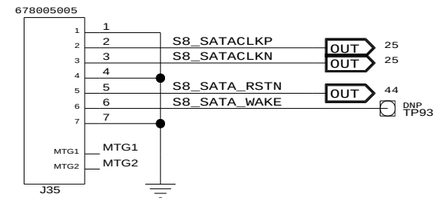
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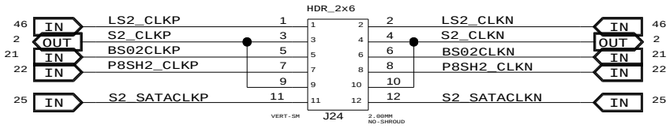
SXXCLK - SLOT CLK
BSXXLCK - BUFFER SLOT CLK
LSXXCLK - LOCAL CLOCK GEN. SLOT CLK
SHXXCLK - SLOT HDR.CLK

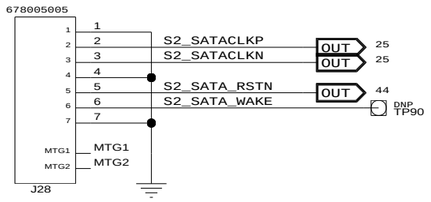


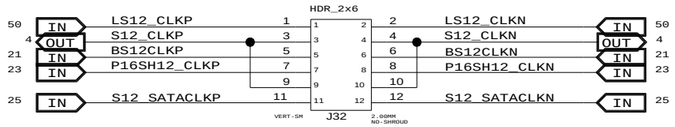


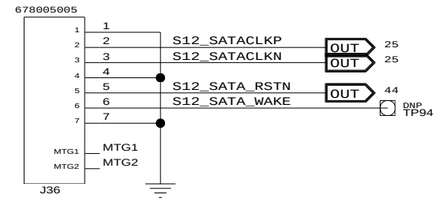


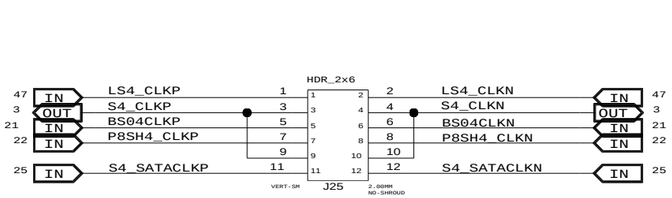


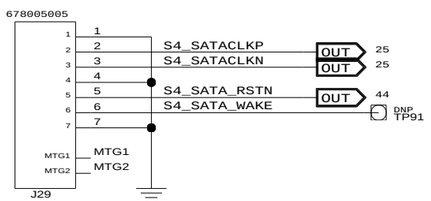


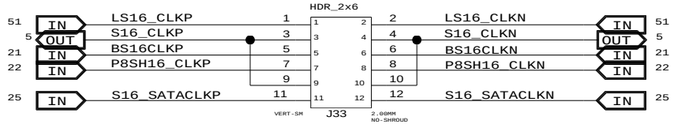


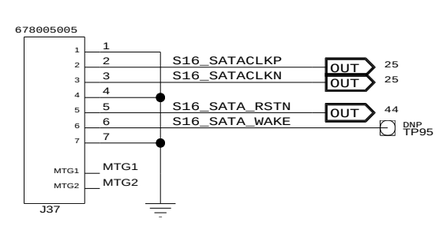


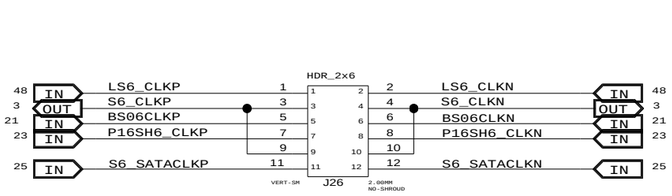


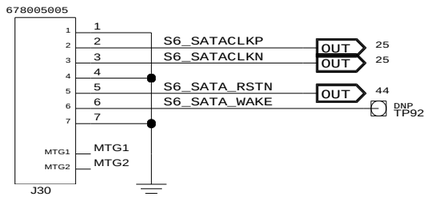


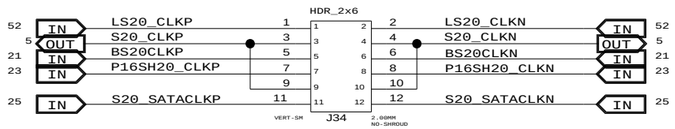


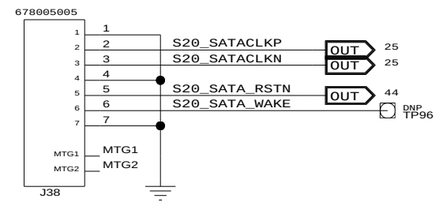












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TITLE EB-LOGAN-23

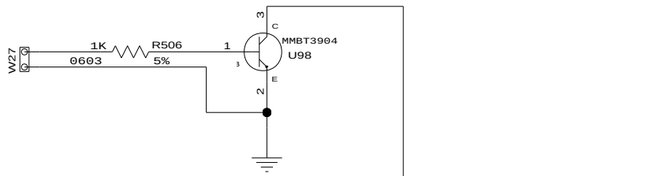
CLOCK SELECTOR SLOTS 0-20

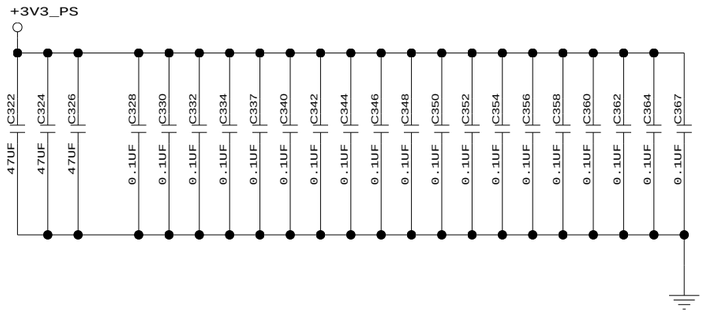
SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-PESEB-001	18-691-001	2.0

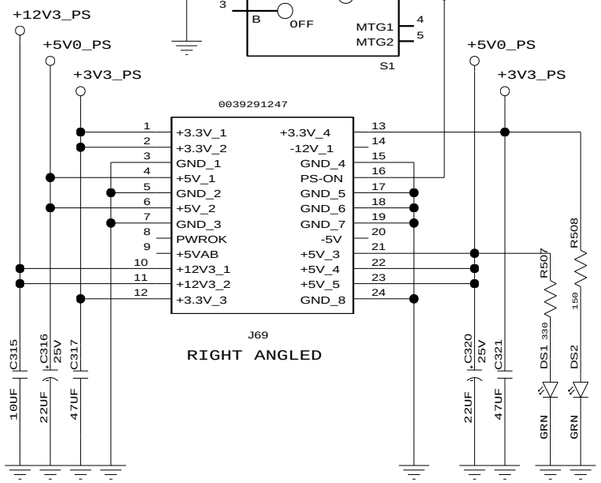
AUTHOR	CHECKED BY
Tony Tran	Derek Huang

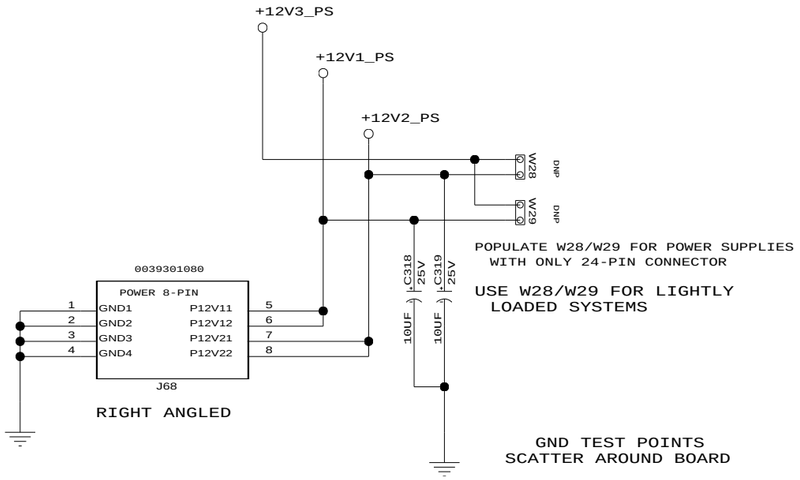
Thu Jul 01 15:00:59 2010 SHEET 25 OF 52

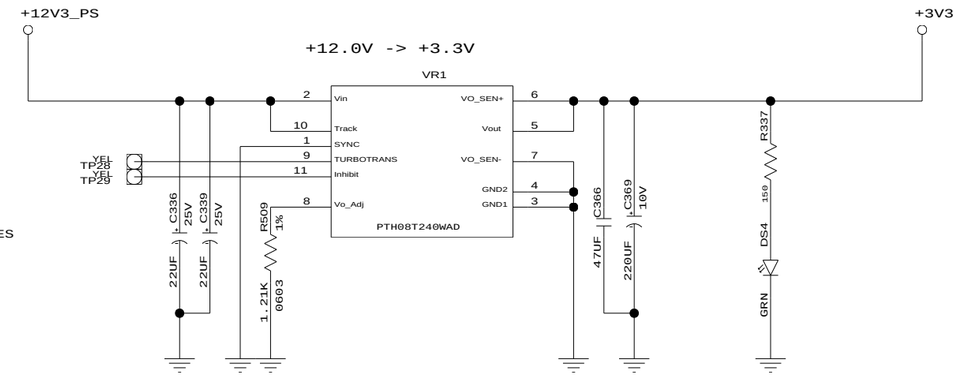
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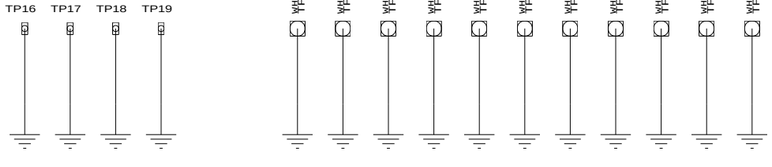












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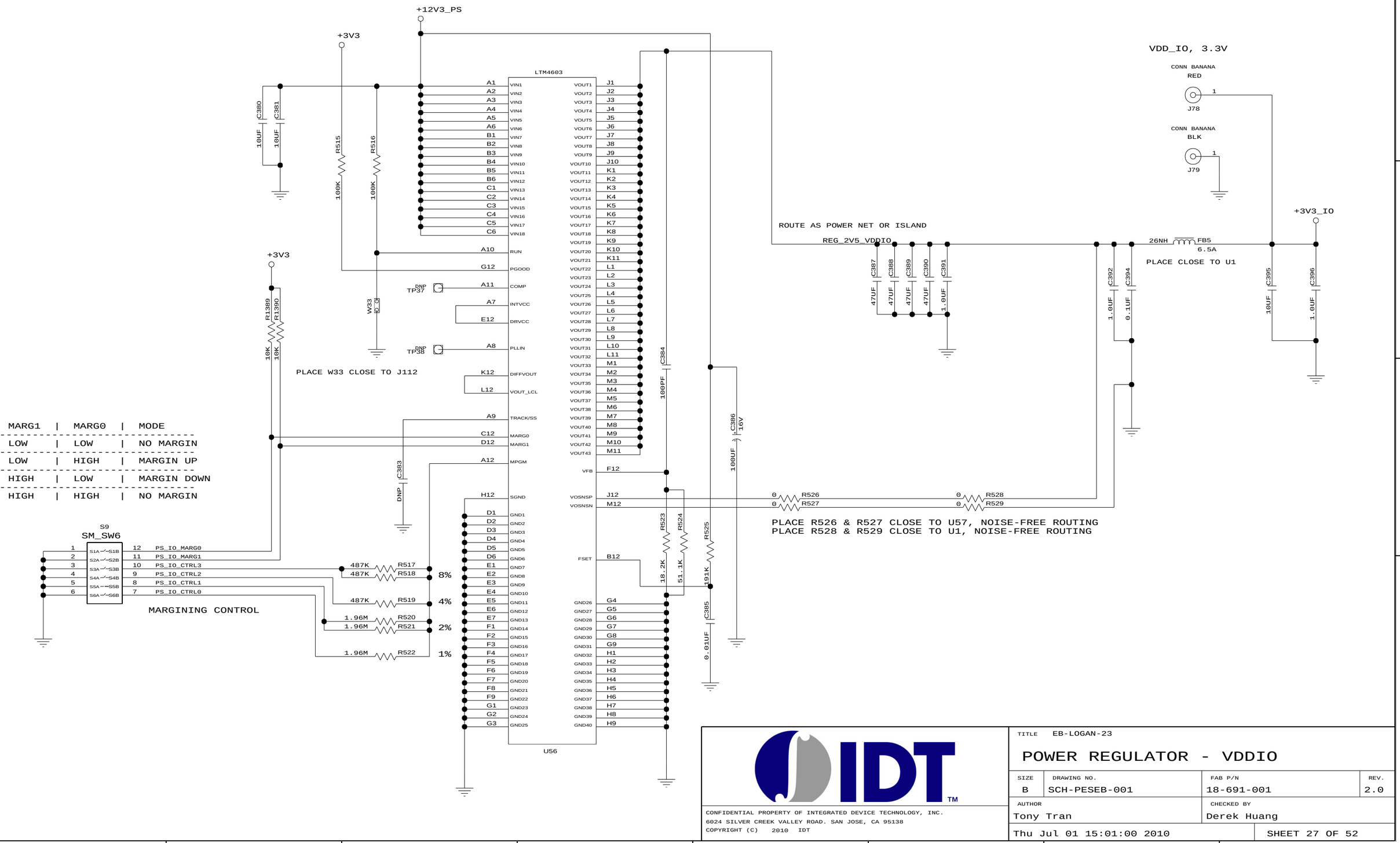
POWER CONNECTORS

SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-PESEB-001	18-691-001	2.0

AUTHOR	CHECKED BY
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Thu Jul 01 15:01:00 2010 SHEET 26 OF 52

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TITLE	EB-LOGAN-23		
POWER REGULATOR - VDDIO			
SIZE: B	DRAWING NO.: SCH-PESEB-001	FAB P/N: 18-691-001	REV.: 2.0
AUTHOR: Tony Tran		CHECKED BY: Derek Huang	
Thu Jul 01 15:01:00 2010		SHEET 27 OF 52	

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+12V3_PS

+3V3

LTM4603

C397 10UF, C398 10UF

R533 100K, R534 100K

A1 VIN1, A2 VIN2, A3 VIN3, A4 VIN4, A5 VIN5, A6 VIN6, B1 VIN7, B2 VIN8, B3 VIN9, B4 VIN10, B5 VIN11, B6 VIN12, C1 VIN13, C2 VIN14, C3 VIN15, C4 VIN16, C5 VIN17, C6 VIN18

VOUT1 J1, VOUT2 J2, VOUT3 J3, VOUT4 J4, VOUT5 J5, VOUT6 J6, VOUT7 J7, VOUT8 J8, VOUT9 J9, VOUT10 J10, VOUT11 K1, VOUT12 K2, VOUT13 K3, VOUT14 K4, VOUT15 K5, VOUT16 K6, VOUT17 K7, VOUT18 K8, VOUT19 K9, VOUT20 K10, VOUT21 K11, VOUT22 L1, VOUT23 L2, VOUT24 L3, VOUT25 L4, VOUT26 L5, VOUT27 L6, VOUT28 L7, VOUT29 L8, VOUT30 L9, VOUT31 L10, VOUT32 L11, VOUT33 M1, VOUT34 M2, VOUT35 M3, VOUT36 M4, VOUT37 M5, VOUT38 M6, VOUT39 M7, VOUT40 M8, VOUT41 M9, VOUT42 M10, VOUT43 M11

A10 RUN, G12 PGOOD, A11 COMP, A7 INTVCC, E12 DRVCC, A8 PLLIN, K12 DIFFVOUT, L12 VOUT_LCL, A9 TRACK/SS, C12 MARG0, D12 MARG1, A12 MPGM, H12 SGND, VFB F12, VOSNSP J12, VOSNSN M12, FSET B12

GND1 D1, GND2 D2, GND3 D3, GND4 D4, GND5 D5, GND6 D6, GND7 E1, GND8 E2, GND9 E3, GND10 E4, GND11 E5, GND12 E6, GND13 E7, GND14 F1, GND15 F2, GND16 F3, GND17 F4, GND18 F5, GND19 F6, GND20 F7, GND21 F8, GND22 F9, GND23 G1, GND24 G2, GND25 G3, GND26 G4, GND27 G5, GND28 G6, GND29 G7, GND30 G8, GND31 G9, GND32 H1, GND33 H2, GND34 H3, GND35 H4, GND36 H5, GND37 H6, GND38 H7, GND39 H8, GND40 H9

U59

+3V3

R1391 10K, R1392 10K

W34 0

DNP TP41, DNP TP42

PLACE W34 CLOSE TO J114

C400 DNP

C401 100PF

C403 100UF 16V

R541 127K 1%, R542 316K 1%, R543 191K

C402 0.01UF

ROUTE AS POWER NET OR ISLAND

REG_1V0_CORE

C404 47UF, C405 47UF, C406 47UF, C407 47UF, C408 1.0UF

VDD_CORE, 1.0V

CONN BANANA RED J114

CONN BANANA BLK J113

26NH FB6 6.5A

PLACE CLOSE TO U1

+1V0_CORE

C409 1.0UF, C411 0.1UF

C412 10UF, C413 1.0UF

0 R544, 0 R545

0 R546, 0 R547

PLACE R544 & R545 CLOSE TO U57, NOISE-FREE ROUTING
PLACE R546 & R547 CLOSE TO U1, NOISE-FREE ROUTING

S6
SM_SW6

1 S1A, 2 S2A, 3 S3A, 4 S4A, 5 S5A, 6 S6A — 12 S1B, 11 S2B, 10 S3B, 9 S4B, 8 S5B, 7 S6B

PS_CORE_MARG0, PS_CORE_MARG1, PS_CORE_CTRL3, PS_CORE_CTRL2, PS_CORE_CTRL1, PS_CORE_CTRL0

487K R535, 487K R536 — 8%
487K R537 — 4%
1.96M R538, 1.96M R539 — 2%
1.96M R540 — 1%

MARGINING CONTROL

MARG1	MARG0	MODE
LOW	LOW	NO MARGIN
LOW	HIGH	MARGIN UP
HIGH	LOW	MARGIN DOWN
HIGH	HIGH	NO MARGIN

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TITLE EB-LOGAN-23

POWER REGULATOR - VDDCORE

SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-PESEB-001	18-691-001	2.0

AUTHOR	CHECKED BY
Tony Tran	Derek Huang

Thu Jul 01 15:01:00 2010 SHEET 28 OF 52

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+12V3_PS

+3V3

LTM4603

C414 10UF
C415 10UF
R551 100K
R552 100K

A1 VIN1
A2 VIN2
A3 VIN3
A4 VIN4
A5 VIN5
A6 VIN6
B1 VIN7
B2 VIN8
B3 VIN9
B4 VIN10
B5 VIN11
B6 VIN12
C1 VIN13
C2 VIN14
C3 VIN15
C4 VIN16
C5 VIN17
C6 VIN18

A10 RUN
G12 PGOOD
A11 COMP — DNP TP45
A7 INTVCC
E12 DRVCC
A8 PLLIN — DNP TP46
K12 DIFFVOUT
L12 VOUT_LCL
A9 TRACK/SS
C12 MARG0
D12 MARG1
A12 MPGM
H12 SGND
VFB F12
VOSNSP J12
VOSNSN M12
FSET B12

D1 GND1
D2 GND2
D3 GND3
D4 GND4
D5 GND5
D6 GND6
E1 GND7
E2 GND8
E3 GND9
E4 GND10
E5 GND11
E6 GND12
E7 GND13
F1 GND14
F2 GND15
F3 GND16
F4 GND17
F5 GND18
F6 GND19
F7 GND20
F8 GND21
F9 GND22
G1 GND23
G2 GND24
G3 GND25
GND26 G4
GND27 G5
GND28 G6
GND29 G7
GND30 G8
GND31 G9
GND32 H1
GND33 H2
GND34 H3
GND35 H4
GND36 H5
GND37 H6
GND38 H7
GND39 H8
GND40 H9

VOUT1 J1
VOUT2 J2
VOUT3 J3
VOUT4 J4
VOUT5 J5
VOUT6 J6
VOUT7 J7
VOUT8 J8
VOUT9 J9
VOUT10 J10
VOUT11 K1
VOUT12 K2
VOUT13 K3
VOUT14 K4
VOUT15 K5
VOUT16 K6
VOUT17 K7
VOUT18 K8
VOUT19 K9
VOUT20 K10
VOUT21 K11
VOUT22 L1
VOUT23 L2
VOUT24 L3
VOUT25 L4
VOUT26 L5
VOUT27 L6
VOUT28 L7
VOUT29 L8
VOUT30 L9
VOUT31 L10
VOUT32 L11
VOUT33 M1
VOUT34 M2
VOUT35 M3
VOUT36 M4
VOUT37 M5
VOUT38 M6
VOUT39 M7
VOUT40 M8
VOUT41 M9
VOUT42 M10
VOUT43 M11

U62

+3V3
R1393 10K
R1394 10K
W35 0 Ω
PLACE W35 CLOSE TO J115

C417 DNP
C418 100PF
C420 16V 100UF
R559 127K 1%
R560 316K 1%
R561 191K
C419 0.01UF

MARG1	MARG0	MODE
LOW	LOW	NO MARGIN
LOW	HIGH	MARGIN UP
HIGH	LOW	MARGIN DOWN
HIGH	HIGH	NO MARGIN

S7
SM_SW6

1 S1A — S1B 12 PS_PEA_MARG0
2 S2A — S2B 11 PS_PEA_MARG1
3 S3A — S3B 10 PS_PEA_CTRL3
4 S4A — S4B 9 PS_PEA_CTRL2
5 S5A — S5B 8 PS_PEA_CTRL1
6 S6A — S6B 7 PS_PEA_CTRL0

487K R553
487K R554 — 8%
487K R555 — 4%
1.96M R556
1.96M R557 — 2%
1.96M R558 — 1%

MARGINING CONTROL

ROUTE AS POWER NET OR ISLAND

REG_1V0_PEA
C421 47UF
C422 47UF
C423 47UF
C424 47UF
C425 1.0UF

26NH FB7 6.5A
PLACE CLOSE TO U1

C426 1.0UF
C428 0.1UF
C429 10UF
C430 1.0UF

+1V0_PEA

VDD_PEA, 1.0V
CONN BANANA
RED
J115

0 R562
0 R563
0 R564
0 R565

PLACE R562 & R563 CLOSE TO U60, NOISE-FREE ROUTING
PLACE R564 & R565 CLOSE TO U1, NOISE-FREE ROUTING

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TITLE EB-LOGAN-23

POWER REGULATOR - VDDPEA

SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-PESEB-001	18-691-001	2.0

AUTHOR	CHECKED BY
Tony Tran	Derek Huang

Thu Jul 01 15:01:00 2010 | SHEET 29 OF 52

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+12V3_PS

+3V3

LTM4603

C431 10UF
C432 10UF
R569 100K
R570 100K

A1 VIN1
A2 VIN2
A3 VIN3
A4 VIN4
A5 VIN5
A6 VIN6
B1 VIN7
B2 VIN8
B3 VIN9
B4 VIN10
B5 VIN11
B6 VIN12
C1 VIN13
C2 VIN14
C3 VIN15
C4 VIN16
C5 VIN17
C6 VIN18

A10 RUN
G12 PGOOD
A11 COMP
A7 INTVCC
E12 DRVCC
A8 PLLIN
K12 DIFFVOUT
L12 VOUT_LCL
A9 TRACK/SS
C12 MARG0
D12 MARG1
A12 MPGM
H12 SGND

VOUT1 J1
VOUT2 J2
VOUT3 J3
VOUT4 J4
VOUT5 J5
VOUT6 J6
VOUT7 J7
VOUT8 J8
VOUT9 J9
VOUT10 J10
VOUT11 K1
VOUT12 K2
VOUT13 K3
VOUT14 K4
VOUT15 K5
VOUT16 K6
VOUT17 K7
VOUT18 K8
VOUT19 K9
VOUT20 K10
VOUT21 K11
VOUT22 L1
VOUT23 L2
VOUT24 L3
VOUT25 L4
VOUT26 L5
VOUT27 L6
VOUT28 L7
VOUT29 L8
VOUT30 L9
VOUT31 L10
VOUT32 L11
VOUT33 M1
VOUT34 M2
VOUT35 M3
VOUT36 M4
VOUT37 M5
VOUT38 M6
VOUT39 M7
VOUT40 M8
VOUT41 M9
VOUT42 M10
VOUT43 M11
VFB F12
VOSNSP J12
VOSNSN M12
FSET B12
GND26 G4
GND27 G5
GND28 G6
GND29 G7
GND30 G8
GND31 G9
GND32 H1
GND33 H2
GND34 H3
GND35 H4
GND36 H5
GND37 H6
GND38 H7
GND39 H8
GND40 H9
GND1 D1
GND2 D2
GND3 D3
GND4 D4
GND5 D5
GND6 D6
GND7 E1
GND8 E2
GND9 E3
GND10 E4
GND11 E5
GND12 E6
GND13 E7
GND14 F1
GND15 F2
GND16 F3
GND17 F4
GND18 F5
GND19 F6
GND20 F7
GND21 F8
GND22 F9
GND23 G1
GND24 G2
GND25 G3

U65

+3V3
R1395 10K
R1396 10K
W36 0
PLACE W36 CLOSE TO J116

DNP TP49
DNP TP50

C435 100PF
C437 100UF 16V
C434 DNP
R577 42.2K
R578 34.8K
R579 DNP
C436 0.01UF

ROUTE AS POWER NET OR ISLAND
REG_2V5_PEHA

C438 47UF
C439 47UF
C440 47UF
C441 47UF
C442 1.0UF

26NH FB8 6.5A
PLACE CLOSE TO U1

C443 1.0UF
C445 0.1UF
C446 10UF
C447 1.0UF

+2V5_PEHA

VDD_PEHA, 2.5V
CONN BANANA
RED
J116

0 R580
0 R581
0 R582
0 R583

PLACE R580 & R581 CLOSE TO U63, NOISE-FREE ROUTING
PLACE R582 & R583 CLOSE TO U1, NOISE-FREE ROUTING

MARG1	MARG0	MODE
LOW	LOW	NO MARGIN
LOW	HIGH	MARGIN UP
HIGH	LOW	MARGIN DOWN
HIGH	HIGH	NO MARGIN

S8
SM_SW6

1 S1A — S1B 12 PS_PEHA_MARG0
2 S2A — S2B 11 PS_PEHA_MARG1
3 S3A — S3B 10 PS_PEHA_CTRL3
4 S4A — S4B 9 PS_PEHA_CTRL2
5 S5A — S5B 8 PS_PEHA_CTRL1
6 S6A — S6B 7 PS_PEHA_CTRL0

487K R571
487K R572 8%
487K R573 4%
1.96M R574
1.96M R575 2%
1.96M R576 1%

MARGINING CONTROL

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TITLE EB-LOGAN-23

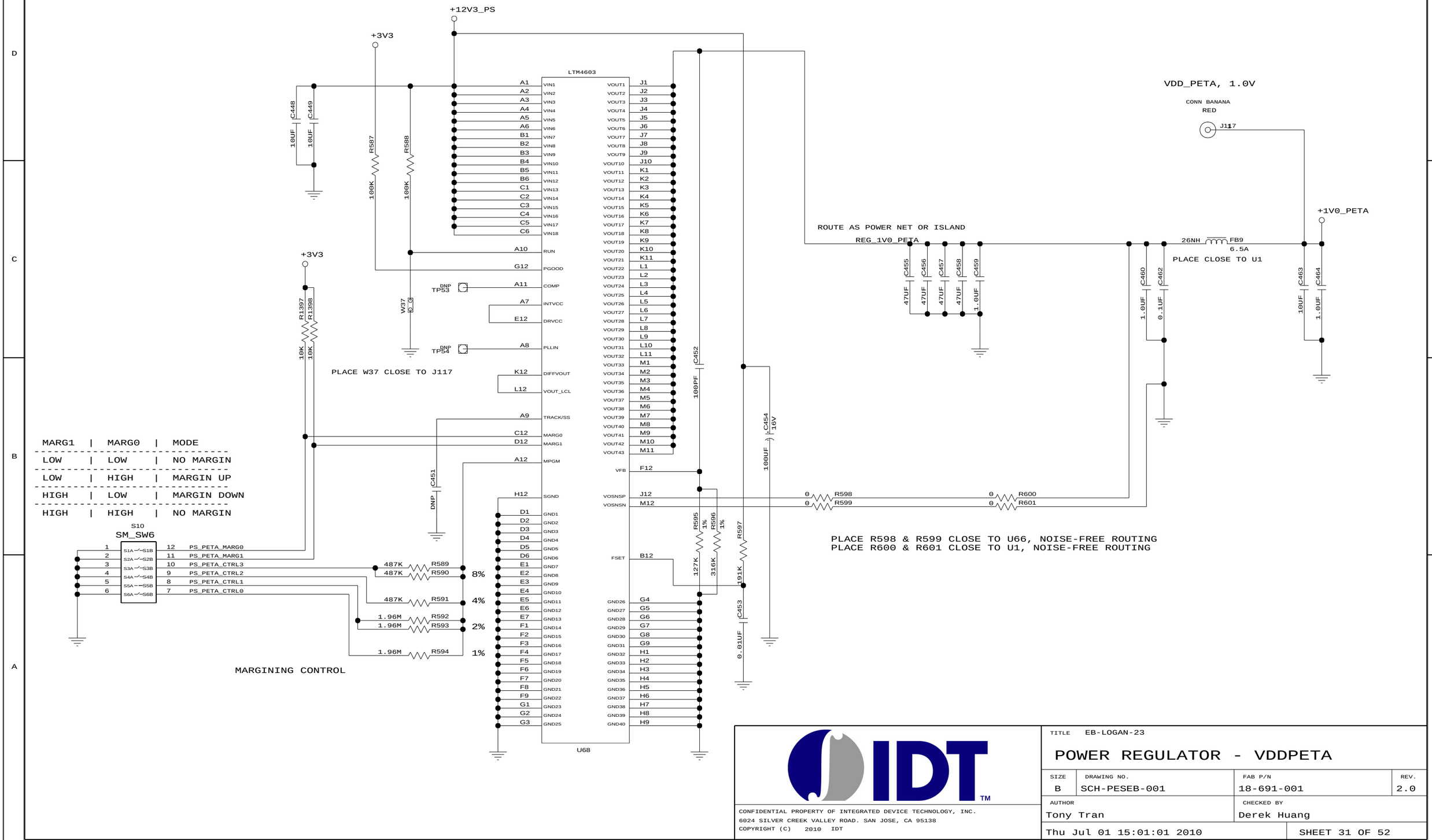
POWER REGULATOR - VDDPEHA

SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-PESEB-001	18-691-001	2.0

AUTHOR	CHECKED BY
Tony Tran	Derek Huang

Thu Jul 01 15:01:01 2010 SHEET 30 OF 52

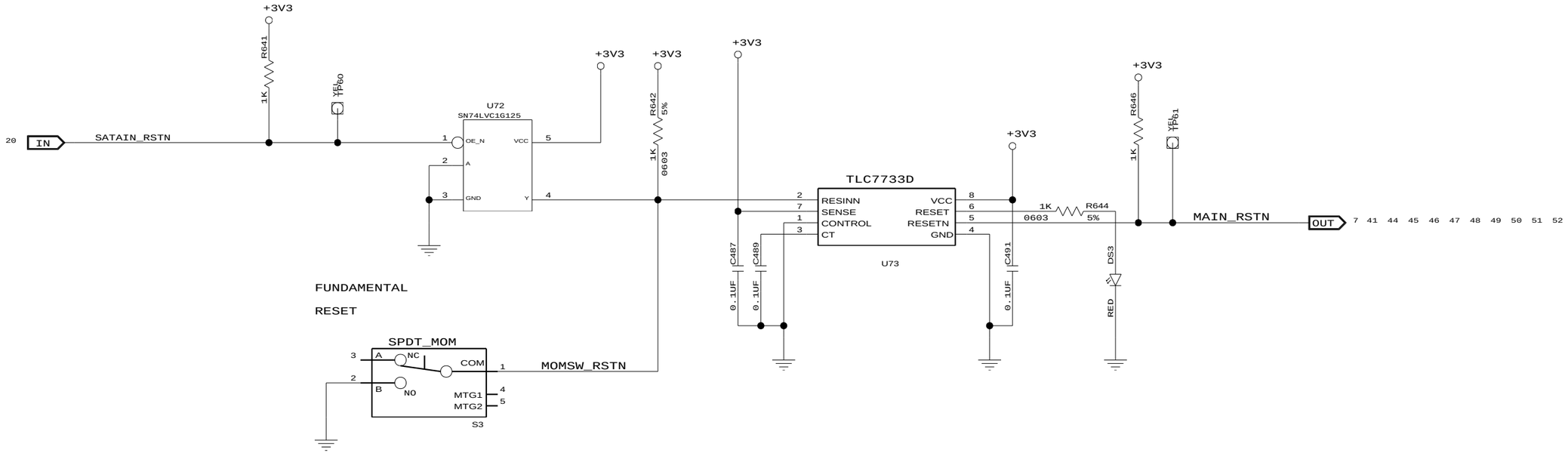
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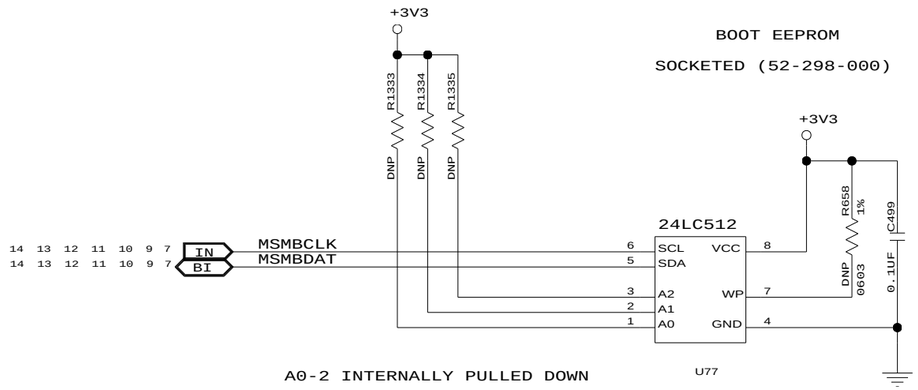


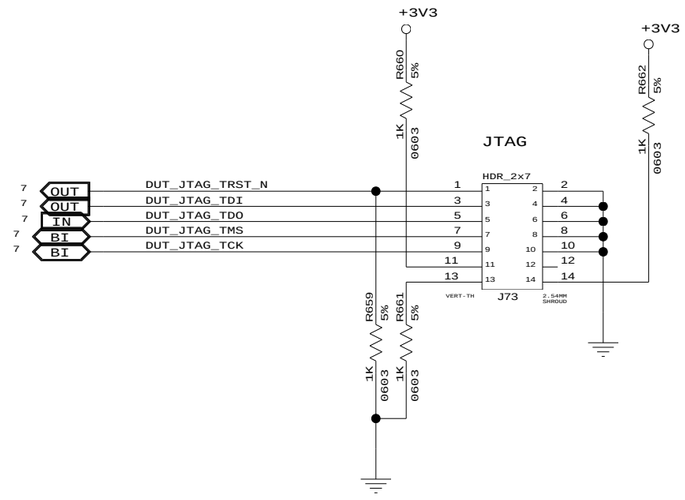
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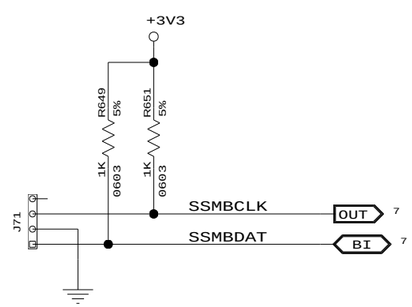
TITLE	EB-LOGAN-23		
POWER REGULATOR - VDDPETA			
SIZE: B	DRAWING NO.: SCH-PESEB-001	FAB P/N: 18-691-001	REV.: 2.0
AUTHOR: Tony Tran		CHECKED BY: Derek Huang	
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TITLE EB-LOGAN-23

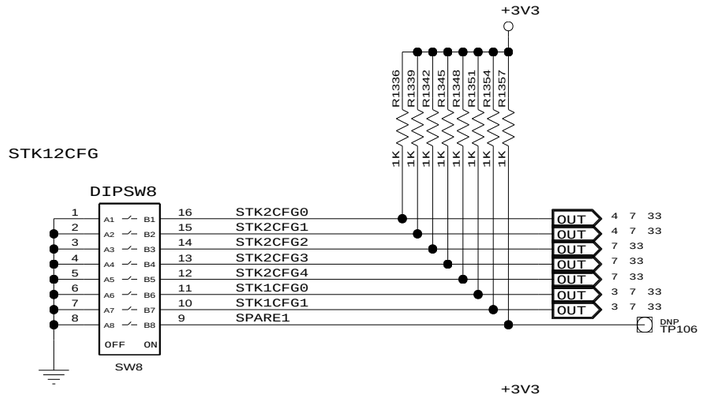
RESET, SMBUS, EEPROM, JTAG

SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-PESEB-001	18-691-001	2.0

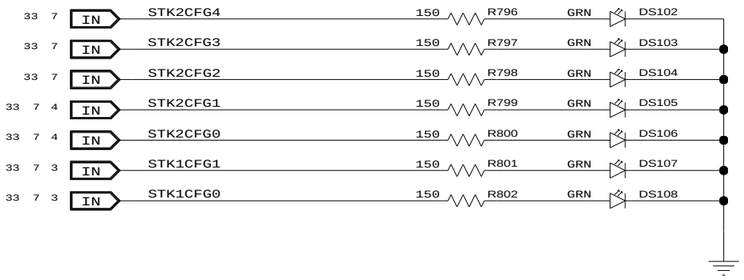
AUTHOR	CHECKED BY
Tony Tran	Derek Huang

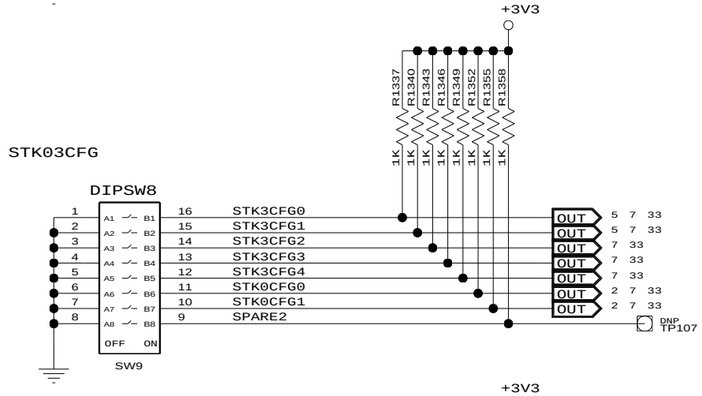
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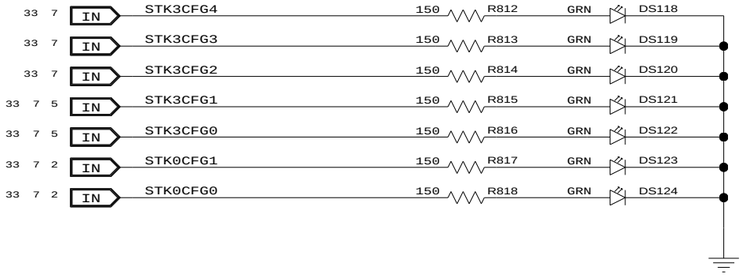


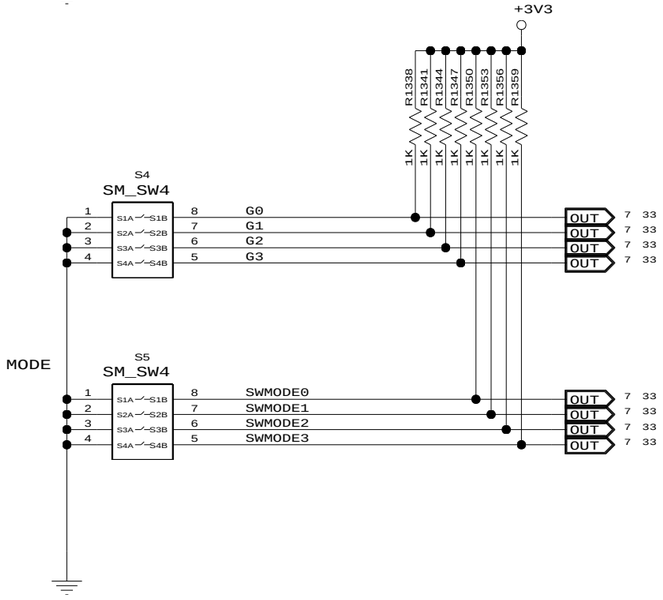
(GREEN) ACTIVE HIGH - DIP STK12CFG



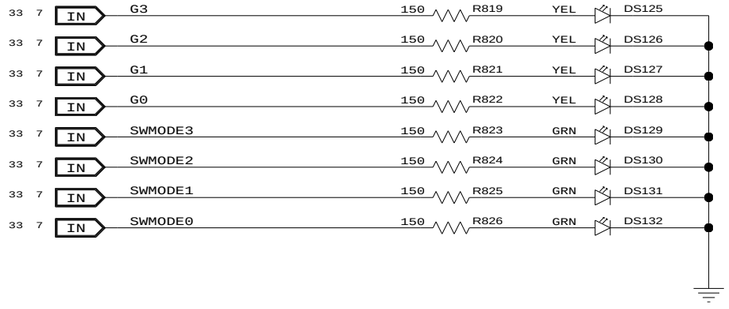


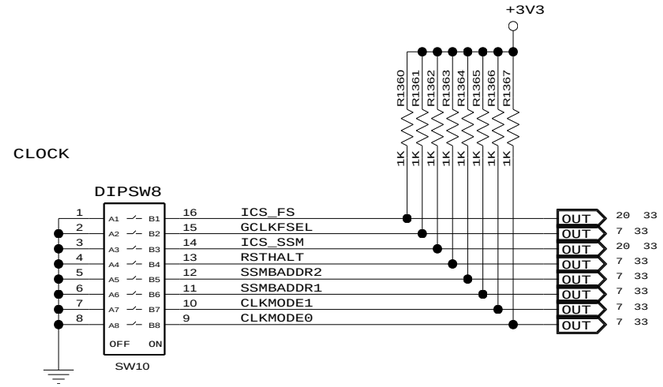
(GREEN) ACTIVE HIGH - DIP STK03CFG



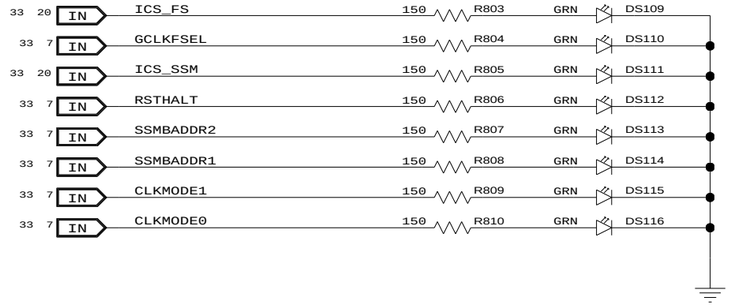


(GREEN) ACTIVE HIGH - DIP MODE





(GREEN) ACTIVE HIGH - DIP CLOCK



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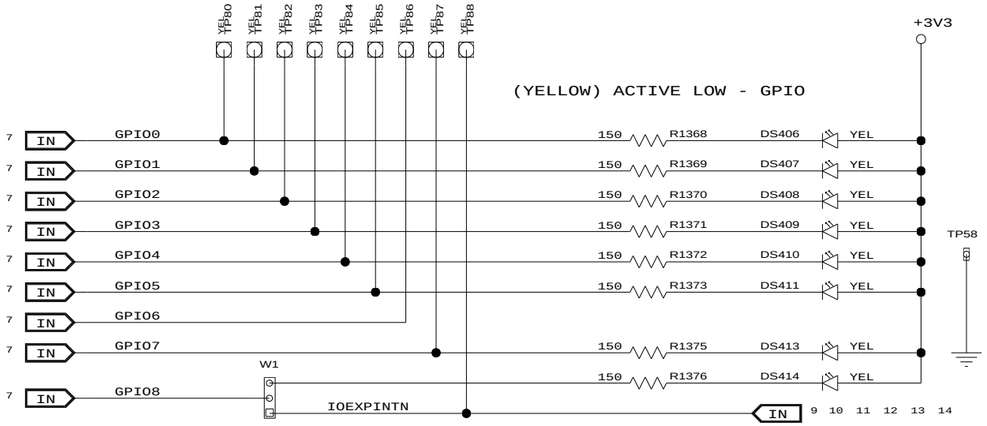
DIP SWITCHES

SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-PESEB-001	18-691-001	2.0

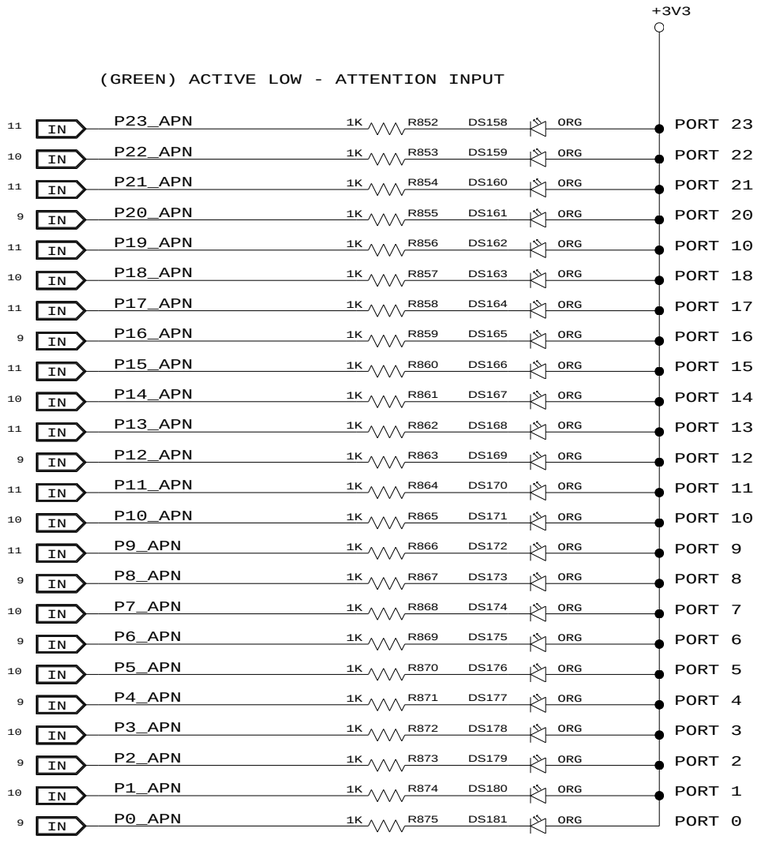
AUTHOR	CHECKED BY
Tony Tran	Derek Huang

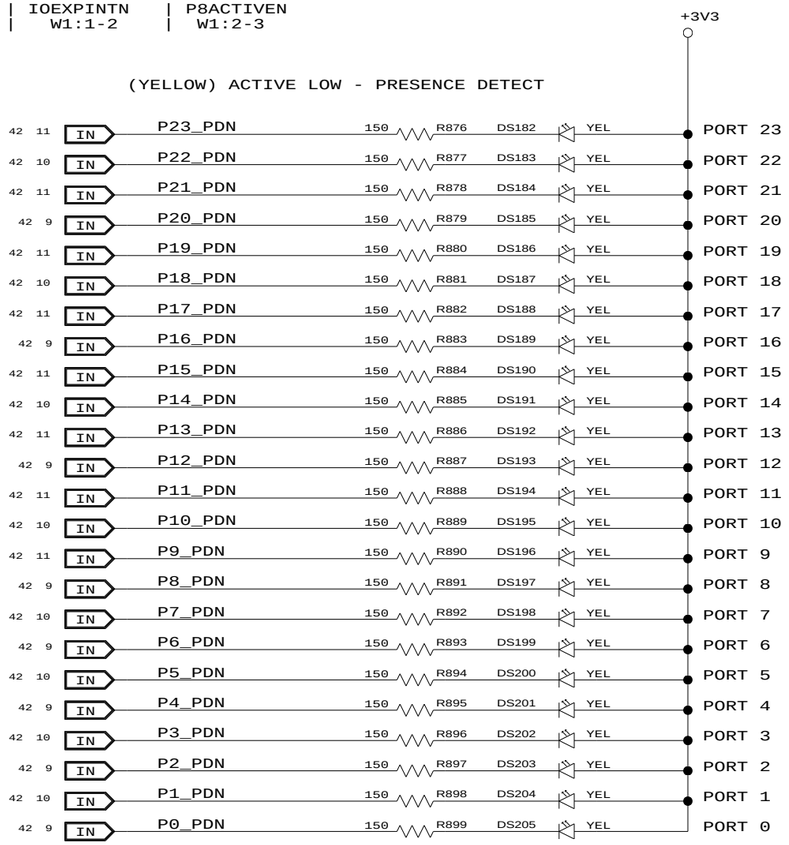
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GPIO	ALT0	ALT1
0	PART0PERSTN	P16LINKUPN
1	PART1PERSTN	P16ACTIVEN
2	PART2PERSTN	P4LINKUPN
3	PART3PERSTN	P4ACTIVEN
4	FAILOVER0	P0LINKUPN
5	GPEN	P0ACTIVEN
6	FAILOVER1	FAILOVER3
7	FAILOVER2	P8LINKUPN
8	IOEXPINTN W1:1-2	P8ACTIVEN W1:2-3





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TITLE EB-LOGAN-23

LED - PORT STATUS (1 OF 7)

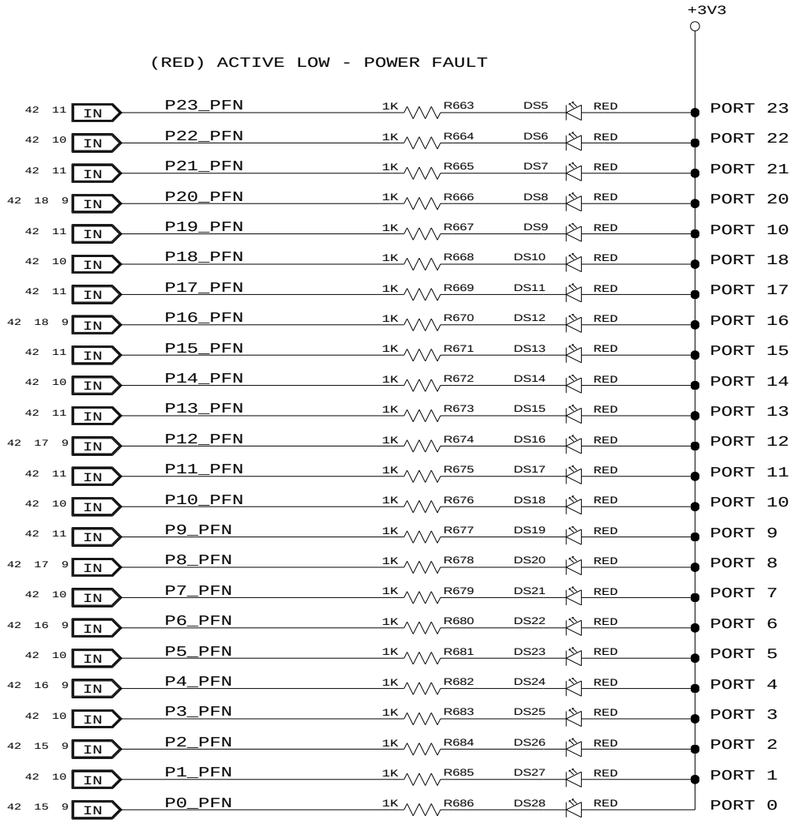
SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-PESEB-001	18-691-001	2.0

AUTHOR	CHECKED BY
Tony Tran	Derek Huang

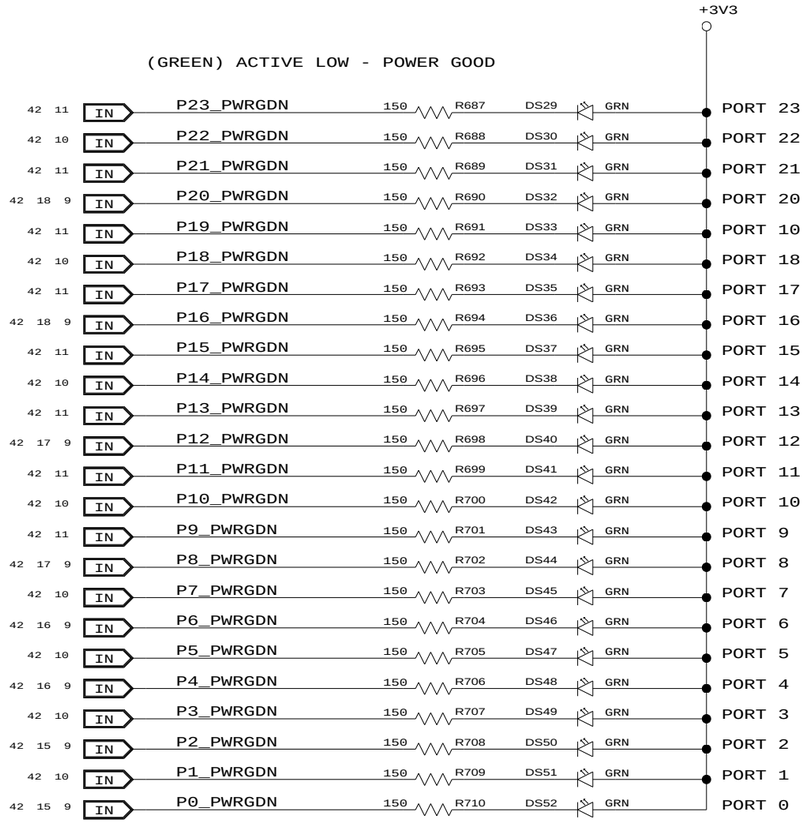
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(RED) ACTIVE LOW - POWER FAULT



(GREEN) ACTIVE LOW - POWER GOOD



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LED - PORT STATUS (2 OF 7)

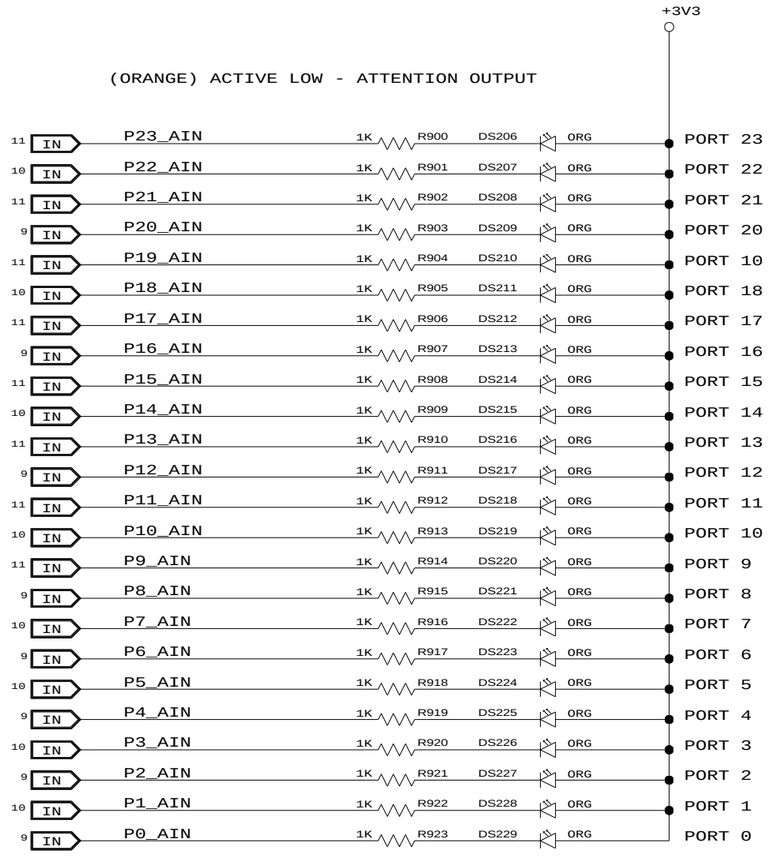
SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-PESEB-001	18-691-001	2.0

AUTHOR	CHECKED BY
Tony Tran	Derek Huang

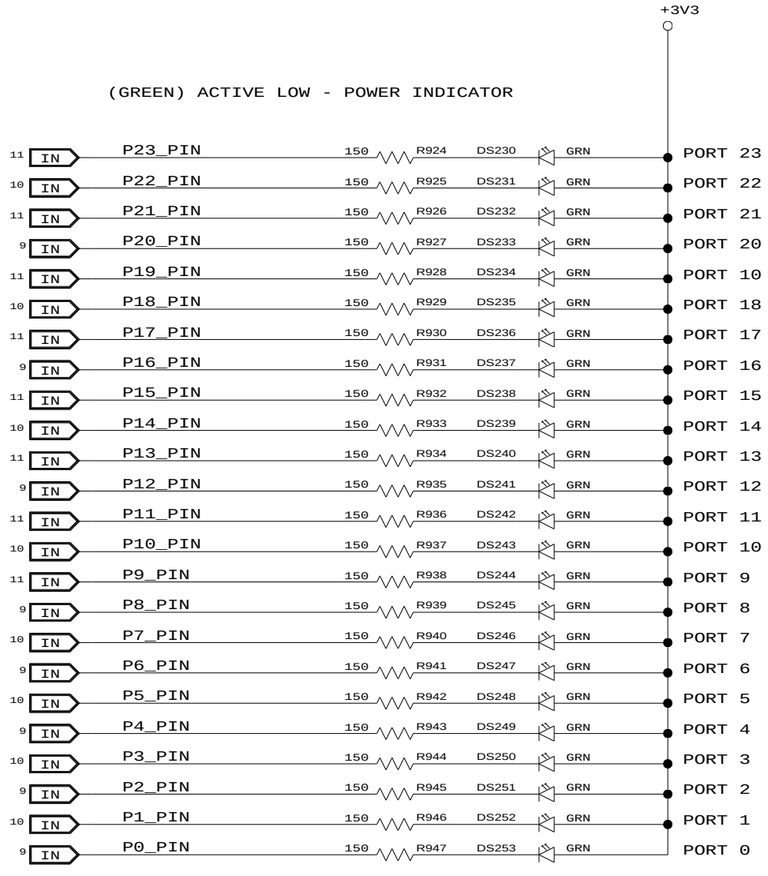
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(ORANGE) ACTIVE LOW - ATTENTION OUTPUT



(GREEN) ACTIVE LOW - POWER INDICATOR



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LED - PORT STATUS (3 OF 7)

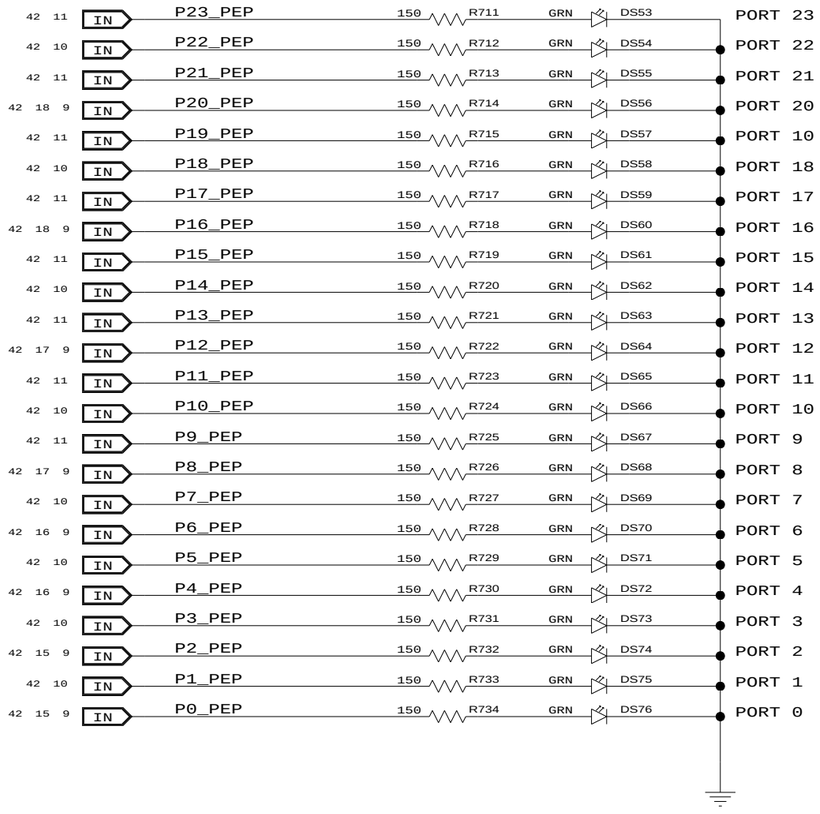
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B	SCH-PESEB-001	18-691-001	2.0

AUTHOR	CHECKED BY
Tony Tran	Derek Huang

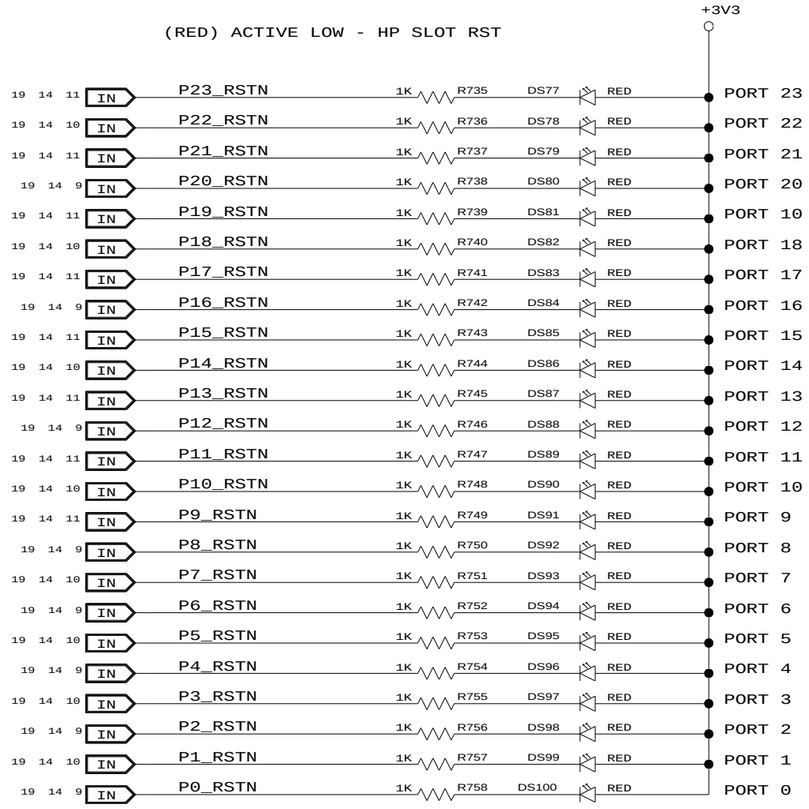
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(GREEN) ACTIVE HIGH - POWER ENABLE



(RED) ACTIVE LOW - HP SLOT RST



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TITLE EB-LOGAN-23

LED - PORT STATUS (4 OF 7)

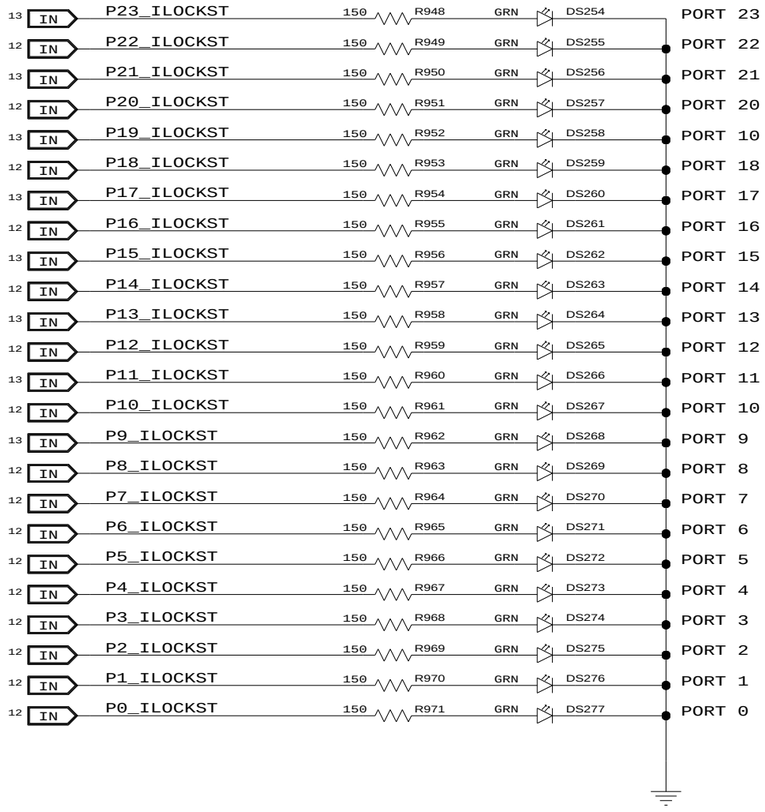
SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-PESEB-001	18-691-001	2.0

AUTHOR	CHECKED BY
Tony Tran	Derek Huang

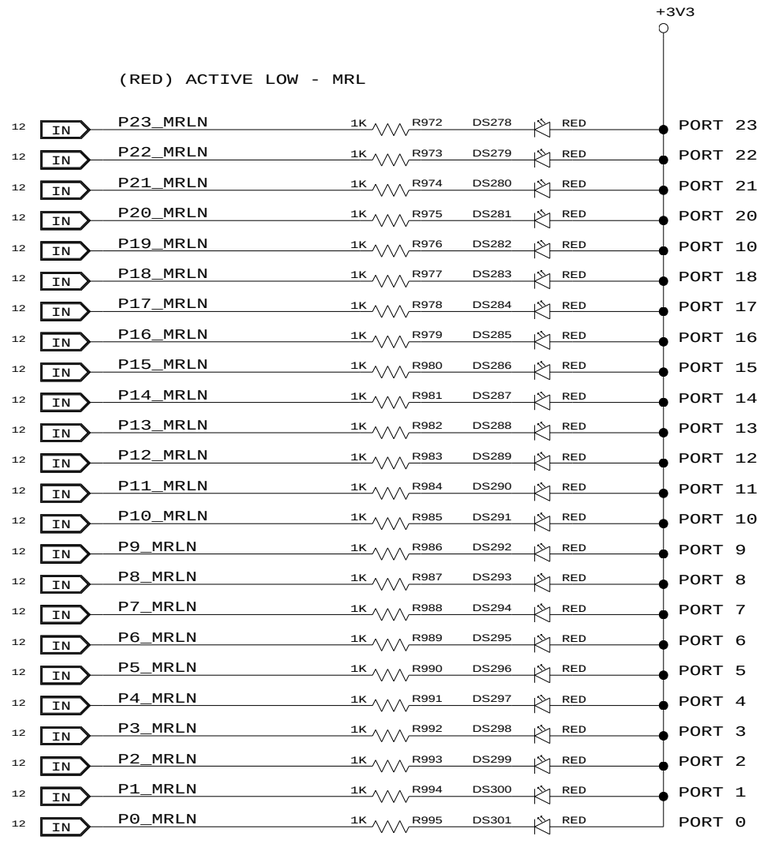
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(GREEN) ACTIVE HIGH - INTERLOCK INPUT



(RED) ACTIVE LOW - MRL



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TITLE EB-LOGAN-23

LED - PORT STATUS (5 OF 7)

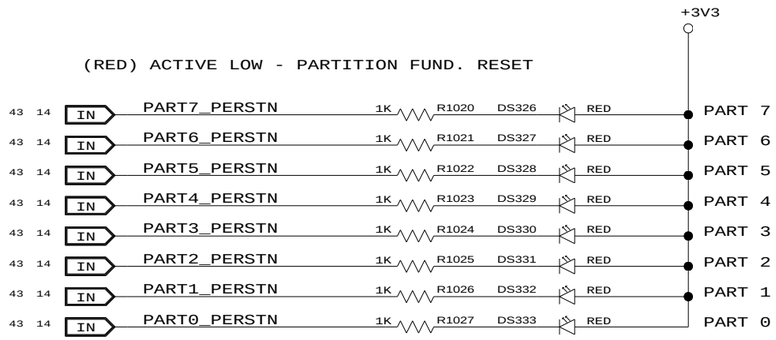
SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-PESEB-001	18-691-001	2.0

AUTHOR	CHECKED BY
Tony Tran	Derek Huang

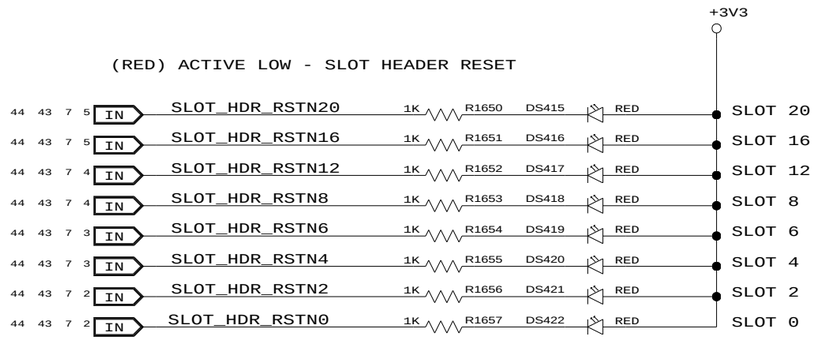
Thu Jul 01 15:01:03 2010 SHEET 38 OF 52

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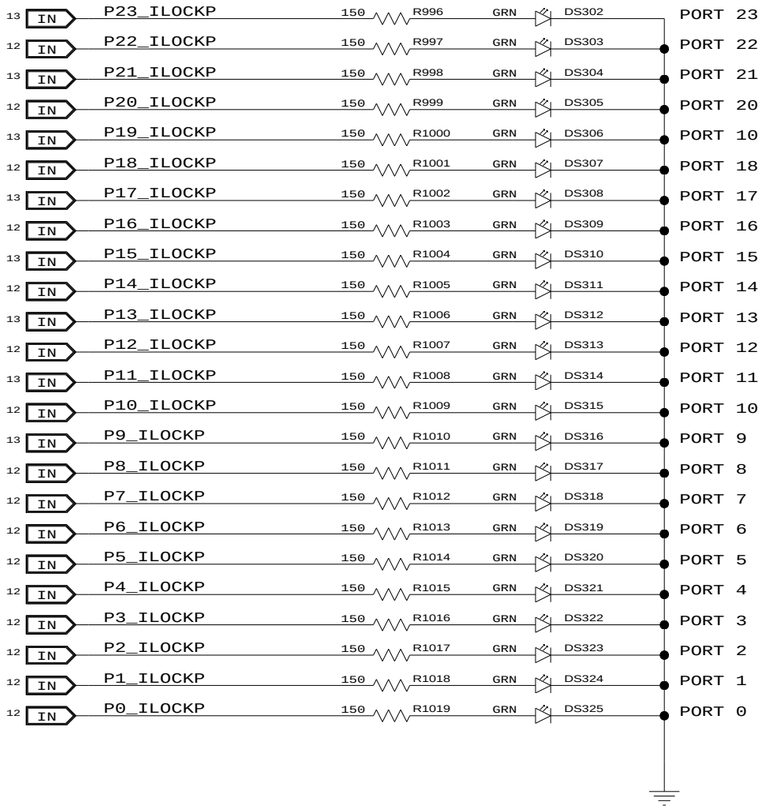
(RED) ACTIVE LOW - PARTITION FUND. RESET



(RED) ACTIVE LOW - SLOT HEADER RESET



(GREEN) ACTIVE HIGH - INTERLOCK OUTPUT



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TITLE EB-LOGAN-23

LED - PORT STATUS (6 OF 7)

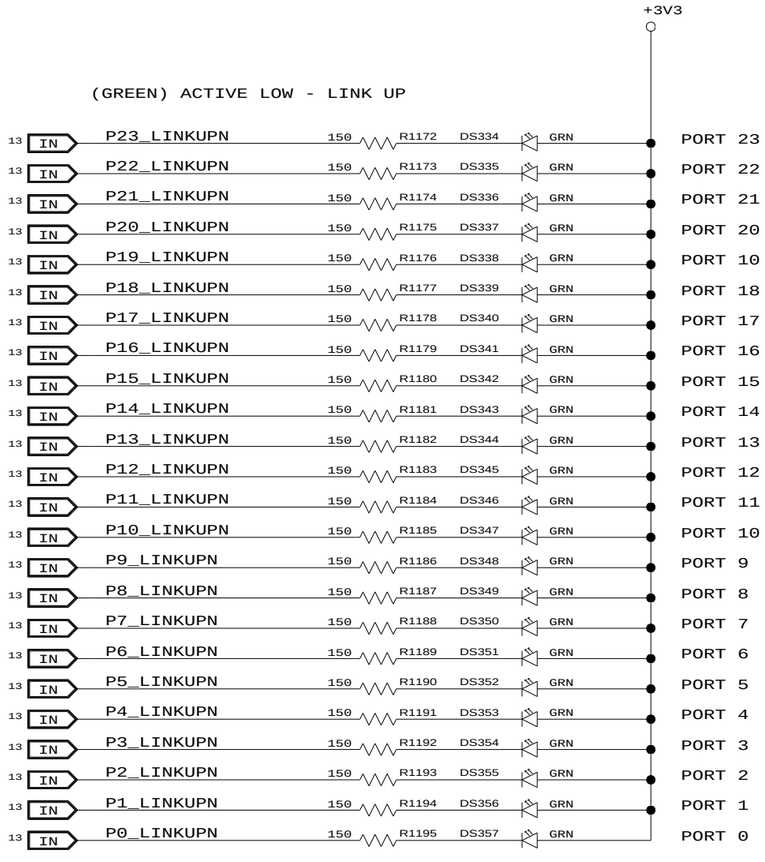
SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-PESEB-001	18-691-001	2.0

AUTHOR	CHECKED BY
Tony Tran	Derek Huang

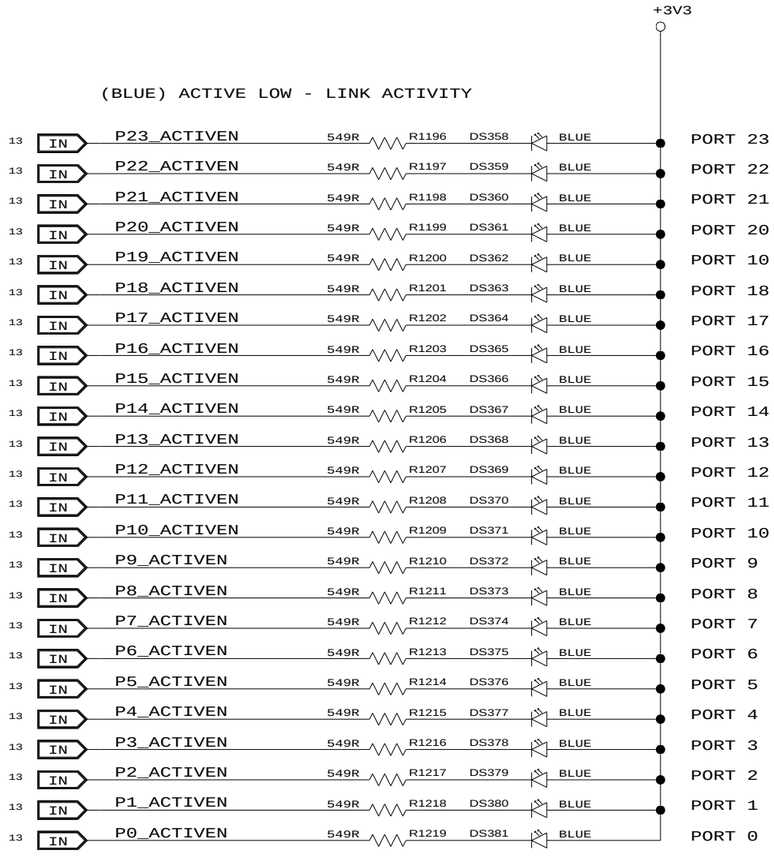
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(GREEN) ACTIVE LOW - LINK UP



(BLUE) ACTIVE LOW - LINK ACTIVITY



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LED - PORT STATUS (7 OF 7)

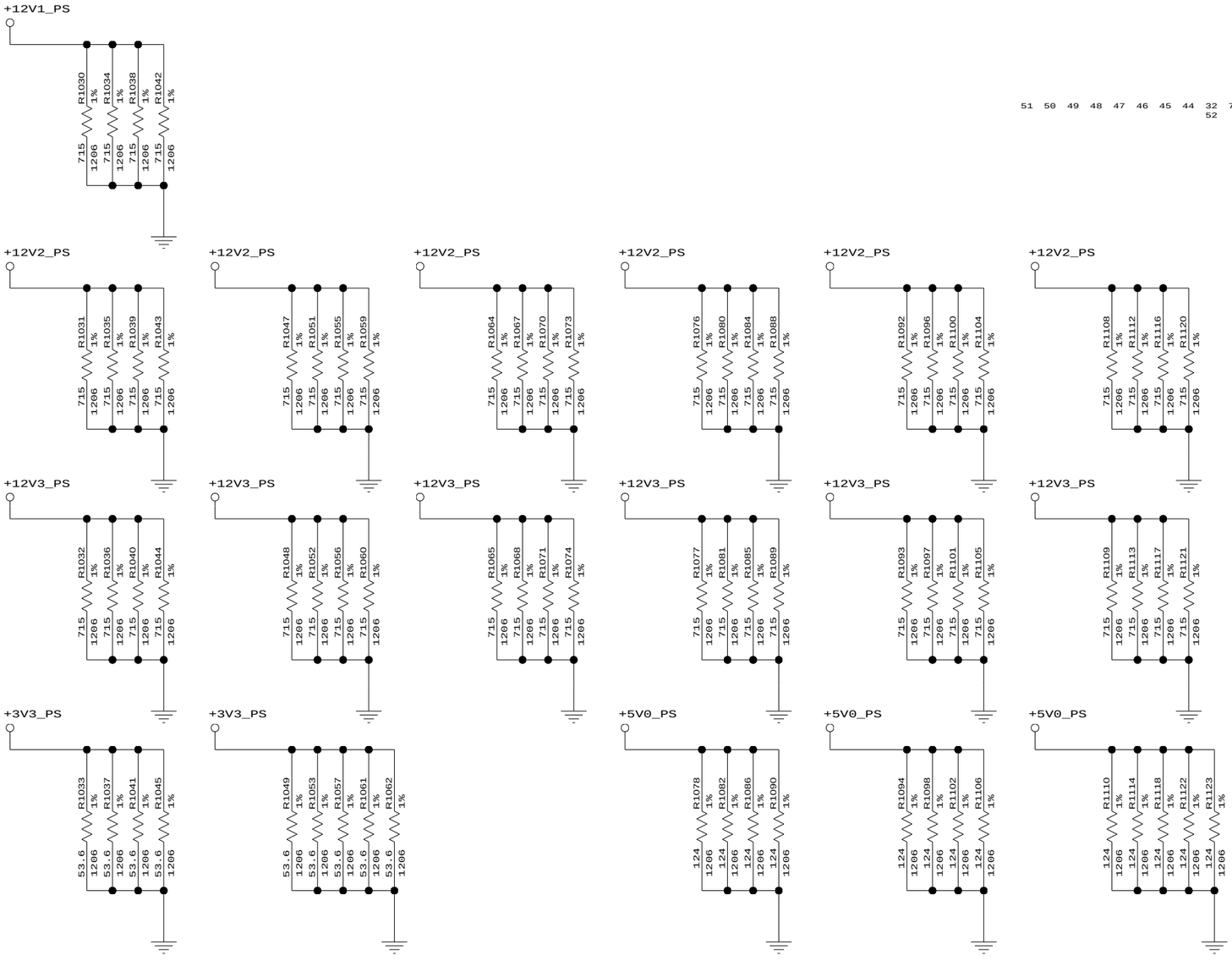
SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-PESEB-001	18-691-001	2.0

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Tony Tran	Derek Huang

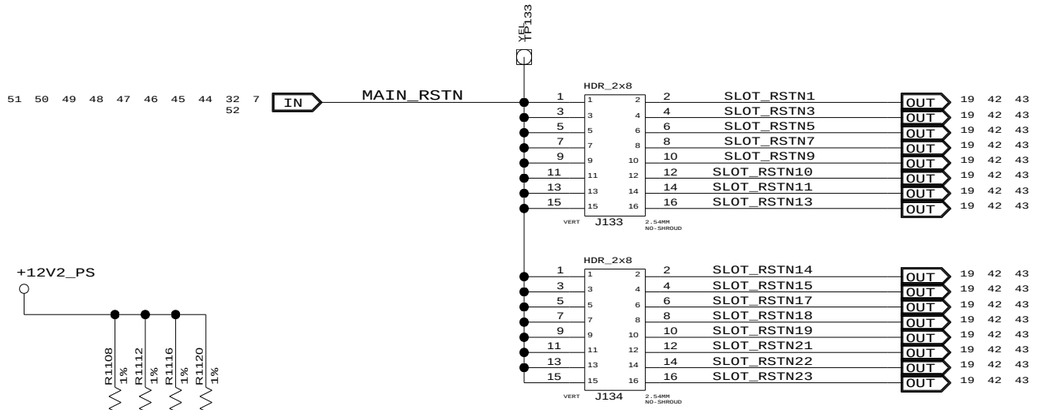
Thu Jul 01 15:01:04 2010 SHEET 40 OF 52

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MINIMUM POWER SUPPLY LOADS



NOTE: DNP JUMPERS WHEN IOEXPANDER IS ENABLED



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MIN LOAD RESISTORS

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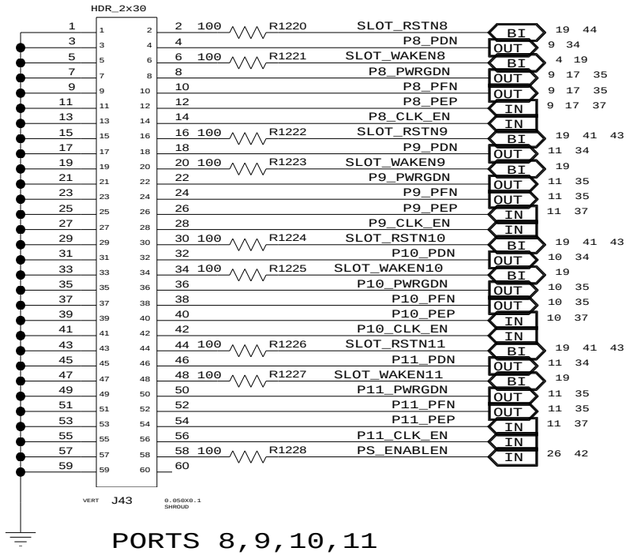
AUTHOR	CHECKED BY
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Thu Jul 01 15:01:04 2010 SHEET 41 OF 52

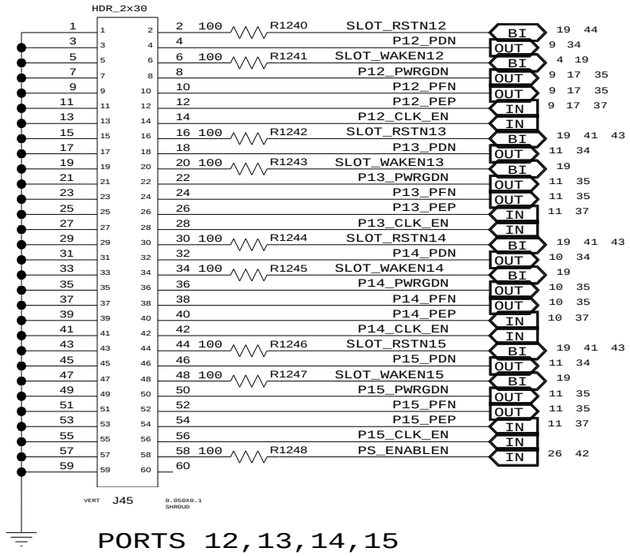
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SLOT_RESETN
CARD_PRESENTN
WAKEN
POWERGOOD
PWR_FLTN
PWR_ENABLE
CLOCK_ENABLEN

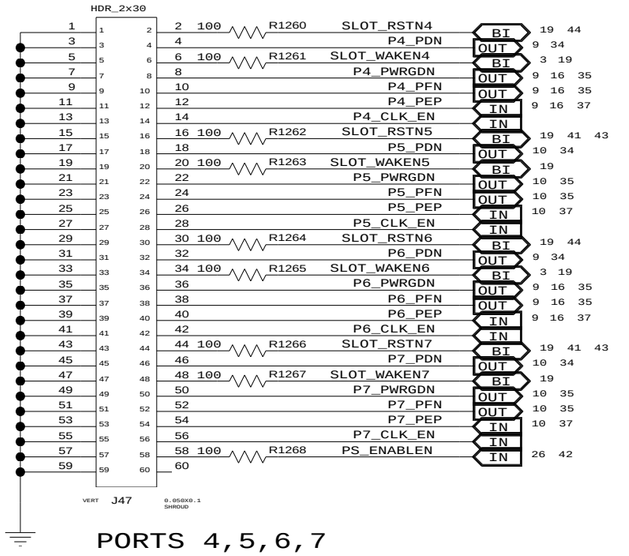
PS_ENABLEN
CABLE SENSE



PORTS 8,9,10,11



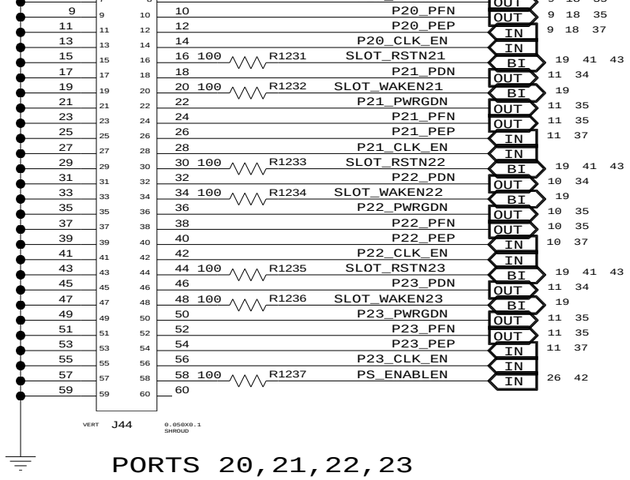
PORTS 12,13,14,15



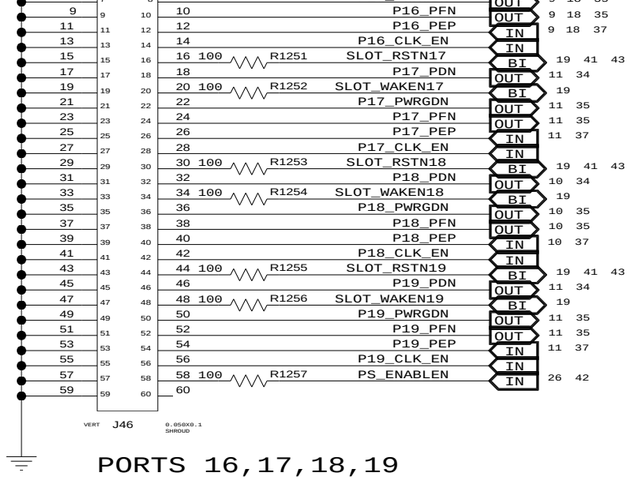
PORTS 4,5,6,7

SLOT_RESETN
CARD_PRESENTN
WAKEN
POWERGOOD
PWR_FLTN
PWR_ENABLE
CLOCK_ENABLEN

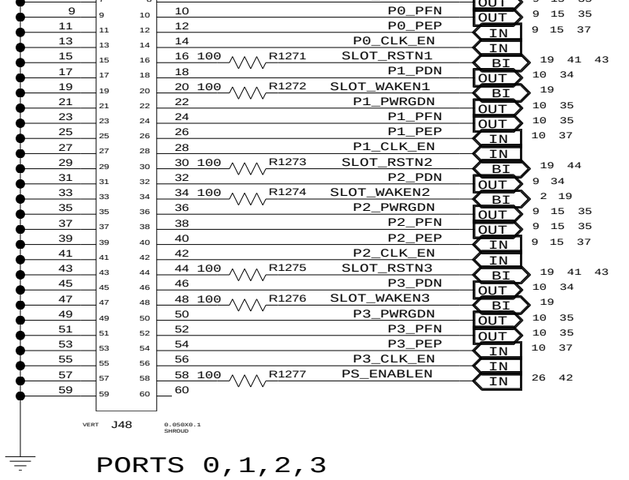
PS_ENABLEN
CABLE SENSE



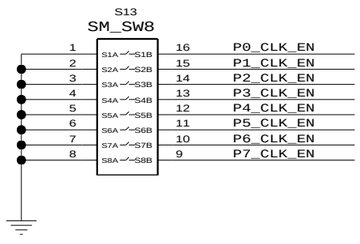
PORTS 20,21,22,23

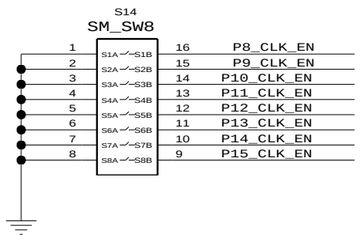


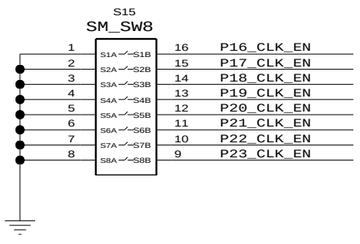
PORTS 16,17,18,19



PORTS 0,1,2,3







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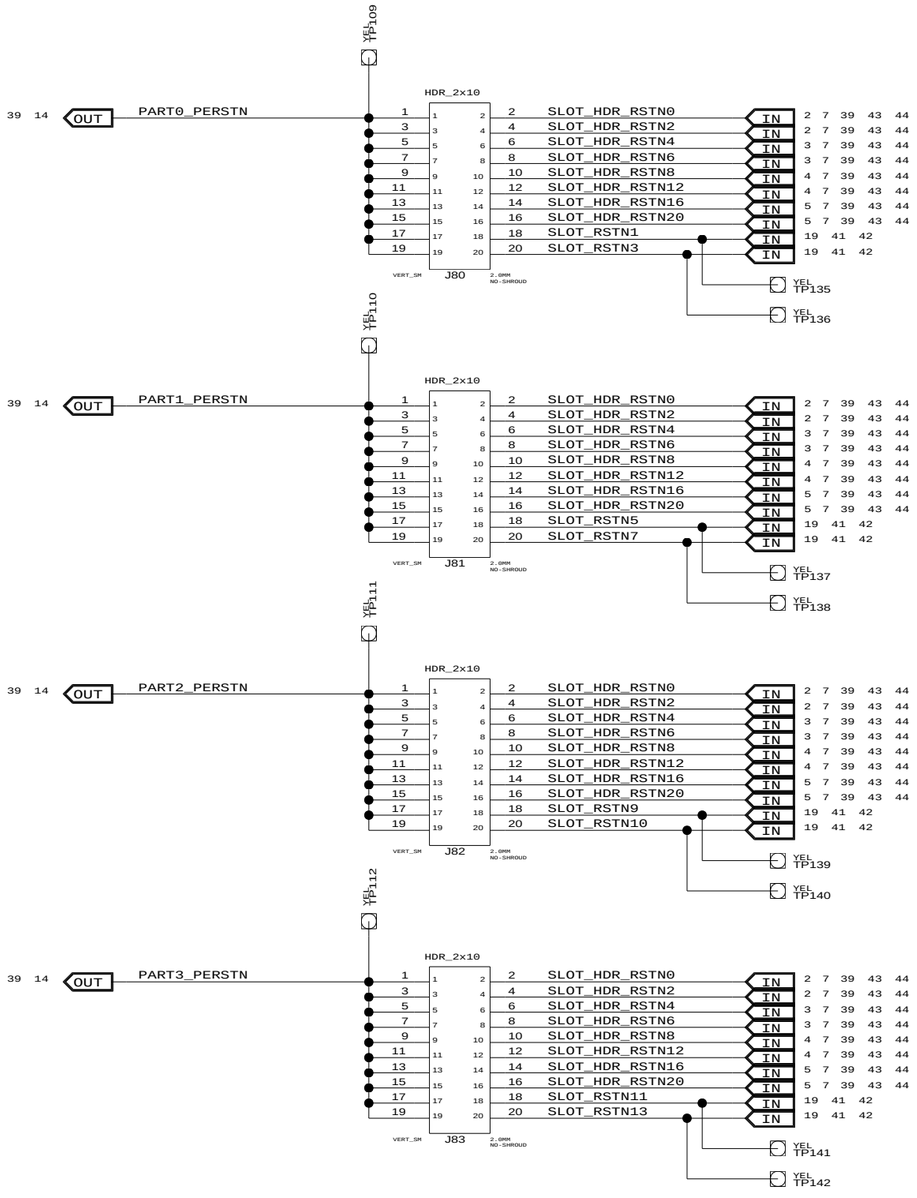
SIDEBAND CONNECTORS

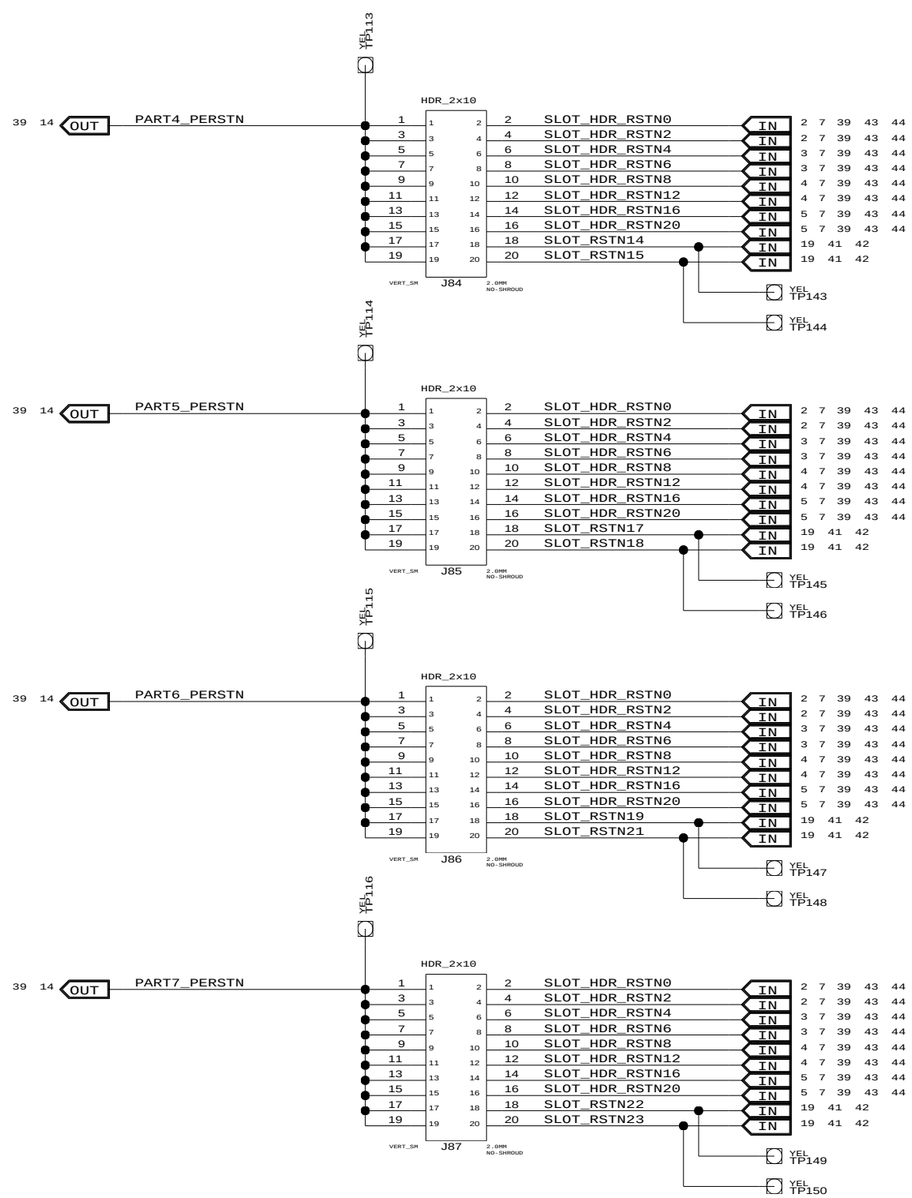
SIZE	DRAWING NO.	FAB P/N	REV.
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CHECKED BY: Derek Huang

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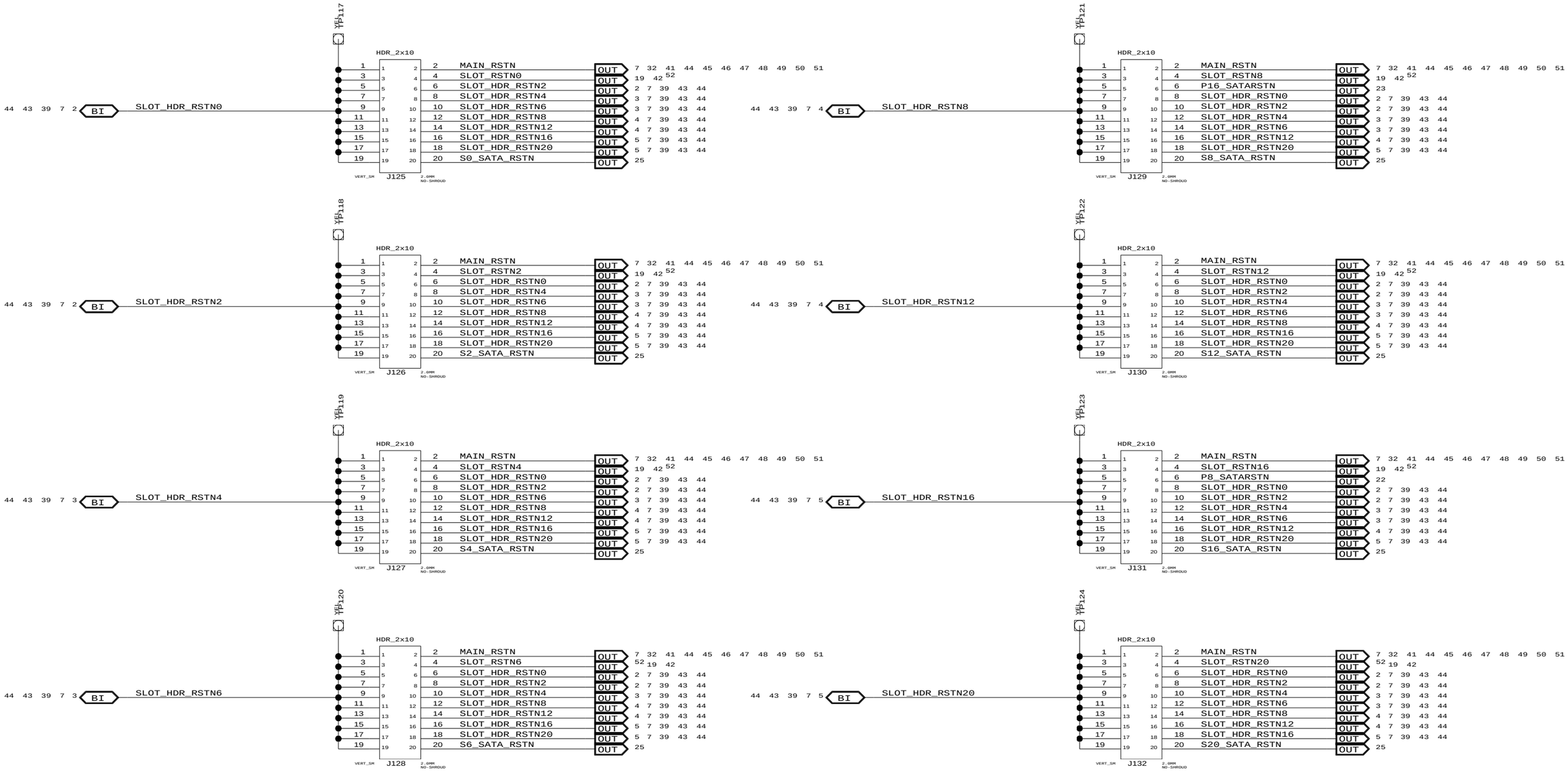
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PARTITION RESET SELECT HEADERS

SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-PESEB-001	18-691-001	2.0

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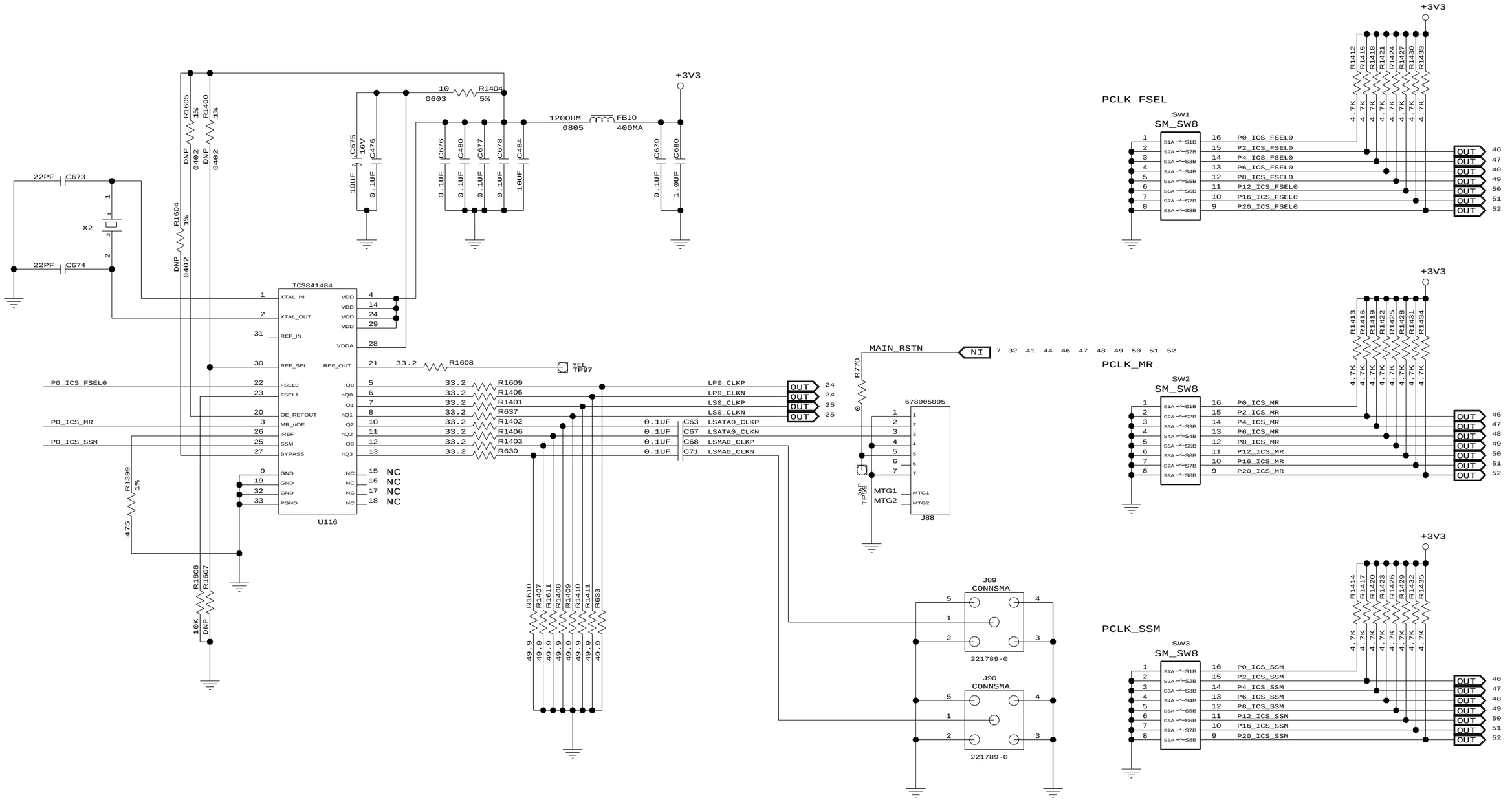
SLOT RESET SELECT HEADERS

SIZE	DRAWING NO.	FAB P/N	REV.
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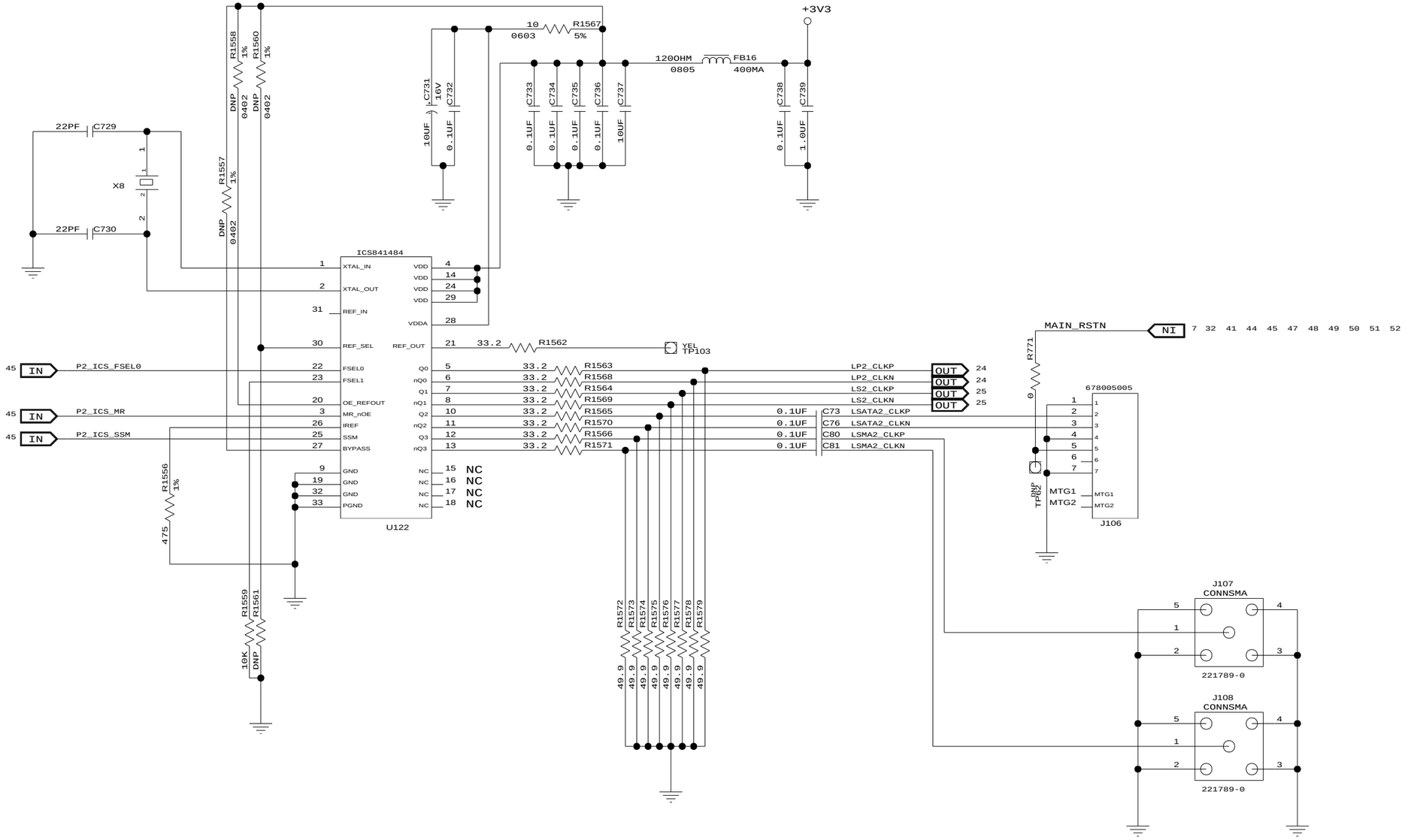
PORT 0 CLOCK GENERATOR

SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-PESEB-001	18-691-001	2.0

AUTHOR	CHECKED BY
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Thu Jul 01 15:01:05 2010 SHEET 45 OF 52

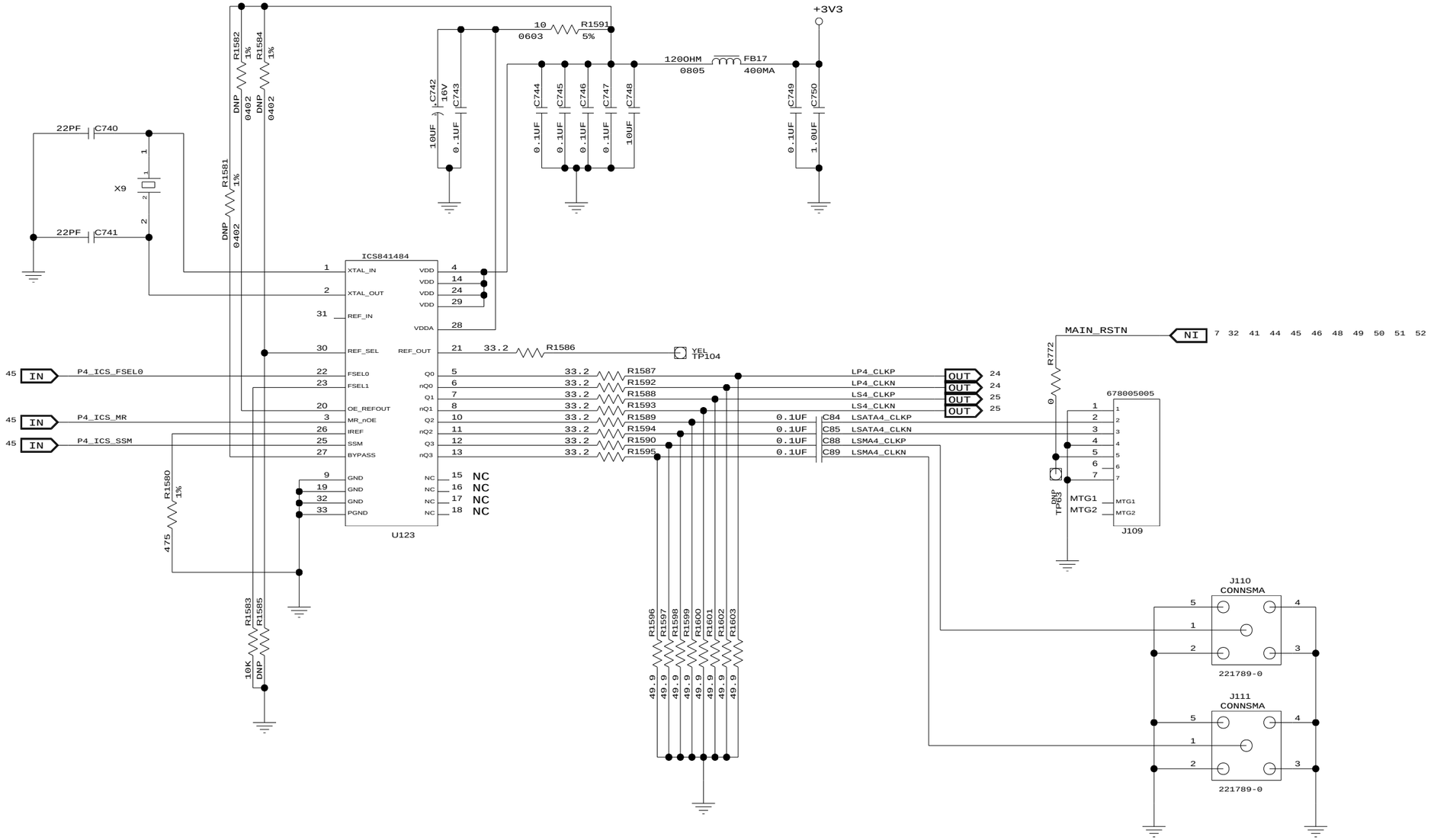
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TITLE	EB-LOGAN-23
	PORT 2 CLOCK GENERATOR
SIZE	B
DRAWING NO.	SCH-PESEB-001
FAB P/N	18-691-001
REV.	2.0
AUTHOR	Tony Tran
CHECKED BY	Derek Huang
	Thu Jul 01 15:01:06 2010
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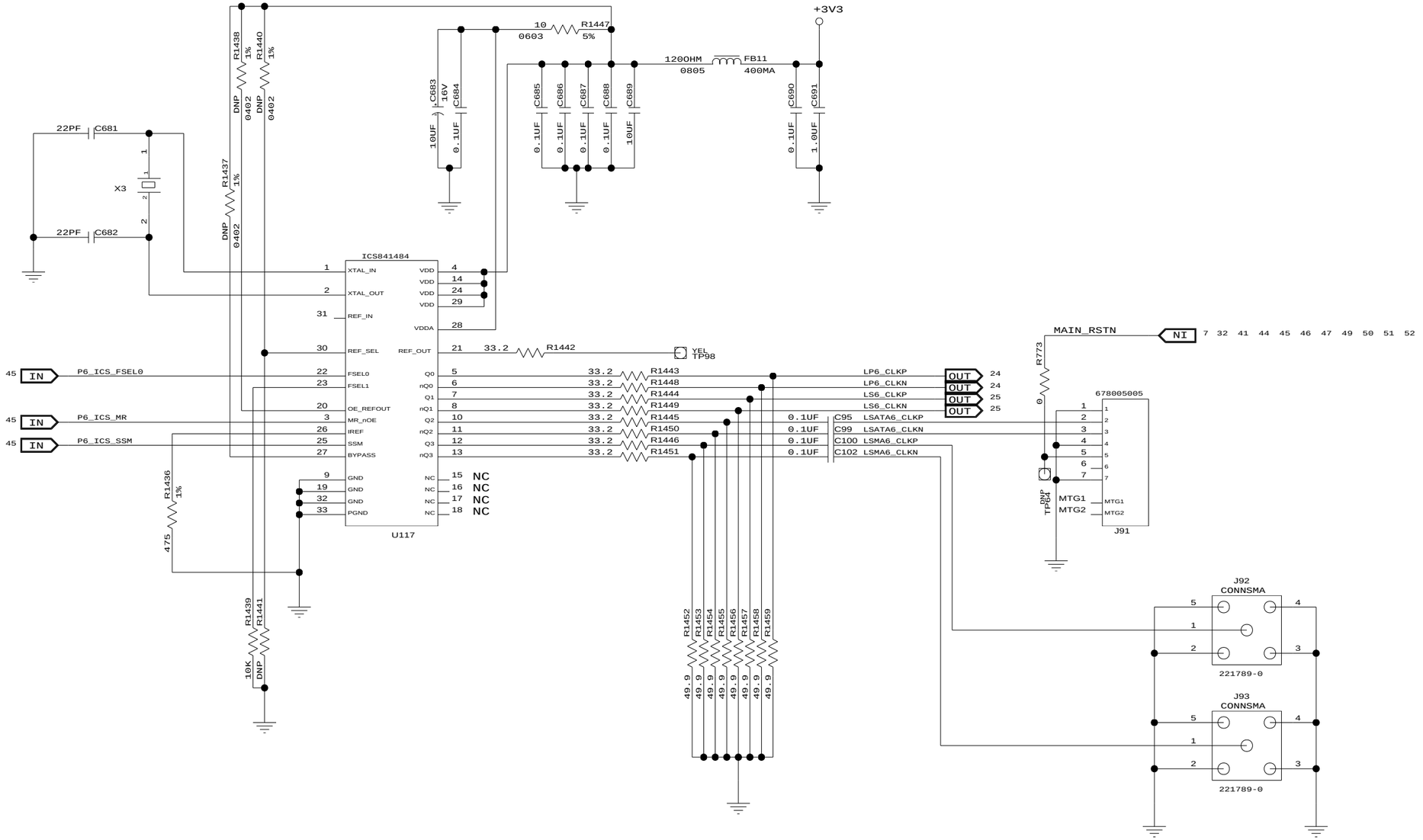
PORT 4 CLOCK GENERATOR

SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-PESEB-001	18-691-001	2.0

AUTHOR	CHECKED BY
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Thu Jul 01 15:01:06 2010 SHEET 47 OF 52

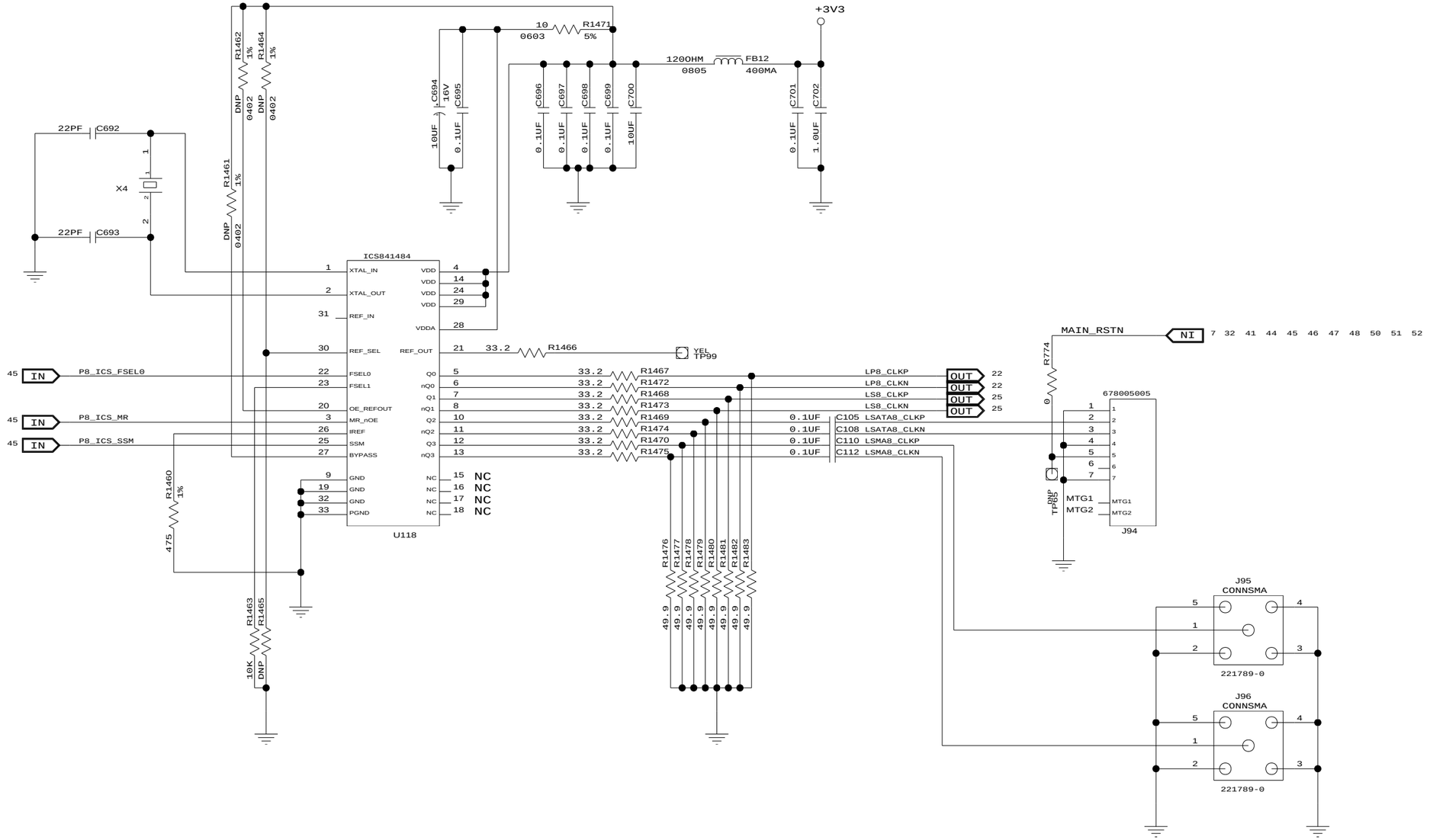
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TITLE	EB-LOGAN-23
	PORT 6 CLOCK GENERATOR
SIZE	B
DRAWING NO.	SCH-PESEB-001
FAB P/N	18-691-001
REV.	2.0
AUTHOR	Tony Tran
CHECKED BY	Derek Huang
	Thu Jul 01 15:01:06 2010
	SHEET 48 OF 52

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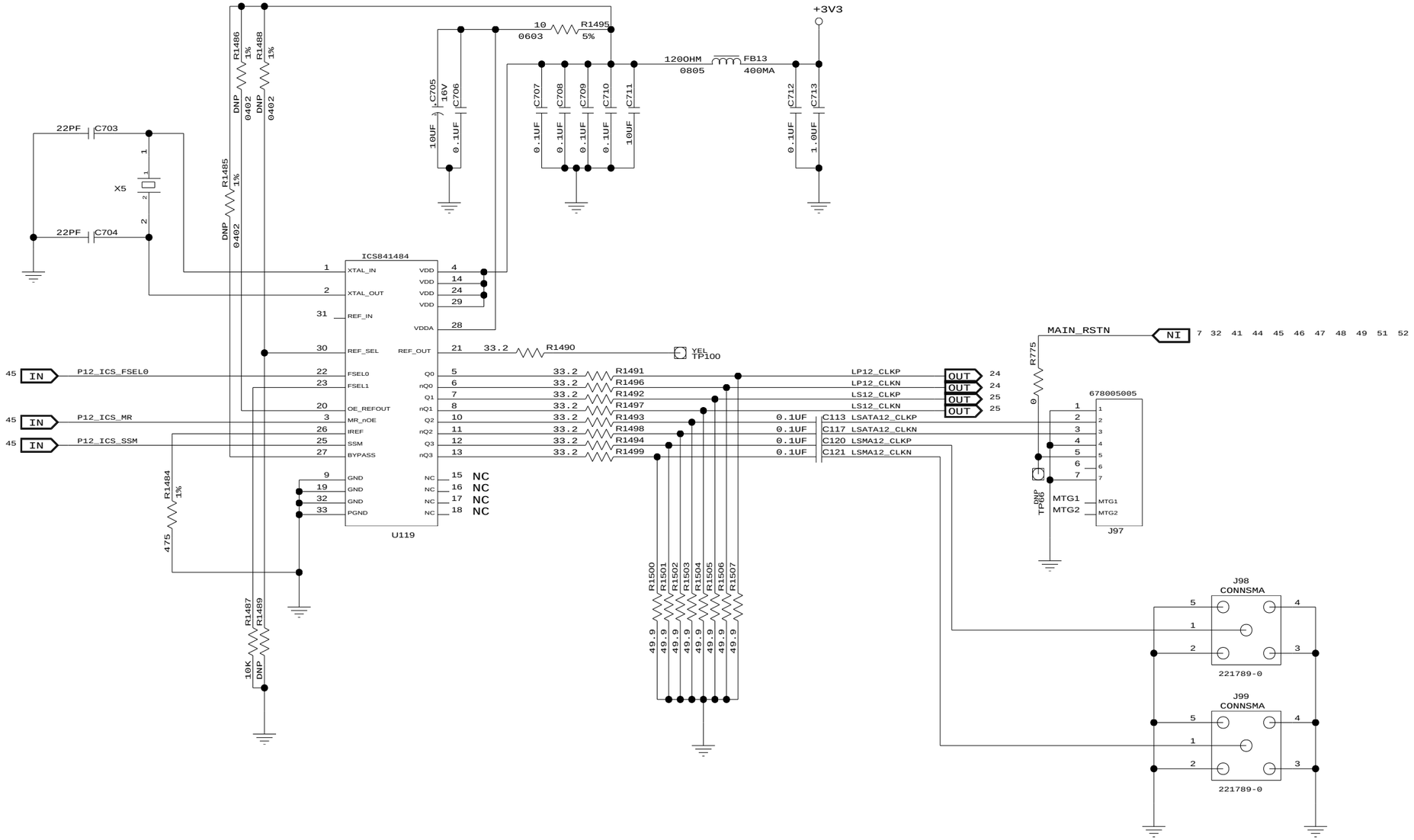
PORT 8 CLOCK GENERATOR

SIZE	DRAWING NO.	FAB P/N	REV.
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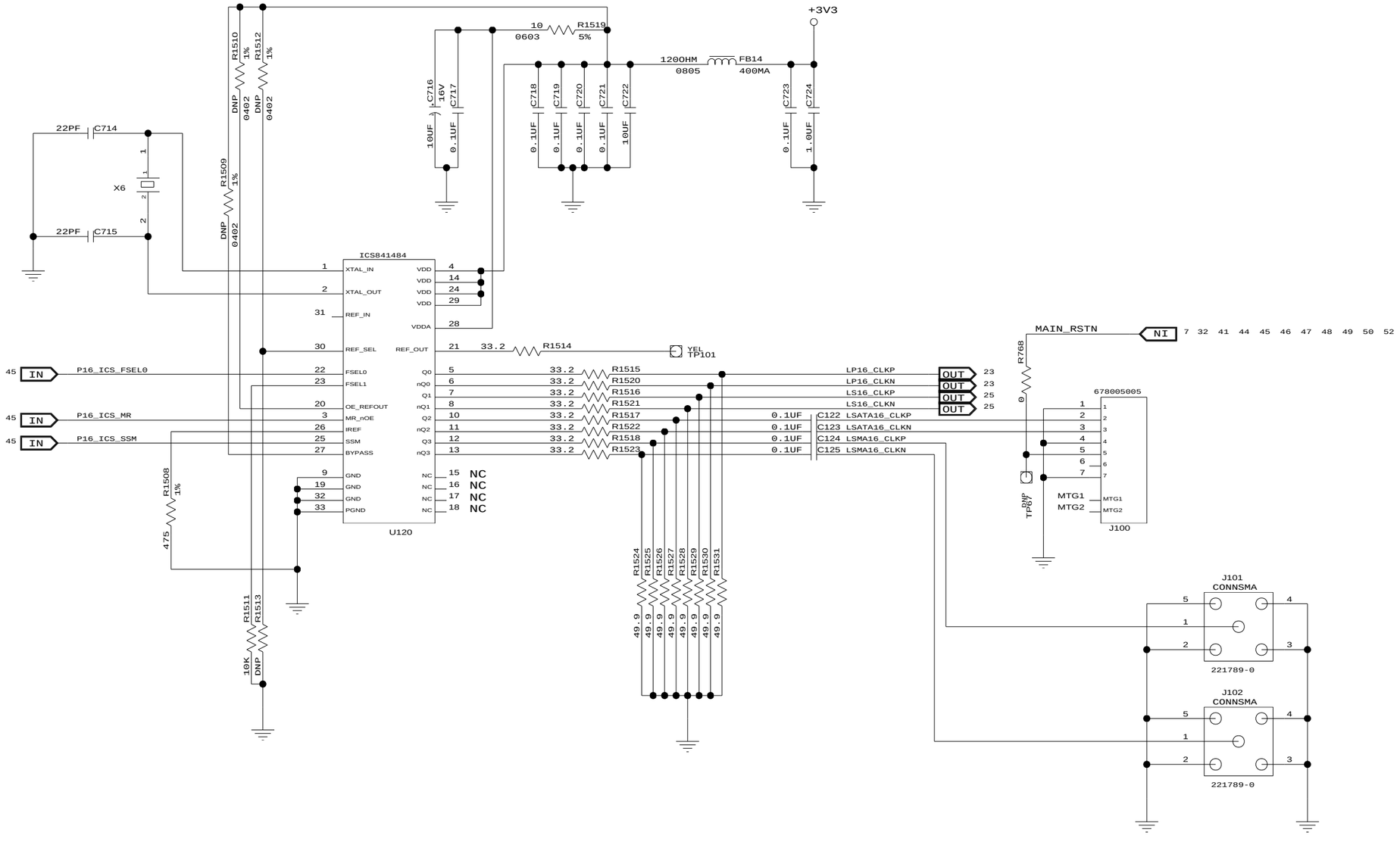
PORT 12 CLOCK GENERATOR

SIZE	DRAWING NO.	FAB P/N	REV.
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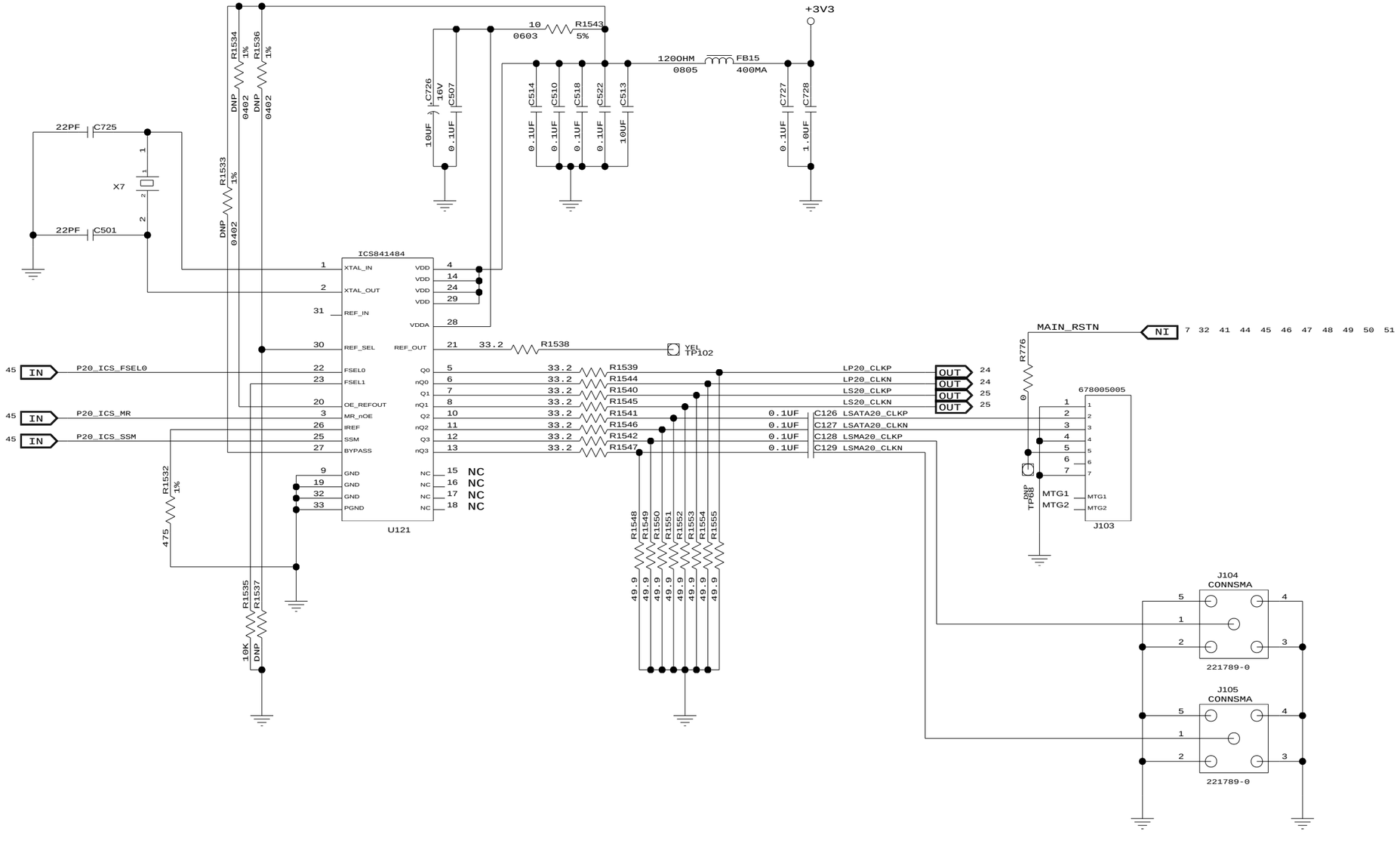
PORT 16 CLOCK GENERATOR

SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-PESEB-001	18-691-001	2.0

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PORT 20 CLOCK GENERATOR

SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-PESEB-001	18-691-001	2.0

AUTHOR	CHECKED BY
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Thu Jul 01 15:01:07 2010 SHEET 52 OF 52

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