Device Overview

The 89HPES48H12G2 is a member of the IDT PRECISE™ family of PCI Express® switching solutions. The PES48H12G2 is a 48-lane, 12-port system interconnect switch optimized for PCI Express Gen2 packet switching in high-performance applications, supporting multiple simultaneous peer-to-peer traffic flows. Target applications include servers, storage, communications, embedded systems, and multi-host or intelligent I/O based systems with inter-domain communication.

Features

- **High Performance Non-Blocking Switch Architecture**
  - 48-lane 12-port PCIe switch
    - *Six x8 ports switch ports each of which can bifurcate to two x4 ports (total of twelve x4 ports)*
  - Integrated SerDes supports 5.0 GT/s Gen2 and 2.5 GT/s Gen1 operation
  - Delivers up to *48 GBps (384 Gbps)* of switching capacity
  - Supports 128 Bytes to 2 KB maximum payload size
  - Low latency cut-through architecture
  - Supports one virtual channel and eight traffic classes
- **Standards and Compatibility**
  - PCI Express Base Specification 2.0 compliant
  - Implements the following optional PCI Express features
    - *Advanced Error Reporting (AER) on all ports*
    - *End-to-End CRC (ECRC)*
    - *Access Control Services (ACS)*
    - *Power Budgeting Enhanced Capability*
    - *Device Serial Number Enhanced Capability*
    - *Sub-System ID and Sub-System Vendor ID Capability*
    - *Internal Error Reporting ECN*
    - *Multicast ECN*
    - *VGA and ISA enable*
    - *L0s and L1 ASPM*
    - *ARI ECN*
- **Port Configurability**
  - x4 and x8 ports
    - *Ability to merge adjacent x4 ports to create a x8 port*
  - Automatic per port link width negotiation (x8 → x4 → x2 → x1)
  - Crosslink support
  - Automatic lane reversal
  - Autonomous and software managed link width and speed control
  - Per lane SerDes configuration
    - *De-emphasis*
    - *Receive equalization*
    - *Drive strength*
- **Switch Partitioning**
  - IDT proprietary feature that creates logically independent switches in the device
  - Supports up to 12 fully independent switch partitions
  - Configurable downstream port device numbering
  - Supports dynamic reconfiguration of switch partitions
    - *Dynamic port reconfiguration — downstream, upstream*
    - *Dynamic migration of ports between partitions*
    - *Movable upstream port within and between switch partitions*
- **Initialization / Configuration**
  - Supports Root (BIOS, OS, or driver), Serial EEPROM, or SMBus switch initialization
  - Common switch configurations are supported with pin strapping (no external components)
  - Supports in-system Serial EEPROM initialization/programming
- **Quality of Service (QoS)**
  - Port arbitration
    - *Round robin*
  - Request metering
    - *IDT proprietary feature that balances bandwidth among switch ports for maximum system throughput*
  - High performance switch core architecture
    - *Combined Input Output Queued (CIOQ) switch architecture with large buffers*
- **Multicast**
  - Compliant to the PCI-SIG multicast ECN
  - Supports arbitrary multicasting of Posted transactions
  - Supports 64 multicast groups
  - Multicast overlay mechanism support
  - ECRC regeneration support
- **Clocking**
  - Supports 100 MHz and 125 MHz reference clock frequencies
  - Flexible clocking modes
    - *Common clock*
    - *Non-common clock*
    - *Local port clock with SSC and port reference clock input*
- **Hot-Plug and Hot Swap**
  - Hot-plug controller on all ports
    - *Hot-plug supported on all downstream switch ports*

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- All ports support hot-plug using low-cost external I^2C I/O expanders
- Configurable presence detect supports card and cable applications
- GPE output pin for hot-plug event notification
  - *Enables SCI/SMI generation for legacy operating system support*
- Hot swap capable I/O

◆ **Power Management**

- Supports D0, D3hot and D3 power management states
- Active State Power Management (ASPM)
  - *Supports L0, L0s, L1, L2/L3 Ready and L3 link states*
  - *Configurable L0s and L1 entry timers allow performance/ power-savings tuning*
- Supports PCI Express Power Budgeting Capability
- SerDes power savings
  - *Supports low swing / half-swing SerDes operation*
  - *SerDes optionally turned-off in D3hot*
  - *SerDes associated with unused ports are turned-off*
  - *SerDes associated with unused lanes are placed in a low power state*

◆ **9 General Purpose I/O**

◆ **Reliability, Availability and Serviceability (RAS)**

- ECRC support
- AER on all ports
- SECDED ECC protection on all internal RAMs
- End-to-end data path parity protection
- Checksum Serial EEPROM content protected
- Autonomous link reliability (preserves system operation in the presence of faulty links)
- Ability to generate an interrupt (INTx or MSI) on link up/down transitions

◆ **Test and Debug**

- On-chip link activity and status outputs available for Port 0 (upstream port)
- Per port link activity and status outputs available using external I^2C I/O expander for all other ports
- SerDes test modes
- Supports IEEE 1149.6 AC JTAG and IEEE 1149.1 JTAG

◆ **Power Supplies**

- Requires only two power supply voltages (1.0 V and 2.5 V) Note that a 3.3V is preferred for V_{DD}I/O
- No power sequencing requirements

◆ **Packaged in a 27mm x 27mm 676-ball Flip Chip BGA with 1mm ball spacing**

Product Description

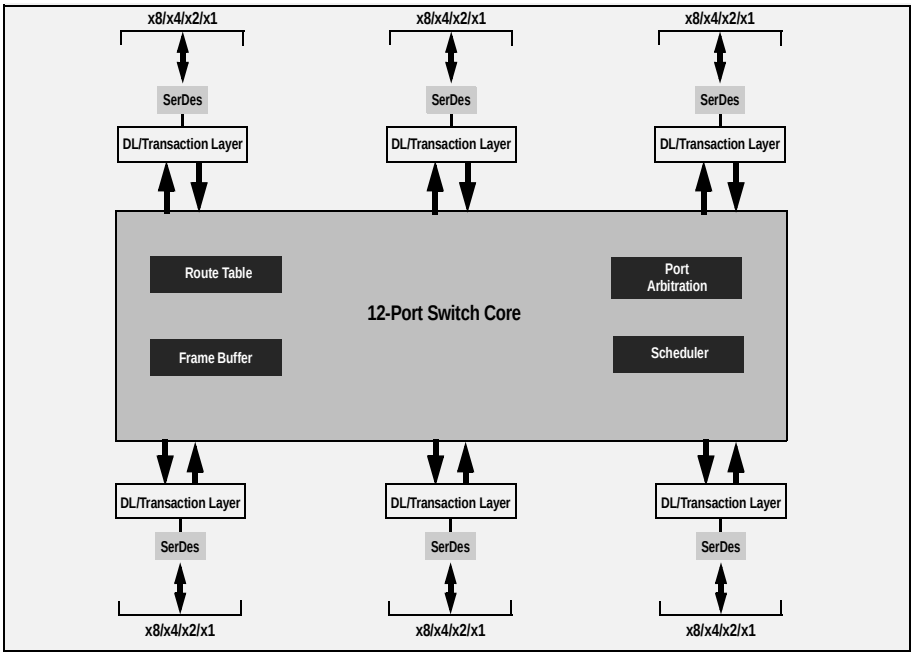
Utilizing standard PCI Express Gen2 interconnect, the PES48H12G2 provides the most efficient system interconnect switching solution for applications requiring high throughput, low latency, and simple board layout with a minimum number of board layers. It provides 48 GBps (384 Gbps) of aggregated, full-duplex switching capacity through 48 integrated serial lanes, using proven and robust IDT technology. Each lane is capable of 5 GT/s of bandwidth in both directions and is fully compliant with PCI Express Base specification 2.0.

The PES48H12G2 is based on a flexible and efficient layered architecture. The PCI Express layer consists of SerDes, Physical, Data Link and Transaction layers in compliance with PCI Express Base specification Revision 2.0. The PES48H12G2 can operate either as a store and forward or cut-through switch. It supports eight Traffic Classes (TCs) and one Virtual Channel (VC) with sophisticated resource management to enable efficient switching and I/O connectivity for servers, storage, and embedded processors with limited connectivity.

The PES48H12G2 is a *partitionable* PCIe switch. This means that in addition to operating as a standard PCI express switch, the PES48H12G2 ports may be partitioned into groups that logically operate as completely independent PCIe switches. Figure 2 illustrates a three partition PES48H12G2 configuration.

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Block Diagram



48 PCI Express Lanes
Up to 6 x8 ports or 12 x4 Ports

Figure 1 Internal Block Diagram

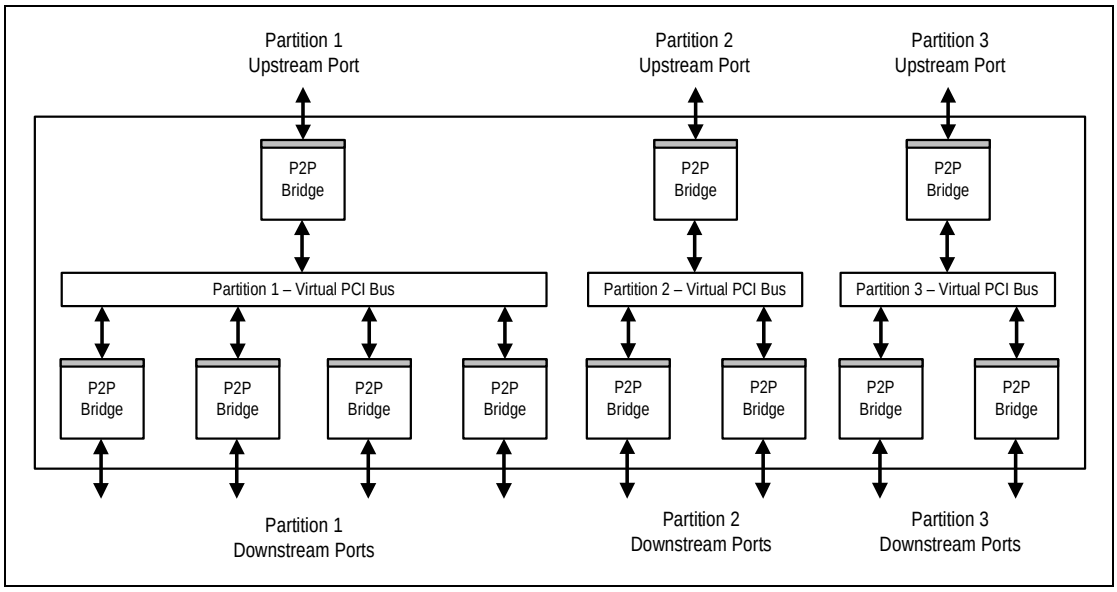


Figure 2 Example of Usage of Switch Partitioning

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SMBus Interface

The PES48H12G2 contains an SMBus master interface. This master interface allows the default configuration register values of the PES48H12G2 to be overridden following a reset with values programmed in an external serial EEPROM. The master interface is also used by an external Hot-Plug I/O expander. Two pins make up the SMBus master interface: an SMBus clock pin and an SMBus data pin. Four pins make up the SMBus slave interface: an SMBus clock pin and an SMBus data pin plus two address pins, SSMBADDR[2,1].

As shown in Figure 3, the master and slave SMBuses may only be used in a split configuration.

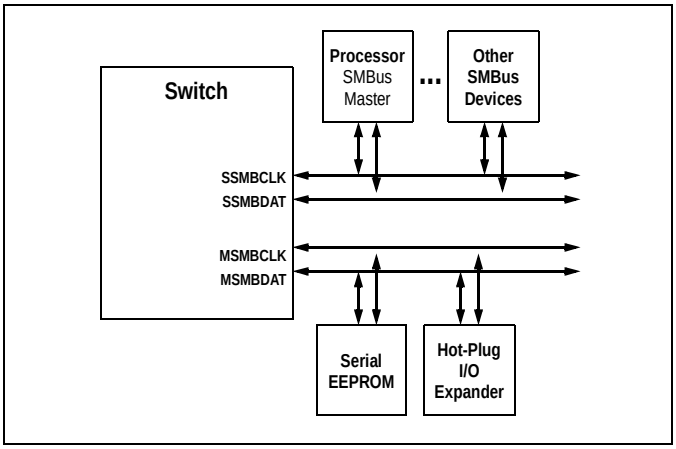


Figure 3 Split SMBus Interface Configuration

The switch's SMBus master interface does not support SMBus arbitration. As a result, the switch's SMBus master must be the only master in the SMBus lines that connect to the serial EEPROM and I/O expander slaves. In the split configuration, the master and slave SMBuses operate as two independent buses; thus, multi-master arbitration is not required.

Hot-Plug Interface

The PES48H12G2 supports PCI Express Hot-Plug on each downstream port. To reduce the number of pins required on the device, the PES48H12G2 utilizes an external I/O expander, such as that used on PC motherboards, connected to the SMBus master interface. Following reset and configuration, whenever the state of a Hot-Plug output needs to be modified, the PES48H12G2 generates an SMBus transaction to the I/O expander with the new value of all of the outputs. Whenever a Hot-Plug input changes, the I/O expander generates an interrupt which is received on the IOEXPINTN input pin (alternate function of GPIO) of the PES48H12G2. In response to an I/O expander interrupt, the PES48H12G2 generates an SMBus transaction to read the state of all of the Hot-Plug inputs from the I/O expander.

General Purpose Input/Output

The PES48H12G2 provides 9 General Purpose Input/Output (GPIO) pins that may be used by the system designer as bit I/O ports. Each GPIO pin may be configured independently as an input or output through software control. Some GPIO pins are shared with other on-chip functions. These alternate functions may be enabled via software, SMBus slave interface, or serial configuration EEPROM.

Pin Description

The following tables list the functions of the pins provided on the PES48H12G2. Some of the functions listed may be multiplexed onto the same pin. The active polarity of a signal is defined using a suffix. Signals ending with an "N" are defined as being active, or asserted, when at a logic zero (low) level. All other signals (including clocks, buses, and select lines) will be interpreted as being active, or asserted, when at a logic one (high) level.

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Signal	Type	Name/Description
PE00RP[3:0] PE00RN[3:0]	I	**PCI Express Port 0 Serial Data Receive.** Differential PCI Express receive pairs for port 0.
PE00TP[3:0] PE00TN[3:0]	O	**PCI Express Port 0 Serial Data Transmit.** Differential PCI Express transmit pairs for port 0.
PE01RP[3:0] PE01RN[3:0]	I	**PCI Express Port 1 Serial Data Receive.** Differential PCI Express receive pairs for port 1. When port 0 is merged with port 1, these signals become port 0 receive pairs for lanes 4 through 7.
PE01TP[3:0] PE01TN[3:0]	O	**PCI Express Port 1 Serial Data Transmit.** Differential PCI Express transmit pairs for port 1. When port 0 is merged with port 1, these signals become port 0 transmit pairs for lanes 4 through 7.
PE02RP[3:0] PE02RN[3:0]	I	**PCI Express Port 2 Serial Data Receive.** Differential PCI Express receive pairs for port 2.
PE02TP[3:0] PE02TN[3:0]	O	**PCI Express Port 2 Serial Data Transmit.** Differential PCI Express transmit pairs for port 2.
PE03RP[3:0] PE03RN[3:0]	I	**PCI Express Port 3 Serial Data Receive.** Differential PCI Express receive pairs for port 3. When port 2 is merged with port 3, these signals become port 2 receive pairs for lanes 4 through 7.
PE03TP[3:0] PE03TN[3:0]	O	**PCI Express Port 3 Serial Data Transmit.** Differential PCI Express transmit pairs for port 3. When port 2 is merged with port 3, these signals become port 2 transmit pairs for lanes 4 through 7.
PE04RP[3:0] PE04RN[3:0]	I	**PCI Express Port 4 Serial Data Receive.** Differential PCI Express receive pairs for port 4.
PE04TP[3:0] PE04TN[3:0]	O	**PCI Express Port 4 Serial Data Transmit.** Differential PCI Express transmit pairs for port 4.
PE05RP[3:0] PE05RN[3:0]	I	**PCI Express Port 5 Serial Data Receive.** Differential PCI Express receive pairs for port 5. When port 4 is merged with port 5, these signals become port 4 receive pairs for lanes 4 through 7.
PE05TP[3:0] PE05TN[3:0]	O	**PCI Express Port 5 Serial Data Transmit.** Differential PCI Express transmit pairs for port 5. When port 4 is merged with port 5, these signals become port 4 transmit pairs for lanes 4 through 7.
PE06RP[3:0] PE06RN[3:0]	I	**PCI Express Port 6 Serial Data Receive.** Differential PCI Express receive pairs for port 6.
PE06TP[3:0] PE06TN[3:0]	O	**PCI Express Port 6 Serial Data Transmit.** Differential PCI Express transmit pairs for port 6.
PE07RP[3:0] PE07RN[3:0]	I	**PCI Express Port 7 Serial Data Receive.** Differential PCI Express receive pairs for port 7. When port 6 is merged with port 7, these signals become port 6 receive pairs for lanes 4 through 7.
PE07TP[3:0] PE07TN[3:0]	O	**PCI Express Port 7 Serial Data Transmit.** Differential PCI Express transmit pairs for port 7. When port 6 is merged with port 7, these signals become port 6 transmit pairs for lanes 4 through 7.
PE08RP[3:0] PE08RN[3:0]	I	**PCI Express Port 8 Serial Data Receive.** Differential PCI Express receive pairs for port 8.
PE08TP[3:0] PE08TN[3:0]	O	**PCI Express Port 8 Serial Data Transmit.** Differential PCI Express transmit pairs for port 8.

Table 1 PCI Express Interface Pins (Part 1 of 2)

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Signal	Type	Name/Description
PE09RP[3:0] PE09RN[3:0]	I	**PCI Express Port 9 Serial Data Receive.** Differential PCI Express receive pairs for port 9. When port 8 is merged with port 9, these signals become port 8 receive pairs for lanes 4 through 7.
PE09TP[3:0] PE09TN[3:0]	O	**PCI Express Port 9 Serial Data Transmit.** Differential PCI Express transmit pairs for port 9. When port 8 is merged with port 9, these signals become port 8 transmit pairs for lanes 4 through 7.
PE12RP[3:0] PE12RN[3:0]	I	**PCI Express Port 12 Serial Data Receive.** Differential PCI Express receive pairs for port 12.
PE12TP[3:0] PE12TN[3:0]	O	**PCI Express Port 12 Serial Data Transmit.** Differential PCI Express transmit pairs for port 12.
PE13RP[3:0] PE13RN[3:0]	I	**PCI Express Port 13 Serial Data Receive.** Differential PCI Express receive pairs for port 13. When port 12 is merged with port 13, these signals become port 12 receive pairs for lanes 4 through 7.
PE13TP[3:0] PE13TN[3:0]	O	**PCI Express Port 13 Serial Data Transmit.** Differential PCI Express transmit pairs for port 13. When port 12 is merged with port 13, these signals become port 12 transmit pairs for lanes 4 through 7.

Table 1 PCI Express Interface Pins (Part 2 of 2)

Signal	Type	Name/Description
GCLKN[1:0] GCLKP[1:0]	I	**Global Reference Clock.** Differential reference clock input pair. This clock is used as the reference clock by on-chip PLLs to generate the clocks required for the system logic. The frequency of the differential reference clock is determined by the GCLKFSEL signal.
P[2,0]CLKN P[2,0]CLKP	I	**Port Reference Clock**. Differential reference clock pair associated with ports 0 and 2.[1]

Table 2 Reference Clock Pins

1. Unused port clock pins should be connected to Vss on the board.

Signal	Type	Name/Description
MSMBCLK	I/O	**Master SMBus Clock.** This bidirectional signal is used to synchronize transfers on the master SMBus.
MSMBDAT	I/O	**Master SMBus Data.** This bidirectional signal is used for data on the master SMBus.
SSMBADDR[2,1]	I	**Slave SMBus Address.** These pins determine the SMBus address to which the slave SMBus interface responds.
SSMBCLK	I/O	**Slave SMBus Clock.** This bidirectional signal is used to synchronize transfers on the slave SMBus.
SSMBDAT	I/O	**Slave SMBus Data.** This bidirectional signal is used for data on the slave SMBus.

Table 3 SMBus Interface Pins

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Signal	Type	Name/Description
GPIO[0]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: PART0PERSTN Alternate function pin type: Input/Output Alternate function: Assertion of this signal initiated a partition fundamental reset in the corresponding partition.
GPIO[1]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: PART1PERSTN Alternate function pin type: Input/Output Alternate function: Assertion of this signal initiated a partition fundamental reset in the corresponding partition.
GPIO[2]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: PART2PERSTN Alternate function pin type: Input/Output Alternate function: Assertion of this signal initiated a partition fundamental reset in the corresponding partition.
GPIO[3]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: PART3PERSTN Alternate function pin type: Input/Output Alternate function: Assertion of this signal initiated a partition fundamental reset in the corresponding partition.
GPIO[4]	I	General Purpose I/O. This pin can be configured as a general purpose I/O pin. 1st Alternate function — Reserved 2nd Alternate function pin name: P0LINKUPN 2nd Alternate function pin type: Output 2nd Alternate function: Port 0 Link Up Status output.
GPIO[5]	O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. 1st Alternate function pin name: GPEN 1st Alternate function pin type: Output 1st Alternate function: Hot-plug general purpose even output. 2nd Alternate function pin name: P0ACTIVEN 2nd Alternate function pin type: Output 2nd Alternate function: Port 0 Link Active Status Output.
GPIO[6]	I	General Purpose I/O. This pin can be configured as a general purpose I/O pin.
GPIO[7]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin.
GPIO[8]	I	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: IOEXPINTN Alternate function pin type: Input Alternate function: IO expander interrupt.

Table 4 General Purpose I/O Pins

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Signal	Type	Name/Description
CLKMODE[2:0]		**Clock Mode.** These signals determine the port clocking mode used by ports of the device.
GCLKFSEL	I	**Global Clock Frequency Select.** These signals select the frequency of the GCLKP and GCLKN signals. 0x0 100 MHz 0x1 125 MHz
P01MERGEN	I	**Port 0 and 1 Merge.** P01MERGEN is an active low signal. It is pulled low internally. When this pin is low, port 0 is merged with port 1 to form a single x8 port. The Serdes lanes associated with port 1 become lanes 4 through 7 of port 0. When this pin is high, port 0 and port 1 are not merged, and each operates as a single x4 port.
P23MERGEN	I	**Port 2 and 3 Merge.** P23MERGEN is an active low signal. It is pulled low internally. When this pin is low, port 2 is merged with port 3 to form a single x8 port. The Serdes lanes associated with port 3 become lanes 4 through 7 of port 2. When this pin is high, port 2 and port 3 are not merged, and each operates as a single x4 port.
P45MERGEN	I	**Port 4 and 5 Merge.** P45MERGEN is an active low signal. It is pulled low internally. When this pin is low, port 4 is merged with port 5 to form a single x8 port. The Serdes lanes associated with port 5 become lanes 4 through 7 of port 4. When this pin is high, port 4 and port 5 are not merged, and each operates as a single x4 port.
P67MERGEN	I	**Port 6 and 7 Merge.** P67MERGEN is an active low signal. It is pulled low internally. When this pin is low, port 6 is merged with port 7 to form a single x8 port. The Serdes lanes associated with port 7 become lanes 4 through 7 of port 6. When this pin is high, port 6 and port 7 are not merged, and each operates as a single x4 port.
P89MERGEN	I	**Port 8 and 9 Merge.** P89MERGEN is an active low signal. It is pulled low internally. When this pin is low, port 8 is merged with port 9 to form a single x8 port. The Serdes lanes associated with port 9 become lanes 4 through 7 of port 8. When this pin is high, port 8 and port 9 are not merged, and each operates as a single x4 port.
P1213MERGEN	I	**Port 12 and 13 Merge.** P1213MERGEN is an active low signal. It is pulled low internally. When this pin is low, port 12 is merged with port 13 to form a single x8 port. The Serdes lanes associated with port 13 become lanes 4 through 7 of port 12. When this pin is high, port 12 and port 13 are not merged, and each operates as a single x4 port.

Table 5 System Pins (Part 1 of 2)

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Signal	Type	Name/Description
PERSTN	I	**Global Reset.** Assertion of this signal resets all logic inside PES48H12G2.
RSTHALT	I	**Reset Halt.** When this signal is asserted during a PCI Express fundamental reset, PES48H12G2 executes the reset procedure and remains in a reset state with the Master and Slave SMBuses active. This allows software to read and write registers internal to the device before normal device operation begins. The device exits the reset state when the RSTHALT bit is cleared in the SWCTL register by an SMBus master.
SWMODE[3:0]	I	**Switch Mode.** These configuration pins determine the PES48H12G2 switch operating mode. **Note:** These pins should be static and not change following the negation of PERSTN. 0x0 - Single partition 0x1 - Single partition with Serial EEPROM initialization 0x2 through 0x7 - Reserved 0x8 - Single partition with port 0 selected as the upstream port (port 2 disabled) 0x9 - Single partition with port 2 selected as the upstream port (port 0 disabled) 0xA - Single partition with Serial EEPROM initialization and port 0 selected as the upstream port (port 2 disabled) 0xB - Single partition with Serial EEPROM initialization and port 2 selected as the upstream port (port 0 disabled) 0xC - Multi-partition 0xD - Multi-partition with Serial EEPROM initialization 0xE - Reserved 0xF - Reserved

Table 5 System Pins (Part 2 of 2)

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Signal	Type	Name/Description
JTAG_TCK	I	**JTAG Clock**. This is an input test clock used to clock the shifting of data into or out of the boundary scan logic or JTAG Controller. JTAG_TCK is independent of the system clock with a nominal 50% duty cycle.
JTAG_TDI	I	**JTAG Data Input**. This is the serial data input to the boundary scan logic or JTAG Controller.
JTAG_TDO	O	**JTAG Data Output**. This is the serial data shifted out from the boundary scan logic or JTAG Controller. When no data is being shifted out, this signal is tri-stated.
JTAG_TMS	I	**JTAG Mode**. The value on this signal controls the test mode select of the boundary scan logic or JTAG Controller.
JTAG_TRST_N	I	**JTAG Reset**. This active low signal asynchronously resets the boundary scan logic and JTAG TAP Controller. An external pull-up on the board is recommended to meet the JTAG specification in cases where the tester can access this signal. However, for systems running in functional mode, one of the following should occur: 1) actively drive this signal low with control logic 2) statically drive this signal low with an external pull-down on the board

Table 6 Test Pins

Signal	Type	Name/Description
REFRES[13,12,9:0]	I/O	**External Reference Resistors.** Provides a reference for the SerDes bias currents and PLL calibration circuitry. A 3 kOhm +/- 1% resistor should be connected from these pins to ground.
REFRESPLL	I/O	**PLL External Reference Resistor.** Provides a reference for the PLL bias currents and PLL calibration circuitry. A 3K Ohm +/- 1% resistor should be connected from this pin to ground.
V_{DD}CORE	I	**Core V_{DD}.** Power supply for core logic (1.0V).
V_{DD}I/O	I	**I/O V_{DD}.** LVTTL I/O buffer power supply (2.5V or preferred 3.3V).
V_{DD}PEA	I	**PCI Express Analog Power.** Serdes analog power supply (1.0V).
V_{DD}PEHA	I	**PCI Express Analog High Power.** Serdes analog power supply (2.5V).
V_{DD}PETA	I	**PCI Express Transmitter Analog Voltage.** Serdes transmitter analog power supply (1.0V).
V_{SS}	I	**Ground.**

Table 7 Power, Ground, and SerDes Resistor Pins

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Pin Characteristics

Note: Some input pads of the switch do not contain internal pull-ups or pull-downs. Unused SMBus and System inputs should be tied off to appropriate levels. This is especially critical for unused control signal inputs which, if left floating, could adversely affect operation. Also, any of these pins left floating can cause a slight increase in power consumption. Finally, unused Serdes (Rx and Tx) pins should be left floating.

Function	Pin Name	Type	Buffer	I/O Type	Internal Resistor[1]	Notes
PCI Express Interface	PE00RN[3:0]	I	PCIe Differential[2]	Serial Link		
	PE00RP[3:0]	I				
	PE00TN[3:0]	O				
	PE00TP[3:0]	O				
	PE01RN[3:0]	I				
	PE01RP[3:0]	I				
	PE01TN[3:0]	O				
	PE01TP[3:0]	O				
	PE02RN[3:0]	I				
	PE02RP[3:0]	I				
	PE02TN[3:0]	O				
	PE02TP[3:0]	O				
	PE03RN[3:0]	I				
	PE03RP[3:0]	I				
	PE03TN[3:0]	O				
	PE03TP[3:0]	O				
	PE04RN[3:0]	I				
	PE04RP[3:0]	I				
	PE04TN[3:0]	O				
	PE04TP[3:0]	O				
	PE05RN[3:0]	I				
	PE05RP[3:0]	I				
	PE05TN[3:0]	O				
	PE05TP[3:0]	O				
	PE06RN[3:0]	I				
	PE06RP[3:0]	I				
	PE06TN[3:0]	O				
	PE06TP[3:0]	O				
	PE07RN[3:0]	I				
	PE07RP[3:0]	I				
	PE07TN[3:0]	O				
	PE07TP[3:0]	O				
	PE08RN[3:0]	I				
	PE08RP[3:0]	I				
	PE08TN[3:0]	O				

Table 8 Pin Characteristics (Part 1 of 3)

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Function	Pin Name	Type	Buffer	I/O Type	Internal Resistor[1]	Notes
PCI Express Interface (Cont.)	PE08TP[3:0]	O	PCIe Differential	Serial Link		
	PE09RN[3:0]	I				
	PE09RP[3:0]	I				
	PE09TN[3:0]	O				
	PE09TP[3:0]	O				
	PE12RN[3:0]	I				
	PE12RP[3:0]	I				
	PE12TN[3:0]	O				
	PE12TP[3:0]	O				
	PE13RN[3:0]	I				
	PE13RP[3:0]	I				
	PE13TN[3:0]	O				
	PE13TP[3:0]	O				
	GCLKN[1:0]	I	HCSL	Diff. Clock Input		Refer to Table 9
	GCLKP[1:0]	I				
	P00CLKN, P00CLKP	I				
	P02CLKN, P02CLKP	I				
SMBus	MSMBCLK	I/O	LVTTL	STI[3]		pull-up on board
	MSMBDAT	I/O		STI		pull-up on board
	SSMBADDR[2:1]	I		Input	pull-up	
	SSMBCLK	I/O		STI		pull-up on board
	SSMBDAT	I/O		STI		pull-up on board
General Purpose I/O	GPIO[8:0]	I/O	LVTTL	STI, High Drive	pull-up	
System Pins	CLKMODE[1:0]	I	LVTTL	Input	pull-up	
	CLKMODE[2]	I			pull-down	
	GCLKFSEL	I			pull-down	
	P01MERGEN	I			pull-down	
	P23MERGEN	I			pull-down	
	P45MERGEN	I			pull-down	
	P67MERGEN	I			pull-down	
	P89MERGEN	I			pull-down	
	P1213MERGEN	I			pull-down	
	PERSTN	I		STI		
	RSTHALT	I		Input	pull-down	
	SWMODE[3:0]	I			pull-down	

Table 8 Pin Characteristics (Part 2 of 3)

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Function	Pin Name	Type	Buffer	I/O Type	Internal Resistor[1]	Notes
EJTAG / JTAG	JTAG_TCK	I	LVTTL	STI	pull-up	
	JTAG_TDI	I		STI	pull-up	
	JTAG_TDO	O				
	JTAG_TMS	I		STI	pull-up	
	JTAG_TRST_N	I		STI	pull-up	
SerDes Reference Resistors	REFRES00	I/O	Analog			
	REFRES01	I/O				
	REFRES02	I/O				
	REFRES03	I/O				
	REFRES04	I/O				
	REFRES05	I/O				
	REFRES06	I/O				
	REFRES07	I/O				
	REFRES08	I/O				
	REFRES09	I/O				
	REFRES12	I/O				
	REFRES13	I/O				
	REFRESPLL	I/O				

Table 8 Pin Characteristics (Part 3 of 3)

1. Internal resistor values under typical operating conditions are 92K Ω for pull-up and 91K Ω for pull-down.

2. All receiver pins set the DC common mode voltage to ground. All transmitters must be AC coupled to the media.

3. Schmitt Trigger Input (STI).

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Logic Diagram — PES48H12G2

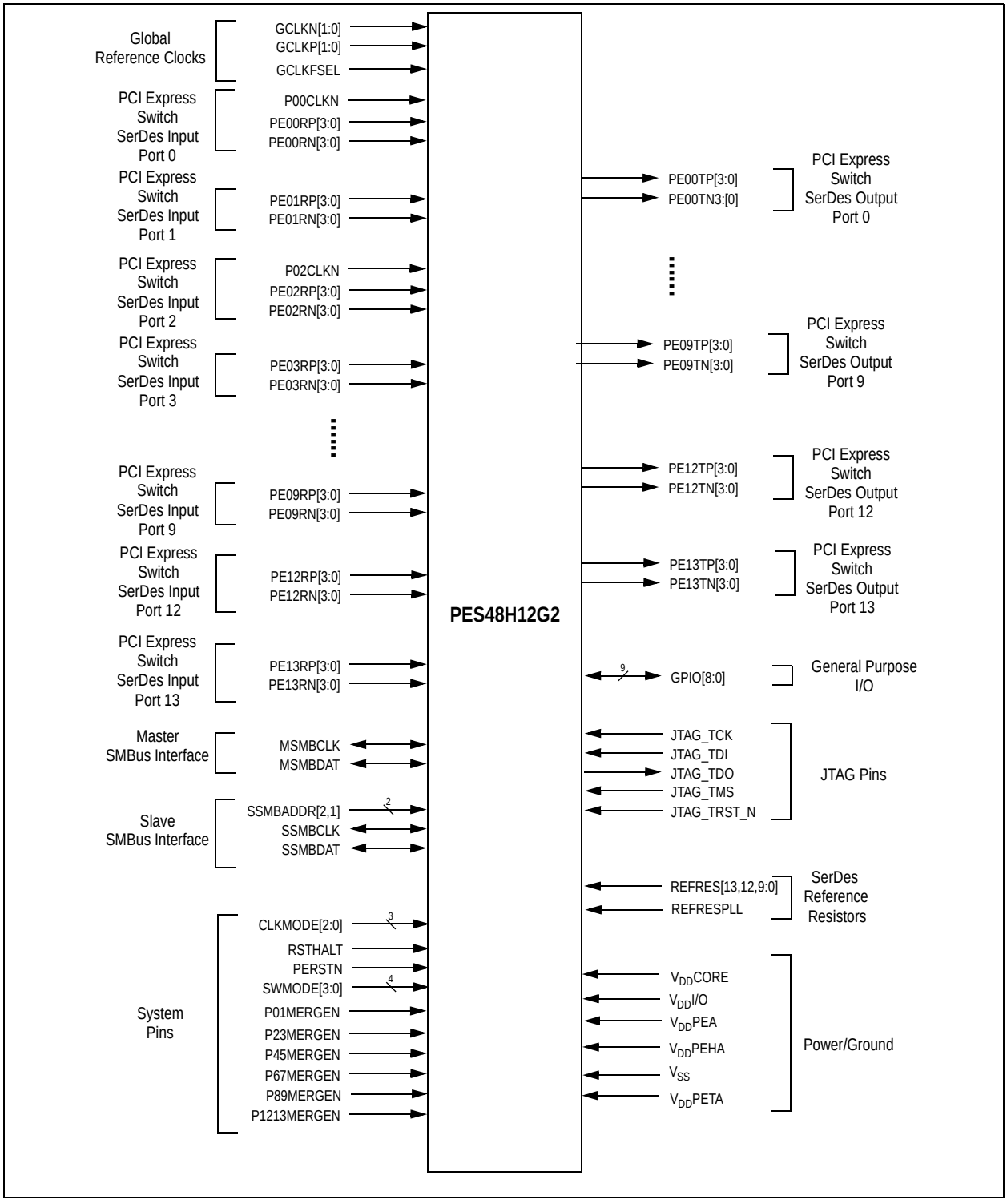


Figure 4 PES48H12G2 Logic Diagram

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System Clock Parameters

Values based on systems running at recommended supply voltages and operating temperatures, as shown in Tables 13 and 14.

Parameter	Description	Condition	Min	Typical	Max	Unit
$Refclk_{FREQ}$	Input reference clock frequency range		100		125[1]	MHz
T_{C-RISE}	Rising edge rate	Differential	0.6		4	V/ns
T_{C-FALL}	Falling edge rate	Differential	0.6		4	V/ns
V_{IH}	Differential input high voltage	Differential	+150			mV
V_{IL}	Differential input low voltage	Differential			-150	mV
V_{CROSS}	Absolute single-ended crossing point voltage	Single-ended	+250		+550	mV
$V_{CROSS-DELTA}$	Variation of V_{CROSS} over all rising clock edges	Single-ended			+140	mV
V_{RB}	Ring back voltage margin	Differential	-100		+100	mV
T_{STABLE}	Time before V_{RB} is allowed	Differential	500			ps
$T_{PERIOD-AVG}$	Average clock period accuracy		-300		2800	ppm
$T_{PERIOD-ABS}$	Absolute period, including spread-spectrum and jitter		9.847		10.203	ns
$T_{CC-JITTER}$	Cycle to cycle jitter				150	ps
V_{MAX}	Absolute maximum input voltage				+1.15	V
V_{MIN}	Absolute minimum input voltage		-0.3			V
Duty Cycle	Duty cycle		40		60	%
Rise/Fall Matching	Single ended rising Refclk edge rate versus falling Refclk edge rate			20		%
Z_{C-DC}	Clock source output DC impedance		40		60	Ω

Table 9 Input Clock Requirements

1. The input clock frequency will be either 100 or 125 MHz depending on signal GCLKFSEL.

AC Timing Characteristics

Parameter	Description	Gen 1			Gen 2			Units
		Min[1]	Typ[1]	Max[1]	Min[1]	Typ[1]	Max[1]	
PCIe Transmit								
UI	Unit Interval	399.88	400	400.12	199.94	200	200.06	ps
T_{TX-EYE}	Minimum Tx Eye Width	0.75			0.75			UI
$T_{TX-EYE-MEDIAN-to-MAX-JITTER}$	Maximum time between the jitter median and maximum deviation from the median			0.125				UI
$T_{TX-RISE}$, $T_{TX-FALL}$	TX Rise/Fall Time: 20% - 80%	0.125			0.15			UI
$T_{TX-IDLE-MIN}$	Minimum time in idle	20			20			UI

Table 10 PCIe AC Timing Characteristics (Part 1 of 2)

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Parameter	Description	Gen 1			Gen 2			Units
		Min[1]	Typ[1]	Max[1]	Min[1]	Typ[1]	Max[1]	
$T_{TX-IDLE-SET-TO-IDLE}$	Maximum time to transition to a valid Idle after sending an Idle ordered set			8			8	ns
$T_{TX-IDLE-TO-DIFF-DATA}$	Maximum time to transition from valid idle to diff data			8			8	ns
$T_{TX-SKEW}$	Transmitter data skew between any 2 lanes			1.3			1.3	ns
$T_{MIN-PULSED}$	Minimum Instantaneous Lone Pulse Width	NA			0.9			UI
$T_{TX-HF-DJ-DD}$	Transmitter Deterministic Jitter > 1.5MHz Bandwidth	NA					0.15	UI
$T_{RF-MISMATCH}$	Rise/Fall Time Differential Mismatch	NA					0.1	UI
PCIe Receive								
UI	Unit Interval	399.88	400	400.12	199.94		200.06	ps
$T_{RX-EYE\ (with\ jitter)}$	Minimum Receiver Eye Width (jitter tolerance)	0.4			0.4			UI
$T_{RX-EYE-MEDIUM\ TO\ MAX\ JITTER}$	Max time between jitter median & max deviation			0.3				UI
$T_{RX-SKEW}$	Lane to lane input skew			20			8	ns
$T_{RX-HF-RMS}$	1.5 — 100 MHz RMS jitter (common clock)	NA					3.4	ps
$T_{RX-HF-DJ-DD}$	Maximum tolerable DJ by the receiver (common clock)	NA					88	ps
$T_{RX-LF-RMS}$	10 KHz to 1.5 MHz RMS jitter (common clock)	NA					4.2	ps
$T_{RX-MIN-PULSE}$	Minimum receiver instantaneous eye width	NA			0.6			UI

Table 10 PCIe AC Timing Characteristics (Part 2 of 2)

1. Minimum, Typical, and Maximum values meet the requirements under PCI Specification 2.0

Signal	Symbol	Reference Edge	Min	Max	Unit	Timing Diagram Reference
GPIO						
GPIO[8:0][1]	Tpw[2]	None	50	—	ns	

Table 11 GPIO AC Timing Characteristics

1. GPIO signals must meet the setup and hold times if they are synchronous or the minimum pulse width if they are asynchronous.

2. The values for this symbol were determined by calculation, not by testing.

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Signal	Symbol	Reference Edge	Min	Max	Unit	Timing Diagram Reference
JTAG						
JTAG_TCK	Tper_16a	none	50.0	—	ns	See Figure 5.
	Thigh_16a, Tlow_16a		10.0	25.0	ns	
JTAG_TMS[1], JTAG_TDI	Tsu_16b	JTAG_TCK rising	2.4	—	ns	
	Thld_16b		1.0	—	ns	
JTAG_TDO	Tdo_16c	JTAG_TCK falling	—	20	ns	
	Tdz_16c[2]		—	20	ns	
JTAG_TRST_N	Tpw_16d[2]	none	25.0	—	ns	

Table 12 JTAG AC Timing Characteristics

1. The JTAG specification, IEEE 1149.1, recommends that JTAG_TMS should be held at 1 while the signal applied at JTAG_TRST_N changes from 0 to 1. Otherwise, a race may occur if JTAG_TRST_N is deasserted (going from low to high) on a rising edge of JTAG_TCK when JTAG_TMS is low, because the TAP controller might go to either the Run-Test/Idle state or stay in the Test-Logic-Reset state.

2. The values for this symbol were determined by calculation, not by testing.

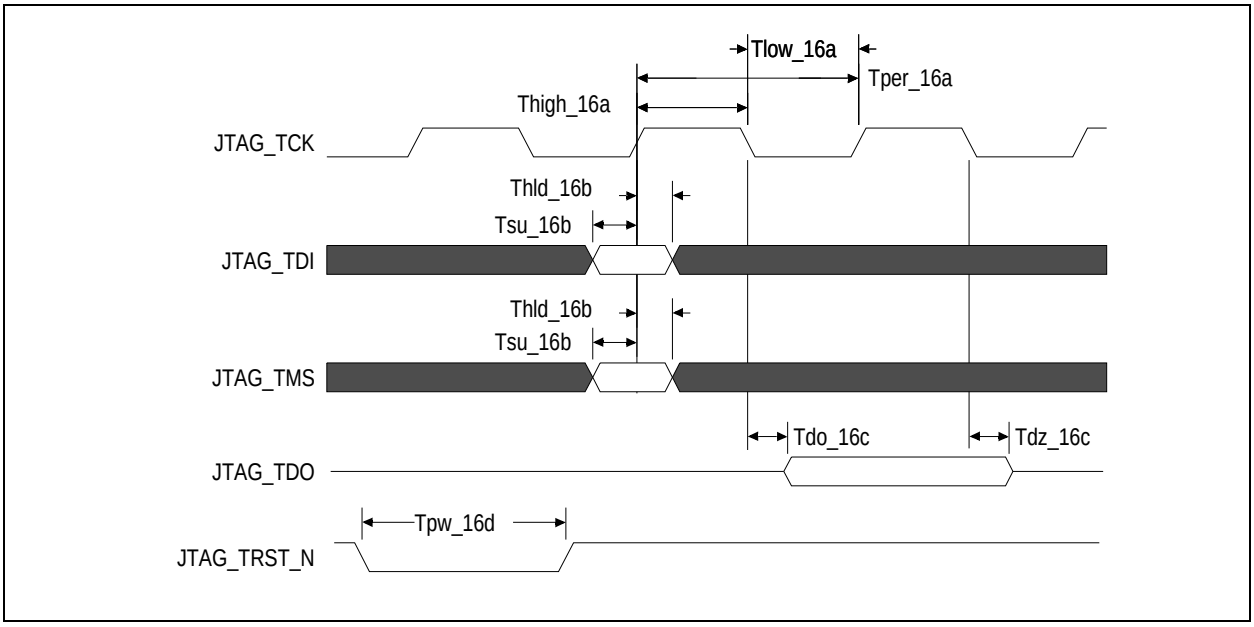


Figure 5 JTAG AC Timing Waveform

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Recommended Operating Supply Voltages

Symbol	Parameter	Minimum	Typical	Maximum	Unit
V_{DD}CORE	Internal logic supply	0.9	1.0	1.1	V
V_{DD}I/O	I/O supply except for SerDes	2.25	2.5	2.75	V
		3.125	3.3	3.465	V
V_{DD}PEA[1]	PCI Express Analog Power	0.95	1.0	1.1	V
V_{DD}PEHA[2]	PCI Express Analog High Power	2.25	2.5	2.75	V
V_{DD}PETA[1]	PCI Express Transmitter Analog Voltage	0.95	1.0	1.1	V
V_{SS}	Common ground	0	0	0	V

Table 13 PES48H12G2 Operating Voltages

1. V_{DD}PEA and V_{DD}PETA should have no more than 25m$V_{peak-peak}$ AC power supply noise superimposed on the 1.0V nominal DC value.
2. V_{DD}PEHA should have no more than 50m$V_{peak-peak}$ AC power supply noise superimposed on the 2.5V nominal DC value.

Power-Up/Power-Down Sequence

During power supply ramp-up, V_{DD}CORE must remain at least 1.0V below V_{DD}I/O at all times. There are no other power-up sequence requirements for the various operating supply voltages.

The power-down sequence can occur in any order.

Recommended Operating Temperature

Grade	Temperature
Commercial	0°C to +70°C Ambient
Industrial	-40°C to +85°C Ambient

Table 14 PES48H12G2 Operating Temperatures

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Power Consumption

Typical power is measured under the following conditions: 25°C Ambient, 35% total link usage on all ports, typical voltages defined in Table 13 (and also listed below).

Maximum power is measured under the following conditions: 70°C Ambient, 85% total link usage on all ports, maximum voltages defined in Table 13 (and also listed below).

Number of Active Lanes per Port		Core Supply		PCIe Analog Supply		PCIe Analog High Supply		PCIe Transmitter Supply		I/O Supply		Total	
		Typ 1.0V	Max 1.1V	Typ 1.0V	Max 1.1V	Typ 2.5V	Max 2.75V	Typ 1.0V	Max 1.1V	Typ 2.5V	Max 2.75V	Typ Power	Max Power
8/8/8/8/8/8 (Full Swing)	**mA**	3360	5529	2313	2705	816	825	845	898	24	29		
	Watts	3.36	6.08	2.31	2.98	2.04	2.27	0.85	0.99	0.06	0.08	8.62	12.40
8/8/8/8/8/8 (Half Swing)	**mA**	3360	5529	1989	2327	816	825	439	467	24	29		
	Watts	3.36	6.08	1.99	2.56	2.04	2.27	0.44	0.51	0.06	0.08	7.89	11.50

Table 15 PES48H12G2 Power Consumption — 2.5V I/O

Number of Active Lanes per Port		Core Supply		PCIe Analog Supply		PCIe Analog High Supply		PCIe Transmitter Supply		I/O Supply		Total	
		Typ 1.0V	Max 1.1V	Typ 1.0V	Max 1.1V	Typ 2.5V	Max 2.75V	Typ 1.0V	Max 1.1V	Typ 3.3V	Max 3.465V	Typ Power	Max Power
8/8/8/8/8/8 (Full Swing)	**mA**	3360	5529	2313	2705	816	825	845	898	30	35		
	Watts	3.36	6.08	2.31	2.98	2.04	2.27	0.85	0.99	0.10	0.12	8.66	12.44
8/8/8/8/8/8 (Half Swing)	**mA**	3360	5529	1989	2327	816	825	439	467	30	35		
	Watts	3.36	6.08	1.99	2.56	2.04	2.27	0.44	0.51	0.10	0.12	7.93	11.54

Table 16 PES48H12G2 Power Consumption — 3.3V I/O

Note 1: I/O supply of 3.3V is preferred.

Note 2: The above power consumption assumes that all ports are functioning at Gen2 (5.0 GT/S) speeds. Power consumption can be reduced by turning off unused ports through software or through boot EEPROM. Power savings will occur in V_{DD}PEA, V_{DD}PEHA, and V_{DD}PETA. Power savings can be estimated as directly proportional to the number of unused ports, since the power consumption of a turned-off port is close to zero. For example, if 2 ports out of 12 are turned off, then the power savings for each of the above three power rails can be calculated quite simply as 2/12 multiplied by the power consumption indicated in the above table.

Note 3: Using a port in Gen1 mode (2.5GT/S) results in approximately 18% power savings for each power rail: V_{DD}PEA, V_{DD}PEHA, and V_{DD}PETA.

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Thermal Considerations

This section describes thermal considerations for the PES48H12G2 (27mm^2 FCBGA676 package). The data in Table 17 below contains information that is relevant to the thermal performance of the PES48H12G2 switch.

Symbol	Parameter	Value	Units	Conditions
$T_{J(max)}$	Junction Temperature	125	^{0}C	Maximum
$T_{A(max)}$	Ambient Temperature	70	^{0}C	Maximum for commercial-rated products
		85	^{0}C	Maximum for industrial-rated products
$\theta_{JA(effective)}$	Effective Thermal Resistance, Junction-to-Ambient	14.6	^{0}C/W	Zero air flow
		7.8	^{0}C/W	1 m/S air flow
		6.4	^{0}C/W	2 m/S air flow
θ_{JB}	Thermal Resistance, Junction-to-Board	2.7	^{0}C/W	
θ_{JC}	Thermal Resistance, Junction-to-Case	0.15	^{0}C/W	
P	Power Dissipation of the Device	12.44	Watts	Maximum

Table 17 Thermal Specifications for PES48H12G2, 27x27 mm FCBGA676 Package

Note: It is important for the reliability of this device in any user environment that the junction temperature not exceed the $T_{J(max)}$ value specified in Table 17. Consequently, the effective junction to ambient thermal resistance (θ_{JA}) for the worst case scenario must be maintained below the value determined by the formula:

$$\theta_{JA} = (T_{J(max)} - T_{A(max)})/P$$

Given that the values of $T_{J(max)}$, $T_{A(max)}$, and P are known, the value of desired θ_{JA} becomes a known entity to the system designer. How to achieve the desired θ_{JA} is left up to the board or system designer, but in general, it can be achieved by adding the effects of θ_{JC} (value provided in Table 17), thermal resistance of the chosen adhesive (θ_{CS}), that of the heat sink (θ_{SA}), amount of airflow, and properties of the circuit board (number of layers and size of the board). It is strongly recommended that users perform their own thermal analysis for their own board and system design scenarios.

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DC Electrical Characteristics

Values based on systems running at recommended supply voltages, as shown in Table 13.

Note: See Table 8, Pin Characteristics, for a complete I/O listing.

I/O Type	Parameter	Description	Gen1			Gen2			Unit	Conditions
			Min[1]	Typ[1]	Max[1]	Min[1]	Typ[1]	Max[1]		
Serial Link	PCIe Transmit									
	$V_{TX-DIFFp-p}$	Differential peak-to-peak output voltage	800		1200	800		1200	mV	
	$V_{TX-DIFFp-p-LOW}$	Low-Drive Differential Peak to Peak Output Voltage	400		1200	400		1200	mV	
	$V_{TX-DE-RATIO-3.5dB}$	De-emphasized differential output voltage	-3		-4	-3.0	-3.5	-4.0	dB	
	$V_{TX-DE-RATIO-6.0dB}$	De-emphasized differential output voltage	NA			-5.5	-6.0	-6.5	dB	
	$V_{TX-DC-CM}$	DC Common mode voltage	0		3.6	0		3.6	V	
	$V_{TX-CM-ACP}$	RMS AC peak common mode output voltage			20				mV	
	$V_{TX-CM-DC-active-idle-delta}$	Abs delta of DC common mode voltage between L0 and idle			100			100	mV	
	$V_{TX-CM-DC-line-delta}$	Abs delta of DC common mode voltage between D+ and D-			25			25	mV	
	$V_{TX-Idle-DiffP}$	Electrical idle diff peak output			20			20	mV	
	$RL_{TX-DIFF}$	Transmitter Differential Return loss	10					10	dB	0.05 - 1.25GHz
								8	dB	1.25 - 2.5GHz
	RL_{TX-CM}	Transmitter Common Mode Return loss	6					6	dB	
	$Z_{TX-DIFF-DC}$	DC Differential TX impedance	80	100	120			120	Ω	
	VTX-CM-ACpp	Peak-Peak AC Common	NA					100	mV	
	$V_{TX-DC-CM}$	Transmit Driver DC Common Mode Voltage	0		3.6	0		3.6	V	
	$V_{TX-RCV-DETECT}$	The amount of voltage change allowed during Receiver Detection			600			600	mV	
	$I_{TX-SHORT}$	Transmitter Short Circuit Current Limit	0		90				90	mA

Table 18 DC Electrical Characteristics (Part 1 of 2)

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I/O Type	Parameter	Description	Gen1			Gen2			Unit	Conditions
			Min[1]	Typ[1]	Max[1]	Min[1]	Typ[1]	Max[1]		
Serial Link (cont.)	PCIe Receive									
	$V_{RX-DIFFp-p}$	Differential input voltage (peak-to-peak)	175		1200	120		1200	mV	
	$RL_{RX-DIFF}$	Receiver Differential Return Loss	10					10	dB	0.05 - 1.25GHz
								8		1.25 - 2.5GHz
	RL_{RX-CM}	Receiver Common Mode Return Loss	6					6	dB	
	$Z_{RX-DIFF-DC}$	Differential input impedance (DC)	80	100	120	Refer to return loss spec			Ω	
	Z_{RX--DC}	DC common mode impedance	40	50	60	40		60	Ω	
	$Z_{RX-COMM-DC}$	Powered down input common mode impedance (DC)	200k	350k				50k	Ω	
	$Z_{RX-HIGH-IMP-DC-POS}$	DC input CM input impedance for V>0 during reset or power down			50k			50k	Ω	
	$Z_{RX-HIGH-IMP-DC-NEG}$	DC input CM input impedance for V<0 during reset or power down			1.0k			1.0k	Ω	
	$V_{RX-IDLE-DET-DIFFp-p}$	Electrical idle detect threshold	65		175	65		175	mV	
	$V_{RX-CM-ACp}$	Receiver AC common-mode peak voltage			150			150	mV	$V_{RX-CM-ACp}$
PCIe REFCLK										
	C_{IN}	Input Capacitance	1.5	—		1.5	—		pF	
Other I/Os										
LOW Drive Output	I_{OL}		—	2.5	—	—	2.5	—	mA	V_{OL} = 0.4v
	I_{OH}		—	-5.5	—	—	-5.5	—	mA	V_{OH} = 1.5V
High Drive Output	I_{OL}		—	12.0	—	—	12.0	—	mA	V_{OL} = 0.4v
	I_{OH}		—	-20.0	—	—	-20.0	—	mA	V_{OH} = 1.5V
Schmitt Trigger Input (STI)	V_{IL}		-0.3	—	0.8	-0.3	—	0.8	V	—
	V_{IH}		2.0	—	V_{DD}I/O + 0.5	2.0	—	V_{DD}I/O + 0.5	V	—
Input	V_{IL}		-0.3	—	0.8	-0.3	—	0.8	V	—
	V_{IH}		2.0	—	V_{DD}I/O + 0.5	2.0	—	V_{DD}I/O + 0.5	V	—
Capacitance	C_{IN}		—	—	8.5	—	—	8.5	pF	—
Leakage	Inputs		—	—	± 10	—	—	± 10	µA	V_{DD}I/O (max)
	$I/O_{LEAK\ W/O}$ Pull-ups/downs		—	—	± 10	—	—	± 10	µA	V_{DD}I/O (max)
	$I/O_{LEAK\ WITH}$ Pull-ups/downs		—	—	± 80	—	—	± 80	µA	V_{DD}I/O (max)

Table 18 DC Electrical Characteristics (Part 2 of 2)

1. Minimum, Typical, and Maximum values meet the requirements under PCI Specification 2.0.

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Absolute Maximum Voltage Rating

Core Supply	PCIe Analog Supply	PCIe Analog High Supply	PCIe Transmitter Supply	I/O Supply
1.5V	1.5V	4.6V	1.5V	4.6V

Table 19 PES48H12G2 Absolute Maximum Voltage Rating

Warning: For proper and reliable operation in adherence with this data sheet, the device should not exceed the recommended operating voltages in Table 13. The absolute maximum operating voltages in Table 19 are offered to provide guidelines for voltage excursions outside the recommended voltage ranges. Device functionality is not guaranteed at these conditions and sustained operation at these values or any exposure to voltages outside the maximum range may adversely affect device functionality and reliability.

SMBus Characterization

Symbol	Parameter	SMBus 2.0 Char. Data[1]			Unit
		3V	3.3V	3.6V	
DC Parameter for SDA Pin					
V_{IL}	Input Low	1.16	1.26	1.35	V
V_{IH}	Input High	1.56	1.67	1.78	V
$V_{OL@350uA}$	Output Low	15	15	15	mV
$I_{OL@0.4V}$		23	24	25	mA
I_{Pullup}	Current Source	—	—	—	µA
I_{IL_Leak}	Input Low Leakage	0	0	0	µA
I_{IH_Leak}	Input High Leakage	0	0	0	µA
DC Parameter for SCL Pin					
$V_{IL\ (V)}$	Input Low	1.11	1.2	1.31	V
$V_{IH\ (V)}$	Input High	1.54	1.65	1.76	V
I_{IL_Leak}	Input Low Leakage	0	0	0	µA
I_{IH_Leak}	Input High Leakage	0	0	0	µA

Table 20 SMBus DC Characterization Data

1. Data at room and hot temperature.

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Symbol	Parameter	SMBus @3.3V ±10%[1]		Unit
		Min	Max	
F_{SCL}	Clock frequency	5	600	KHz
T_{BUF}	Bus free time between Stop and Start	3.5	—	µs
$T_{HD:STA}$	Start condition hold time	1	—	µs
$T_{SU:STA}$	Start condition setup time	1	—	µs
$T_{SU:STO}$	Stop condition setup time	1	—	µs
$T_{HD:DAT}$	Data hold time	1	—	ns
$T_{SU:DAT}$	Data setup time	1	—	ns
$T_{TIMEOUT}$	Detect clock low time out	—	74.7	ms
T_{LOW}	Clock low period	3.7	—	µs
T_{HIGH}	Clock high period	3.7	—	µs
T_F	Clock/Data fall time	—	72.2	ns
T_R	Clock/Data rise time	—	68.3	ns
$T_{POR@10kHz}$	Time which a device must be operational after power-on reset	20	—	ms

Table 21 SMBus AC Timing Data

1. Data at room and hot temperature.

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PES48H12G2 Package Pinout, 27x27mm 676-BGA Signal Pinout

The following table lists the pin numbers and signal names for the PES48H12G2 (27x27mm) device.

Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt
A1	V_{SS}		B9	PE08TN0		C17	V_{SS}		D25	V_{DD}I/O	
A2	V_{SS}		B10	V_{SS}		C18	V_{SS}		D26	V_{DD}I/O	
A3	V_{DD}I/O		B11	PE03TN3		C19	V_{SS}		E1	V_{SS}	
A4	V_{SS}		B12	PE03TN2		C20	V_{SS}		E2	V_{SS}	
A5	PE08TP3		B13	V_{SS}		C21	V_{SS}		E3	V_{SS}	
A6	PE08TP2		B14	PE03TN1		C22	V_{SS}		E4	V_{SS}	
A7	V_{SS}		B15	PE03TN0		C23	JTAG_TDO		E5	PE08RP3	
A8	PE08TP1		B16	V_{SS}		C24	JTAG_TDI		E6	PE08RP2	
A9	PE08TP0		B17	PE02TN3		C25	SSMBCLK		E7	V_{SS}	
A10	V_{SS}		B18	PE02TN2		C26	SSMBADDR1		E8	PE08RP1	
A11	PE03TP3		B19	V_{SS}		D1	V_{DD}I/O		E9	PE08RP0	
A12	PE03TP2		B20	PE02TN1		D2	V_{DD}I/O		E10	V_{SS}	
A13	V_{SS}		B21	PE02TN0		D3	V_{SS}		E11	PE03RP3	
A14	PE03TP1		B22	V_{DD}I/O		D4	V_{SS}		E12	PE03RP2	
A15	PE03TP0		B23	MSMBCLK		D5	PE08RN3		E13	V_{SS}	
A16	V_{SS}		B24	PERSTN		D6	PE08RN2		E14	PE03RP1	
A17	PE02TP3		B25	SSMBDAT		D7	V_{SS}		E15	PE03RP0	
A18	PE02TP2		B26	SSMBADDR2		D8	PE08RN1		E16	V_{SS}	
A19	V_{SS}		C1	V_{SS}		D9	PE08RN0		E17	PE02RP3	
A20	PE02TP1		C2	V_{SS}		D10	V_{SS}		E18	PE02RP2	
A21	PE02TP0		C3	V_{SS}		D11	PE03RN3		E19	V_{SS}	
A22	V_{DD}I/O		C4	V_{SS}		D12	PE03RN2		E20	PE02RP1	
A23	MSMBDAT		C5	V_{SS}		D13	REFRES03		E21	PE02RP0	
A24	JTAG_TMS		C6	V_{SS}		D14	PE03RN1		E22	PE01RP3	
A25	CLKMODE1		C7	V_{SS}		D15	PE03RN0		E23	PE01RN3	
A26	JTAG_TCK		C8	V_{SS}		D16	V_{SS}		E24	V_{SS}	
B1	V_{SS}		C9	V_{SS}		D17	PE02RN3		E25	PE01TN3	
B2	V_{SS}		C10	V_{SS}		D18	PE02RN2		E26	PE01TP3	
B3	V_{DD}I/O		C11	V_{SS}		D19	V_{SS}		F1	PE09TP0	
B4	V_{SS}		C12	V_{SS}		D20	PE02RN1		F2	PE09TN0	
B5	PE08TN3		C13	V_{SS}		D21	PE02RN0		F3	V_{SS}	
B6	PE08TN2		C14	V_{SS}		D22	JTAG_TRST_N		F4	PE09RN0	
B7	V_{SS}		C15	V_{SS}		D23	V_{SS}		F5	PE09RP0	
B8	PE08TN1		C16	V_{SS}		D24	V_{SS}		F6	V_{SS}	

Table 22 PES48H12G2 Signal Pin-Out (Part 1 of 5)

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Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt
F7	V_{SS}		G18	V_{DD}PETA		J3	V_{SS}		K14	V_{SS}	
F8	V_{DD}PEHA		G19	V_{DD}PEHA		J4	PE09RN2		K15	V_{DD}CORE	
F9	REFRES08		G20	V_{SS}		J5	PE09RP2		K16	V_{DD}CORE	
F10	V_{DD}PEHA		G21	V_{SS}		J6	V_{DD}PEA		K17	V_{SS}	
F11	V_{DD}PETA		G22	V_{SS}		J7	V_{DD}PEA		K18	V_{SS}	
F12	REFRESPLL		G23	V_{SS}		J8	V_{DD}PEA		K19	V_{DD}PETA	
F13	GCLKP0		G24	V_{SS}		J9	V_{SS}		K20	V_{DD}PETA	
F14	V_{DD}PEA		G25	V_{SS}		J10	V_{SS}		K21	V_{DD}PETA	
F15	P02CLKP		G26	V_{SS}		J11	V_{DD}CORE		K22	V_{SS}	
F16	REFRES02		H1	V_{SS}		J12	V_{DD}CORE		K23	V_{SS}	
F17	V_{DD}PEA		H2	V_{SS}		J13	V_{SS}		K24	V_{SS}	
F18	V_{DD}PETA		H3	V_{SS}		J14	V_{SS}		K25	V_{SS}	
F19	V_{DD}PEHA		H4	V_{SS}		J15	V_{DD}CORE		K26	V_{SS}	
F20	V_{SS}		H5	V_{SS}		J16	V_{DD}CORE		L1	V_{SS}	
F21	V_{SS}		H6	V_{DD}PEA		J17	V_{SS}		L2	V_{SS}	
F22	PE01RP2		H7	V_{DD}PEA		J18	V_{SS}		L3	V_{SS}	
F23	PE01RN2		H8	V_{DD}PEA		J19	V_{DD}PEA		L4	V_{SS}	
F24	V_{SS}		H9	V_{SS}		J20	V_{DD}PEA		L5	V_{SS}	
F25	PE01TN2		H10	V_{SS}		J21	V_{DD}PEA		L6	V_{DD}PEHA	
F26	PE01TP2		H11	V_{DD}CORE		J22	PE01RP0		L7	V_{DD}PEHA	
G1	PE09TP1		H12	V_{DD}CORE		J23	PE01RN0		L8	V_{DD}PEHA	
G2	PE09TN1		H13	V_{SS}		J24	V_{SS}		L9	V_{SS}	
G3	V_{SS}		H14	V_{SS}		J25	PE01TN0		L10	V_{SS}	
G4	PE09RN1		H15	V_{DD}CORE		J26	PE01TP0		L11	V_{DD}CORE	
G5	PE09RP1		H16	V_{DD}CORE		K1	PE09TP3		L12	V_{DD}CORE	
G6	V_{SS}		H17	V_{SS}		K2	PE09TN3		L13	V_{SS}	
G7	V_{SS}		H18	V_{SS}		K3	V_{SS}		L14	V_{SS}	
G8	V_{DD}PEHA		H19	V_{DD}PEA		K4	PE09RN3		L15	V_{DD}CORE	
G9	REFRES09		H20	V_{DD}PEA		K5	PE09RP3		L16	V_{DD}CORE	
G10	V_{DD}PEHA		H21	V_{DD}PEA		K6	V_{DD}PETA		L17	V_{SS}	
G11	V_{DD}PETA		H22	PE01RP1		K7	V_{DD}PETA		L18	V_{SS}	
G12	V_{SS}		H23	PE01RN1		K8	V_{DD}PETA		L19	V_{DD}PEHA	
G13	GCLKN0		H24	V_{SS}		K9	V_{SS}		L20	REFRES01	
G14	V_{DD}PEA		H25	PE01TN1		K10	V_{SS}		L21	V_{DD}PETA	
G15	P02CLKN		H26	PE01TP1		K11	V_{DD}CORE		L22	PE00RP3	
G16	NC		J1	PE09TP2		K12	V_{DD}CORE		L23	PE00RN3	
G17	V_{DD}PEA		J2	PE09TN2		K13	V_{SS}		L24	V_{SS}	

Table 22 PES48H12G2 Signal Pin-Out (Part 2 of 5)

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Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt
L25	PE00TN3		N10	V_{SS}		P21	V_{DD}PEA		T6	V_{DD}PETA	
L26	PE00TP3		N11	V_{DD}CORE		P22	PE00RP1		T7	V_{DD}PETA	
M1	PE04TP0		N12	V_{DD}CORE		P23	PE00RN1		T8	V_{DD}PETA	
M2	PE04TN0		N13	V_{SS}		P24	V_{SS}		T9	V_{SS}	
M3	V_{SS}		N14	V_{SS}		P25	PE00TN1		T10	V_{SS}	
M4	PE04RN0		N15	V_{DD}CORE		P26	PE00TP1		T11	V_{DD}CORE	
M5	PE04RP0		N16	V_{DD}CORE		R1	PE04TP2		T12	V_{DD}CORE	
M6	V_{SS}		N17	V_{SS}		R2	PE04TN2		T13	V_{SS}	
M7	V_{SS}		N18	V_{SS}		R3	V_{SS}		T14	V_{SS}	
M8	V_{SS}		N19	V_{DD}PEHA		R4	PE04RN2		T15	V_{DD}CORE	
M9	V_{SS}		N20	NC		R5	PE04RP2		T16	V_{DD}CORE	
M10	V_{SS}		N21	NC		R6	REFRES05		T17	V_{SS}	
M11	V_{DD}CORE		N22	NC		R7	REFRES04		T18	V_{SS}	
M12	V_{DD}CORE		N23	REFRES00		R8	V_{DD}PETA		T19	V_{DD}PEHA	
M13	V_{SS}		N24	V_{SS}		R9	V_{SS}		T20	V_{DD}PEHA	
M14	V_{SS}		N25	V_{SS}		R10	V_{SS}		T21	V_{DD}PEHA	
M15	V_{DD}CORE		N26	V_{SS}		R11	V_{DD}CORE		T22	V_{SS}	
M16	V_{DD}CORE		P1	V_{SS}		R12	V_{DD}CORE		T23	V_{SS}	
M17	V_{SS}		P2	V_{SS}		R13	V_{SS}		T24	V_{SS}	
M18	V_{SS}		P3	V_{SS}		R14	V_{SS}		T25	V_{SS}	
M19	V_{DD}PEHA		P4	V_{SS}		R15	V_{DD}CORE		T26	V_{SS}	
M20	P00CLKN		P5	V_{SS}		R16	V_{DD}CORE		U1	V_{SS}	
M21	P00CLKP		P6	NC		R17	V_{SS}		U2	V_{SS}	
M22	PE00RP2		P7	NC		R18	V_{SS}		U3	V_{SS}	
M23	PE00RN2		P8	V_{DD}PEA		R19	V_{DD}PETA		U4	V_{SS}	
M24	V_{SS}		P9	V_{SS}		R20	V_{DD}PETA		U5	V_{SS}	
M25	PE00TN2		P10	V_{SS}		R21	V_{DD}PETA		U6	V_{DD}PEHA	
M26	PE00TP2		P11	V_{DD}CORE		R22	PE00RP0		U7	V_{DD}PEHA	
N1	PE04TP1		P12	V_{DD}CORE		R23	PE00RN0		U8	V_{DD}PEHA	
N2	PE04TN1		P13	V_{SS}		R24	V_{SS}		U9	V_{SS}	
N3	V_{SS}		P14	V_{SS}		R25	PE00TN0		U10	V_{SS}	
N4	PE04RN1		P15	V_{DD}CORE		R26	PE00TP0		U11	V_{DD}CORE	
N5	PE04RP1		P16	V_{DD}CORE		T1	PE04TP3		U12	V_{DD}CORE	
N6	V_{DD}PEA		P17	V_{SS}		T2	PE04TN3		U13	V_{SS}	
N7	V_{DD}PEA		P18	V_{SS}		T3	V_{SS}		U14	V_{SS}	
N8	V_{DD}PEA		P19	V_{DD}PEA		T4	PE04RN3		U15	V_{DD}CORE	
N9	V_{SS}		P20	V_{DD}PEA		T5	PE04RP3		U16	V_{DD}CORE	

Table 22 PES48H12G2 Signal Pin-Out (Part 3 of 5)

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Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt
U17	V_{SS}		W2	PE05TN1		Y13	V_{DD}PEHA		AA24	V_{SS}	
U18	V_{SS}		W3	V_{SS}		Y14	GCLKN1		AA25	PE13TN0	
U19	V_{SS}		W4	PE05RN1		Y15	REFRES12		AA26	PE13TP0	
U20	V_{SS}		W5	PE05RP1		Y16	REFRES13		AB1	PE05TP3	
U21	V_{SS}		W6	V_{DD}PEA		Y17	V_{DD}PEA		AB2	PE05TN3	
U22	PE13RP3		W7	V_{DD}PEA		Y18	V_{DD}PEHA		AB3	V_{DD}I/O	
U23	PE13RN3		W8	V_{DD}PEA		Y19	V_{DD}PETA		AB4	PE05RN3	
U24	V_{SS}		W9	V_{SS}		Y20	V_{SS}		AB5	PE05RP3	
U25	PE13TN3		W10	V_{SS}		Y21	V_{SS}		AB6	PE06RP0	
U26	PE13TP3		W11	V_{DD}CORE		Y22	PE13RP1		AB7	PE06RP1	
V1	PE05TP0		W12	V_{DD}CORE		Y23	PE13RN1		AB8	V_{SS}	
V2	PE05TN0		W13	V_{SS}		Y24	V_{SS}		AB9	PE06RP2	
V3	V_{SS}		W14	V_{SS}		Y25	PE13TN1		AB10	PE06RP3	
V4	PE05RN0		W15	V_{DD}CORE		Y26	PE13TP1		AB11	V_{SS}	
V5	PE05RP0		W16	V_{DD}CORE		AA1	PE05TP2		AB12	PE07RP0	
V6	V_{DD}PEA		W17	V_{SS}		AA2	PE05TN2		AB13	PE07RP1	
V7	V_{DD}PEA		W18	V_{SS}		AA3	V_{DD}I/O		AB14	V_{SS}	
V8	V_{DD}PEA		W19	V_{DD}PEA		AA4	PE05RN2		AB15	PE07RP2	
V9	V_{SS}		W20	V_{DD}PEA		AA5	PE05RP2		AB16	PE07RP3	
V10	V_{SS}		W21	V_{DD}PEA		AA6	V_{SS}		AB17	V_{SS}	
V11	V_{DD}CORE		W22	V_{SS}		AA7	V_{SS}		AB18	PE12RP0	
V12	V_{DD}CORE		W23	V_{SS}		AA8	V_{DD}PETA		AB19	PE12RP1	
V13	V_{SS}		W24	V_{SS}		AA9	V_{DD}PEHA		AB20	V_{SS}	
V14	V_{SS}		W25	V_{SS}		AA10	V_{DD}PEA		AB21	PE12RP2	
V15	V_{DD}CORE		W26	V_{SS}		AA11	V_{DD}PETA		AB22	PE12RP3	
V16	V_{DD}CORE		Y1	V_{SS}		AA12	V_{DD}PETA		AB23	V_{SS}	
V17	V_{SS}		Y2	V_{SS}		AA13	V_{DD}PEHA		AB24	V_{DD}I/O	
V18	V_{SS}		Y3	V_{SS}		AA14	GCLKP1		AB25	V_{SS}	
V19	V_{DD}PEA		Y4	V_{SS}		AA15	V_{SS}		AB26	V_{SS}	
V20	V_{DD}PEA		Y5	V_{SS}		AA16	V_{SS}		AC1	V_{DD}I/O	
V21	V_{DD}PEA		Y6	V_{SS}		AA17	V_{DD}PEA		AC2	V_{DD}I/O	
V22	PE13RP2		Y7	V_{SS}		AA18	V_{DD}PEHA		AC3	V_{SS}	
V23	PE13RN2		Y8	V_{DD}PETA		AA19	V_{DD}PETA		AC4	V_{SS}	
V24	V_{SS}		Y9	V_{DD}PEHA		AA20	V_{SS}		AC5	CLKMODE2	
V25	PE13TN2		Y10	V_{DD}PEA		AA21	V_{SS}		AC6	PE06RN0	
V26	PE13TP2		Y11	REFRES06		AA22	PE13RP0		AC7	PE06RN1	
W1	PE05TP1		Y12	REFRES07		AA23	PE13RN0		AC8	V_{SS}	

Table 22 PES48H12G2 Signal Pin-Out (Part 4 of 5)

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Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt
AC9	PE06RN2		AD7	V_{SS}		AE5	SWMODE1		AF3	RSTHALT	
AC10	PE06RN3		AD8	V_{SS}		AE6	PE06TN0		AF4	SWMODE2	
AC11	V_{SS}		AD9	V_{SS}		AE7	PE06TN1		AF5	SWMODE3	
AC12	PE07RN0		AD10	V_{SS}		AE8	V_{SS}		AF6	PE06TP0	
AC13	PE07RN1		AD11	V_{SS}		AE9	PE06TN2		AF7	PE06TP1	
AC14	V_{SS}		AD12	V_{SS}		AE10	PE06TN3		AF8	V_{SS}	
AC15	PE07RN2		AD13	V_{SS}		AE11	V_{SS}		AF9	PE06TP2	
AC16	PE07RN3		AD14	V_{SS}		AE12	PE07TN0		AF10	PE06TP3	
AC17	V_{SS}		AD15	V_{SS}		AE13	PE07TN1		AF11	V_{SS}	
AC18	PE12RN0		AD16	V_{SS}		AE14	V_{SS}		AF12	PE07TP0	
AC19	PE12RN1		AD17	V_{SS}		AE15	PE07TN2		AF13	PE07TP1	
AC20	V_{SS}		AD18	V_{SS}		AE16	PE07TN3		AF14	V_{SS}	
AC21	PE12RN2		AD19	V_{SS}		AE17	V_{SS}		AF15	PE07TP2	
AC22	PE12RN3		AD20	V_{SS}		AE18	PE12TN0		AF16	PE07TP3	
AC23	V_{SS}		AD21	V_{SS}		AE19	PE12TN1		AF17	V_{SS}	
AC24	V_{DD}I/O		AD22	V_{SS}		AE20	V_{SS}		AF18	PE12TP0	
AC25	GPIO_04	1	AD23	V_{SS}		AE21	PE12TN2		AF19	PE12TP1	
AC26	GPIO_08	1	AD24	V_{DD}I/O		AE22	PE12TN3		AF20	V_{SS}	
AD1	V_{DD}I/O		AD25	GPIO_05	2	AE23	V_{SS}		AF21	PE12TP2	
AD2	P23MERGEN		AD26	GPIO_06		AE24	V_{DD}I/O		AF22	PE12TP3	
AD3	P1213MERGEN		AE1	P01MERGEN		AE25	GPIO_02	1	AF23	V_{SS}	
AD4	GCLKFSEL		AE2	P67MERGEN		AE26	GPIO_07		AF24	GPIO_01	1
AD5	SWMODE0		AE3	P89MERGEN		AF1	CLKMODE0		AF25	GPIO_00	1
AD6	V_{SS}		AE4	V_{DD}I/O		AF2	P45MERGEN		AF26	GPIO_03	1

Table 22 PES48H12G2 Signal Pin-Out (Part 5 of 5)

Alternate Signal Functions

Pin	GPIO	1st Alternate	2nd Alternate
AF25	GPIO_00	PART0PERSTN	—
AF24	GPIO_01	PART1PERSTN	—
AE25	GPIO_02	PART2PERSTN	—
AF26	GPIO_03	PART3PERSTN	
AC25	GPIO_04	—	P0LINKUPN
AD25	GPIO_05	GPEN	P0ACTIVEN
AC26	GPIO_08	IOEXPINTN	—

Table 23 PES48H12G2 Alternate Signal Functions

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Power Pins

V_{DD}Core	V_{DD}Core	V_{DD}I/O	V_{DD}PEA	V_{DD}PEA	V_{DD}PEHA	V_{DD}PETA
H11	P11	A3	F14	P19	F8	F11
H12	P12	A22	F17	P20	F10	F18
H15	P15	B3	G14	P21	F19	G11
H16	P16	B22	G17	V6	G8	G18
J11	R11	D1	H6	V7	G10	K6
J12	R12	D2	H7	V8	G19	K7
J15	R15	D25	H8	V19	L6	K8
J16	R16	D26	H19	V20	L7	K19
K11	T11	AA3	H20	V21	L8	K20
K12	T12	AB3	H21	W6	L19	K21
K15	T15	AB24	J6	W7	M19	L21
K16	T16	AC1	J7	W8	N19	R8
L11	U11	AC2	J8	W19	T19	R19
L12	U12	AC24	J19	W20	T20	R20
L15	U15	AD1	J20	W21	T21	R21
L16	U16	AD24	J21	Y10	U6	T6
M11	V11	AE4	N6	Y17	U7	T7
M12	V12	AE24	N7	AA10	U8	T8
M15	V15		N8	AA17	Y9	Y8
M16	V16		P8	—	Y13	Y19
N11	W11				Y18	AA8
N12	W12				AA9	AA11
N15	W15				AA13	AA12
N16	W16				AA18	AA19

Table 24 PES48H12G2 Power Pins

No Connection Pins

NC	
G16	N22
N20	P6
N21	P7

Table 25 PES48H12G2 No Connection Pins

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Ground Pins

V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}
A1	C19	G22	K24	N25	U1	W26	AD6
A2	C20	G23	K25	N26	U2	Y1	AD7
A4	C21	G24	K26	P1	U3	Y2	AD8
A7	C22	G25	L1	P2	U4	Y3	AD9
A10	D3	G26	L2	P3	U5	Y4	AD10
A13	D4	H1	L3	P4	U9	Y5	AD11
A16	D7	H2	L4	P5	U10	Y6	AD12
A19	D10	H3	L5	P9	U13	Y7	AD13
B1	D16	H4	L9	P10	U14	Y20	AD14
B2	D19	H5	L10	P13	U17	Y21	AD15
B4	D23	H9	L13	P14	U18	Y24	AD16
B7	D24	H10	L14	P17	U19	AA6	AD17
B10	E1	H13	L17	P18	U20	AA7	AD18
B13	E2	H14	L18	P24	U21	AA15	AD19
B16	E3	H17	L24	R3	U24	AA16	AD20
B19	E4	H18	M3	R9	V3	AA20	AD21
C1	E7	H24	M6	R10	V9	AA21	AD22
C2	E10	J3	M7	R13	V10	AA24	AD23
C3	E13	J9	M8	R14	V13	AB8	AE8
C4	E16	J10	M9	R17	V14	AB11	AE11
C5	E19	J13	M10	R18	V17	AB14	AE14
C6	E24	J14	M13	R24	V18	AB17	AE17
C7	F3	J17	M14	T3	V24	AB20	AE20
C8	F6	J18	M17	T9	W3	AB23	AE23
C9	F7	J24	M18	T10	W9	AB25	AF8
C10	F20	K3	M24	T13	W10	AB26	AF11
C11	F21	K9	N3	T14	W13	AC3	AF14
C12	F24	K10	N9	T17	W14	AC4	AF17
C13	G3	K13	N10	T18	W17	AC8	AF20
C14	G6	K14	N13	T22	W18	AC11	AF23
C15	G7	K17	N14	T23	W22	AC14	
C16	G12	K18	N17	T24	W23	AC17	
C17	G20	K22	N18	T25	W24	AC20	
C18	G21	K23	N24	T26	W25	AC23	

Table 26 PES48H12G2 Ground Pins

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Signals Listed Alphabetically

Signal Name	I/O Type	Location	Signal Category
CLKMODE0	I	AF1	System
CLKMODE1	I	A25	
CLKMODE2	I	AC5	
GCLKFSEL	I	AD4	
GCLKN0	I	G13	
GCLKN1	I	Y14	
GCLKP0	I	F13	
GCLKP1	I	AA14	
GPIO_00	I/O	AF25	General Purpose I/O
GPIO_01	I/O	AF24	
GPIO_02	I/O	AE25	
GPIO_03	I/O	AF26	
GPIO_04	I/O	AC25	
GPIO_05	I/O	AD25	
GPIO_06	I/O	AD26	
GPIO_07	I/O	AE26	
GPIO_08	I/O	AC26	
JTAG_TCK	I	A26	Test
JTAG_TDI	I	C24	
JTAG_TDO	O	C23	
JTAG_TMS	I	A24	
JTAG_TRST_N	I	D22	
MSMBCLK	I/O	B23	SMBus Interface
MSMBDAT	I/O	A23	
NO CONNECT	See Table 25 for a listing of No Connect pins.		
P00CLKN	I	M20	PCI Express
P00CLKP	I	M21	
P02CLKN	I	G15	
P02CLKP	I	F15	

Table 27 PES48H12G2 Alphabetical Signal List (Part 1 of 8)

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Signal Name	I/O Type	Location	Signal Category
P01MERGEN	I	AE1	System
P23MERGEN	I	AD2	
P45MERGEN	I	AF2	
P67MERGEN	I	AE2	
P89MERGEN	I	AE3	
P1213MERGEN	I	AD3	
PE00RN0	I	R23	PCI Express
PE00RN1	I	P23	
PE00RN2	I	M23	
PE00RN3	I	L23	
PE00RP0	I	R22	
PE00RP1	I	P22	
PE00RP2	I	M22	
PE00RP3	I	L22	
PE00TN0	O	R25	
PE00TN1	O	P25	
PE00TN2	O	M25	
PE00TN3	O	L25	
PE00TP0	O	R26	
PE00TP1	O	P26	
PE00TP2	O	M26	
PE00TP3	O	L26	
PE01RN0	I	J23	
PE01RN1	I	H23	
PE01RN2	I	F23	
PE01RN3	I	E23	
PE01RP0	I	J22	
PE01RP1	I	H22	
PE01RP2	I	F22	
PE01RP3	I	E22	
PE01TN0	O	J25	
PE01TN1	O	H25	
PE01TN2	O	F25	
PE01TN3	O	E25	
PE01TP0	O	J26	
PE01TP1	O	H26	

Table 27 PES48H12G2 Alphabetical Signal List (Part 2 of 8)

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Signal Name	I/O Type	Location	Signal Category
PE01TP2	O	F26	PCI Express (cont.)
PE01TP3	O	E26	
PE02RN0	I	D21	
PE02RN1	I	D20	
PE02RN2	I	D18	
PE02RN3	I	D17	
PE02RP0	I	E21	
PE02RP1	I	E20	
PE02RP2	I	E18	
PE02RP3	I	E17	
PE02TN0	O	B21	
PE02TN1	O	B20	
PE02TN2	O	B18	
PE02TN3	O	B17	
PE02TP0	O	A21	
PE02TP1	O	A20	
PE02TP2	O	A18	
PE02TP3	O	A17	
PE03RN0	I	D15	
PE03RN1	I	D14	
PE03RN2	I	D12	
PE03RN3	I	D11	
PE03RP0	I	E15	
PE03RP1	I	E14	
PE03RP2	I	E12	
PE03RP3	I	E11	
PE03TN0	O	B15	
PE03TN1	O	B14	
PE03TN2	O	B12	
PE03TN3	O	B11	
PE03TP0	O	A15	
PE03TP1	O	A14	
PE03TP2	O	A12	
PE03TP3	O	A11	
PE04RN0	I	M4	
PE04RN1	I	N4	

Table 27 PES48H12G2 Alphabetical Signal List (Part 3 of 8)

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Signal Name	I/O Type	Location	Signal Category
PE04RN2	I	R4	PCI Express (cont.)
PE04RN3	I	T4	
PE04RP0	I	M5	
PE04RP1	I	N5	
PE04RP2	I	R5	
PE04RP3	I	T5	
PE04TN0	O	M2	
PE04TN1	O	N2	
PE04TN2	O	R2	
PE04TN3	O	T2	
PE04TP0	O	M1	
PE04TP1	O	N1	
PE04TP2	O	R1	
PE04TP3	O	T1	
PE05RN0	I	V4	
PE05RN1	I	W4	
PE05RN2	I	AA4	
PE05RN3	I	AB4	
PE05RP0	I	V5	
PE05RP1	I	W5	
PE05RP2	I	AA5	
PE05RP3	I	AB5	
PE05TN0	O	V2	
PE05TN1	O	W2	
PE05TN2	O	AA2	
PE05TN3	O	AB2	
PE05TP0	O	V1	
PE05TP1	O	W1	
PE05TP2	O	AA1	
PE05TP3	O	AB1	
PE06RN0	I	AC6	
PE06RN1	I	AC7	
PE06RN2	I	AC9	
PE06RN3	I	AC10	
PE06RP0	I	AB6	
PE06RP1	I	AB7	

Table 27 PES48H12G2 Alphabetical Signal List (Part 4 of 8)

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Signal Name	I/O Type	Location	Signal Category
PE06RP2	I	AB9	PCI Express (cont.)
PE06RP3	I	AB10	
PE06TN0	O	AE6	
PE06TN1	O	AE7	
PE06TN2	O	AE9	
PE06TN3	O	AE10	
PE06TP0	O	AF6	
PE06TP1	O	AF7	
PE06TP2	O	AF9	
PE06TP3	O	AF10	
PE07RN0	I	AC12	
PE07RN1	I	AC13	
PE07RN2	I	AC15	
PE07RN3	I	AC16	
PE07RP0	I	AB12	
PE07RP1	I	AB13	
PE07RP2	I	AB15	
PE07RP3	I	AB16	
PE07TN0	O	AE12	
PE07TN1	O	AE13	
PE07TN2	O	AE15	
PE07TN3	O	AE16	
PE07TP0	O	AF12	
PE07TP1	O	AF13	
PE07TP2	O	AF15	
PE07TP3	O	AF16	
PE08RN0	I	D9	
PE08RN1	I	D8	
PE08RN2	I	D6	
PE08RN3	I	D5	
PE08RP0	I	E9	
PE08RP1	I	E8	
PE08RP2	I	E6	
PE08RP3	I	E5	
PE08TN0	O	B9	
PE08TN1	O	B8	

Table 27 PES48H12G2 Alphabetical Signal List (Part 5 of 8)

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Signal Name	I/O Type	Location	Signal Category
PE08TN2	O	B6	PCI Express (cont.)
PE08TN3	O	B5	
PE08TP0	O	A9	
PE08TP1	O	A8	
PE08TP2	O	A6	
PE08TP3	O	A5	
PE09RN0	I	F4	
PE09RN1	I	G4	
PE09RN2	I	J4	
PE09RN3	I	K4	
PE09RP0	I	F5	
PE09RP1	I	G5	
PE09RP2	I	J5	
PE09RP3	I	K5	
PE09TN0	O	F2	
PE09TN1	O	G2	
PE09TN2	O	J2	
PE09TN3	O	K2	
PE09TP0	O	F1	
PE09TP1	O	G1	
PE09TP2	O	J1	
PE09TP3	O	K1	
PE12RN0	I	AC18	
PE12RN1	I	AC19	
PE12RN2	I	AC21	
PE12RN3	I	AC22	
PE12RP0	I	AB18	
PE12RP1	I	AB19	
PE12RP2	I	AB21	
PE12RP3	I	AB22	
PE12TN0	O	AE18	
PE12TN1	O	AE19	
PE12TN2	O	AE21	
PE12TN3	O	AE22	
PE12TP0	O	AF18	
PE12TP1	O	AF19	

Table 27 PES48H12G2 Alphabetical Signal List (Part 6 of 8)

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Signal Name	I/O Type	Location	Signal Category
PE12TP2	O	AF21	PCI Express (cont.)
PE12TP3	O	AF22	
PE13RN0	I	AA23	
PE13RN1	I	Y23	
PE13RN2	I	V23	
PE13RN3	I	U23	
PE13RP0	I	AA22	
PE13RP1	I	Y22	
PE13RP2	I	V22	
PE13RP3	I	U22	
PE13TN0	O	AA25	
PE13TN1	O	Y25	
PE13TN2	O	V25	
PE13TN3	O	U25	
PE13TP0	O	AA26	
PE13TP1	O	Y26	
PE13TP2	O	V26	
PE13TP3	O	U26	
PERSTN	I	B24	System
REFRES00	I/O	N23	SerDes Reference Resistors
REFRES01	I/O	L20	
REFRES02	I/O	F16	
REFRES03	I/O	D13	
REFRES04	I/O	R7	
REFRES05	I/O	R6	
REFRES06	I/O	Y11	
REFRES07	I/O	Y12	
REFRES08	I/O	F9	
REFRES09	I/O	G9	
REFRES12	I/O	Y15	
REFRES13	I/O	Y16	
REFRESPLL	I/O	F12	
RSTHALT	I	AF3	System

Table 27 PES48H12G2 Alphabetical Signal List (Part 7 of 8)

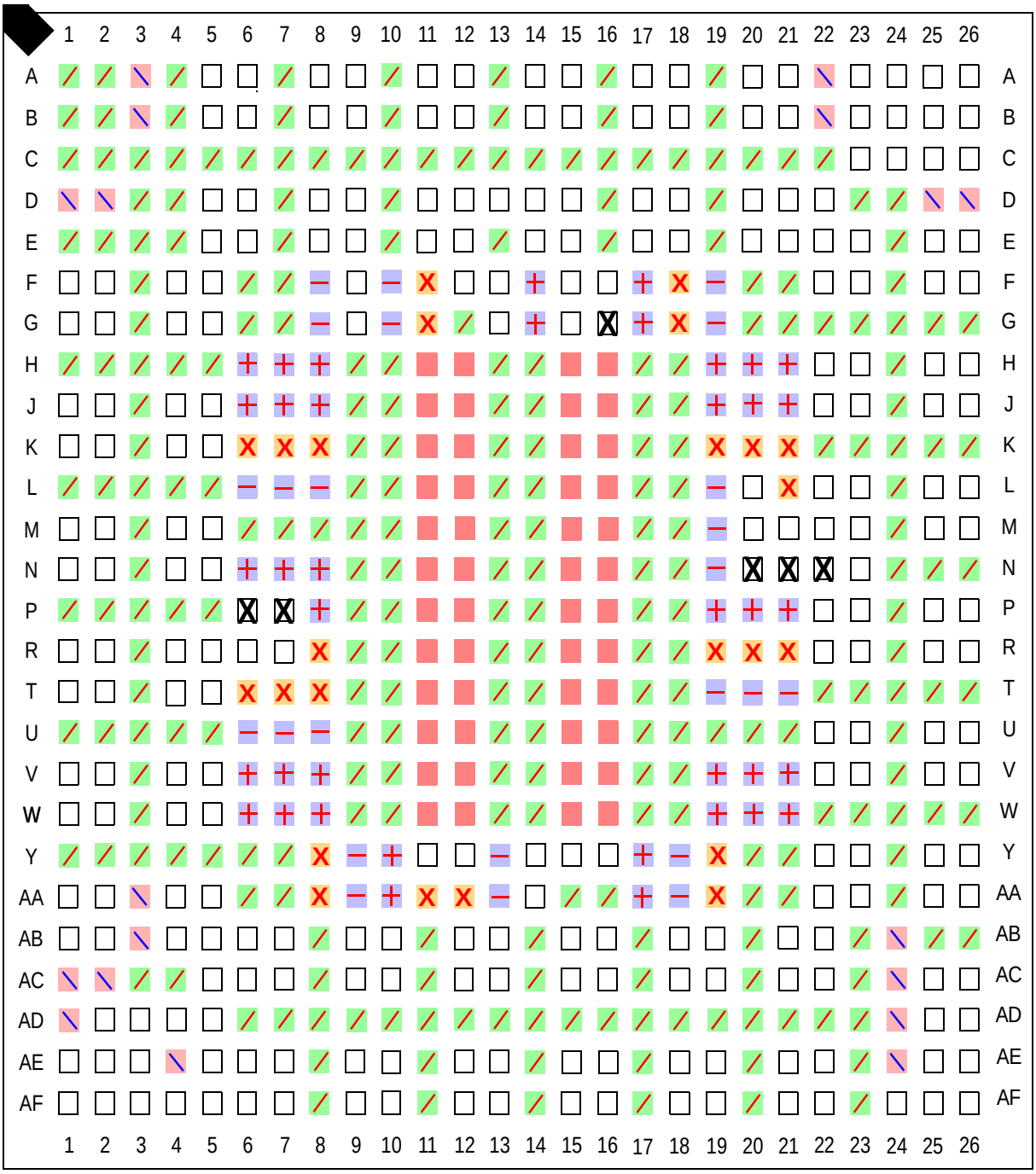
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Signal Name	I/O Type	Location	Signal Category
SSMBADDR1	I	C26	SMBus Interface
SSMBADDR2	I	B26	
SSMBCLK	I/O	C25	
SSMBDAT	I/O	B25	
SWMODE0	I	AD5	System
SWMODE1	I	AE5	
SWMODE2	I	AF4	
SWMODE3	I	AF5	
V_{DD}CORE, V_{DD}I/O, V_{DD}PEA, V_{DD}PEHA, V_{DD}PETA	See Table 24 for a listing of power pins.		
V_{SS}	See Table 26 for a listing of ground pins.		

Table 27 PES48H12G2 Alphabetical Signal List (Part 8 of 8)

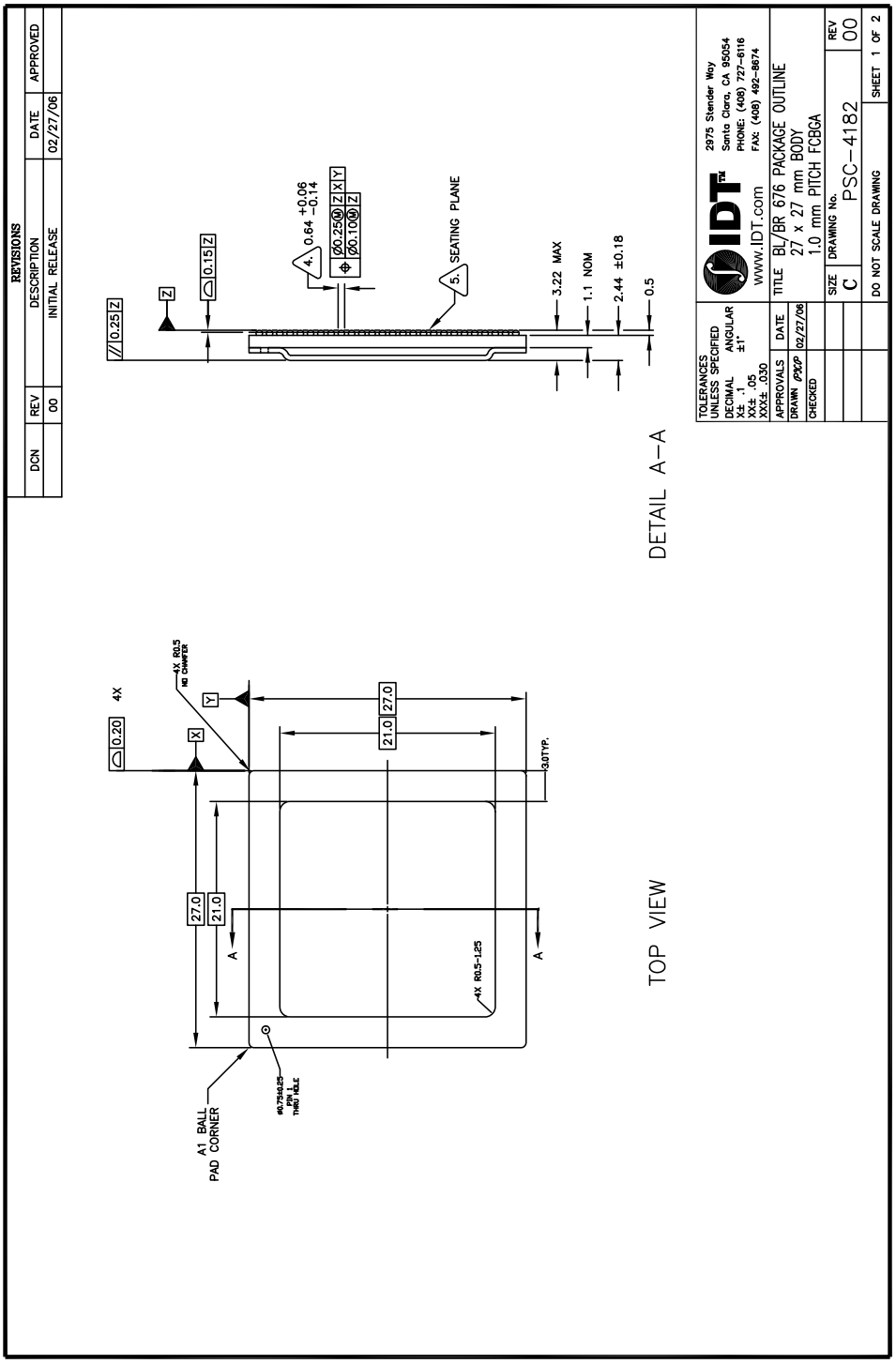
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PES48H12G2 Pinout — Top View



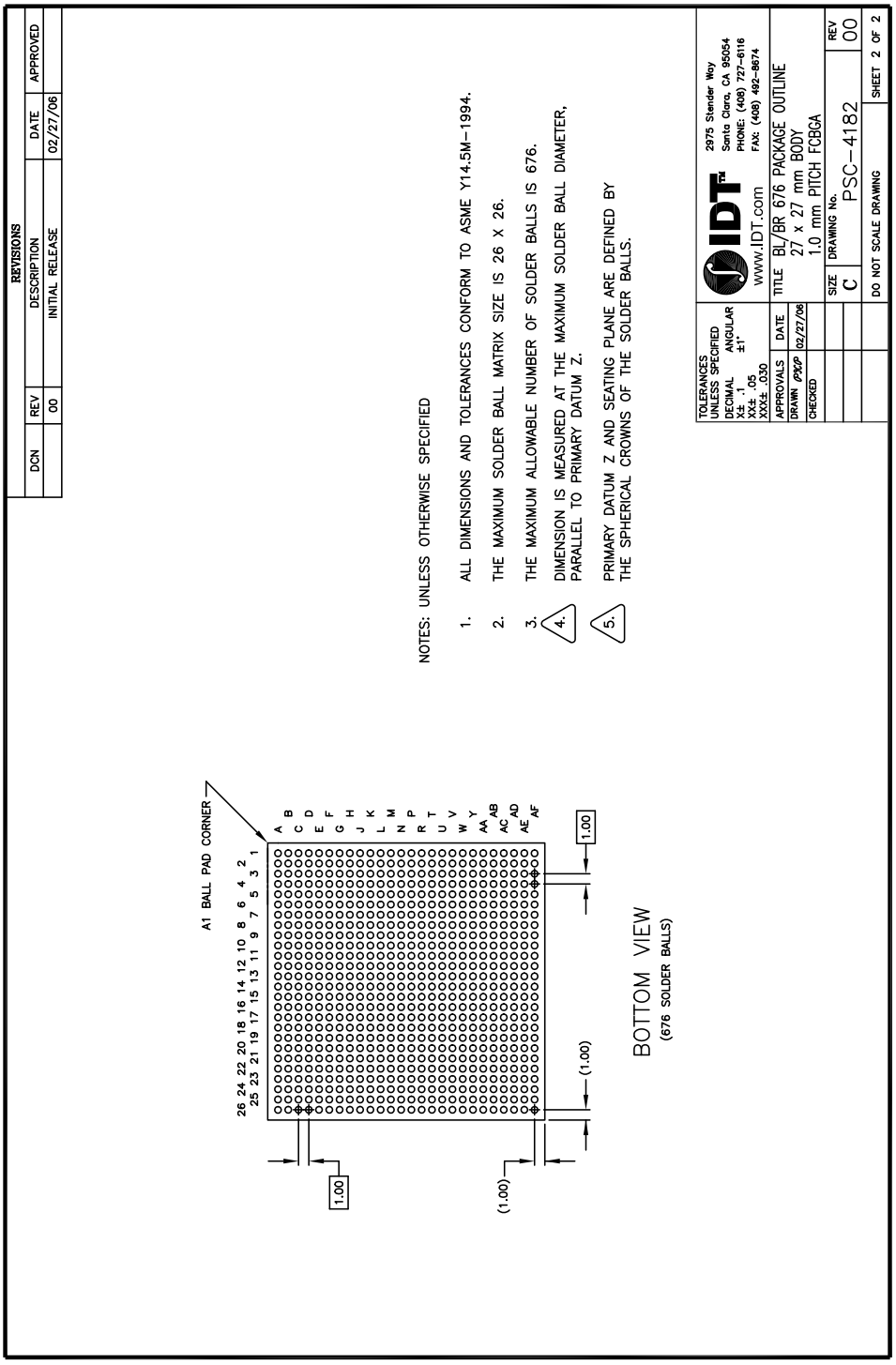
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PES48H12G2 Package Drawing — 676-Pin BL676/BLG676



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Option A Package Drawing — Page Two



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Revision History

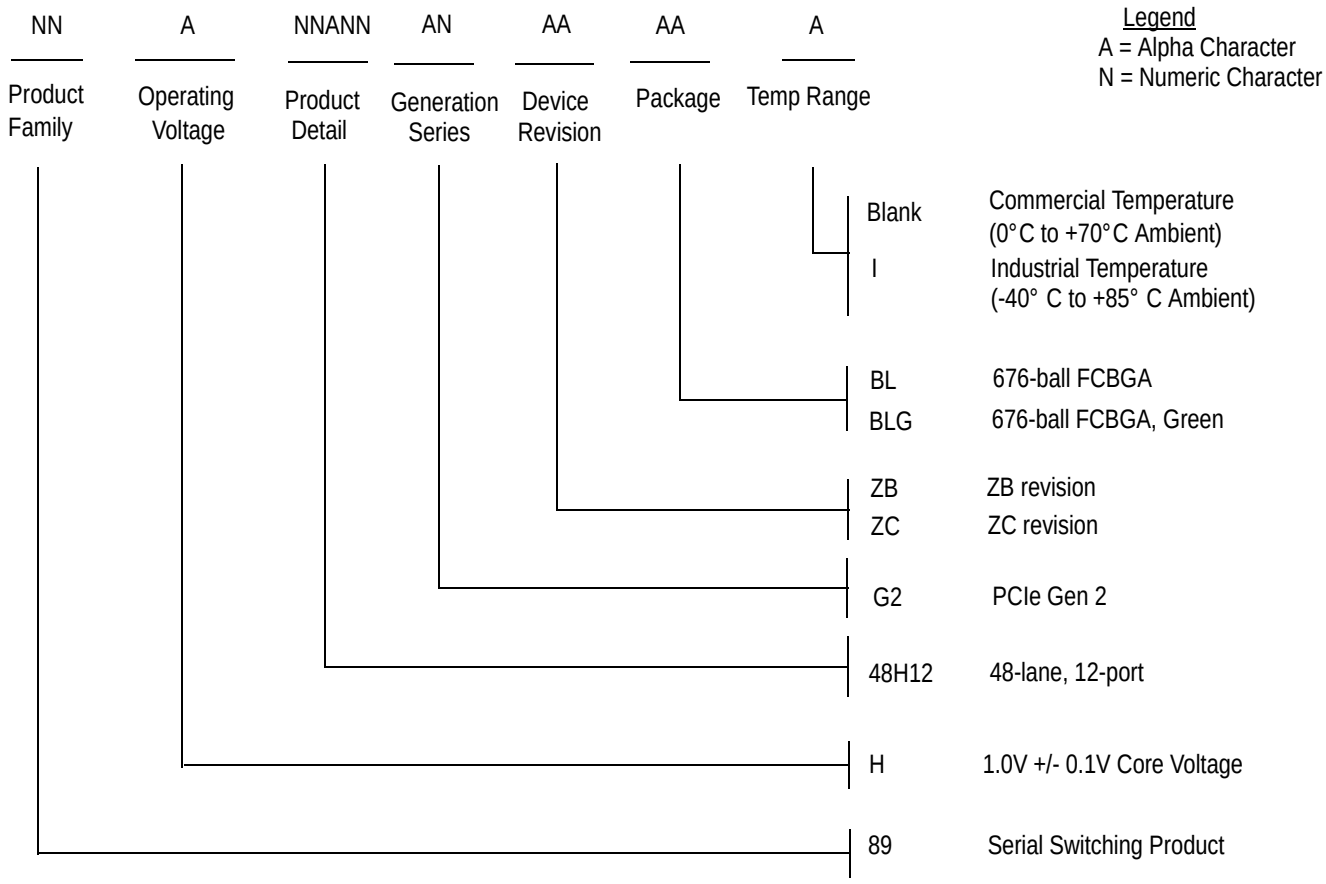
January 21, 2010: Publication of Final data sheet.

March 30, 2011: In Table 13, added V_{DD}PETA to footnote #1.

November 28, 2011: Added new Tables 20 and 21, SMBus Characterization and Timing.

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Ordering Information



Valid Combinations

89H48H12G2ZBBL	676-ball FCBGA package, Commercial Temperature
89H48H12G2ZBBLG	676-ball Green FCBGA package, Commercial Temperature
89H48H12G2ZBBLI	676-ball FCBGA package, Industrial Temperature
89H48H12G2ZBBLGI	676-ball Green FCBGA package, Industrial Temperature
89H48H12G2ZCBL	676-ball FCBGA package, Commercial Temperature
89H48H12G2ZCBLG	676-ball Green FCBGA package, Commercial Temperature
89H48H12G2ZCBLI	676-ball FCBGA package, Industrial Temperature
89H48H12G2ZCBLGI	676-ball Green FCBGA package, Industrial Temperature

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