Device Overview

The 89HPES64H16G2 is a member of the IDT PRECISE™ family of PCI Express® switching solutions. The PES64H16G2 is a 64-lane, 16-port system interconnect switch optimized for PCI Express Gen2 packet switching in high-performance applications, supporting multiple simultaneous peer-to-peer traffic flows. Target applications include servers, storage, communications, embedded systems, and multi-host or intelligent I/O based systems with inter-domain communication.

Features

- **High Performance Non-Blocking Switch Architecture**
  - 64-lane 16-port PCIe switch
    - *Eight x8 ports switch ports each of which can bifurcate to two x4 ports (total of sixteen x4 ports)*
  - Integrated SerDes supports 5.0 GT/s Gen2 and 2.5 GT/s Gen1 operation
  - Delivers up to 64 GBps (512 Gbps) of switching capacity
  - Supports 128 Bytes to 2 KB maximum payload size
  - Low latency cut-through architecture
  - Supports one virtual channel and eight traffic classes
- **Standards and Compatibility**
  - PCI Express Base Specification 2.0 compliant
  - Implements the following optional PCI Express features
    - *Advanced Error Reporting (AER) on all ports*
    - *End-to-End CRC (ECRC)*
    - *Access Control Services (ACS)*
    - *Power Budgeting Enhanced Capability*
    - *Device Serial Number Enhanced Capability*
    - *Sub-System ID and Sub-System Vendor ID Capability*
    - *Internal Error Reporting ECN*
    - *Multicast ECN*
    - *VGA and ISA enable*
    - *L0s and L1 ASPM*
    - *ARI ECN*
  - Compatible with IDT 89HPES64H16 PCIe Gen1 switch
- **Port Configurability**
  - x4 and x8 ports
    - *Ability to merge adjacent x4 ports to create a x8 port*
  - Automatic per port link width negotiation (x8 → x4 → x2 → x1)
  - Crosslink support
  - Automatic lane reversal
  - Autonomous and software managed link width and speed control
  - Per lane SerDes configuration
    - *De-emphasis*
    - *Receive equalization*
    - *Drive strength*
- **Switch Partitioning**
  - IDT proprietary feature that creates logically independent switches in the device
  - Supports up to 16 fully independent switch partitions
  - Configurable downstream port device numbering
  - Supports dynamic reconfiguration of switch partitions
    - *Dynamic port reconfiguration — downstream, upstream*
    - *Dynamic migration of ports between partitions*
    - *Movable upstream port within and between switch partitions*
- **Initialization / Configuration**
  - Supports Root (BIOS, OS, or driver), Serial EEPROM, or SMBus switch initialization
  - Common switch configurations are supported with pin strapping (no external components)
  - Supports in-system Serial EEPROM initialization/programming
- **Quality of Service (QoS)**
  - Port arbitration
    - *Round robin*
  - Request metering
    - *IDT proprietary feature that balances bandwidth among switch ports for maximum system throughput*
  - High performance switch core architecture
    - *Combined Input Output Queued (CIOQ) switch architecture with large buffers*
- **Multicast**
  - Compliant to the PCI-SIG multicast ECN
  - Supports arbitrary multicasting of Posted transactions
  - Supports 64 multicast groups
  - Independent multicast support within each switch partition
- **Clocking**
  - Supports 100 MHz and 125 MHz reference clock frequencies
  - Flexible clocking modes
    - *Common clock*
    - *Non-common clock*
- **Hot-Plug and Hot Swap**
  - Hot-plug controller on all ports
    - *Hot-plug supported on all downstream switch ports*

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- All ports support hot-plug using low-cost external I^2C I/O expanders
- Configurable presence detect supports card and cable applications
- GPE output pin for hot-plug event notification
  - *Enables SCI/SMI generation for legacy operating system support*
- Hot-swap capable I/O

◆ **Power Management**

- Supports D0, D3hot and D3 power management states
- Active State Power Management (ASPM)
  - *Supports L0, L0s, L1, L2/L3 Ready and L3 link states*
  - *Configurable L0s and L1 entry timers allow performance/ power-savings tuning*
- Supports PCI Express Power Budgeting Capability
- SerDes power savings
  - *Supports low swing / half-swing SerDes operation*
  - *SerDes optionally turned-off in D3hot*
  - *SerDes associated with unused ports are turned-off*
  - *SerDes associated with unused lanes are placed in a low power state*

◆ **32 General Purpose I/O**

◆ **Reliability, Availability and Serviceability (RAS)**

- ECRC support
- AER on all ports
- SECDED ECC protection on all internal RAMs
- End-to-end data path parity protection
- Checksum Serial EEPROM content protected
- Autonomous link reliability (preserves system operation in the presence of faulty links)
- Ability to generate an interrupt (INTx or MSI) on link up/down transitions

◆ **Test and Debug**

- On-chip link activity and status outputs available for Port 0 (upstream port)
- Per port link activity and status outputs available using external I^2C I/O expander for all other ports
- SerDes test modes
- Supports IEEE 1149.6 AC JTAG and IEEE 1149.1 JTAG

◆ **Power Supplies**

- Requires only two power supply voltages (1.0 V and 2.5 V) Note that a 3.3V is preferred for V_{DD}I/O
- No power sequencing requirements

◆ **Packaged in a 35mm x 35mm 1156-ball Flip Chip BGA with 1mm ball spacing**

- Compatible with IDT 89HPES64H16 PCIe Gen1 switch

Note: For pin compatibility issues, contact the IDT help desk at ssdhelp@idt.com.

Product Description

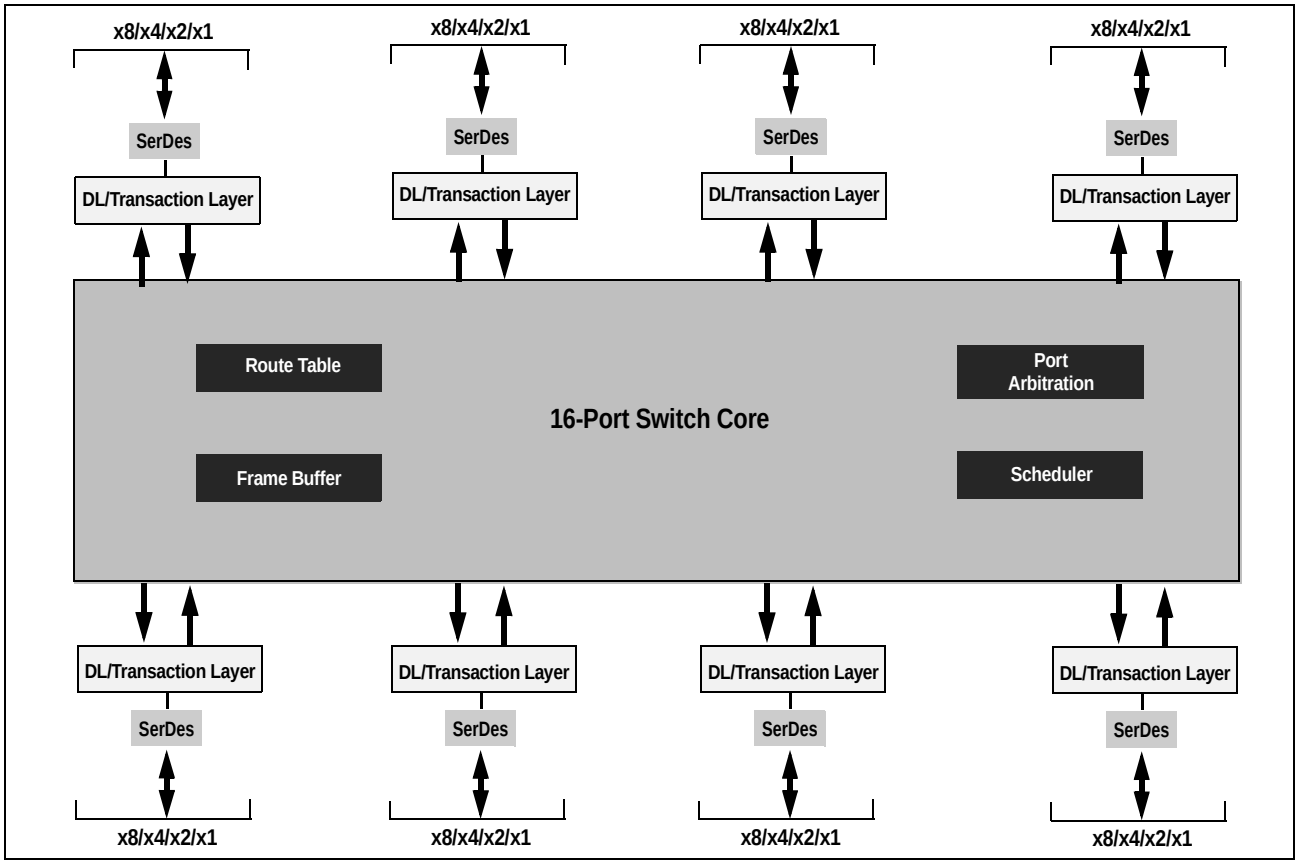
Utilizing standard PCI Express interconnect, the PES64H16G2 provides the most efficient fan-out solution for applications requiring high throughput, low latency, and simple board layout with a minimum number of board layers. It provides 64 GBps (512 Gbps) of aggregated, full-duplex switching capacity through 64 integrated serial lanes, using proven and robust IDT technology. Each lane provides 5 GT/s of bandwidth in both directions and is fully compliant with PCI Express Base Specification, Revision 2.0.

The PES64H16G2 is based on a flexible and efficient layered architecture. The PCI Express layer consists of SerDes, Physical, Data Link and Transaction layers in compliance with PCI Express Base specification Revision 2.0. The PES64H16G2 can operate either as a store and forward or cut-through switch. It supports eight Traffic Classes (TCs) and one Virtual Channel (VC) with sophisticated resource management to enable efficient switching and I/O connectivity for servers, storage, and embedded processors with limited connectivity.

The PES64H16G2 is a *partitionable* PCIe switch. This means that in addition to operating as a standard PCI express switch, the PES64H16G2 ports may be partitioned into groups that logically operate as completely independent PCIe switches. Figure 2 illustrates a three partition PES64H16G2 configuration.

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Block Diagram



64 PCI Express Lanes
Up to 8 x8 ports or 16 x4 Ports

Figure 1 Internal Block Diagram

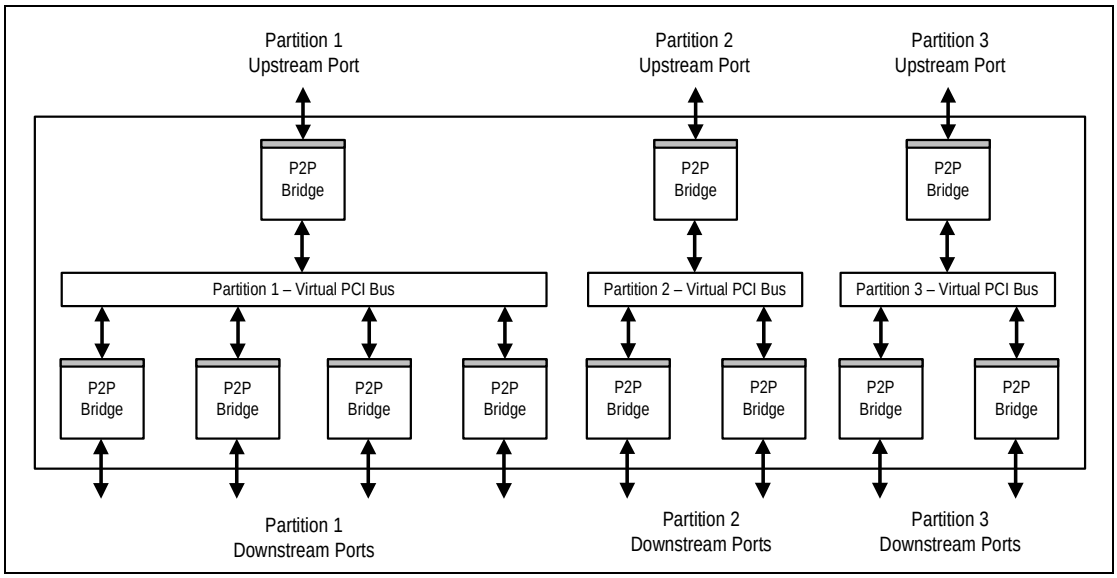


Figure 2 Example of Usage of Switch Partitioning

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SMBus Interface

The PES64H16G2 contains two SMBus interfaces. The slave interface provides full access to the configuration registers in the PES64H16G2, allowing every configuration register in the device to be read or written by an external agent. The master interface allows the default configuration register values of the PES64H16G2 to be overridden following a reset with values programmed in an external serial EEPROM. The master interface is also used by an external Hot-Plug I/O expander.

Six pins make up each of the two SMBus interfaces. These pins consist of an SMBus clock pin, an SMBus data pin, and 4 SMBus address pins. In the slave interface, these address pins allow the SMBus address to which the device responds to be configured. In the master interface, these address pins allow the SMBus address of the serial configuration EEPROM from which data is loaded to be configured. The SMBus address is set up on negation of PERSTN by sampling the corresponding address pins. When the pins are sampled, the resulting address is assigned as shown in Table 1.

Bit	Slave SMBus Address	Master SMBus Address
1	SSMBADDR[1]	MSMBADDR[1]
2	SSMBADDR[2]	MSMBADDR[2]
3	SSMBADDR[3]	MSMBADDR[3]
4	0	MSMBADDR[4]
5	SSMBADDR[5]	1
6	1	0
7	1	1

Table 1 Master and Slave SMBus Address Assignment

As shown in Figure 3, the master and slave SMBuses may only be used in a split configuration.

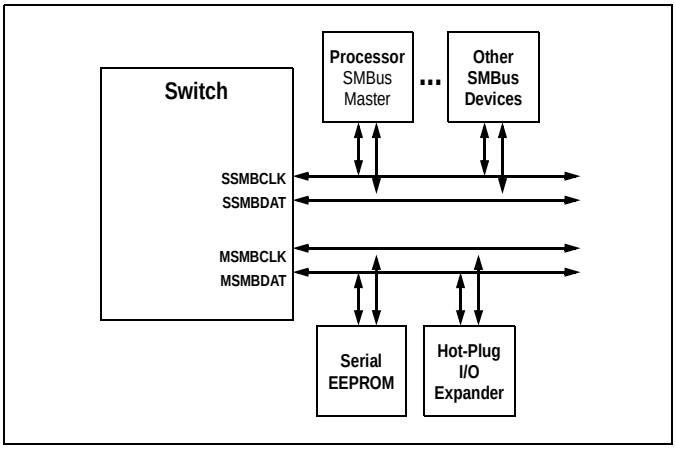


Figure 3 Split SMBus Interface Configuration

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The switch's SMBus master interface does not support SMBus arbitration. As a result, the switch's SMBus master must be the only master in the SMBus lines that connect to the serial EEPROM and I/O expander slaves. In the split configuration, the master and slave SMBuses operate as two independent buses; thus, multi-master arbitration is not required.

Hot-Plug Interface

The PES64H16G2 supports PCI Express Hot-Plug on each downstream port. To reduce the number of pins required on the device, the PES64H16G2 utilizes an external I/O expander, such as that used on PC motherboards, connected to the SMBus master interface. Following reset and configuration, whenever the state of a Hot-Plug output needs to be modified, the PES64H16G2 generates an SMBus transaction to the I/O expander with the new value of all of the outputs. Whenever a Hot-Plug input changes, the I/O expander generates an interrupt which is received on the IOEXPINTN input pin (alternate function of GPIO) of the PES64H16G2. In response to an I/O expander interrupt, the PES64H16G2 generates an SMBus transaction to read the state of all of the Hot-Plug inputs from the I/O expander.

General Purpose Input/Output

The PES64H16G2 provides 32 General Purpose Input/Output (GPIO) pins that may be used by the system designer as bit I/O ports. Each GPIO pin may be configured independently as an input or output through software control. Some GPIO pins are shared with other on-chip functions. These alternate functions may be enabled via software, SMBus slave interface, or serial configuration EEPROM.

Pin Description

The following tables list the functions of the pins provided on the PES64H16G2. Some of the functions listed may be multiplexed onto the same pin. The active polarity of a signal is defined using a suffix. Signals ending with an "N" are defined as being active, or asserted, when at a logic zero (low) level. All other signals (including clocks, buses, and select lines) will be interpreted as being active, or asserted, when at a logic one (high) level.

Signal	Type	Name/Description
PE00RP[3:0] PE00RN[3:0]	I	**PCI Express Port 0 Serial Data Receive.** Differential PCI Express receive pairs for port 0.
PE00TP[3:0] PE00TN[3:0]	O	**PCI Express Port 0 Serial Data Transmit.** Differential PCI Express transmit pairs for port 0.
PE01RP[3:0] PE01RN[3:0]	I	**PCI Express Port 1 Serial Data Receive.** Differential PCI Express receive pairs for port 1. When port 0 is merged with port 1, these signals become port 0 receive pairs for lanes 4 through 7.
PE01TP[3:0] PE01TN[3:0]	O	**PCI Express Port 1 Serial Data Transmit.** Differential PCI Express transmit pairs for port 1. When port 0 is merged with port 1, these signals become port 0 transmit pairs for lanes 4 through 7.
PE02RP[3:0] PE02RN[3:0]	I	**PCI Express Port 2 Serial Data Receive.** Differential PCI Express receive pairs for port 2.
PE02TP[3:0] PE02TN[3:0]	O	**PCI Express Port 2 Serial Data Transmit.** Differential PCI Express transmit pairs for port 2.
PE03RP[3:0] PE03RN[3:0]	I	**PCI Express Port 3 Serial Data Receive.** Differential PCI Express receive pairs for port 3. When port 2 is merged with port 3, these signals become port 2 receive pairs for lanes 4 through 7.
PE03TP[3:0] PE03TN[3:0]	O	**PCI Express Port 3 Serial Data Transmit.** Differential PCI Express transmit pairs for port 3. When port 2 is merged with port 3, these signals become port 2 transmit pairs for lanes 4 through 7.
PE04RP[3:0] PE04RN[3:0]	I	**PCI Express Port 4 Serial Data Receive.** Differential PCI Express receive pairs for port 4.
PE04TP[3:0] PE04TN[3:0]	O	**PCI Express Port 4 Serial Data Transmit.** Differential PCI Express transmit pairs for port 4.

Table 2 PCI Express Interface Pins (Part 1 of 3)

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Signal	Type	Name/Description
PE05RP[3:0] PE05RN[3:0]	I	**PCI Express Port 5 Serial Data Receive.** Differential PCI Express receive pairs for port 5. When port 4 is merged with port 5, these signals become port 4 receive pairs for lanes 4 through 7.
PE05TP[3:0] PE05TN[3:0]	O	**PCI Express Port 5 Serial Data Transmit.** Differential PCI Express transmit pairs for port 5. When port 4 is merged with port 5, these signals become port 4 transmit pairs for lanes 4 through 7.
PE06RP[3:0] PE06RN[3:0]	I	**PCI Express Port 6 Serial Data Receive.** Differential PCI Express receive pairs for port 6.
PE06TP[3:0] PE06TN[3:0]	O	**PCI Express Port 6 Serial Data Transmit.** Differential PCI Express transmit pairs for port 6.
PE07RP[3:0] PE07RN[3:0]	I	**PCI Express Port 7 Serial Data Receive.** Differential PCI Express receive pairs for port 7. When port 6 is merged with port 7, these signals become port 6 receive pairs for lanes 4 through 7.
PE07TP[3:0] PE07TN[3:0]	O	**PCI Express Port 7 Serial Data Transmit.** Differential PCI Express transmit pairs for port 7. When port 6 is merged with port 7, these signals become port 6 transmit pairs for lanes 4 through 7.
PE08RP[3:0] PE08RN[3:0]	I	**PCI Express Port 8 Serial Data Receive.** Differential PCI Express receive pairs for port 8.
PE08TP[3:0] PE08TN[3:0]	O	**PCI Express Port 8 Serial Data Transmit.** Differential PCI Express transmit pairs for port 8.
PE09RP[3:0] PE09RN[3:0]	I	**PCI Express Port 9 Serial Data Receive.** Differential PCI Express receive pairs for port 9. When port 8 is merged with port 9, these signals become port 8 receive pairs for lanes 4 through 7.
PE09TP[3:0] PE09TN[3:0]	O	**PCI Express Port 9 Serial Data Transmit.** Differential PCI Express transmit pairs for port 9. When port 8 is merged with port 9, these signals become port 8 transmit pairs for lanes 4 through 7.
PE10RP[3:0] PE10RN[3:0]	I	**PCI Express Port 10 Serial Data Receive.** Differential PCI Express receive pairs for port 10.
PE10TP[3:0] PE10TN[3:0]	O	**PCI Express Port 10 Serial Data Transmit.** Differential PCI Express transmit pairs for port 10.
PE11RP[3:0] PE11RN[3:0]	I	**PCI Express Port 11 Serial Data Receive.** Differential PCI Express receive pairs for port 11. When port 10 is merged with port 11, these signals become port 10 receive pairs for lanes 4 through 7.
PE11TP[3:0] PE11TN[3:0]	O	**PCI Express Port 11 Serial Data Transmit.** Differential PCI Express transmit pairs for port 11. When port 10 is merged with port 11, these signals become port 10 transmit pairs for lanes 4 through 7.
PE12RP[3:0] PE12RN[3:0]	I	**PCI Express Port 12 Serial Data Receive.** Differential PCI Express receive pairs for port 12.
PE12TP[3:0] PE12TN[3:0]	O	**PCI Express Port 12 Serial Data Transmit.** Differential PCI Express transmit pairs for port 12.
PE13RP[3:0] PE13RN[3:0]	I	**PCI Express Port 13 Serial Data Receive.** Differential PCI Express receive pairs for port 13. When port 12 is merged with port 13, these signals become port 12 receive pairs for lanes 4 through 7.
PE13TP[3:0] PE13TN[3:0]	O	**PCI Express Port 13 Serial Data Transmit.** Differential PCI Express transmit pairs for port 13. When port 12 is merged with port 13, these signals become port 12 transmit pairs for lanes 4 through 7.

Table 2 PCI Express Interface Pins (Part 2 of 3)

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Signal	Type	Name/Description
PE14RP[3:0] PE14RN[3:0]	I	**PCI Express Port 14 Serial Data Receive.** Differential PCI Express receive pairs for port 14.
PE14TP[3:0] PE14TN[3:0]	O	**PCI Express Port 14 Serial Data Transmit.** Differential PCI Express transmit pairs for port 14.
PE15RP[3:0] PE15RN[3:0]	I	**PCI Express Port 15 Serial Data Receive.** Differential PCI Express receive pairs for port 15. When port 14 is merged with port 15, these signals become port 14 receive pairs for lanes 4 through 7.
PE15TP[3:0] PE15TN[3:0]	O	**PCI Express Port 15 Serial Data Transmit.** Differential PCI Express transmit pairs for port 15. When port 14 is merged with port 15, these signals become port 14 transmit pairs for lanes 4 through 7.

Table 2 PCI Express Interface Pins (Part 3 of 3)

Signal	Type	Name/Description
GCLKN[1:0] GCLKP[1:0]	I	**Global Reference Clock.** Differential reference clock input pair. This clock is used as the reference clock by on-chip PLLs to generate the clocks required for the system logic. The frequency of the differential reference clock is determined by the GCLKFSEL signal.

Table 3 Reference Clock Pins

Signal	Type	Name/Description
MSMBADDR[4:1]	I	**Master SMBus Address.** These pins determine the SMBus address of the serial EEPROM from which configuration information is loaded.
MSMBCLK	I/O	**Master SMBus Clock.** This bidirectional signal is used to synchronize transfers on the master SMBus.
MSMBDAT	I/O	**Master SMBus Data.** This bidirectional signal is used for data on the master SMBus.
SSMBADDR[5,3:1]	I	**Slave SMBus Address.** These pins determine the SMBus address to which the slave SMBus interface responds.
SSMBCLK	I/O	**Slave SMBus Clock.** This bidirectional signal is used to synchronize transfers on the slave SMBus.
SSMBDAT	I/O	**Slave SMBus Data.** This bidirectional signal is used for data on the slave SMBus.

Table 4 SMBus Interface Pins

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Signal	Type	Name/Description
GPIO[0]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: PART0PERSTN Alternate function pin type: Input/Output Alternate function: Assertion of this signal initiated a partition fundamental reset in the corresponding partition.
GPIO[1]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: PART1PERSTN Alternate function pin type: Input/Output Alternate function: Assertion of this signal initiated a partition fundamental reset in the corresponding partition.
GPIO[2]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: PART2PERSTN Alternate function pin type: Input/Output Alternate function: Assertion of this signal initiated a partition fundamental reset in the corresponding partition.
GPIO[3]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: PART3PERSTN Alternate function pin type: Input/Output Alternate function: Assertion of this signal initiated a partition fundamental reset in the corresponding partition.
GPIO[4]	I	General Purpose I/O. This pin can be configured as a general purpose I/O pin. 1st Alternate function — Reserved 2nd Alternate function pin name: P0LINKUPN 2nd Alternate function pin type: Output 2nd Alternate function: Port 0 Link Up Status output.
GPIO[5]	O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. 1st Alternate function pin name: GPEN 1st Alternate function pin type: Output 1st Alternate function: Hot-plug general purpose even output. 2nd Alternate function pin name: P0ACTIVEN 2nd Alternate function pin type: Output 2nd Alternate function: Port 0 Link Active Status Output.
GPIO[6]	I	General Purpose I/O. This pin can be configured as a general purpose I/O pin.
GPIO[7]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin.
GPIO[8]	I	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: IOEXPINTN Alternate function pin type: Input Alternate function: IO expander interrupt.
GPIO[9]	I	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: HP0APN Alternate function pin type: Input Alternate function: Hot Plug Signal Group 0 Attention Push Button Input.

Table 5 General Purpose I/O Pins (Part 1 of 4)

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Signal	Type	Name/Description
GPIO[10]	I	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: HP0PDN Alternate function pin type: Input Alternate function: Hot Plug Signal Group 0 Presence Detect Input.
GPIO[11]	I	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: HP0PFN Alternate function pin type: Input Alternate function: Hot Plug Signal Group 0 Power Fault Input.
GPIO[12]	I	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: HP0PWRGDN Alternate function pin type: Input Alternate function: Hot Plug Signal Group 0 Power Good Input.
GPIO[13]	I	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: HP0MRLN Alternate function pin type: Input Alternate function: Hot Plug Signal Group 0 Manually Operated Retention latch Input.
GPIO[14]	O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: HP0AIN Alternate function pin type: Output Alternate function: Hot Plug Signal Group 0 Attention Indicator Output.
GPIO[15]	O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: HP0PIN Alternate function pin type: Output Alternate function: Hot Plug Signal Group 0 Power Indicator Output.
GPIO[16]	O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: HP0PEP Alternate function pin type: Output Alternate function: Hot Plug Signal Group 0 Power Enable Output.
GPIO[17]	O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: HP0RSTN Alternate function pin type: Output Alternate function: Hot Plug Signal Group 0 Reset Output.
GPIO[18]	I	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: HP1APN Alternate function pin type: Input Alternate function: Hot Plug Signal Group 1 Attention Push Button Input.
GPIO[19]	I	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: HP1PDN Alternate function pin type: Input Alternate function: Hot Plug Signal Group 1 Presence Detect Input.

Table 5 General Purpose I/O Pins (Part 2 of 4)

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Signal	Type	Name/Description
GPIO[20]	I	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: HP1PFN Alternate function pin type: Input Alternate function: Hot Plug Signal Group 1 Power Fault Input.
GPIO[21]	I	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: HP1PWRGDN Alternate function pin type: Input Alternate function: Hot Plug Signal Group 1 Power Good Input.
GPIO[22]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. 1st Alternate function pin name: HP1MRLN 1st Alternate function pin type: Input 1st Alternate function: Hot Plug Signal Group 1 Manually Operated Retention. 2nd Alternate function pin name: P1LINKUPN 2nd Alternate function pin type: Output 2nd Alternate function: Port 1 Link Up Status Output.
GPIO[23]	O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. 1st Alternate function pin name: HP1AIN 1st Alternate function pin type: Output 1st Alternate function: Hot Plug Signal Group 1 Attention Indicator Output. 2nd Alternate function pin name: P1ACTIVEN 2nd Alternate function pin type: Output 2nd Alternate function: Port 1 Link Active Status Output.
GPIO[24]	O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. 1st Alternate function pin name: HP1PIN 1st Alternate function pin type: Output 1st Alternate function: Hot Plug Signal Group 1 Power Indicator Output. 2nd Alternate function pin name: P2LINKUPN 2nd Alternate function pin type: Output 2nd Alternate function: Port 2 Link Up Status Output.
GPIO[25]	O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. 1st Alternate function pin name: HP1PEP 1st Alternate function pin type: Output 1st Alternate function: Hot Plug Signal Group 1 Power Enable Output. 2nd Alternate function pin name: P2ACTIVEN 2nd Alternate function pin type: Output 2nd Alternate function: Port 2 Link Active Status Output.
GPIO[26]	O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. 1st Alternate function pin name: HP1RSTN 1st Alternate function pin type: Output 1st Alternate function: Hot Plug Signal Group 1 Reset Output. 2nd Alternate function pin name: P3LINKUPN 2nd Alternate function pin type: Output 2nd Alternate function: Port 3 Link Up Status Output.

Table 5 General Purpose I/O Pins (Part 3 of 4)

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Signal	Type	Name/Description
GPIO[27]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. 1st Alternate function pin name: HP2APN 1st Alternate function pin type: Input 1st Alternate function: Hot Plug Signal Group 2 Attention Push Button Input. 2nd Alternate function pin name: P3ACTIVEN 2nd Alternate function pin type: Output 2nd Alternate function: Port 3 Link Active Status Output.
GPIO[28]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. 1st Alternate function pin name: HP2PDN 1st Alternate function pin type: Input 1st Alternate function: Hot Plug Signal Group 0 Presence Detect Input. 2nd Alternate function pin name: P4LINKUPN 2nd Alternate function pin type: Output 2nd Alternate function: Port 4 Link Up Status Output.
GPIO[29]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. 1st Alternate function pin name: HP2PFN 1st Alternate function pin type: Input 1st Alternate function: Hot Plug Signal Group 2 Power Fault Input. 2nd Alternate function pin name: P4ACTIVEN 2nd Alternate function pin type: Output 2nd Alternate function: Port 4 Link Active Status Output.
GPIO[30]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. 1st Alternate function pin name: HP2PWRGDN 1st Alternate function pin type: Input 1st Alternate function: Hot Plug Signal Group 2 Power Good Input. 2nd Alternate function pin name: P5LINKUPN 2nd Alternate function pin type: Output 2nd Alternate function: Port 5 Link Up Status Output.
GPIO[31]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. 1st Alternate function pin name: HP2MRLN 1st Alternate function pin type: Input 1st Alternate function: Hot Plug Signal Group 2 Manually Operated Retention Latch Input. 2nd Alternate function pin name: P5ACTIVEN 2nd Alternate function pin type: Output 2nd Alternate function: Port 5 Link Active Status Output.

Table 5 General Purpose I/O Pins (Part 4 of 4)

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Signal	Type	Name/Description
CLKMODE[1:0]		**Clock Mode.** These signals determine the port clocking mode used by ports of the device.
GCLKFSEL	I	**Global Clock Frequency Select.** These signals select the frequency of the GCLKP and GCLKN signals. 0x0 100 MHz 0x1 125 MHz
MSMBSMODE	I	**Master SMBus Slow Mode.** The assertion of this pin indicates that the master SMBus should operate at 100 KHz instead of 400 KHz. This value may not be overridden.
P01MERGEN	I	**Port 0 and 1 Merge.** P01MERGEN is an active low signal. It is pulled low internally. When this pin is low, port 0 is merged with port 1 to form a single x8 port. The Serdes lanes associated with port 1 become lanes 4 through 7 of port 0. When this pin is high, port 0 and port 1 are not merged, and each operates as a single x4 port.
P23MERGEN	I	**Port 2 and 3 Merge.** P23MERGEN is an active low signal. It is pulled low internally. When this pin is low, port 2 is merged with port 3 to form a single x8 port. The Serdes lanes associated with port 3 become lanes 4 through 7 of port 2. When this pin is high, port 2 and port 3 are not merged, and each operates as a single x4 port.
P45MERGEN	I	**Port 4 and 5 Merge.** P45MERGEN is an active low signal. It is pulled low internally. When this pin is low, port 4 is merged with port 5 to form a single x8 port. The Serdes lanes associated with port 5 become lanes 4 through 7 of port 4. When this pin is high, port 4 and port 5 are not merged, and each operates as a single x4 port.
P67MERGEN	I	**Port 6 and 7 Merge.** P67MERGEN is an active low signal. It is pulled low internally. When this pin is low, port 6 is merged with port 7 to form a single x8 port. The Serdes lanes associated with port 7 become lanes 4 through 7 of port 6. When this pin is high, port 6 and port 7 are not merged, and each operates as a single x4 port.
P89MERGEN	I	**Port 8 and 9 Merge.** P89MERGEN is an active low signal. It is pulled low internally. When this pin is low, port 8 is merged with port 9 to form a single x8 port. The Serdes lanes associated with port 9 become lanes 4 through 7 of port 8. When this pin is high, port 8 and port 9 are not merged, and each operates as a single x4 port.
P1011MERGEN	I	**Port 10 and 11 Merge.** P1011MERGEN is an active low signal. It is pulled low internally. When this pin is low, port 10 is merged with port 11 to form a single x8 port. The Serdes lanes associated with port 11 become lanes 4 through 7 of port 10. When this pin is high, port 10 and port 11 are not merged, and each operates as a single x4 port.
P1213MERGEN	I	**Port 12 and 13 Merge.** P1213MERGEN is an active low signal. It is pulled low internally. When this pin is low, port 12 is merged with port 13 to form a single x8 port. The Serdes lanes associated with port 13 become lanes 4 through 7 of port 12. When this pin is high, port 12 and port 13 are not merged, and each operates as a single x4 port.
P1415MERGEN	I	**Port 14 and 15 Merge.** P1415MERGEN is an active low signal. It is pulled low internally. When this pin is low, port 14 is merged with port 15 to form a single x8 port. The Serdes lanes associated with port 15 become lanes 4 through 7 of port 14. When this pin is high, port 14 and port 15 are not merged, and each operates as a single x4 port.

Table 6 System Pins (Part 1 of 2)

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Signal	Type	Name/Description
PERSTN	I	**Global Reset.** Assertion of this signal resets all logic inside PES64H16G2.
RSTHALT	I	**Reset Halt.** When this signal is asserted during a PCI Express fundamental reset, PES64H16G2 executes the reset procedure and remains in a reset state with the Master and Slave SMBuses active. This allows software to read and write registers internal to the device before normal device operation begins. The device exits the reset state when the RSTHALT bit is cleared in the SWCTL register by an SMBus master.
SWMODE[3:0]	I	**Switch Mode.** These configuration pins determine the PES64H16G2 switch operating mode. **Note:** These pins should be static and not change following the negation of PERSTN. 0x0 - Single partition 0x1 - Single partition with Serial EEPROM initialization 0x2 through 0x7 - Reserved 0x8 - Single partition with port 0 selected as the upstream port (port 2 disabled) 0x9 - Single partition with port 2 selected as the upstream port (port 0 disabled) 0xA - Single partition with Serial EEPROM initialization and port 0 selected as the upstream port (port 2 disabled) 0xB - Single partition with Serial EEPROM initialization and port 2 selected as the upstream port (port 0 disabled) 0xC - Multi-partition 0xD - Multi-partition with Serial EEPROM initialization 0xE - Reserved 0xF - Reserved

Table 6 System Pins (Part 2 of 2)

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Signal	Type	Name/Description
JTAG_TCK	I	**JTAG Clock**. This is an input test clock used to clock the shifting of data into or out of the boundary scan logic or JTAG Controller. JTAG_TCK is independent of the system clock with a nominal 50% duty cycle.
JTAG_TDI	I	**JTAG Data Input**. This is the serial data input to the boundary scan logic or JTAG Controller.
JTAG_TDO	O	**JTAG Data Output**. This is the serial data shifted out from the boundary scan logic or JTAG Controller. When no data is being shifted out, this signal is tri-stated.
JTAG_TMS	I	**JTAG Mode**. The value on this signal controls the test mode select of the boundary scan logic or JTAG Controller.
JTAG_TRST_N	I	**JTAG Reset**. This active low signal asynchronously resets the boundary scan logic and JTAG TAP Controller. An external pull-up on the board is recommended to meet the JTAG specification in cases where the tester can access this signal. However, for systems running in functional mode, one of the following should occur: 1) actively drive this signal low with control logic 2) statically drive this signal low with an external pull-down on the board

Table 7 Test Pins

Signal	Type	Name/Description
REFRES00	I/O	**Port 0 External Reference Resistor.** Provides a reference for the Port 0 SerDes bias currents and PLL calibration circuitry. A 3 kOhm +/- 1% resistor should be connected from this pin to ground.
REFRES01	I/O	**Port 1 External Reference Resistor.** Provides a reference for the Port 1 SerDes bias currents and PLL calibration circuitry. A 3 kOhm +/- 1% resistor should be connected from this pin to ground.
REFRES02	I/O	**Port 2 External Reference Resistor.** Provides a reference for the Port 2 SerDes bias currents and PLL calibration circuitry. A 3 kOhm +/- 1% resistor should be connected from this pin to ground.
REFRES03	I/O	**Port 3 External Reference Resistor.** Provides a reference for the Port 3 SerDes bias currents and PLL calibration circuitry. A 3 kOhm +/- 1% resistor should be connected from this pin to ground.
REFRES04	I/O	**Port 4 External Reference Resistor.** Provides a reference for the Port 4 SerDes bias currents and PLL calibration circuitry. A 3 kOhm +/- 1% resistor should be connected from this pin to ground.
REFRES05	I/O	**Port 5 External Reference Resistor.** Provides a reference for the Port 5 SerDes bias currents and PLL calibration circuitry. A 3 kOhm +/- 1% resistor should be connected from this pin to ground.
REFRES06	I/O	**Port 6 External Reference Resistor.** Provides a reference for the Port 6 SerDes bias currents and PLL calibration circuitry. A 3 kOhm +/- 1% resistor should be connected from this pin to ground.

Table 8 Power, Ground, and SerDes Resistor Pins (Part 1 of 2)

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Signal	Type	Name/Description
REFRES07	I/O	**Port 7 External Reference Resistor.** Provides a reference for the Port 7 SerDes bias currents and PLL calibration circuitry. A 3 kOhm +/- 1% resistor should be connected from this pin to ground.
REFRES08	I/O	**Port 8 External Reference Resistor.** Provides a reference for the Port 8 SerDes bias currents and PLL calibration circuitry. A 3 kOhm +/- 1% resistor should be connected from this pin to ground.
REFRES09	I/O	**Port 9 External Reference Resistor.** Provides a reference for the Port 9 SerDes bias currents and PLL calibration circuitry. A 3 kOhm +/- 1% resistor should be connected from this pin to ground.
REFRES10	I/O	**Port 10 External Reference Resistor.** Provides a reference for the Port 10 SerDes bias currents and PLL calibration circuitry. A 3 kOhm +/- 1% resistor should be connected from this pin to ground.
REFRES11	I/O	**Port 11 External Reference Resistor.** Provides a reference for the Port 11 SerDes bias currents and PLL calibration circuitry. A 3 kOhm +/- 1% resistor should be connected from this pin to ground.
REFRES12	I/O	**Port 12 External Reference Resistor.** Provides a reference for the Port 12 SerDes bias currents and PLL calibration circuitry. A 3 kOhm +/- 1% resistor should be connected from this pin to ground.
REFRES13	I/O	**Port 13 External Reference Resistor.** Provides a reference for the Port 13 SerDes bias currents and PLL calibration circuitry. A 3 kOhm +/- 1% resistor should be connected from this pin to ground.
REFRES14	I/O	**Port 14 External Reference Resistor.** Provides a reference for the Port 14 SerDes bias currents and PLL calibration circuitry. A 3 kOhm +/- 1% resistor should be connected from this pin to ground.
REFRES15	I/O	**Port 15 External Reference Resistor.** Provides a reference for the Port 15 SerDes bias currents and PLL calibration circuitry. A 3 kOhm +/- 1% resistor should be connected from this pin to ground.
REFRESPLL	I/O	**PLL External Reference Resistor.** Provides a reference for the PLL bias currents and PLL calibration circuitry. A 3K Ohm +/- 1% resistor should be connected from this pin to ground.
V_{DD}CORE	I	**Core V_{DD}.** Power supply for core logic (1.0V).
V_{DD}I/O	I	**I/O V_{DD}.** LVTTL I/O buffer power supply (2.5V or preferred 3.3V).
V_{DD}PEA	I	**PCI Express Analog Power.** Serdes analog power supply (1.0V).
V_{DD}PEHA	I	**PCI Express Analog High Power.** Serdes analog power supply (2.5V).
V_{DD}PETA	I	**PCI Express Transmitter Analog Voltage.** Serdes transmitter analog power supply (1.0V).
V_{SS}	I	**Ground.**

Table 8 Power, Ground, and SerDes Resistor Pins (Part 2 of 2)

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Pin Characteristics

Note: Some input pads of the switch do not contain internal pull-ups or pull-downs. Unused SMBus and System inputs should be tied off to appropriate levels. This is especially critical for unused control signal inputs which, if left floating, could adversely affect operation. Also, any of these pins left floating can cause a slight increase in power consumption. Finally, unused Serdes (Rx and Tx) pins should be left floating.

Function	Pin Name	Type	Buffer	I/O Type	Internal Resistor[1]	Notes
PCI Express Interface	PE00RN[3:0]	I	PCIe differential[2]	Serial Link		
	PE00RP[3:0]	I				
	PE00TN[3:0]	O				
	PE00TP[3:0]	O				
	PE01RN[3:0]	I				
	PE01RP[3:0]	I				
	PE01TN[3:0]	O				
	PE01TP[3:0]	O				
	PE02RN[3:0]	I				
	PE02RP[3:0]	I				
	PE02TN[3:0]	O				
	PE02TP[3:0]	O				
	PE03RN[3:0]	I				
	PE03RP[3:0]	I				
	PE03TN[3:0]	O				
	PE03TP[3:0]	O				
	PE04RN[3:0]	I				
	PE04RP[3:0]	I				
	PE04TN[3:0]	O				
	PE04TP[3:0]	O				
	PE05RN[3:0]	I				
	PE05RP[3:0]	I				
	PE05TN[3:0]	O				
	PE05TP[3:0]	O				
	PE06RN[3:0]	I				
	PE06RP[3:0]	I				
	PE06TN[3:0]	O				
	PE06TP[3:0]	O				
	PE07RN[3:0]	I				
	PE07RP[3:0]	I				
	PE07TN[3:0]	O				
	PE07TP[3:0]	O				
	PE08RN[3:0]	I				
	PE08RP[3:0]	I				
	PE08TN[3:0]	O				

Table 9 Pin Characteristics (Part 1 of 3)

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Function	Pin Name	Type	Buffer	I/O Type	Internal Resistor[1]	Notes
PCI Express Interface (Cont.)	PE08TP[3:0]	O	PCIe differential	Serial Link		
	PE09RN[3:0]	I				
	PE09RP[3:0]	I				
	PE09TN[3:0]	O				
	PE09TP[3:0]	O				
	PE10RN[3:0]	I				
	PE10RP[3:0]	I				
	PE10TN[3:0]	O				
	PE10TP[3:0]	O				
	PE11RN[3:0]	I				
	PE11RP[3:0]	I				
	PE11TN[3:0]	O				
	PE11TP[3:0]	O				
	PE12RN[3:0]	I				
	PE12RP[3:0]	I				
	PE12TN[3:0]	O				
	PE12TP[3:0]	O				
	PE13RN[3:0]	I				
	PE13RP[3:0]	I				
	PE13TN[3:0]	O				
	PE13TP[3:0]	O				
	PE14RN[3:0]	I				
	PE14RP[3:0]	I				
	PE14TN[3:0]	O				
	PE14TP[3:0]	O				
	PE15RN[3:0]	I				
	PE15RP[3:0]	I				
	PE15TN[3:0]	O				
	PE15TP[3:0]	O				
	GCLKN[1:0]	I	HCSL	Diff. Clock Input		Refer to Table 10
	GCLKP[1:0]	I				
SMBus	MSMBADDR[4:1]	I	LVTTL	Input	pull-down	
	MSMBCLK	I/O		STI[3]		pull-up on board
	MSMBDAT	I/O		STI		pull-up on board
	SSMBADDR[5,3:1]	I		Input	pull-up	
	SSMBCLK	I/O		STI		pull-up on board
	SSMBDAT	I/O		STI		pull-up on board
General Purpose I/O	GPIO[31:0]	I/O	LVTTL	STI, High Drive	pull-up	

Table 9 Pin Characteristics (Part 2 of 3)

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Function	Pin Name	Type	Buffer	I/O Type	Internal Resistor[1]	Notes
System Pins	CLKMODE[1:0]	I	LVTTL	Input	pull-up	
	GCLKFSEL	I			pull-down	
	MSMBSMODE	I			pull-down	
	P01MERGEN	I			pull-down	
	P23MERGEN	I			pull-down	
	P45MERGEN	I			pull-down	
	P67MERGEN	I			pull-down	
	P89MERGEN	I			pull-down	
	P1011MERGEN	I			pull-down	
	P1213MERGEN	I			pull-down	
	P1415MERGEN	I			pull-down	
	PERSTN	I		STI		
	RSTHALT	I		Input	pull-down	
	SWMODE[3:0]	I			pull-down	
EJTAG / JTAG	JTAG_TCK	I	LVTTL	STI	pull-up	
	JTAG_TDI	I		STI	pull-up	
	JTAG_TDO	O				
	JTAG_TMS	I		STI	pull-up	
	JTAG_TRST_N	I		STI	pull-up	
SerDes Reference Resistors	REFRES00	I/O	Analog			
	REFRES01	I/O				
	REFRES02	I/O				
	REFRES03	I/O				
	REFRES04	I/O				
	REFRES05	I/O				
	REFRES06	I/O				
	REFRES07	I/O				
	REFRES08	I/O				
	REFRES09	I/O				
	REFRES10	I/O				
	REFRES11	I/O				
	REFRES12	I/O				
	REFRES13	I/O				
	REFRES14	I/O				
	REFRES15	I/O				
	REFRESPLL	I/O				

Table 9 Pin Characteristics (Part 3 of 3)

1. Internal resistor values under typical operating conditions are 92K Ω for pull-up and 91K Ω for pull-down.
2. All receiver pins set the DC common mode voltage to ground. All transmitters must be AC coupled to the media.
3. Schmitt Trigger Input (STI).

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Logic Diagram — PES64H16G2

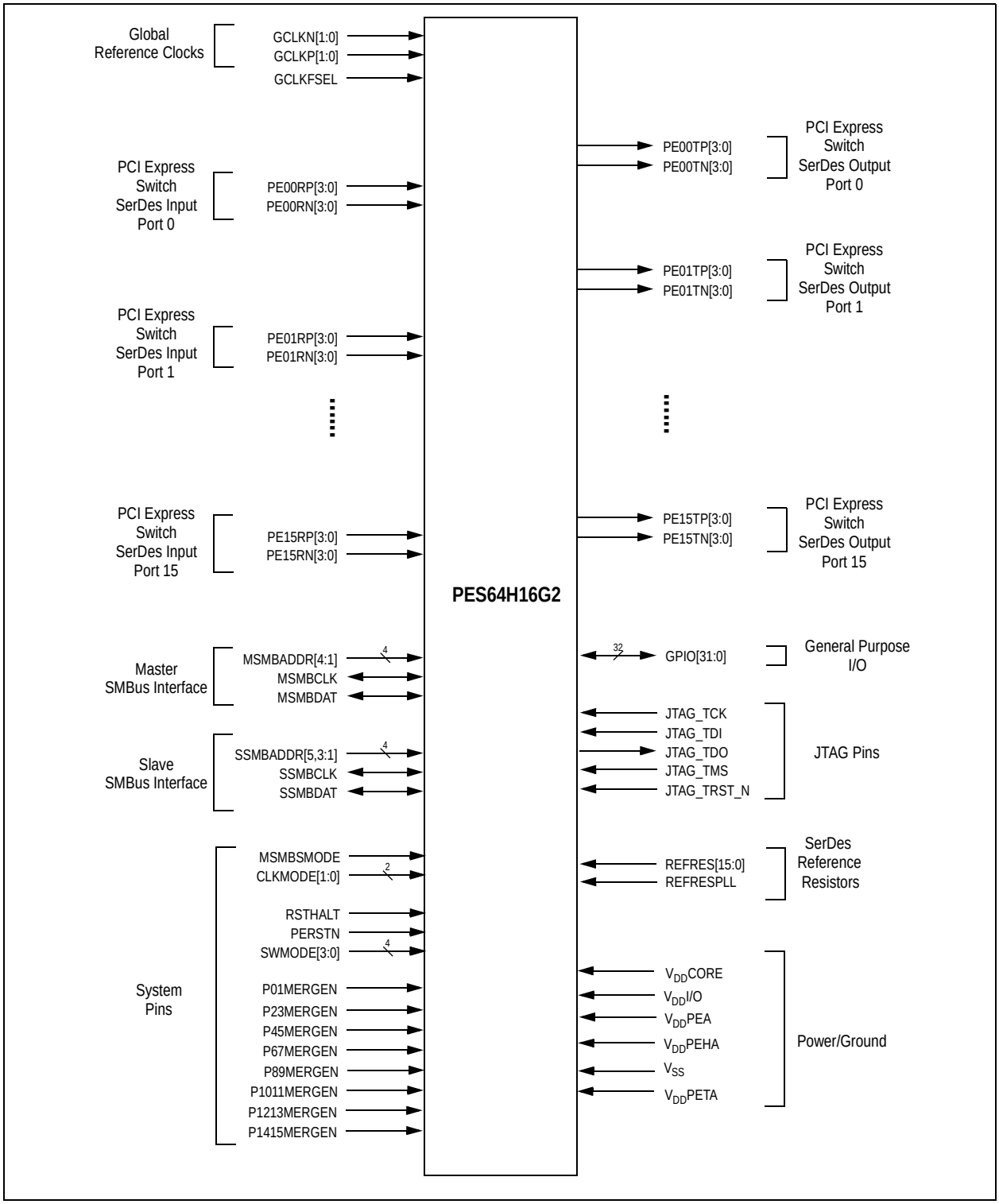


Figure 4 PES64H16G2 Logic Diagram

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System Clock Parameters

Values based on systems running at recommended supply voltages and operating temperatures, as shown in Tables 14 and 15.

Parameter	Description	Condition	Min	Typical	Max	Unit
$Refclk_{FREQ}$	Input reference clock frequency range		100		125[1]	MHz
T_{C-RISE}	Rising edge rate	Differential	0.6		4	V/ns
T_{C-FALL}	Falling edge rate	Differential	0.6		4	V/ns
V_{IH}	Differential input high voltage	Differential	+150			mV
V_{IL}	Differential input low voltage	Differential			-150	mV
V_{CROSS}	Absolute single-ended crossing point voltage	Single-ended	+250		+550	mV
$V_{CROSS-DELTA}$	Variation of V_{CROSS} over all rising clock edges	Single-ended			+140	mV
V_{RB}	Ring back voltage margin	Differential	-100		+100	mV
T_{STABLE}	Time before V_{RB} is allowed	Differential	500			ps
$T_{PERIOD-AVG}$	Average clock period accuracy		-300		2800	ppm
$T_{PERIOD-ABS}$	Absolute period, including spread-spectrum and jitter		9.847		10.203	ns
$T_{CC-JITTER}$	Cycle to cycle jitter				150	ps
V_{MAX}	Absolute maximum input voltage				+1.15	V
V_{MIN}	Absolute minimum input voltage		-0.3			V
Duty Cycle	Duty cycle		40		60	%
Rise/Fall Matching	Single ended rising Refclk edge rate versus falling Refclk edge rate			20		%
Z_{C-DC}	Clock source output DC impedance		40		60	Ω

Table 10 Input Clock Requirements

1. The input clock frequency will be either 100 or 125 MHz depending on signal GCLKFSEL.

AC Timing Characteristics

Parameter	Description	Gen 1			Gen 2			Units
		Min[1]	Typ[1]	Max[1]	Min[1]	Typ[1]	Max[1]	
PCIe Transmit								
UI	Unit Interval	399.88	400	400.12	199.94	200	200.06	ps
T_{TX-EYE}	Minimum Tx Eye Width	0.75			0.75			UI
$T_{TX-EYE-MEDIAN-to-MAX-JITTER}$	Maximum time between the jitter median and maximum deviation from the median			0.125				UI
$T_{TX-RISE}$, $T_{TX-FALL}$	TX Rise/Fall Time: 20% - 80%	0.125			0.15			UI
$T_{TX-IDLE-MIN}$	Minimum time in idle	20			20			UI

Table 11 PCIe AC Timing Characteristics (Part 1 of 2)

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Parameter	Description	Gen 1			Gen 2			Units
		Min[1]	Typ[1]	Max[1]	Min[1]	Typ[1]	Max[1]	
$T_{TX-IDLE-SET-TO-IDLE}$	Maximum time to transition to a valid Idle after sending an Idle ordered set			8			8	ns
$T_{TX-IDLE-TO-DIFF-DATA}$	Maximum time to transition from valid idle to diff data			8			8	ns
$T_{TX-SKEW}$	Transmitter data skew between any 2 lanes			1.3			1.3	ns
$T_{MIN-PULSED}$	Minimum Instantaneous Lone Pulse Width	NA			0.9			UI
$T_{TX-HF-DJ-DD}$	Transmitter Deterministic Jitter > 1.5MHz Bandwidth	NA					0.15	UI
$T_{RF-MISMATCH}$	Rise/Fall Time Differential Mismatch	NA					0.1	UI
PCIe Receive								
UI	Unit Interval	399.88	400	400.12	199.94		200.06	ps
$T_{RX-EYE\ (with\ jitter)}$	Minimum Receiver Eye Width (jitter tolerance)	0.4			0.4			UI
$T_{RX-EYE-MEDIUM\ TO\ MAX\ JITTER}$	Max time between jitter median & max deviation			0.3				UI
$T_{RX-SKEW}$	Lane to lane input skew			20			8	ns
$T_{RX-HF-RMS}$	1.5 — 100 MHz RMS jitter (common clock)	NA					3.4	ps
$T_{RX-HF-DJ-DD}$	Maximum tolerable DJ by the receiver (common clock)	NA					88	ps
$T_{RX-LF-RMS}$	10 KHz to 1.5 MHz RMS jitter (common clock)	NA					4.2	ps
$T_{RX-MIN-PULSE}$	Minimum receiver instantaneous eye width	NA			0.6			UI

Table 11 PCIe AC Timing Characteristics (Part 2 of 2)

1. Minimum, Typical, and Maximum values meet the requirements under PCI Specification 2.0

Signal	Symbol	Reference Edge	Min	Max	Unit	Timing Diagram Reference
GPIO						
GPIO[31:0][1]	Tpw[2]	None	50	—	ns	

Table 12 GPIO AC Timing Characteristics

1. GPIO signals must meet the setup and hold times if they are synchronous or the minimum pulse width if they are asynchronous.

2. The values for this symbol were determined by calculation, not by testing.

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Signal	Symbol	Reference Edge	Min	Max	Unit	Timing Diagram Reference
JTAG						
JTAG_TCK	Tper_16a	none	50.0	—	ns	See Figure 5.
	Thigh_16a, Tlow_16a		10.0	25.0	ns	
JTAG_TMS[1], JTAG_TDI	Tsu_16b	JTAG_TCK rising	2.4	—	ns	
	Thld_16b		1.0	—	ns	
JTAG_TDO	Tdo_16c	JTAG_TCK falling	—	20	ns	
	Tdz_16c[2]		—	20	ns	
JTAG_TRST_N	Tpw_16d[2]	none	25.0	—	ns	

Table 13 JTAG AC Timing Characteristics

1. The JTAG specification, IEEE 1149.1, recommends that JTAG_TMS should be held at 1 while the signal applied at JTAG_TRST_N changes from 0 to 1. Otherwise, a race may occur if JTAG_TRST_N is deasserted (going from low to high) on a rising edge of JTAG_TCK when JTAG_TMS is low, because the TAP controller might go to either the Run-Test/Idle state or stay in the Test-Logic-Reset state.

2. The values for this symbol were determined by calculation, not by testing.

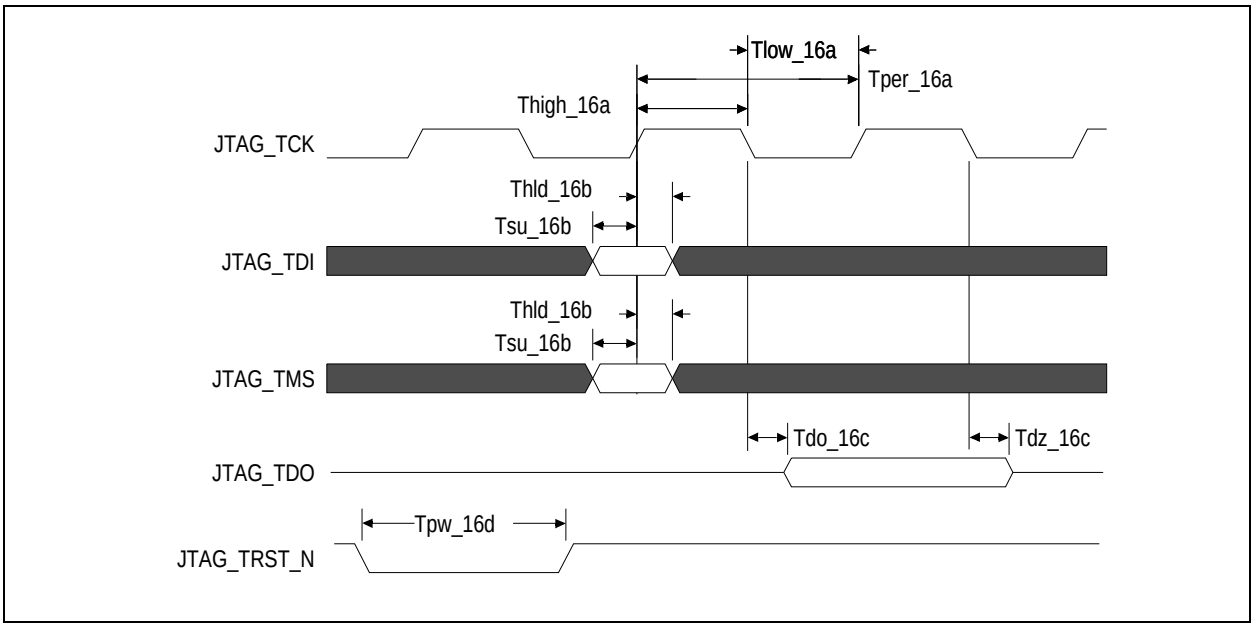


Figure 5 JTAG AC Timing Waveform

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Recommended Operating Supply Voltages

Symbol	Parameter	Minimum	Typical	Maximum	Unit
V_{DD}CORE	Internal logic supply	0.9	1.0	1.1	V
V_{DD}I/O	I/O supply except for SerDes	2.25	2.5	2.75	V
		3.125	3.3	3.465	V
V_{DD}PEA[1]	PCI Express Analog Power	0.95	1.0	1.1	V
V_{DD}PEHA[2]	PCI Express Analog High Power	2.25	2.5	2.75	V
V_{DD}PETA[1]	PCI Express Transmitter Analog Voltage	0.95	1.0	1.1	V
V_{SS}	Common ground	0	0	0	V

Table 14 PES64H16G2 Operating Voltages

1. V_{DD}PEA and V_{DD}PETA should have no more than 25m$V_{peak-peak}$ AC power supply noise superimposed on the 1.0V nominal DC value.
2. V_{DD}PEHA should have no more than 50m$V_{peak-peak}$ AC power supply noise superimposed on the 2.5V nominal DC value.

Power-Up/Power-Down Sequence

During power supply ramp-up, V_{DD}CORE must remain at least 1.0V below V_{DD}I/O at all times. There are no other power-up sequence requirements for the various operating supply voltages.

The power-down sequence can occur in any order.

Recommended Operating Temperature

Grade	Temperature
Commercial	0°C to +70°C Ambient
Industrial	-40°C to +85°C Ambient

Table 15 PES64H16G2 Operating Temperatures

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Power Consumption

Typical power is measured under the following conditions: 25°C Ambient, 35% total link usage on all ports, typical voltages defined in Table 14 (and also listed below).

Maximum power is measured under the following conditions: 70°C Ambient, 85% total link usage on all ports, maximum voltages defined in Table 14 (and also listed below).

Number of Active Lanes per Port		Core Supply		PCIe Analog Supply		PCIe Analog High Supply		PCIe Transmitter Supply		I/O Supply		Total	
		Typ 1.0V	Max 1.1V	Typ 1.0V	Max 1.1V	Typ 2.5V	Max 2.75V	Typ 1.0V	Max 1.1V	Typ 2.5V	Max 2.75V	Typ Power	Max Power
8/8/8/8/8/8/8/8 (Full Swing)	**mA**	3900	6275	2621	2875	847	872	1092	1172	32	40		
	Watts	3.90	6.90	2.62	3.16	2.12	2.40	1.09	1.29	0.08	0.11	9.81	13.86
8/8/8/8/8/8/8/8 (Half Swing)	**mA**	3900	6275	2254	2472	847	872	568	609	32	40		
	Watts	3.90	6.90	2.25	2.72	2.12	2.40	0.57	0.67	0.08	0.11	8.92	12.80

Table 16 PES64H16G2 Power Consumption — 2.5V I/O

Number of Active Lanes per Port		Core Supply		PCIe Analog Supply		PCIe Analog High Supply		PCIe Transmitter Supply		I/O Supply		Total	
		Typ 1.0V	Max 1.1V	Typ 1.0V	Max 1.1V	Typ 2.5V	Max 2.75V	Typ 1.0V	Max 1.1V	Typ 3.3V	Max 3.465V	Typ Power	Max Power
8/8/8/8/8/8/8/8 (Full Swing)	**mA**	3900	6275	2621	2875	847	872	1092	1172	36	46		
	Watts	3.90	6.90	2.62	3.16	2.12	2.40	1.09	1.29	0.12	0.16	9.85	13.91
8/8/8/8/8/8/8/8 (Half Swing)	**mA**	3900	6275	2254	2472	847	872	568	609	36	46		
	Watts	3.90	6.90	2.25	2.72	2.12	2.40	0.57	0.67	0.12	0.16	8.96	12.85

Table 17 PES64H16G2 Power Consumption — 3.3V I/O

Note 1: I/O supply of 3.3V is preferred.

Note 2: The above power consumption assumes that all ports are functioning at Gen2 (5.0 GT/S) speeds. Power consumption can be reduced by turning off unused ports through software or through boot EEPROM. Power savings will occur in V_{DD}PEA, V_{DD}PEHA, and V_{DD}PETA. Power savings can be estimated as directly proportional to the number of unused ports, since the power consumption of a turned-off port is close to zero. For example, if 3 ports out of 16 are turned off, then the power savings for each of the above three power rails can be calculated quite simply as 3/16 multiplied by the power consumption indicated in the above table.

Note 3: Using a port in Gen1 mode (2.5GT/S) results in approximately 18% power savings for each power rail: V_{DD}PEA, V_{DD}PEHA, and V_{DD}PETA.

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Thermal Considerations

This section describes thermal considerations for the PES64H16G2 (35mm^2 FCBGA1156 package). The data in Table 18 below contains information that is relevant to the thermal performance of the PES64H16G2 switch.

Symbol	Parameter	Value	Units	Conditions
$T_{J(max)}$	Junction Temperature	125	^{0}C	Maximum
$T_{A(max)}$	Ambient Temperature	70	^{0}C	Maximum for commercial-rated products
		85	^{0}C	Maximum for industrial-rated products
$\theta_{JA(effective)}$	Effective Thermal Resistance, Junction-to-Ambient	13.0	^{0}C/W	Zero air flow
		6.8	^{0}C/W	1 m/S air flow
		5.8	^{0}C/W	2 m/S air flow
θ_{JB}	Thermal Resistance, Junction-to-Board	2.5	^{0}C/W	
θ_{JC}	Thermal Resistance, Junction-to-Case	0.15	^{0}C/W	
P	Power Dissipation of the Device	13.91	Watts	Maximum

Table 18 Thermal Specifications for PES64H16G2, 35x35 mm FCBGA1156 Package

Note: It is important for the reliability of this device in any user environment that the junction temperature not exceed the $T_{J(max)}$ value specified in Table 18. Consequently, the effective junction to ambient thermal resistance (θ_{JA}) for the worst case scenario must be maintained below the value determined by the formula:

$$\theta_{JA} = (T_{J(max)} - T_{A(max)})/P$$

Given that the values of $T_{J(max)}$, $T_{A(max)}$, and P are known, the value of desired θ_{JA} becomes a known entity to the system designer. How to achieve the desired θ_{JA} is left up to the board or system designer, but in general, it can be achieved by adding the effects of θ_{JC} (value provided in Table 18), thermal resistance of the chosen adhesive (θ_{CS}), that of the heat sink (θ_{SA}), amount of airflow, and properties of the circuit board (number of layers and size of the board). It is strongly recommended that users perform their own thermal analysis for their own board and system design scenarios.

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DC Electrical Characteristics

Values based on systems running at recommended supply voltages, as shown in Table 14.

Note: See Table 9, Pin Characteristics, for a complete I/O listing.

I/O Type	Parameter	Description	Gen1			Gen2			Unit	Condi-tions
			Min[1]	Typ[1]	Max[1]	Min[1]	Typ[1]	Max[1]		
Serial Link	PCIe Transmit									
	$V_{TX-DIFFp-p}$	Differential peak-to-peak output voltage	800		1200	800		1200	mV	
	$V_{TX-DIFFp-p-LOW}$	Low-Drive Differential Peak to Peak Output Voltage	400		1200	400		1200	mV	
	$V_{TX-DE-RATIO-3.5dB}$	De-emphasized differential output voltage	-3		-4	-3.0	-3.5	-4.0	dB	
	$V_{TX-DE-RATIO-6.0dB}$	De-emphasized differential output voltage	NA			-5.5	-6.0	-6.5	dB	
	$V_{TX-DC-CM}$	DC Common mode voltage	0		3.6	0		3.6	V	
	$V_{TX-CM-ACP}$	RMS AC peak common mode output voltage			20				mV	
	$V_{TX-CM-DC-active-idle-delta}$	Abs delta of DC common mode voltage between L0 and idle			100			100	mV	
	$V_{TX-CM-DC-line-delta}$	Abs delta of DC common mode voltage between D+ and D-			25			25	mV	
	$V_{TX-Idle-DiffP}$	Electrical idle diff peak output			20			20	mV	
	$RL_{TX-DIFF}$	Transmitter Differential Return loss	10					10	dB	0.05 - 1.25GHz
								8	dB	1.25 - 2.5GHz
	RL_{TX-CM}	Transmitter Common Mode Return loss	6					6	dB	
	$Z_{TX-DIFF-DC}$	DC Differential TX impedance	80	100	120			120	Ω	
	VTX-CM-ACpp	Peak-Peak AC Common	NA					100	mV	
	$V_{TX-DC-CM}$	Transmit Driver DC Common Mode Voltage	0		3.6	0		3.6	V	
	$V_{TX-RCV-DETECT}$	The amount of voltage change allowed during Receiver Detec-tion			600			600	mV	
	$I_{TX-SHORT}$	Transmitter Short Circuit Current Limit	0		90				90	mA

Table 19 DC Electrical Characteristics (Part 1 of 2)

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I/O Type	Parameter	Description	Gen1			Gen2			Unit	Conditions
			Min[1]	Typ[1]	Max[1]	Min[1]	Typ[1]	Max[1]		
Serial Link (cont.)	PCIe Receive									
	$V_{RX-DIFFp-p}$	Differential input voltage (peak-to-peak)	175		1200	120		1200	mV	
	$RL_{RX-DIFF}$	Receiver Differential Return Loss	10					10	dB	0.05 - 1.25GHz
								8		1.25 - 2.5GHz
	RL_{RX-CM}	Receiver Common Mode Return Loss	6					6	dB	
	$Z_{RX-DIFF-DC}$	Differential input impedance (DC)	80	100	120	Refer to return loss spec			Ω	
	Z_{RX--DC}	DC common mode impedance	40	50	60	40		60	Ω	
	$Z_{RX-COMM-DC}$	Powered down input common mode impedance (DC)	200k	350k				50k	Ω	
	$Z_{RX-HIGH-IMP-DC-POS}$	DC input CM input impedance for V>0 during reset or power down			50k			50k	Ω	
	$Z_{RX-HIGH-IMP-DC-NEG}$	DC input CM input impedance for V<0 during reset or power down			1.0k			1.0k	Ω	
	$V_{RX-IDLE-DET-DIFFp-p}$	Electrical idle detect threshold	65		175	65		175	mV	
	$V_{RX-CM-ACp}$	Receiver AC common-mode peak voltage			150			150	mV	$V_{RX-CM-ACp}$
PCIe REFCLK										
	C_{IN}	Input Capacitance	1.5	—		1.5	—		pF	
Other I/Os										
LOW Drive Output	I_{OL}		—	2.5	—	—	2.5	—	mA	V_{OL} = 0.4v
	I_{OH}		—	-5.5	—	—	-5.5	—	mA	V_{OH} = 1.5V
High Drive Output	I_{OL}		—	12.0	—	—	12.0	—	mA	V_{OL} = 0.4v
	I_{OH}		—	-20.0	—	—	-20.0	—	mA	V_{OH} = 1.5V
Schmitt Trigger Input (STI)	V_{IL}		-0.3	—	0.8	-0.3	—	0.8	V	—
	V_{IH}		2.0	—	V_{DD}I/O + 0.5	2.0	—	V_{DD}I/O + 0.5	V	—
Input	V_{IL}		-0.3	—	0.8	-0.3	—	0.8	V	—
	V_{IH}		2.0	—	V_{DD}I/O + 0.5	2.0	—	V_{DD}I/O + 0.5	V	—
Capacitance	C_{IN}		—	—	8.5	—	—	8.5	pF	—
Leakage	Inputs		—	—	± 10	—	—	± 10	µA	V_{DD}I/O (max)
	$I/O_{LEAK\ W/O}$ Pull-ups/downs		—	—	± 10	—	—	± 10	µA	V_{DD}I/O (max)
	$I/O_{LEAK\ WITH}$ Pull-ups/downs		—	—	± 80	—	—	± 80	µA	V_{DD}I/O (max)

Table 19 DC Electrical Characteristics (Part 2 of 2)

1. Minimum, Typical, and Maximum values meet the requirements under PCI Specification 2.0.

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Absolute Maximum Voltage Rating

Core Supply	PCIe Analog Supply	PCIe Analog High Supply	PCIe Transmitter Supply	I/O Supply
1.5V	1.5V	4.6V	1.5V	4.6V

Table 20 PES64H16G2 Absolute Maximum Voltage Rating

Warning: For proper and reliable operation in adherence with this data sheet, the device should not exceed the recommended operating voltages in Table 14. The absolute maximum operating voltages in Table 20 are offered to provide guidelines for voltage excursions outside the recommended voltage ranges. Device functionality is not guaranteed at these conditions and sustained operation at these values or any exposure to voltages outside the maximum range may adversely affect device functionality and reliability.

SMBus Characterization

Symbol	Parameter	SMBus 2.0 Char. Data[1]			Unit
		3V	3.3V	3.6V	
DC Parameter for SDA Pin					
V_{IL}	Input Low	1.16	1.26	1.35	V
V_{IH}	Input High	1.56	1.67	1.78	V
$V_{OL@350uA}$	Output Low	15	15	15	mV
$I_{OL@0.4V}$		23	24	25	mA
I_{Pullup}	Current Source	—	—	—	µA
I_{IL_Leak}	Input Low Leakage	0	0	0	µA
I_{IH_Leak}	Input High Leakage	0	0	0	µA
DC Parameter for SCL Pin					
$V_{IL\ (V)}$	Input Low	1.11	1.2	1.31	V
$V_{IH\ (V)}$	Input High	1.54	1.65	1.76	V
I_{IL_Leak}	Input Low Leakage	0	0	0	µA
I_{IH_Leak}	Input High Leakage	0	0	0	µA

Table 21 SMBus DC Characterization Data

1. Data at room and hot temperature.

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Symbol	Parameter	SMBus @3.3V ±10%[1]		Unit
		Min	Max	
F_{SCL}	Clock frequency	5	600	KHz
T_{BUF}	Bus free time between Stop and Start	3.5	—	µs
$T_{HD:STA}$	Start condition hold time	1	—	µs
$T_{SU:STA}$	Start condition setup time	1	—	µs
$T_{SU:STO}$	Stop condition setup time	1	—	µs
$T_{HD:DAT}$	Data hold time	1	—	ns
$T_{SU:DAT}$	Data setup time	1	—	ns
$T_{TIMEOUT}$	Detect clock low time out	—	74.7	ms
T_{LOW}	Clock low period	3.7	—	µs
T_{HIGH}	Clock high period	3.7	—	µs
T_F	Clock/Data fall time	—	72.2	ns
T_R	Clock/Data rise time	—	68.3	ns
$T_{POR@10kHz}$	Time which a device must be operational after power-on reset	20	—	ms

Table 22 SMBus AC Timing Data

1. Data at room and hot temperature.

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Package Pinout — 1156-BGA Signal Pinout for PES64H16G2

The following table lists the pin numbers and signal names for the PES64H16G2 device.

Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt
A1	V_{SS}		B1	V_{SS}		C1	GPIO_29	2	D1	GPIO_28	2
A2	V_{SS}		B2	V_{DD}I/O		C2	GPIO_27	2	D2	GPIO_26	2
A3	GPIO_19	1	B3	GPIO_18	1	C3	GPIO_21	1	D3	V_{DD}I/O	
A4	V_{DD}I/O		B4	GPIO_17	1	C4	GPIO_16	1	D4	GPIO_23	2
A5	V_{SS}		B5	V_{SS}		C5	V_{SS}		D5	V_{SS}	
A6	PE09TP3		B6	PE09TN3		C6	V_{SS}		D6	PE09RN3	
A7	PE09TP2		B7	PE09TN2		C7	V_{SS}		D7	PE09RN2	
A8	V_{SS}		B8	V_{SS}		C8	V_{SS}		D8	V_{SS}	
A9	PE09TP1		B9	PE09TN1		C9	V_{SS}		D9	PE09RN1	
A10	PE09TP0		B10	PE09TN0		C10	V_{SS}		D10	PE09RN0	
A11	V_{SS}		B11	V_{SS}		C11	V_{SS}		D11	V_{SS}	
A12	PE08TP3		B12	PE08TN3		C12	V_{SS}		D12	PE08RN3	
A13	PE08TP2		B13	PE08TN2		C13	V_{SS}		D13	PE08RN2	
A14	V_{SS}		B14	V_{SS}		C14	V_{SS}		D14	V_{SS}	
A15	PE08TP1		B15	PE08TN1		C15	V_{SS}		D15	PE08RN1	
A16	PE08TP0		B16	PE08TN0		C16	V_{SS}		D16	PE08RN0	
A17	V_{SS}		B17	V_{SS}		C17	V_{SS}		D17	V_{SS}	
A18	PE03TP3		B18	PE03TN3		C18	V_{SS}		D18	PE03RN3	
A19	PE03TP2		B19	PE03TN2		C19	V_{SS}		D19	PE03RN2	
A20	V_{SS}		B20	V_{SS}		C20	V_{SS}		D20	V_{SS}	
A21	PE03TP1		B21	PE03TN1		C21	V_{SS}		D21	PE03RN1	
A22	PE03TP0		B22	PE03TN0		C22	V_{SS}		D22	PE03RN0	
A23	V_{SS}		B23	V_{SS}		C23	V_{SS}		D23	V_{SS}	
A24	PE02TP3		B24	PE02TN3		C24	V_{SS}		D24	PE02RN3	
A25	PE02TP2		B25	PE02TN2		C25	V_{SS}		D25	PE02RN2	
A26	V_{SS}		B26	V_{SS}		C26	V_{SS}		D26	V_{SS}	
A27	PE02TP1		B27	PE02TN1		C27	V_{SS}		D27	PE02RN1	
A28	PE02TP0		B28	PE02TN0		C28	V_{SS}		D28	PE02RN0	
A29	V_{SS}		B29	V_{SS}		C29	V_{SS}		D29	V_{SS}	
A30	V_{DD}I/O		B30	MSMBADDR_3		C30	MSMBADDR_4		D30	JTAG_TMS	
A31	MSMBADDR_1		B31	MSMBADDR_2		C31	JTAG_TDI		D31	V_{DD}I/O	
A32	MSMBSMODE		B32	PERSTN		C32	JTAG_TRST_N		D32	SSMBADDR_5	
A33	V_{SS}		B33	V_{DD}I/O		C33	SSMBADDR_2		D33	SSMBADDR_3	
A34	V_{SS}		B34	V_{SS}		C34	SSMBADDR_1		D34	V_{DD}I/O	

Table 23 PES64H16G2 1156-pin Signal Pin-Out (Part 1 of 9)

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Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt
E1	V_{DD}I/O		F1	V_{SS}		G1	PE10TP0		H1	PE10TP1	
E2	GPIO_30	2	F2	V_{SS}		G2	PE10TN0		H2	PE10TN1	
E3	GPIO_31	2	F3	V_{SS}		G3	V_{SS}		H3	V_{SS}	
E4	GPIO_24	2	F4	V_{SS}		G4	PE10RN0		H4	PE10RN1	
E5	V_{SS}		F5	V_{SS}		G5	PE10RP0		H5	PE10RP1	
E6	PE09RP3		F6	V_{SS}		G6	V_{SS}		H6	V_{SS}	
E7	PE09RP2		F7	V_{SS}		G7	V_{SS}		H7	V_{SS}	
E8	V_{SS}		F8	V_{SS}		G8	V_{SS}		H8	GPIO_20	1
E9	PE09RP1		F9	V_{SS}		G9	V_{SS}		H9	V_{DD}I/O	
E10	PE09RP0		F10	REFRES09		G10	V_{SS}		H10	V_{SS}	
E11	V_{SS}		F11	V_{SS}		G11	V_{SS}		H11	V_{SS}	
E12	PE08RP3		F12	V_{SS}		G12	NC		H12	V_{SS}	
E13	PE08RP2		F13	V_{SS}		G13	V_{SS}		H13	V_{DD}PEHA	
E14	V_{SS}		F14	V_{SS}		G14	V_{SS}		H14	V_{SS}	
E15	PE08RP1		F15	V_{SS}		G15	NC		H15	V_{DD}PETA	
E16	PE08RP0		F16	V_{SS}		G16	V_{SS}		H16	V_{SS}	
E17	V_{SS}		F17	REFRESPLL		G17	GCLKN0		H17	V_{SS}	
E18	PE03RP3		F18	V_{SS}		G18	GCLKP0		H18	V_{SS}	
E19	PE03RP2		F19	REFRES03		G19	NC		H19	V_{SS}	
E20	V_{SS}		F20	V_{SS}		G20	V_{SS}		H20	V_{DD}PETA	
E21	PE03RP1		F21	V_{SS}		G21	V_{SS}		H21	REFRES02	
E22	PE03RP0		F22	V_{SS}		G22	NC		H22	V_{DD}PEHA	
E23	V_{SS}		F23	V_{SS}		G23	V_{SS}		H23	V_{SS}	
E24	PE02RP3		F24	V_{SS}		G24	V_{SS}		H24	V_{SS}	
E25	PE02RP2		F25	V_{SS}		G25	V_{SS}		H25	V_{SS}	
E26	V_{SS}		F26	V_{SS}		G26	V_{SS}		H26	MSMBDAT	
E27	PE02RP1		F27	V_{SS}		G27	MSMBCLK		H27	V_{DD}I/O	
E28	PE02RP0		F28	V_{SS}		G28	V_{SS}		H28	SSMBCLK	
E29	V_{SS}		F29	V_{SS}		G29	V_{SS}		H29	V_{SS}	
E30	V_{SS}		F30	PE01RP3		G30	PE01RP2		H30	V_{SS}	
E31	V_{SS}		F31	PE01RN3		G31	PE01RN2		H31	V_{SS}	
E32	V_{SS}		F32	V_{SS}		G32	V_{SS}		H32	V_{SS}	
E33	V_{SS}		F33	PE01TN3		G33	PE01TN2		H33	V_{SS}	
E34	V_{SS}		F34	PE01TP3		G34	PE01TP2		H34	V_{SS}	

Table 23 PES64H16G2 1156-pin Signal Pin-Out (Part 2 of 9)

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Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt
J1	V_{SS}		K1	PE10TP2		L1	PE10TP3		M1	V_{SS}	
J2	V_{SS}		K2	PE10TN2		L2	PE10TN3		M2	V_{SS}	
J3	V_{SS}		K3	V_{SS}		L3	V_{SS}		M3	V_{SS}	
J4	V_{SS}		K4	PE10RN2		L4	PE10RN3		M4	V_{SS}	
J5	V_{SS}		K5	PE10RP2		L5	PE10RP3		M5	V_{SS}	
J6	V_{SS}		K6	V_{SS}		L6	V_{SS}		M6	V_{SS}	
J7	V_{SS}		K7	V_{SS}		L7	V_{SS}		M7	V_{SS}	
J8	V_{SS}		K8	V_{SS}		L8	V_{SS}		M8	V_{SS}	
J9	GPIO_25	2	K9	V_{DD}I/O		L9	V_{SS}		M9	V_{SS}	
J10	V_{SS}		K10	GPIO_22	2	L10	V_{SS}		M10	V_{SS}	
J11	V_{SS}		K11	V_{SS}		L11	V_{SS}		M11	V_{SS}	
J12	V_{SS}		K12	V_{SS}		L12	V_{SS}		M12	V_{SS}	
J13	V_{SS}		K13	V_{DD}PEHA		L13	V_{DD}PEA		M13	V_{DD}PEA	
J14	V_{DD}PEA		K14	V_{SS}		L14	V_{DD}PEA		M14	V_{SS}	
J15	REFRES08		K15	V_{DD}PETA		L15	V_{DD}PEA		M15	V_{DD}PEA	
J16	V_{SS}		K16	V_{SS}		L16	V_{SS}		M16	V_{SS}	
J17	V_{DD}PEHA		K17	V_{DD}PEHA		L17	V_{DD}PEA		M17	V_{DD}PEA	
J18	V_{DD}PEHA		K18	V_{DD}PEHA		L18	V_{DD}PEA		M18	V_{DD}PEA	
J19	V_{SS}		K19	V_{SS}		L19	V_{SS}		M19	V_{SS}	
J20	V_{SS}		K20	V_{DD}PETA		L20	V_{DD}PEA		M20	V_{DD}PEA	
J21	V_{DD}PEA		K21	V_{SS}		L21	V_{DD}PEA		M21	V_{SS}	
J22	V_{SS}		K22	V_{DD}PEHA		L22	V_{DD}PEA		M22	V_{DD}PEA	
J23	V_{SS}		K23	V_{SS}		L23	V_{SS}		M23	V_{SS}	
J24	V_{SS}		K24	V_{SS}		L24	V_{SS}		M24	V_{SS}	
J25	JTAG_TDO		K25	CLKMODE1		L25	V_{SS}		M25	V_{SS}	
J26	V_{DD}I/O		K26	JTAG_TCK		L26	V_{SS}		M26	V_{SS}	
J27	SSMBDAT		K27	V_{SS}		L27	V_{SS}		M27	V_{SS}	
J28	V_{SS}		K28	V_{SS}		L28	V_{SS}		M28	REFRES01	
J29	V_{SS}		K29	V_{SS}		L29	V_{SS}		M29	V_{SS}	
J30	PE01RP1		K30	PE01RP0		L30	V_{SS}		M30	PE00RP3	
J31	PE01RN1		K31	PE01RN0		L31	V_{SS}		M31	PE00RN3	
J32	V_{SS}		K32	V_{SS}		L32	V_{SS}		M32	V_{SS}	
J33	PE01TN1		K33	PE01TN0		L33	V_{SS}		M33	PE00TN3	
J34	PE01TP1		K34	PE01TP0		L34	V_{SS}		M34	PE00TP3	

Table 23 PES64H16G2 1156-pin Signal Pin-Out (Part 3 of 9)

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Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt
N1	PE11TP0		P1	PE11TP1		R1	V_{SS}		T1	PE11TP2	
N2	PE11TN0		P2	PE11TN1		R2	V_{SS}		T2	PE11TN2	
N3	V_{SS}		P3	V_{SS}		R3	V_{SS}		T3	V_{SS}	
N4	PE11RN0		P4	PE11RN1		R4	V_{SS}		T4	PE11RN2	
N5	PE11RP0		P5	PE11RP1		R5	V_{SS}		T5	PE11RP2	
N6	V_{SS}		P6	V_{SS}		R6	V_{SS}		T6	NC	
N7	NC		P7	V_{SS}		R7	REFRES10		T7	V_{SS}	
N8	V_{DD}PEHA		P8	V_{SS}		R8	V_{DD}PETA		T8	V_{SS}	
N9	V_{SS}		P9	V_{DD}PEA		R9	V_{SS}		T9	REFRES11	
N10	V_{DD}PEHA		P10	V_{SS}		R10	V_{DD}PETA		T10	V_{SS}	
N11	V_{DD}PEA		P11	V_{DD}PEA		R11	V_{DD}PEA		T11	V_{SS}	
N12	V_{DD}PEA		P12	V_{SS}		R12	V_{DD}PEA		T12	V_{SS}	
N13	V_{DD}CORE		P13	V_{DD}CORE		R13	V_{DD}CORE		T13	V_{SS}	
N14	V_{DD}CORE		P14	V_{SS}		R14	V_{DD}CORE		T14	V_{SS}	
N15	V_{DD}CORE		P15	V_{DD}CORE		R15	V_{SS}		T15	V_{DD}CORE	
N16	V_{SS}		P16	V_{SS}		R16	V_{DD}CORE		T16	V_{SS}	
N17	V_{DD}CORE		P17	V_{DD}CORE		R17	V_{SS}		T17	V_{DD}CORE	
N18	V_{SS}		P18	V_{SS}		R18	V_{DD}CORE		T18	V_{SS}	
N19	V_{DD}CORE		P19	V_{DD}CORE		R19	V_{SS}		T19	V_{DD}CORE	
N20	V_{DD}CORE		P20	V_{SS}		R20	V_{DD}CORE		T20	V_{SS}	
N21	V_{DD}CORE		P21	V_{DD}CORE		R21	V_{SS}		T21	V_{DD}CORE	
N22	V_{DD}CORE		P22	V_{DD}CORE		R22	V_{DD}CORE		T22	V_{DD}CORE	
N23	V_{DD}PEA		P23	V_{SS}		R23	V_{DD}PEA		T23	V_{SS}	
N24	V_{DD}PEA		P24	V_{DD}PEA		R24	V_{DD}PEA		T24	V_{SS}	
N25	V_{DD}PEHA		P25	V_{SS}		R25	V_{DD}PETA		T25	V_{SS}	
N26	V_{SS}		P26	V_{DD}PEA		R26	V_{SS}		T26	V_{SS}	
N27	V_{DD}PEHA		P27	V_{SS}		R27	V_{DD}PETA		T27	V_{SS}	
N28	NC		P28	V_{SS}		R28	V_{SS}		T28	V_{SS}	
N29	V_{SS}		P29	V_{SS}		R29	REFRES00		T29	NC	
N30	PE00RP2		P30	V_{SS}		R30	PE00RP1		T30	PE00RP0	
N31	PE00RN2		P31	V_{SS}		R31	PE00RN1		T31	PE00RN0	
N32	V_{SS}		P32	V_{SS}		R32	V_{SS}		T32	V_{SS}	
N33	PE00TN2		P33	V_{SS}		R33	PE00TN1		T33	PE00TN0	
N34	PE00TP2		P34	V_{SS}		R34	PE00TP1		T34	PE00TP0	

Table 23 PES64H16G2 1156-pin Signal Pin-Out (Part 4 of 9)

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Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt
U1	PE11TP3		V1	V_{SS}		W1	PE04TP0		Y1	PE04TP1	
U2	PE11TN3		V2	V_{SS}		W2	PE04TN0		Y2	PE04TN1	
U3	V_{SS}		V3	V_{SS}		W3	V_{SS}		Y3	V_{SS}	
U4	PE11RN3		V4	V_{SS}		W4	PE04RN0		Y4	PE04RN1	
U5	PE11RP3		V5	V_{SS}		W5	PE04RP0		Y5	PE04RP1	
U6	V_{SS}		V6	V_{SS}		W6	V_{SS}		Y6	NC	
U7	NC		V7	NC		W7	V_{SS}		Y7	REFRES04	
U8	V_{SS}		V8	V_{SS}		W8	V_{SS}		Y8	V_{DD}PETA	
U9	V_{DD}PEHA		V9	V_{DD}PEHA		W9	V_{SS}		Y9	V_{SS}	
U10	V_{DD}PEHA		V10	V_{DD}PEHA		W10	V_{SS}		Y10	V_{DD}PETA	
U11	V_{DD}PEA		V11	V_{DD}PEA		W11	V_{SS}		Y11	V_{DD}PEA	
U12	V_{DD}PEA		V12	V_{DD}PEA		W12	V_{SS}		Y12	V_{DD}PEA	
U13	V_{DD}CORE		V13	V_{SS}		W13	V_{DD}CORE		Y13	V_{DD}CORE	
U14	V_{DD}CORE		V14	V_{SS}		W14	V_{DD}CORE		Y14	V_{SS}	
U15	V_{SS}		V15	V_{DD}CORE		W15	V_{SS}		Y15	V_{DD}CORE	
U16	V_{DD}CORE		V16	V_{SS}		W16	V_{DD}CORE		Y16	V_{SS}	
U17	V_{SS}		V17	V_{DD}CORE		W17	V_{SS}		Y17	V_{DD}CORE	
U18	V_{DD}CORE		V18	V_{SS}		W18	V_{DD}CORE		Y18	V_{SS}	
U19	V_{SS}		V19	V_{DD}CORE		W19	V_{SS}		Y19	V_{DD}CORE	
U20	V_{DD}CORE		V20	V_{SS}		W20	V_{DD}CORE		Y20	V_{SS}	
U21	V_{SS}		V21	V_{DD}CORE		W21	V_{SS}		Y21	V_{DD}CORE	
U22	V_{SS}		V22	V_{DD}CORE		W22	V_{SS}		Y22	V_{DD}CORE	
U23	V_{DD}PEA		V23	V_{DD}PEA		W23	V_{SS}		Y23	V_{DD}PEA	
U24	V_{DD}PEA		V24	V_{DD}PEA		W24	V_{SS}		Y24	V_{DD}PEA	
U25	V_{DD}PEHA		V25	V_{DD}PEHA		W25	V_{SS}		Y25	V_{DD}PETA	
U26	V_{DD}PEHA		V26	V_{DD}PEHA		W26	NC		Y26	V_{SS}	
U27	V_{SS}		V27	V_{SS}		W27	V_{SS}		Y27	V_{DD}PETA	
U28	NC		V28	NC		W28	V_{SS}		Y28	V_{SS}	
U29	V_{SS}		V29	V_{SS}		W29	REFRES15		Y29	NC	
U30	V_{SS}		V30	PE15RP3		W30	PE15RP2		Y30	V_{SS}	
U31	V_{SS}		V31	PE15RN3		W31	PE15RN2		Y31	V_{SS}	
U32	V_{SS}		V32	V_{SS}		W32	V_{SS}		Y32	V_{SS}	
U33	V_{SS}		V33	PE15TN3		W33	PE15TN2		Y33	V_{SS}	
U34	V_{SS}		V34	PE15TP3		W34	PE15TP2		Y34	V_{SS}	

Table 23 PES64H16G2 1156-pin Signal Pin-Out (Part 5 of 9)

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Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt
AA1	V_{SS}		AB1	PE04TP2		AC1	PE04TP3		AD1	V_{SS}	
AA2	V_{SS}		AB2	PE04TN2		AC2	PE04TN3		AD2	V_{SS}	
AA3	V_{SS}		AB3	V_{SS}		AC3	V_{SS}		AD3	V_{SS}	
AA4	V_{SS}		AB4	PE04RN2		AC4	PE04RN3		AD4	V_{SS}	
AA5	V_{SS}		AB5	PE04RP2		AC5	PE04RP3		AD5	V_{SS}	
AA6	V_{SS}		AB6	REFRES05		AC6	V_{SS}		AD6	V_{SS}	
AA7	V_{SS}		AB7	NC		AC7	V_{SS}		AD7	V_{SS}	
AA8	V_{SS}		AB8	V_{DD}PEHA		AC8	V_{SS}		AD8	V_{SS}	
AA9	V_{DD}PEA		AB9	V_{SS}		AC9	V_{SS}		AD9	NC	
AA10	V_{SS}		AB10	V_{DD}PEHA		AC10	V_{SS}		AD10	NC	
AA11	V_{DD}PEA		AB11	V_{DD}PEA		AC11	V_{SS}		AD11	V_{SS}	
AA12	V_{SS}		AB12	V_{DD}PEA		AC12	V_{SS}		AD12	V_{SS}	
AA13	V_{DD}CORE		AB13	V_{DD}CORE		AC13	V_{DD}PEA		AD13	V_{DD}PEA	
AA14	V_{DD}CORE		AB14	V_{DD}CORE		AC14	V_{SS}		AD14	V_{DD}PEA	
AA15	V_{SS}		AB15	V_{DD}CORE		AC15	V_{DD}PEA		AD15	V_{DD}PEA	
AA16	V_{DD}CORE		AB16	V_{DD}CORE		AC16	V_{SS}		AD16	V_{SS}	
AA17	V_{SS}		AB17	V_{SS}		AC17	V_{DD}PEA		AD17	V_{DD}PEA	
AA18	V_{DD}CORE		AB18	V_{DD}CORE		AC18	V_{DD}PEA		AD18	V_{DD}PEA	
AA19	V_{SS}		AB19	V_{SS}		AC19	V_{SS}		AD19	V_{SS}	
AA20	V_{DD}CORE		AB20	V_{DD}CORE		AC20	V_{DD}PEA		AD20	V_{DD}PEA	
AA21	V_{SS}		AB21	V_{DD}CORE		AC21	V_{SS}		AD21	V_{DD}PEA	
AA22	V_{DD}CORE		AB22	V_{DD}CORE		AC22	V_{DD}PEA		AD22	V_{DD}PEA	
AA23	V_{SS}		AB23	V_{DD}PEA		AC23	V_{SS}		AD23	V_{SS}	
AA24	V_{DD}PEA		AB24	V_{DD}PEA		AC24	V_{SS}		AD24	V_{SS}	
AA25	V_{SS}		AB25	V_{DD}PEHA		AC25	V_{SS}		AD25	V_{SS}	
AA26	V_{DD}PEA		AB26	V_{SS}		AC26	V_{SS}		AD26	V_{SS}	
AA27	V_{SS}		AB27	V_{DD}PEHA		AC27	V_{SS}		AD27	V_{SS}	
AA28	V_{SS}		AB28	V_{SS}		AC28	V_{SS}		AD28	V_{SS}	
AA29	REFRES14		AB29	V_{SS}		AC29	V_{SS}		AD29	V_{SS}	
AA30	PE15RP1		AB30	PE15RP0		AC30	V_{SS}		AD30	PE14RP3	
AA31	PE15RN1		AB31	PE15RN0		AC31	V_{SS}		AD31	PE14RN3	
AA32	V_{SS}		AB32	V_{SS}		AC32	V_{SS}		AD32	V_{SS}	
AA33	PE15TN1		AB33	PE15TN0		AC33	V_{SS}		AD33	PE14TN3	
AA34	PE15TP1		AB34	PE15TP0		AC34	V_{SS}		AD34	PE14TP3	

Table 23 PES64H16G2 1156-pin Signal Pin-Out (Part 6 of 9)

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Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt
AE1	PE05TP0		AF1	PE05TP1		AG1	V_{SS}		AH1	PE05TP2	
AE2	PE05TN0		AF2	PE05TN1		AG2	V_{SS}		AH2	PE05TN2	
AE3	V_{SS}		AF3	V_{SS}		AG3	V_{SS}		AH3	V_{SS}	
AE4	PE05RN0		AF4	PE05RN1		AG4	V_{SS}		AH4	PE05RN2	
AE5	PE05RP0		AF5	PE05RP1		AG5	V_{SS}		AH5	PE05RP2	
AE6	V_{SS}		AF6	V_{SS}		AG6	V_{SS}		AH6	V_{SS}	
AE7	V_{SS}		AF7	V_{SS}		AG7	CLKMODE0		AH7	V_{SS}	
AE8	V_{SS}		AF8	V_{SS}		AG8	V_{DD}I/O		AH8	GCLKFSEL	
AE9	V_{DD}I/O		AF9	V_{DD}I/O		AG9	V_{DD}I/O		AH9	V_{SS}	
AE10	V_{DD}I/O		AF10	V_{DD}I/O		AG10	V_{SS}		AH10	V_{SS}	
AE11	V_{SS}		AF11	V_{SS}		AG11	V_{SS}		AH11	V_{SS}	
AE12	V_{SS}		AF12	V_{SS}		AG12	V_{SS}		AH12	V_{SS}	
AE13	V_{DD}PEHA		AF13	V_{SS}		AG13	V_{DD}PEHA		AH13	V_{SS}	
AE14	V_{SS}		AF14	V_{DD}PEA		AG14	V_{SS}		AH14	REFRES06	
AE15	V_{DD}PETA		AF15	V_{SS}		AG15	V_{DD}PETA		AH15	V_{SS}	
AE16	V_{SS}		AF16	V_{SS}		AG16	V_{SS}		AH16	NC	
AE17	V_{DD}PEHA		AF17	V_{DD}PEHA		AG17	V_{SS}		AH17	GCLKP1	
AE18	V_{DD}PEHA		AF18	V_{DD}PEHA		AG18	V_{SS}		AH18	GCLKN1	
AE19	V_{SS}		AF19	V_{SS}		AG19	V_{SS}		AH19	V_{SS}	
AE20	V_{DD}PETA		AF20	V_{SS}		AG20	V_{DD}PETA		AH20	REFRES12	
AE21	V_{SS}		AF21	V_{DD}PEA		AG21	NC		AH21	V_{SS}	
AE22	V_{DD}PEHA		AF22	V_{SS}		AG22	V_{DD}PEHA		AH22	NC	
AE23	V_{SS}		AF23	V_{SS}		AG23	V_{SS}		AH23	REFRES13	
AE24	V_{SS}		AF24	V_{SS}		AG24	V_{SS}		AH24	V_{SS}	
AE25	GPIO_06		AF25	V_{SS}		AG25	V_{SS}		AH25	V_{SS}	
AE26	V_{DD}I/O		AF26	GPIO_09	1	AG26	V_{DD}I/O		AH26	V_{SS}	
AE27	V_{SS}		AF27	V_{SS}		AG27	GPIO_04	1	AH27	V_{SS}	
AE28	V_{SS}		AF28	V_{SS}		AG28	V_{SS}		AH28	V_{SS}	
AE29	V_{SS}		AF29	V_{SS}		AG29	V_{SS}		AH29	V_{SS}	
AE30	PE14RP2		AF30	V_{SS}		AG30	PE14RP1		AH30	PE14RP0	
AE31	PE14RN2		AF31	V_{SS}		AG31	PE14RN1		AH31	PE14RN0	
AE32	V_{SS}		AF32	V_{SS}		AG32	V_{SS}		AH32	V_{SS}	
AE33	PE14TN2		AF33	V_{SS}		AG33	PE14TN1		AH33	PE14TN0	
AE34	PE14TP2		AF34	V_{SS}		AG34	PE14TP1		AH34	PE14TP0	

Table 23 PES64H16G2 1156-pin Signal Pin-Out (Part 7 of 9)

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Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt
AJ1	PE05TP3		AK1	V_{SS}		AL1	V_{DD}I/O		AM1	P23MERGEN	
AJ2	PE05TN3		AK2	V_{SS}		AL2	P01MERGEN		AM2	P67MERGEN	
AJ3	V_{SS}		AK3	V_{SS}		AL3	P45MERGEN		AM3	P1415MERGEN	
AJ4	PE05RN3		AK4	V_{SS}		AL4	V_{DD}I/O		AM4	P1011MERGEN	
AJ5	PE05RP3		AK5	V_{SS}		AL5	P89MERGEN		AM5	SWMODE_3	
AJ6	V_{SS}		AK6	V_{SS}		AL6	V_{SS}		AM6	V_{SS}	
AJ7	V_{SS}		AK7	PE06RP0		AL7	PE06RN0		AM7	V_{SS}	
AJ8	V_{SS}		AK8	PE06RP1		AL8	PE06RN1		AM8	V_{SS}	
AJ9	V_{SS}		AK9	V_{SS}		AL9	V_{SS}		AM9	V_{SS}	
AJ10	V_{SS}		AK10	PE06RP2		AL10	PE06RN2		AM10	V_{SS}	
AJ11	V_{SS}		AK11	PE06RP3		AL11	PE06RN3		AM11	V_{SS}	
AJ12	V_{SS}		AK12	V_{SS}		AL12	V_{SS}		AM12	V_{SS}	
AJ13	V_{SS}		AK13	PE07RP0		AL13	PE07RN0		AM13	V_{SS}	
AJ14	NC		AK14	PE07RP1		AL14	PE07RN1		AM14	V_{SS}	
AJ15	V_{SS}		AK15	V_{SS}		AL15	V_{SS}		AM15	V_{SS}	
AJ16	REFRES07		AK16	PE07RP2		AL16	PE07RN2		AM16	V_{SS}	
AJ17	V_{SS}		AK17	PE07RP3		AL17	PE07RN3		AM17	V_{SS}	
AJ18	V_{SS}		AK18	V_{SS}		AL18	V_{SS}		AM18	V_{SS}	
AJ19	V_{SS}		AK19	PE12RP0		AL19	PE12RN0		AM19	V_{SS}	
AJ20	V_{SS}		AK20	PE12RP1		AL20	PE12RN1		AM20	V_{SS}	
AJ21	V_{SS}		AK21	V_{SS}		AL21	V_{SS}		AM21	V_{SS}	
AJ22	V_{SS}		AK22	PE12RP2		AL22	PE12RN2		AM22	V_{SS}	
AJ23	V_{SS}		AK23	PE12RP3		AL23	PE12RN3		AM23	V_{SS}	
AJ24	V_{SS}		AK24	V_{SS}		AL24	V_{SS}		AM24	V_{SS}	
AJ25	V_{SS}		AK25	PE13RP0		AL25	PE13RN0		AM25	V_{SS}	
AJ26	V_{SS}		AK26	PE13RP1		AL26	PE13RN1		AM26	V_{SS}	
AJ27	V_{SS}		AK27	V_{SS}		AL27	V_{SS}		AM27	V_{SS}	
AJ28	V_{SS}		AK28	PE13RP2		AL28	PE13RN2		AM28	V_{SS}	
AJ29	V_{SS}		AK29	PE13RP3		AL29	PE13RN3		AM29	V_{SS}	
AJ30	V_{SS}		AK30	V_{SS}		AL30	V_{SS}		AM30	V_{SS}	
AJ31	V_{SS}		AK31	GPIO_08	1	AL31	GPIO_07		AM31	GPIO_00	1
AJ32	V_{SS}		AK32	GPIO_15	1	AL32	V_{DD}I/O		AM32	GPIO_05	2
AJ33	V_{SS}		AK33	GPIO_14	1	AL33	GPIO_10	1	AM33	GPIO_11	1
AJ34	V_{SS}		AK34	V_{DD}I/O		AL34	GPIO_12	1	AM34	GPIO_13	1

Table 23 PES64H16G2 1156-pin Signal Pin-Out (Part 8 of 9)

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Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt
AN1	V_{SS}		AN18	V_{SS}		AP1	V_{SS}		AP18	V_{SS}	
AN2	V_{DD}I/O		AN19	PE12TN0		AP2	V_{SS}		AP19	PE12TP0	
AN3	P1213MERGEN		AN20	PE12TN1		AP3	RSTHALT		AP20	PE12TP1	
AN4	SWMODE_0		AN21	V_{SS}		AP4	SWMODE_1		AP21	V_{SS}	
AN5	SWMODE_2		AN22	PE12TN2		AP5	V_{DD}I/O		AP22	PE12TP2	
AN6	V_{SS}		AN23	PE12TN3		AP6	V_{SS}		AP23	PE12TP3	
AN7	PE06TN0		AN24	V_{SS}		AP7	PE06TP0		AP24	V_{SS}	
AN8	PE06TN1		AN25	PE13TN0		AP8	PE06TP1		AP25	PE13TP0	
AN9	V_{SS}		AN26	PE13TN1		AP9	V_{SS}		AP26	PE13TP1	
AN10	PE06TN2		AN27	V_{SS}		AP10	PE06TP2		AP27	V_{SS}	
AN11	PE06TN3		AN28	PE13TN2		AP11	PE06TP3		AP28	PE13TP2	
AN12	V_{SS}		AN29	PE13TN3		AP12	V_{SS}		AP29	PE13TP3	
AN13	PE07TN0		AN30	V_{SS}		AP13	PE07TP0		AP30	V_{SS}	
AN14	PE07TN1		AN31	GPIO_01	1	AP14	PE07TP1		AP31	V_{DD}I/O	
AN15	V_{SS}		AN32	GPIO_02	1	AP15	V_{SS}		AP32	GPIO_03	1
AN16	PE07TN2		AN33	V_{DD}I/O		AP16	PE07TP2		AP33	V_{SS}	
AN17	PE07TN3		AN34	V_{SS}		AP17	PE07TP3		AP34	V_{SS}	

Table 23 PES64H16G2 1156-pin Signal Pin-Out (Part 9 of 9)

Alternate Signal Functions

Pin	GPIO	1st Alternate	2nd Alternate	Pin	GPIO	1st Alternate	2nd Alternate
AM31	GPIO_00	PART0PERSTN	—	B4	GPIO_17	HP0RSTN	—
AN31	GPIO_01	PART1PERSTN	—	B3	GPIO_18	HP1APN	—
AN32	GPIO_02	PART2PERSTN	—	A3	GPIO_19	HP1PDN	—
AP32	GPIO_03	PART3PERSTN		H8	GPIO_20	HP1PFN	—
AG27	GPIO_04	—	P0LINKUPN	C3	GPIO_21	HP1PWRGDN	—
AM32	GPIO_05	GPEN	P0ACTIVEN	K10	GPIO_22	HP1MRLN	P1LINKUPN
AK31	GPIO_08	IOEXPINTN	—	D4	GPIO_23	HP1AIN	P1ACTIVEN
AF26	GPIO_09	HP0APN	—	E4	GPIO_24	HP1PIN	P2LINKUPN
AL33	GPIO_10	HP0PDN	—	J9	GPIO_25	HP1PEP	P2ACTIVEN
AM33	GPIO_11	HP0PFN	—	D2	GPIO_26	HP1RSTN	P3LINKUPN
AL34	GPIO_12	HP0PWRGDN	—	C2	GPIO_27	HP2APN	P3ACTIVEN
AM34	GPIO_13	HP0MRLN	—	D1	GPIO_28	HP2PDN	P4LINKUPN
AK33	GPIO_14	HP0AIN	—	C1	GPIO_29	HP2PFN	P4ACTIVEN
AK32	GPIO_15	HP0PIN	—	E2	GPIO_30	HP2PWRGDN	P5LINKUPN
C4	GPIO_16	HP0PEP	—	E3	GPIO_31	HP2MRLN	P5ACTIVEN

Table 24 PES64H16G2 Alternate Signal Functions

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Power Pins

V_{DD}Core	V_{DD}Core	V_{DD}I/O	V_{DD}PEA	V_{DD}PEA	V_{DD}PEHA	V_{DD}PETA
N13	V19	A4	J14	V11	H13	H15
N14	V21	A30	J21	V12	H22	H20
N15	V22	B2	L13	V23	J17	K15
N17	W13	B33	L14	V24	J18	K20
N19	W14	D3	L15	Y11	K13	R8
N20	W16	D31	L17	Y12	K17	R10
N21	W18	D34	L18	Y23	K18	R25
N22	W20	E1	L20	Y24	K22	R27
P13	Y13	H9	L21	AA9	N8	Y8
P15	Y15	H27	L22	AA11	N10	Y10
P17	Y17	J26	M13	AA24	N25	Y25
P19	Y19	K9	M15	AA26	N27	Y27
P21	Y21	AE9	M17	AB11	U9	AE15
P22	Y22	AE10	M18	AB12	U10	AE20
R13	AA13	AE26	M20	AB23	U25	AG15
R14	AA14	AF9	M22	AB24	U26	AG20
R16	AA16	AF10	N11	AC13	V9	
R18	AA18	AG8	N12	AC15	V10	
R20	AA20	AG9	N23	AC17	V25	
R22	AA22	AG26	N24	AC18	V26	
T15	AB13	AK34	P9	AC20	AB8	
T17	AB14	AL1	P11	AC22	AB10	
T19	AB15	AL4	P24	AD13	AB25	
T21	AB16	AL32	P26	AD14	AB27	
T22	AB18	AN2	R11	AD15	AE13	
U13	AB20	AN33	R12	AD17	AE17	
U14	AB21	AP5	R23	AD18	AE18	
U16	AB22	AP31	R24	AD20	AE22	
U18			U11	AD21	AF17	
U20			U12	AD22	AF18	
V15			U23	AF14	AG13	
V17			U24	AF21	AG22	

Table 25 PES64H16G2 Power Pins

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Ground Pins

V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}
A1	C16	E33	G11	J3	L3	M16	P32
A2	C17	E34	G13	J4	L6	M19	P33
A5	C18	F1	G14	J5	L7	M21	P34
A8	C19	F2	G16	J6	L8	M23	R1
A11	C20	F3	G20	J7	L9	M24	R2
A14	C21	F4	G21	J8	L10	M25	R3
A17	C22	F5	G23	J10	L11	M26	R4
A20	C23	F6	G24	J11	L12	M27	R5
A23	C24	F7	G25	J12	L16	M29	R6
A26	C25	F8	G26	J13	L19	M32	R9
A29	C26	F9	G28	J16	L23	N3	R15
A33	C27	F11	G29	J19	L24	N6	R17
A34	C28	F12	G32	J20	L25	N9	R19
B1	C29	F13	H3	J22	L26	N16	R21
B5	D5	F14	H6	J23	L27	N18	R26
B8	D8	F15	H7	J24	L28	N26	R28
B11	D11	F16	H10	J28	L29	N29	R32
B14	D14	F18	H11	J29	L30	N32	T3
B17	D17	F20	H12	J32	L31	P3	T7
B20	D20	F21	H14	K3	L32	P6	T8
B23	D23	F22	H16	K6	L33	P7	T10
B26	D26	F23	H17	K7	L34	P8	T11
B29	D29	F24	H18	K8	M1	P10	T12
B34	E5	F25	H19	K11	M2	P12	T13
C5	E8	F26	H23	K12	M3	P14	T14
C6	E11	F27	H24	K14	M4	P16	T16
C7	E14	F28	H25	K16	M5	P18	T18
C8	E17	F29	H29	K19	M6	P20	T20
C9	E20	F32	H30	K21	M7	P23	T23
C10	E23	G3	H31	K23	M8	P25	T24
C11	E26	G6	H32	K24	M9	P27	T25
C12	E29	G7	H33	K27	M10	P28	T26
C13	E30	G8	H34	K28	M11	P29	T27
C14	E31	G9	J1	K29	M12	P30	T28
C15	E32	G10	J2	K32	M14	P31	T32

Table 26 PES64H16G2 Ground Pins (Part 1 of 3)

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V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}
U3	W12	AA19	AC33	AE32	AG19	AJ19	AL27
U6	W15	AA21	AC34	AF3	AG23	AJ20	AL30
U8	W17	AA23	AD1	AF6	AG24	AJ21	AM6
U15	W19	AA25	AD2	AF7	AG25	AJ22	AM7
U17	W21	AA27	AD3	AF8	AG28	AJ23	AM8
U19	W22	AA28	AD4	AF11	AG29	AJ24	AM9
U21	W23	AA32	AD5	AF12	AG32	AJ25	AM10
U22	W24	AB3	AD6	AF13	AH3	AJ26	AM11
U27	W25	AB9	AD7	AF15	AH6	AJ27	AM12
U29	W27	AB17	AD8	AF16	AH7	AJ28	AM13
U30	W28	AB19	AD11	AF19	AH9	AJ29	AM14
U31	W32	AB26	AD12	AF20	AH10	AJ30	AM15
U32	Y3	AB28	AD16	AF22	AH11	AJ31	AM16
U33	Y9	AB29	AD19	AF23	AH12	AJ32	AM17
U34	Y14	AB32	AD23	AF24	AH13	AJ33	AM18
V1	Y16	AC3	AD24	AF25	AH15	AJ34	AM19
V2	Y18	AC6	AD25	AF27	AH19	AK1	AM20
V3	Y20	AC7	AD26	AF28	AH21	AK2	AM21
V4	Y26	AC8	AD27	AF29	AH24	AK3	AM22
V5	Y28	AC9	AD28	AF30	AH25	AK4	AM23
V6	Y30	AC10	AD29	AF31	AH26	AK5	AM24
V8	Y31	AC11	AD32	AF32	AH27	AK6	AM25
V13	Y32	AC12	AE3	AF33	AH28	AK9	AM26
V14	Y33	AC14	AE6	AF34	AH29	AK12	AM27
V16	Y34	AC16	AE7	AG1	AH32	AK15	AM28
V18	AA1	AC19	AE8	AG2	AJ3	AK18	AM29
V20	AA2	AC21	AE11	AG3	AJ6	AK21	AM30
V27	AA3	AC23	AE12	AG4	AJ7	AK24	AN1
V29	AA4	AC24	AE14	AG5	AJ8	AK27	AN6
V32	AA5	AC25	AE16	AG6	AJ9	AK30	AN9
W3	AA6	AC26	AE19	AG10	AJ10	AL6	AN12
W6	AA7	AC27	AE21	AG11	AJ11	AL9	AN15
W7	AA8	AC28	AE23	AG12	AJ12	AL12	AN18
W8	AA10	AC29	AE24	AG14	AJ13	AL15	AN21
W9	AA12	AC30	AE27	AG16	AJ15	AL18	AN24
W10	AA15	AC31	AE28	AG17	AJ17	AL21	AN27
W11	AA17	AC32	AE29	AG18	AJ18	AL24	AN30

Table 26 PES64H16G2 Ground Pins (Part 2 of 3)

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V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}
AN34	AP2	AP9	AP15	AP21	AP27	AP33	
AP1	AP6	AP12	AP18	AP24	AP30	AP34	

Table 26 PES64H16G2 Ground Pins (Part 3 of 3)

No Connection Pins

NC	NC	NC
G12	U7	AD9
G15	U28	AD10
G19	V7	AG21
G22	V28	AH16
N7	W26	AH22
N28	Y6	AJ14
T6	Y29	
T29	AB7	

Table 27 PES64H16G2 No Connection Pins

Signals Listed Alphabetically

Signal Name	I/O Type	Location	Signal Category
CLKMODE0	I	AG7	System
CLKMODE1	I	K25	
GCLKFSEL	I	AH8	
GCLKN0	I	G17	
GCLKN1	I	AH18	
GCLKP0	I	G18	
GCLKP1	I	AH17	
GPIO_00	I/O	AM31	General Purpose I/O
GPIO_01	I/O	AN31	
GPIO_02	I/O	AN32	
GPIO_03	I/O	AP32	
GPIO_04	I/O	AG27	
GPIO_05	I/O	AM32	
GPIO_06	I/O	AE25	
GPIO_07	I/O	AL31	
GPIO_08	I/O	AK31	

Table 28 89PES64H16G2 Alphabetical Signal List (Part 1 of 11)

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Signal Name	I/O Type	Location	Signal Category
GPIO_09	I/O	AF26	General Purpose I/O (Cont.)
GPIO_10	I/O	AL33	
GPIO_11	I/O	AM33	
GPIO_12	I/O	AL34	
GPIO_13	I/O	AM34	
GPIO_14	I/O	AK33	
GPIO_15	I/O	AK32	
GPIO_16	I/O	C4	
GPIO_17	I/O	B4	
GPIO_18	I/O	B3	
GPIO_19	I/O	A3	
GPIO_20	I/O	H8	
GPIO_21	I/O	C3	
GPIO_22	I/O	K10	
GPIO_23	I/O	D4	
GPIO_24	I/O	E4	
GPIO_25	I/O	J9	
GPIO_26	I/O	D2	
GPIO_27	I/O	C2	
GPIO_28	I/O	D1	
GPIO_29	I/O	C1	
GPIO_30	I/O	E2	
GPIO_31	I/O	E3	
JTAG_TCK	I	K26	Test
JTAG_TDI	I	C31	
JTAG_TDO	O	J25	
JTAG_TMS	I	D30	
JTAG_TRST_N	I	C32	
MSMBADDR_1	I	A31	SMBus Interface
MSMBADDR_2	I	B31	
MSMBADDR_3	I	B30	
MSMBADDR_4	I	C30	
MSMBCLK	I/O	G27	
MSMBDAT	I/O	H26	
MSMBSMODE	I	A32	System
NO CONNECTION	See Table 27 for a listing of No Connect pins.		

Table 28 89PES64H16G2 Alphabetical Signal List (Part 2 of 11)

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Signal Name	I/O Type	Location	Signal Category
P01MERGEN	I	AL2	System
P23MERGEN	I	AM1	
P45MERGEN	I	AL3	
P67MERGEN	I	AM2	
P89MERGEN	I	AL5	
P1011MERGEN	I	AM4	
P1213MERGEN	I	AN3	
P1415MERGEN	I	AM3	
PE00RN0	I	T31	PCI Express
PE00RN1	I	R31	
PE00RN2	I	N31	
PE00RN3	I	M31	
PE00RP0	I	T30	
PE00RP1	I	R30	
PE00RP2	I	N30	
PE00RP3	I	M30	
PE00TN0	O	T33	
PE00TN1	O	R33	
PE00TN2	O	N33	
PE00TN3	O	M33	
PE00TP0	O	T34	
PE00TP1	O	R34	
PE00TP2	O	N34	
PE00TP3	O	M34	
PE01RN0	I	K31	
PE01RN1	I	J31	
PE01RN2	I	G31	
PE01RN3	I	F31	
PE01RP0	I	K30	
PE01RP1	I	J30	
PE01RP2	I	G30	
PE01RP3	I	F30	
PE01TN0	O	K33	
PE01TN1	O	J33	
PE01TN2	O	G33	
PE01TN3	O	F33	

Table 28 89PES64H16G2 Alphabetical Signal List (Part 3 of 11)

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Signal Name	I/O Type	Location	Signal Category
PE01TP0	O	K34	PCI Express (cont.)
PE01TP1	O	J34	
PE01TP2	O	G34	
PE01TP3	O	F34	
PE02RN0	I	D28	
PE02RN1	I	D27	
PE02RN2	I	D25	
PE02RN3	I	D24	
PE02RP0	I	E28	
PE02RP1	I	E27	
PE02RP2	I	E25	
PE02RP3	I	E24	
PE02TN0	O	B28	
PE02TN1	O	B27	
PE02TN2	O	B25	
PE02TN3	O	B24	
PE02TP0	O	A28	
PE02TP1	O	A27	
PE02TP2	O	A25	
PE02TP3	O	A24	
PE03RN0	I	D22	
PE03RN1	I	D21	
PE03RN2	I	D19	
PE03RN3	I	D18	
PE03RP0	I	E22	
PE03RP1	I	E21	
PE03RP2	I	E19	
PE03RP3	I	E18	
PE03TN0	O	B22	
PE03TN1	O	B21	
PE03TN2	O	B19	
PE03TN3	O	B18	
PE03TP0	O	A22	
PE03TP1	O	A21	
PE03TP2	O	A19	
PE03TP3	O	A18	

Table 28 89PES64H16G2 Alphabetical Signal List (Part 4 of 11)

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Signal Name	I/O Type	Location	Signal Category
PE04RN0	I	W4	PCI Express (cont.)
PE04RN1	I	Y4	
PE04RN2	I	AB4	
PE04RN3	I	AC4	
PE04RP0	I	W5	
PE04RP1	I	Y5	
PE04RP2	I	AB5	
PE04RP3	I	AC5	
PE04TN0	O	W2	
PE04TN1	O	Y2	
PE04TN2	O	AB2	
PE04TN3	O	AC2	
PE04TP0	O	W1	
PE04TP1	O	Y1	
PE04TP2	O	AB1	
PE04TP3	O	AC1	
PE05RN0	I	AE4	
PE05RN1	I	AF4	
PE05RN2	I	AH4	
PE05RN3	I	AJ4	
PE05RP0	I	AE5	
PE05RP1	I	AF5	
PE05RP2	I	AH5	
PE05RP3	I	AJ5	
PE05TN0	O	AE2	
PE05TN1	O	AF2	
PE05TN2	O	AH2	
PE05TN3	O	AJ2	
PE05TP0	O	AE1	
PE05TP1	O	AF1	
PE05TP2	O	AH1	
PE05TP3	O	AJ1	
PE06RN0	I	AL7	
PE06RN1	I	AL8	
PE06RN2	I	AL10	
PE06RN3	I	AL11	

Table 28 89PES64H16G2 Alphabetical Signal List (Part 5 of 11)

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Signal Name	I/O Type	Location	Signal Category
PE06RP0	I	AK7	PCI Express (cont.)
PE06RP1	I	AK8	
PE06RP2	I	AK10	
PE06RP3	I	AK11	
PE06TN0	O	AN7	
PE06TN1	O	AN8	
PE06TN2	O	AN10	
PE06TN3	O	AN11	
PE06TP0	O	AP7	
PE06TP1	O	AP8	
PE06TP2	O	AP10	
PE06TP3	O	AP11	
PE07RN0	I	AL13	
PE07RN1	I	AL14	
PE07RN2	I	AL16	
PE07RN3	I	AL17	
PE07RP0	I	AK13	
PE07RP1	I	AK14	
PE07RP2	I	AK16	
PE07RP3	I	AK17	
PE07TN0	O	AN13	
PE07TN1	O	AN14	
PE07TN2	O	AN16	
PE07TN3	O	AN17	
PE07TP0	O	AP13	
PE07TP1	O	AP14	
PE07TP2	O	AP16	
PE07TP3	O	AP17	
PE08RN0	I	D16	
PE08RN1	I	D15	
PE08RN2	I	D13	
PE08RN3	I	D12	
PE08RP0	I	E16	
PE08RP1	I	E15	
PE08RP2	I	E13	
PE08RP3	I	E12	

Table 28 89PES64H16G2 Alphabetical Signal List (Part 6 of 11)

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Signal Name	I/O Type	Location	Signal Category
PE08TN0	O	B16	PCI Express (cont.)
PE08TN1	O	B15	
PE08TN2	O	B13	
PE08TN3	O	B12	
PE08TP0	O	A16	
PE08TP1	O	A15	
PE08TP2	O	A13	
PE08TP3	O	A12	
PE09RN0	I	D10	
PE09RN1	I	D9	
PE09RN2	I	D7	
PE09RN3	I	D6	
PE09RP0	I	E10	
PE09RP1	I	E9	
PE09RP2	I	E7	
PE09RP3	I	E6	
PE09TN0	O	B10	
PE09TN1	O	B9	
PE09TN2	O	B7	
PE09TN3	O	B6	
PE09TP0	O	A10	
PE09TP1	O	A9	
PE09TP2	O	A7	
PE09TP3	O	A6	
PE10RN0	I	G4	
PE10RN1	I	H4	
PE10RN2	I	K4	
PE10RN3	I	L4	
PE10RP0	I	G5	
PE10RP1	I	H5	
PE10RP2	I	K5	
PE10RP3	I	L5	
PE10TN0	O	G2	
PE10TN1	O	H2	
PE10TN2	O	K2	
PE10TN3	O	L2	
PE10TP0	O	G1	

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Signal Name	I/O Type	Location	Signal Category
PE10TP1	O	H1	PCI Express (cont.)
PE10TP2	O	K1	
PE10TP3	O	L1	
PE11RN0	I	N4	
PE11RN1	I	P4	
PE11RN2	I	T4	
PE11RN3	I	U4	
PE11RP0	I	N5	
PE11RP1	I	P5	
PE11RP2	I	T5	
PE11RP3	I	U5	
PE11TN0	O	N2	
PE11TN1	O	P2	
PE11TN2	O	T2	
PE11TN3	O	U2	
PE11TP0	O	N1	
PE11TP1	O	P1	
PE11TP2	O	T1	
PE11TP3	O	U1	
PE12RN0	I	AL19	
PE12RN1	I	AL20	
PE12RN2	I	AL22	
PE12RN3	I	AL23	
PE12RP0	I	AK19	
PE12RP1	I	AK20	
PE12RP2	I	AK22	
PE12RP3	I	AK23	
PE12TN0	O	AN19	
PE12TN1	O	AN20	
PE12TN2	O	AN22	
PE12TN3	O	AN23	
PE12TP0	O	AP19	
PE12TP1	O	AP20	
PE12TP2	O	AP22	
PE12TP3	O	AP23	
PE13RN0	I	AL25	

Table 28 89PES64H16G2 Alphabetical Signal List (Part 8 of 11)

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Signal Name	I/O Type	Location	Signal Category
PE13RN1	I	AL26	PCI Express (cont.)
PE13RN2	I	AL28	
PE13RN3	I	AL29	
PE13RP0	I	AK25	
PE13RP1	I	AK26	
PE13RP2	I	AK28	
PE13RP3	I	AK29	
PE13TN0	O	AN25	
PE13TN1	O	AN26	
PE13TN2	O	AN28	
PE13TN3	O	AN29	
PE13TP0	O	AP25	
PE13TP1	O	AP26	
PE13TP2	O	AP28	
PE13TP3	O	AP29	
PE14RN0	I	AH31	
PE14RN1	I	AG31	
PE14RN2	I	AE31	
PE14RN3	I	AD31	
PE14RP0	I	AH30	
PE14RP1	I	AG30	
PE14RP2	I	AE30	
PE14RP3	I	AD30	
PE14TN0	O	AH33	
PE14TN1	O	AG33	
PE14TN2	O	AE33	
PE14TN3	O	AD33	
PE14TP0	O	AH34	
PE14TP1	O	AG34	
PE14TP2	O	AE34	
PE14TP3	O	AD34	
PE15RN0	I	AB31	
PE15RN1	I	AA31	
PE15RN2	I	W31	
PE15RN3	I	V31	
PE15RP0	I	AB30	

Table 28 89PES64H16G2 Alphabetical Signal List (Part 9 of 11)

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Signal Name	I/O Type	Location	Signal Category
PE15RP1	I	AA30	PCI Express (cont.)
PE15RP2	I	W30	
PE15RP3	I	V30	
PE15TN0	O	AB33	
PE15TN1	O	AA33	
PE15TN2	O	W33	
PE15TN3	O	V33	
PE15TP0	O	AB34	
PE15TP1	O	AA34	
PE15TP2	O	W34	
PE15TP3	O	V34	
PERSTN	I	B32	System
REFRES00	I/O	R29	SerDes Reference Resistors
REFRES01	I/O	M28	
REFRES02	I/O	H21	
REFRES03	I/O	F19	
REFRES04	I/O	Y7	
REFRES05	I/O	AB6	
REFRES06	I/O	AH14	
REFRES07	I/O	AJ16	
REFRES08	I/O	J15	
REFRES09	I/O	F10	
REFRES10	I/O	R7	
REFRES11	I/O	T9	
REFRES12	I/O	AH20	
REFRES13	I/O	AH23	
REFRES14	I/O	AA29	
REFRES15	I/O	W29	
REFRESPLL	I/O	F17	
RSTHALT	I	AP3	System
SSMBADDR_1	I	C34	SMBus Interface
SSMBADDR_2	I	C33	
SSMBADDR_3	I	D33	
SSMBADDR_5	I	D32	
SSMBCLK	I/O	H28	
SSMBDAT	I/O	J27	

Table 28 89PES64H16G2 Alphabetical Signal List (Part 10 of 11)

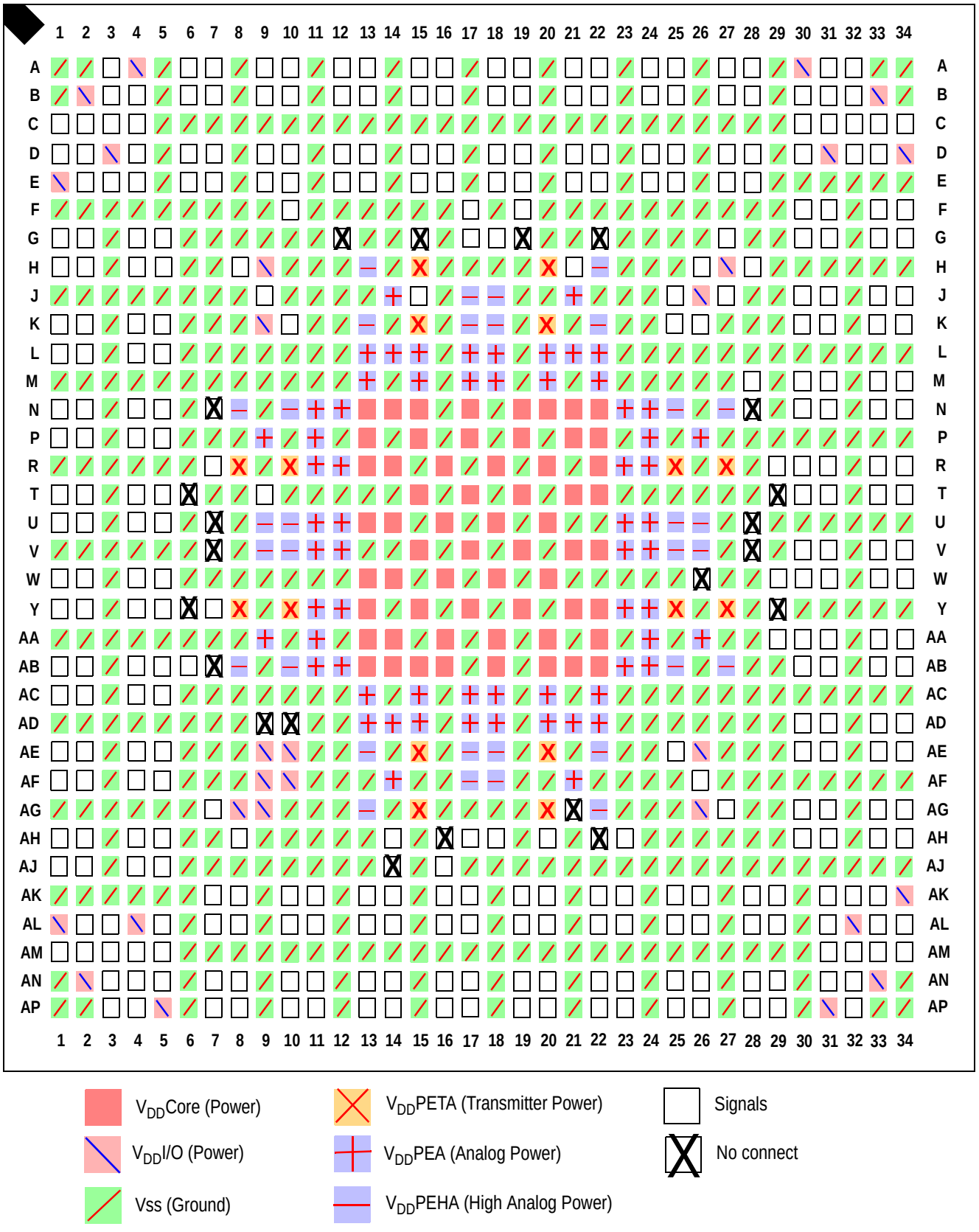
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Signal Name	I/O Type	Location	Signal Category
SWMODE_0	I	AN4	System
SWMODE_1	I	AP4	
SWMODE_2	I	AN5	
SWMODE_3	I	AM5	
V_{DD}CORE, V_{DD}I/O, V_{DD}PEA, V_{DD}PEHA, V_{DD}PETA	See Table 25 for a listing of power pins.		
V_{SS}	See Table 26 for a listing of ground pins.		

Table 28 89PES64H16G2 Alphabetical Signal List (Part 11 of 11)

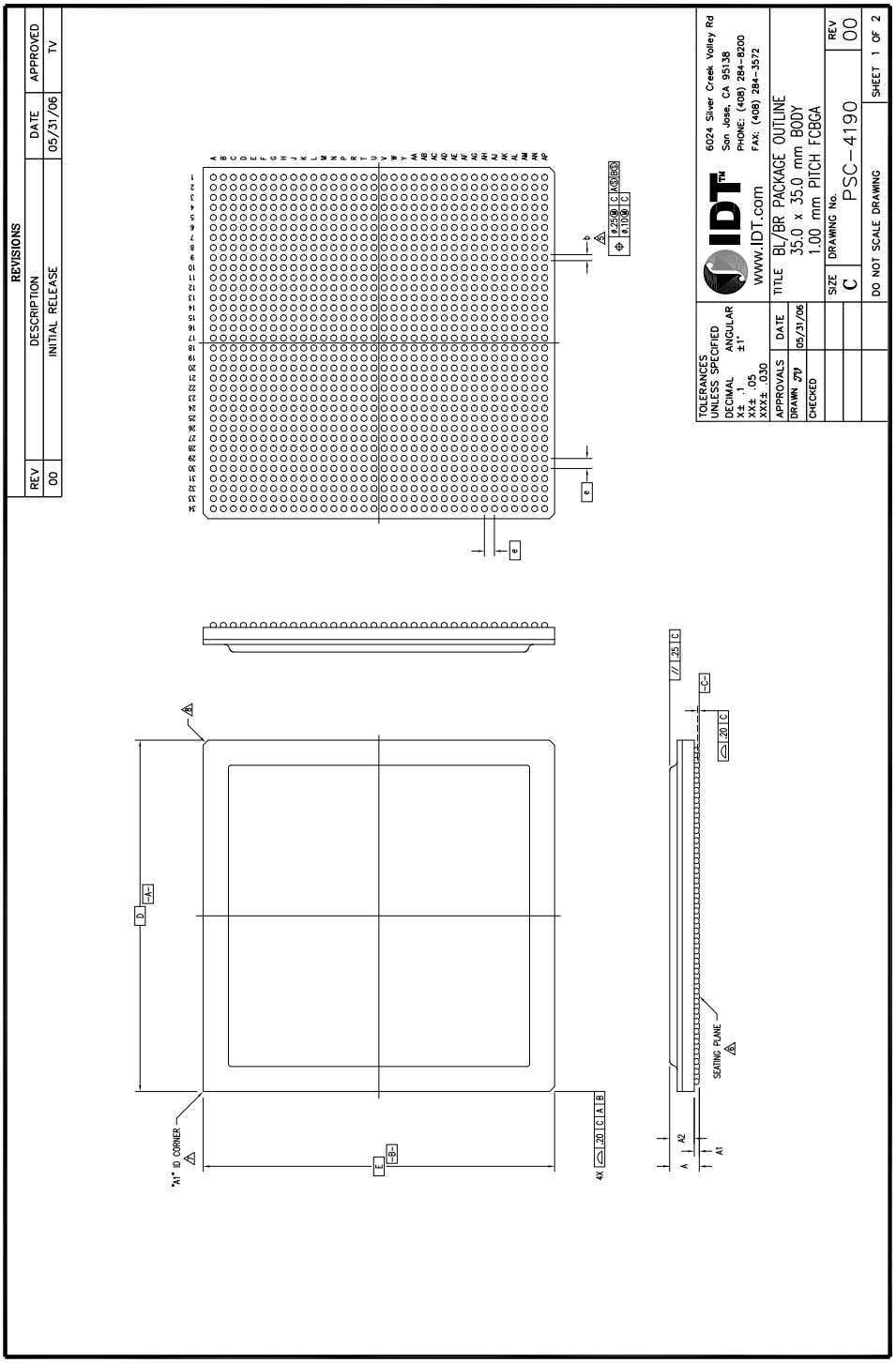
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PES64H16G2 Pinout — Top View



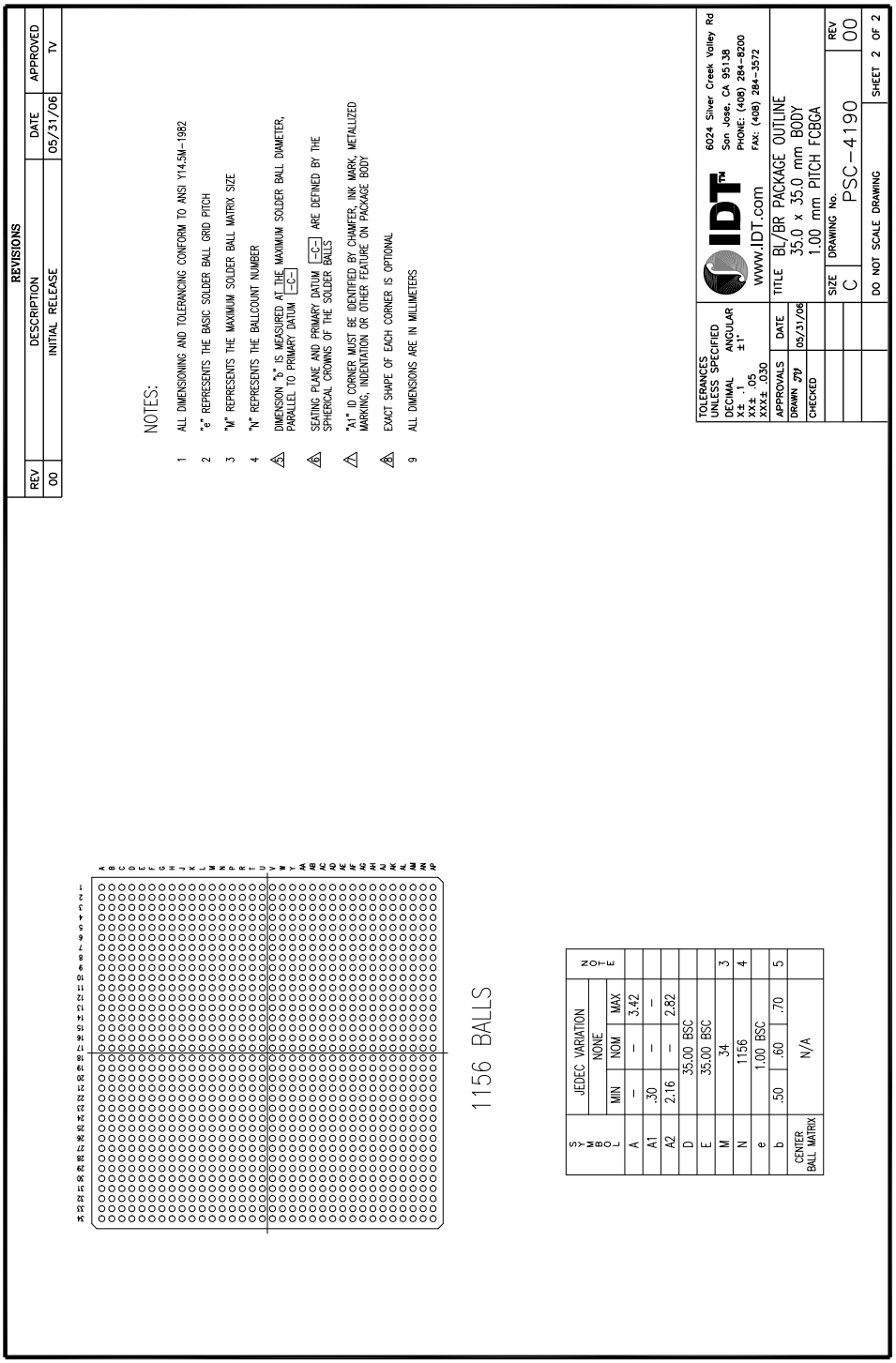
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PES64H16G2 Package Drawing — 1156-Pin BL1156/BR1156



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PES64H16G2 Package Drawing — Page Two



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Revision History

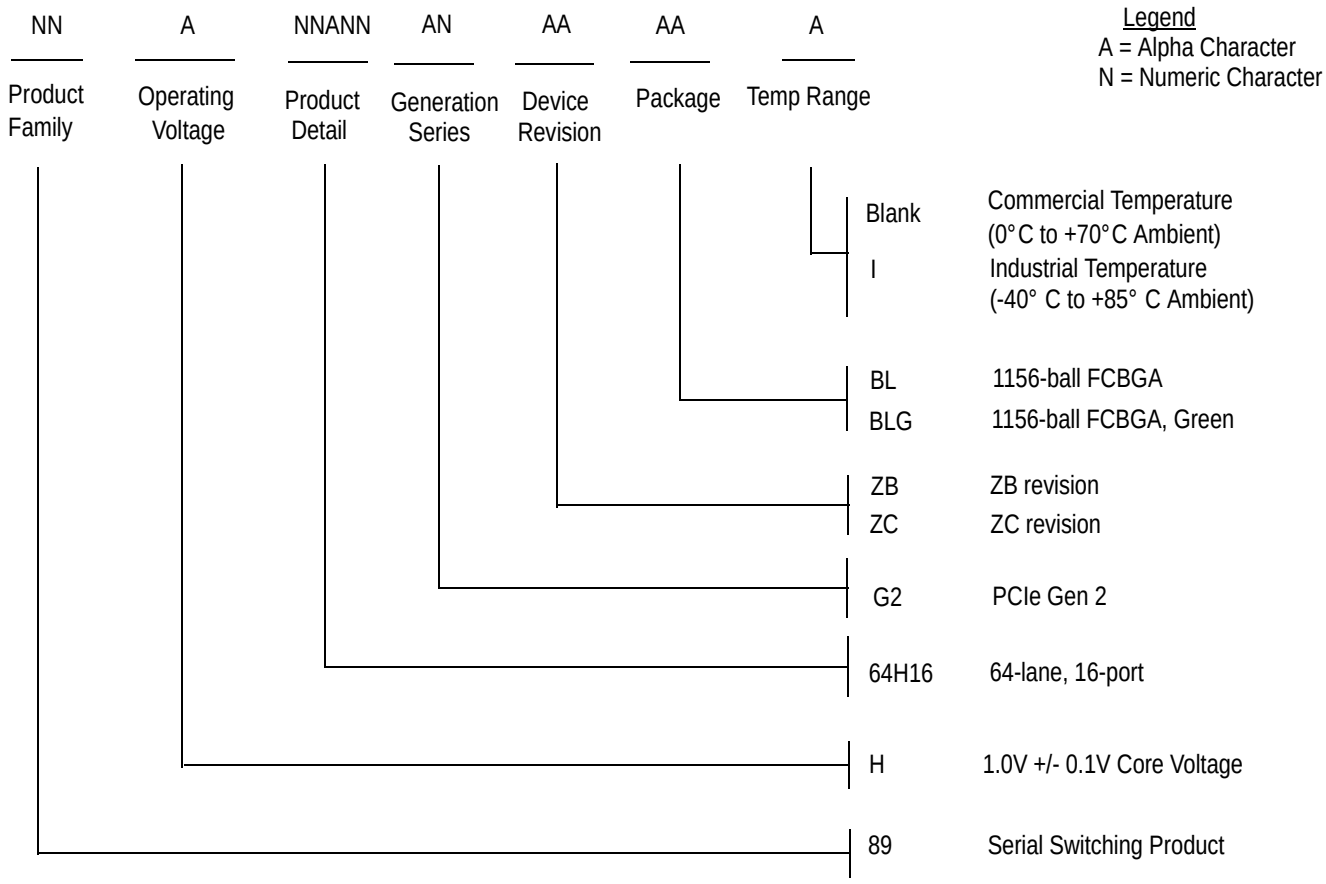
January 21, 2010: Publication of Final data sheet.

March 30, 2011: In Table 14, added V_{DD}PETA to footnote #1.

November 28, 2011: Added new Tables 21 and 22, SMBus Characterization and Timing.

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Ordering Information



Valid Combinations

89H64H16G2ZBBL	1156-ball FCBGA package, Commercial Temperature
89H64H16G2ZBBLG	1156-ball Green FCBGA package, Commercial Temperature
89H64H16G2ZBBLI	1156-ball FCBGA package, Industrial Temperature
89H64H16G2ZBBLGI	1156-ball Green FCBGA package, Industrial Temperature
89H64H16G2ZCBL	1156-ball FCBGA package, Commercial Temperature
89H64H16G2ZCBLG	1156-ball Green FCBGA package, Commercial Temperature
89H64H16G2ZCBLI	1156-ball FCBGA package, Industrial Temperature
89H64H16G2ZCBLGI	1156-ball Green FCBGA package, Industrial Temperature

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