Device Overview

The 89HPES12NT3 is a member of the IDT PRECISE™ family of PCI Express® switching solutions offering the next-generation I/O interconnect standard. The PES12NT3 is a 12-lane, 3-port peripheral chip that performs PCI Express Base switching with a feature set optimized for high performance applications such as servers, storage, and communications/networking. It provides high-performance I/O connectivity and switching functions between a PCIe® upstream port, a transparent downstream port, and a non-transparent downstream port.

With non-transparent bridging (NTB) functionality, the PES12NT3 can be used standalone or as a chipset with IDT PCIe System Interconnect Switches in multi-host and intelligent I/O applications such as communications, storage, and blade servers where inter-domain communication is required.

Features

- **High Performance PCI Express Switch**
  - Twelve PCI Express lanes (2.5Gbps), three switch ports
  - Delivers 48 Gbps (6 GBps) of aggregate switching capacity
  - Low latency cut-through switch architecture
  - Support for Max Payload size up to 2048 bytes
  - Supports one virtual channel and eight traffic classes
  - PCI Express Base specification Revision 1.0a compliant
- **Flexible Architecture with Numerous Configuration Options**
  - Port arbitration schemes utilizing round robin
  - Supports automatic per port link width negotiation (x4, x2, or x1)
  - Static lane reversal on all ports
  - Automatic polarity inversion on all lanes
  - Supports locked transactions, allowing use with legacy software
  - Ability to load device configuration from serial EEPROM
  - Ability to control device via SMBus
- **Non-Transparent Port**
  - Crosslink support on NTB port
  - Four mapping windows supported
    - Each may be configured as a 32-bit memory or I/O window
    - May be paired to form a 64-bit memory window
  - Interprocessor communication
    - Thirty-two inbound and outbound doorbells
    - Four inbound and outbound message registers
    - Two shared scratchpad registers
  - Allows up to sixteen masters to communicate through the non-transparent port
  - No limit on the number of supported outstanding transactions through the non-transparent bridge
  - Completely symmetric non-transparent bridge operation allows similar/same configuration software to be run
  - Supports direct connection to a transparent or non-transparent port of another switch

Block Diagram

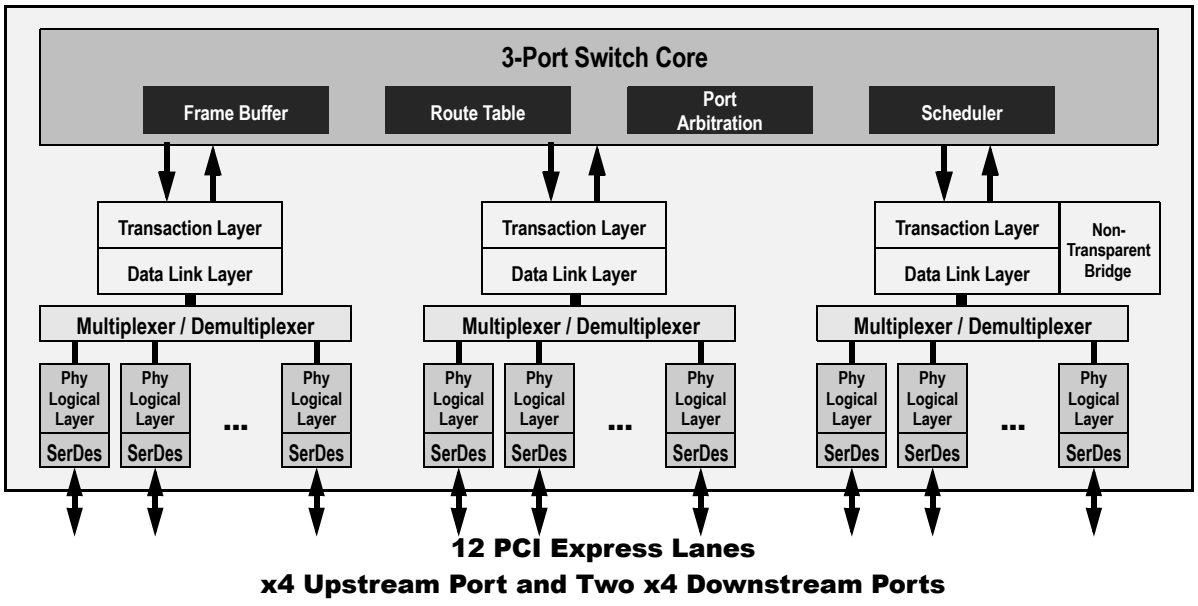


Figure 1 Internal Block Diagram

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- **Highly Integrated Solution**
  - Requires no external components
  - Incorporates on-chip internal memory for packet buffering and queueing
  - Integrates twelve 2.5 Gbps embedded full duplex SerDes, 8B/10B encoder/decoder (no separate transceivers needed)
- **Reliability, Availability, and Serviceability (RAS) Features**
  - Upstream port can be dynamically swapped with non-transparent downstream port to support failover applications
  - Internal end-to-end parity protection on all TLPs ensures data integrity even in systems that do not implement end-to-end CRC (ECRC)
  - Supports ECRC pass-through in transparent and non-transparent ports
  - Supports Hot-Swap
- **Power Management**
  - Supports PCI Power Management Interface specification, Revision 1.1 (PCI-PM)
  - Unused SerDes are disabled
- **Testability and Debug Features**
  - Built in SerDes Pseudo-Random Bit Stream (PRBS) generator
  - Ability to read and write any internal register via the SMBus
  - Ability to bypass link training and force any link into any mode
  - Provides statistics and performance counters
- **Two SMBus Interfaces**
  - Slave interface provides full access to all software-visible registers by an external SMBus master
  - Master interface provides connection for an optional serial EEPROM used for initialization
  - Master and slave interfaces may be tied together so the switch can act as both master and slave
- **Eight General Purpose Input/Output pins**
- **Packaged in 19x19mm 324-ball BGA with 1mm ball spacing**

Product Description

Utilizing standard PCI Express interconnect, the PES12NT3 provides the most efficient high-performance I/O connectivity solution for applications requiring high throughput, low latency, and simple board layout with a minimum number of board layers. With support for non-transparent bridging, the PES12NT3, as a standalone switch or as a chipset with IDT PCIe System Interconnect Switches, enables multi-host and intelligent I/O applications requiring inter-domain communication. The PES12NT3 provides 48 Gbps (6 GBps) of aggregated, full-duplex switching capacity through 12 integrated serial lanes, using proven and robust IDT technology. Each lane provides 2.5 Gbps of bandwidth in both directions and is fully compliant with PCI Express Base specification 1.0a.

The PES12NT3 is based on a flexible and efficient layered architecture. The PCI Express layer consists of SerDes, Physical, Data Link and Transaction layers in compliance with PCI Express Base specification Revision 1.0a. The PES12NT3 can operate either as a store and forward or cut-through switch depending on the packet size and is designed to switch memory and I/O transactions. It supports eight Traffic Classes (TCs) and one Virtual Channel (VC) with sophisticated resource management. This includes round robin port arbitration, guaranteeing bandwidth allocation and/or latency for critical traffic classes in applications such as high throughput 10 GbE I/Os, SATA controllers, and Fibre Channel HBAs.

Switch Configuration

The PES12NT3 is a three port switch that contains 12 PCI Express lanes. Each of the three ports is statically allocated 4 lanes with ports labeled as A, B and C. Port A is the upstream port, port B is the transparent downstream port, and port C is the non-transparent downstream port.

During link training, link width is automatically negotiated. Each PES12NT3 port is capable of independently negotiating to a x4, x2 or x1 width. Thus, the PES12NT3 may be used in virtually any three port switch configuration (e.g., {x4, x4, x4}, {x4, x2, x2}, {x4, x2, x1}, etc.). The PES12NT3 supports static lane reversal. For example, lane reversal for upstream port A may be configured by asserting the PCI Express Port A Lane Reverse (PEALREV) input signal or through serial EEPROM or SMBus initialization. Lane reversal for ports B and C may be enabled via a configuration space register, serial EEPROM, or the SMBus.

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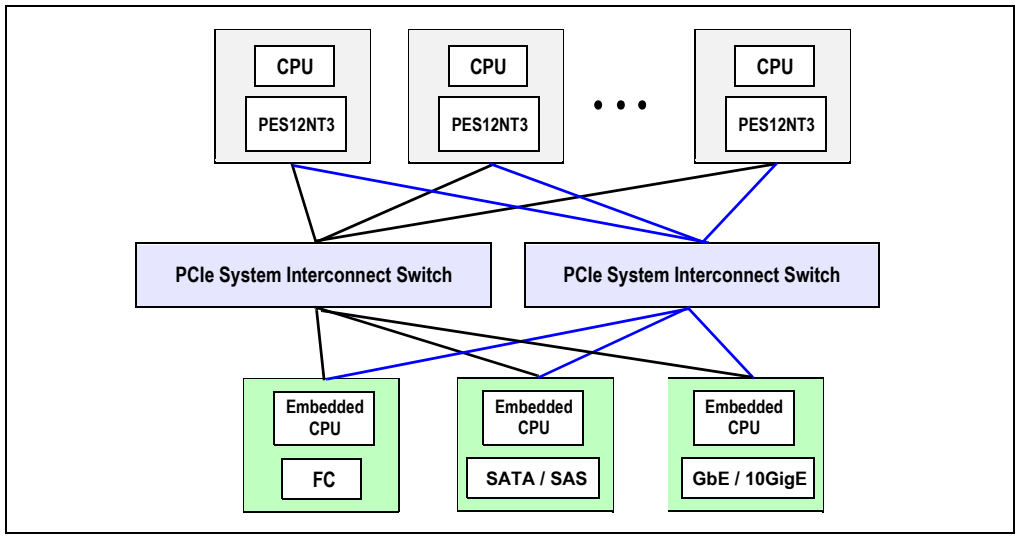


Figure 2 PCIe System Interconnect Architecture Block Diagram

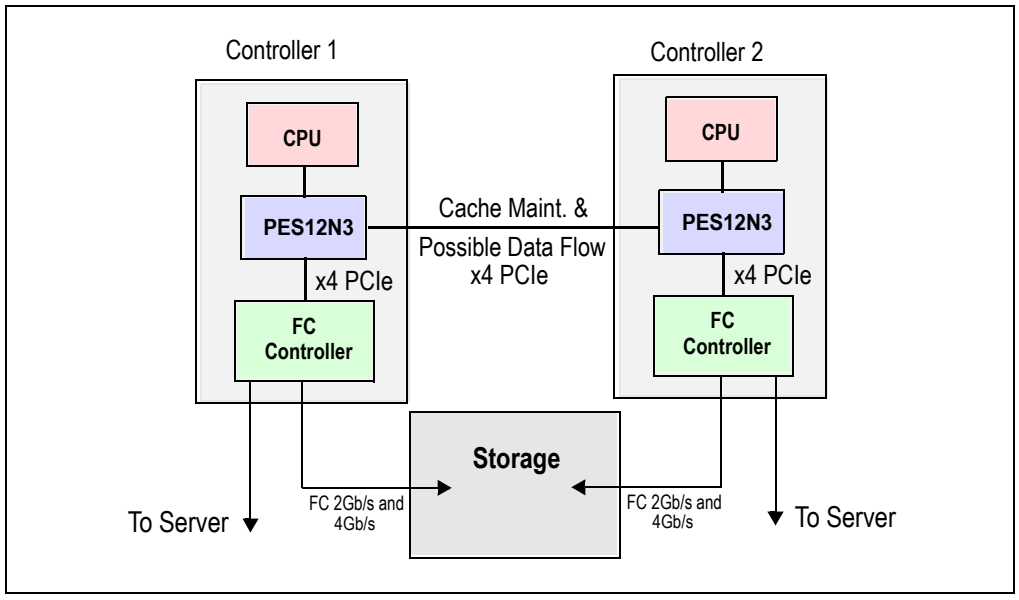


Figure 3 Dual Host Storage System

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Pin Description

The following tables list the functions of the pins provided on the PES12NT3. Some of the functions listed may be multiplexed onto the same pin. The active polarity of a signal is defined using a suffix. Signals ending with an "N" are defined as being active, or asserted, when at a logic zero (low) level. All other signals (including clocks, buses, and select lines) will be interpreted as being active, or asserted, when at a logic one (high) level.

Signal	Type	Name/Description
PEALREV	I	**PCI Express Port A Lane Reverse.** When this bit is asserted, the lanes of PCI Express Port A are reversed. This value may be overridden by modifying the value of the PALREV bit in the PA_SWCTL register.
PEARP[3:0] PEARN[3:0]	I	**PCI Express Port A Serial Data Receive.** Differential PCI Express receive pairs for port A.
PEATP[3:0] PEATN[3:0]	O	**PCI Express Port A Serial Data Transmit.** Differential PCI Express transmit pairs for port A
PEBLREV	I	**PCI Express Port B Lane Reverse.** When this bit is asserted, the lanes of PCI Express Port B are reversed. This value may be overridden by modifying the value of the PBLREV bit in the PA_SWCTL register.
PEBRP[3:0] PEBRN[3:0]	I	**PCI Express Port B Serial Data Receive.** Differential PCI Express receive pairs for port B.
PEBTP[3:0] PEBTN[3:0]	O	**PCI Express Port B Serial Data Transmit.** Differential PCI Express transmit pairs for port B
PECLREV	I	**PCI Express Port C Lane Reverse.** When this bit is asserted, the lanes of PCI Express Port C are reversed. This value may be overridden by modifying the value of the PCLREV bit in the PA_SWCTL register.
PECRP[3:0] PECRN[3:0]	I	**PCI Express Port C Serial Data Receive.** Differential PCI Express receive pairs for port C.
PECTP[3:0] PECTN[3:0]	O	**PCI Express Port C Serial Data Transmit.** Differential PCI Express transmit pairs for port C
PEREFCLKP[1:0] PEREFCLKN[1:0]	I	**PCI Express Reference Clock.** Differential reference clock pair input. This clock is used as the reference clock by on-chip PLLs to generate the clocks required for the system logic and on-chip SerDes. The frequency of the differential reference clock is determined by the REFCLKM signal.
REFCLKM	I	**PCI Express Reference Clock Mode Select.** These signals select the frequency of the reference clock input. 0x0 - 100 MHz 0x1 - 125 MHz

Table 1 PCI Express Interface Pins

Signal	Type	Name/Description
MSMBADDR[4:1]	I	**Master SMBus Address.** These pins determine the SMBus address of the serial EEPROM from which configuration information is loaded.
MSMBCLK	I/O	**Master SMBus Clock.** This bidirectional signal is used to synchronize transfers on the master SMBus. It is active and generating the clock only when the EEPROM is being accessed.
MSMBDAT	I/O	**Master SMBus Data.** This bidirectional signal is used for data on the master SMBus.

Table 2 SMBus Interface Pins (Part 1 of 2)

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Signal	Type	Name/Description
SSMBADDR[5,3:1]	I	**Slave SMBus Address.** These pins determine the SMBus address to which the slave SMBus interface responds.
SSMBCLK	I/O	**Slave SMBus Clock.** This bidirectional signal is used to synchronize transfers on the slave SMBus.
SSMBDAT	I/O	**Slave SMBus Data.** This bidirectional signal is used for data on the slave SMBus.

Table 2 SMBus Interface Pins (Part 2 of 2)

Signal	Type	Name/Description
GPIO[0]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: PEBRSTN Alternate function pin type: Output Alternate function: Reset output for downstream port B
GPIO[1]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: PECRSTN Alternate function pin type: Output Alternate function: Reset output for downstream port C
GPIO[2]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: PALINKUPN Alternate function pin type: Output Alternate function: Port A link up status output
GPIO[3]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: PBLINKUPN Alternate function pin type: Output Alternate function: Port B link up status output
GPIO[4]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: PCLINKUPN Alternate function pin type: Output Alternate function: Port C link up status output
GPIO[5]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: FAILOVERP Alternate function pin type: Input Alternate function: NTB upstream port failover
GPIO[6]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin.
GPIO[7]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin.

Table 3 General Purpose I/O Pins

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Signal	Type	Name/Description
CCLKDS	I	**Common Clock Downstream.** When the CCLKDS pin is asserted, it indicates that a common clock is being used between the downstream device and the downstream port.
CCLKUS	I	**Common Clock Upstream.** When the CCLKUS pin is asserted, it indicates that a common clock is being used between the upstream device and the upstream port.
MSMBSMODE	I	**Master SMBus Slow Mode.** The assertion of this pin indicates that the master SMBus should operate at 100 KHz instead of 400 KHz. This value may not be overridden.
PENTBRSTN	I	**Non-Transparent Bridge Reset.** Assertion of this signal indicates a reset on the external side of the non-transparent bridge. This signal is only used when the switch mode selects a non-transparent mode and has no effect otherwise.
PERSTN	I	**Fundamental Reset.** Assertion of this signal resets all logic inside the PES12NT3 and initiates a PCI Express fundamental reset.
RSTHALT	I	**Reset Halt.** When this signal is asserted during a PCI Express fundamental reset, the PES12NT3 executes the reset procedure and remains in a reset state with the Master and Slave SMBuses active. This allows software to read and write registers internal to the device before normal device operation begins. The device exits the reset state when the RSTHALT bit is cleared in the PA_SWCTL register by an SMBus master.
SWMODE[3:0]	I	**Switch Mode.** These configuration pins determine the PES12NT3 switch operating mode. 0x0 - Reserved 0x1 - Reserved 0x2 - Non-transparent mode 0x3 - Non-transparent mode with serial EEPROM initialization 0x4 - Non-transparent failover mode 0x5 - Non-transparent failover mode with serial EEPROM initialization 0x6 through 0xF - Reserved

Table 4 System Pins

Signal	Type	Name/Description
JTAG_TCK	I	**JTAG Clock**. This is an input test clock used to clock the shifting of data into or out of the boundary scan logic or JTAG Controller. JTAG_TCK is independent of the system clock with a nominal 50% duty cycle.
JTAG_TDI	I	**JTAG Data Input**. This is the serial data input to the boundary scan logic or JTAG Controller.

Table 5 Test Pins (Part 1 of 2)

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Signal	Type	Name/Description
JTAG_TDO	O	**JTAG Data Output**. This is the serial data shifted out from the boundary scan logic or JTAG Controller. When no data is being shifted out, this signal is tri-stated.
JTAG_TMS	I	**JTAG Mode**. The value on this signal controls the test mode select of the boundary scan logic or JTAG Controller.
JTAG_TRST_N	I	**JTAG Reset**. This active low signal asynchronously resets the boundary scan logic and JTAG TAP Controller. An external pull-up on the board is recommended to meet the JTAG specification in cases where the tester can access this signal. However, for systems running in functional mode, one of the following should occur: 1) actively drive this signal low with control logic 2) statically drive this signal low with an external pull-down on the board

Table 5 Test Pins (Part 2 of 2)

Signal	Type	Name/Description
V_{DD}CORE	I	**Core V_{DD}.** Power supply for core logic.
V_{DD}IO	I	**I/O V_{DD}.** LVTTL I/O buffer power supply.
V_{DD}PE	I	**PCI Express Digital Power.** PCI Express digital power used by the digital power of the SerDes.
V_{DD}APE	I	**PCI Express Analog Power.** PCI Express analog power used by the PLL and bias generator.
V_{TT}PE	I	**PCI Express Termination Power.**
V_{SS}	I	Ground.

Table 6 Power and Ground Pins

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Pin Characteristics

Note: Some input pads of the PES12NT3 do not contain internal pull-ups or pull-downs. Unused inputs should be tied off to appropriate levels. This is especially critical for unused control signal inputs which, if left floating, could adversely affect operation. Also, any input pin left floating can cause a slight increase in power consumption.

Function	Pin Name	Type	Buffer	I/O Type	Internal Resistor	Notes
PCI Express Interface	PEALREV	I	LVTTL	Input	pull-down	
	PEARN[3:0]	I	CML	Serial link		
	PEARP[3:0]	I				
	PEATN[3:0]	O				
	PEATP[3:0]	O				
	PEBLREV	I	LVTTL	Input	pull-down	
	PEBRN[3:0]	I	CML	Serial link		
	PEBRP[3:0]	I				
	PEBTN[3:0]	O				
	PEBTP[3:0]	O				
	PECLREV	I	LVTTL	Input	pull-down	
	PECRN[3:0]	I	CML	Serial link		
	PECRP[3:0]	I				
	PECTN[3:0]	O				
	PECTP[3:0]	O				
	PEREFCLKN[1:0]	I	LVPECL/ CML	Diff. Clock Input		Refer to Table 8
	PEREFCLKP[1:0]	I				
	REFCLKM	I	LVTTL	Input	pull-down	
SMBus	MSMBADDR[4:1]	I	LVTTL	Input	pull-up	
	MSMBCLK	I/O		STI		
	MSMBDAT	I/O				
	SSMBADDR[5,3:1]	I		Input	pull-up	
	SSMBCLK	I/O		STI		
	SSMBDAT	I/O				
General Purpose I/O	GPIO[7:0]	I/O	LVTTL	Input, High Drive	pull-up	

Table 7 Pin Characteristics (Part 1 of 2)

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Function	Pin Name	Type	Buffer	I/O Type	Internal Resistor	Notes
System Pins	CCLKDS	I	LVTTL	Input	pull-up	
	CCLKUS	I			pull-up	
	MSMBSMODE	I			pull-down	
	PENTBRSTN	I				
	PERSTN	I				
	RSTHALT	I			pull-down	
	SWMODE[3:0]	I			pull-up	
JTAG	JTAG_TCK	I	LVTTL	STI	pull-up	
	JTAG_TDI	I			pull-up	
	JTAG_TDO	O		Low Drive		
	JTAG_TMS	I		STI	pull-up	
	JTAG_TRST_N	I			pull-up	External pull-down

Table 7 Pin Characteristics (Part 2 of 2)

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Logic Diagram — PES12NT3

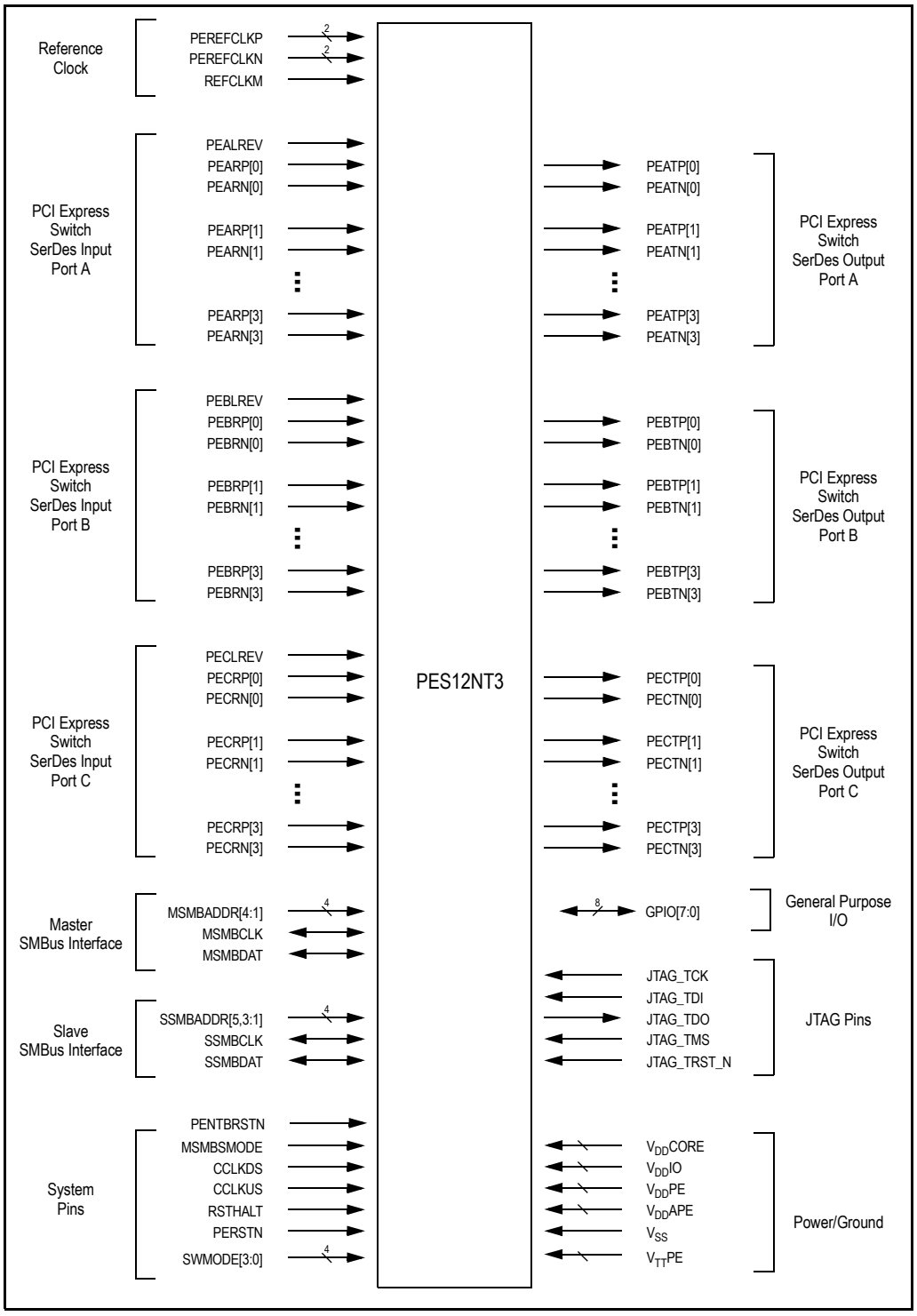


Figure 4 PES12NT3 Logic Diagram

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System Clock Parameters

Values based on systems running at recommended supply voltages and operating temperatures, as shown in Tables 12 and 13.

Parameter	Description	Min	Typical	Max	Unit
$Refclk_{FREQ}$	Input reference clock frequency range	100		125[1]	MHz
$Refclk_{DC}$[2]	Duty cycle of input clock	40	50	60	%
T_R, T_F	Rise/Fall time of input clocks			0.2*RCUI	RCUI[3]
V_{SW}	Differential input voltage swing[4]	0.6		1.6	V
T_{jitter}	Input clock jitter (cycle-to-cycle)			125	ps
R_T	Termination Resistor		110		Ohms

Table 8 Input Clock Requirements

1. The input clock frequency will be either 100 or 125 MHz depending on signal REFCLKM.
2. ClkIn must be AC coupled. Use 0.01 — 0.1 µF ceramic capacitors.
3. RCUI (Reference Clock Unit Interval) refers to the reference clock period.
4. AC coupling required.

AC Timing Characteristics

Parameter	Description	Min[1]	Typical[1]	Max[1]	Units
PCIe Transmit					
UI	Unit Interval	399.88	400	400.12	ps
T_{TX-EYE}	Minimum Tx Eye Width	0.7	.9		UI
$T_{TX-EYE-MEDIAN-to-MAX-JITTER}$	Maximum time between the jitter median and maximum deviation from the median			0.15	UI
$T_{TX-RISE}$, $T_{TX-FALL}$	D+ / D- Tx output rise/fall time	50	90		ps
$T_{TX- IDLE-MIN}$	Minimum time in idle	50			UI
$T_{TX-IDLE-SET-TO-IDLE}$	Maximum time to transition to a valid Idle after sending an Idle ordered set			20	UI
$T_{TX-IDLE-TO-DIFF-DATA}$	Maximum time to transition from valid idle to diff data			20	UI
$T_{TX-IDLE-RCV-DET-MAX}$	Max time spend in idle before initiating a RX detect sequence		20	100	ms
$T_{TX-SKEW}$	Transmitter data skew between any 2 lanes		500	1300	ps
PCIe Receive					
UI	Unit Interval	399.88	400	400.12	ps
T_{RX-EYE} (with jitter)	Minimum Receiver Eye Width (jitter tolerance)	0.4			UI

Table 9 PCIe AC Timing Characteristics (Part 1 of 2)

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Parameter	Description	Min[1]	Typical[1]	Max[1]	Units
$T_{RX-EYE-MEDIUM\ TO\ MAX\ JITTER}$	Max time between jitter median & max deviation			0.3	UI
$T_{RX-IDLE-DET-DIFF-ENTER\ TIME}$	Unexpected Idle Enter Detect Threshold Integration Time			10	ms
$T_{RX-SKEW}$	Lane to lane input skew			20	ns

Table 9 PCIe AC Timing Characteristics (Part 2 of 2)

1. Minimum, Typical, and Maximum values meet the requirements under PCI Specification 1.0a

Signal	Symbol	Reference Edge	Min	Max	Unit	Timing Diagram Reference
GPIO						
GPIO[7:0][1]	Tpw_13b[2]	None	50	—	ns	

Table 10 GPIO AC Timing Characteristics

1. GPIO signals must meet the setup and hold times if they are synchronous or the minimum pulse width if they are asynchronous.
2. The values for this symbol were determined by calculation, not by testing.

Signal	Symbol	Reference Edge	Min	Max	Unit	Timing Diagram Reference
JTAG						
JTAG_TCK	Tper_16a	none	50.0	—	ns	See Figure 5.
	Thigh_16a, Tlow_16a		10.0	25.0	ns	
JTAG_TMS[1], JTAG_TDI	Tsu_16b	JTAG_TCK rising	2.4	—	ns	
	Thld_16b		1.0	—	ns	
JTAG_TDO	Tdo_16c	JTAG_TCK falling	—	20	ns	
	Tdz_16c[2]		—	20	ns	
JTAG_TRST_N	Tpw_16d[2]	none	25.0	—	ns	

Table 11 JTAG AC Timing Characteristics

1. The JTAG specification, IEEE 1149.1, recommends that JTAG_TMS should be held at 1 while the signal applied at JTAG_TRST_N changes from 0 to 1. Otherwise, a race may occur if JTAG_TRST_N is deasserted (going from low to high) on a rising edge of JTAG_TCK when JTAG_TMS is low, because the TAP controller might go to either the Run-Test/Idle state or stay in the Test-Logic-Reset state.
2. The values for this symbol were determined by calculation, not by testing.

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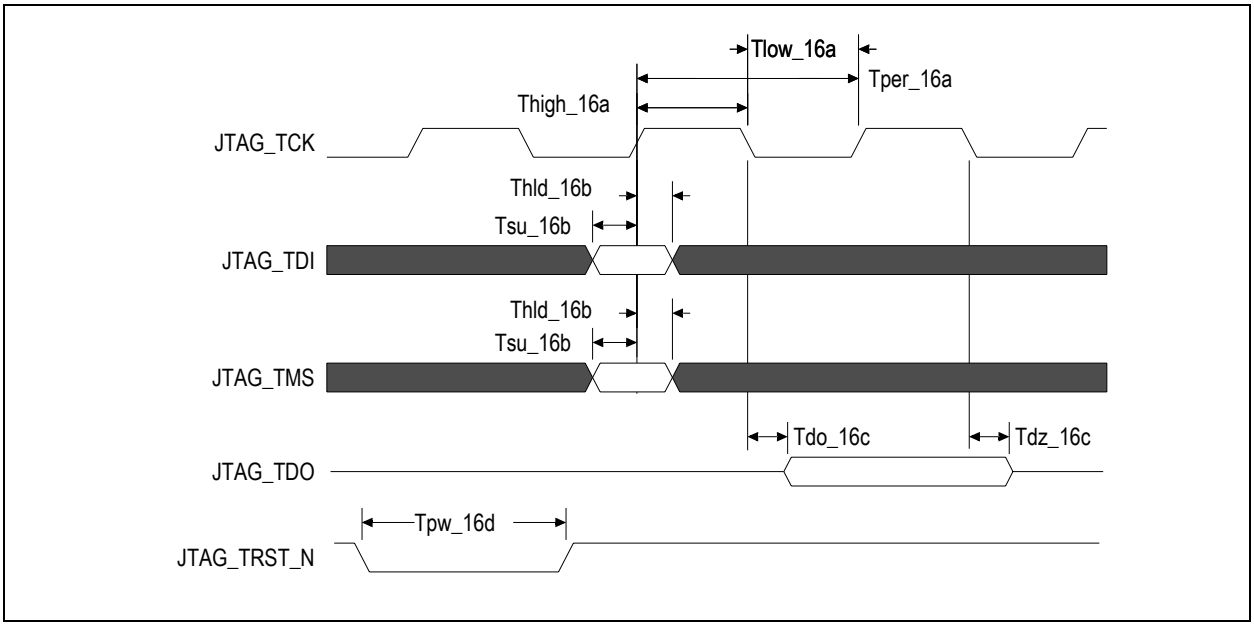


Figure 5 JTAG AC Timing Waveform

Recommended Operating Supply Voltages

Symbol	Parameter	Minimum	Typical	Maximum	Unit
V_{DD}CORE	Internal logic supply	0.9	1.0	1.1	V
V_{DD}I/O	I/O supply except for SerDes LVPECL/CML	3.0	3.3	3.6	V
V_{DD}PE	PCI Express Digital Power	0.9	1.0	1.1	V
V_{DD}APE	PCI Express Analog Power	0.9	1.0	1.1	V
V_{TT}PE	PCI Express Serial Data Transmit Termination Voltage	1.425	1.5	1.575	V
V_{SS}	Common ground	0	0	0	V

Table 12 PES12NT3 Operating Voltages

Recommended Operating Temperature

Grade	Temperature
Commercial	0°C to +70°C Ambient
Industrial	-40°C to +85°C Ambient

Table 13 PES12NT3 Operating Temperatures

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Power-Up Sequence

This section describes the sequence in which various voltages must be applied to the part during power-up to ensure proper functionality. For the PES12NT3, the power-up sequence must be as follows:

1. V_{DD}I/O — 3.3V
2. V_{DD}Core, V_{DD}PE, V_{DD}APE — 1.0V
3. V_{TT}PE — 1.5V

When powering up, each voltage level must ramp and stabilize prior to applying the next voltage in the sequence to ensure internal latch-up issues are avoided. There are no maximum time limitations in ramping to valid power levels. The power-down sequence must be in the reverse order of the power-up sequence.

Power Consumption

Typical power is measured under the following conditions: 25°C Ambient, 35% total link usage on all ports, typical voltages defined in Table 14.

Maximum power is measured under the following conditions: 70°C Ambient, 85% total link usage on all ports, maximum voltages defined in Table 14.

All power measurements assume that the part is mounted on a 10 layer printed circuit board with 0 LFM airflow.

Number of Connected Lanes: Port-A/Port-B/Port-C	Core (Watts) (1.0V supply)		PCIe Digital (Watts) (1.0V supply)		PCIe Analog (Watts) (1.0V supply)		PCIe Termination (Watts) (1.5V supply)		I/O (Watts) (3.3V supply)		Total (Watts)	
	Typ	Max	Typ	Max	Typ	Max	Typ	Max	Typ	Max	Typ	Max
1/1/1	0.52	0.67	0.27	0.36	0.13	0.16	0.11	0.13	0.01	0.01	1.04	1.33
4/1/1	0.56	0.76	0.47	0.58	0.19	0.21	0.22	0.26	0.01	0.01	1.44	1.81
4/4/4	0.65	0.89	0.68	0.81	0.21	0.25	0.38	0.51	0.01	0.01	1.92	2.47

Table 14 PES12NT3 Power Consumption

Thermal Considerations

This section describes thermal considerations for the PES12NT3 (19mm^2 BCG324 package). The data in Table 15 below contains information that is relevant to the thermal performance of the PES12NT3 switch.

Symbol	Parameter	Value	Units	Conditions
$T_{J(max)}$	Junction Temperature	125	°C	Maximum
$T_{A(max)}$	Ambient Temperature	70	°C	Maximum for commercial-rated products
$\theta_{JA(effective)}$	Effective Thermal Resistance, Junction-to-Ambient	21.8	°C/W	Zero air flow
		15.1	°C/W	1 m/S air flow
		13.9	°C/W	2 m/S air flow
θ_{JB}	Thermal Resistance, Junction-to-Board	11.4	°C/W	
θ_{JC}	Thermal Resistance, Junction-to-Case	5.1	°C/W	
P	Power Dissipation of the Device	2.47	Watts	Maximum

Table 15 Thermal Specifications for PES12NT3, 19x19mm BCG324 Package

Note: The parameter $\theta_{JA(eff)}$ is not the *absolute* thermal resistance for the package as defined by JEDEC (JESD-51). Because resistance can vary with the number of board layers, size of the board, and airflow, $\theta_{JA(eff)}$ is the *effective* thermal resistance. The values for effective θ_{JA} given above are based on a 10-layer, standard height, full length (4.3"x12.2") PCIe add-in card.

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DC Electrical Characteristics

Values based on systems running at recommended supply voltages, as shown in Table 12.

Note: See Table 7, Pin Characteristics, for a complete I/O listing.

I/O Type	Parameter	Description	Min[1]	Typ[1]	Max[1]	Unit	Conditions
Serial Link	**PCIe Transmit**						
	$V_{TX-DIFFp-p}$	Differential peak-to-peak output voltage	800		1200	mV	
	$V_{TX-DE-RATIO}$	De-emphasized differential output voltage	-3		-4	dB	
	$V_{TX-DC-CM}$	DC Common mode voltage	-0.1	1	3.7	V	
	$V_{TX-CM-ACP}$	RMS AC peak common mode output voltage			20	mV	
	$V_{TX-CM-DC-active-idle-delta}$	Abs delta of DC common mode voltage between L0 and idle			100	mV	
	$V_{TX-CM-DC-line-delta}$	Abs delta of DC common mode voltage between D+ and D-			25	mV	
	$V_{TX-Idle-DiffP}$	Electrical idle diff peak output			20	mV	
	$V_{TX-RCV-Detect}$	Voltage change during receiver detection			600	mV	
	$RL_{TX-DIFF}$	Transmitter Differential Return loss	12			dB	
	RL_{TX-CM}	Transmitter Common Mode Return loss	6			dB	
	$Z_{TX-DEFF-DC}$	DC Differential TX impedance	80	100	120	Ω	
	Z_{OSE}	Single ended TX Impedance	40	50	60	Ω	
	Transmitter Eye Diagram	TX Eye Height (De-emphasized bits)	505	650		mV	
	Transmitter Eye Diagram	TX Eye Height (Transition bits)	800	950		mV	
	PCIe Receive						
	$V_{RX-DIFFp-p}$	Differential input voltage (peak-to-peak)	175		1200	mV	
	$V_{RX-CM-AC}$	Receiver common-mode voltage for AC coupling			150	mV	
	$RL_{RX-DIFF}$	Receiver Differential Return Loss	15			dB	
	RL_{RX-CM}	Receiver Common Mode Return Loss	6			dB	
	$Z_{RX-DIFF-DC}$	Differential input impedance (DC)	80	100	120	Ω	
	$Z_{RX-COMM-DC}$	Single-ended input impedance	40	50	60	Ω	
	$Z_{RX-COMM-HIGH-Z-DC}$	Powered down input common mode impedance (DC)	200k	350k		Ω	
	$V_{RX-IDLE-DET-DIFFp-p}$	Electrical idle detect threshold	65		175	mV	
PCIe REFCLK							
	C_{IN}	Input Capacitance	1.5	—		pF	

Table 16 DC Electrical Characteristics (Part 1 of 2)

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I/O Type	Parameter	Description	Min[1]	Typ[1]	Max[1]	Unit	Conditions
Other I/Os							
LOW Drive Output	I_{OL}		—	2.5	—	mA	V_{OL} = 0.4v
	I_{OH}		—	-5.5	—	mA	V_{OH} = 1.5V
High Drive Output	I_{OL}		—	12.0	—	mA	V_{OL} = 0.4v
	I_{OH}		—	-20.0	—	mA	V_{OH} = 1.5V
Schmitt Trigger Input (STI)	V_{IL}		-0.3	—	0.8	V	—
	V_{IH}		2.0	—	V_{DD}IO + 0.5	V	—
Input	V_{IL}		-0.3	—	0.8	V	—
	V_{IH}		2.0	—	V_{DD}IO + 0.5	V	—
Capacitance	C_{IN}		—	—	8.5	pF	—
Leakage	Inputs		—	—	± 10	µA	V_{DD}I/O (max)
	$I/O_{LEAK\ W/O}$ Pull-ups/downs		—	—	± 10	µA	V_{DD}I/O (max)
	$I/O_{LEAK\ WITH}$ Pull-ups/downs		—	—	± 80	µA	V_{DD}I/O (max)

Table 16 DC Electrical Characteristics (Part 2 of 2)

1. Minimum, Typical, and Maximum values meet the requirements under PCI Specification 1.0a.

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Package Pinout — 324-BGA Signal Pinout for PES12NT3

The following table lists the pin numbers and signal names for the PES12NT3 device.

Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt
A1	V_{SS}		E10	V_{DD}PE		K1	V_{DD}CORE		P10	V_{DD}IO	
A2	V_{SS}		E11	V_{SS}		K2	V_{SS}		P11	V_{DD}IO	
A3	PEARP03		E12	V_{DD}PE		K3	V_{TT}PE		P12	V_{DD}IO	
A4	V_{DD}CORE		E13	V_{SS}		K4	V_{DD}CORE		P13	V_{DD}IO	
A5	PEATN03		E14	V_{DD}CORE		K5	V_{DD}PE		P14	V_{DD}IO	
A6	V_{DD}CORE		E15	V_{DD}APE		K6	V_{SS}		P15	V_{SS}	
A7	PEATP02		E16	V_{SS}		K7	V_{SS}		P16	V_{TT}PE	
A8	V_{DD}CORE		E17	PECTP03		K8	V_{SS}		P17	V_{SS}	
A9	PEARN02		E18	PECTN03		K9	V_{SS}		P18	V_{DD}CORE	
A10	V_{DD}CORE		F1	V_{DD}CORE		K10	V_{SS}		R1	PEBTN03	
A11	PEARP01		F2	V_{SS}		K11	V_{SS}		R2	PEBTP03	
A12	V_{DD}CORE		F3	V_{DD}CORE		K12	V_{SS}		R3	V_{SS}	
A13	PEATP01		F4	V_{DD}APE		K13	V_{SS}		R4	V_{DD}IO	
A14	V_{DD}CORE		F5	V_{SS}		K14	V_{SS}		R5	V_{SS}	
A15	V_{DD}CORE		F6	V_{DD}CORE		K15	V_{DD}PE		R6	V_{DD}CORE	
A16	PEATN00		F7	V_{SS}		K16	V_{TT}PE		R7	MSMBDAT	
A17	V_{SS}		F8	V_{DD}CORE		K17	V_{SS}		R8	SSMBADDR_5	
A18	V_{SS}		F9	V_{SS}		K18	V_{DD}CORE		R9	PEALREV	
B1	V_{DD}CORE		F10	V_{DD}CORE		L1	PEBRN02		R10	SWMODE_2	
B2	V_{DD}CORE		F11	V_{SS}		L2	PEBRP02		R11	RSTHALT	
B3	PEARN03		F12	V_{SS}		L3	V_{SS}		R12	GPIO_04	1
B4	V_{SS}		F13	V_{DD}PE		L4	V_{DD}PE		R13	V_{DD}CORE	
B5	PEATP03		F14	V_{SS}		L5	V_{SS}		R14	V_{SS}	
B6	V_{SS}		F15	V_{DD}IO		L6	V_{DD}CORE		R15	V_{DD}IO	
B7	PEATN02		F16	V_{SS}		L7	V_{DD}CORE		R16	V_{SS}	
B8	V_{SS}		F17	V_{SS}		L8	V_{DD}CORE		R17	PECTP00	
B9	PEARP02		F18	V_{DD}CORE		L9	V_{DD}CORE		R18	PECTN00	
B10	V_{SS}		G1	PEBTP01		L10	V_{DD}CORE		T1	V_{DD}CORE	
B11	PEARN01		G2	PEBTN01		L11	V_{DD}CORE		T2	V_{SS}	
B12	V_{SS}		G3	V_{SS}		L12	V_{DD}CORE		T3	V_{SS}	
B13	PEATN01		G4	V_{DD}PE		L13	V_{DD}CORE		T4	JTAG_TCK	
B14	V_{SS}		G5	V_{DD}APE		L14	V_{SS}		T5	JTAG_TDO	
B15	V_{SS}		G6	V_{SS}		L15	V_{DD}PE		T6	MSMBADDR_1	
B16	PEATP00		G7	V_{SS}		L16	V_{SS}		T7	MSMBCLK	

Table 17 PES12NT3 324-pin Signal Pin-Out (Part 1 of 3)

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Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt
B17	V_{DD}CORE		G8	V_{DD}IO		L17	PECRP01		T8	SSMBADDR_2	
B18	V_{DD}CORE		G9	V_{SS}		L18	PECRN01		T9	CCLKDS	
C1	PEBRP00		G10	V_{DD}IO		M1	V_{DD}CORE		T10	SWMODE_1	
C2	PEBRN00		G11	V_{SS}		M2	V_{SS}		T11	PERSTN	
C3	V_{SS}		G12	V_{DD}CORE		M3	V_{SS}		T12	GPIO_03	1
C4	V_{DD}CORE		G13	V_{SS}		M4	V_{DD}APE		T13	GPIO_07	
C5	V_{SS}		G14	V_{DD}APE		M5	V_{SS}		T14	V_{SS}	
C6	V_{TT}PE		G15	V_{DD}PE		M6	V_{DD}CORE		T15	REFCLKM	
C7	V_{SS}		G16	V_{SS}		M7	V_{SS}		T16	V_{SS}	
C8	V_{TT}PE		G17	PECTN02		M8	V_{SS}		T17	V_{SS}	
C9	V_{SS}		G18	PECTP02		M9	V_{DD}CORE		T18	V_{DD}CORE	
C10	V_{TT}PE		H1	V_{DD}CORE		M10	V_{DD}CORE		U1	PEBRP03	
C11	V_{SS}		H2	V_{SS}		M11	V_{SS}		U2	PEBRN03	
C12	V_{TT}PE		H3	V_{TT}PE		M12	V_{SS}		U3	V_{SS}	
C13	V_{DD}CORE		H4	V_{DD}APE		M13	V_{DD}CORE		U4	JTAG_TDI	
C14	PEARP00		H5	V_{SS}		M14	V_{SS}		U5	JTAG_TMS	
C15	PEARN00		H6	V_{SS}		M15	V_{DD}APE		U6	MSMBADDR_2	
C16	V_{DD}CORE		H7	V_{DD}CORE		M16	V_{SS}		U7	MSMBADDR_4	
C17	PECRN03		H8	V_{SS}		M17	V_{SS}		U8	SSMBADDR_3	
C18	PECRP03		H9	V_{DD}CORE		M18	V_{DD}CORE		U9	CCLKUS	
D1	V_{DD}CORE		H10	V_{DD}CORE		N1	PEBTP02		U10	SWMODE_0	
D2	V_{SS}		H11	V_{SS}		N2	PEBTN02		U11	PECLREV	
D3	V_{SS}		H12	V_{DD}CORE		N3	V_{TT}PE		U12	GPIO_00	
D4	V_{DD}CORE		H13	V_{SS}		N4	V_{DD}APE		U13	GPIO_02	1
D5	V_{SS}		H14	V_{DD}APE		N5	V_{SS}		U14	GPIO_06	
D6	V_{DD}APE		H15	V_{DD}PE		N6	V_{SS}		U15	MSMBSMODE	
D7	V_{SS}		H16	V_{TT}PE		N7	V_{SS}		U16	V_{SS}	
D8	V_{DD}APE		H17	V_{SS}		N8	V_{SS}		U17	PECRN00	
D9	V_{SS}		H18	V_{DD}CORE		N9	V_{SS}		U18	PECRP00	
D10	V_{DD}APE		J1	PEBRP01		N10	V_{SS}		V1	V_{DD}CORE	
D11	V_{SS}		J2	PEBRN01		N11	V_{SS}		V2	V_{SS}	
D12	V_{DD}APE		J3	V_{SS}		N12	V_{SS}		V3	PEREFCLKP0	
D13	V_{SS}		J4	V_{DD}PE		N13	V_{SS}		V4	PEREFCLKN0	
D14	V_{DD}CORE		J5	V_{SS}		N14	V_{SS}		V5	JTAG_TRST_N	
D15	V_{SS}		J6	V_{DD}CORE		N15	V_{DD}APE		V6	MSMBADDR_3	
D16	V_{SS}		J7	V_{SS}		N16	V_{TT}PE		V7	SSMBADDR_1	
D17	V_{SS}		J8	V_{SS}		N17	PECTN01		V8	SSMBCLK	

Table 17 PES12NT3 324-pin Signal Pin-Out (Part 2 of 3)

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Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt
D18	V_{DD}CORE		J9	V_{DD}CORE		N18	PECTP01		V9	SSMBDAT	
E1	PEBTN00		J10	V_{DD}CORE		P1	V_{DD}CORE		V10	PEBLREV	
E2	PEBTP00		J11	V_{SS}		P2	V_{SS}		V11	SWMODE_3	
E3	V_{DD}CORE		J12	V_{SS}		P3	V_{TT}PE		V12	PENTBRSTN	
E4	V_{SS}		J13	V_{DD}CORE		P4	V_{SS}		V13	GPIO_01	
E5	V_{DD}CORE		J14	V_{SS}		P5	V_{DD}IO		V14	GPIO_05	1
E6	V_{SS}		J15	V_{DD}CORE		P6	V_{DD}IO		V15	PEREFCLKP1	
E7	V_{SS}		J16	V_{SS}		P7	V_{DD}IO		V16	PEREFCLKN1	
E8	V_{DD}PE		J17	PECRP02		P8	V_{DD}IO		V17	V_{SS}	
E9	V_{SS}		J18	PECRN02		P9	V_{DD}IO		V18	V_{DD}CORE	

Table 17 PES12NT3 324-pin Signal Pin-Out (Part 3 of 3)

Alternate Signal Functions

Pin	GPIO	Alternate
U13	GPIO[2]	IOEXPINTN
T12	GPIO[3]	PAABN
R12	GPIO[4]	PAAIN
V14	GPIO[5]	PAPIN

Table 18 PES12NT3 Alternate Signal Functions

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Power Pins

V_{DD}Core	V_{DD}Core	V_{DD}Core	V_{DD}IO	V_{DD}PE	V_{DD}APE	V_{TT}PE
A4	F3	L8	F15	E8	D6	C6
A6	F6	L9	G8	E10	D8	C8
A8	F8	L10	G10	E12	D10	C10
A10	F10	L11	P5	F13	D12	C12
A12	F18	L12	P6	G4	E15	H3
A14	G12	L13	P7	G15	F4	H16
A15	H1	M1	P8	H15	G5	K3
B1	H7	M6	P9	J4	G14	K16
B2	H9	M9	P10	K5	H4	N3
B17	H10	M10	P11	K15	H14	N16
B18	H12	M13	P12	L4	M4	P3
C4	H18	M18	P13	L15	M15	P16
C13	J6	P1	P14		N4	
C16	J9	P18	R4		N15	
D1	J10	R6	R15			
D4	J13	R13				
D14	J15	T1				
D18	K1	T18				
E3	K4	V1				
E5	K18	V18				
E14	L6					
F1	L7					

Table 19 PES12NT3 Power Pins

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Ground Pins

V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}
A1	D16	G16	K13	N12
A2	D17	H2	K14	N13
A17	E4	H5	K17	N14
A18	E6	H6	L3	P2
B4	E7	H8	L5	P4
B6	E9	H11	L14	P15
B8	E11	H13	L16	P17
B10	E13	H17	M2	R3
B12	E16	J3	M3	R5
B14	F2	J5	M5	R14
B15	F5	J7	M7	R16
C3	F7	J8	M8	T2
C5	F9	J11	M11	T3
C7	F11	J12	M12	T14
C9	F12	J14	M14	T16
C11	F14	J16	M16	T17
D2	F16	K2	M17	U3
D3	F17	K6	N5	U16
D5	G3	K7	N6	V2
D7	G6	K8	N7	V17
D9	G7	K9	N8	
D11	G9	K10	N9	
D13	G11	K11	N10	
D15	G13	K12	N11	

Table 20 PES12NT3 Ground Pins

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Signals Listed Alphabetically

Signal Name	I/O Type	Location	Signal Category
CCLKDS	I	T9	System
CCLKUS	I	U9	
GPIO_00	I/O	U12	General Purpose Input/Output
GPIO_01	I/O	V13	
GPIO_02	I/O	U13	
GPIO_03	I/O	T12	
GPIO_04	I/O	R12	
GPIO_05	I/O	V14	
GPIO_06	I/O	U14	
GPIO_07	I/O	T13	
JTAG_TCK	I	T4	JTAG
JTAG_TDI	I	U4	
JTAG_TDO	O	T5	
JTAG_TMS	I	U5	
JTAG_TRST_N	I	V5	
MSMBADDR_1	I	T6	SMBus
MSMBADDR_2	I	U6	
MSMBADDR_3	I	V6	
MSMBADDR_4	I	U7	
MSMBCLK	I/O	T7	
MSMBDAT	I/O	R7	
MSMBSMODE	I	U15	System
PEALREV	I	R9	PCI Express
PEARN00	I	C15	
PEARN01	I	B11	
PEARN02	I	A9	
PEARN03	I	B3	
PEARP00	I	C14	
PEARP01	I	A11	
PEARP02	I	B9	
PEARP03	I	A3	
PEATN00	O	A16	
PEATN01	O	B13	
PEATN02	O	B7	

Table 21 PES12NT3 Alphabetical Signal List (Part 1 of 3)

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Signal Name	I/O Type	Location	Signal Category
PEATN03	O	A5	PCI Express
PEATP00	O	B16	
PEATP01	O	A13	
PEATP02	O	A7	
PEATP03	O	B5	
PEBLREV	I	V10	
PEBRN00	I	C2	
PEBRN01	I	J2	
PEBRN02	I	L1	
PEBRN03	I	U2	
PEBRP00	I	C1	
PEBRP01	I	J1	
PEBRP02	I	L2	
PEBRP03	I	U1	
PEBTN00	O	E1	
PEBTN01	O	G2	
PEBTN02	O	N2	
PEBTN03	O	R1	
PEBTP00	O	E2	
PEBTP01	O	G1	
PEBTP02	O	N1	
PEBTP03	O	R2	
PECLREV	I	U11	
PECRN00	I	U17	
PECRN01	I	L18	
PECRN02	I	J18	
PECRN03	I	C17	
PECRP00	I	U18	
PECRP01	I	L17	
PECRP02	I	J17	
PECRP03	I	C18	
PECTN00	O	R18	
PECTN01	O	N17	
PECTN02	O	G17	
PECTN03	O	E18	
PECTP00	O	R17	

Table 21 PES12NT3 Alphabetical Signal List (Part 2 of 3)

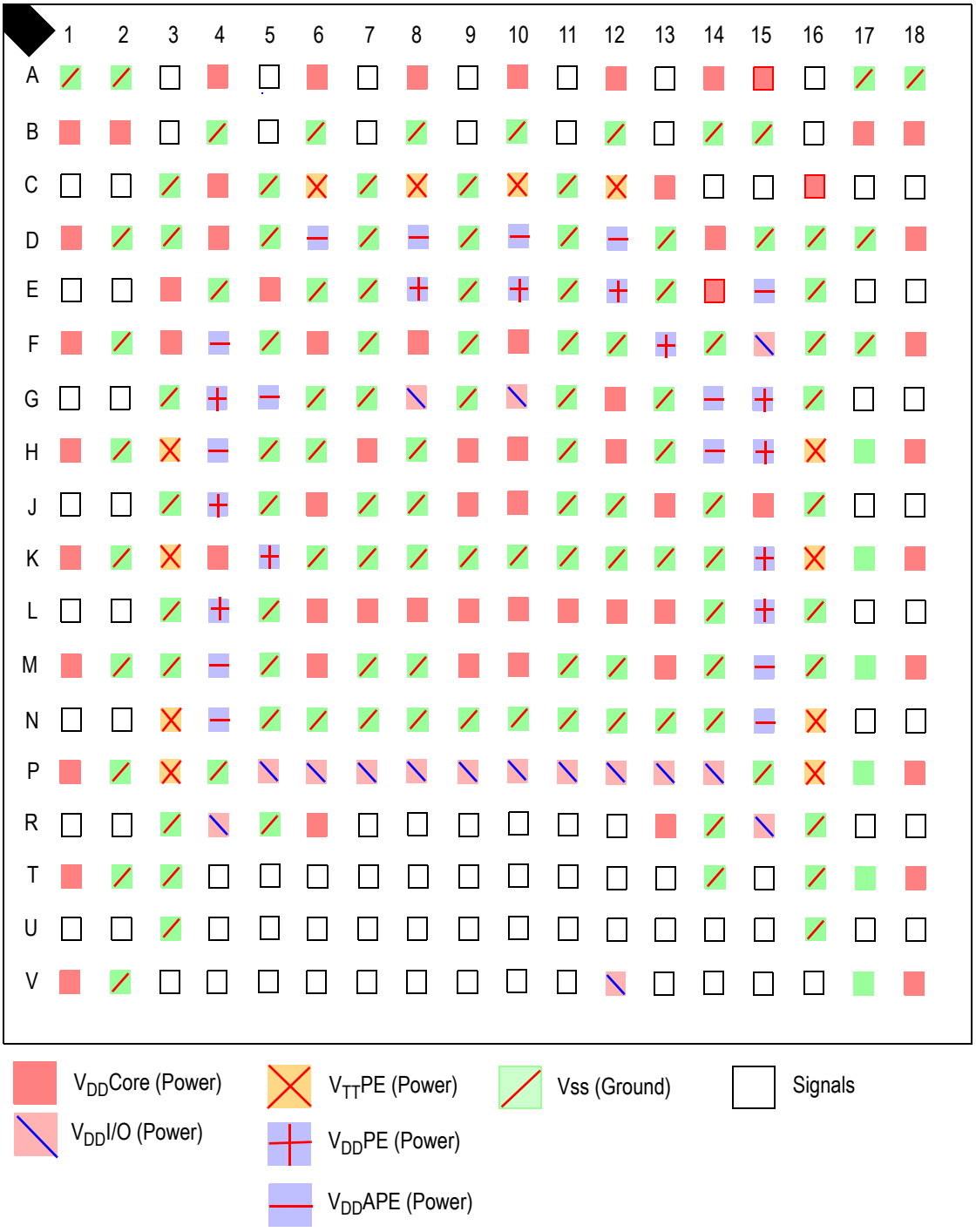
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Signal Name	I/O Type	Location	Signal Category
PECTP01	O	N18	PCI Express
PECTP02	O	G18	
PECTP03	O	E17	
PENTBRSTN	I	V12	System
PEREFCLKN0	I	V4	PCI Express
PEREFCLKN1	I	V16	
PEREFCLKP0	I	V3	
PEREFCLKP1	I	V15	
PERSTN	I	T11	System
REFCLKM	I	T15	PCI Express
RSTHALT	I	R11	System
SSMBADDR_1	I	V7	SMBus
SSMBADDR_2	I	T8	
SSMBADDR_3	I	U8	
SSMBADDR_5	I	R8	
SSMBCLK	I/O	V8	SMBus
SSMBDAT	I/O	V9	
SWMODE_0	I	U10	System
SWMODE_1	I	T10	
SWMODE_2	I	R10	
SWMODE_3	I	V11	System
V_{DD}CORE, V_{DD}APE, V_{DD}IO, V_{DD}PE, V_{TT}PE	See Table 19 for a listing of power pins.		
V_{SS}	See Table 20 for a listing of ground pins.		

Table 21 PES12NT3 Alphabetical Signal List (Part 3 of 3)

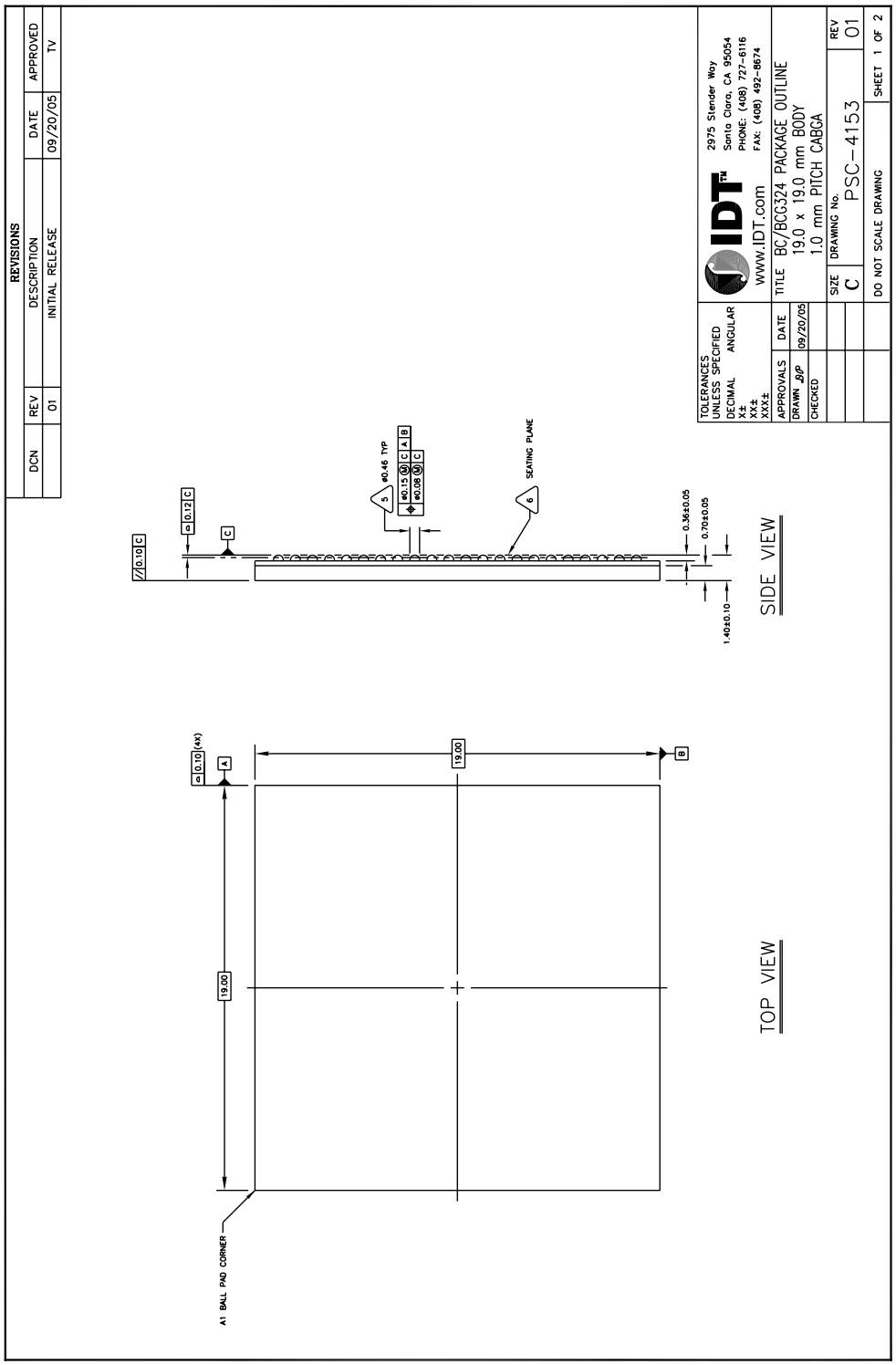
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PES12NT3 Pinout — Top View



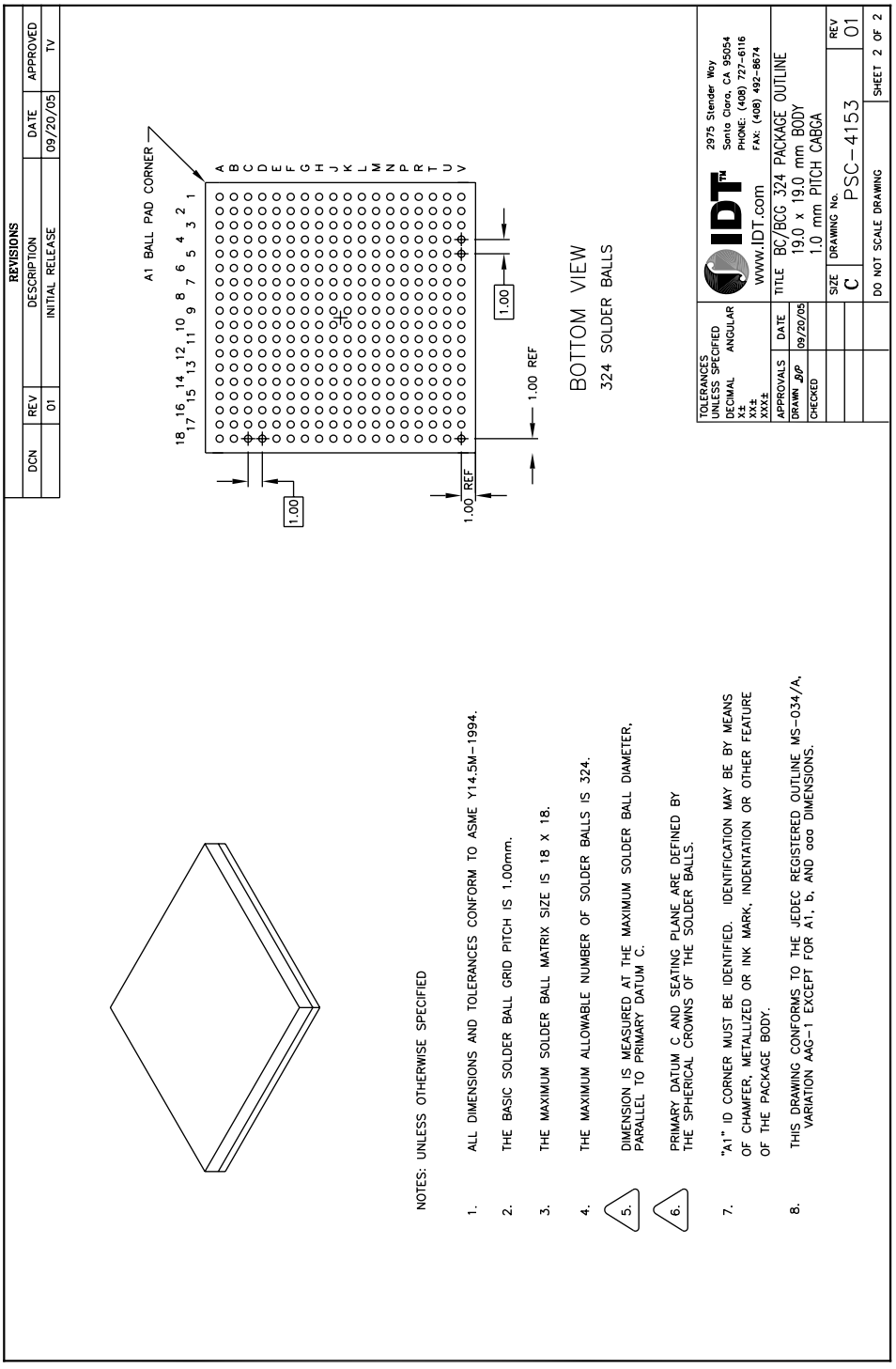
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PES12NT3 Package Drawing — 324-Pin BC324/BCG324



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PES12NT3 Package Drawing — Page Two



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Revision History

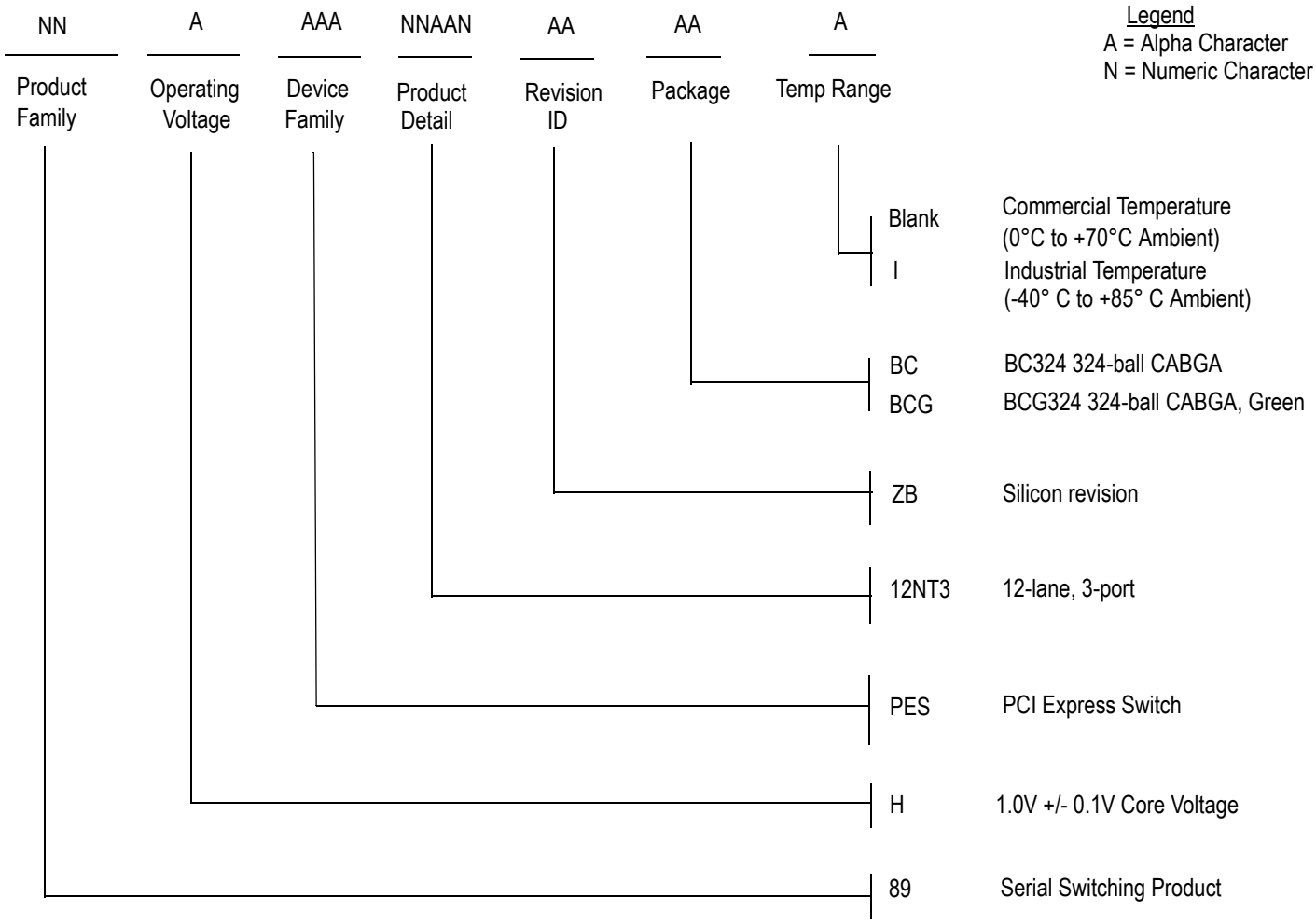
April 15, 2008: Initial publication of data sheet.

January 5, 2009: On the Ordering Information page, changed silicon revision from ZA to ZB.

February 19, 2009: Added industrial temperature to Table 13 and to Order page.

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Ordering Information



Valid Combinations

89HPES12NT3ZBBC	324-pin BC324 package, Commercial Temperature
89HPES12NT3ZBBCG	324-pin Green BC324 package, Commercial Temperature
89HPES12NT3ZBBCI	324-pin BC324 package, Industrial Temperature
89HPES12NT3ZBBCGI	324-pin Green BC324 package, Industrial Temperature

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